TMS320 DSP
DESIGNER'S NOTEBOOK

TMS320C40 DMA Memory Transfer Timing

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TEXAS INSTRUMENTS

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TMS320C40 DMA Memory Transfer Timing

Abstract

This document discusses how many cycles it takes the DMA to read/write to external memory. Several tables are given to allow the developer to determine this information for several different types of configurations.

Design Problem

How many cycles does it take the DMA to read/write to external memory?

Solution

To maximize CPU computational power and unload the CPU of the data transfer burden, the TMS320C40 provides six DMA channels (12 DMA channels in split mode) to handle data transfer concurrently with CPU operations. These DMA channels and the CPU share the internal/external buses. Hence, a user-configurable DMA fixed/rotate priority arbitration scheme and CPU/DMA priority scheme are created to prioritize the bus resource conflict situations (see TMS320C4x User's Guide, Section 9 for more information).

The combination of bus resource conflicts can make DMA memory transfer timing very complicated. However, there are certain guidelines to follow to calculate the transfer timing for certain DMA setups. The single-channel DMA memory transfer timing with no CPU or other DMA channel conflict is discussed below. The actual DMA transfer timing can be obtained by combining the single-channel DMA transfer timing with bus resource conflict situations.

When the DMA memory transfer has no conflict with the CPU or any other DMA channels, the number of cycles of a DMA transfer is dependent upon whether the source and destination location are designated as on-chip memory, peripheral, or external ports. When an external port is used, the DMA transfer speed is affected by two factors: the external bus wait state and the read/write conflict (i.e., if a write is followed by a read, the read takes two cycles).

Tables 1 through 3 show the number of cycles a DMA transfer requires from different sources to different destinations. Each entry in the table represents the total cycles required to do the T transfers, assuming that there are no pipeline conflicts.

Each table below illustrates the timing of the DMA transfer.

Table 1. Timing and Cycle Count for DMA Transfers – Destination: On-Chip

Cycles (H1)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Source On-chip Destination On-chip	R	W	R	W	R	W	R	W	R	W	R	W	R	W	R
Source Local Bus Destination On-chip	R	R Cr	R Cr	W	R	R Cr	R Cr	W	R	R Cr	R Cr	W	R	R Cr	R Cr
Source Global Bus Destination On-chip		R	R Cr	R Cr W	R	R Cr	R Cr	W	R	R Cr	R Cr	W	R	R Cr	R Cr

Source	Destination: On-chip
On-chip	(1+1) T
Local Bus	[(1 + Cr) + 1] T
Global bus	[(1 + Cr) + 1] T

Notes: 1) T = Number of transfers
2) Cr = Source-read wait states
3) Cw = Destination-write wait states
4) |R| = Single-cycle reads
5) |W| = Single-cycle writes
6) |R.R| = Multi-cycle reads
7) |W.W| = Multi-cycle writes
8) |Cr| = Number of wait cycles for a read
9) |Cw| = Number of wait cycles for a write

Externally, on the global and local buses, writes take at least two cycles. However, the CPU/DMA requires one cycle to perform the write to the external memory bus. Therefore the DMA/ CPU can transfer data on the next cycle. For example, the DMA transfers 1024 words from internal memory RAM block 1 to one-wait-state memory on the global bus while the CPU runs from memory on the local bus and fetches operands from RAM block 0. DMA transfer time is calculated from Table 2 as 1 + (2 + 1) 1024 = 1 + 3072 = 3073 cycles.

Table 2. Timing and Cycle Count for DMA Transfers – Destination: Local Bus

Cycles (H1)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Source On-chip	R		R				R				R				R
Destination Local Bus		W	W	W Cw	W Cw	W	W	W Cw	W Cw	W	W	W Cw	W Cw	W	W
Source Local Bus	R	R Cr	R Cr					R	R	R Cr	R Cr				
Destination Local Bus				W	W	W Cw	W Cw					W	W	W Cw	W Cw
Source Global Bus	R	R Cr	R Cr		R	R Cr	R Cr		R	R Cr	R Cr		R		
Destination Local Bus				W	W	W Cw	W Cw	W	W	W Cw	W Cw	W	W	W Cw	W Cw

Source	Destination: Local Bus
On-chip	1 + (2 + Cw) T
Local Bus	[(2 + Cr) + (2 + Cw)] T – 1
Global bus	[(1 + Cr) + (2 + Cw)] + [2 + max(Cr, Cw)] (T – 1)

Table 3. Timing and Cycle Count for DMA Transfers – Destination: Global Bus

Cycles (H1)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Source On-chip	R		R				R			R					R
Destination Global Bus		W	W	W Cw	W Cw	W	W	W Cw	W Cw	W	W	W Cw	W Cw	W	W
Source Local Bus	R	R Cr	R Cr		R	R Cr	R Cr		R	R Cr	R Cr		R		
Destination Global Bus				W	W	W Cw	W	W	W	W	W	W	W	W Cw	W
Source Global Bus		R Cr	R Cr					R	R	R Cr	R Cr				
Destination Global Bus				W	W	W Cw	W Cw					W	W	W Cw	W Cw

Source	Destination: Global Bus
On-chip	1 + (2 + Cw) T
Local Bus	[(1 + Cr) + (2 + Cw)] + [2 + max(Cr, Cw)] (T –1)
Global bus	[(2 + Cr) + (2 + Cw)] T – 1