Designing Low-Power Applications with the TMS320LC54x

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Designing Low-Power Applications with the TMS320LC54x

Abstract

This technical brief is an overview of the low power architectural features and design considerations of the TMS320LC54x DSP (Digital Signal Processor) family. For those with a deeper interest in low-power DSP design, this technical brief also provides an overview of a more detailed application brief titled, *Calculation of TMS320C54x Power Dissipation*, TI literature number SPRA164. The audience for this and the above referenced paper are designers of portable, power-sensitive, and battery-operated applications such as digital cellular telephones, laptop modems, and voice-mail pagers.

Introduction

TI is the DSP of choice in low-power applications. One out of every two digital cellular phones shipped in the world has a TI DSP. This includes industry leaders like Nokia and Ericsson who rely on TI for their DSP solutions.

TI research and development in Dallas recently demonstrated the operation of a 1V DSP based off the C54x core. That is another reason why designers of low-power end-equipments look to TI, for their design solutions. With the C54x core, TI currently offers world-class, low-power, high-performance DSP solutions, and continued aggressive improvements in both power consumption and processing power are planned for the future. This is just one reason why TI is the leader in DSP Solutions.

This technical brief provides insight in the following areas:

- **Architectural Features of a Low-Power Design** - Describes key TMS320LC54x features designed to minimize power usage yet provide high performance.
- **System Design Considerations** - Summary of key areas critical to designing low-power applications.
- **Total Power Dissipation** - Overview of what the designer must consider when predicting power usage.
- **TMS320LC54x Road Map** - The future of TI low-power DSPs.
- **Summary of *Calculation of TMS320C54x Power Dissipation* Application Report** - For designers needing specific information on techniques for analyzing system and device conditions to determine operating current levels and device thermal management requirements.

Architectural Features of a Low-Power Design

The TMS320C54x devices are a family of 16-bit fixed-point processors with enhanced processing capabilities over the previous fixed-point family of DSPs. Architecture, design, and process enhancements have produced a generation of processors which provide high performance while maintaining low power dissipation.

The TMS320C54x family of DSPs is capable of processing speeds as high as 100 million instructions per second (MIPS), sufficient to handle a wide variety of high-performance applications. In addition, the device is designed to exhibit very low power dissipation, and features flexible power management features which allow further reduction in power requirements.

These characteristics make the TMS320C54x devices uniquely well-suited to portable power-sensitive and battery-operated applications such as digital cellular telephones, laptop modems, voicemail pagers, etc.

Here are the key power-management features of the TMS320C54x:

- **CMOS technology** yields typical active current requirements of 0.45 mA per MIPS for 2.5-volt operation. The static CMOS technology used in fabrication of the TMS320C54x family of devices combines high density with low power dissipation. Because CMOS devices ideally draw current only when switching, this technology offers the potential for fully static devices with standby modes exhibiting very low current drain.
- **Flexible low-power modes** (IDLE instructions) conserve power by halting sections of the device when their use is not required. Operation of the CPU, the on-chip peripherals, and the clock generation circuitry can be halted independently. See Table 1 below for an overview of the low-power modes.
- **CLKOUT switching** allows the external CLKOUT signal to be stopped providing power savings when external clock synchronization is not necessary.
- **Bus holder circuitry** integrated into the device prevents floating buses, eliminating the need for power-wasting external pull-up resistors.

Table 1. TMS320LC54x Activity During Low-Power Modes

Mode	CPU	PLL	Timer	Standard Serial Ports	Buffered Serial port	Host Port Interface	CLKOUT
Normal	•	•	•	•	•	•	•
IDLE1		•	•	•	•	•	•
Hold		•	•	•	•	•	•
IDLE2		•			•	•	
IDLE3					•†	•†	
Stop					•†	•†	

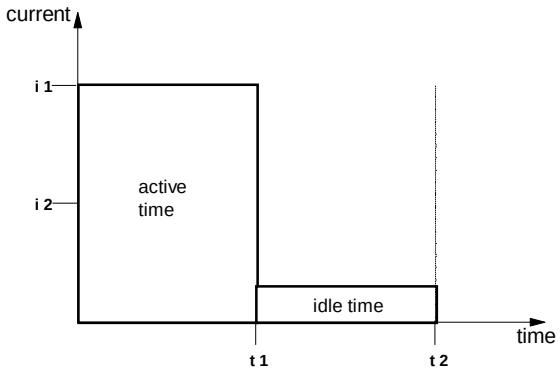
† - under special conditions

System Design Considerations for Minimizing Power Dissipation

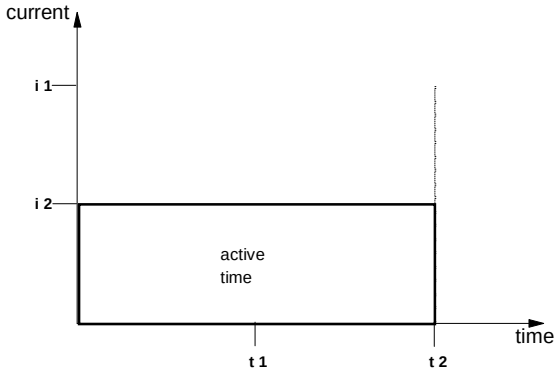
There are several issues that can be considered in the design process to reduce power consumption of a particular TMS320LC54x application:

- **Internal CPU Activity** - The power use of the TMS320LC54x devices is directly related to the level of CPU activity. Many factors affect the CPU current use including the instruction complexity (the amount of parallel operation being performed by the instruction), the utilization of the internal buses (including the data patterns on the buses), and the effects of using repeat option on instructions.
- **System Clock and Switching Rates -** The power consumption of the TMS320LC54x device is directly proportional to the system clock (CLKOUT) switching speed. If the clock speed doubles, the current will double. See Figure 1 below.

Figure 1. Algorithm current use vs. clock speed



(a) (Twice as fast as clock b below)



(b)

- **On-chip vs. Off-chip Memory** - On-chip memory requires less power because the external memory interface is not driven during internal accesses.
- **On-chip ROM vs. on-chip RAM -** Use of internal ROM requires less power than use of internal RAM. Code execution from internal ROM requires about 10% less CPU current than the same code executing from internal SARAM.
- **Capacitive Loading of Outputs -** Increased capacitive loading on device outputs increases the current required to drive the output pins. Minimizing this loading will minimize the current required to operate these pins.
- **Address Visibility -** When address visibility is enabled, addresses are passed to the external address bus even during internal memory accesses. This feature is very useful primarily as a development and debugging tool, but it should be disabled when debugging is complete.

- **DC Loading of Outputs -** DC loading of outputs due to TTL or other sources should be minimized to conserve power.
- **Power-down Mode -** When device CPU activity is not necessary, the device should be placed in one of the IDLE modes to conserve power. See the TMS320LC54x Reference Set Volume 1 for more information.

Total Power Dissipation

The total power consumption of the device is the sum of the individual components. This total current value is determined as the total current supplied to the device through all of the V_{DD} inputs.

Below is a summary of the steps used to calculate overall device power consumption. For a more detailed explanation, refer to the detailed TI application report *Calculation of TMS320C54x Power Dissipation*:

1) **Algorithm Partitioning** - The algorithm under consideration should be broken into sections of unique device activity and the power requirements for these sections calculated separately. The sections can then be time-averaged to determine the overall device current requirement. This includes IDLE time as Figure 1 demonstrates.

2) **CPU Activity** - The current contribution due to CPU activity can be determined by examining the code and determining the time-averaged current for each algorithm partition.

3) **Memory Usage** - Scale the current calculated in step 2 based on memory usage. Use of on-chip memory requires less current than off-chip memory (because of the additional current due to the external memory interface). Running code from internal ROM requires less current than running from internal RAM.

4) **Peripherals** - Consider the additional current required by use of the timer, standard serial port, buffered serial port, and host port interface.

5) **Current Due to Outputs** - Consider the current required by the algorithm to operate the external address and data buses.

6) **Calculation of Average Current** - If power supply current is observed over the full duration of device activity, different segments of activity will exhibit different current levels for different lengths of time.

7) **Effects of Temperature and Supply Voltage on Device Operating Current** - Include the effects of these factors after the total device current has been calculated.

LC54x Road Map

One of the primary vectors for future DSP applications is that of low power. We see a wealth of portable devices such as cellular phones filtering into our everyday lives. Each, while demanding performance, also requires miserly power consumption for longer usage time between recharging. TI's low power vector in DSP enables many of today's applications as well as opening the door for tomorrow.

This can best be seen by looking at the C54x product roadmap presented below in Table 2.

Table 2. LC54x Low-Power, High-Performance Road Map

MIPS	Node (process)	When placed in production	mA/MIPS	Core Voltage	mW/MIPS
40	0.60um	1996	1.00	3.0	3.00
50	0.45um	1996	0.80	3.0	2.40
66	0.35um	1997	0.65	3.0	1.95
80	0.35um	1997	0.65	3.0	1.95
100	0.25um	1H98	0.45	2.5	1.13

The proven success in the C54x family of DSPs in low power devices is also being fanned out to other families. In the microcontroller realm where increased performance coupled with low power are driving the high end of that market, the LC203 is introducing low power DSPs to cost-sensitive applications, and as the C2xx product family continues to mature, more low-power members will be introduced.

Contents of Power Dissipation Application Report

For those with a deeper interest in low-power DSP design with the TMS320C54x, designers can download the detailed application brief titled, *Calculation of TMS320C54x Power Dissipation*, TI literature number SPRA164 from our web site (www.ti.com). This application report describes in detail, techniques for analyzing system and device conditions to determine operating current levels.

From this analysis, power dissipation can in turn be used to determine device thermal management requirements. This application report contains:

- Detailed power testing set-ups
- Instruction set power characteristics
- Bus switching power considerations
- Detailed device internal power considerations
- Device interface power considerations
- The relationship between clock speed and current use
- Specific suggestions for minimizing power usage
- Thermal management

Summary

By now it should be understood that the real-time processing of digital information is best handled by the engine designed specifically for the task, the DSP, a technology developed by Texas Instruments, Inc. Real-time, high-performance processing may seem like the antithesis of low power design, but it is not. The TMS320LC54x family of DSPs provides exceptionally high performance with much lower than expected power requirements. The future promises even faster, more efficient versions specifically optimized for portable, high-performance end equipment.