Application Report
SPRA522

How to Begin Development with the TMS320C6711 DSP

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Abstract

This application report describes how you can begin development now for the Texas Instruments (TI™) TMS320C6711 digital signal processor (DSP) systems. Because of the compatibility between TMS320C6000 generation devices, existing ‘C6000 software tools and development platforms can be used to develop code for the ‘C6711 and other future devices. This capability allows for systems to be up and running when silicon becomes available.

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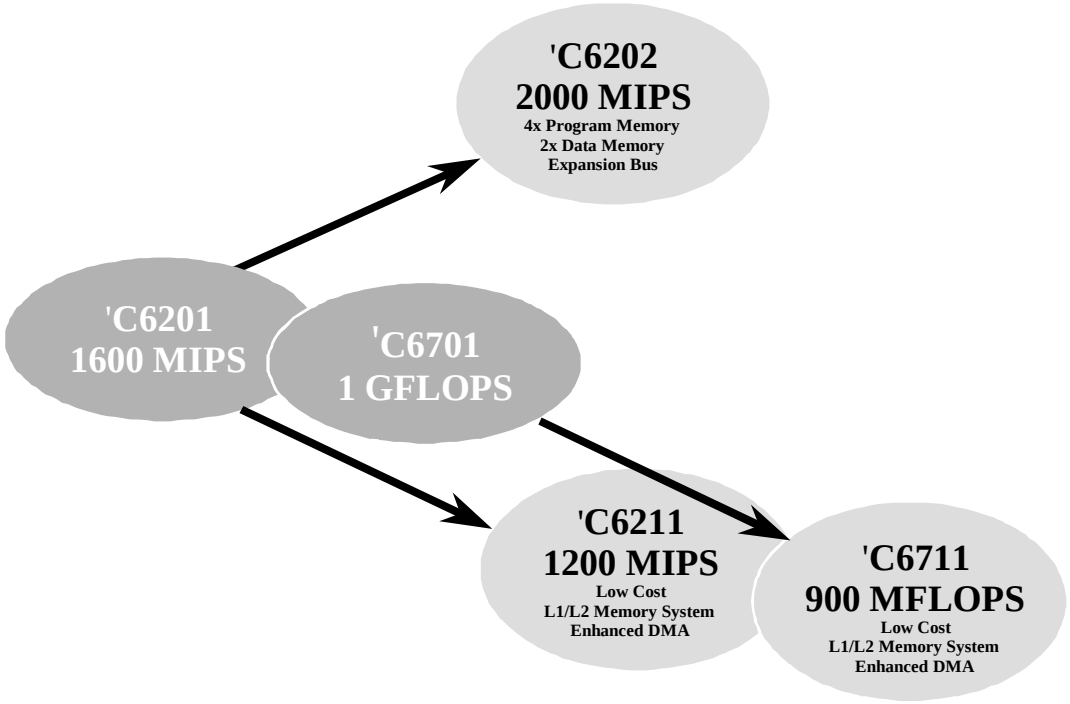
The Texas Instruments TMS320C6000 generation of high-performance DSPs now includes the TMS320C6711. The ‘C6711 is a low-cost version of the original ‘C6000 floating-point device, the ‘C6701. The ‘C6711 device will begin sampling in fourth quarter 1999, providing 900 MFLOPS (million floating-point operations per second) at 150MHz, with a lower cost version available at 100MHz.

Introduced in February 1997, the ‘C6000 generation is based on TI’s VelociTI™ architecture, an advanced very long instruction word (VLIW) architecture for DSPs. Figure 1 shows the roadmap for ‘C6000 platform.

Figure 1. TMS320C6000 Roadmap



TMS320C6000 Compatibility

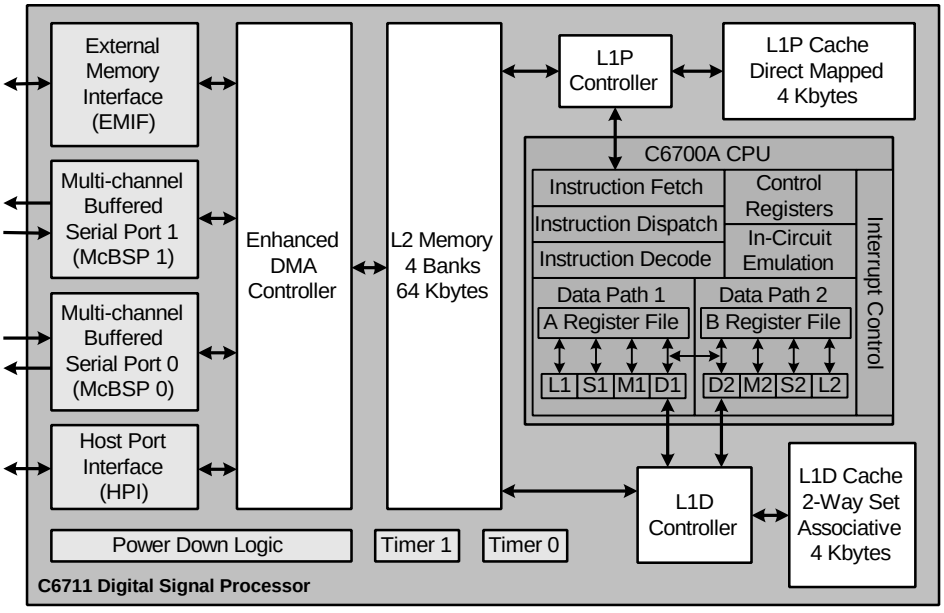
All ‘C6000 generation devices are code-compatible with one another, with the exception that there are some floating-point instructions that are only valid on the floating-point (‘C67x) members. All of the 'C67x devices are based on the same CPU designed to achieve high performance through increased instruction-level parallelism. Surpassing the throughput of traditional superscalar designs, VelociTI provides eight execution units, including two multipliers and six arithmetic logic units (ALUs). These units operate in parallel and can perform up to six floating-point instructions during a single clock cycle—up to 900 MFLOPS at 150MHz.

VelociTI's advanced features include instruction packing, conditional branching, and pre-fetched branching, all of which overcome problems that were associated with previous VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the 'C6000 compiler.

This common architecture allows designers to begin development with existing ‘C6000 software tools for those devices currently in development. This also allows for migration from one ‘C6000 processor to another, as design specifications require.

In addition to the CPU, many of the on-chip peripherals are common between ‘C6000 devices. Figure 2 shows a block diagram of the ‘C6711. Those blocks in dark gray are shared between the ‘C6701 and ‘C6711, those blocks in white are shared between the ‘C6211 and ‘C6711, and those blocks in light gray are shared between all ‘C6000 devices. The ‘C6711 is essentially a merger of the ‘C6701 and ‘C6211 processors.

Figure 2. TMS320C6711 DSP Block Diagram



Similarities between the ’C6711 and ’C6701 DSPs

The ‘C6711 is highly-compatible with the first ‘C67x device, the ‘C6701. The following device components are identical between the two devices:

- C6700 CPU
- Multi-channel Buffered Serial Ports (McBSPs)
- Host-Port Interface (HPI)
- 32-bit Timers
- Interrupt Selector

Differences between the ’C6711 and ’C6701 DSPs

The ‘C6711 is available at a significantly lower cost than the original ‘C6701, through the use of the ‘C6211 peripherals. These include:

- **Slower clock rate**: The maximum clock frequency has been decreased from 167 to 150MHz. This will still allow 900 MFLOPS during operation.
- **Cache memory architecture**: The ‘C6711 is a two-level cache-based device, with separate level-one program and data caches. These small, fast L1 caches are always active, and typically provide the CPU with a high (~98%) hit rate. The L2 is available for use as a level-two cache, as statically memory mapped SRAM space, or as a combination of the two.
- **Enhanced Direct Memory Access (EDMA) controller**: An enhanced DMA has been implemented on the ‘C6711 to provide more flexibility in programming data transfers.
- **External Memory Interface (EMIF)**: The EMIF has been enhanced to allow the device to interface to additional memory types. The ‘C6711 can interface to 8- and 16-bit wide SDRAM, SBSRAM, and asynchronous memory, in addition to the 32-bit wide memory interface capability provided by the ‘C6701. These narrower interfaces allow development of lower cost systems with a single 8- or 16-bit wide memory.

Differences between the ’C6711 and ’C6211 DSPs

There are only two difference between the ‘C6711 and ‘C6211:

- The ‘C6711 has a floating-point CPU, while the ‘C6211 is fixed-point.
- A 100MHz version of the ‘C6711 is available providing the lowest cost entry into the ‘C6000 platform.

Best Price/Performance

The cache architecture of the ‘C6711 allows for this device to be offered at a low cost, while keeping the high performance floating-point capabilities of the ’C6000 generation. By having an efficient on-chip cache, system designers may use slower, cheaper external memory devices for data and program storage without significantly impeding the performance of the device. In addition, a cache helps programmers to achieve their performance goals faster, shortening code development and accelerating time to market. The ‘C6711 was designed with TI’s low-power high-density TSC6000 ASIC Standard Cell library for low cost, while still providing 150MHz performance.

The enhanced direct memory access (EDMA) controller allows designers to optimize data organization in their systems. Capable of accessing any location in the ‘C6711 memory map, the EDMA controller transfers data in the background of CPU operation. The EDMA controller can handle multiple transfers simultaneously and can interleave bursts. The EDMA controller offers 16 independent channels, with a separate RAM space to hold additional transfer configurations. Each EDMA controller channel is synchronized by an event to allow minimal intervention by the CPU.

The on-chip memory is organized to allow design flexibility and ensure efficient memory usage. Like the ‘C6211, the ‘C6711 has 72 Kbytes of on-chip memory, with 8 Kbytes serving as a level-one (L1) cache that the CPU can directly access. The L1 cache is divided into 4 Kbytes of program (L1P) and 4 Kbytes of data (L1D) cache memory. The remaining 64 Kbytes of on-chip memory is a unified program and data memory space. It can serve as a level-two (L2) cache, be directly mapped as internal memory, or serve as a combination of these functions.

L1P is direct-mapped, so that each instruction byte occupies a unique location in the cache. It has a 256-bit wide data path to the CPU, so that the CPU may fetch eight instructions (one fetch packet) every cycle.

L1D is two-way set associative, so that it can hold two different sets of information with independent address ranges. The L1D cache is a dual-ported memory that allows simultaneous accesses from both CPU data ports, so that the CPU can load or store two 32-bit values in a single L1D data cycle. The cache uses a least-recently-used (LRU) replacement scheme to select between the two possible cache locations on a cache miss.

The L2 memory is divided into four 8-Kbyte banks, each of which can be programmed as a cache or RAM space. Each bank selected as cache adds one way of associativity, allowing the L2 cache to be 1-, 2-, 3-, or 4-way associative. Banks of L2 that are selected as cache are not included in the ‘C6711 memory map. The mapability of L2 blocks as addressable locations allows critical code and data to be locked into internal memory.

TI has run extensive tests on this L1/L2 architecture to determine how it performs with an enhanced full-rate GSM vocoder, system-level applications in ADSL, V.90 modems, and other commonly used algorithms. For both data and program, TI's tests indicate L1 cache hit rates greater than 98 percent. In other words, only one instruction or data word in fifty needs to be fetched from L2 or external memory.

The high L1 hit rate, combined with the flexibility of L2 memory organization, means that this architecture can operate at more than 80 percent of the cycle performance of a more expensive device with an traditional memory organization where all system memory is on the chip. This high degree of efficiency allows systems such as DSL client modems to rely on inexpensive external memory for program and data storage, while at the same time performing high-speed number-crunching routines in real time.

Begin Writing Code for the ’C6711 Today

The identical CPUs in the ‘C6711 and ‘C6701 devices allow for code to be written for the ‘C6711 using existing ‘C6000 tools. ‘C6701 code will require no modification to use on the ‘C6711. All peripheral-specific code, with the exception of the EDMA controller, will also run unchanged on the ‘C6711.

The identical architectures of the ‘C6711 and ‘C6211 devices allow for many system-level issues to be resolved prior to obtaining ‘C6711 silicon. EDMA controller programming may be tested on the ‘C6211 and incorporated in with floating-point code that has been verified on a ‘C6701.

This high level of compatibility between the processors allows for system development to begin now. By taking advantage of the ‘C6000 software and hardware tools currently available, ‘C6711 systems can have a running start for when silicon becomes available.

The ‘C6000 compiler may be used for all members of the ‘C6000 device platform. Floating-point devices are object code compatible, so code written for the ‘C6701 may be used by the ‘C6711.

The ‘C6000 simulator may be used to provide a cycle-accurate account of device performance and provides a good environment to learn the ‘C6000 VLIW architecture. The ‘C6701 configuration of the simulator may be used to simulate device peripherals. ‘C6711 designs may be worked out in detail on the simulator prior to purchasing actual silicon, with cycle-accurate accounts of DMA and EMIF performance. The peripherals on the ‘C6711, with the exception of the EDMA controller, are identical to those modeled with the ‘C6701 configuration.

A ‘C6711 configuration is also available to model the cache performance of the device. Using this configuration, it is possible to optimize code structure and data organization to take advantage of the ‘C6711 cache structure. L1 cache misses to L2 are supported with 100% cycle accuracy. The ‘C6711 configuration will support the EMIF and L2 cache misses in third quarter 1999 and will support the EDMA controller in fourth quarter 1999.

For a development start in hardware, the ‘C6701 EVM may be used to understand the ‘C6000 functionality. In this environment, floating-point code can be debugged while running in real time. All of the peripherals on the ‘C6711 are identical to those of the ‘C6701, with the exception of the EDMA controller, so the EVM is a good tool to understand how to incorporate the peripherals into a real-time system. Applications running on the ‘C6701 EVM will not be 100% cycle accurate to a ‘C6711 system, due to the difference in the internal memory architecture, but the ‘C6711 will provide approximately the same performance as the ‘C6701 operating at 150MHz.

Applications written on a ‘C6211 will work with 100% cycle accuracy on the ‘C6711. The only hindrance will be that the ‘C6211 will not be able to execute floating-point code.

Using these development platforms, as well as the ‘C6000 literature currently available will enable ‘C6711 systems to be completed soon after ‘C6711 silicon is made available.

‘C6000 tools support

‘C6000 tools are available now for use in all ‘C6000 designs. ‘C6711 will be added to the development tools in early third quarter 1999. The ‘C6000 development tools available today for the ‘C6711 are:

- ‘C6000 Simulator Software
- ‘C6000 Optimizing C Compiler/Assembler
- TMS320C6201 Multi-channel Evaluation Module (McEVM)
- TMS320C6701 Evaluation Module (EVM)
- XDS510 ‘C6000 C Source Debugger Software
- XDS510 Emulator Hardware with JTAG Emulation Cable

‘C6000 literature available

A great deal of literature is available today for the ‘C6000 devices.

- TMS320C6000 CPU and Instruction Set Reference Guide
- TMS320C6000 Peripherals Reference Guide
- TMS320C6000 Technical Brief
- TMS320C6000 Programmer’s Guide
- TMS320C6000 Evaluation Module Reference Guide
- TMS320C6000 Peripheral Support Library Programmer’s Reference
- TMS320C6000 Assembly Language Tools User’s Guide
- TMS320C6000 Optimizing C Compiler User’s Guide
- TMS320C6000 C Source Debugger User’s Guide
- TMS320C6000 C Source Debugger For SPARCstation’s

Many application notes also exist for assistance with ‘C6711 applications.

- Bit-Reverse/Digit-Reverse: Linear-Time Small Lookup Table Implementation-C6000
- Guidelines For Software Development Efficiency On the TMS320C6000 VelociTI Architecture
- Implementation Of G.726 ADPCM On TMS320C62XX DSP
- Implementing V.32BIS VITERBI Decoding on the TMS320C62XX DSP
- Performance Analysis of Line Echo Cancellation Implementation Using TMS320C6201

- TMS320C6201 Power Supply
- TMS320C6201 System Clock Circuit Example
- TMS320C6X EMIF to External SDRAM/SGRAM Interface
- TMS320C6X Manufacturing With the BGA Package
- TMS320C6X Reset Circuit
- TMS320C6X Thermal Design Considerations
- Using the TMS320C6X McBSP as a High Speed Communication Port

See http://www.ti.com/sc/docs/dsps/products/c6000/index.htm for more information.

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