Comparison of the TMS320C55x DSP EMIF and the TMS320C6000 DSP EMIF

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ABSTRACT

This document compares the features of the TMS320C55x™ DSP external memory interface (EMIF) and the TMS320C6000™ DSP EMIF. Both interfaces support asynchronous memory, synchronous burst static random access memory (SBSRAM), and synchronous dynamic random access memory (SDRAM).

This application note is not a complete reference of the features of these EMIFs. For full details, see *TMS320C55x DSP Peripherals Reference Guide* (SPRU317) and *TMS320C6000 Peripherals Reference Guide* (SPRU190).

Overview

The TMS320C55x™ DSP and the TMS320C6000™ DSP have similar external memory interfaces (EMIFs). Both EMIFs provide support for synchronous dynamic random access memory (SDRAM), synchronous burst static random access memory (SBSRAM), and asynchronous memories (ROM, RAM, and flash). This application report lists the EMIF differences in the following C55x™ DSPs and C6000™ DSPs:

- TMS320VC5510 DSP
- TMS320C6201 DSP
- TMS320C6202 DSP
- TMS320C6211 DSP
- TMS320C6701 DSP
- TMS320C6711 DSP

C55x™ DSP and C6000™ DSP EMIF Differences

Table 1 provides a cross reference of the EMIF features supported on the DSPs. The table provides separate sections for clock, SDRAM, SBSRAM, asynchronous, and miscellaneous features. S, W, and P in the miscellaneous section are synchronous, write performance, and power savings.

Table 1. EMIF Features Supported on C55x DSPs and C6000 DSPs

C55x DSP or C6000 DSP Device	EMIF Features																																
	Clock				SDRAM														SBSRAM						Asynch.					Misc.				
	C1	C2	C3	C4	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	B1	B2	B3	B4	B5	B6	A1	A2	A3	A4	A5	S1	W1	P1		
VC5510	X	X	X			X	X		X	X			X		X		X	X			X	X		X	X	X	X	X	X	X	X		
C6201/C6701	X	X	X	X			X	X	X				X		X		X	X			X	X		X	X	X	X	X	X		X		
C6202		X	X				X	X	X				X		X		X	X			X	X		X	X	X	X	X			X		
C6211/C6711	X	X			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			X		

Table 2 describes the EMIF features on C55x DSPs and C6000 DSPs. The order of the feature sections in Table 2 matches the order of features provided in Table 1.

Table 2. Description of EMIF Features on C55x DSPs and C6000 DSPs

Feature		Description	Supported on Devices	
			C55x DSP	C6000 DSP
Clocks				
C1	Synchronous memory clock at 1X DSP	SDRAM/SBSRAM clock at a DSP CPU clock frequency multiple of 1X	VC5510	6201(SBSRAM) 6701(SBSRAM 6211(external) 6711(external)
C2	Synchronous memory clock at 1/2X DSP	SDRAM/SBSRAM clock at a DSP CPU clock frequency multiple of 1/2X	VC5510	6201, 6701, 6202, 6211(external), 6711(external)
C3	Synchronous memory clock output disable	Enable/disable of synchronous memory clock output	VC5510	6201, 6701, 6202
C4	Separate clocks for SBS/SDRAM	SBSRAM and SDRAM have separate synchronous memory clock outputs.	None	6201, 6701
SDRAM				
D1	256-Mbit SDRAM	SDRAM 256M-bit memory size supported	None	6211, 6711
D2	128-Mbit SDRAM	SDRAM 128M-bit memory size supported	VC5510	6211, 6711
D3	64-Mbit SDRAM	SDRAM 64M-bit memory size supported	VC5510	All
D4	16-Mbit SDRAM	SDRAM 16M-bit memory size supported	None	All
D5	32-bit SDRAM	SDRAM data bus interface width of 32 bits	VC5510	All
D6	16-bit SDRAM	SDRAM data bus interface width of 16 bits	VC5510	6211, 6711
D7	8-bit SDRAM	SDRAM data bus interface width of 8 bits	None	6211, 6711
D8	SDRAM CAS latency 2	SDRAM read latency of 2 memory clock cycles	None	6211, 6711
D9	SDRAM CAS latency 3	SDRAM read latency of 3 memory clock cycles	VC5510	All
DA	SDRAM serial burst length 4	SDRAM serial (sequential) burst length of 4 locations	None	6211, 6711

Table 2. Description of EMIF Features on C55x DSPs and C6000 DSPs (Continued)

Feature		Description	Supported on Devices	
			C55XX	6XXX
SDRAM (Continued)				
DB	SDRAM serial burst length 1	SDRAM serial (sequential) burst length of 1 location	VC5510	All
DC	SDRAM multiple pages open	Multiple SDRAM pages simultaneously open	None	6211, 6711
DD	SDRAM timing configuration	SDRAM timing parameters programmability	VC5510	All
SBSRAM				
B1	32-bit SBSRAM	Non-parity SBSRAM data bus width of 32 bits	VC5510	All
B2	16-bit SBSRAM	Non-parity SBSRAM data bus width of 16 bits	None	6211, 6711
B3	8-bit SBSRAM	Non-parity SBSRAM data bus width of 8 bits	None	6211, 6711
B4	SBSRAM P, SCD	Pipeline, single cycle deselect SBSRAM support	VC5510	All
B5	SBSRAM linear burst	SBSRAM linear burst mode support	VC5510	All
B6	SBSRAM/ADV	SBSRAM /ADV internal burst advance support	None	6211, 6711
Asynchronous				
A1	32-bit asynchronous	Asynchronous memory 32-bit data bus width supported	VC5510	All
A2	16-bit asynchronous	Asynchronous memory 16-bit data bus width supported	VC5510	6201(ROM), 6701(ROM), 6202(ROM), 6211, 6711
A3	8-bit asynchronous	Asynchronous memory 8-bit data bus width supported	VC5510(ROM)	6201(ROM), 6701(ROM), 6202(ROM), 6211, 6711
A4	Asynchronous ready	Asynchronous memory ready input used to insert wait states for slow memories	VC5510	All
A5	Asynchronous timing configuration	Asynchronous memory read/write: strobe, setup, and hold width programmability	VC5510	All
Synchronous				
S1	Both SDRAM and SBSRAM	Both SDRAM and SBSRAM possible in same system	VC5510	6201, 6701
Write Performance				
W1	Write posting	Write posting support for improved write performance	VC5510	None
Power Savings				
P1	Power down	Power down of internal EMIF clock	VC5510 (idle domain)	All

References

1. *TMS320C55x DSP Peripherals Reference Guide* (SPRU317)
2. *TMS320C6000 Peripherals Reference Guide* (SPRU190)

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