

CompactFlash Memory Card Interface to the TMS320VC54x

Miguel Hernandez IV
C5000 Hardware Applications

ABSTRACT

This document contains information on how to interface the TMS320VC54x™ to a CompactFlash Memory Card in True IDE mode. A complete reference design is shown, including hardware and software interfaces. The software consists of a set of file system independent subroutines that perform the functions required to store and retrieve information from a CompactFlash Memory Card. Function descriptions are shown in this document, and the source code is available electronically from the TI web site. Although this application note specifically describes a C54x™ to CompactFlash interface, the hardware and software can be easily adapted to function with the TMS320C55x™ generation of DSPs.

Contents

1	Introduction	3
2	CompactFlash Overview	3
2.1	Data Storage	3
2.2	CompactFlash Memory Card Interface	7
2.2.1	CompactFlash Signal Descriptions	8
2.2.2	ATA Registers	9
2.3	ATA Register Functions	13
2.3.1	Reading and Writing the ATA Registers	13
2.3.2	Polling the Busy and Ready Status Bits	14
2.3.3	Polling the Data Request Bit (DRQ)	15
2.4	ATA Commands	16
2.4.1	Execute Drive Diagnostic	17
2.4.2	Identify Drive	17
2.4.3	Read Sectors	17
2.4.4	Set Features	20
2.4.5	Write Sectors	20
3	C54x External Memory Interface Operation	23
3.1	Wait-State Generator	24
3.2	Bank Switching Control Register (BSCR)	25
4	CompactFlash Interface to the C54x	26
4.1	Hardware Interface	27
4.2	Software Interface	32
5	Conclusion	34
6	References	34

TMS320C54x and TMS320C55x are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

List of Figures

Figure 1	Read/Write Head	4
Figure 2	Cylinder	4
Figure 3	Sector	5
Figure 4	C/H/S Mode Addressing	5
Figure 5	LBA Mode Addressing	6
Figure 6	CompactFlash Interface to the C54x Block Diagram	7
Figure 7	Status/Alternate Status Register	11
Figure 8	Read/Write an ATA Register (R1)	13
Figure 9	CompactFlash Busy/Ready Status Check (R2)	14
Figure 10	Data Request (DRQ) Status Check (R3)	15
Figure 11	Read Sector(s) Routine Part 1	18
Figure 12	Read Sector(s) Routine Part 2	19
Figure 13	Read Sector(s) Routine Part 3	20
Figure 14	Write Sector(s) Routine Part 1	21
Figure 15	Write Sector(s) Routine Part 2	22
Figure 16	Write Sector(s) Routine Part 3	23
Figure 17	Software Wait-State Register (SWWSR) Diagram	25
Figure 18	Software Wait-State Control Register (SWCR) Diagram	25
Figure 19	Bank-Switching Control Register (BSCR) Diagram	26
Figure 20	C54x Interface to the CompactFlash Block Diagram	27
Figure 21	CompactFlash Interface to the C54x Schematic	31

List of Tables

Table 1	CompactFlash Memory Card Signal Descriptions (True IDE Mode)	8
Table 2	ATA Register Addresses	10
Table 3	Status/Alternate Status Register Bit Summary	11
Table 4	ATA Command Set	16
Table 5	Diagnostic Error Codes	17
Table 6	Key External Interface Signals	24
Table 7	Software Wait-State Register (SWWSR) Bit Summary	25
Table 8	Bank-Switching Control Register (BSCR) Bit Summary	26
Table 9	SN74LVC138A 3-Line to 8-Line Decoder/Demultiplexer Signal Description	28
Table 10	SN74LVC138A 3-Line to 8-Line Decoder/Demultiplexer I/O	29
Table 11	ATA Register Addresses	29
Table 12	CompactFlash Card Detection Truth Table	30

1 Introduction

The C54x DSP is a suitable processor for a variety of handheld portable applications, many of which require a compact, removable, high-density storage media. Examples of such applications include digital cameras, digital music players, and personal digital assistants (PDAs). The CompactFlash Memory Card meets these requirements, and can be easily interfaced to the C54x. This application note describes how to interface the C54x to a CompactFlash Memory Card. A complete reference design is shown, including hardware and software interfaces.

The software consists of a set of subroutines that perform the functions required to store and retrieve information from a CompactFlash Memory Card. Function descriptions are shown in this document, and the source code is available electronically from the TI web site. These functions access the Compact Flash card at the sector level and do not implement any particular file system. Additional higher-level software can be added to the routines provided in this example to implement a file system in applications that require a particular file system, such as DOS FAT.

Although this application note specifically describes a C54x to CompactFlash interface, the hardware and software can be easily adapted to function with the C55x generation of DSPs.

2 CompactFlash Overview

CompactFlash is a removable mass storage device that electrically complies with the Personal Computer Memory Card International Association ATA standard, and supports a True IDE mode that is electrically compatible with an IDE disk drive. CompactFlash cards support both +5V and +3.3V operation and can function at either voltage level. CompactFlash uses standard ATA registers and command set, and has automatic error correction and retry capabilities, including an error correction code.

CompactFlash supports three different modes of operation: PC Card Memory Mode, PC Card I/O Mode, and True IDE Mode. True IDE Mode allows the CompactFlash to function like a hard disk drive. This document focuses on True IDE Mode operation.

2.1 Data Storage

The unit of data storage for the CompactFlash Memory Card is the sector (1 sector = 512 bytes). All reads and writes to the CompactFlash must be at least 512 bytes.

Sectors are identified according to two addressing schemes: Cylinder/Head/Sector (C/H/S) and Logical Block Addressing (LBA). When operating in C/H/S mode, a sector is identified according to three parameters: cylinder, head, and sector. To understand C/H/S addressing, the CompactFlash should be thought of as a hard disk drive.

A hard disk usually consists of several platters. Each platter requires two read/write heads, one for each side. The head is the mechanism that reads or writes data to the hard disk, and can do so on either side of a platter. Figure 1 is a geometric view of the head parameter in C/H/S mode addressing.

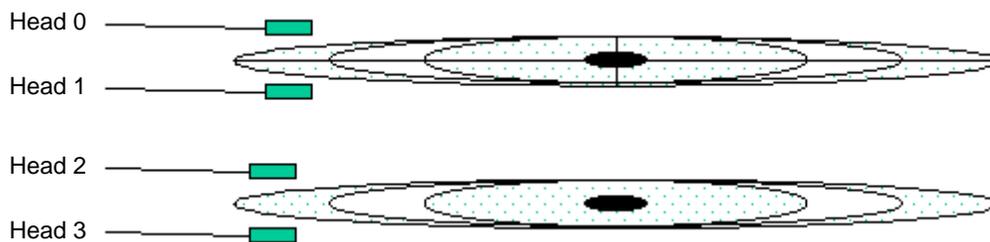


Figure 1. Read/Write Head

Each platter is divided into concentric circles, called tracks. A cylinder is a set of similar tracks across all platters. Figure 2 is a geometric view of the cylinder parameter in C/H/S mode addressing.

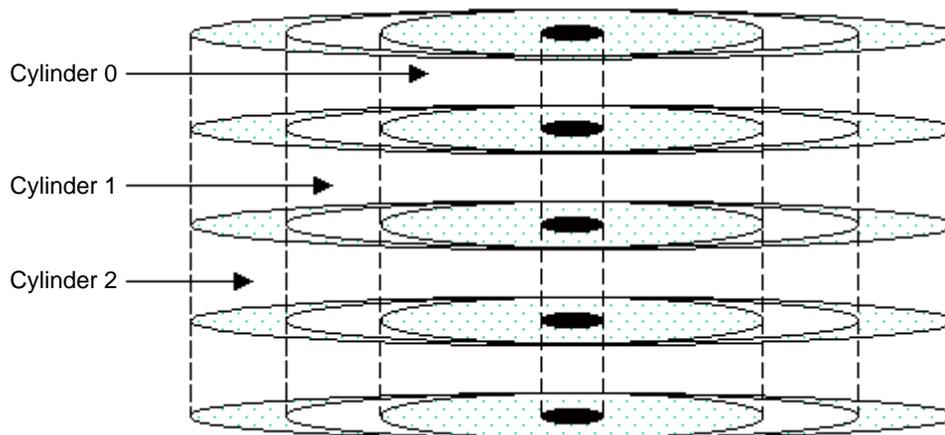


Figure 2. Cylinder

Tracks are areas around the disk where data can be written, and are divided into sectors. A sector is the smallest unit that can be accessed on a disk (1 sector = 512 bytes). Figure 3 is a geometric view of the sector parameter in C/H/S mode addressing.

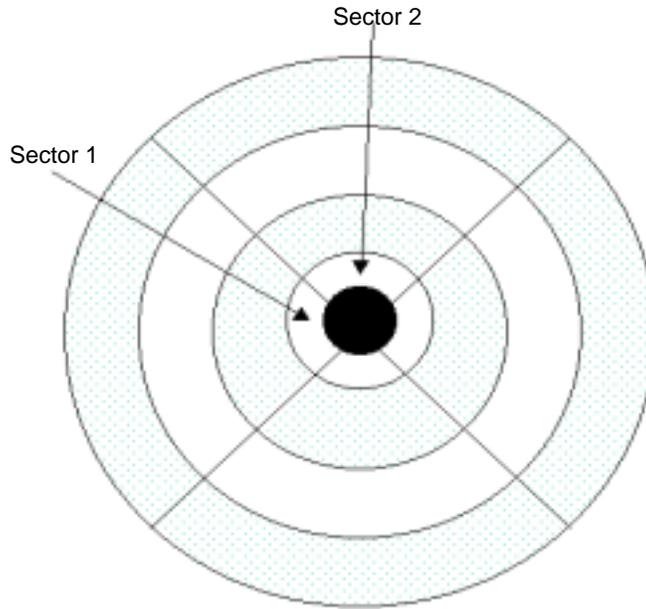


Figure 3. Sector

When used together, the cylinder, head and sector parameters completely describe the storage capacity of a hard disk drive (as well as the CompactFlash Memory Card). It is important to note that the first sector in C/H/S mode is 0/0/1 (0/0/0 is undefined). Figure 4 demonstrates an access to cylinder 1, head 1, and sector 1 (1/1/1).

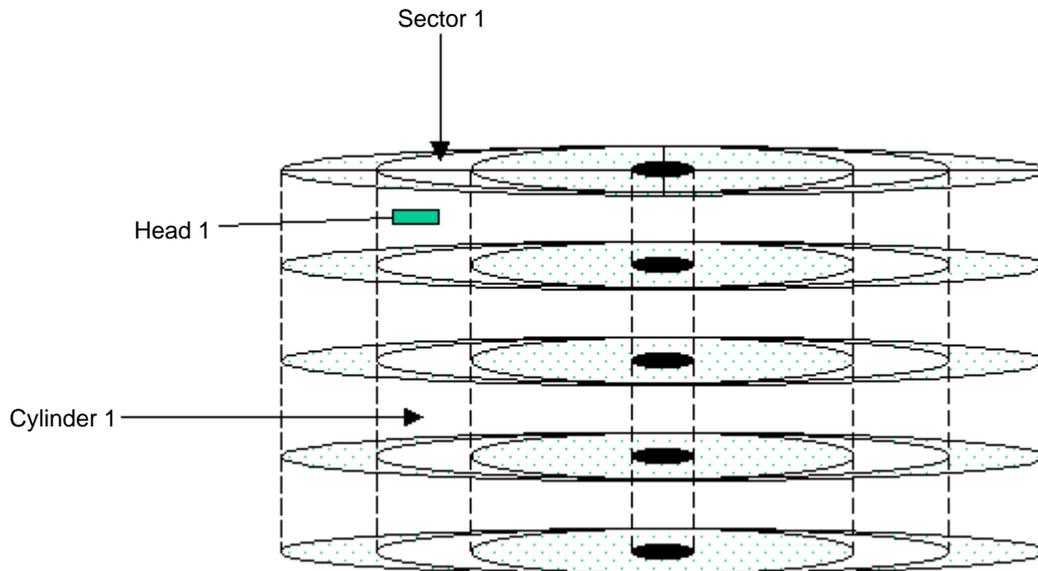


Figure 4. C/H/S Mode Addressing

The alternative to C/H/S mode addressing is LBA mode addressing. Rather than specifying three parameters for a data process (C/H/S), LBA mode addressing requires only one parameter, LBA X, where X can be any sector up to the last sector on the hard disk. LBA mode addressing is a scheme that assigns each sector a unique sector number. In essence, the sectors are linearly mapped and numbered from 0 up to N – 1, where N is the number of sectors on the disk. LBA mode addressing completely describes the storage capacity of a hard disk drive (as well as the CompactFlash Memory Card) with a single parameter. Figure 5 shows how LBA mode addressing linearly maps each sector.

LBA
0
1
2
3
4
.
.
.
N-1 (Last Sector)

Figure 5. LBA Mode Addressing

The equation to find the total number of sectors per card is:

$$SectorsPerCard_{Total} = C \cdot H \cdot S$$

Total disk capacity in bytes can be found as follows:

$$DiskCapacity_{Total} = C \cdot H \cdot S \cdot 512$$

2.2 CompactFlash Memory Card Interface

This section describes the physical and logical interfaces of the CompactFlash Memory Card in the context of a CompactFlash to C54x interface. Figure 6 gives a high-level view of this interface. A detailed description of this interface is covered in subsequent sections of this document. Although there are many ways to interface the C54x to a CompactFlash Memory Card, Figure 6 represents the interface used in this document.

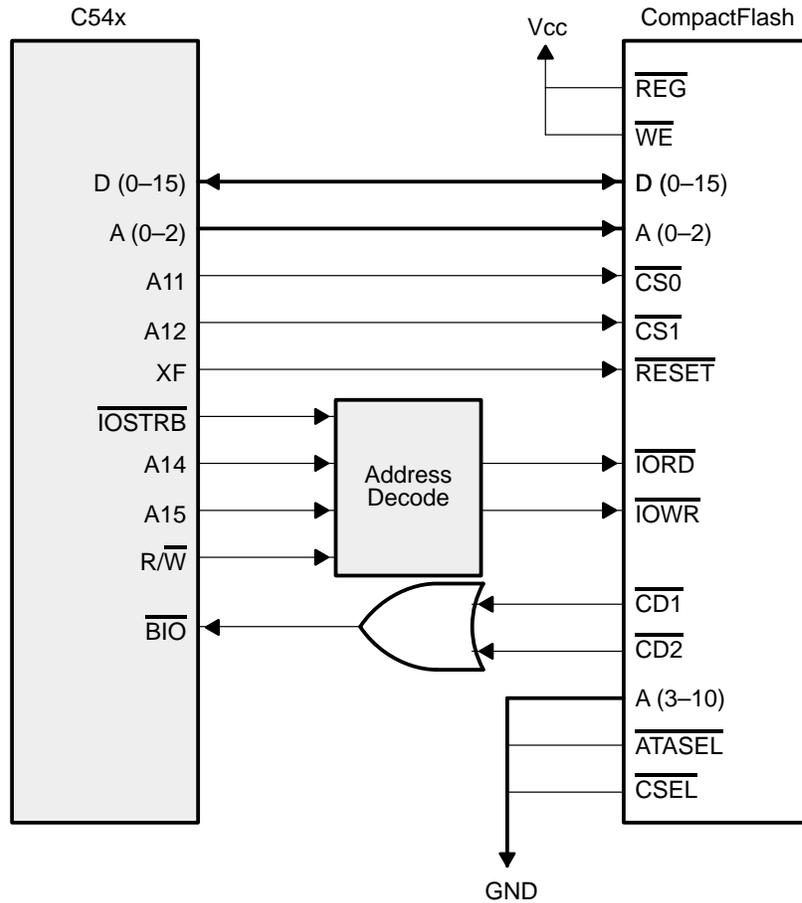


Figure 6. CompactFlash Interface to the C54x Block Diagram

2.2.1 CompactFlash Signal Descriptions

Table 1 lists and describes the CompactFlash Memory Card I/O signals as they pertain to the C54x interface. Signals generated by the C54x are designated as inputs, signals generated by the CompactFlash are outputs, and bi-directional signals are designated as I/O. Note that some signals are not used while operating in True IDE Mode.

Table 1. CompactFlash Memory Card Signal Descriptions (True IDE Mode)

Signal Name	I/O†	CF Pin	Description	
A2–A0	Address Bus	I	18, 19, 20	Used to access a register or data port.
A10–A3	Address Bus	I	8, 10, 11, 12, 14, 15, 16, 17	Not used and should be grounded.
$\overline{\text{PDIAG}}$	Passed Diagnostics	I/O	46	Indicates whether or not the CompactFlash has passed its diagnostic tests.
$\overline{\text{DASP}}$	Disk Active/Slave Present	I/O	45	Indicates that a card is active, or that card 1 is present.
$\overline{\text{CD1}}, \overline{\text{CD2}}$	Card Detect	O	26, 25	Connected to ground on the CompactFlash. Used by the C54x to determine if the card is in its socket.
$\overline{\text{CS0}}$	Chip Select 0	I	7	Used to select the Command Block Registers.
$\overline{\text{CS1}}$	Chip Select 1	I	32	Used to select the Control Block Registers.
$\overline{\text{CSEL}}$	Cable Select	I	39	The CompactFlash card is configured as card 0 if CSEL is grounded, and as card 1 if CSEL is open.
D15–D0	Data Bus	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	8-bit or 16-bit data bus. The lower 8 bits are used for ATA Register data transfers. All Data Register data transfers are 16-bit using D15–D0.
GND	Ground	N/A	1, 50	Ground.
$\overline{\text{INPACK}}$	Input Acknowledge	O	43	Not used and should not be connected.
$\overline{\text{IORD}}$	I/O Read	I	34	Read strobe signal.
$\overline{\text{IOWR}}$	I/O Write	I	35	Write strobe signal.
$\overline{\text{ATASEL}}$	ATA Select	I	9	This input should be grounded to enable True IDE mode.
INTRQ	Interrupt Request	O	37	INTRQ is asserted <u>only</u> when the card has a pending interrupt and the $\overline{\text{IEN}}$ bit in the Device Control Register has been cleared. This signal is not used in the interface described in this document.
$\overline{\text{REG}}$		I	44	Not used and should be connected to VCC by the host.
$\overline{\text{RESET}}$	Hardware Reset	I	41	Hardware reset. Must be asserted for at least 25 microseconds.
VCC	Vcc	N/A	13, 38	+5 Volts, +3.3 Volts

† I/O – Input/Output

Table 1. CompactFlash Memory Card Signal Descriptions (True IDE Mode) (Continued)

Signal Name	I/O†	CF Pin	Description
$\overline{VS1}$, $\overline{VS2}$	O	33, 40	Voltage sense signals.
IORDY	O	42	This signal is negated to extend the transfer cycle of any register access when the card is not ready to respond to a data transfer request.
\overline{WE}	I	36	Not used and should be connected to VCC.
$\overline{IOCS16}$	O	24	Indicates that the 16-bit data port has been addressed and is prepared to accept or transmit data.

† I/O – Input/Output

2.2.2 ATA Registers

Communication to and from the CompactFlash Memory Card is accomplished through a set of registers called ATA Registers. All registers are 8-bit except the Data Register, which can be configured as a 16-bit or 8-bit register. Since the native data width of the C54x is 16 bits, the Data Register is configured as a 16-bit register in the interface used in this document. Each register is selected by an access code applied on signals $\overline{CS1}$, $\overline{CS0}$, A2, A1, and A0. A read or write process is specified with the \overline{IORD} and \overline{IOWR} signals respectively.

The ATA registers are grouped into 2 categories: Control Block Registers and Command Block Registers. The Command Block Registers are used for sending commands to the CompactFlash and returning the status of the CompactFlash. The status conditions include whether or not the CompactFlash is busy or ready, and if errors have been detected. The Control Block Registers are used for control and provide an alternate means of returning the status of the CompactFlash.

It is important to note that some ATA Registers support only read or write accesses, while others support both read and write accesses. For this reason, some access codes are shared between two registers. For example, the Alternate Status Register and the Device Control Register share the same access code, yet they differ in the processes they support. The Alternate Status Register is a read only register, and the Control Register is a write only register. Table 2 lists the ATA Registers and their corresponding access codes. See the CompactFlash Memory Card Product Manual for True IDE Mode read and write timing diagrams for the ATA Registers.

Table 2. ATA Register Addresses

Addresses					Functions	
$\overline{CS1}$	$\overline{CS0}$	A2	A1	A0	\overline{IORD}	\overline{IOWR}
Control Block Registers						
0	1	1	1	0	Alternate Status Register	Device Control Register
0	1	1	1	1	Card Address Register	Reserved
Command Block Registers						
1	0	0	0	0	Data Register	Data Register
1	0	0	0	1	Error Register	Features Register
1	0	0	1	0	Sector Count Register	Sector Count Register
1	0	0	1	1	Sector Number Register	Sector Number Register
1	0	1	0	0	Cylinder Low Register	Cylinder Low Register
1	0	1	0	1	Cylinder High Register	Cylinder High Register
1	0	1	1	0	Drive/Head Register	Drive/Head Register
1	0	1	1	1	Status Register	Command Register
0	0	X	X	X	Invalid Mode	Invalid Mode
1	1	X	X	X	Standby Mode	Standby Mode

X = Don't Care Term

The following sections describe each ATA Register. For bitwise descriptions, see the *CompactFlash Memory Card Product Manual*.

2.2.2.1 Status/Alternate Status Registers (read)

The Status and Alternate Status registers return the status of the CompactFlash Memory Card. Both registers return the same information, but differ in that reading the Status Register clears a pending interrupt while reading the Alternate Status Register does not. If a process that generates interrupts is used, and interrupts are enabled in the Control Register, the Status Register should be read to clear the interrupt. Otherwise, the Alternate Status Register should be read. If interrupts will not be used, either register can be read. The BUSY and RDY bits in these registers indicate whether or not the CompactFlash Card is ready to accept commands and perform operations. The Status Register is shown in Figure 7 and a bitwise description of the Status Register is given in Table 3.

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Figure 7. Status/Alternate Status Register
Table 3. Status/Alternate Status Register Bit Summary

Bit Name	Description
BUSY	When set, no other bits are valid in this register. Indicates that the CompactFlash has access to the Command Block Registers. See Figure 8 for a sample routine that checks the busy status.
RDY	Indicates that the CompactFlash is ready to perform operations. See Figure 9 for a sample routine that checks the ready status.
DWF	Indicates that a Write Fault has occurred.
DSC	Indicates that the CompactFlash is ready.
DRQ	Indicates that the CompactFlash is ready for data transfer. See Figure 10 for a sample routine that checks the DRQ status.
CORR	Indicates that a correctable error has occurred.
0	Always 0.
ERR	Indicates that an error has occurred. The bits in the Error Register are now valid and contain additional information.

2.2.2.2 Device Control Register (write)

This register is responsible for two CompactFlash functions. It is used to enable or disable interrupt requests to the C54x and to issue a software reset to the CompactFlash.

2.2.2.3 Card (Drive) Address Register (read)

This register contains the inverted drive and head addresses of the currently selected drive. It also indicates that the CompactFlash Card is being written to. As recommended by the CompactFlash Memory Card Product Manual, this register should not be mapped into the C54x I/O space because of potential conflicts on bit 7. See the CompactFlash Memory Card Product Manual for more details on these conflicts and this register.

2.2.2.4 Data Register (read/write)

This register is used for all data transfers to and from the CompactFlash. It is the only 16-bit register in the CompactFlash interface, but can be configured for 8-bit transfers through the Features Register and the Set Features command.

2.2.2.5 Error Register (read)

This register contains information about the source of an error and is valid only when ERR = 1 in the Status Register. Error conditions such as uncorrectable data errors and invalid sector requests are reflected in the Error Register.

2.2.2.6 Features Register (write)

The Features Register is a command specific register that may be used to disable or enable certain features of the device. This register is used in conjunction with the Set Features command to disable or enable features such as 8-bit data transfers through the Data Register.

2.2.2.7 Sector Count Register (read/write)

This register contains the number of sectors of data requested for a read or write process. If the value in this register is zero, 256 sectors will be transferred. If the read/write process was successful, this register will equal 0 at command completion. Otherwise, the number of sectors that need to be transferred in order to complete the request will be specified.

2.2.2.8 Sector Number Register (read/write)

This register contains the sector number or bits 7–0 of the Logical Block Address (LBA) for a CompactFlash read or write process.

2.2.2.9 Cylinder Low Register (read/write)

This register contains the low order 8 bits of the cylinder address or bits 15–8 of the LBA for a CompactFlash read or write process.

2.2.2.10 Cylinder High Register (read/write)

This register contains the high order bits of the cylinder address or bits 23–16 of the LBA for a CompactFlash read or write process.

2.2.2.11 Card/Head Register (read/write)

The Card/Head Register is used to select the card number for a CompactFlash operation. It contains the head number or bits 24–27 of the LBA for a CompactFlash read or write process. It is also used to select LBA or C/H/S mode addressing.

2.2.2.12 Command Register (write)

This register is used to issue commands to the CompactFlash. Command execution begins once this register is written. See section 2.4 for details on the ATA Command Set.

2.3 ATA Register Functions

The ATA register set supports a number of status and control functions, all of which entail read or write processes. This section describes the software flow for reading and writing the ATA registers and for polling certain bits.

2.3.1 Reading and Writing the ATA Registers

The most common operations used on the ATA registers are the read and write operations. The steps in the read and write operations are very similar and are illustrated in Figure 8. Note that the only difference between the read and write operations is the code applied on the \overline{IORD} and \overline{IOWR} signals. To write an ATA register, $\overline{IORD} = 1$ and $\overline{IOWR} = 0$. To read an ATA register, $\overline{IORD} = 0$ and $\overline{IOWR} = 1$.

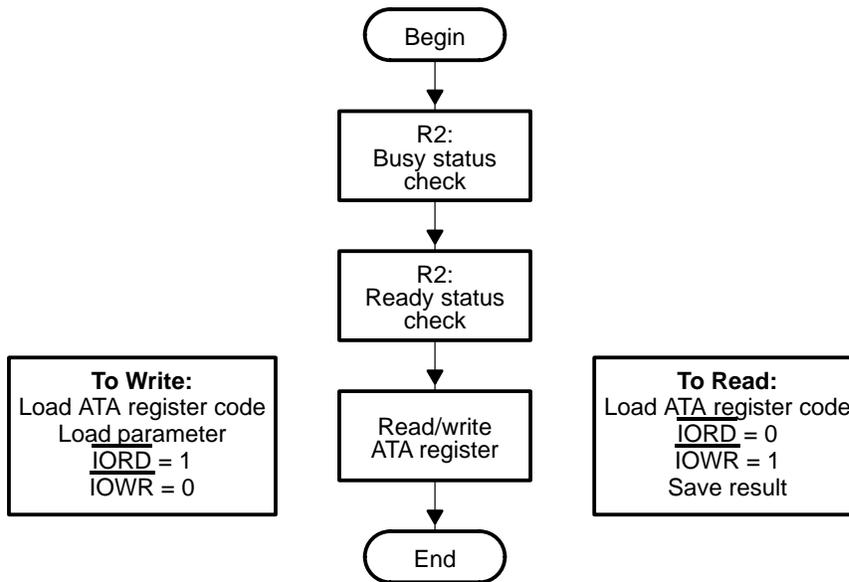


Figure 8. Read/Write an ATA Register (R1)

2.3.2 Polling the Busy and Ready Status Bits

Polling the busy and ready status of the CompactFlash are fundamental operations that will be used over and over again in software. The BUSY bit is set whenever the CompactFlash has access to the Command Block registers. During this time, the ATA Registers cannot be accessed by the C54x. The RDY bit is set whenever the CompactFlash is ready to accept and respond to a command. The steps involved in polling the BUSY and RDY status are very similar and are illustrated in Figure 9. Note that a not busy status does not translate into a ready status. Both bits should be polled to ensure that the CompactFlash is ready to perform register operations.

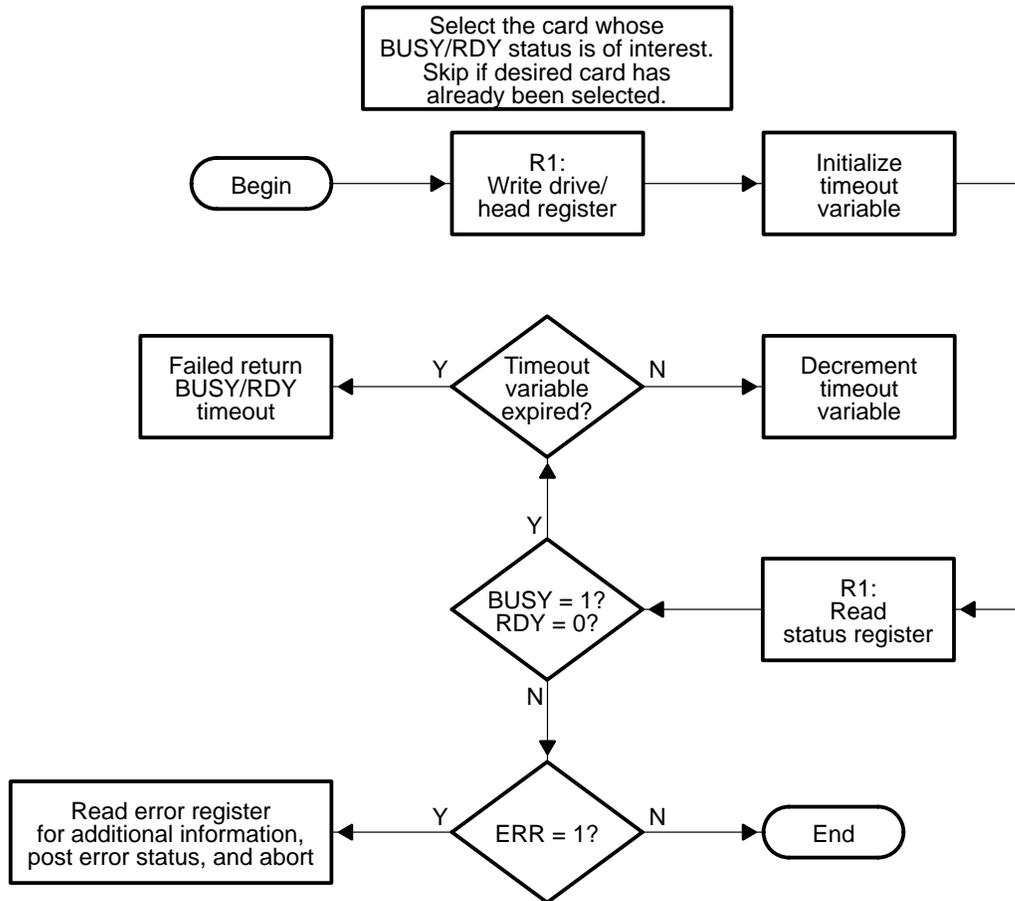


Figure 9. CompactFlash Busy/Ready Status Check (R2)

2.3.3 Polling the Data Request Bit (DRQ)

The DRQ bit indicates whether or not the CompactFlash is ready for data transfer. If a read command has been issued and DRQ is set, then the CompactFlash is ready to transfer data to the C54x. Otherwise, the CompactFlash is not ready for data transfer. If a write command has been issued and DRQ is set, then the CompactFlash is ready to accept data from the C54x. Otherwise, the CompactFlash is not ready for data transfer. Figure 10 illustrates a routine that polls the DRQ bit.

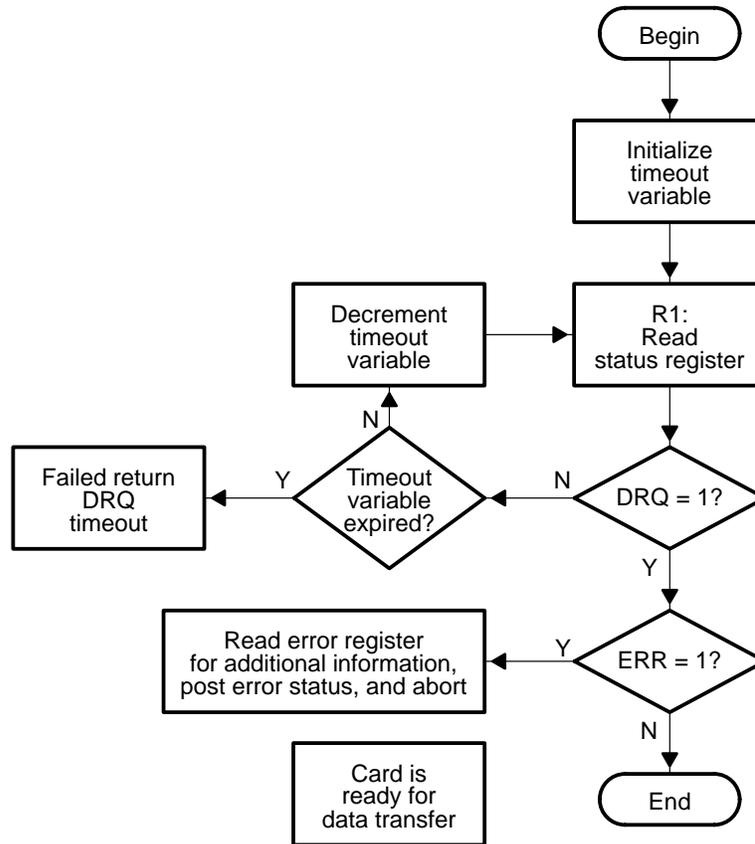


Figure 10. Data Request (DRQ) Status Check (R3)

2.4 ATA Commands

This section describes the ATA Command Set and provides sample routines for CompactFlash read and write processes. The ATA Commands are used to perform specific operations such as reading and writing the CompactFlash, performing diagnostic tests, and enabling or disabling certain features of the CompactFlash. Commands are issued to the CompactFlash by loading the pertinent registers in the command block with the necessary parameters, then writing the command code to the Command Register. Commands are accepted according to three different classes, all of which depend on the BUSY bit being equal to zero (CompactFlash not busy) before a command is issued. The three classes of command acceptance are described below.

- When a Class 1 command is issued and accepted, the CompactFlash will set the BUSY bit within 400 nanoseconds.
- When a Class 2 command is issued and accepted, the CompactFlash will:
 - Set the BUSY bit within 400 nanoseconds (ns)
 - Prepare the sector buffer for a write operation
 - Set the DRQ bit within 700 microseconds (us)
 - Clear the BUSY bit within 400ns of setting the DRQ bit.
- When a Class 3 command is issued and accepted, the CompactFlash will:
 - Set the BUSY bit within 400ns
 - Prepare the sector buffer for a write operation
 - Set the DRQ bit within 20 milliseconds (ms)
 - Clear the BUSY bit within 400ns of setting the DRQ bit.

Table 4 is an abbreviated version of the ATA Command Set that specifies the required parameters for a particular command. A letter 'C' under a register heading indicates that only the card number is valid for the command. A letter 'V' under a register heading indicates that the register contains a valid parameter for the command. Subsequent sections describe each command listed in the table. For a complete discussion on the ATA Command Set, see the CompactFlash Memory Card Product Manual. Note that Class 3 commands are not discussed in this document.

Table 4. ATA Command Set

Command	Class [†]	Code	ATA Registers					
			Features	Sector Cnt	Sector Num	Cylinder H/L	Card/Head	LBA
Execute Drive Diagnostic	1	0x90					C	
Identify Drive	1	0xEC					C	
Read Sector(s)	1	0x20		V	V	V	V	V
Set Features	1	0xEF	V				C	
Write Sector(s)	2	0x30		V	V	V	V	V

[†] Class 3 commands are not used in this document.

V – The register contains a valid parameter for this command.

C – Only the Drive parameter is valid.

2.4.1 *Execute Drive Diagnostic*

This command performs diagnostic tests on the CompactFlash Memory Card. A diagnostic code is returned upon completion in the Error Register. The diagnostic codes are listed in Table 5.

Table 5. Diagnostic Error Codes

Code	Error
0x01	No Errors
0x02	Formatter Device Error
0x03	Sector Buffer Error
0x04	ECC Circuitry Error
0x05	Microprocessor Error
0x8X	Slave Failed

X – Don't Care Term

2.4.2 *Identify Drive*

This command enables the C54x to receive parameter information from the CompactFlash. When this command is issued, the CompactFlash sets BUSY, then sets DRQ and generates an interrupt when ready to transfer data. The parameter information is read from the Data Register. For a detailed description of the parameter words, see the CompactFlash Memory Card Product Manual.

2.4.3 *Read Sectors*

This command reads 1 to 256 sectors as specified by the Sector Count Register. Once the Read Sectors command has been issued, the DRQ bit will be set every time the CompactFlash is ready to transfer data to the C54x. Be aware that the INTRQ signal is not used in the interface described in this document. As a result, the interrupts generated during the Read Sectors command will be ignored. For information on interrupt generation, see the CompactFlash Memory Card Product Manual.

At command completion, the Command Block Registers contain the C/H/S or LBA of the last sector read. If an error occurs, the read process will terminate at the C/H/S or LBA where the error occurred. A sample Read Sectors routine (with interrupts ignored) is shown in Figure 11 through Figure 13.

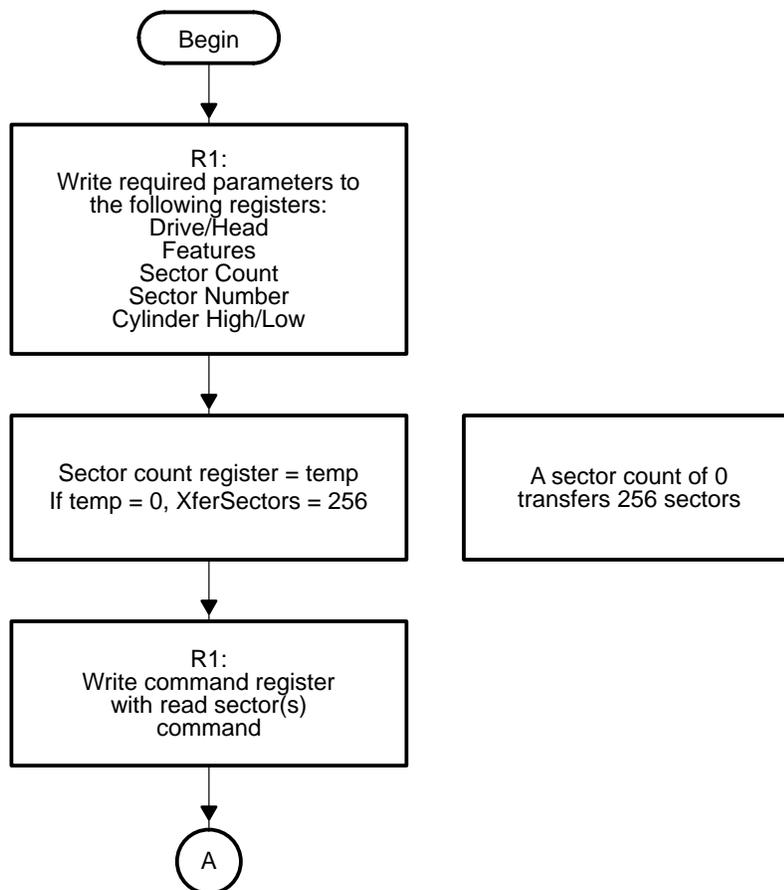


Figure 11. Read Sector(s) Routine Part 1

The Read Sectors software flow in Figure 11 begins by writing all the required parameters to the Command Block Registers as specified in Table 4. This includes specifying the card number, the addressing mode, the sector to begin reading from, the number of sectors to read, and any special features. This routine does not use interrupts, so the \overline{IEN} bit in the Device Control Register should be set to disable interrupts. The value written to the Sector Count Register is tested to determine how many sectors will be read. Recall that writing zero to the Sector Count Register transfers 256 sectors. The Command Register is then written with the Read Sector(s) command.

The Read Sectors software flow continues in Figure 12. The DRQ bit is polled until the CompactFlash indicates that it is ready for data transfer. Once DRQ is set, one sector of data is transferred through the Data Register to the C54x. The routine repeats until all sectors have been transferred as specified by the Sector Count Register. Note that the read process will be aborted prematurely if the ERR bit is set at any time.

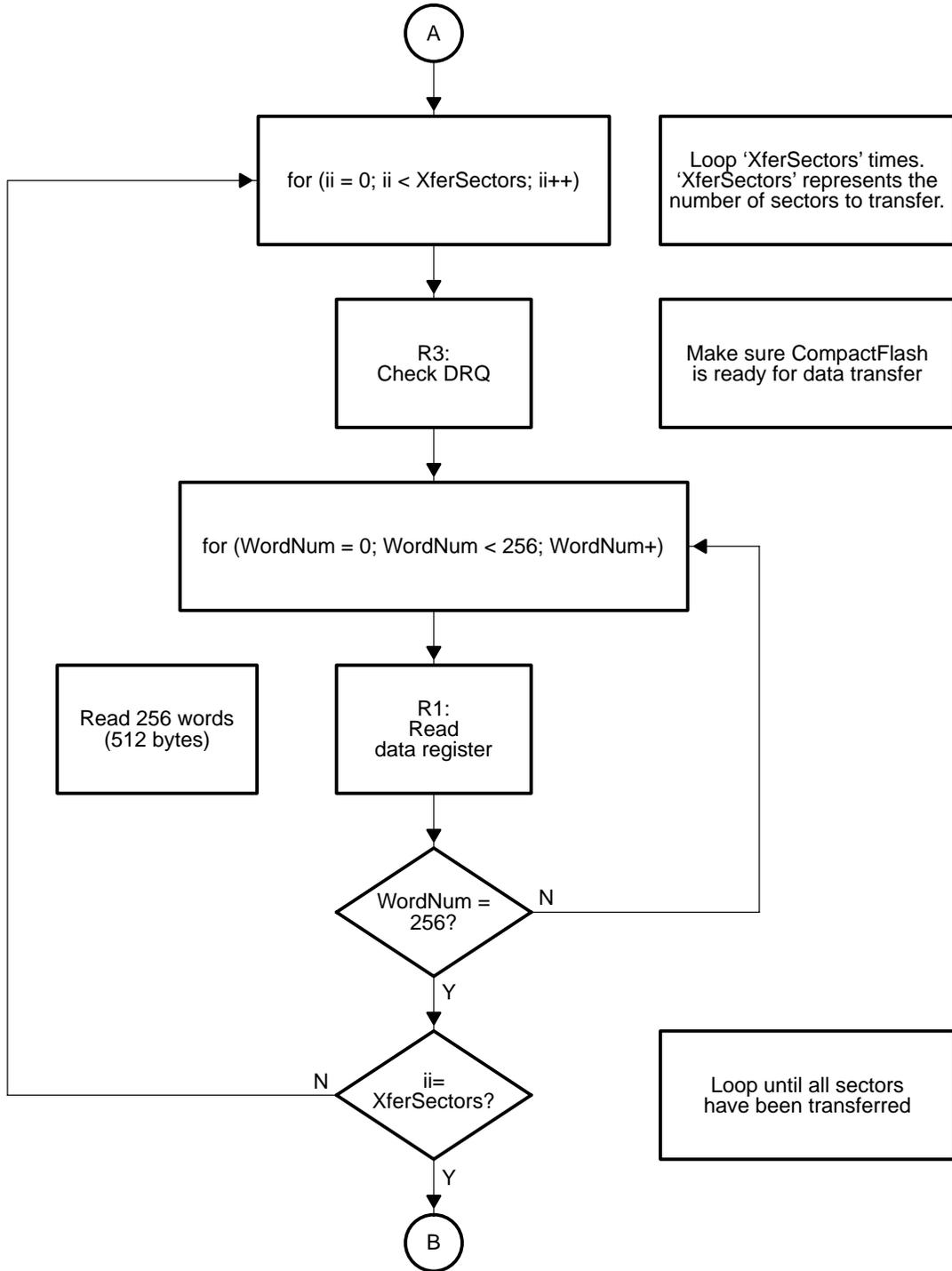


Figure 12. Read Sector(s) Routine Part 2

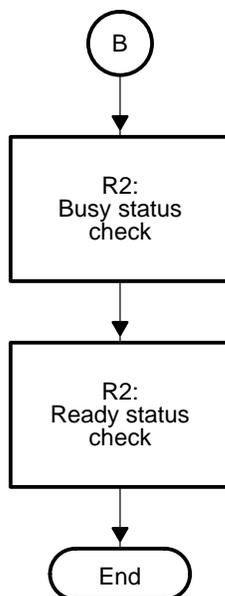


Figure 13. Read Sector(s) Routine Part 3

The Read Sectors software flow ends in Figure 13. Once the read process has completed, the BUSY and RDY bits are polled until a ready status is indicated by the CompactFlash. If an error has been detected, as indicated by the ERR bit set to one, the Error Register should be read and the error serviced.

2.4.4 Set Features

This command enables or disables certain features of the CompactFlash as specified by the Features Register. For example, feature code 0x01 enables 8-bit data transfers through the Data Register. A description of the features supported can be found in the CompactFlash Memory Card Product Manual.

2.4.5 Write Sectors

This command writes 1 to 256 sectors to the CompactFlash as specified in the Sector Count Register. Once the Write Sectors command has been issued, the DRQ bit will be set every time the CompactFlash is ready to accept data from the C54x. Be aware that the INTRQ signal is not used in the interface described in this document. As a result, the interrupts generated during the Write Sectors command will be ignored. For information on interrupt generation, see the CompactFlash Memory Card Product Manual.

If an error occurs during a sector write, the write process will terminate. The Command Block Registers will contain the C/H/S or the LBA of the sector where the error occurred. A sample Write Sectors routine (with interrupts ignored) is shown in Figure 14 through Figure 16.

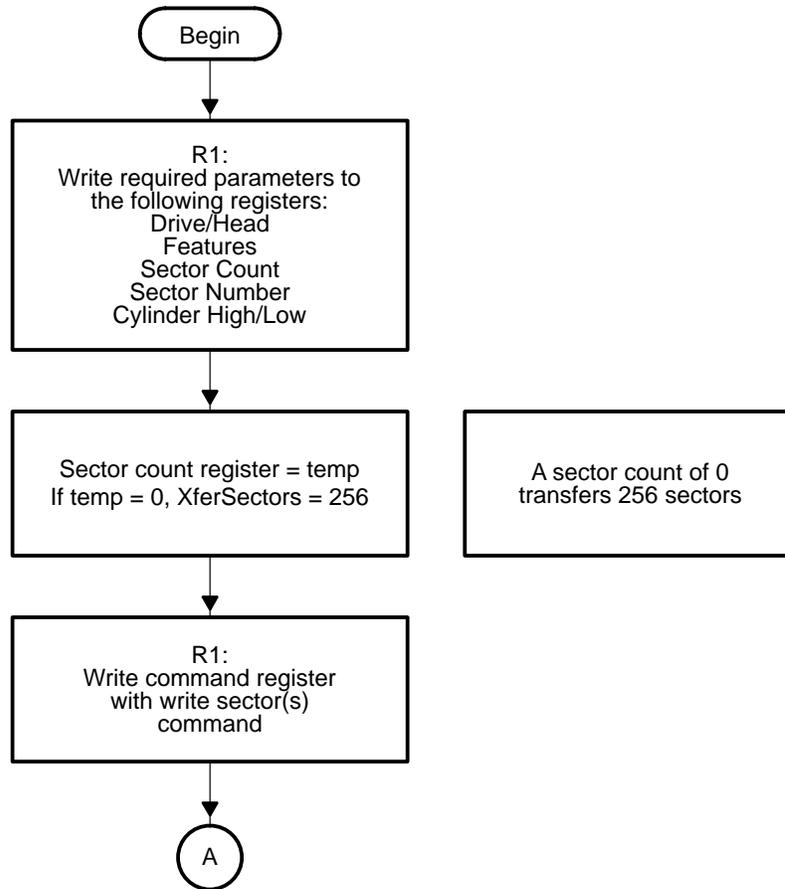


Figure 14. Write Sector(s) Routine Part 1

The Write Sectors software flow in Figure 14 begins just as the Read Sectors routine does. The required parameters are written to the Command Block Registers as specified in Table 4. This includes specifying the card number, the addressing mode, the sector to begin reading from, the number of sectors to read, and any special features. This routine does not use interrupts, so the $\overline{\text{IEn}}$ bit in the Device Control Register should be set to disable interrupts. The value written to the Sector Count Register is tested to determine how many sectors will be read. Recall that writing zero to the Sector Count Register transfers 256 sectors. The Command Register is then written with the Write Sector(s) command.

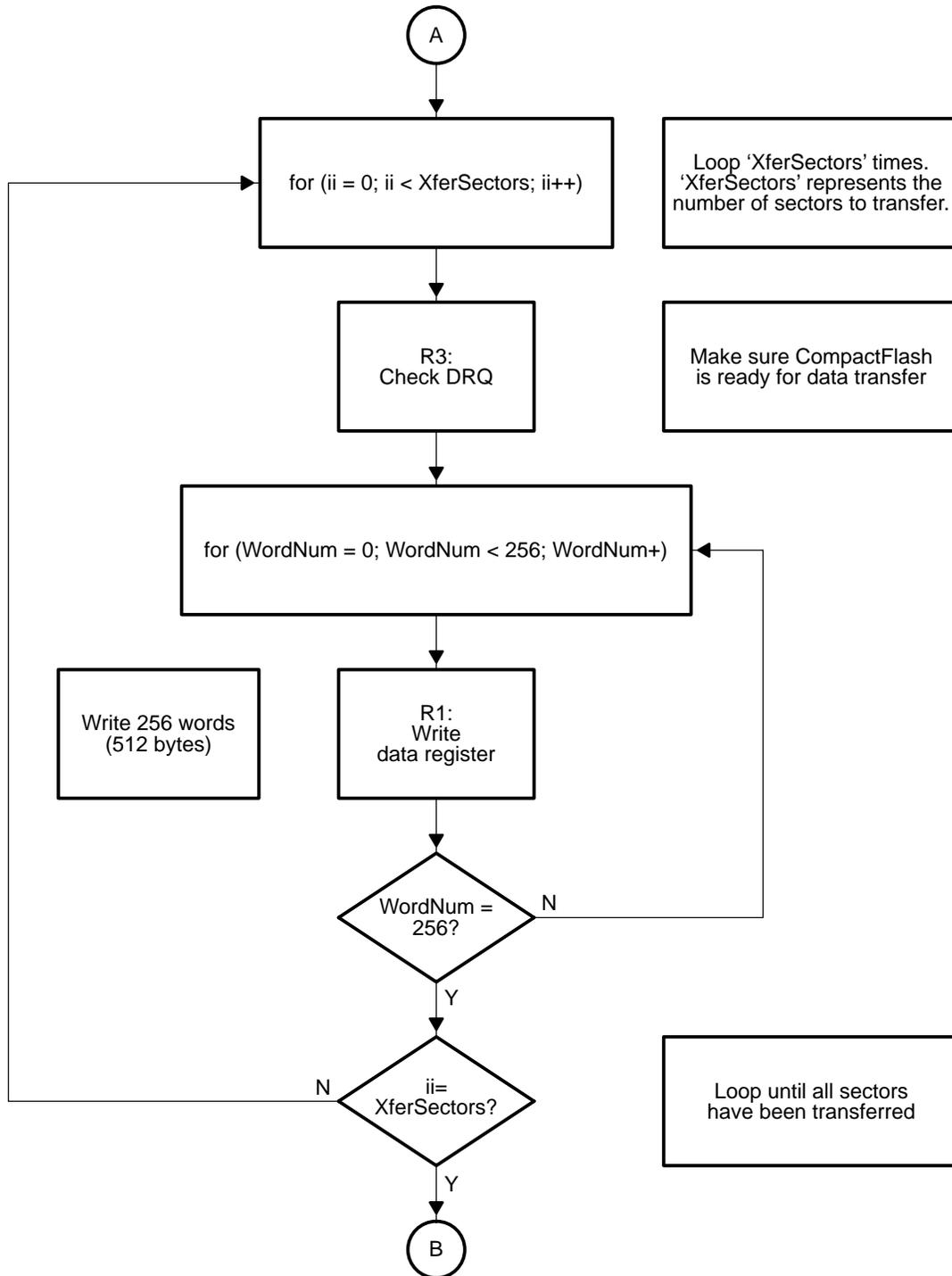


Figure 15. Write Sector(s) Routine Part 2

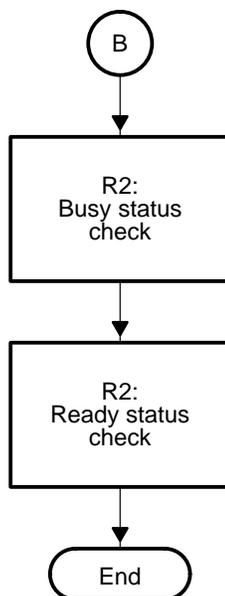


Figure 16. Write Sector(s) Routine Part 3

The Write Sectors software flow continues in Figure 15. The DRQ bit is polled until the CompactFlash indicates that it is ready to accept data from the C54x. Once DRQ is set, one sector of data is transferred from the C54x through the Data Register to the CompactFlash. The routine repeats until all sectors have been transferred as specified by the Sector Count Register. Note that the write process will be aborted prematurely if the ERR bit is set at any time.

The Write Sectors software flow ends in Figure 16. Once the write process has completed, the BUSY and RDY bits are polled until a ready status is indicated by the CompactFlash. If an error has been detected, as indicated by the ERR bit set to one, the Error Register should be read and the error serviced.

3 C54x External Memory Interface Operation

This section describes the external memory interface (EMIF) operation and control used to interface the C54x to the CompactFlash Memory Card. For a full discussion on the EMIF, see the *TMS320C54x DSP CPU Reference Guide* (SPRU131).

The EMIF consists of a data bus, an address bus, and a set of control signals for accessing off-chip memory and I/O ports. Table 6 lists and describes key signals for the external memory interface.

Table 6. Key External Interface Signals

Signal	Description
A15–A0	Parallel address bus A15 [most significant bit (MSB)] through A0 [least significant bit (LSB)]. These lines are multiplexed to address external memory (program, data) or I/O. This bus is used to select the ATA Registers.
D15–D0	Parallel data bus D15 (MSB) through D0 (LSB). D15–D0 is multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. This bus is used to transfer data to and from the CompactFlash.
$\overline{\text{IOSTRB}}$	IOSTRB is always high unless low-level asserted to indicate an external bus access to an I/O device. This signal is used to choose the $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ signals on the CompactFlash.
$\overline{\text{R/W}}$	Read/write signal. $\overline{\text{R/W}}$ indicates transfer direction during communication to an external device. R/W is normally in the read mode (high), unless it is asserted low when the DSP performs a write operation. This signal is used to choose the $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ signals on the CompactFlash.
READY	Data ready. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states. The external ready input signal (READY) and the software-generated wait states allow the processor to interface with memory and I/O devices of varying speeds. When communicating with slower devices, the CPU waits until the other device completes its function and sends the READY signal to continue execution.
$\overline{\text{MSC}}$	Microstate complete. $\overline{\text{MSC}}$ indicates completion of all software wait states. When two or more software wait states are enabled, the $\overline{\text{MSC}}$ pin goes active at the beginning of the first software wait state and goes inactive high at the beginning of the last software wait state. If connected to the READY input, $\overline{\text{MSC}}$ forces one external wait state after the last internal wait state is completed.
XF*	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or used as a general-purpose output pin. This pin is used to issue a hardware reset to the CompactFlash.
$\overline{\text{BIO}}^\dagger$	$\overline{\text{BIO}}$ can be used to monitor peripheral devices. This general-purpose input pin is used to detect if the CompactFlash Memory Card is properly inserted in its socket.

† Not part of the EMIF, but used to interface the C54x to the CompactFlash.

Two units in the C54x control the EMIF: the wait-state generator and the bank-switching logic. Two registers control these units: the software wait-state register (SWWSR) and the bank-switching control register (BSCR). These registers are described in the following sections.

3.1 Wait-State Generator

The software-programmable wait-state generator can extend external bus cycles by up to seven machine cycles, providing a convenient means to interface the C54x DSP to slower external devices. Devices that require more wait states can be interfaced using the hardware READY line. The SWWSR controls the software-programmable wait-state. The program and data spaces each consist of two 32K-word blocks, and the I/O space consists of one 64K-word block. Each of these blocks has a corresponding 3-bit field in the SWWSR and is shown and described in Figure 17 and Table 7. The value of a 3-bit field in the SWWSR specifies the number of wait states to be inserted for each access in the corresponding space and address range. The minimum value, which adds no wait states, is 0 (000b). A value of 7 (111b) provides the maximum number of wait states.



Figure 19. Bank-Switching Control Register (BSCR) Diagram

Table 8. Bank-Switching Control Register (BSCR) Bit Summary

Bit	Name	Function
15–12	BNKCMP	Bank compare. Determines the external memory-bank size.
11	PS–DS	Program read-data read access. Inserts an extra cycle between consecutive accesses of program read and data read, or data read and program read. PS-DS = 0 No extra cycles are inserted unless banks are crossed. PS-DS = 1 One extra cycle is inserted between consecutive accesses of program read and data read, or data read and program read.
10–9	Reserved	These bits are reserved.
8	IPIRQ	Interprocessor interrupt request bit.
7–3	Reserved	These bits are reserved.
2	HBH	HPI bus holder bit.
1	BH	Bus holder. Controls the bus holder: BH = 0 The bus holder is disabled. BH = 1 The bus holder is enabled. The data bus, D(15–0), is held in the previous logic level.
0	EXIO	External bus interface off. The EXIO bit controls the external-bus-off function. EXIO = 0 The external-bus-off function is disabled. EXIO = 1 The external-bus-off function is enabled.

4 CompactFlash Interface to the C54x

There are many ways to interface a CompactFlash Memory Card to a C54x DSP in True IDE Mode. This section describes one such implementation of this interface. A complete reference design is shown, including both hardware and software. The software interface consists of a set of file system independent subroutines that perform the functions required to store and retrieve information from a CompactFlash Memory Card at the sector level. The source code is available electronically from the TI web site.

4.1 Hardware Interface

The CompactFlash Memory Card can be easily interfaced to the C54x through the EMIF. A high level view of this interface can be seen in Figure 16, and a more detailed schematic view can be seen in Figure 20. Note that the interface used in this document does not allow hot swapping since Vcc to the CompactFlash is not controlled. In this case, hot swapping, is defined as switching CompactFlash cards from the CompactFlash socket while the system is powered on. Hot swapping with this interface can damage the CompactFlash Memory Card. If hot swapping is desired, Vcc to the CompactFlash must be controlled and turned on after the card is inserted in its socket. The only interface signals on the CompactFlash that may be driven high while Vcc is off are $\overline{CD1}$ and $\overline{CD2}$.

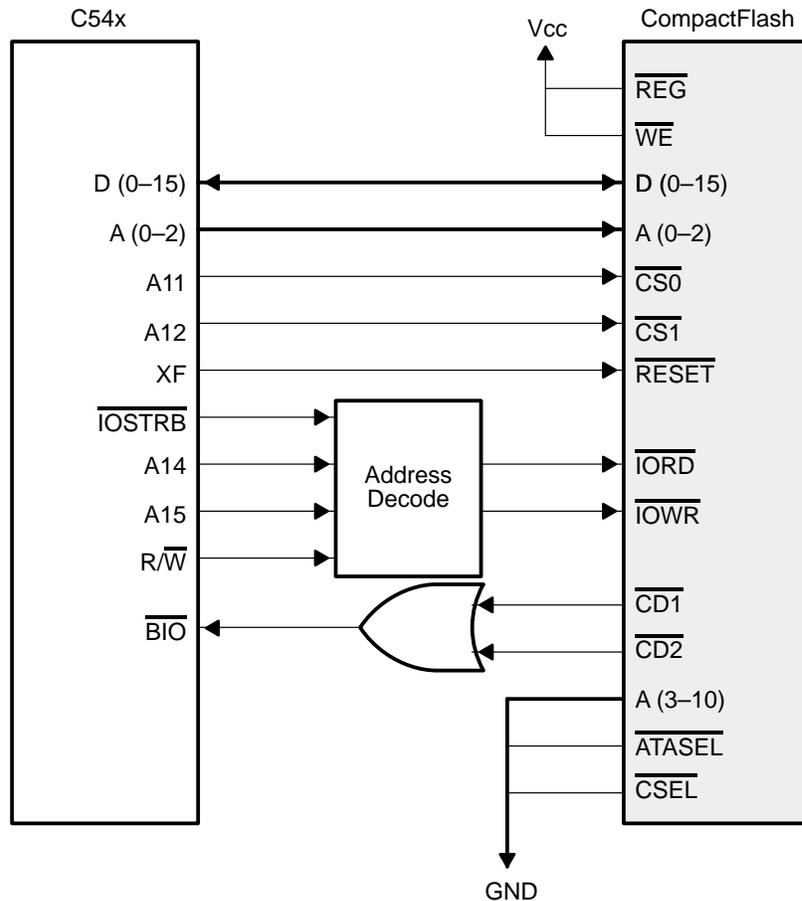


Figure 20. C54x Interface to the CompactFlash Block Diagram

Lines A0–A2 from the C54x parallel address bus are connected to lines A0–A2 on the CompactFlash address bus, and lines A11 and A12 from the C54x address bus are connected to the chip select signals $\overline{CS0}$ and $\overline{CS1}$. This configuration allows the C54x to access the ATA Registers when an access code is applied on signals A0–A2, A11 and A12. The C54x parallel data bus is connected to the CompactFlash data bus and allows the C54x to handle data transfers to and from the ATA Registers. Recall that the ATA Registers are 8-bit registers, except for the Data Register, which can be configured as an 8-bit or 16-bit register. The Data Register is configured as a 16-bit register in this interface. Data lines D15–D8 are don't care terms for all other ATA Register operations and should be ignored.

A decoder is used in conjunction with the C54x to generate the $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ strobes for CompactFlash read and write processes since the C54x does not have two separate read and write strobes. Table 9 lists the I/O signals of the SN74LVC138A decoder.

Table 9. SN74LVC138A 3-Line to 8-Line Decoder/Demultiplexer Signal Description

Pin	I/O	Terminal Name	Description
1	I	A	Select Inputs
2	I	B	
3	I	C	
4	I	$\overline{\text{G2A}}$	Enable Inputs
5	I	$\overline{\text{G2B}}$	
6	I	G1	
7	O	Y7	Outputs
9	O	Y6	
10	O	Y5	
11	O	Y4	
12	O	Y3	
13	O	Y2	
14	O	Y1	
15	O	Y0	
8	N/A	GND	Ground
16	N/A	VCC	Vcc

In Table 9, the signals generated by the C54x for input to the decoder are designated as inputs and signals generated by the decoder for output to the CompactFlash are designated as outputs. The same signal convention applies for Table 10, which describes the truth table of the decoder. The Enable Inputs of the decoder are driven by VCC, GND, and $\overline{\text{IOSTRB}}$, and the Select Inputs are driven by A15, A14, and $\overline{\text{R/W}}$. Together, these signals generate the $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ signals for the CompactFlash whenever the C54x makes an I/O Space access with the PORTR (I/O port read) and PORTW (I/O port write) assembly mnemonics or the C language keyword 'iport'. See the C54x device-specific data sheet for I/O space read and write timing.

Table 10. SN74LVC138A 3-Line to 8-Line Decoder/Demultiplexer I/O

Function Table							
Enable Inputs			Select Inputs			Outputs	
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y4	Y5
VCC	\overline{IOSTRB}	GND	A15	A14	R/ \overline{W}	\overline{IOWR}	\overline{IORD}
X	1	X	X	X	X	1	1
1	0	0	1	0	0	0	1
1	0	0	1	0	1	1	0

I/O – Input/Output

X – Don't Care Term

All unspecified outputs do not apply and can be left unconnected.

To access the ATA Registers with the C54x, an access code is applied on lines A15–A0 of the C54x parallel address bus. Table 11 lists the access codes necessary to access the ATA Registers. Note that all C54x address lines that are not shown are don't care terms since those lines have been left unconnected. For convenience, A13 is held at logic one and all other don't care terms held at logic zero. Note that lines A15 and A14 are inputs to the decoder and used to generate the \overline{IORD} and \overline{IOWR} signals.

Table 11. ATA Register Addresses

Addresses								Functions	
A15–A0	A15	A14	A12 ($\overline{CS1}$)	A11 ($\overline{CS0}$)	A2	A1	A0	\overline{IORD}	\overline{IOWR}
Control Block Registers									
0xA806	1	0	0	1	1	1	0	Alternate Status Register	Control Register
0xA807	1	0	0	1	1	1	1	Drive Address Register	Reserved
Command Block Registers									
0xB000	1	0	1	0	0	0	0	Data Register	Data Register
0xB001	1	0	1	0	0	0	1	Error Register	Features Register
0xB002	1	0	1	0	0	1	0	Sector Count Register	Sector Count Register
0xB003	1	0	1	0	0	1	1	Sector Number Register	Sector Number Register
0xB004	1	0	1	0	1	0	0	Cylinder Low Register	Cylinder Low Register
0xB005	1	0	1	0	1	0	1	Cylinder High Register	Cylinder High Register
0xB006	1	0	1	0	1	1	0	Drive/Head Register	Drive/Head Register
0xB007	1	0	1	0	1	1	1	Status Register	Command Register
0xA000	1	0	0	0	X	X	X	Invalid	Invalid

All address lines not shown are don't care terms

The XF signal from the C54x is connected to $\overline{\text{RESET}}$ on the CompactFlash to issue a hardware reset to the CompactFlash. The RSBX assembly mnemonic drives XF low to assert the $\overline{\text{RESET}}$ signal, and SSBX drives XF high to deassert the $\overline{\text{RESET}}$ signal. Recall from Table 1 that $\overline{\text{RESET}}$ must be asserted for at least 25 us to reset the CompactFlash.

The $\overline{\text{BIO}}$ pin is used in conjunction with an OR gate, the CompactFlash card detect pins ($\overline{\text{CD1}}$ and $\overline{\text{CD2}}$), and two pull-up resistors to determine whether or not the CompactFlash is properly inserted in its socket. Recall from Table 1 that $\overline{\text{CD1}}$ and $\overline{\text{CD2}}$ are grounded on the CompactFlash Card. As long as the CompactFlash is properly inserted in its socket, the card detect pins will drive the lines to the OR gate low and cause the gate to output a low signal to the $\overline{\text{BIO}}$ pin. If the CompactFlash is not properly inserted in its socket, one or both of the inputs to the OR gate will be high and cause the OR gate to output a high signal to the $\overline{\text{BIO}}$ pin. The status of $\overline{\text{BIO}}$ is polled in the CF_Present function. See Section 4.2 and the source code for more details on the CF_Present function. A high signal on $\overline{\text{BIO}}$ implies that the CompactFlash is not properly inserted or not present in its socket, while a low signal on $\overline{\text{BIO}}$ implies that the CompactFlash is properly inserted in its socket. Refer to Table 12 for the CompactFlash card detection truth table and to Figure 21 for a visual on this connection.

Table 12. CompactFlash Card Detection Truth Table

$\overline{\text{CD1}}$	$\overline{\text{CD2}}$	$\overline{\text{BIO}}$	
0	0	0	Card Properly Inserted
0	1	1	Card Not Properly Inserted
1	0	1	Card Not Properly Inserted
1	1	1	Card Not Properly Inserted

$\overline{\text{ATASEL}}$ is tied to GND to permanently enable True IDE Mode operation, and $\overline{\text{CSEL}}$ is tied to GND to configure the CompactFlash card as card (drive) 0.

Some CompactFlash signals are not used while operating in True IDE Mode. As recommended by the CompactFlash Memory Card Product Manual, $\overline{\text{REG}}$ and $\overline{\text{WE}}$ are tied to VCC and A3–A10 are tied to ground. A3–A10 and A13 on the C54x address bus are not used and left unconnected.

Some CompactFlash signals are not essential in the CompactFlash to C54x interface. $\overline{\text{IOCS16}}$, $\overline{\text{CD2}}$, VS1, INTRQ, VS2, IORDY, $\overline{\text{INPACK}}$, $\overline{\text{DASP}}$, and $\overline{\text{PDIAG}}$ on the CompactFlash are not used and left unconnected. Note that because INTRQ is left unconnected, the CompactFlash to C54x interface implemented in this document does not use interrupts from the CompactFlash during read and write processes. Rather, the DRQ bit is polled to indicate whether or not the CompactFlash is ready for data transfer.

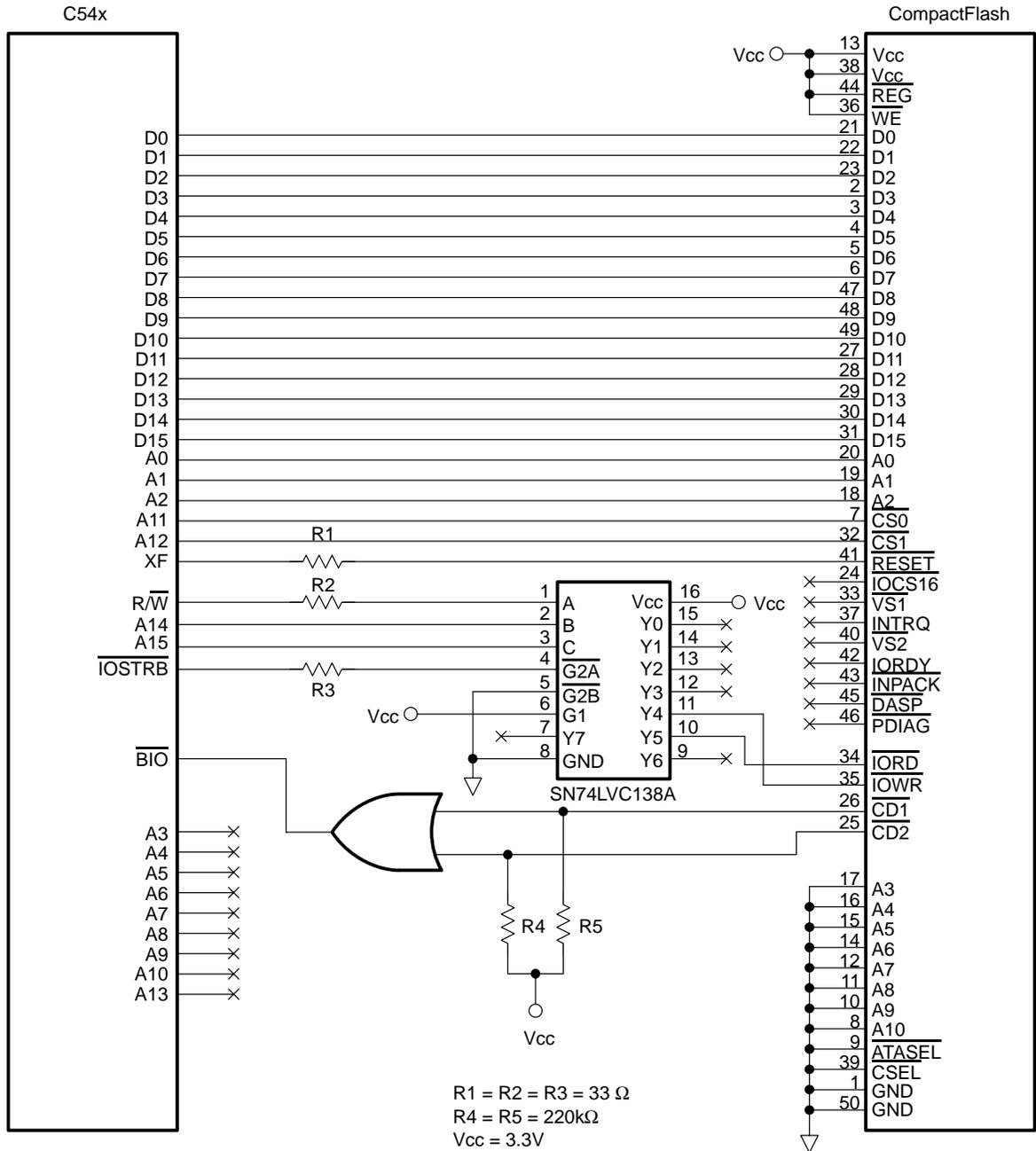


Figure 21. CompactFlash Interface to the C54x Schematic

4.2 Software Interface

This section describes the set of routines used to access the CompactFlash Memory Card. LBA mode addressing is the addressing scheme used in these functions. The source code is available electronically from the TI web site.

void CF_CheckReadyStatus()

Purpose: To determine if the CompactFlash is ready to perform card operations. This routine reads the Status Register, checks the BUSY bit, and waits for the RDY bit to be set. If ERR is set, the Error Register is read. If the routine times out, RDYTimeOut is set and the program is aborted.

Variables Modified: RDYTimeOut if the routine times out

Variables Accepted: None

Returns: Nothing

void CF_CheckBusyStatus()

Purpose: This routine reads the Status Register and waits for the BUSY bit to be cleared. If the routine times out, BUSYTimeOut is set and the program is aborted.

Variables Modified: BUSYTimeOut if the routine times out

Variables Accepted: None

Returns: Nothing

void CF_CheckDrqStatus()

Purpose: To determine if the CompactFlash is ready for data transfer. The Status Register is read until the DRQ bit is set. If the routine times out, DRQTimeOut is set and the program is aborted.

Variables Modified: DRQTimeOut if the routine times out

Variables Accepted: None

Returns: Nothing

void CF_CheckErrorStatus()

Purpose: This routine reads the Status Register and determines if any errors have occurred. If ERR is set, the Error Register is read, saved in ErrorSt, and the program is aborted.

Variables Modified: ERR, ErrorSt if an error has occurred

Variables Accepted: None

Returns: Nothing

void CF_HardwareReset()

Purpose: To issue a hardware reset to the CompactFlash

Variables Modified: None

Variables Accepted: None

Returns: Nothing

void DSP_Init()

Purpose: To initialize the C54x DSP and enable the EMIF.

Variables Modified: None

Variables Accepted: None

Returns: Nothing

void CF_IssueCommand(unsigned long PhysicalSector, unsigned short SectorCount, unsigned short Command)

Purpose: To issue commands to the CompactFlash. This routine initializes the Sector Count, Sector Number, Cylinder High/Low, Card/Head, and Command Registers.

Variables Modified: None

Variables Accepted: PhysicalSector – desired LBA
SectorCount – number of sectors to transfer
Command – command to execute

Returns: Nothing

void CF_IdentifyDrive()

Purpose: To issue the Identify Drive command and read the parameter information from the CompactFlash.

Variables Modified: ReadBuffer[255]

Variables Accepted: None

Returns: Nothing

int CF_Present()

Purpose: This routine polls the BIO pin to determine if the CompactFlash is properly inserted in its socket.

Variables Modified: None

Variables Accepted: None

Returns: int; 1 = CF present, 0 = CF not present

void ReadCF(unsigned long PhysicalSector, unsigned short SectorCount)

Purpose: To read from the CompactFlash.
Variables Modified: XferSectors, ReadBuffer[255]
Variables Accepted: PhysicalSector – desired LBA
SectorCount – number of sectors to transfer
Returns: Nothing

void WriteCF(unsigned long PhysicalSector, unsigned short SectorCount)

Purpose: To write to the CompactFlash.
Variables Modified: XferSectors
Variables Accepted: PhysicalSector – desired LBA
SectorCount – number of sectors to transfer
Returns: Nothing

5 Conclusion

This application note describes how to interface a C54x DSP to a CompactFlash Memory Card in True IDE Mode. A complete reference design is shown, including hardware and software interfaces. The software consists of a set of file system independent subroutines required to store and retrieve information from the CompactFlash and is available electronically from the TI web site. Although this document specifically describes a C54x to CompactFlash interface, the hardware and software can be easily adapted to function with the C55x generation of DSPs.

6 References

1. *AT Attachment Interface for Disk Drives*. Reference No. ANSI X3.221 – 199x
2. *CompactFlash Memory Card Product Manual*. Lit. No. 20-1—00038 Rev. 7 4/2000.
<http://www.sandisk.com>
3. *TMS320C54x DSP CPU Reference Guide* (SPRU131)
4. *SN54LVC138A, SN74LVC138A 3-Line to 8-Line Decoders/Demultiplexers Data Sheet* (SCAS291I)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265