K2G ICE EVM

V 1.0

- See the Hardware Implementation Document for Design Details
- See the Hardware User Guide for Board Details
- See the PCB Build Specification for PCB Design Details

Project :
K2GICE
PROC022

Designed for TI by Mistral Solutions Pvt Ltd

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR
0.1	10th FEB 2017	R501 DNI'd from BOOTCMPLT signal (Page 06) Part number updated for Screws H9-H12 with RoHS and REACH compliant parts (Page 29) Part number updated for Screws H13-H16 with RoHS and REACH compliant parts (Page 29)	Mistral Design Team
0.2	8th MAR 2017	Power Cord H20 removed from Kit Content	Mistral Design Team
1.0	8th MAR 2017	Baselined for Production RevD	Mistral Design Team

Project :
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PROC022

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Texas Instruments

MISTRAL

Title	REVISION HISTORY		
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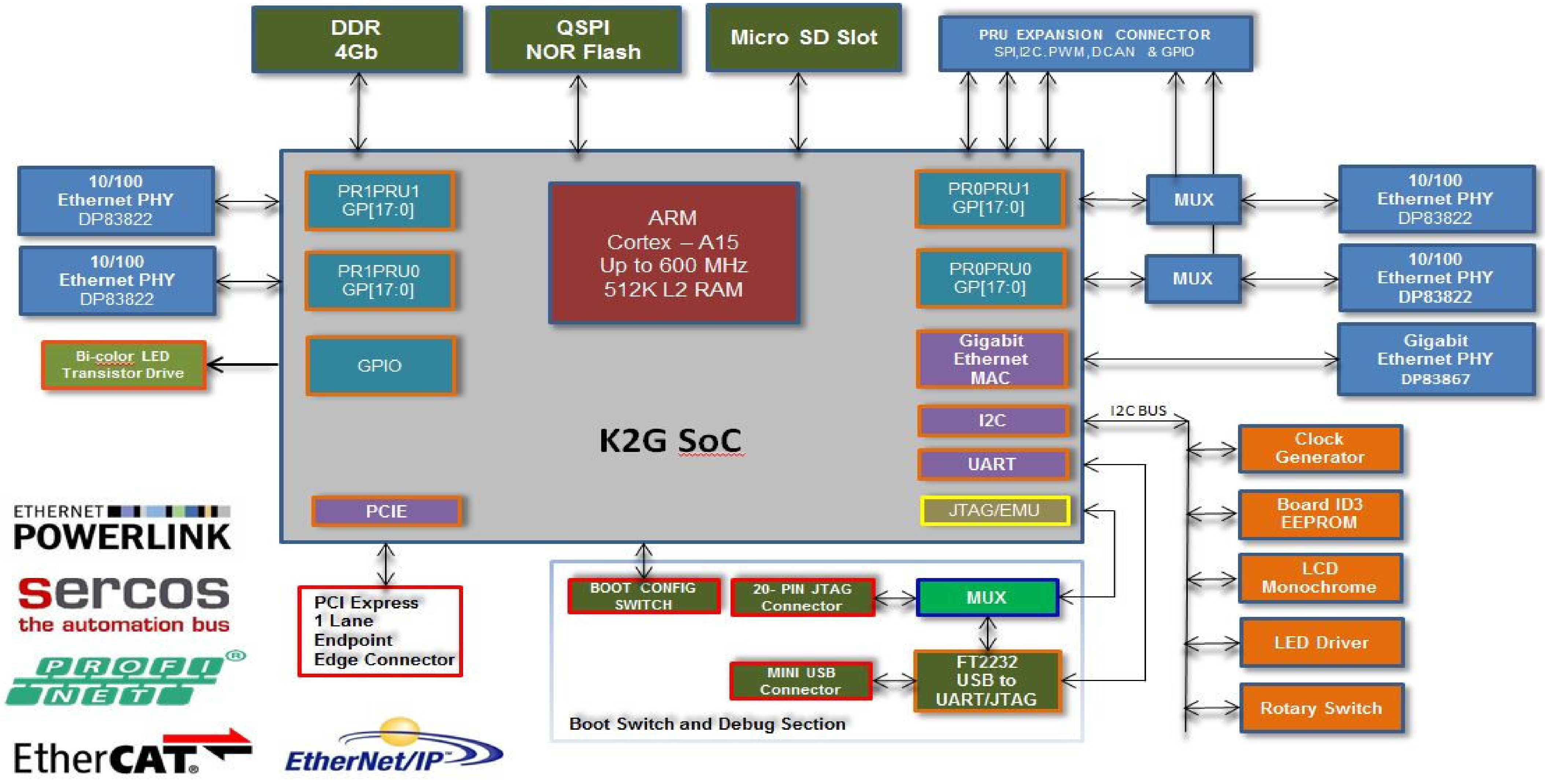
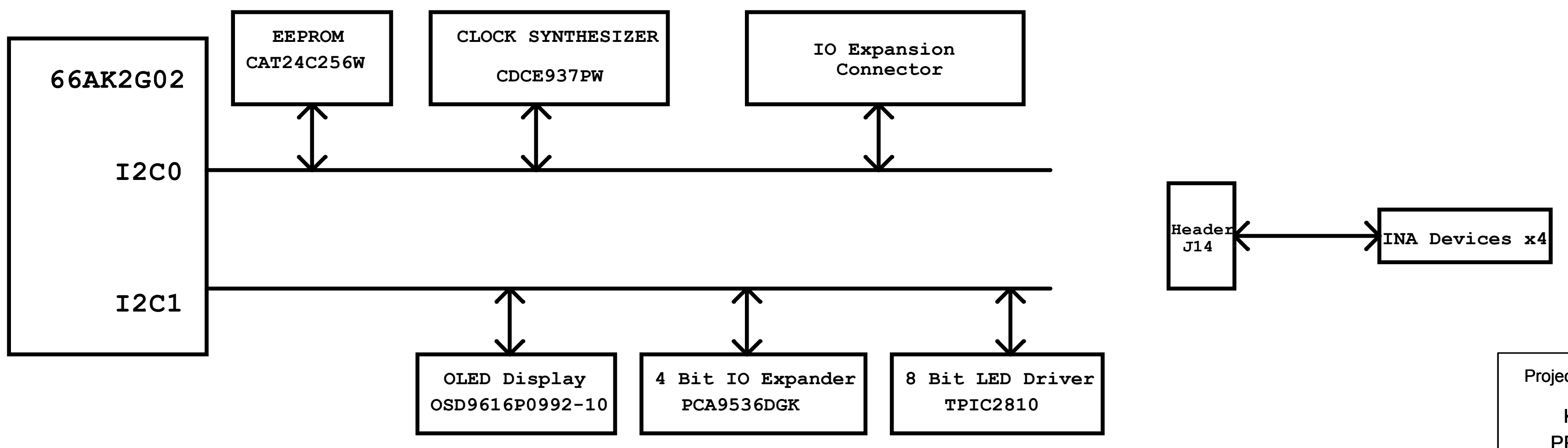
K2G ICE - *INDUSTRIAL COMMUNICATION ENGINE*
SYSTEM BLOCK DIAGRAM



I2C TREE



I2C ADDRESS TABLE

I2C DEVICES	7 BIT ADDRESS
EEPROM	0x50
OLED Display	0x3C
INA Devices	0x40 ,0x41, 0x43, 0x44
4 Bit IO Expander	0x41
8 Bit LED Driver	0x6x
CLOCK SYNTHESIZER	0x6D

Project :
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Title	BLOCK DIAGRAM & I2C TREE	
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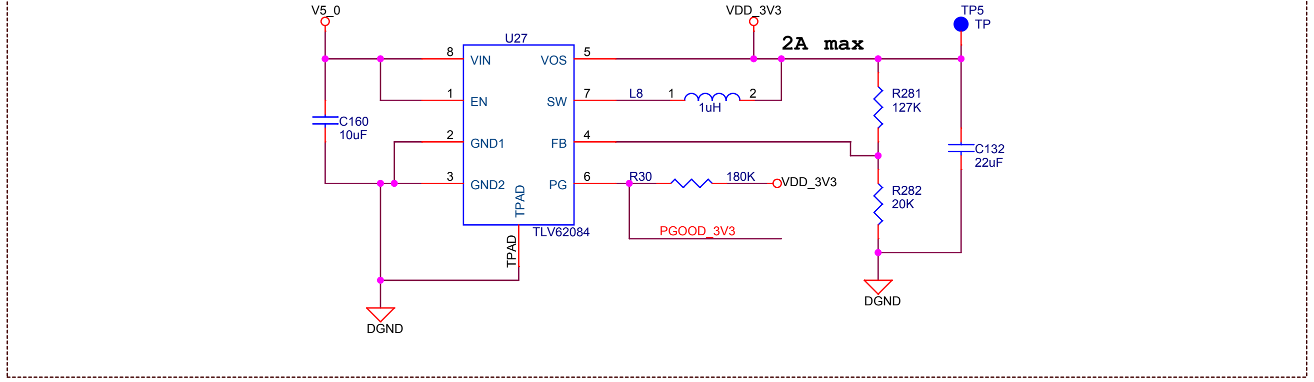
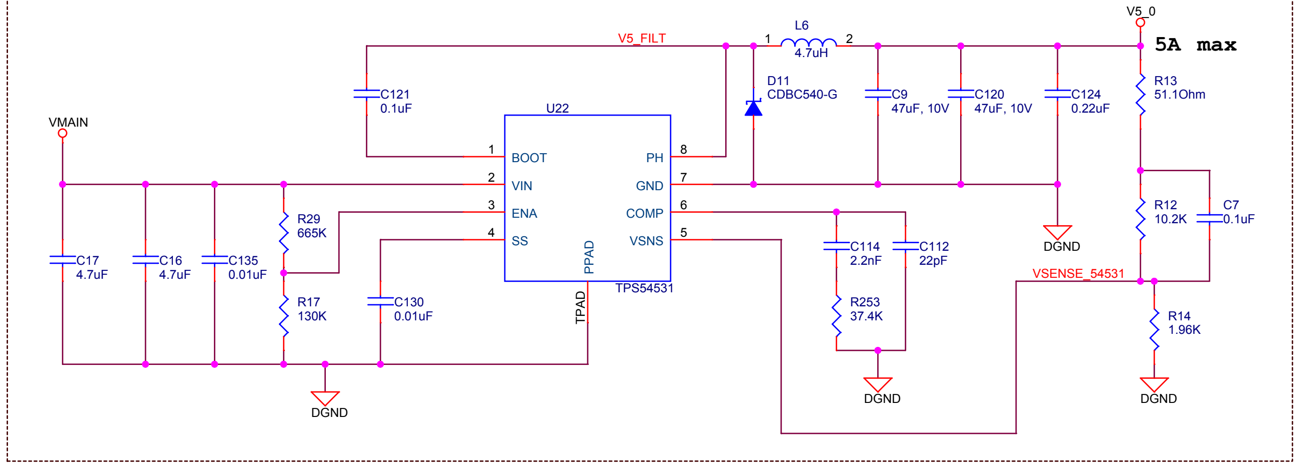
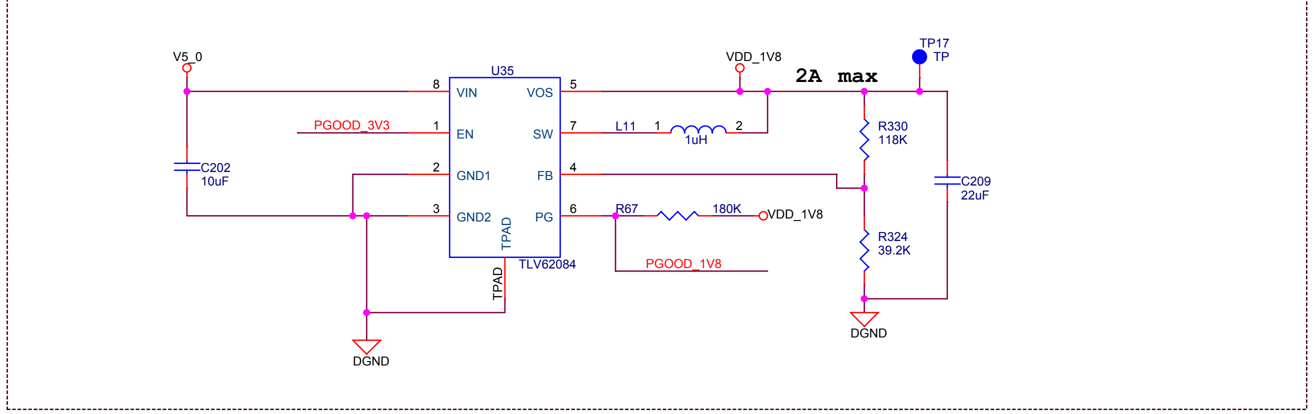
3.3V Power Generation



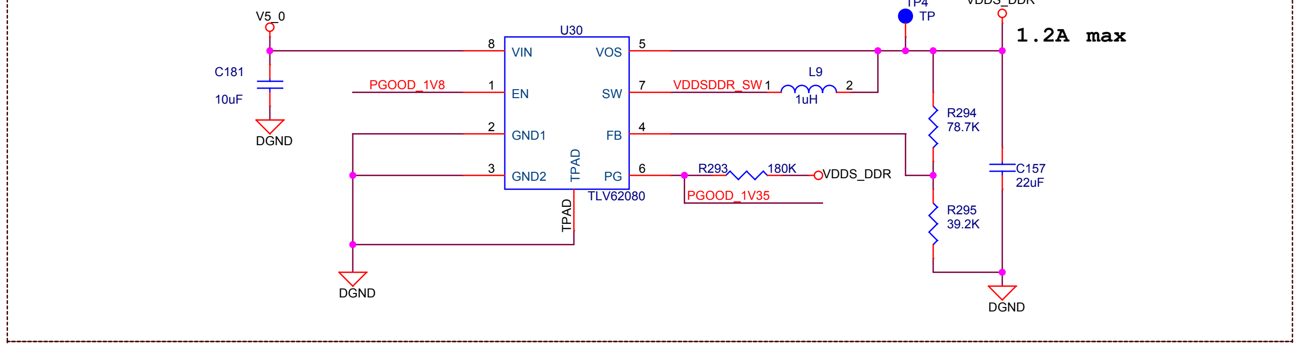
24V - 5V Power Generation



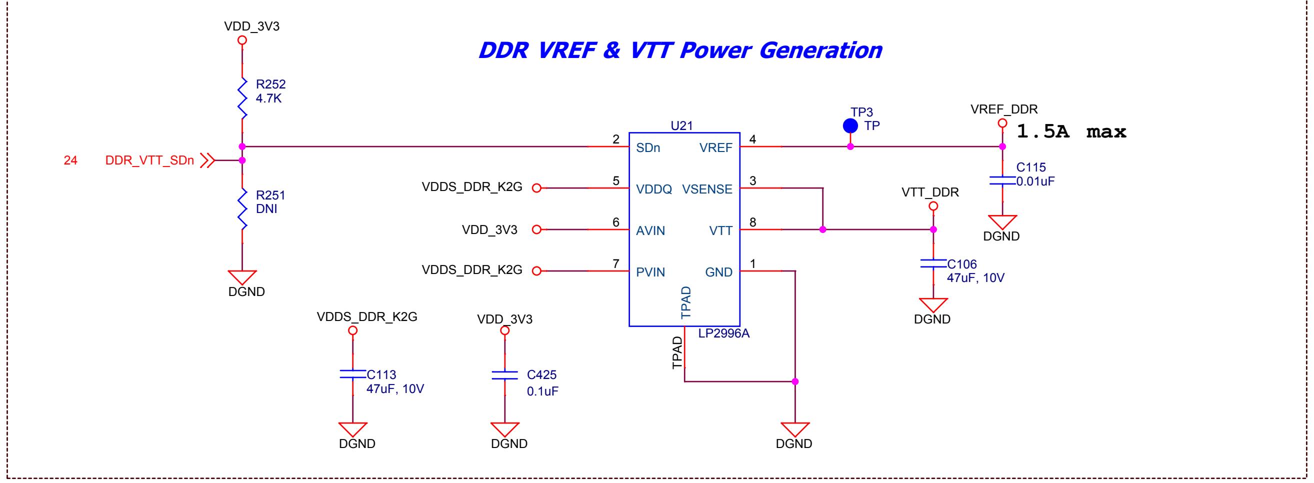
1.8V Power Generation



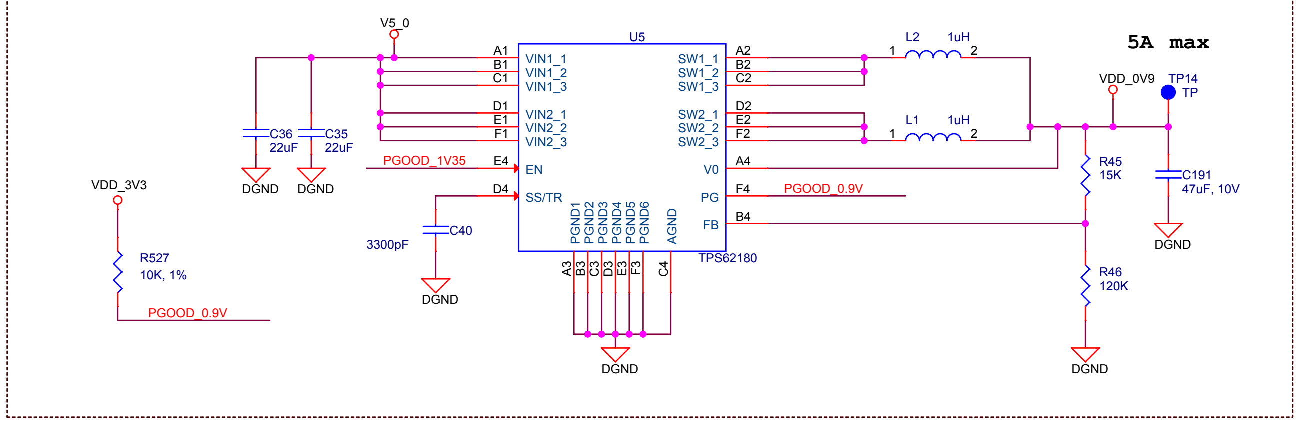
DDR3L 1.35V Power Generation



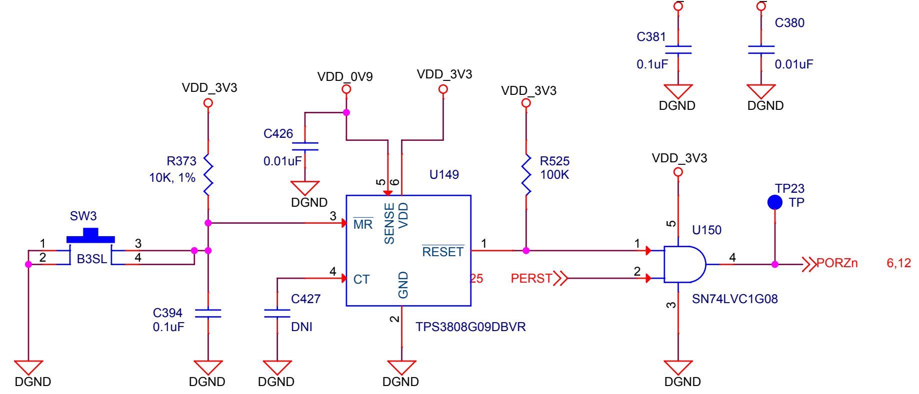
DDR VREF & VTT Power Generation



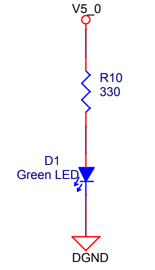
0.9V Power Generation



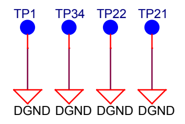
Power On Reset



Power On LED



GROUND PROBING POINTS



Project :

K2GICE
PROC022

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TEXAS INSTRUMENTS

MISTRAL

Title	POWER SUPPLY 1	
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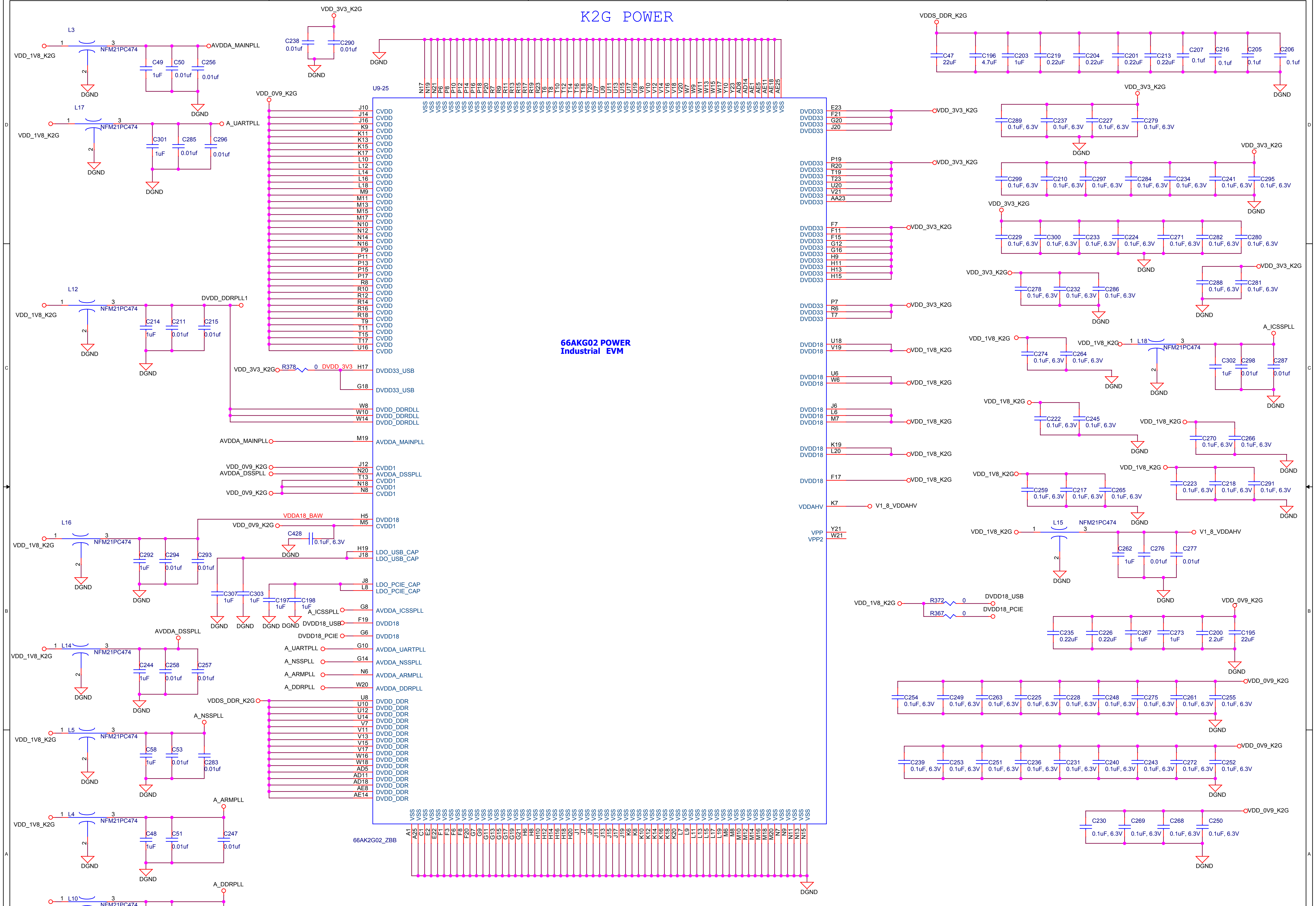
K2G POWER



Project :

K2GICE
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Designed for TI by Mistral Solutions Pvt Ltd

TEXAS INSTRUMENTS

MISTRAL

Title	POWER SUPPLY 2	
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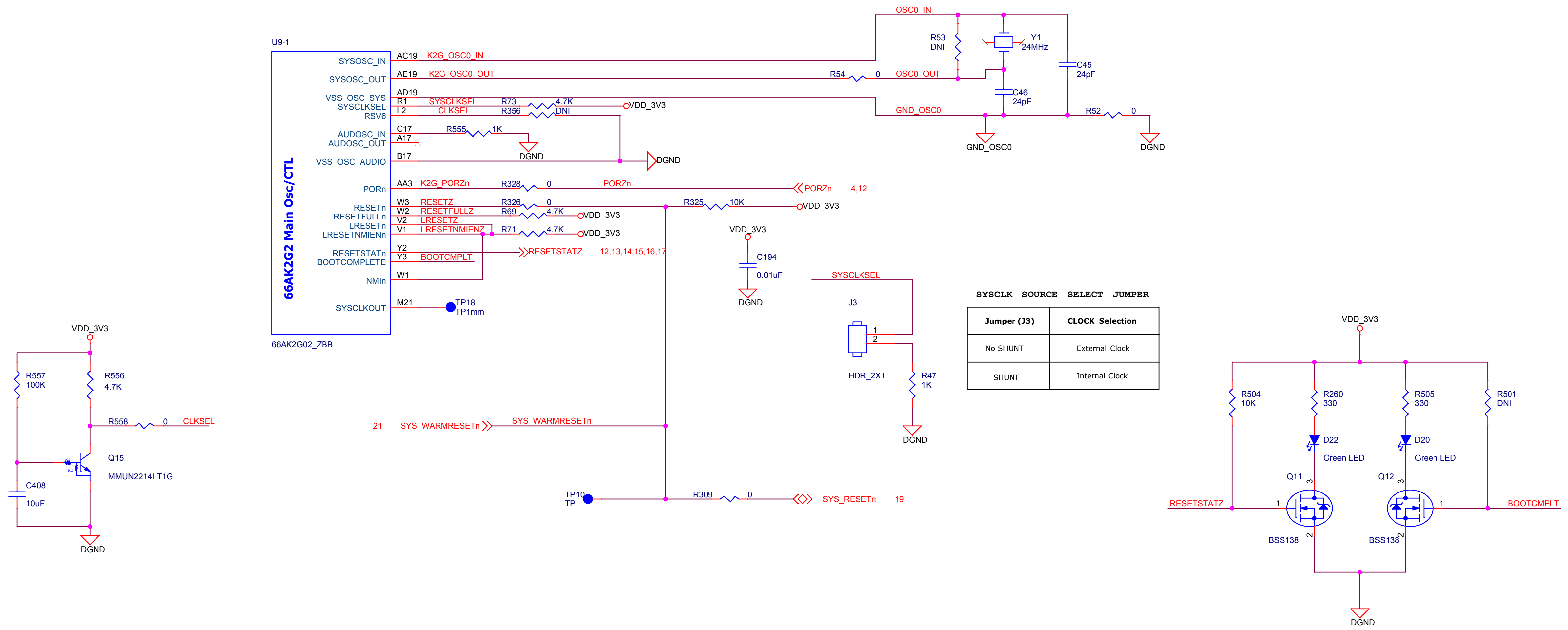
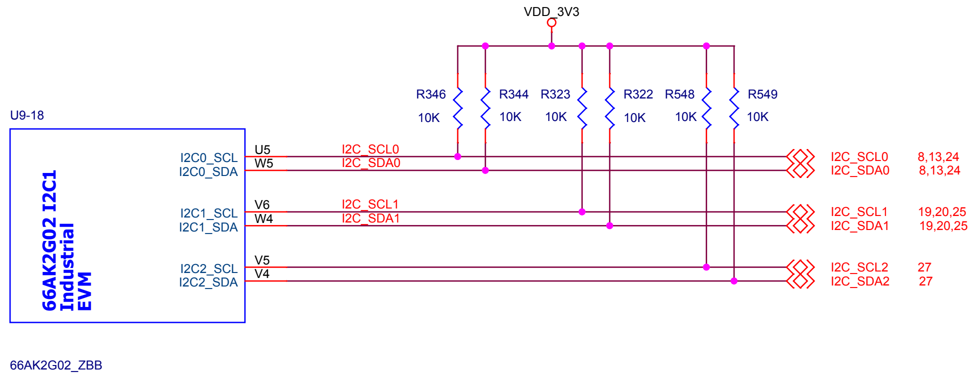
K2G CLOCK & RESET



SYSCLK SOURCE SELECT JUMPER

Jumper (J3)	CLOCK Selection
No SHUNT	External Clock
SHUNT	Internal Clock

I2C



Project :

K2GICE
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Title	SYSTEM_CLOCK_RESET_I2C	
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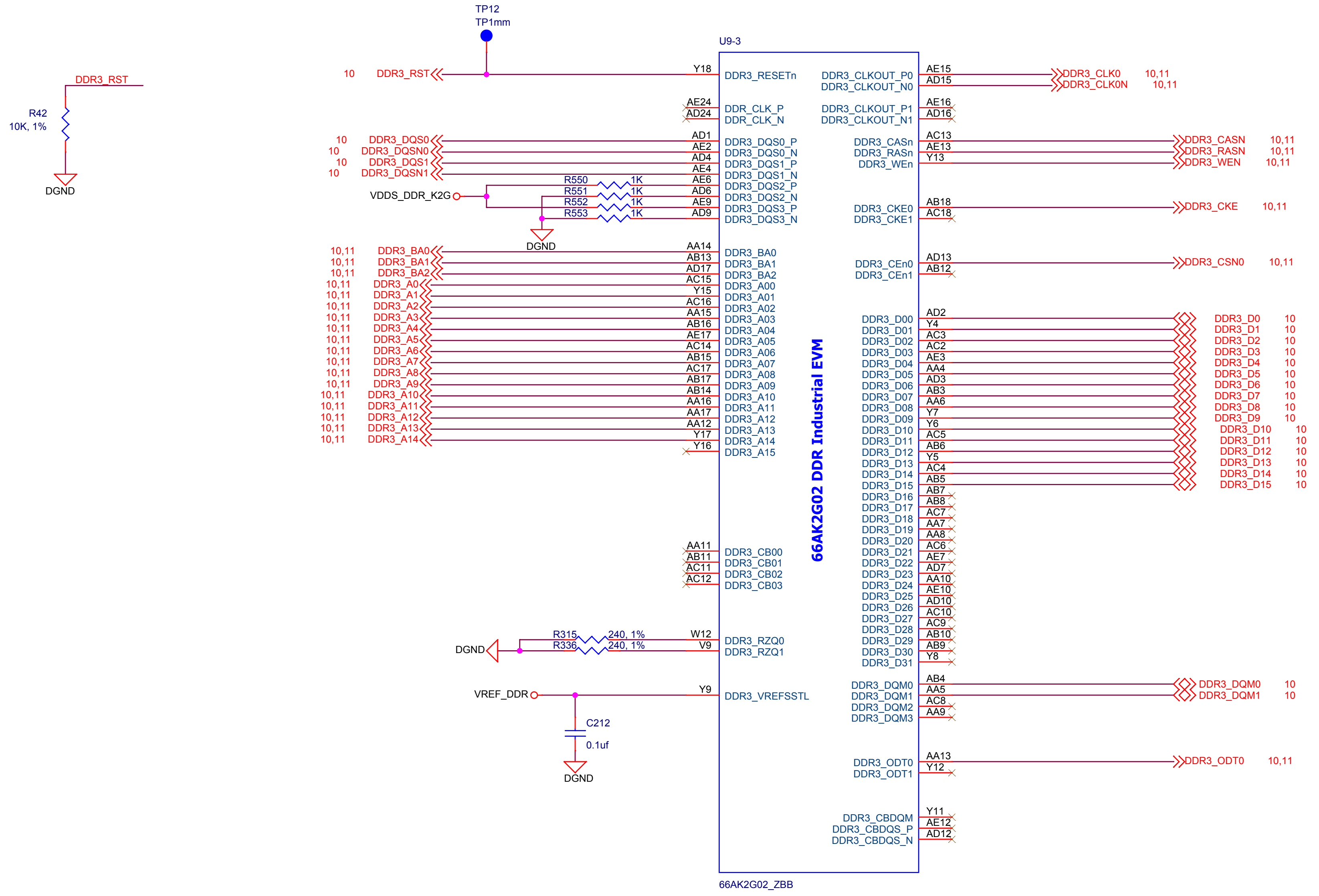
DDR3L INTERFACE



Project :

K2GICE
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Title	DDR_INTERFACE	
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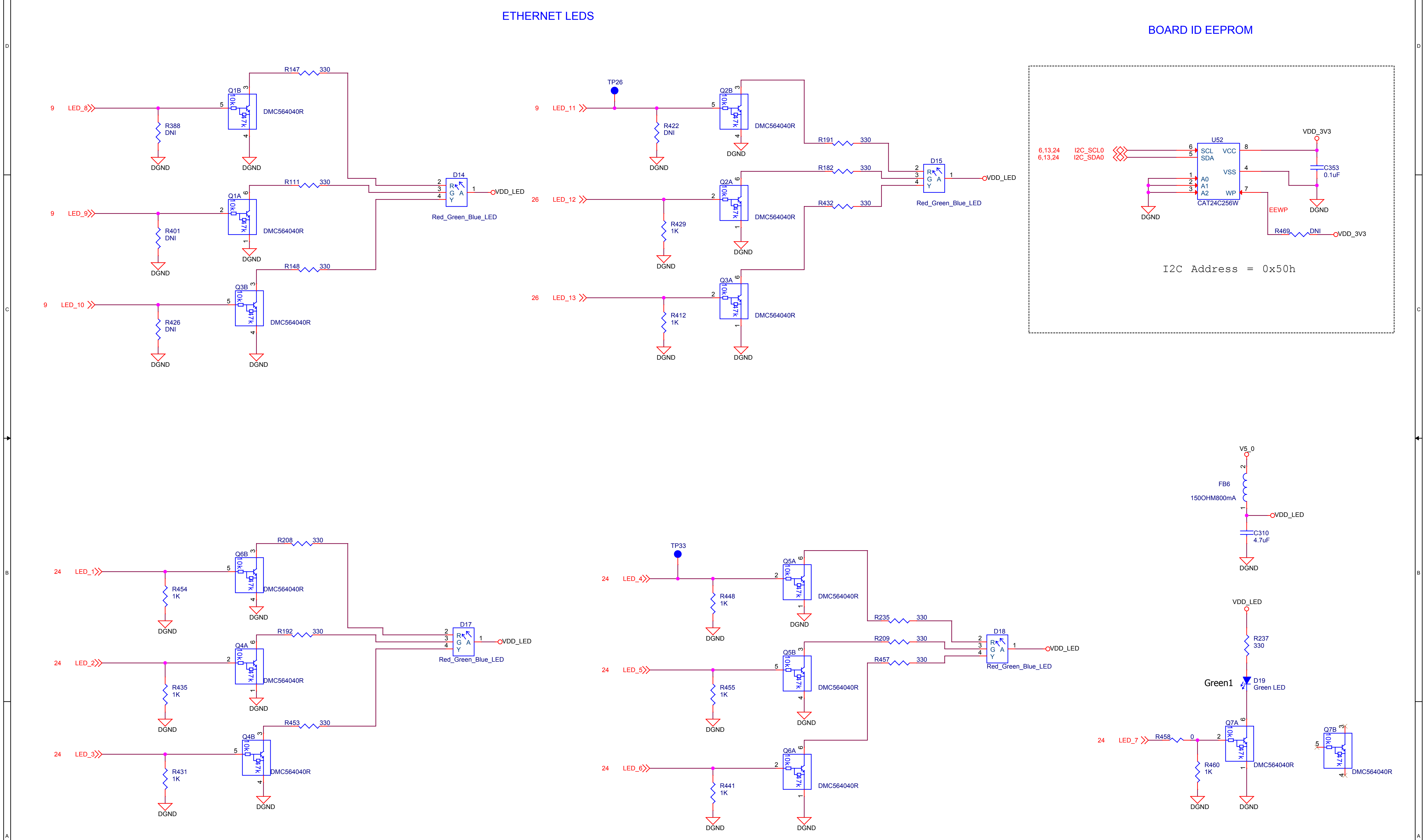

Project : K2GICE PROC022	Designed for TI by Mistral Solutions Pvt Ltd	Title	EEPROM_ETHERNETLEDS
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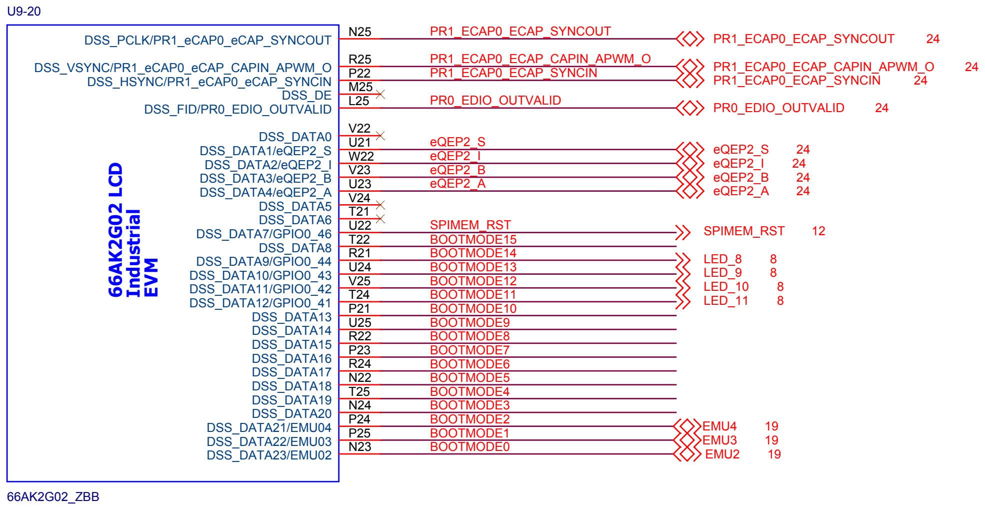
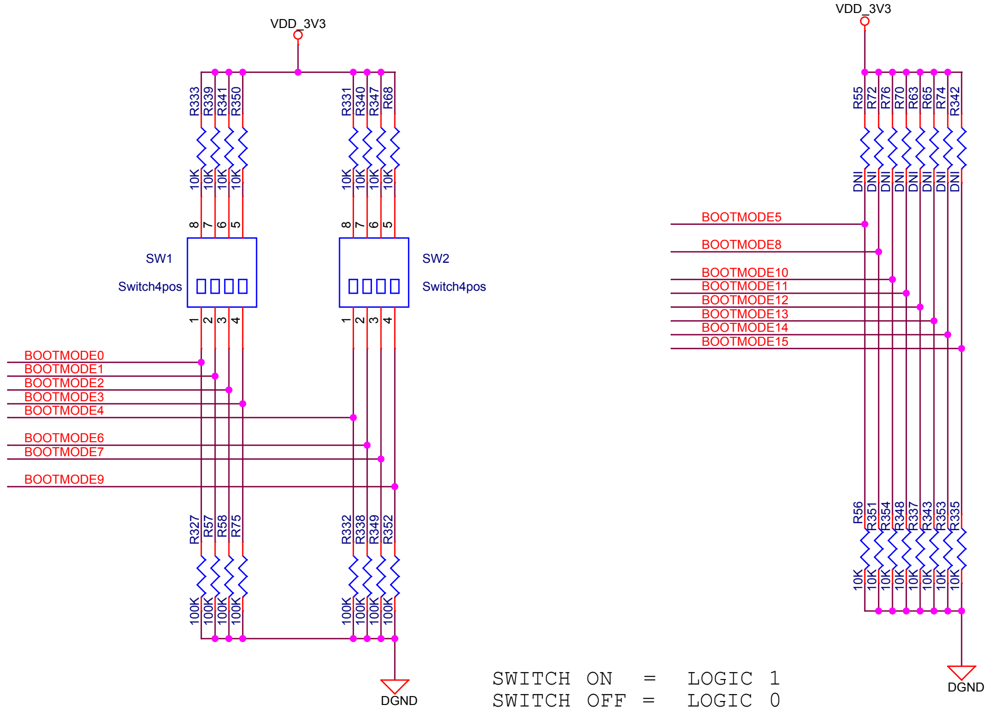


BOOT CONFIGURATION SETTINGS



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

BOOT MODES SUPPORTED

1. QSPI48
2. QSPI96
3. SD CARD
4. EMULATOR
5. PCIe

Project :

K2GICE
PROC022

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TEXAS INSTRUMENTS

MISTRAL

Title	BOOT SETTINGS	
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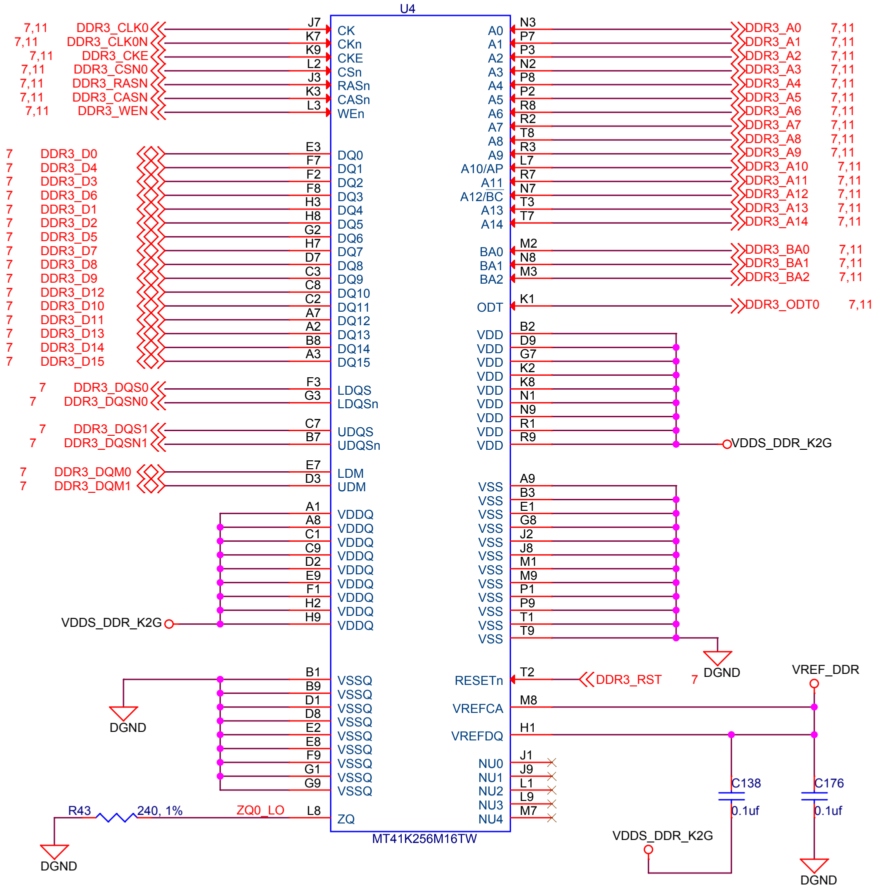
DDR3L



Project :

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TEXAS INSTRUMENTS

MISTRAL

Title DDR3L

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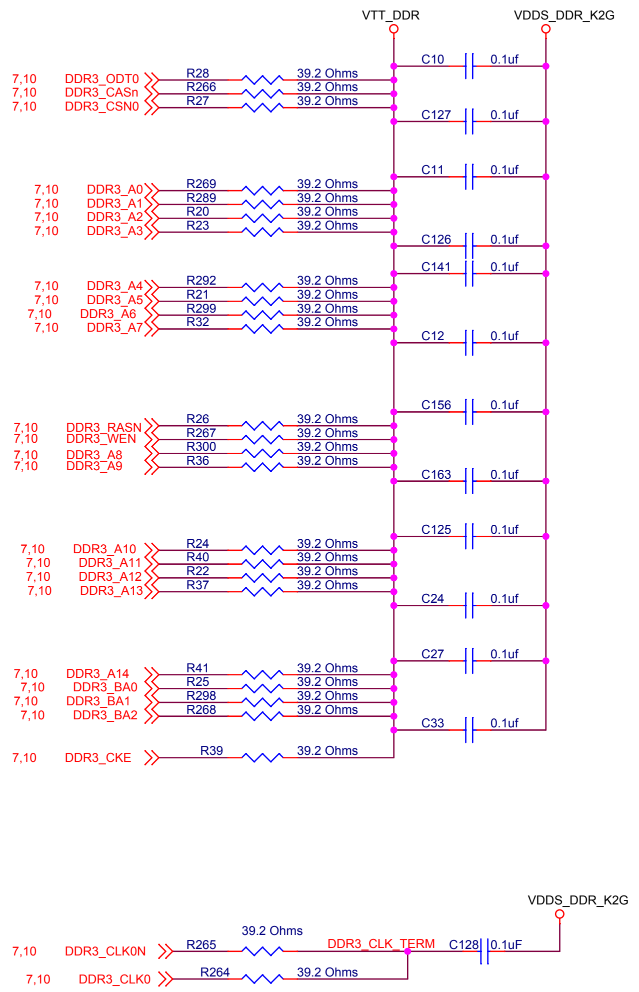
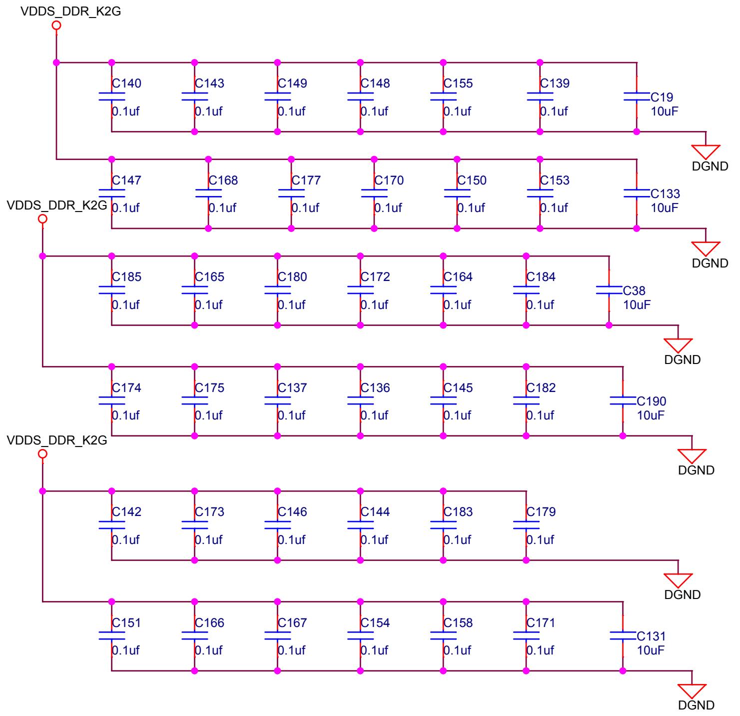
DDR3 SECTION TERMINATIONS



DDR3 SECTION DE-CAPS



Project :
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Title DDR3L DECAPS & TERMINATIONS
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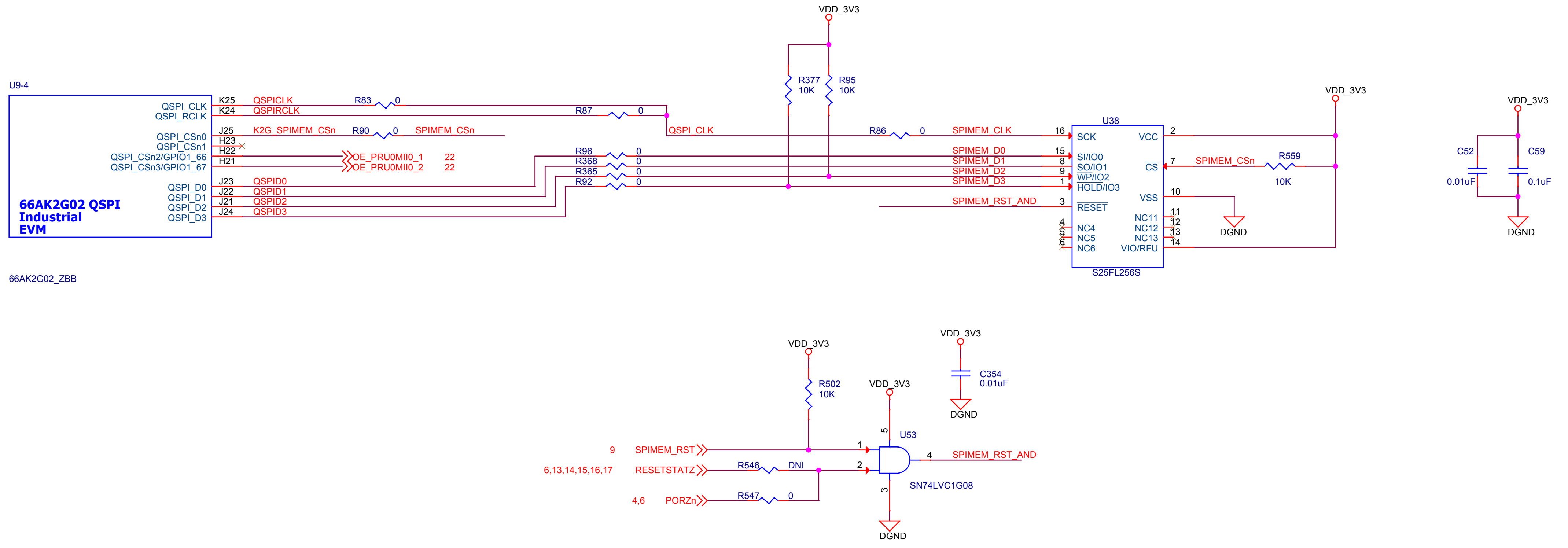
QSPI Flash



Project :

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Title	QSPI_FLASH	
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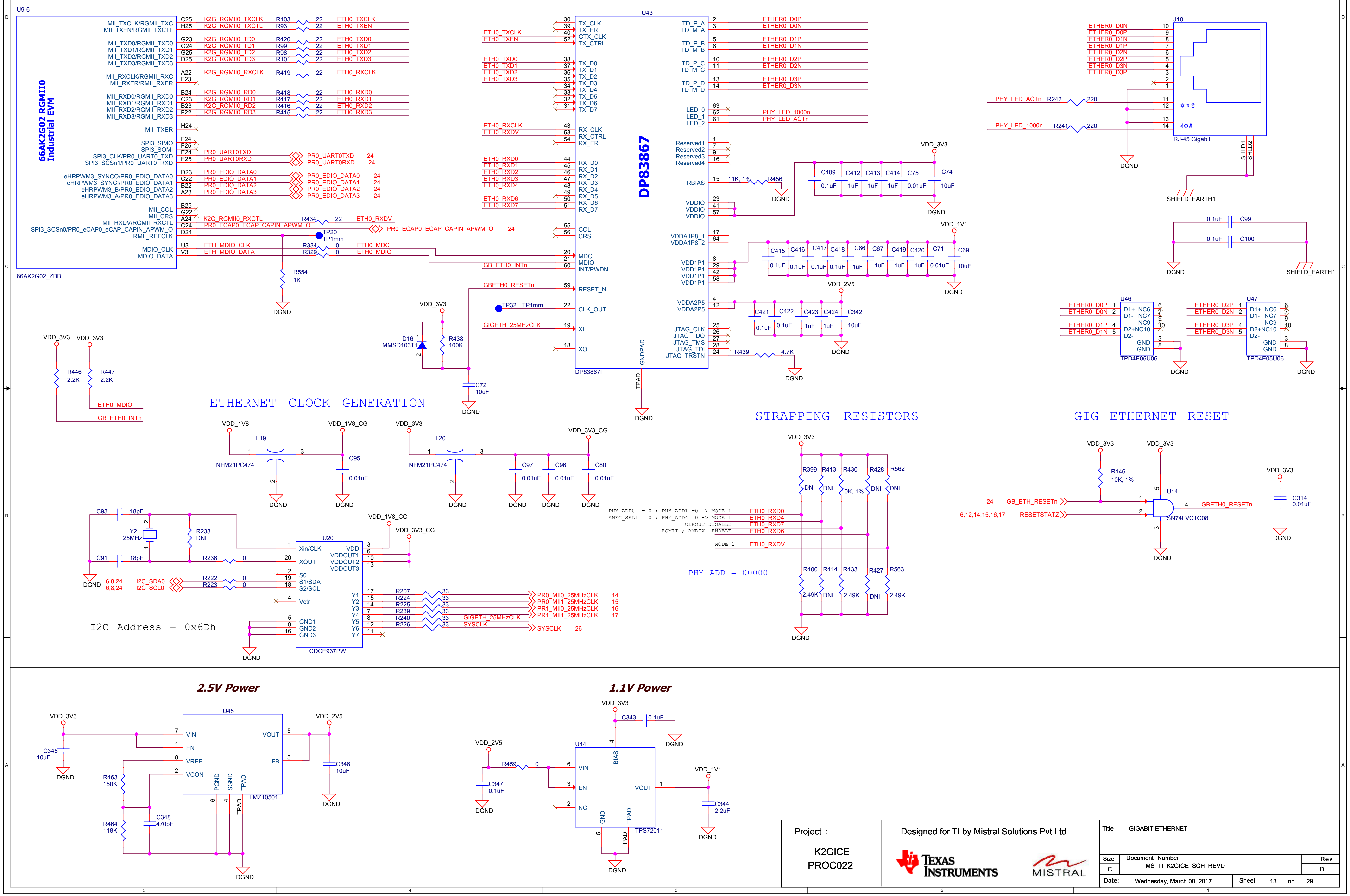
GIGABIT ETHERNET



Project :

K2GICE
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Title GIGABIT ETHERNET

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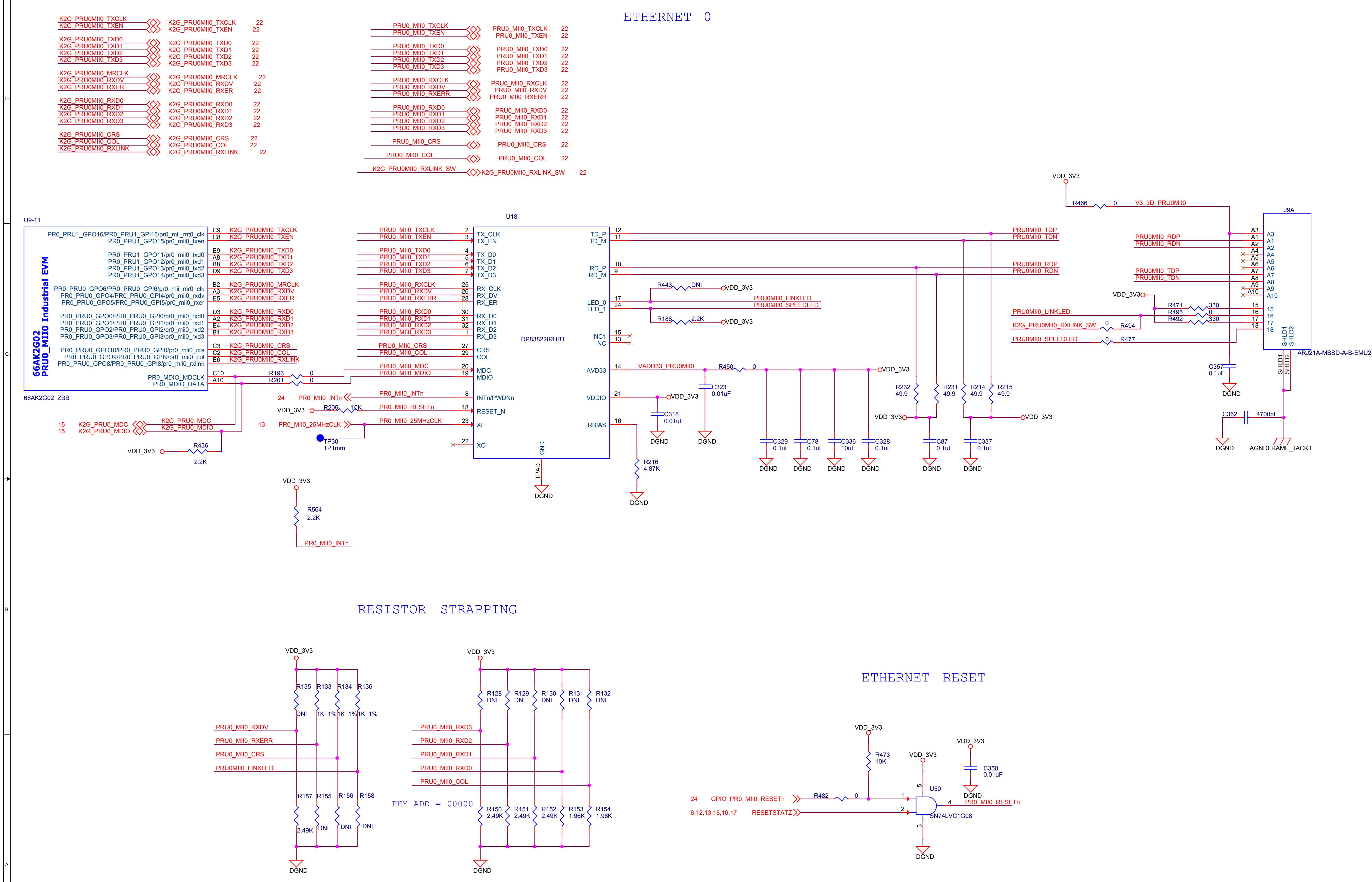

Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title PRU0MII0_Ethernet 0
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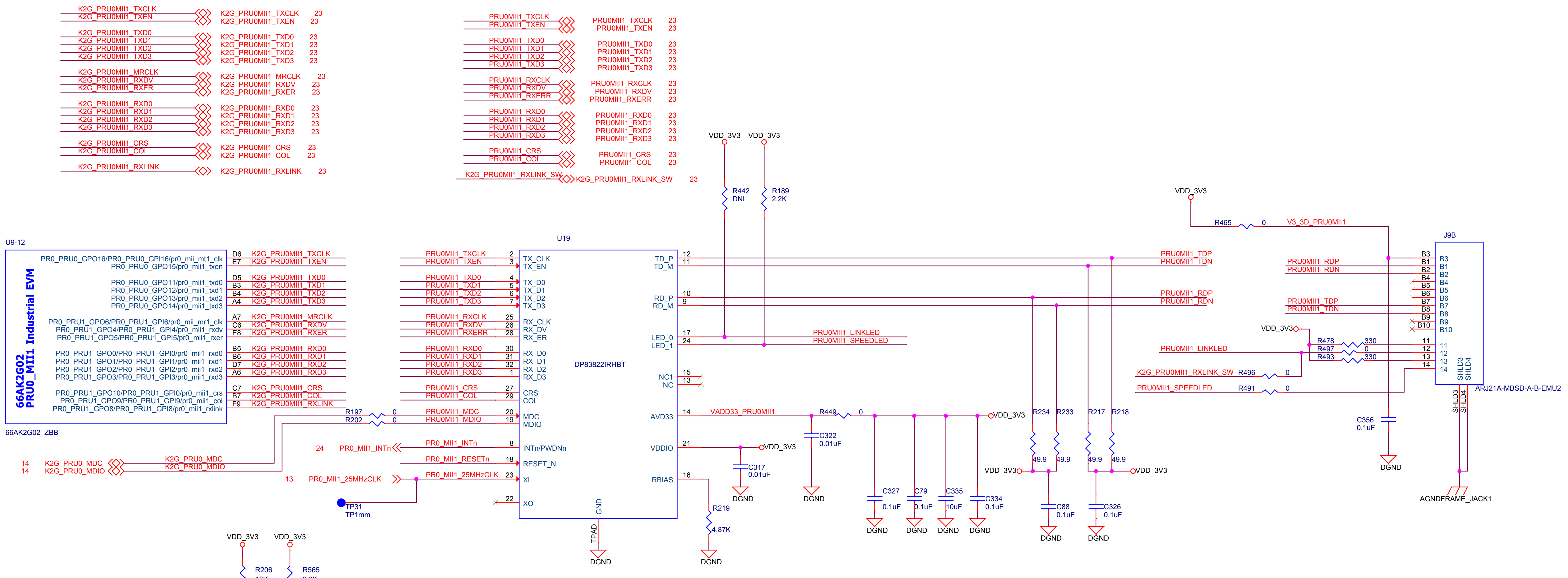
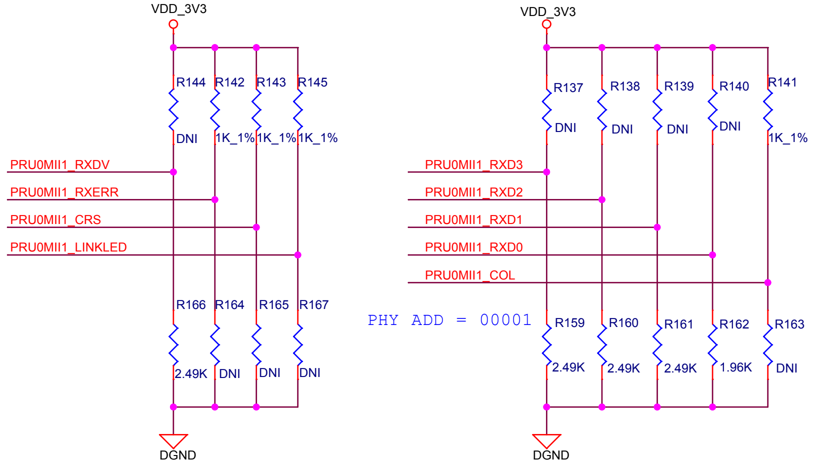
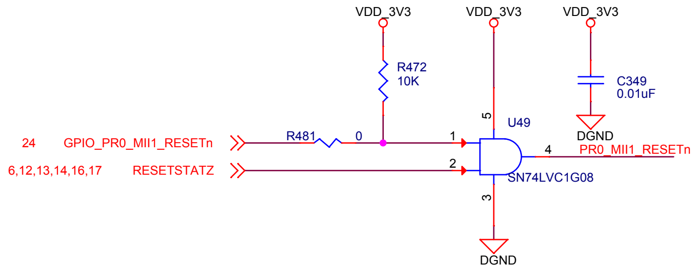
ETHERNET 1





RESISTOR STRAPPING

ETHERNET RESET



Project :

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TEXAS INSTRUMENTS
MISTRAL

Title	PRU0MII1_Ethernet 1		
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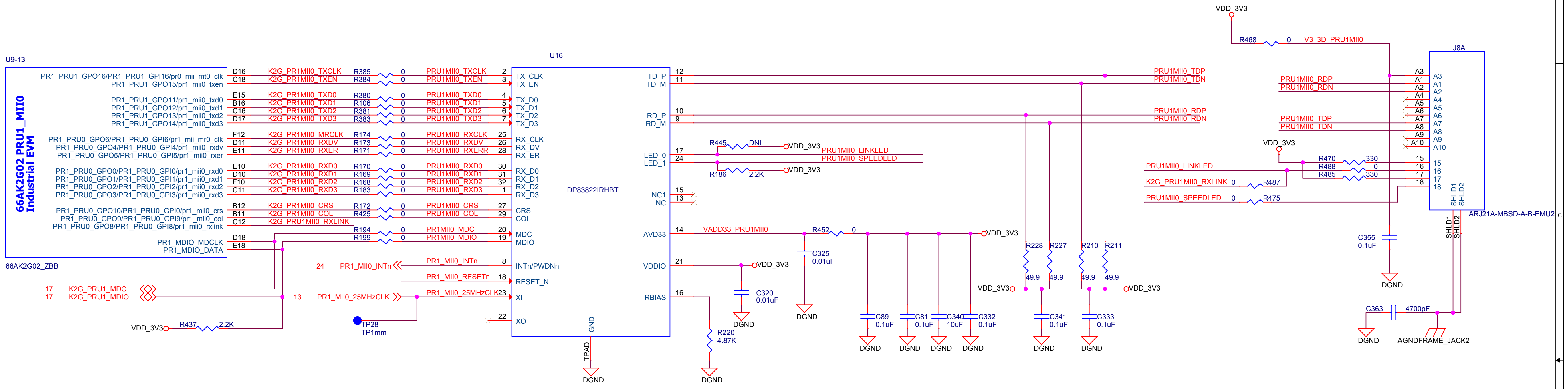
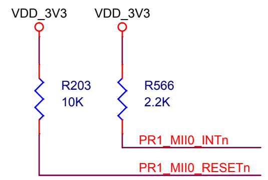
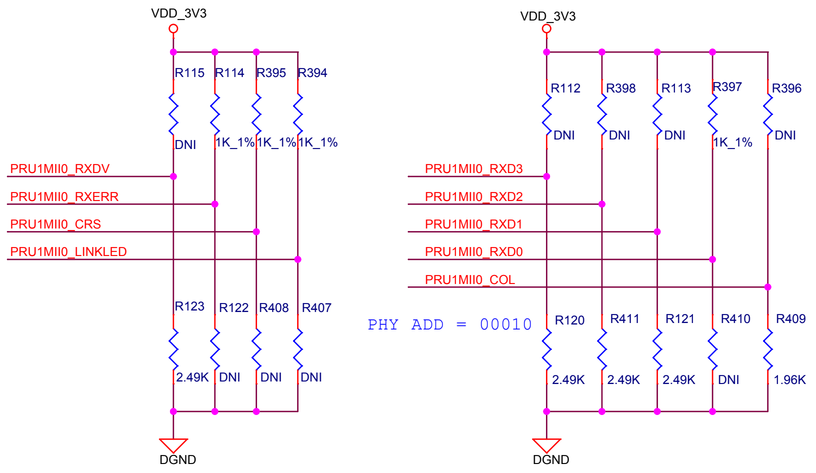
ETHERNET 2

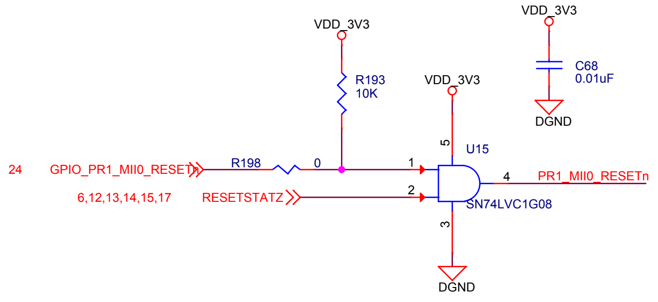




RESISTOR STRAPPING



ETHERNET RESET



Project :

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TEXAS INSTRUMENTS MISTRAL

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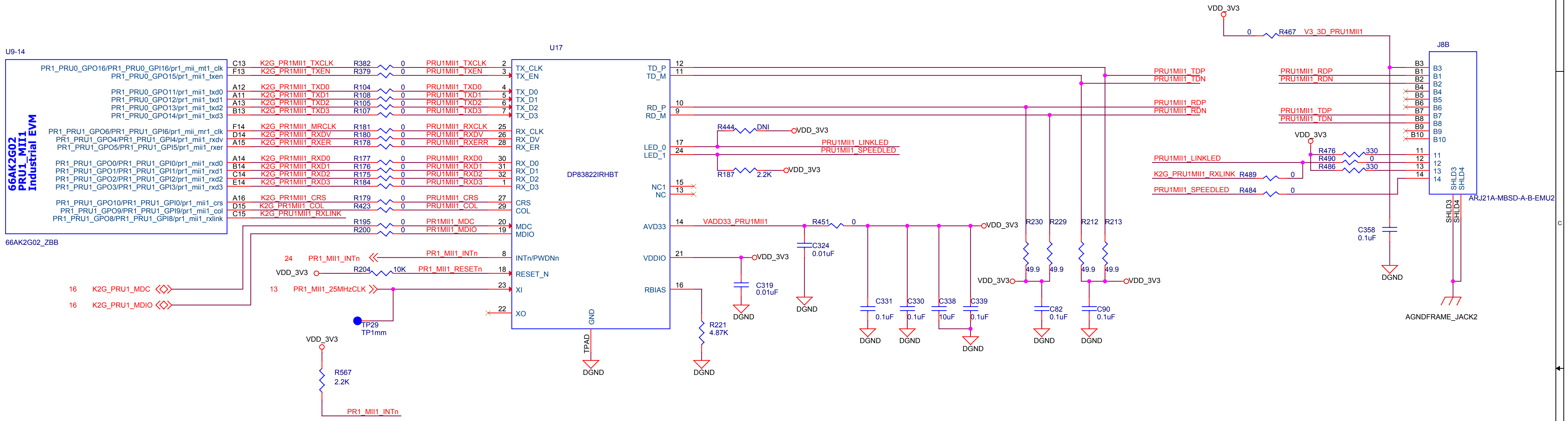
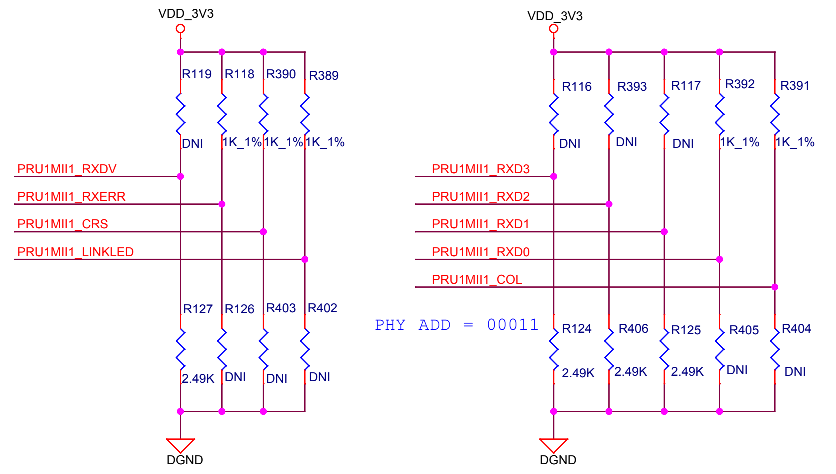
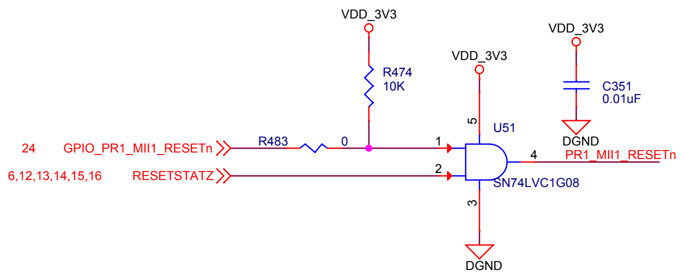
ETHERNET 3



RESISTOR STRAPPING



ETHERNET RESET



Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title PRU1MII1_Ethernet 3
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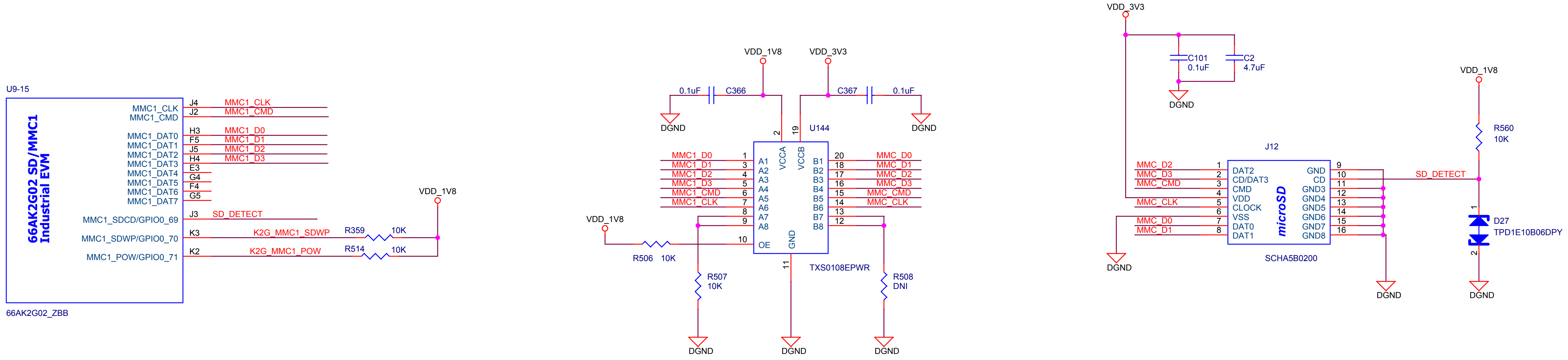
SD/MMC1 Port

SD/MMC1 1.8V to 3.3V VOLTAGE TRANSLATION



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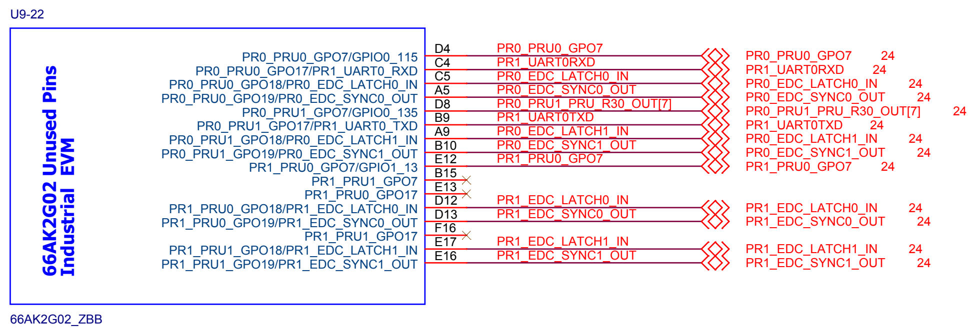
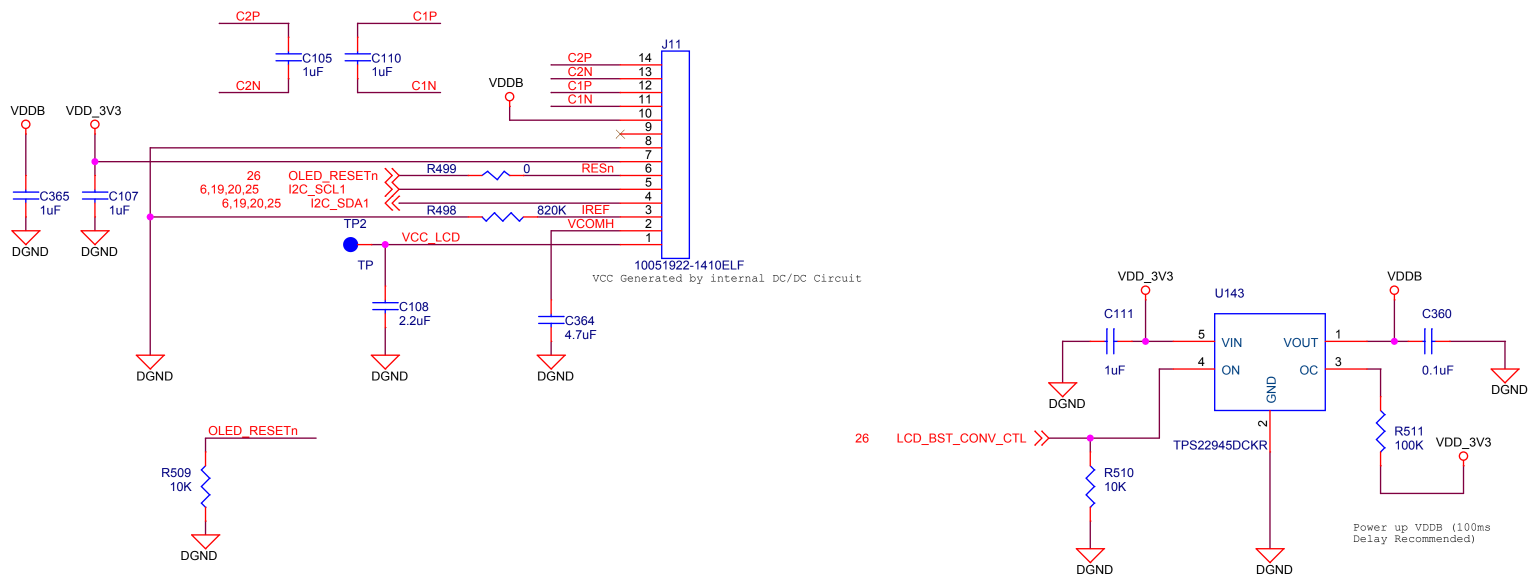
SMART REFLEX & MISC



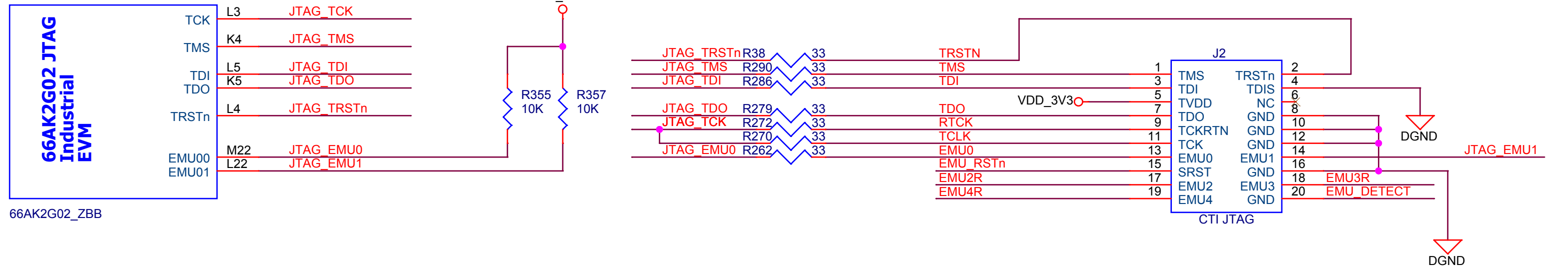
MONOCHROME LCD INTERFACE

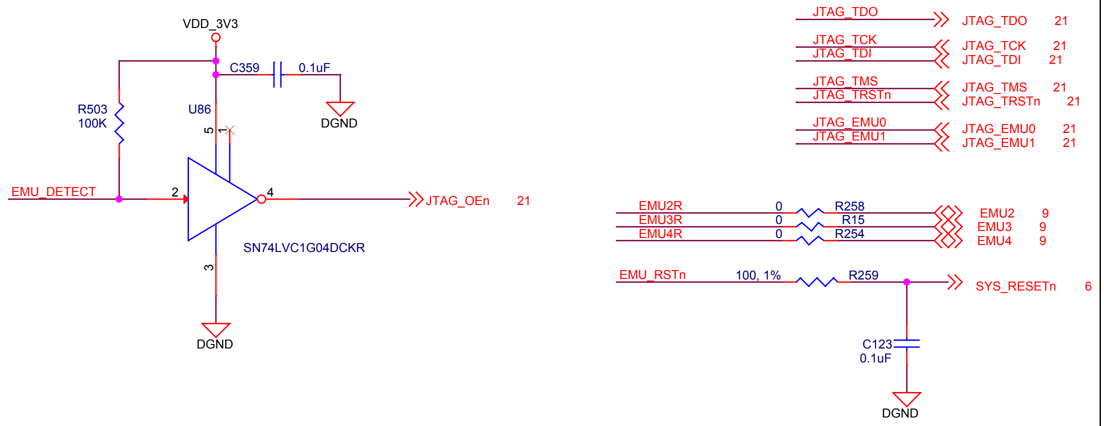


VCC Generated by internal DC/DC Circuit

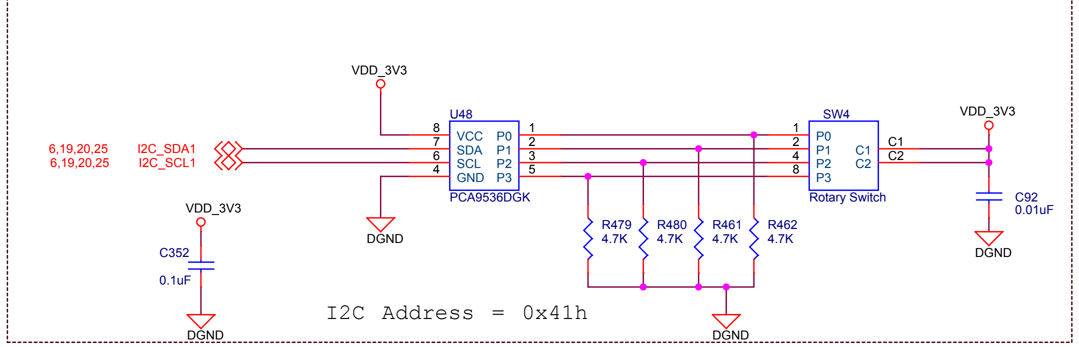
Power up VDDB (100ms
Delay Recommended)

JTAG CONNECTOR





ROTARY SWITCH - INDUSTRIAL ETHERNET SLAVE ADDRESS SELECTOR



I2C Address = 0x41h

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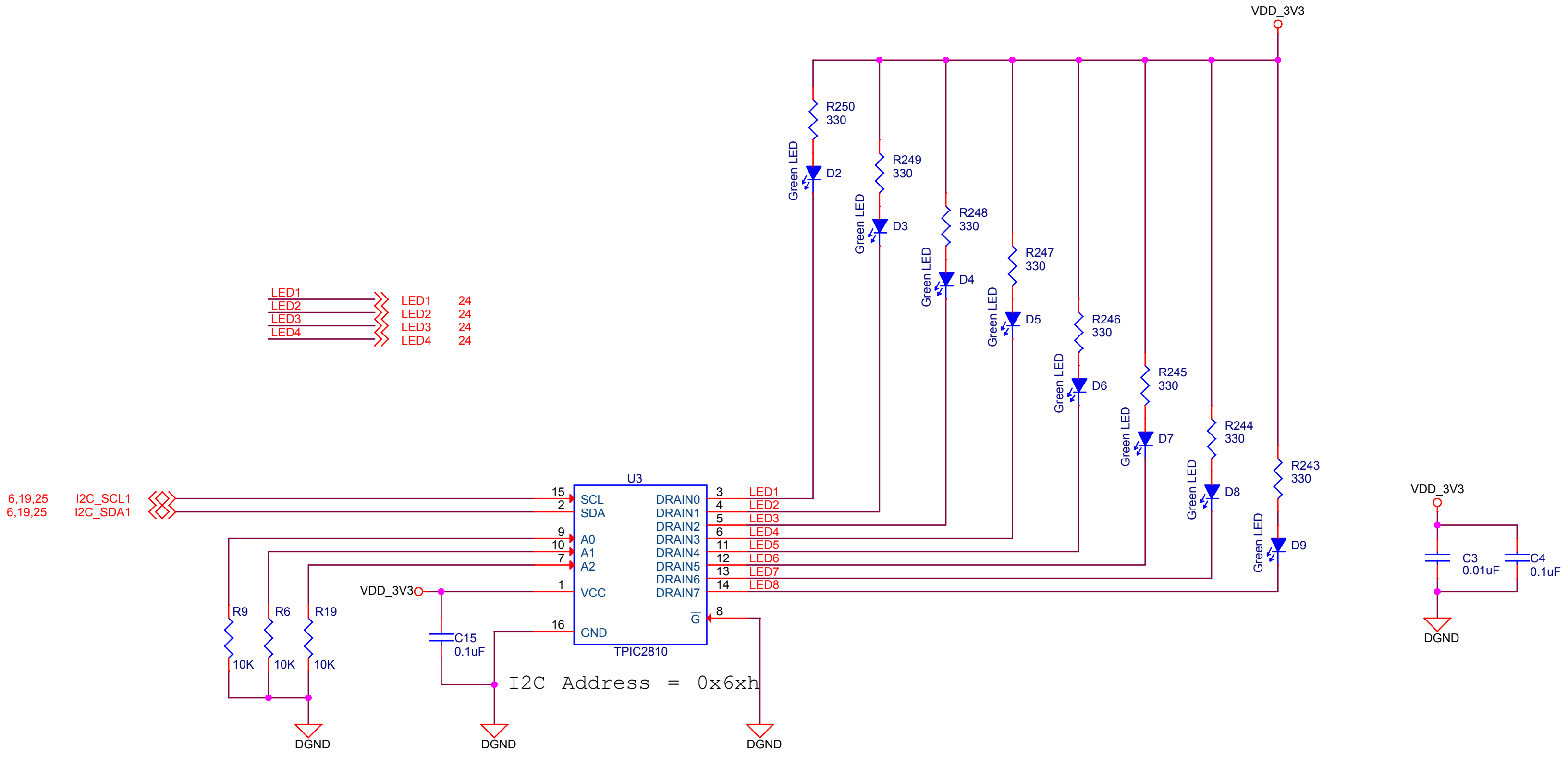
INDUSTRIAL OUTPUT LEDS



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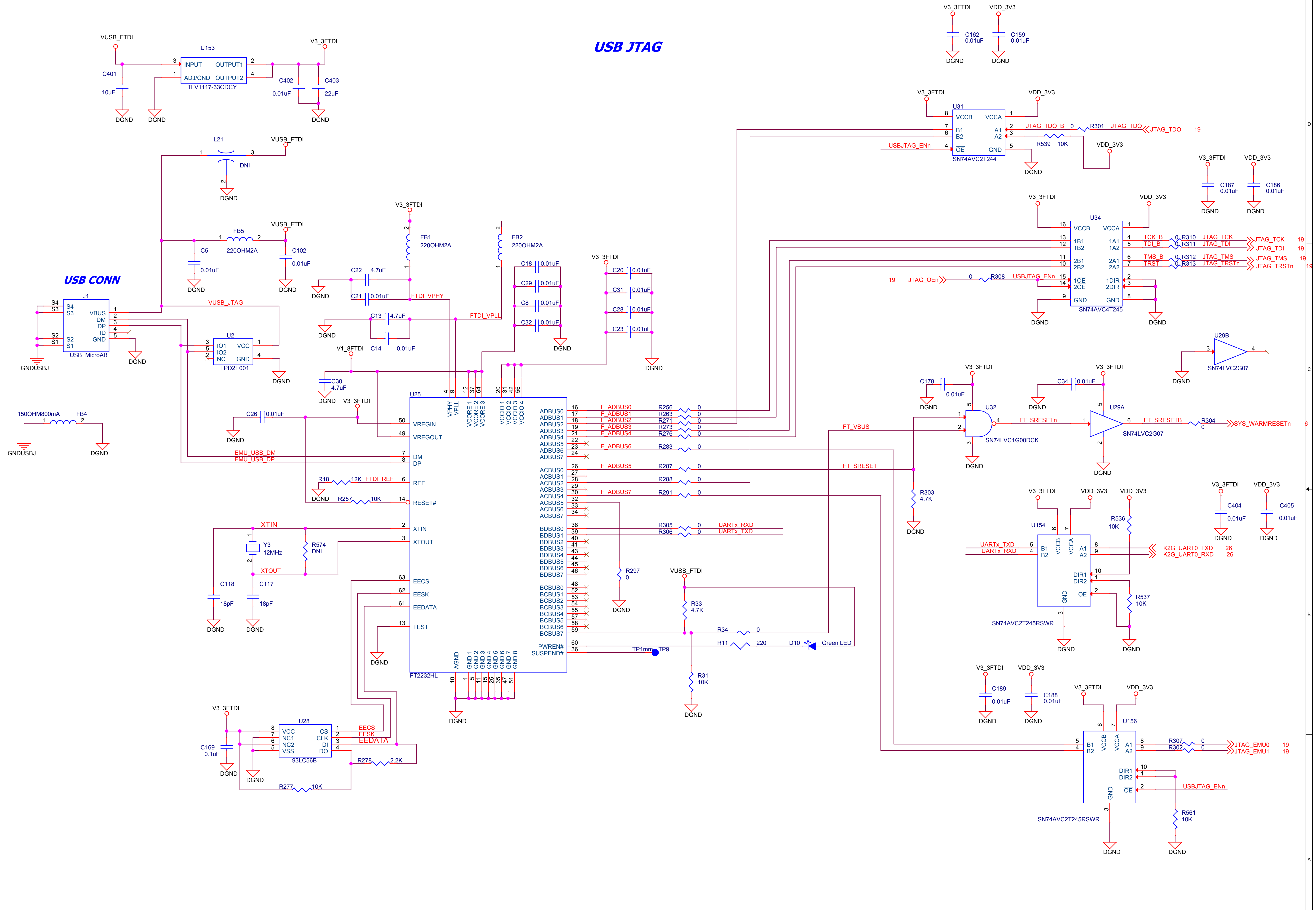

Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title	USB JTAG
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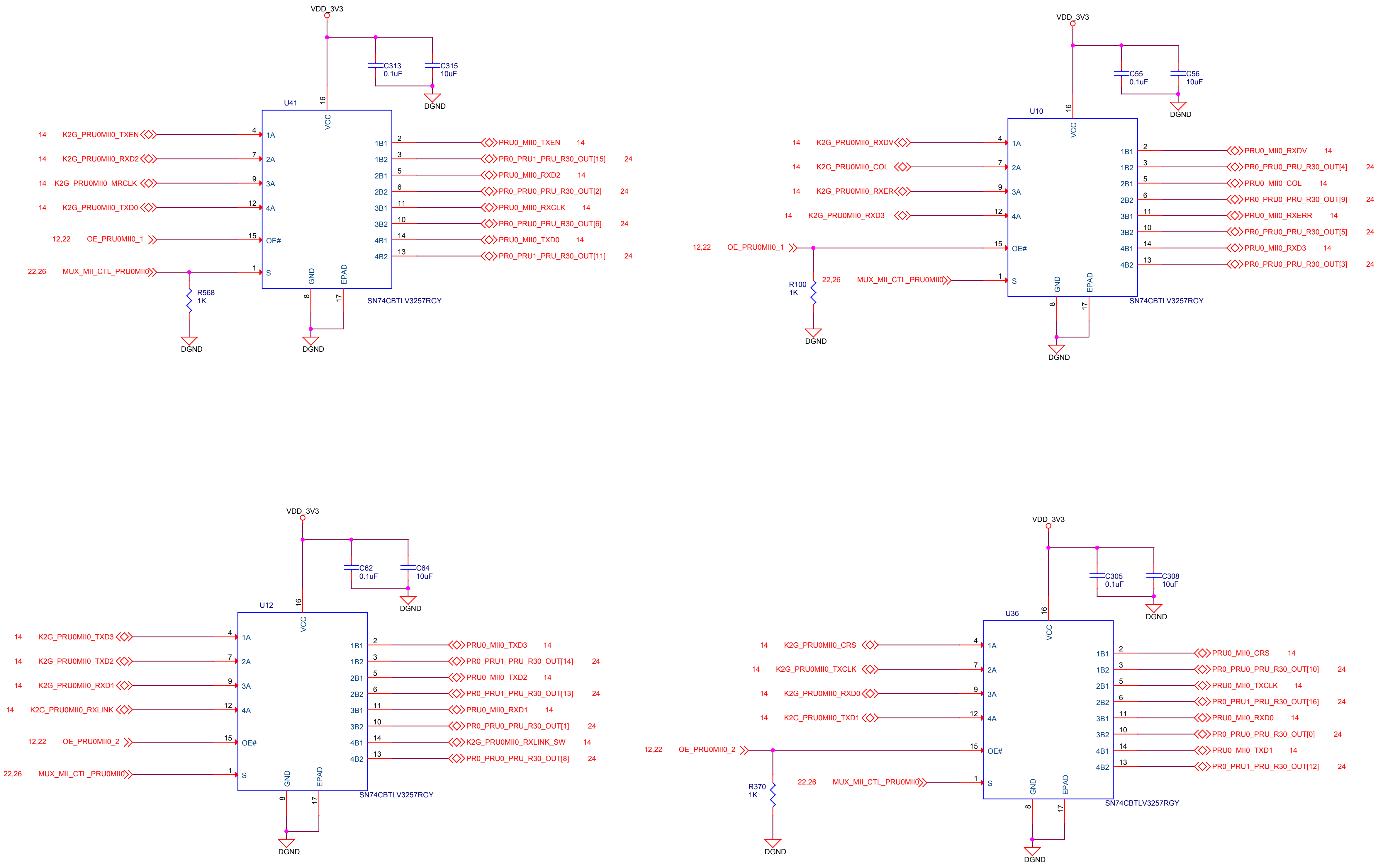
MUX/DEMUX 1



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TEXAS INSTRUMENTS

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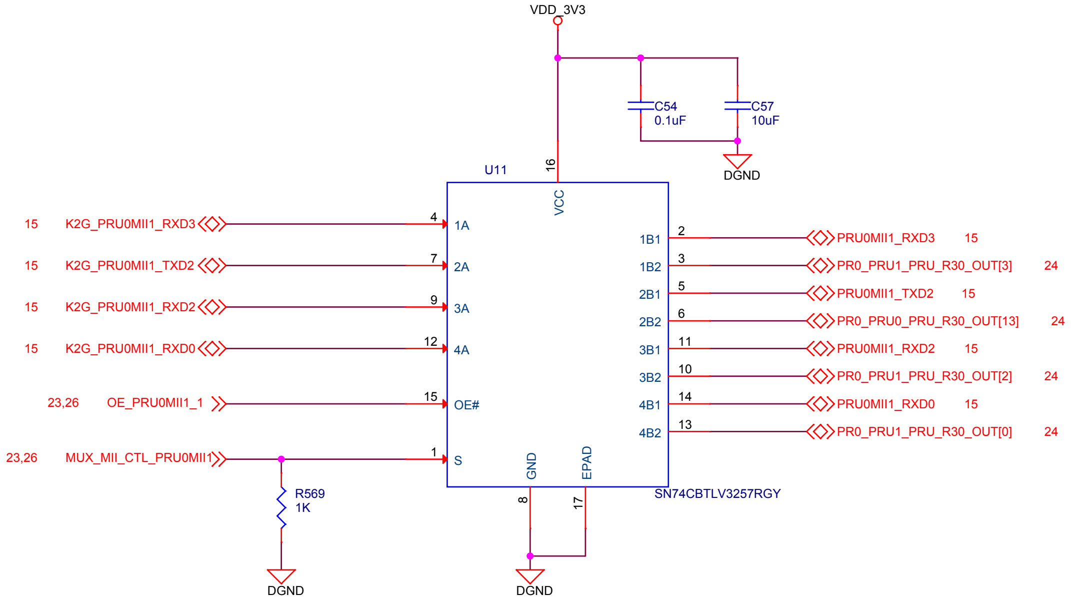
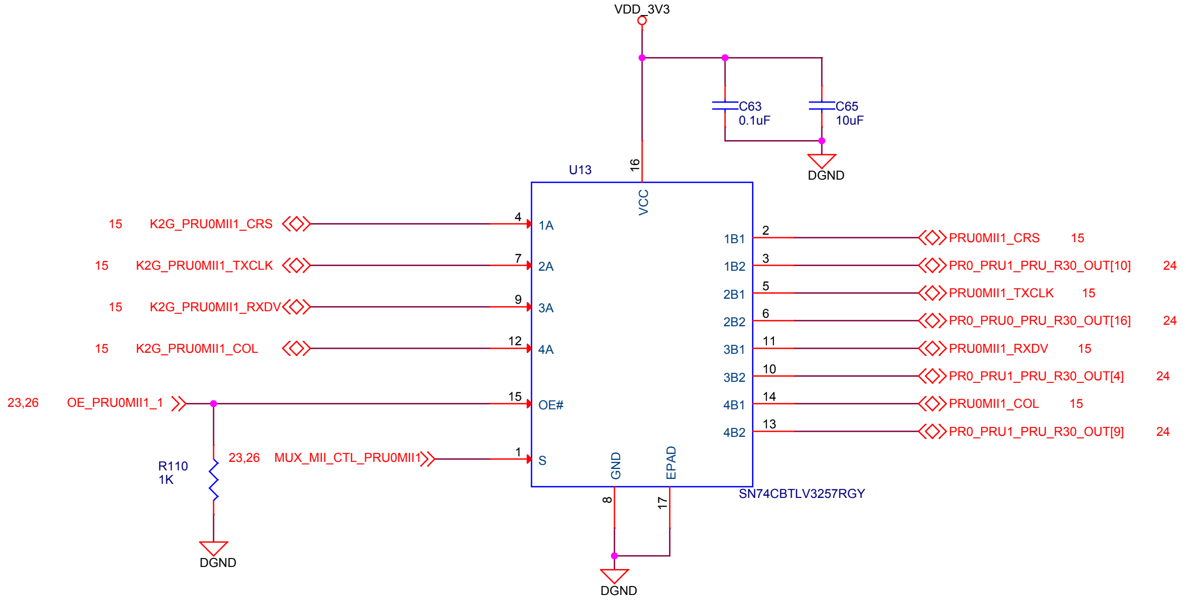
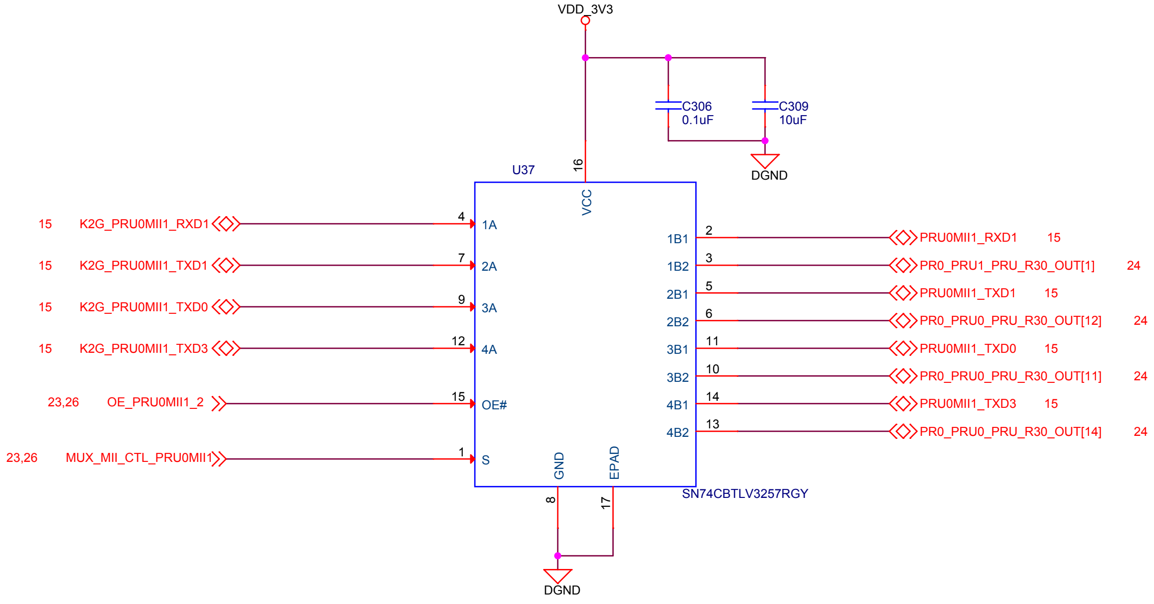
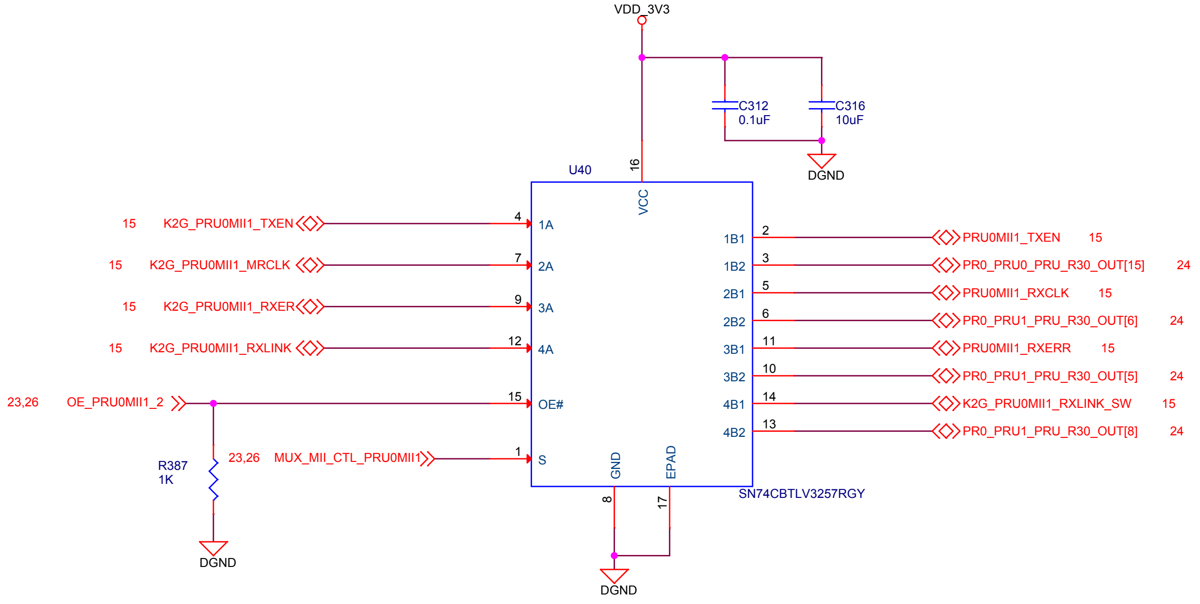
MUX DEMUX 2









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Texas Instruments
MISTRAL

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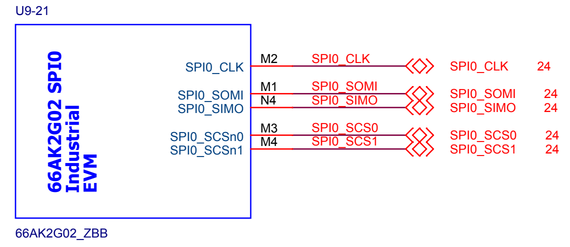
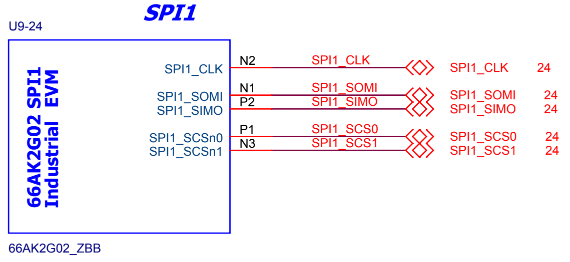
EXPANSION CONNECTOR

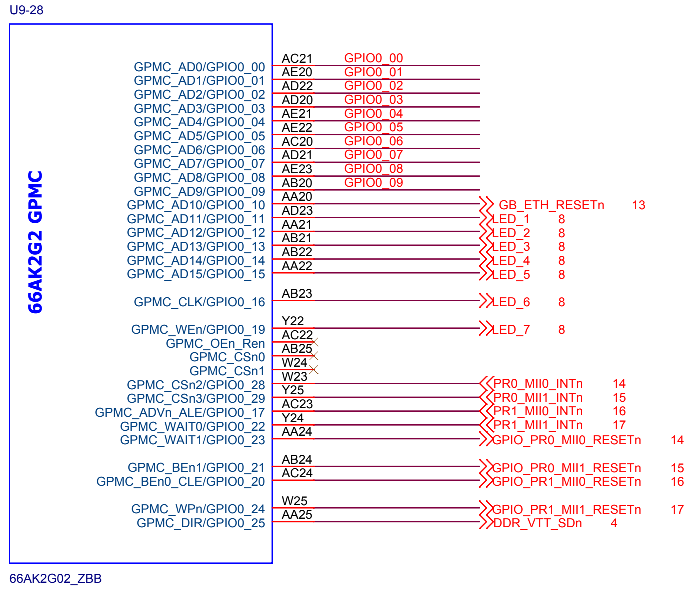
SPI0



SPI1



GPIO EXPANSION



Project :
K2GICE
K2G ICE
PROC022

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TEXAS INSTRUMENTS

MISTRAL

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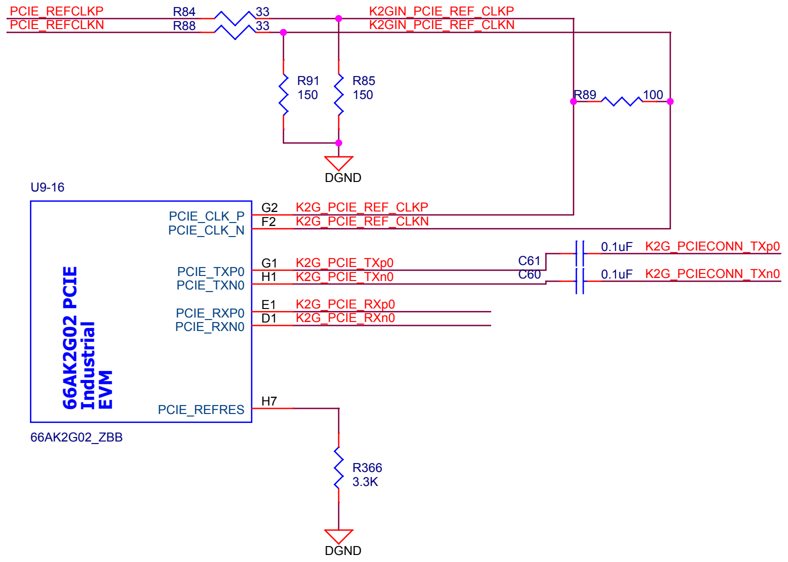
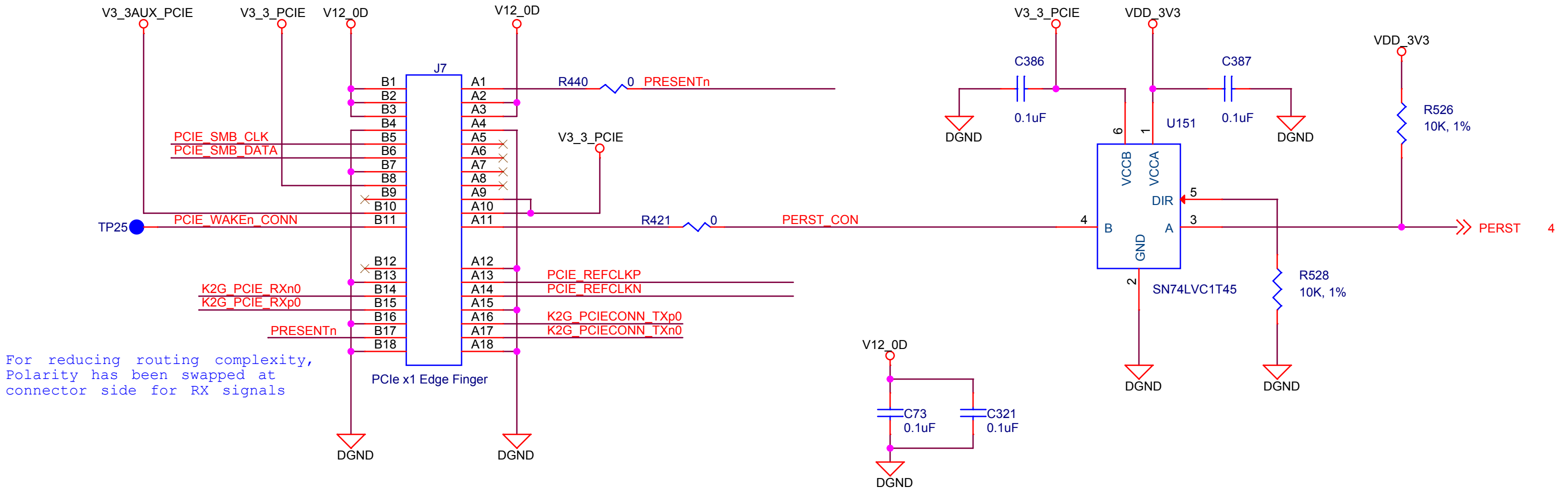
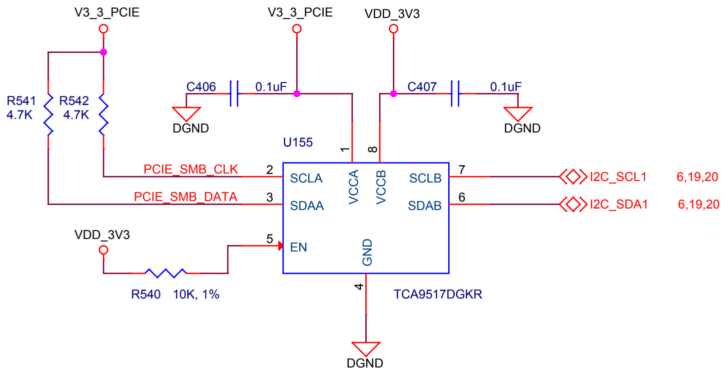


PCIe Edge Fingers





Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title PCIe x1 CONNECTOR
K2GICE PROC022	TEXAS INSTRUMENTS MISTRAL	Size C Document Number MS_TI_K2GICE_SCH_REVD Rev D
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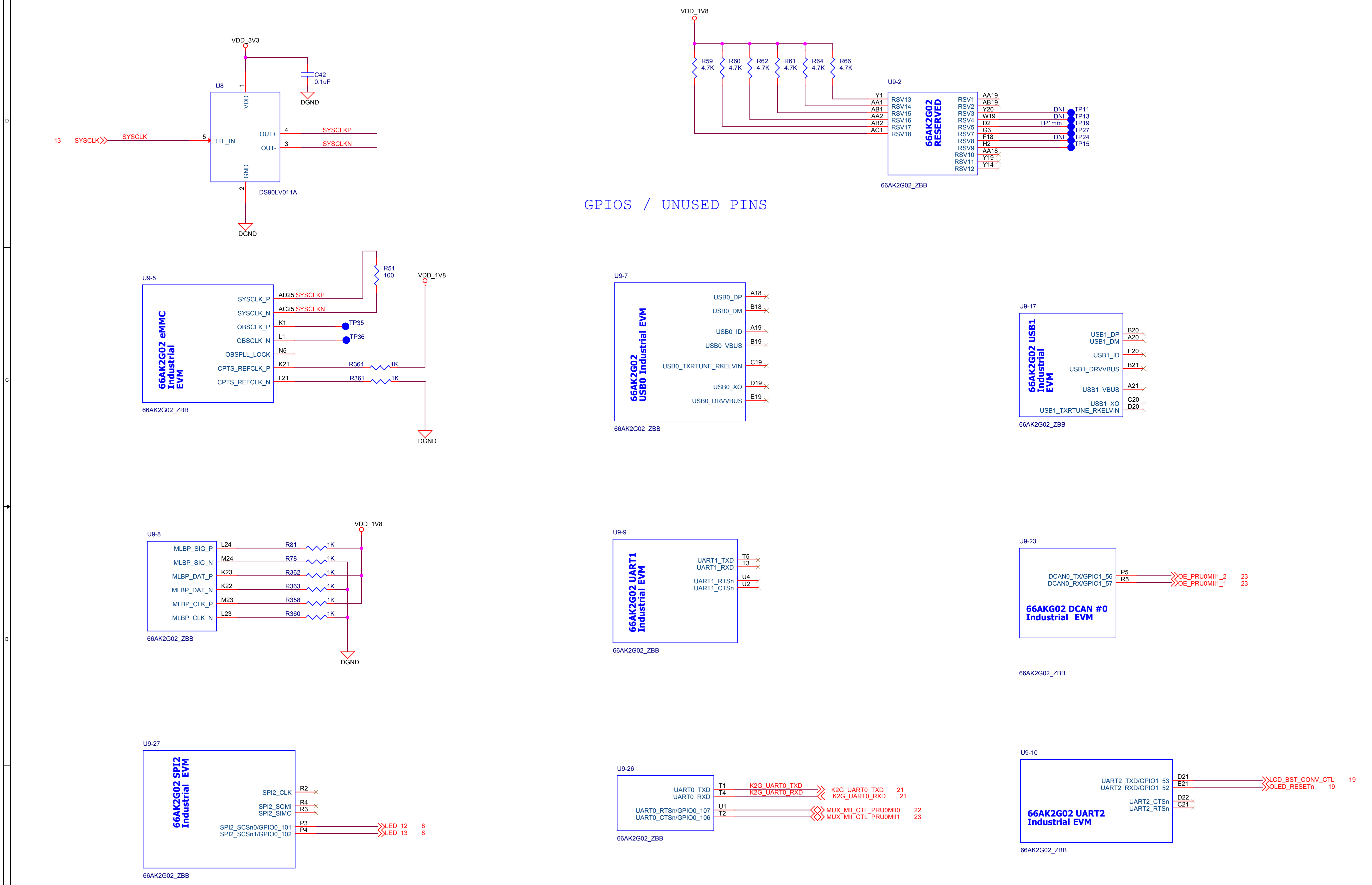
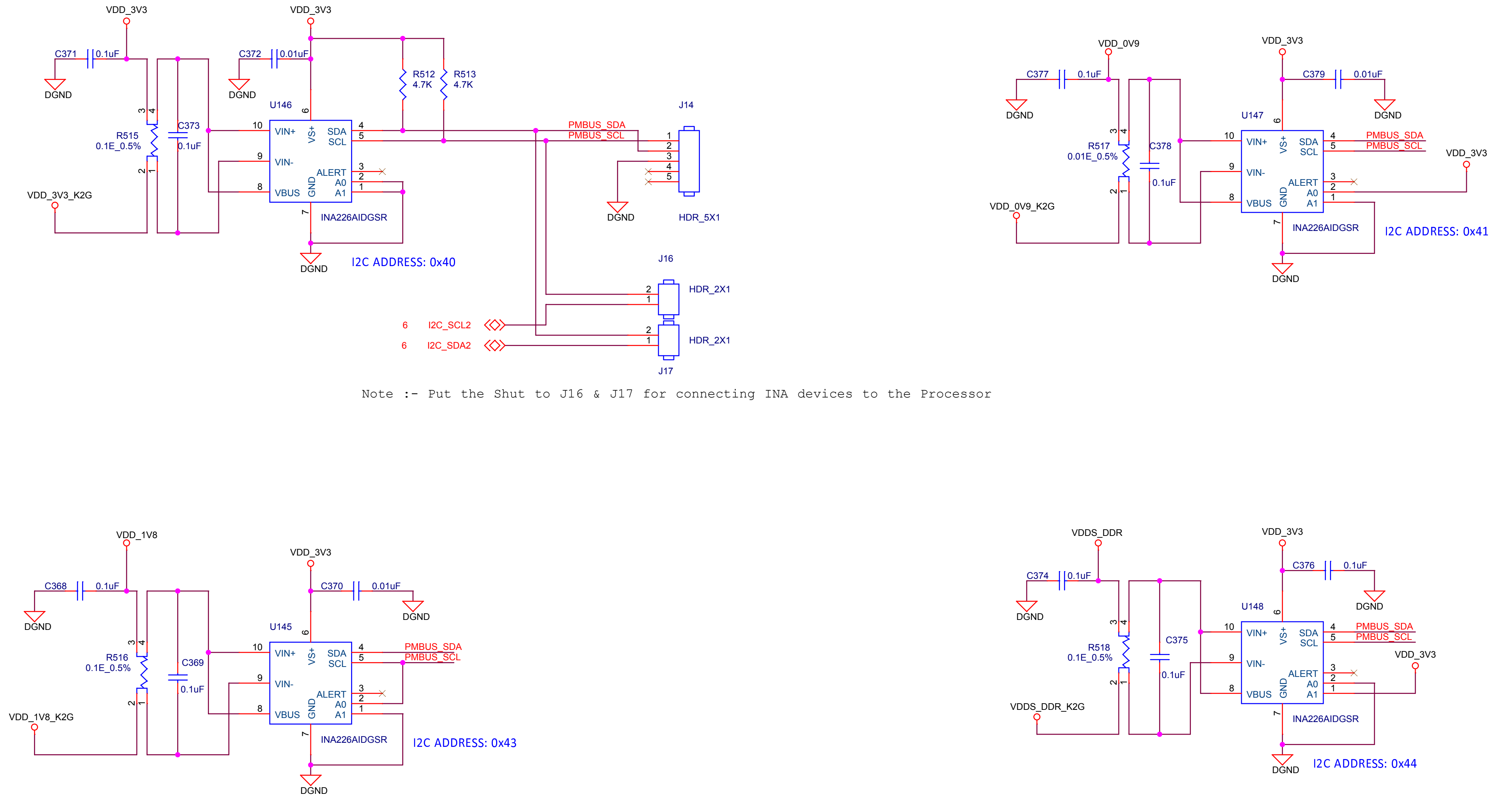


Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title GPIOS
K2GICE PROC022	TEXAS INSTRUMENTS MISTRAL	Size C Document Number MS_TI_K2GICE_SCH_REVD Rev D
		Date: Wednesday, March 08, 2017 Sheet 26 of 29

INA DEVICES



Note :- Put the Shut to J16 & J17 for connecting INA devices to the Processor

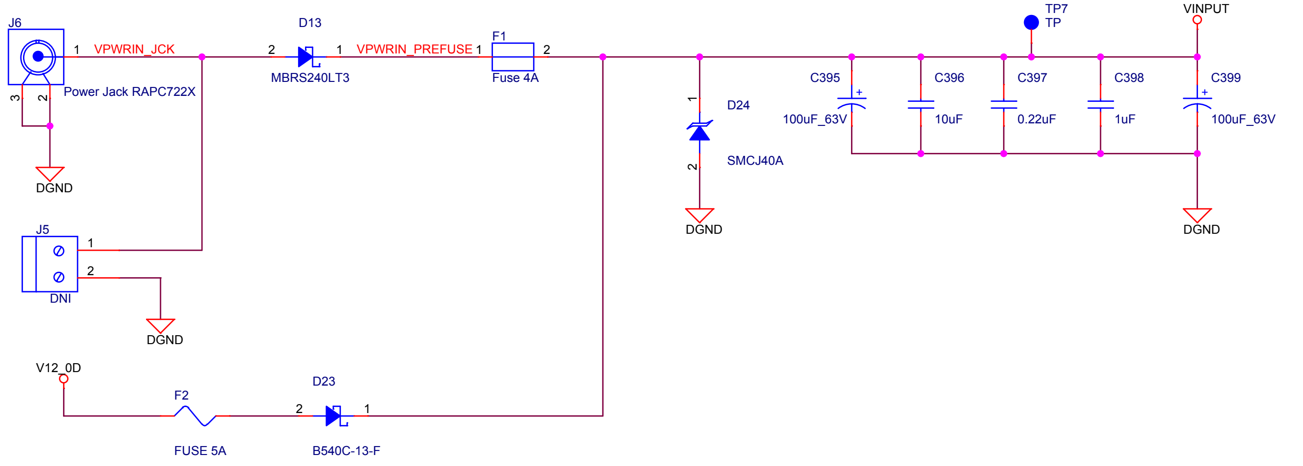
Project :

K2GICE
PROC022

Designed for TI by Mistral Solutions Pvt Ltd

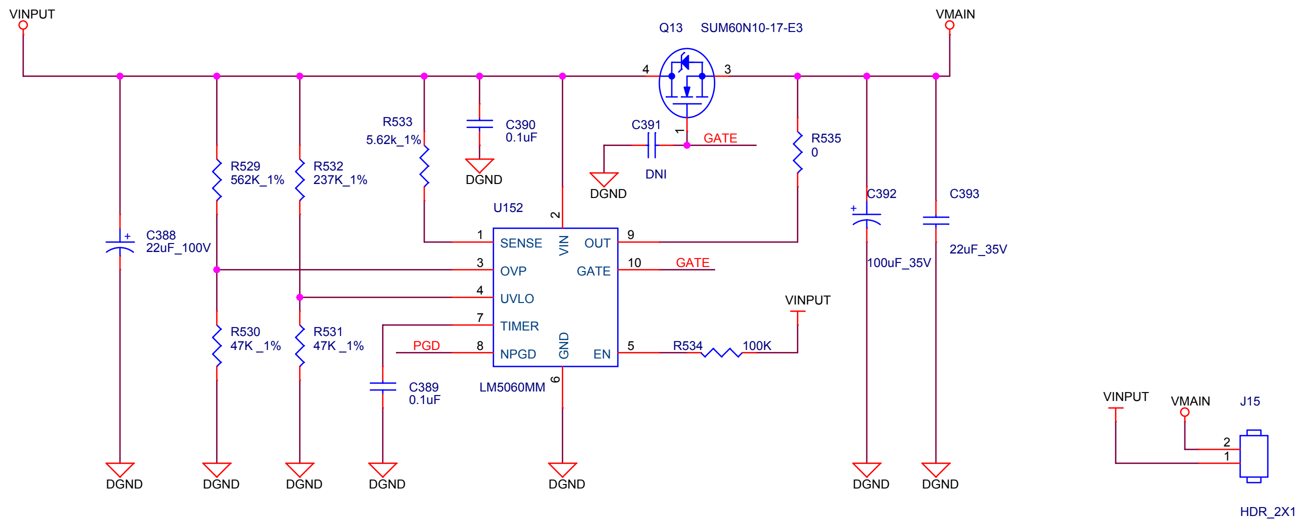
Title	CURRENT MEASUREMENT	
Size C	Document Number MS_TI_K2GICE_SCH_REVD	Rev D
Date: Wednesday, March 08, 2017	Sheet 27 of 29	

Main 24VDC & PCIe 12DC Power Input

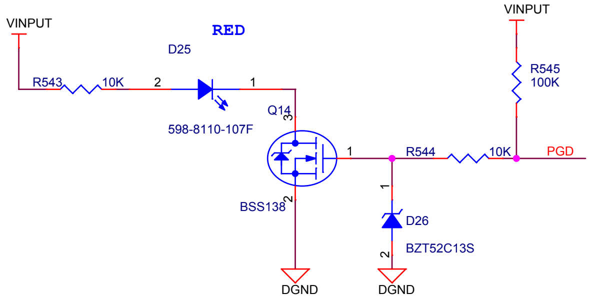


Over Voltage Protection Circuit

UVLO set for 11V
OVP set for 26V



Fault Indication



Condition	LED Status(D25)
VINPUT between 11 to 26V	OFF
VINPUT above 26V or below 11V	ON

Note:- When fault is indicated ,set to proper voltage and power cycle the board.

Project :
K2GICE
PROC022

Designed for TI by Mistral Solutions Pvt Ltd

Title	POWER ORING & OVP CIRCUIT	
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C	MS_TI_K2GICE_SCH_REVD	D
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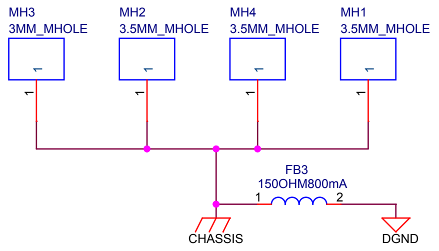
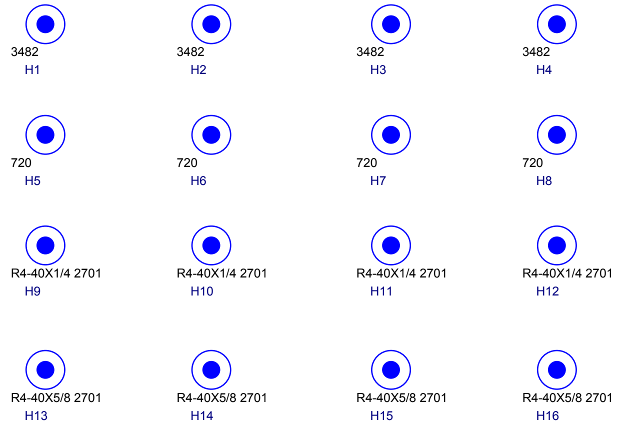
HARDWARE SCHEMATICS

MOUNTING HOLES



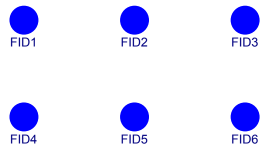
STANDOFFs



M1
Shunt0.1in

SHUNT SHOULD BE PLACED ON J3
FOR INTERNAL SYSCLK SOURCE SELECT

FIDUCIALS



Label Assembly Note
ZZ1
The boards and components must be baked before assembly

Label Assembly Note
ZZ2
Provide serial numbers to the assembled boards for identification

Label Assembly Note
ZZ3
Please carry out the cold points check verification and provide the report for each assembled board

Label Assembly Note
ZZ4
The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

Label Assembly Note
ZZ5
All MSL components should be baked as per JEDEC standard

Label Assembly Note
ZZ6
PCB should be baked at 120 degree for 8 hours

Label Assembly Note
ZZ7
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Label Assembly Note
ZZ8
These assemblies are ESD sensitive, ESD precautions shall be observed.

Label Assembly Note
ZZ9
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

LOGOs & LABELs

PCB
LOGO
Texas Intruments

PCB
LOGO
Pb-Free

PCB
LOGO
For Evaluation only; not FCC approved for resale

PCB1
K2G_BARE_PCB

A1
LCD - Passive Matrix
Monochrome 96x16
Display
OSD-9616

Board Serial No.
PCB Label
Size: 0.7" x 0.2 "
LBL1

MAC ID.
PCB Label
Size: 1.12" x 0.59 "
LBL2

KIT CONTENTS

MicroSD CARD
SDSDQAB-008G
H17

ETHERNET CABLE
N210-007-GY
H18

USB CABLE
0687840001
H19

Project :
K2GICE
PROC022

Designed for TI by Mistral Solutions Pvt Ltd

TEXAS INSTRUMENTS
MISTRAL

Title	HARDWARE SCHEMATICS		
Size	Document Number		Rev
C	MS_TI_K2GICE_SCH_REVD		D
Date:	Wednesday, March 08, 2017	Sheet 29 of 29	

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