DM38x DaVinci™ Digital Media Processor High-Definition Video Processing Subsystem (HDVPSS)

User's Guide

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About This Manual

This document describes the operation of the High-Definition Video Processing Subsystem (HDVPSS) in the DM38x DaVinci™ Digital Media Processor.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers may be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing non-default values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

Related Documentation From Texas Instruments

For product information, visit the Texas Instruments website at http://www.ti.com.

SPRS821 — DM385 and DM388 DaVinci™ Digital Media Processor

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High-Definition Video Processing Subsystem (HDVPSS)

Topic **Page**

1.1 Description of the Subsystem

1.1.1 Overview

The HDVPSS module includes video display and capture processing modules using the latest TI-developed algorithms, flexible compositing and blending engine, and a full range of external video interfaces in order to deliver high-quality video content to end devices.

1.1.2 Acronyms and Definitions

Table 1-1. HDVPSS Acronyms

Acronym	Definition
HDVPSS	High Definition Video Processing Subsystem
DEI	De-Interlacer
DVO	Digital Video Output
GRPX	Graphics Pipeline
HDMI	High Definition Multimedia Interface
NF	Noise Filter
NTSC	National Television System Committee
PAL	Phase Alternating Line
SC	Scaler
SD	Standard Definition
SDK	Software Development Kit
COMP	Compositor
VENC	Video Encoder
VIP	Video Input Port
VPDMA	Video Port Direct Memory Access
FID	Field ID (Modules inside HDVPSS interpret FID = 0 as a TOP-field and FID = 1 as a BOTTOM field)

Table 1-2. HDVPSS Data Format

Name	DataFormat A	Arrangement	Tiler Support
422I/422P	YUV422I_YUYV	Single Buffer: Y U Y V Y U Y V	No
420T	YUV420SP_UV	Y Buffer: Y Y Y Y UV buffer: U V U V	Y: 8-bit container UV: 16-bit container
422S	YUV422SP_UV	Y Buffer: Y Y Y Y UV Buffer: U V U V	Y: 8-bit container UV: 16-bit container
422T	YUV422I_YUYV	Single Buffer: Y U Y V Y U Y V	Yes : 16-bit container
444	YUV444	Single Buffer: Y U V	No
RGB565	RGB565	Single Buffer RGB, 16 bit/pixel	No
RGB24	RGB	Single Buffer RGB, 24 bit/pixel	No
ARGB1555	ARGB1555	Single Buffer: ARGB, 16 bit/pixel	No
ARGB4444	ARGB4444	Single Buffer: ARGB, 16 bit/pixel	No
ARGB24	ARGB24	Single Buffer: ARGB, 24 bit/pixel	No
ARGB32	ARGB32	Single Buffer: ARGB, 32 bit/pixel	No
Bitmap	Bitmap	Single Buffer: Color Lookup Table (RGB input only)	No

1.1.3 Features

1.1.3.1 Overall Features

Features of the HDVPSS module include:

- Supports HD (up to 1080p) and SD (NTSC/PAL) outputs simultaneously.
- Accepts the IVA HD Video Decoder output formats and adjust to several video formats. This includes (but not limited to) scan format conversion, scan rate conversion, aspect-ratio conversion, and frame size conversion.
- Handles both video and graphics efficiently to create high-quality user interfaces. This includes (but not limited to) deinterlacing, scaling, noise reduction, alpha blending, chroma keying, flicker filtering, and pixel format conversion.
- Generates secure video signal with proper content protection mechanisms, that is, HDCP and Macrovision/CGMS-a for digital and analog outputs, respectively.
- Supports VC-1 Range Mapping and Range Reduction on Primary, Auxiliary, and both Independent Transcode 420 Inputs.

1.1.3.2 Video Processing Features

- Two parallel video processing pipelines (main and aux) for concurrent HD and SD display are supported.
- The main video pipeline is used for processing video for the full size HD display. The main video pipeline employs motion-adaptive deinterlacer.
- Supported video input formats are 4:2:0 (aligned-chroma, planar, frame/field), 4:2:2 (planar, frame/field), and 444. The output formats of the HDVICP and video formats of captured external digital video data are supported. *Note:* HDVICP is not available on all devices. Refer to the device data manual for details.
- Scan format conversions (that is, interlaced to progressive and vice versa) is supported. Especially the interlaced to progressive conversion will employ a high quality motion-adaptive 3D deinterlacer to properly render both static and dynamic objects in scenes. In addition, sophisticated film-mode detection based on decoded frames (as well as the input bit-stream) is used for best rendering of film-based video.
- Scan rate conversion (up to 1080p 60Hz) is supported to handle video contents with various scan rates. It can be done via frame/field repeating/skipping. . 1080i inputs must result in 1080 lines of vertical resolution when displayed as a 1080i or P output.
- The output of the video processing will be sent to either compositor or external memory. When the output is sent to external memory, context switching between multiple inputs will be handled efficiently.
- Both the main and auxiliary video pipelines will include a write-back path to the external memory to support memory to memory scaling of video frames independently from the display output frame timing. Performance equivalent to scaling up to 16 QVGA (320x240) video windows per 1/60 sec are supported. (ADD video mosaic support).
- Color keying (transparency) is supported.

1.1.3.3 Graphics Features

- Three independently generated region-based graphics layers are supported.
- Each graphic layer supports full-screen resolution graphics.
- Each graphics layer can be displayed in either HD or SD output or both.
- Each of the graphics pipelines includes an up/down scaler optimized for graphics application. The scaler supports scaling ratios from 0.25x to 4x with 0.01 scaling step size.
- Scaling of individual regions within a graphics layer will be supported. A scaled region will not overlap with another region
- Supported graphics formats are:
  - 32-bit: ARGB8888
  - 24-bit: RGB888

- 16-bit: ARGB1555, RGB565, ARGB4444
- Bitmap: 1, 2, 4, 8-bit CLUT table
- Global and pixel-level alpha blending value is supported (256 levels). For pixel-level blending, the alpha value can come from either source or CLUT table.
- Color keying (transparency)

1.1.3.4 Cursor Features

- A dedicated hardware cursor is not supported. If a cursor function is required, it must be implemented in software.

1.1.3.5 HD/SD Compositor Features

- Supports four independently controlled compositors (HDMI/DVO1,HDCOMP, DV02, SD) .
- The HD compositors will support composition of video and graphics layers to provide full size video display, graphics overlay, video-in-graphics and picture-in-picture modes for HD video outputs.
- The SD compositor supports video display, graphics overlay, and video-in-graphics for SD video outputs..
- Each input layer will be given a display order priority which determines the display and blending orders.
- Each output supports independent layer visibility control.
- The compositor supports 256-level alpha blending of two overlapping layers.
- The compositor supports display outputs to HDMI/DVO1 and DVO2 at different scan rates or different pixel resolutions in addition to the separate SD output. HDCOMP must share either the HDMI or DVO2 pixel clock.

1.1.3.6 Video Output and Encoding Features

- A single HDMI 1.3 compliant interface with HDCP to support 1080p (1080p 24, 30, and 60 are mandatory), 1080i, 720p, 480p, 480i. 640x480, 800x600, 1024x768, 1280x768, and 1920x1200.
- Two DVO interfaces that support up to 1080p at 60 MHz 8/16/24 YCbCr/RGB formats are included. Each DVO port supports both embedded and separated sync outputs. VBI data insertion on DVO outputs are not required.
- HD analog output: Component or VGA, meets all requirements defined in ITR-R BT.470-6
- SD Composite/S-video (NTSC/PAL): meet all requirements defined in ITU-R BT.476-6.
- SD SCART analog outputs.
- All video outputs (SD Composite/S-Video, HDMI/DVO1, HDCOMP, and DVO2) may be active simultaneously and HDCOMP must in the same pixel clock as either HDMI/DVO1 or DVO2.
- Supported resolutions are 480i, 480p, 720p, 1080i, 1080p.

1.1.3.7 VBI Features

- VBI Closed Captioning and other data pass-through.
- EIA/CEA-608-B Line 21 Data services – supports both SCTE 20 and SCTE 21 standards.
- EIA-708-B Digital Television (DTV) Closed Captioning – support SCTE21/ATSC A/53e standards.
- Reconstruction of lines 10 through 21 of the VBI from a data source available to the host CPU (video user data DVS706r8 – DVB/SCTE specifications based on PES encoding of VBI data Raw VBI data, Closed Caption (CC), Teletext (NABTS, WSS), CGMS, VPS, VITC, Gemstar 1x and 2x, Extended Data Service(XDS), Moji, V-Chip).

1.1.3.8 Copy Protection

- NTSC Analog outputs (only for SD modes) – Macrovision version 7.1
- HDMI - HDCP
- All analog outputs – CGMS-A on all analog outputs
- Uses 59.94Hz output frame rate for both 59.94 and 60Hz source materials to maintain the same output

frame rate on both NTSC and HD outputs

1.1.3.9 Video Capture Features

- HDVPSS supports two independently configurable external video input capture ports.
- Each video input capture port can be operated as one 16/24-bit input channel (with separate Y and Cb/Cr inputs) or two clock independent 8-bit input channels (with interleaved Y/C data input). Embedded sync and external sync modes are supported for all input configurations.

1.1.3.10 Input Data Features

NOTE: Due to pinout restrictions, not all combinations are supported on all devices. Refer to the device data manual for details.

- 8-bit input ports:
  - A single non-multiplexed CIF/480i/480p/720p/1080i Y/C data
  - Up to 2-stream multiplexed ED (480p) Y/C data
  - Up to 4-stream multiplexed SD (480i) Y/C data
  - Up to 16-stream multiplexed CIF Y/C data (TBD – 16)
- 16/24-bit input ports:
  - A single non-multiplexed CIF/480i/480p/720p/1080i/1080p Y/C data
  - A single 24-bit YCbCr component or raw RGB data
  - Up to 2-stream multiplexed HD (720p/1080i) Y/C data
  - Up to 4-stream multiplexed ED (480p) Y/C data
  - Up to 8-stream multiplexed SD (480i) Y/C data
  - Up to 8-stream multiplexed CIF Y/C data
- The video capture port channel supports de-multiplexing of both pixel-to-pixel and line-to-line multiplexed streams.
- Up to 1920x1200@60Hz (160MHz) input data rate is supported for 16-bit mode input port.
- Each video capture port supports one scaler capable of both up and down scaling of one non-multiplexed input stream (one of two 8-bit channel inputs or 16-bit input channel input data).
- Each video capture port supports one programmable color space conversion to convert 24-bit RGB data to YCbCr data.
- HDVPSS supports data storage in 444, 422, and 420 formats.
- Each video capture port channel supports chroma down sampling (422 to 420) for any non-multiplexed input data. The chroma down-sampling for multiplexed streams is done as memory-to-memory operations outside of HDVPSS on an individual frame data.
- Deinterlacing is not supported.
- Ancillary data capture is supported for VANC/VBI data (ancillary data within the interval between SAV-EAV sequences during vertical blanking period) on all input channels. HANC data capture is not supported. Decoding of the Ancillary data will be handled by the software.
- Graphics overlay over incoming bitstream is NOT supported.
- Noise Reduction on the incoming video is supported as a separate memory-to-memory operation within the HDVPSS.
- One of the 8-bit channels in each video port may be used as a video write back path for transcoding applications. This channel may also use the color space conversion and/or the scaler. It is up to the application to avoid resource contention.

1.1.3.11 Other Features

- The HDVPSS supports two additional video input source in 420 or 422 tiled format (same as input for main and auxiliary video paths). This path can be used for both video transcode operations (utilizing a

scaler and chroma downsampler within one of the VIP ports in a memory to memory configuration) and/or driving video to the SD output display.

  - Only 1 of the 2 additional video input sources can directly drive the SD display. For display output, there is no processing performed, that is, no scaler or deinterlacing

- The HDVPSS supports video data write back paths for following:
  - Scaled video from aux video channel (for delayed PIP display) saved as 422 video.
  - Scaled video from main video channel saved as 422 video.
  - SD scaled video from the main video compositor (delayed SD output display when CIT is off) saved as 422 video
  - Independently scaled video from main deinterlacer output (transcoding application) – saved as a 420 video using the scaler and chroma_downsampler resources in one of the VIP ports.
  - Independently scaled video from aux output (transcoding application) – saved as a 420 video using the scaler and chroma_downsampler resources in the other VIP port. This path is shared with the independent transcode video input source.
  - Independently scaled video from the 3rd or 4th video input source saved as a 420 video using a scaler and chroma downsampler resource in one of the VIP ports. The 3rd or 4th video input source can be 422 or 420 tiled input data (same as input for main and auxiliary inputs). The 3rd and 4th video input source share the VIP write back paths of the primary and auxiliary deinterlacers.
  - Write back of the scaled video from main, aux or additional video input source video channels supports both tightly (1 frame per 1 display frame period) and loosely (many frames per 1 display frame period) coupled to the display frame period. All other write backs are tightly coupled
  - The HDVPSS includes a highly programmable and bandwidth-efficient DMA controller to support the worst-case bandwidth application.

1.1.3.12 Feature Limitations

The features of the HDVPSS module highlighted above are characteristics of the HDVPSS module and are not supported on all SoCs that use the HDVPSS. Common limitations exist, such as:

- **Device and system bandwidth.** The bandwidth available to the HDVPSS varies based on the frequency and width of the DDR interface provided on the device, the frequency and width of the DDR interface populated on the user's particular board, and the bandwidth demands of the remaining IP in the system. These constraints may limit the data rates that can be concurrently supported on the various input and output interfaces to the HDVPSS.
- **Device and system pinout.** Specific devices within the device family may not provide full availability of all of the Video Input and Video Output ports. In addition, pin multiplexing constraints for a particular end system may further limit the availability of specific HDVPSS signals. Refer to device data manual for details on the device availability and pin muxing with other internal signals.

NOTE: The following list is the convention for pin naming:

- Pins with VIN0 are connected to VIP0
- Pins with VIN1 are connected to VIP1
- Pins with VOUT0 are connected to DVO2
- Pins with VOUT1 are connected to DVO1

There is no need for any pinmux configuration for analog outputs.

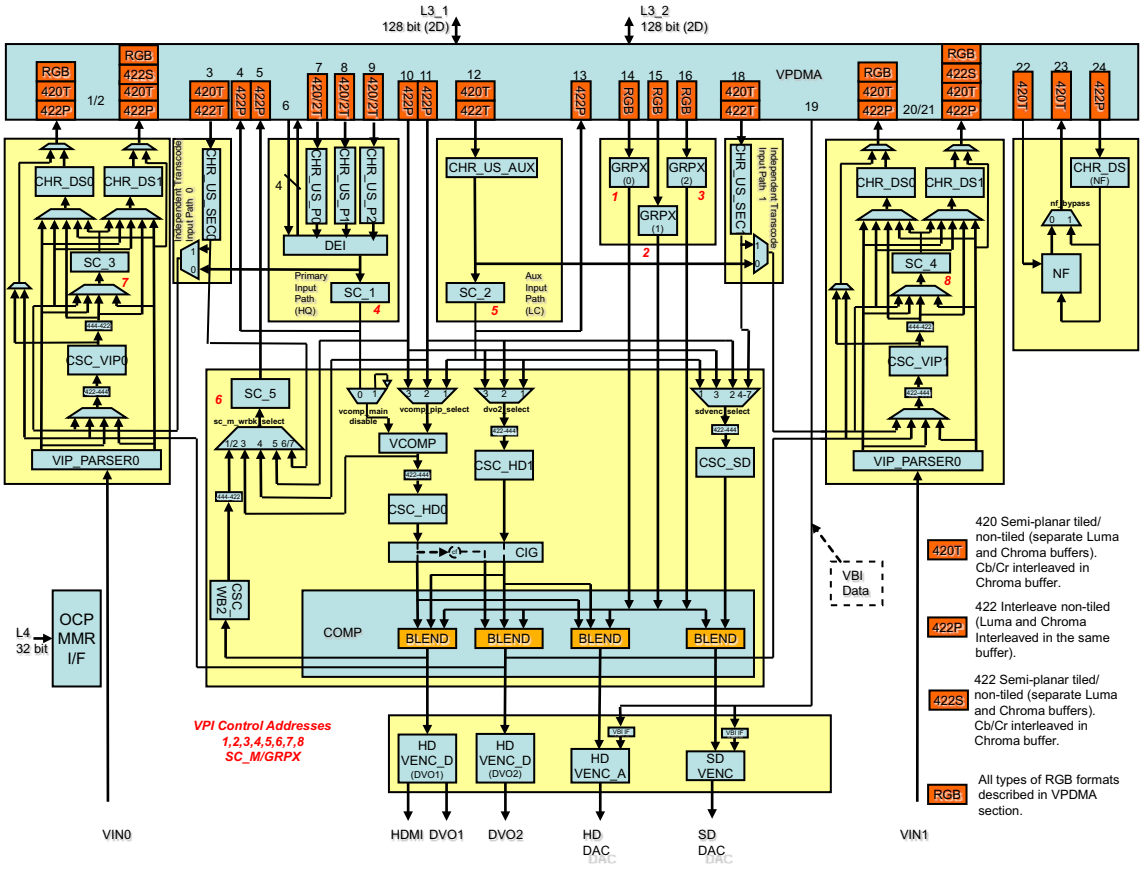
NOTE: The block diagram and text sections of this chapter consistently use the instance numbering for the VIP and GRPX submodules as VIP0/VIP1 and GRPX0/GRPX1/GRPX2. However, the register sections use the numbering VIP1/VIP2 and GRPX1/GRPX2/GRPX3. The following list is the convention for submodule naming to register control:

- Submodule VIP0 is controlled by registers VIP1
- Submodule VIP1 is controlled by registers VIP2
- Submodule GRPX0 is controlled by registers GRPX1
- Submodule GRPX1 is controlled by registers GRPX2
- Submodule GRPX2 is controlled by registers GRPX3

1.1.4 Functional Operation

Figure 1-1 shows a block diagram of the HDVPSS.

Figure 1-1. HDVPSS Detailed Block Diagram



In Figure 1-1, the primary input path contains a deinterlacer and scaler (down-scale only when the source is VIP_PARSER or the destination is VENC). The auxiliary input path contains a scaler. The main path is capable of deinterlacing up to 1080i sources. The CHR_US modules in both paths are identical.

The 4:2:2–4:4:4 and 4:4:4–4:2:2 modules are used to convert data from YUV422 space to YUV444 space, or from YUV444 space to YUV422 space. These blocks do not have any MMR for configuration and are enabled whenever required by the following modules.

Figure 1-1 also shows the VPDMA VPI Control Addresses for modules within the HDVPSS that use this interface (numbers shown in red). Modules that use the VPDMA VPI Control Address mechanism are any SC (SC_1, SC_2, SC_3, SC_4, SC_5), or GRPX module.

Note that VPDMA only supports 422 paths for display only. In addition, the numbers shown on the VPDMA ports correspond to those listed in Table 1-3.

Table 1-3. VPDMA Client Number

VPDMA Client Number	HDVPSS Port
1 / 2	VIP0 YUV/RGB/Ancillary Data (To VPDMA)
3	Secondary-0 Input Path (From VPDMA)
4	Scaler (SC_1) Output Path (To VPDMA)
5	Scaler (SC_5) Output Path (To VPDMA)
6	DEI Motion Data (To/From VPDMA)
7	Primary Video (Fn) Input Path (From VPDMA)
8	Primary Video (Fn-1) Input Path (From VPDMA)
9	Primary Video (Fn-2) Input Path (From VPDMA)
10	Bypass Path-0 Input (BP0) (From VPDMA)
11	Bypass Path-1 Input (BP1) (From VPDMA)
12	Auxiliary Video Input Path (AUX) (From VPDMA)
13	Scaler (SC_2) Output Path (To VPDMA)
14	GRPX0 RGB/Stencil/CLUT Input Path (From VPDMA)
15	GRPX1 RGB/Stencil/CLUT Input Path (From VPDMA)
16	GRPX2 RGB/Stencil/CLUT Input Path (From VPDMA)
18	Secondary Input Path-1 Input (From VPDMA)
19	SDVENC VBI Data (From VPDMA)
20 / 21	VIP1 YUV/RGB/Ancillary Data (To VPDMA)
22	420 Noise Filter Data (From VPDMA)
23	Noise Filter/Chroma Downsampler Output Data (To VPDMA)
24	422 Noise Filter/Chroma Downsampler Input Data (From VPDMA)

Figure 1-2 provides a more detailed view of the Primary Input Path (PRI), showing the interconnection between various modules and bit widths.

Figure 1-2. Primary Input Path (PRI) Detailed Block Diagram

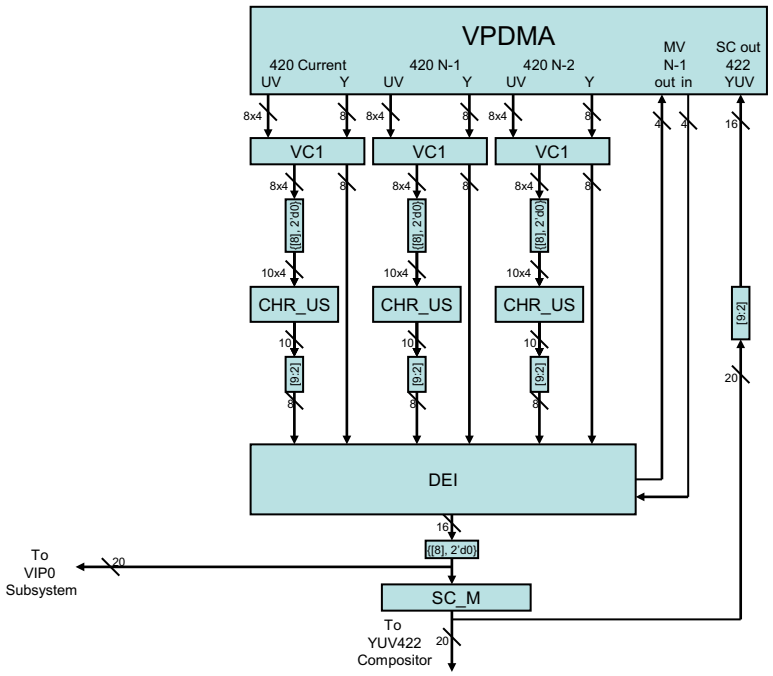
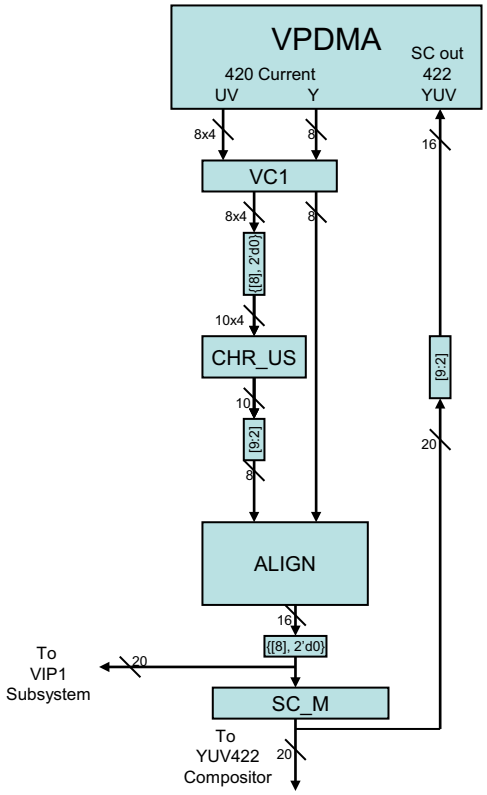


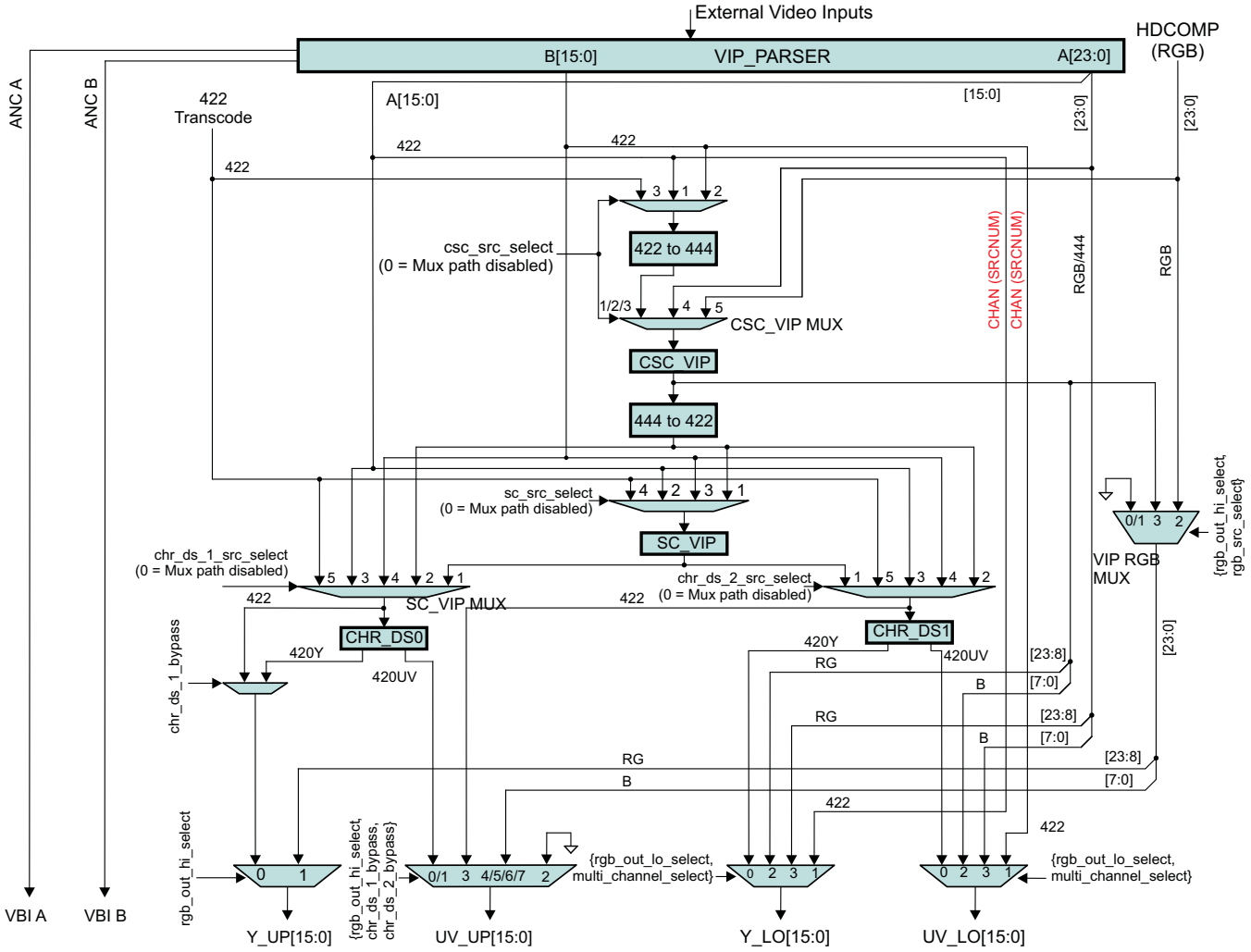
Figure 1-3 provides a more detailed view of the Auxiliary Input Path (AUX), showing the interconnection between various modules and bit widths.

Figure 1-3. Auxiliary Input Path Detailed Block Diagram



The previous diagrams show the details of the interconnect and selections possible within the Video Input Ports. In Figure 1-4, the signals shown on the Video Input Port Parser (VIP_PARSER) module are the outputs generated by this module. External video input drives the input side of this module. A_Y can be in either YUV422 format (A_Y[7:0] in the diagram) or RGB/YUV444 format (A_Y[23:0] in the diagram) depending on the external video input source and configuration options within the VIP_PARSER. If the VIP_PARSER is configured to capture 24bit RGB/444 data, A_Y[23:0] is used and the data path inside the Video Input Port must be configured correctly for it. Multiplexor selections and controls are shown above, and described in CLKC VIN0/2 Data Path Register. The output of the Video Input Port drives the VPDMA module, which sends the resulting video to SDRAM.

Figure 1-4. VIP Subsystem Detailed Block Diagram



1.1.4.1 Functional Module Descriptions

The HDVPSS module is composed of many processing blocks. There are multiple instances of most of these processing blocks. The following module descriptions provide a high-level description of each processing module.

1.1.4.1.1 VPDMA

The VPDMA module is capable of transporting data to and from an external memory location, most often external DDR memory, buffering this data and then delivering the data as demanded to HDVPSS modules as programmed. Additionally in a third-party configuration the VPDMA is capable of performing DMA transfers as requested by the pulsing of an event strobe.

The VPDMA module is also capable of generating an address which may reach any location in the range for which it is configured. It is capable of moving this data either to or from a Shared Buffer and ultimately to or from a Client Buffer. For the two type of Client Buffers that are used to drive data into a subsystem (Streaming Buffer and Random Access Buffer) data is either pushed into the buffer or pulled out of the buffer dependent upon the direction of the data transfer.

For third-party DMA operations the data is transferred into a Client buffer, and then transferred out of the Client Buffer to the transfer destination. These transfers are triggered by an Event pulse to each of the Client Buffers which are Routing Buffer types.

1.1.4.1.1.1 VPDMA Details

The modules that source or sink data are referred to as clients. That is, the physical interface between the processing module and external memory is called a client. A channel is the mechanism inside the VPDMA that connects a specific memory buffer or transfer to a specific client.

Each of the channels has a type of data that it can support based upon the client that it services. Based on this, four kinds of channel has been defined:

- YUV Channel—Clients taking data in YUV format like DEI, NF, and so on.
- RGB Channel—Clients taking RGB data like GRPX
- Miscellaneous Channel—The Miscellaneous channel type is for any data type that is not a normal video type. The Miscellaneous channel type makes no assumptions on data type and just passes the data to the client and supports a single buffer for the client.
- Free Channel—Used in video compositions. The Free channel data type is always ignored as it uses the same data type of the descriptor that first calls the free channel.

The clients of the VPDMA are the physical connection to the processing modules that source or sinks of the data and control when the channel can be updated. Each client can be configured to have specific start event which allows for the channel data to start flowing to or from the external client. The start event can be selected from one of the signals in the FRAME START Interface or it can be selected by a channel attribute or to be controlled by an internal Frame signal controlled by the List Manager.

The VPDMA controller works on lists of descriptors. Descriptors define how data will be transferred through different channel. In other words, channel is described through a Data Transfer descriptor. The client that the channel is mapped to interprets the information in the descriptor to perform the requested data transfer. List is a group of descriptors that makes up a set of DMA transfers that need to be completed. List can contain any kind of descriptor without limitation and be of any size.

The CPU creates a list of descriptors in DDR in the order it wants them executed. The CPU then writes the location of the list to the LIST_ADDR register, followed by writing the size, type of list and list number of the LIST_ATTR register and posts the list. The List Manager module, which manages different lists, will then schedule a DMA transfer to pull in the portion of the list that it can store in the internal VPDMA memory. The List Manager will sequentially process descriptor in the list and performs the data transfers.

1.1.5 HDVPSS Data Flow

1.1.5.1 Data Flow Control

The VPDMA routes input and output video sources to the starting or ending point of each processing pipeline.

Signal routing within the HDVPSS is controlled by an internal protocol referred to as Video Peripheral Protocol (VPI Protocol). This protocol consists of a NewFrame (NF) signal at the start of each frame which indicates to downstream modules that a frame of data is about to start. On the last signal of a frame, an EndofFrame signal is sent to indicate the last pixel of a frame. In addition to preparing downstream modules for frames of data, the NewFrame signal is used in many modules to stage the memory mapped registers. Each processing module will receive a NewFrame signal, and will generate a NewFrame signal to send to its downstream module. Sections in the register section which refer to New Frame, or NF handling, refer to this signal.

Internal Control is accomplished by configuring the selection of data paths available at the input of each of the multiplexers (see Figure 1-1). This configuration can be done in the CLKC Data Path Select Register. This register controls where internal processing pipes are connected.

1.1.5.2 VCOMP Mux

The video compositor (VCOMP) module takes two inputs: MAIN and PIP. The MAIN input comes from Primary Input Path, and PIP input can be selected from one of three sources: Auxiliary Input Path (AUX), Bypass Path0 (BP0), or Bypass Path1 (BP1). The default for the PIP path is disabled, so there is no PIP input unless it is configured.

1.1.5.3 HD Display Mux

The HD display mux selects a data path for HD displays, which include HDMI/DVO1, and DVO2 outputs. The input data path can be selected from three sources: Auxiliary Input Path (AUX), Bypass Path0 (BP0), or Bypass Path1 (BP1). The default for the input data path is disabled, so no input path is selected unless it is configured.

1.1.5.4 SD Display Mux

The SD display mux selects a data path for SD display that includes SDVENC output. The input data path can be selected from one of four sources: Auxiliary Input Path (AUX), Bypass Path0 (BP0), Bypass Path1 (BP1), or Secondary-1 Input Path (SEC1). The default for the input data path is disabled, so no SDVENC input path is selected unless it is configured.

1.1.5.5 SC_5 Mux

The SC_5 mux selects a data path for writing a processed image back to memory. The input data path for this MUX can be selected from one of six sources:

- HDMI Composited Path Output (from COMP)
- VCOMP Block Output
- Bypass Path0 (BP0)
- Bypass Path1 (BP1)
- Secondary-0 Input Path (SEC0)

The default for the input data path is disabled, so there is no scaler input or output.

1.1.5.6 CSC_VIP Mux

The color space converters (CSC_VIP0 and CSC_VIP1) within the VIP subsystem receive data from one of five sources:

- VIP_PARSER PortA Output (422)
- VIP_PARSER PortB Output (422)

- Secondary Path Output (422): SEC0 for CSC_VIP0 and SEC1 for CSC_VIP1
- VIP_PARSER PortA Output (RGB)
- Compositer Output (RGB) from COMP.

The default for this mux is disabled, so there is no CSC_VIP input.

1.1.5.7 SC_VIP Mux

The scaler modules (SC_VIP0 and SC_VIP1) within the VIP subsystem receive data from one of three sources:

- Color Space Converter Output (from CSC_VIP)
- VIP_PARSER PortA Output
- VIP_PARSER PortB Output
- Secondary Path Output: SEC0 for SC_VIP0 and SEC1 for SC_VIP1

The default for this mux is disabled, so there is no SC_VIP input.

1.1.5.8 VIP RGB Mux

The RGB output of the VIP subsystem can come from one of two sources:

- Compositer Output (from COMP)
- Color Space Converter Output (from CSC_VIP)

1.1.5.9 Video Compositor PIP Input

The Video Compositor PIP input path can come from 1 of 3 sources: The Auxiliary Input Pipe, or from either of the Bypass-422 pipes (non-tiled format). These sources will usually be either the Primary Composited Writeback Path or the memory stored version of the Auxiliary Input Path. However, the only requirement on these two VPDMA input paths is that they have been stored in 422 “private data” format, which is an untiled raster format.

The default for this path is disabled, meaning no PIP input.

1.1.5.10 PIP Display Input

The HD Composite VENC path can come from 1 of 3 sources: The Auxiliary Input Pipe, or from either of the Bypass-422 pipes (non-tiled format). These sources will usually be either the Primary Composited Writeback Path or the memory stored version of the Auxiliary Input Path. However, the only requirement on these two VPDMA input paths is that they have been stored in 422 “private data” format, which is an untiled raster format.

The default for this path is disabled, meaning no input.

1.1.5.11 Standard Definition Video Encoder Input

The standard definition vdeo encoder (SD VENC) input path can come from 1 of 4 sources: The auxiliary input pipe, the secondary-2 input pipe or one of the two bypass-422 input pipes. These sources will usually be either the primary composited writeback path or the memory stored version of the Auxiliary Input Path. However, the only requirement on these two VPDMA input paths is that they have been stored in 422 “private data” format, which is an untiled raster format.

The default for this path is disabled, meaning no SD VENC input.

1.1.5.12 Primary Composited Writeback Scaler Input

The primary composited writeback scaler Input is used to scale the primary input path (normally HD) and send to memory so that this data can be fed back into the HDVPSS for display on either the high-definition VENC or standard-definition VENC. The input to this scaler can come from 1 of 6 sources: the output of the video compositor, the composited HDMI output, one of the two bypass-422 paths, or the secondary-1 input.

The default for this path is disabled, meaning no scaler input (or output).

1.1.5.13 Video Input Port Color Space Converter Input (2)

The color space converters within the video inputs ports can come from 1 of 3 sources: The Video Input Port Parser (VIP_PARSER), the composited HD DAC output or from either the Primary Input DEI (Video Input Port 0) or the Auxiliary Input DEI (Video Input Port 1). The feeds from the primary and auxiliary DEIs are for dual stream transcode (Secondary Input Paths) with write back to memory as RGB data.

The default for this path is disabled, meaning no CSC input (or output).

1.1.5.14 Video Input Port Scaler Input (2)

The scalers within each of the video input ports can come from 1 of 3 sources: The Video Input Port Parser (A or B channel), the Video Input Port Color Space Converter or either the Primary Input DEI (Video Input Port 0) or either the Auxiliary Input DEI or Secondary Video Path Input (Video Input Port 1). The feeds from the Primary and Auxiliary input DEIs are for dual stream transcoding purposes.

The default for this path is disabled, meaning no scaler input.

1.1.5.15 Video Input Port RGB Output (2)

The RGB output of the Video Input Port can come from 1 of 2 sources: The Video Input Port Parser or the Video Input Port Color Space Converter. The feed from the Video Input Port Color Space Converter are for dual stream transcode (via Secondary Input Path) with write back to memory as RGB data. The source of this data is either the Primary Input DEI (Video Input Port 0) or the Auxiliary Input DEI (Video Input Port 1). When the source of the Video Input Port Color Space Converter is set to one of the DEI inputs, this mux will pass the output of the Color Space Converter out instead of the output of the Video Input Port Parser.

The default for this path is from the Video Input Port Parser (VIP_PARSER).

1.1.5.16 Noise Filter Output

The Noise Filter Output can come from 1 of 2 inputs: The Noise Filter or from the Noise Filter Chroma Downsampler (allowing this chroma downsampler to be used standalone).

The default for this path is connected to the Noise Filter output.

1.1.5.16.1 Data Formats

The following section describes the data formats for the HDVPSS. Each of the channels has a type of data that it can support based upon the client that it services. Also, for each channel the data type will assume that data is packed in memory a certain way and will be presented to the client in the same manner no matter what the format of the data in memory.

The YUV formatted channels expect video data that is in YUV color space. The YUV data type is for YUV data and it can support both interleaved data where Luma and Chroma are in the same data buffer or it can support co-planar data where the Luma and Chroma are in separate data buffers. The YUV channel also can be configured to give a different start position for the client instead of the default upper left hand corner of the frame. The storage format for YUV data depends on the data type field. The data type must be set to a data type that the channel can support. All the clients that data are provided to will either accept Luma Only, Chroma Only or Luma and Chroma in a parallel data bus.

The data formats in Figure 1-5 map as follows:

422P data:

- 422 interleave non-tiled (luma and chroma interleaved in the same buffer)

422S data:

- 422 semi-planar tiled/non-tiled (separate luma and chroma buffers). Cb/Cr interleaved in chroma buffer.

420T data:

- 420 semi-planar tiled/non-tiled (separate luma and chroma buffers). Cb/Cr interleaved in Chroma buffer.

RGB data:

- All types of RGB formats described in VPDMA section.

Each of these data formats are discussed in the VPDMA data formats section.

1.1.6 Example Data Flows

Several concurrent data flows within the HDVPSS are possible. The following sections outline several of the possible data flow scenarios capable within the HDVPSS, including the HDVPSS level mux register selections required for the flow. The flows shown are not all encompassing, and there are variations within each. For example, the first data flow shown is Dual Display. Single Display is also possible. Dual Transcode (Secondary Input Path 1 and 2) is possible, or Single Transcode (Secondary Input Path 1). Transcode is possible without display, etc.

1.1.6.1 Dual Display

A standard dual display data flow is shown in Figure 1-5.

In this case, the primary display (HDMI) contains two video sources in a Picture-in-Picture format. On the secondary HD display, the auxiliary display is being shown.

Figure 1-5. HDVPSS Dual Display (PIP) Data Flow

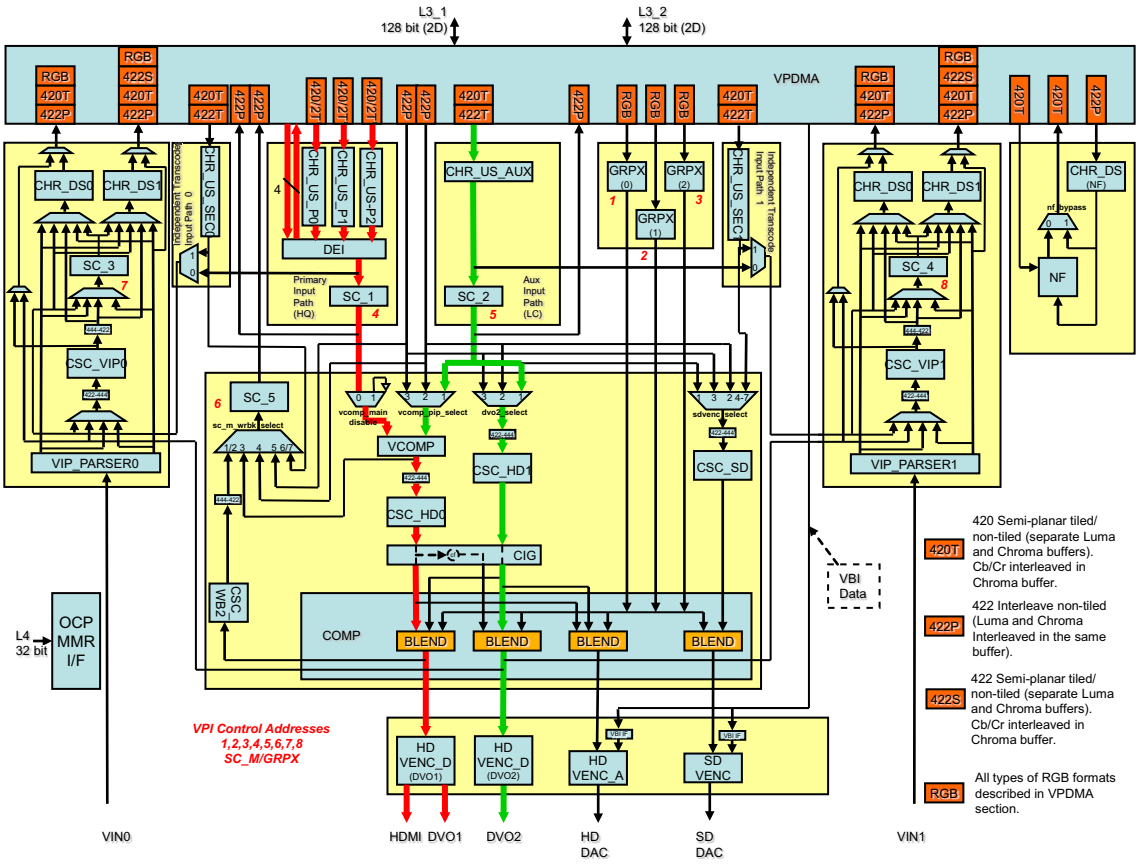


Table 1-4. HDVPSS Mux Select Register 1

HDVPSS Mux Select Register	Value Required
vcomp mux select	1
hdcomp mux select	1
sd mux select	0
sc_5 mux select	0
sec0 mux select	0
sec1 mux select	0
csc_vip0 mux select	0
sc_vip0 mux select	0
chr_ds0_vip0 mux select	0
chr_ds1_vip0 mux select	0
csc_vip1 mux select	0
sc_vip1 mux select	0
chr_ds0_vip1 mux select	0
chr_ds1_vip1 mux select	0

1.1.6.2 Tri Display

There are several display configurations for the Tri-Display format.

The first configuration, Figure 1-6, shows the auxiliary video path on the SD display. In this case, graphics overlays are also being applied to each video encoder output. Because HD DV02 and SD DAC paths are sharing the same input (meaning same size and interlaced format), they share a graphics input. In this case, because the SD path must be interlaced, all video paths must be interlaced.

The second configuration, Figure 1-7, shows the HDMI composited Picture-in-Picture display content on the SD display. In this case, the three output displays are independent. The SC WRBK scaler will be used to scale the primary blended display and convert to interlaced format for the SD output.

Figure 1-6. HDVPSS Tri Display Data Flow 1

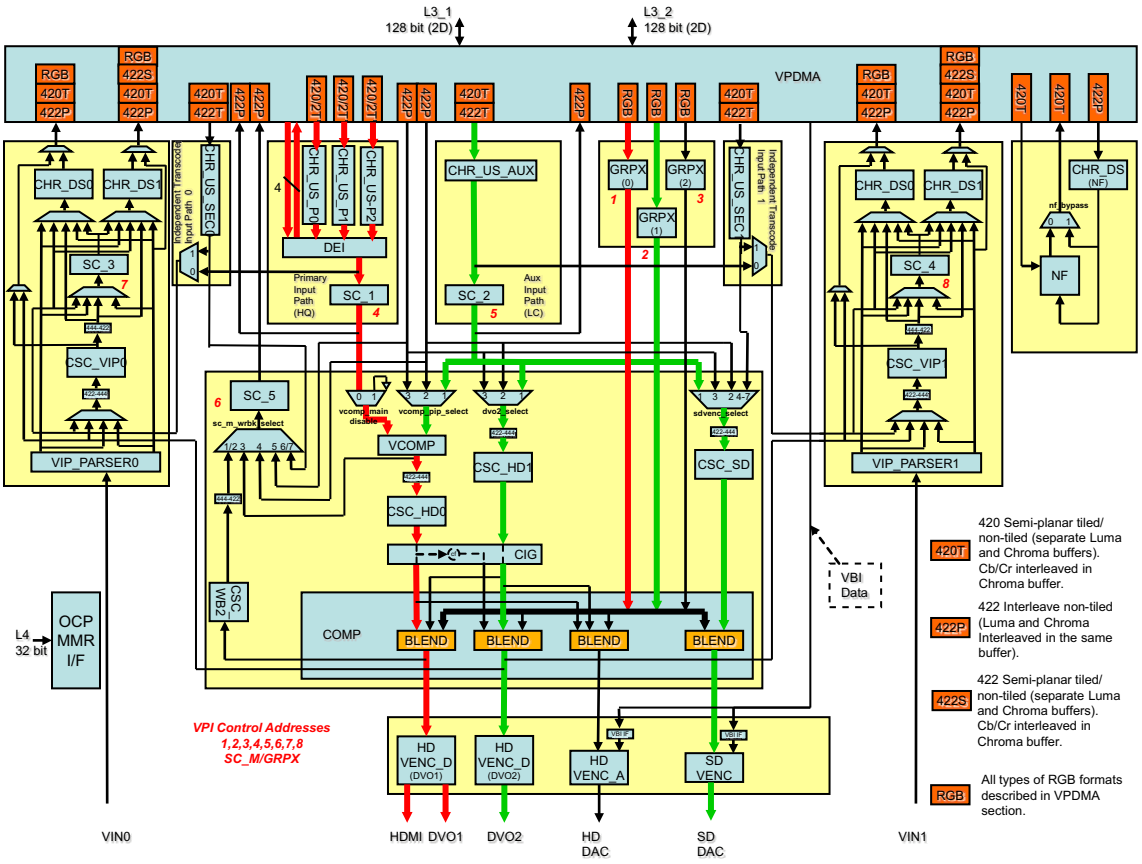


Table 1-5. HDVPSS Mux Select Register 2

HDVPSS Mux Select Register	Value Required
vcomp mux select	1
hdcomp mux select	1
sd mux select	1
sc_5 mux select	0
sec0 mux select	0
sec1 mux select	0
csc_vip0 mux select	0
sc_vip0 mux select	0
chr_ds0_vip0 mux select	0
chr_ds1_vip0 mux select	0
csc_vip1 mux select	0
sc_vip1 mux select	0
chr_ds0_vip1 mux select	0
chr_ds1_vip1 mux select	0

Figure 1-7. HDVPSS Tri Display Data Flow 2

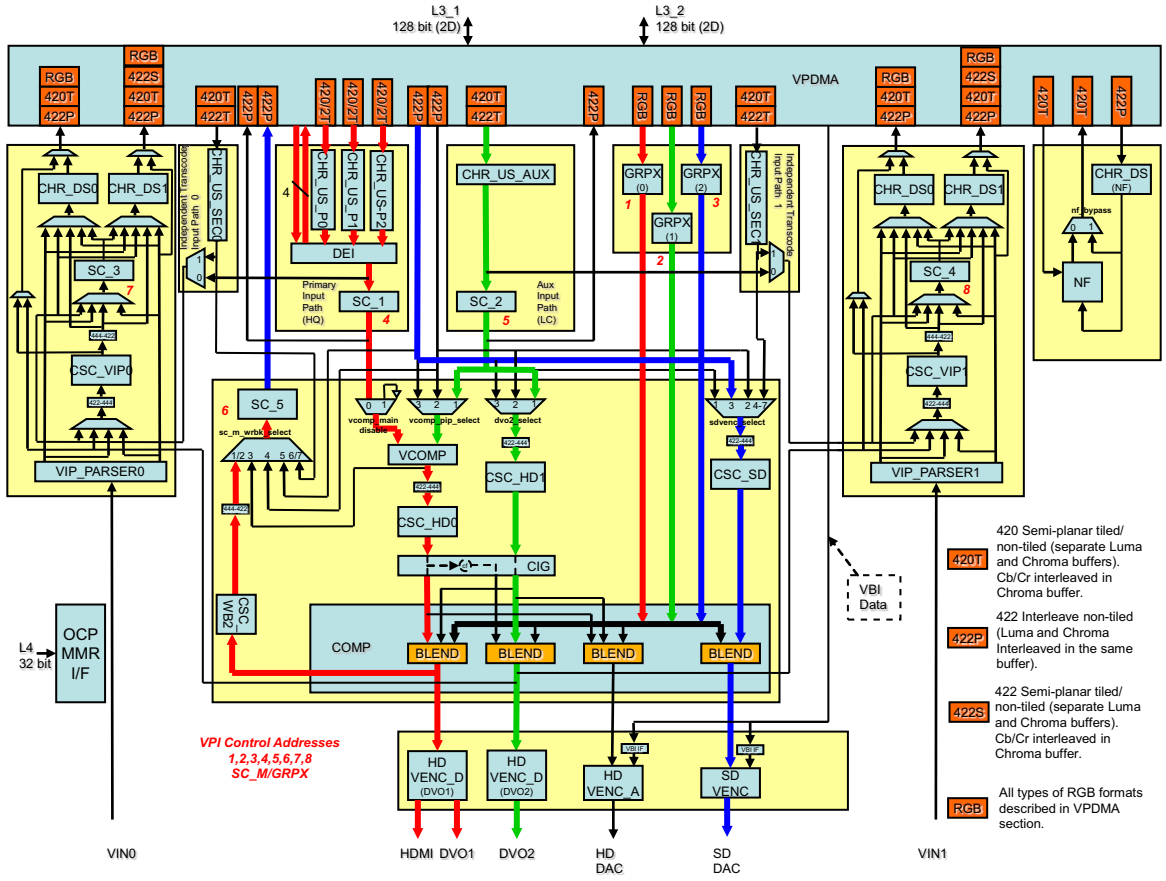


Table 1-6. HDVPSS Mux Select Register 3

HDVPSS Mux Select Register	Value Required
vcomp mux select	1
hdcomp mux select	1
sd mux select	2
sc_5 mux select	1
sec0 mux select	0
sec1 mux select	0
csc_vip0 mux select	0
sc_vip0 mux select	0
chr_ds0_vip0 mux select	0
chr_ds1_vip0 mux select	0
csc_vip1 mux select	0
sc_vip1 mux select	0
chr_ds0_vip1 mux select	0
chr_ds1_vip1 mux select	0

1.1.6.3 Tri Display and Dual Transcode

In addition to display, each video source can be transcoded while being displayed through the use of the Secondary Input Paths.

Either or both video sources can be transcoded while simultaneously being displayed.

Figure 1-8. HDVPSS Tri Display Dual Transcode

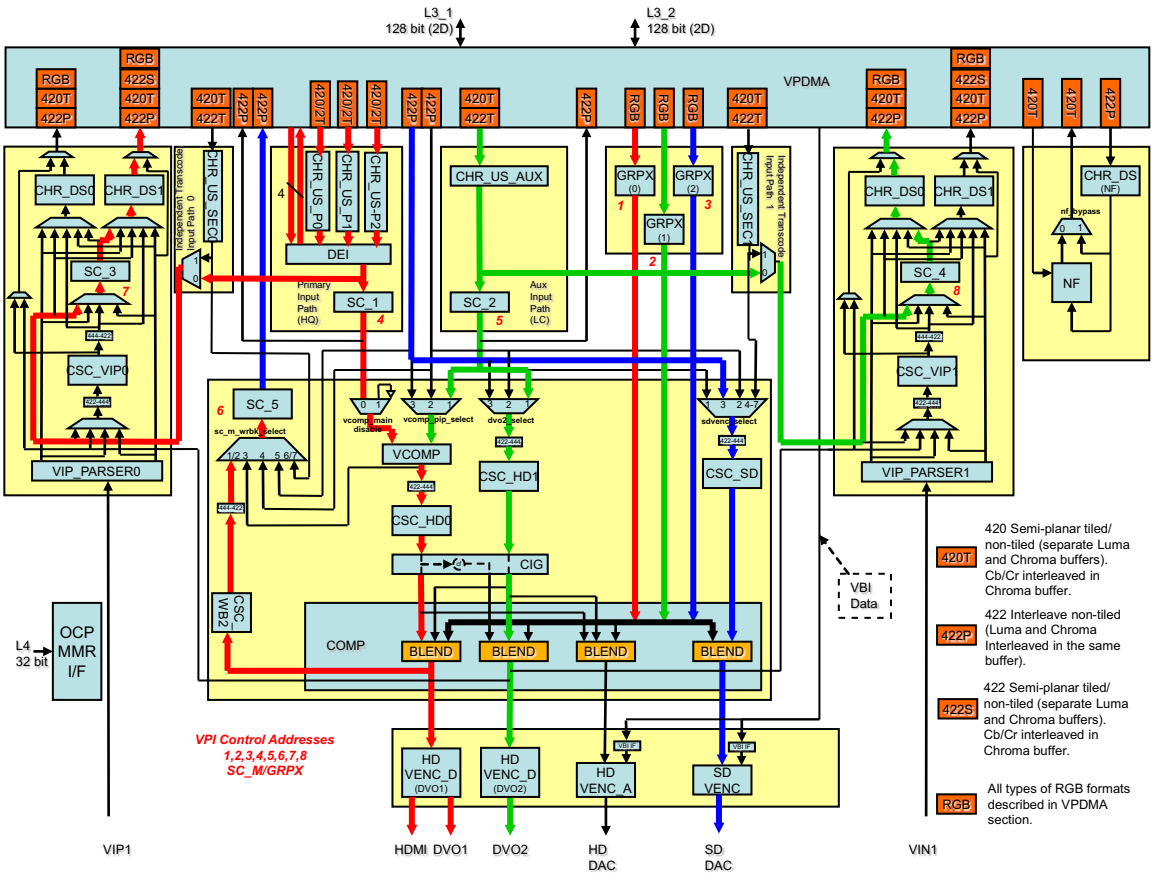


Table 1-7. HDVPSS Mux Select Register 4

HDVPSS Mux Select Register	Value Required
vcomp mux select	1
hdcomp mux select	1
sd mux select	2
sc_5 mux select	1
sec0 mux select	0
sec1 mux select	0
csc_vip0 mux select	0
sc_vip0 mux select	4
chr_ds0_vip0 mux select	0
chr_ds1_vip0 mux select	1
vin0_rgb_out_hi_select	0
vin0_rgb_out_lo_select	0
vin0_multi_channel_select	0
csc_vip1 mux select	0
sc_vip1 mux select	4
chr_ds0_vip1 mux select	1
chr_ds1_vip1 mux select	0
vin1_rgb_out_hi_select	0
vin1_rgb_out_lo_select	0
vin1_multi_channel_select	0

1.1.6.4 Tri Display, Dual Transcode, and Video Capture

The Video Input Port has the capability to capture either one or two video sources. In the previous case, only one video source can be captured per Video Input Port, since the other path is dedicated to transcode. Also in this case, video captured cannot be resized.

Figure 1-9. HDVPSS Tri Display Dual Transcode with Video Capture

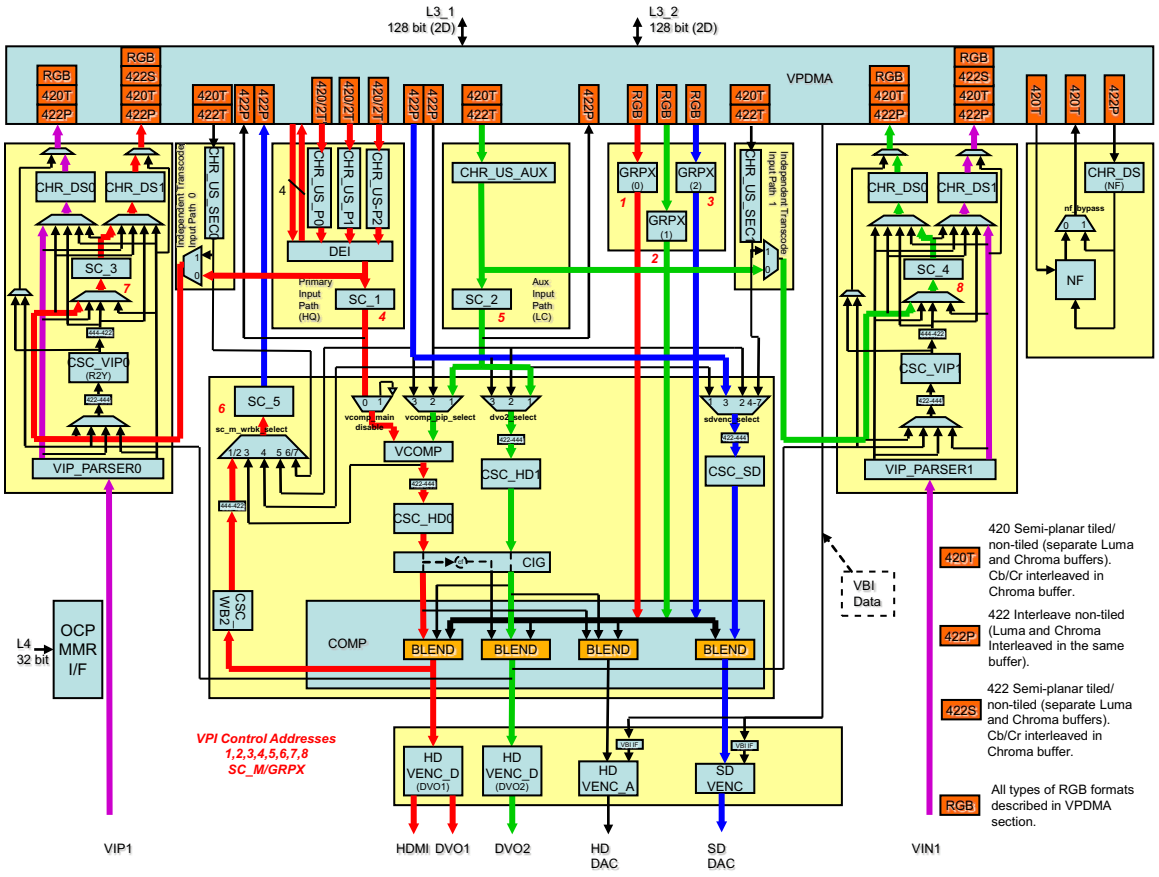


Table 1-8. HDVPSS Mux Select Register 5

HDVPSS Mux Select Register	Value Required
vcomp mux select	1
hdcomp mux select	1
sd mux select	2
sc_5 mux select	1
sec0 mux select	0
sec1 mux select	0
csc_vip0 mux select	0
sc_vip0 mux select	4
chr_ds0_vip0 mux select	3
chr_ds1_vip0 mux select	1
vin0_rgb_out_hi_select	0
vin0_rgb_out_lo_select	0
vin0_multi_channel_select	0
csc_vip1 mux select	0
sc_vip1 mux select	4
chr_ds0_vip1 mux select	1
chr_ds1_vip1 mux select	3
vin1_rgb_out_hi_select	0
vin1_rgb_out_lo_select	0
vin1_multi_channel_select	0

1.1.6.5 Tri Display and Video Capture

As can be seen in Figure 1-10, as long as there is no transcode operations, video display and video capture are independent. In this usage, up to four video sources can be captured (two per video input port) while display is active.

To improve the quality of captured video sources, the Noise Filter (NF) can be used on captured video (see Figure 1-11). This Noise Filter is a memory to memory operation, meaning that captured video goes to memory, and then is read back into to the Noise Filter, operated on, and written back to memory. The below diagram shows this flow (with display active).

Figure 1-10. HDVPSS Tri Display with Video Capture

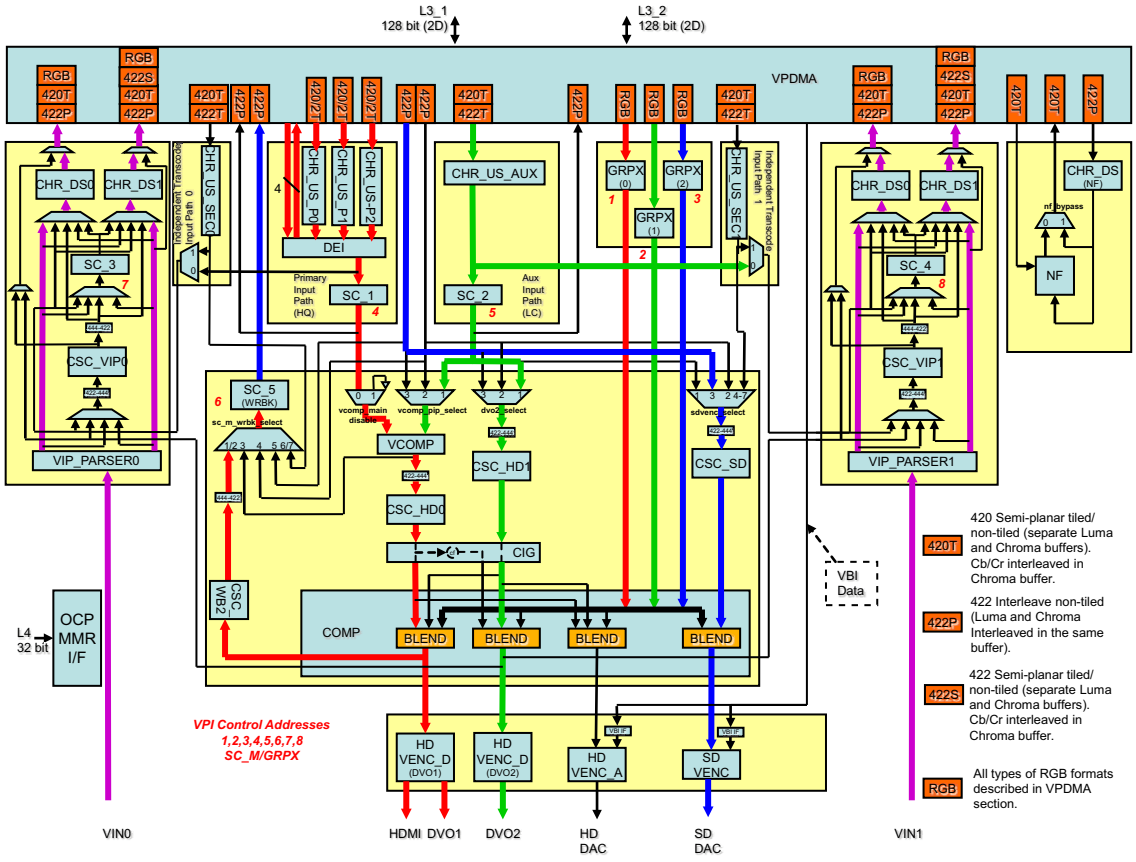


Table 1-9. HDVPSS Mux Select Register 6

HDVPSS Mux Select Register	Value Required
vcomp mux select	1
hdcomp mux select	1
sd mux select	2
sc_5 mux select	1
sec0 mux select	0
sec1 mux select	0
csc_vip0 mux select	0
sc_vip0 mux select	0
chr_ds0_vip0 mux select	3
chr_ds1_vip0 mux select	4
vin0_rgb_out_hi_select	0
vin0_rgb_out_lo_select	0
vin0_multi_channel_select	0
csc_vip1 mux select	0
sc_vip1 mux select	0
chr_ds0_vip1 mux select	3
chr_ds1_vip1 mux select	4
vin1_rgb_out_hi_select	0
vin1_rgb_out_lo_select	0
vin1_multi_channel_select	0

Figure 1-11. HDVPSS Tri Display with Video Capture and Noise Filter

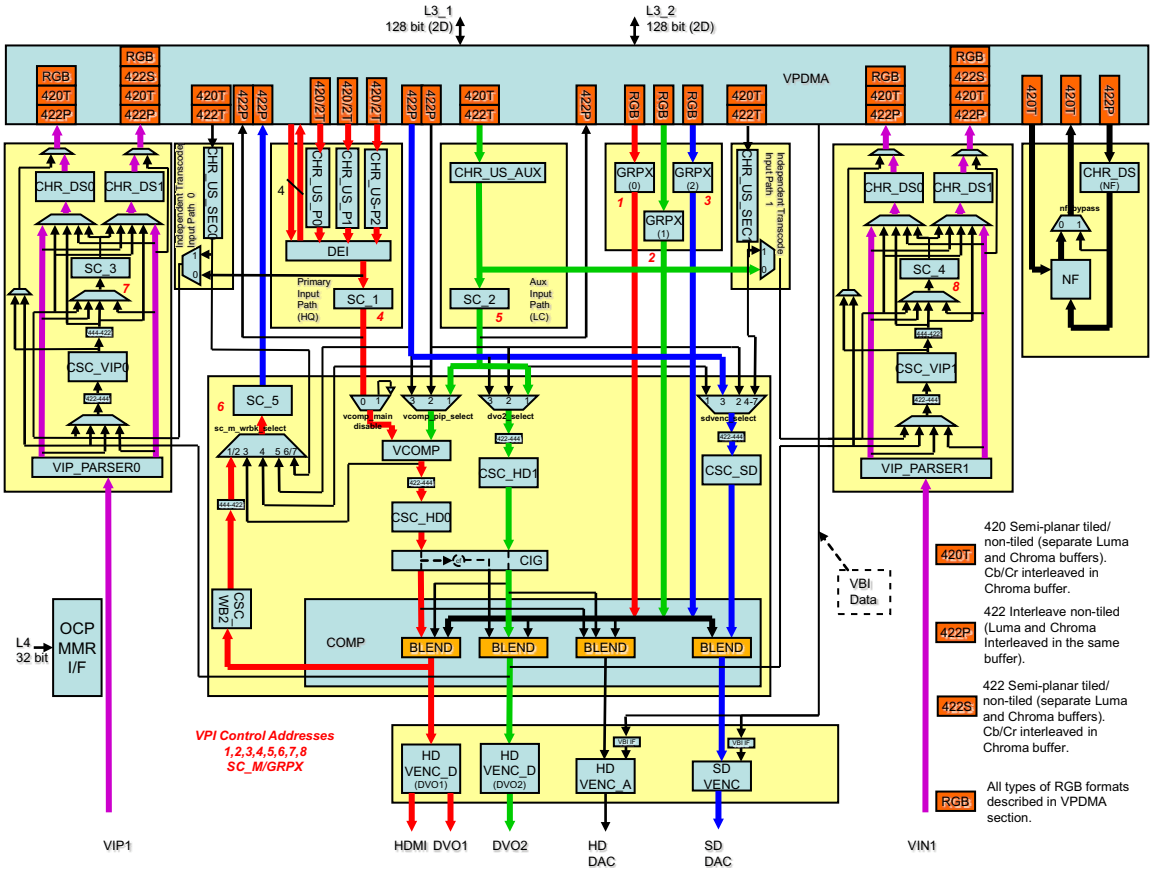


Table 1-10. HDVPSS Mux Select Register 7

HDVPSS Mux Select Register	Value Required
vcomp mux select	1
hdcomp mux select	1
sd mux select	2
sc_5 mux select	1
sec0 mux select	0
sec1 mux select	0
csc_vip0 mux select	0
sc_vip0 mux select	0
chr_ds0_vip0 mux select	3
chr_ds1_vip0 mux select	4
vin0_rgb_out_hi_select	0
vin0_rgb_out_lo_select	0
vin0_multi_channel_select	0
csc_vip1 mux select	0
sc_vip1 mux select	0
chr_ds0_vip1 mux select	3
chr_ds1_vip1 mux select	4
vin1_rgb_out_hi_select	0
vin1_rgb_out_lo_select	0
vin1_multi_channel_select	0

1.1.7 Interrupt Mapping

HDVPSS generates four interrupts which can be mapped different processors as listed in Table 1-11.

Table 1-11. HDVPSS Interrupts

Interrupt No.	Interrupt Name (INTRx)	Mapped Processor	MMR Address Offset Range
0	INTR0	Cortex-A8	0x20 - 0x3F
1	INTR1	GEM	0x40 - 0x5F
2	INTR2	Media controller processors	0x60 - 0x7F
3	INTR3	Media controller processors	0x80 - 0x9F

Interrupts INTR2 and INTR3 are mapped to both media controller processors (Video Media Controller and HDVPSS Media Controller).

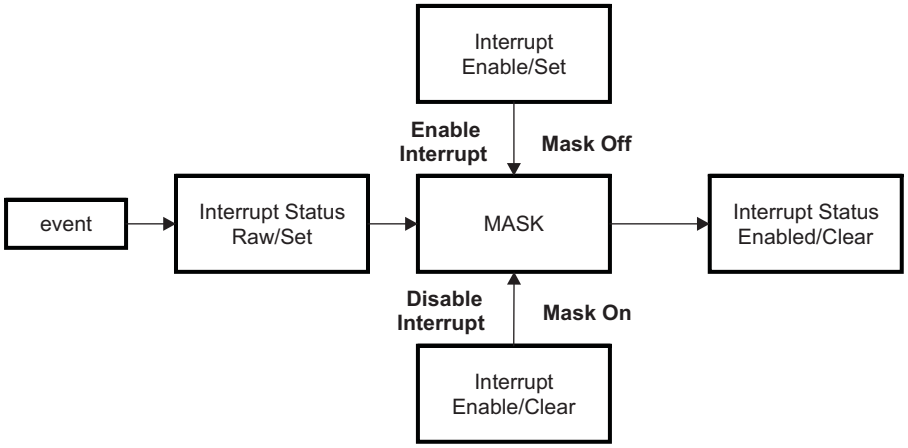
The configuration of each of the above interrupts (INTRx) is controlled by the MMR present in the offset address range mentioned above in INTC (offset: 0x0100) module.

The following group of MMR constitutes the configuration of interrupts.

- Interrupt Status Raw/Set
- Interrupt Status Enabled/Clear
- Interrupt Enable/Set
- Interrupt Enable/Clear

Figure 1-12 shows the functionality of these MMR.

Figure 1-12. MMR Functionality



1.1.7.1 Status Before Mask

Interrupt Status Raw/Set register bit-fields show the status of interrupts before the MASK. A bit-field is set to ‘1’ when either an event happened on the signal mentioned in the corresponding bit-field or manual write of ‘1’ to the corresponding bit-field. Writing ‘0’ has no effect.

1.1.7.2 Status After Mask

Interrupt Status Enabled/Clear register bit-fields show the status of interrupts after the MASK. The value of Interrupt Status Raw/Set register is transferred to Interrupt Status Enabled/Clear register for the bit-fields with MASK off. Writing ‘1’ to a bit-field clears its value to ‘0’ and also clears the corresponding bit-field in Interrupt Status Raw/Set register.

1.1.7.3 Mask OFF (Enable Interrupt)

Interrupt Enable/Set register is used to disable the MASK for selected signals in Interrupt Status Raw/Set register. Writing ‘1’ to a bit-field enables corresponding interrupt to propagate to the processor. Writing ‘0’ has no effect.

1.1.7.4 Mask ON (Disable Interrupt)

Interrupt Enable/Clear register is used to enable the MASK for selected signals in Interrupt Status Raw/Set register. Writing ‘1’ to a bit-field disables corresponding interrupt to the processor. Writing ‘0’ has no effect.

Please note that all interrupts are disabled by default.

There are 50 interrupts that can be mapped to each INTRx at HDVPSS level and everyone of the four INTRx has access to all the 50 available interrupts. One ‘bit’ is allocated for each interrupt in the MMR and spread across two memory mapped registers (Register0 and Register1) to fit in all the 50 interrupts.

The source of interrupts described at HDVPSS level come from Sub-Modules of HDVPSS like VPDMA, DEI, VIP0, etc. Figure 1-13 shows interrupt mapping from module level to HDVPSS level.

Figure 1-13. Module to HDVPSS Interrupt Mapping Level 1

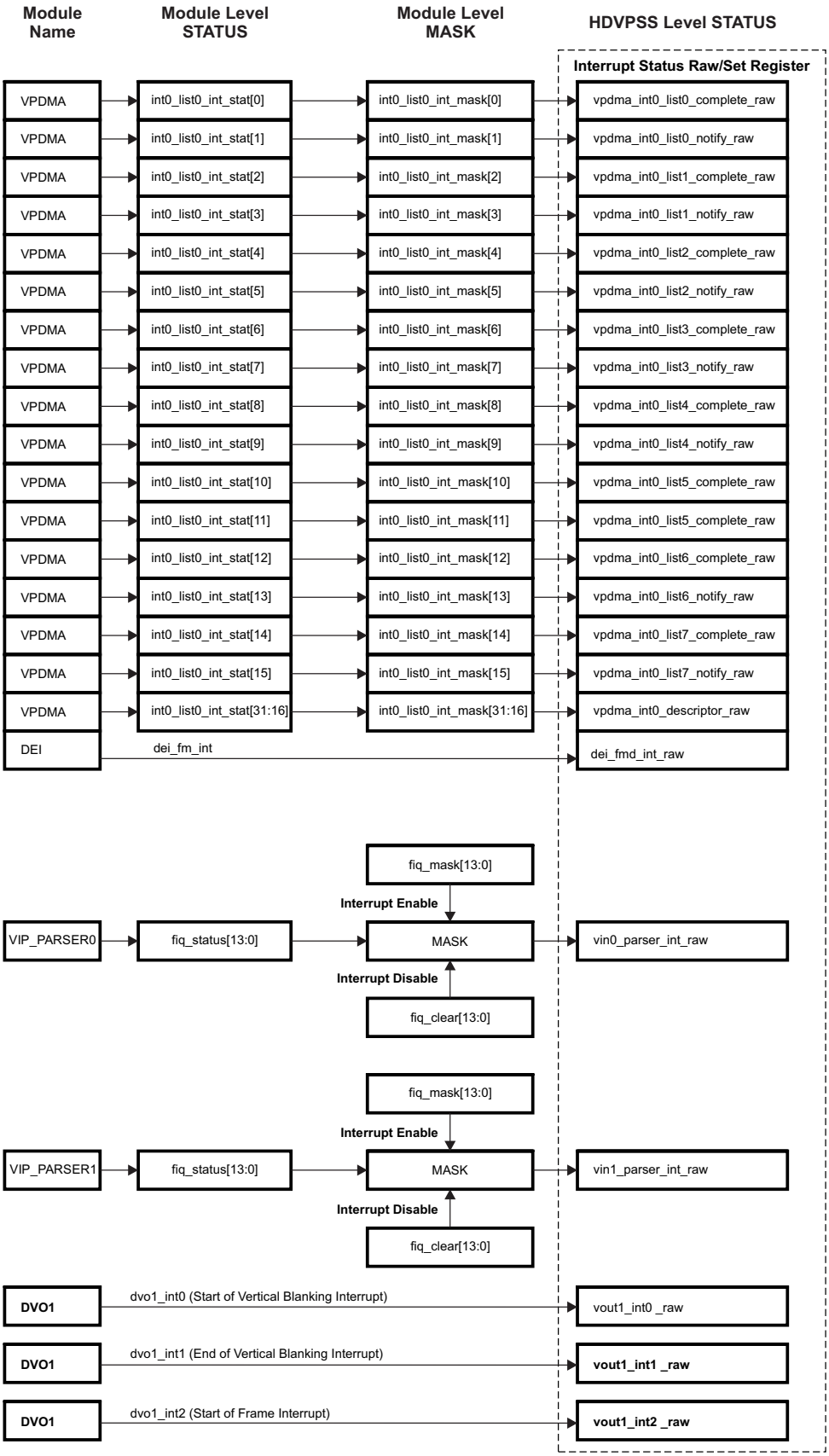
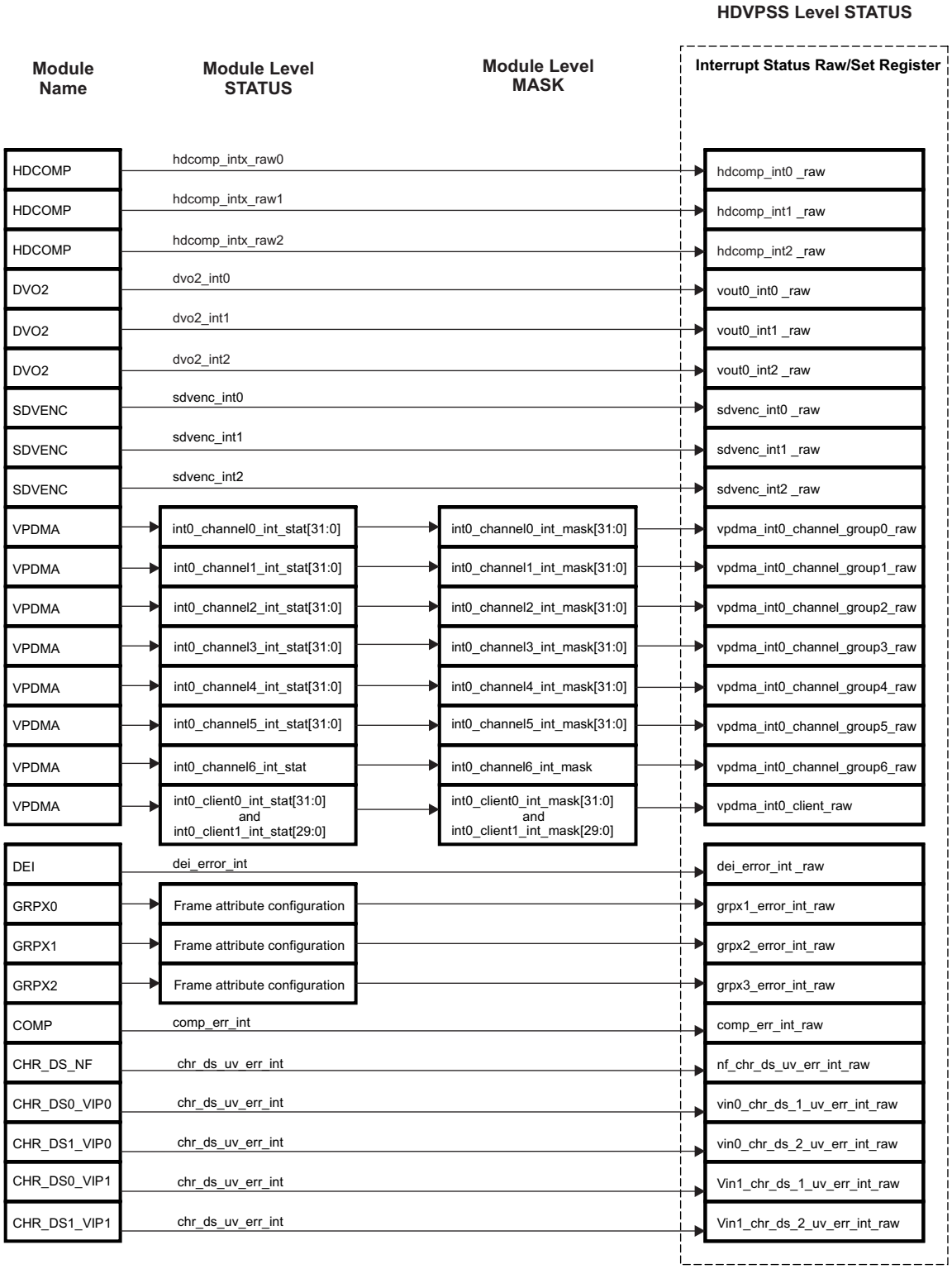


Figure 1-14. Module to HDVPSS Interrupt Mapping Level 2



1.1.8 Clocking

The following section discusses the steps needed to enable HDVPSS clocking.

1.1.8.1 Enable PRCM for HDVPSS Module

Please refer to the *PRCM* chapter to enable PRCM for HDVPSS.

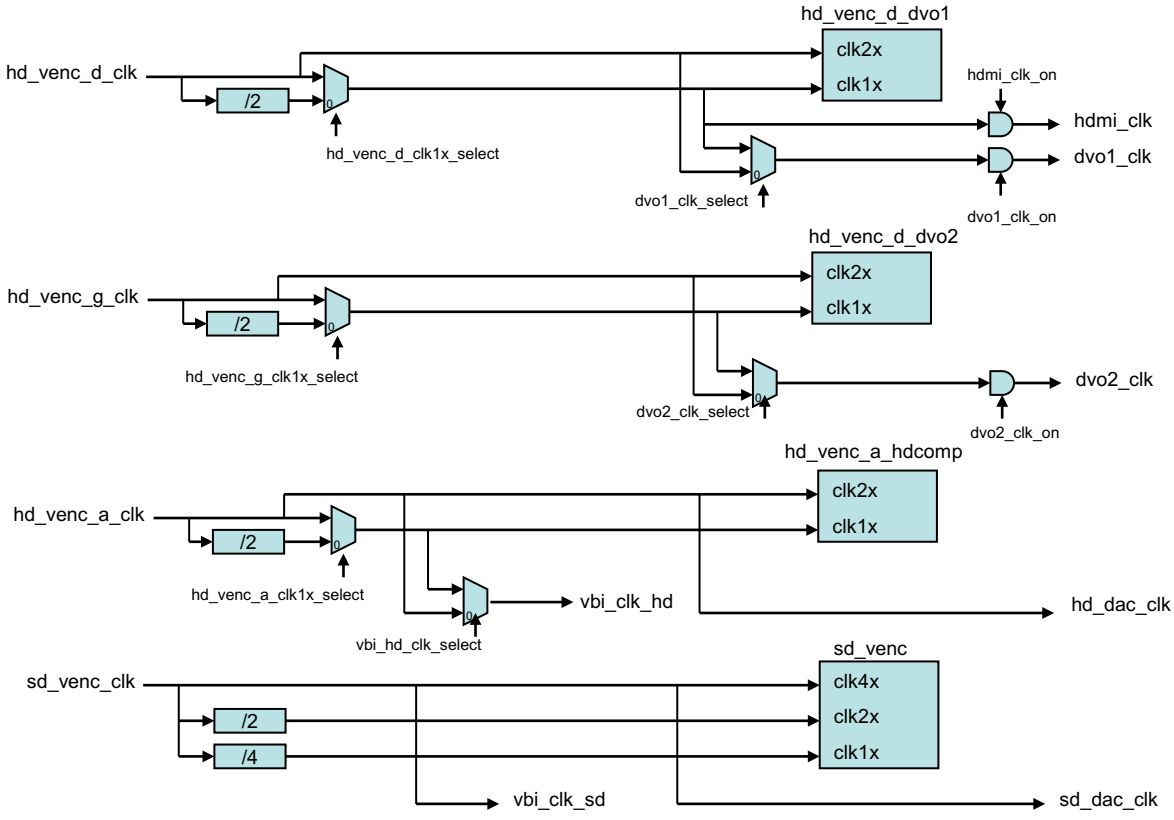
1.1.8.2 Enable HDVPSS Internal Clocks

In HDVPSS, some of the data paths and modules are divided into different clock domains. This enables the user to switch off the paths/modules that are not used, at HDVPSS level. The CLKC→CLKC Module Clock Enable Register (address: 0x48100100) is used to enable the paths that fall in separate clock domains (as mentioned in the CLKC register).

1.1.8.3 VENC Clock Source (HDMI or DVO1/DVO2/HDCOMP/SDVENC Pixel Clock)

Figure 1-15 shows the derivation of pixel clock for different VENCs. In this figure, hd_venc_d_clk (external clock source) directly drives the HDMI/DVO1 (hd_venc_d) video encoder , hd_venc_a_clk(external clock source) directly drives the HDCOMP(hd_venc_a) video encoder, and hd_venc_g_clk (external clock source) directly drives the DVO2 (hd_venc_d) video encoder.

Figure 1-15. Video Encoder Clock/Control Diagram



The output of the muxes (shown in the above diagram) can be controlled in the CLKC Video Encoder Clock Select (address: 0x48100114) register. Please make sure the required VENCs are enabled in the CLKC Video Encoder Enable (address: 0x48100118) register.

1.1.9 Reset

HDVPSS provides separate resets for each of the paths/modules.

The following sequence is used to reset the entire HDVPSS module:

1. Take VPDMA to standby via force standby MMR write. This disconnects master ports.
2. Ensure all VENCs are disabled via MMR writes.
3. Power down VENCs via appropriate MMR writes.
4. Shut down VENC clocks via MMR writes.
5. Shut down VIP clocks.
6. Shut down all module clocks by writing to all enable bits.
7. Reset all modules and Vencs by writing reset bits.
8. Request IDLE, on IDLE acknowledgement, clocks can be shut down.

1.2 Internal Modules

This section describes the internal modules of the high-definition video processing subsystem (HDVPSS).

1.2.1 Chroma Up-Sampler (CHR_US)

The chroma up-sampler (chr_us) module is used to convert from YCbCr 4:2:0 data format input to YCbCr 4:2:2 format output.

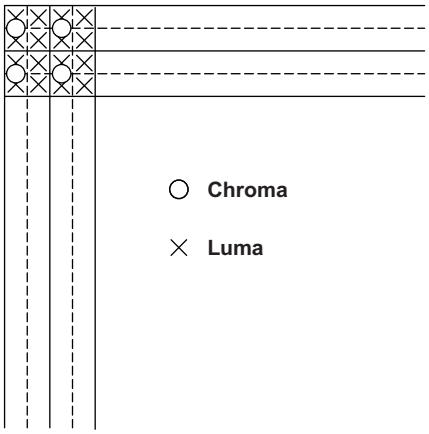
1.2.1.1 Features

- Supports both interlaced and progressive inputs
- 4-tap interpolation filtering
- Filter coefficients are all programmable
- Four sets of coefficients (each set has four coefficients) corresponding to anchor pixels and interpolated pixels of top field and bottom field
- For progressive inputs, the coefficients corresponding to top and bottom field must be identical
- Each coefficient is 14 bit (4.10 format)
- Default filter coefficients are based on Catmull-Rom algorithm
- Capable of removing the half pel vertical offset so all chroma samples are on-grid. This step ensures that the output does not suffer from any kind of rainbow effect due to chroma-upsampling.
- Provides a 10-bit interface in both directions: 10-bit input and 10-bit output
- Support bypass mode for 4:2:2 input

1.2.1.2 Functional Description

The YUV420 input to Chroma Upsampler module must be in the format shown in Figure 1-16, in which the chroma sample lies in the left column of a 2x2 pixel block with half pel vertical shift.

Figure 1-16. 4:2:0 YCrCb Color Space with Chroma Left-aligned



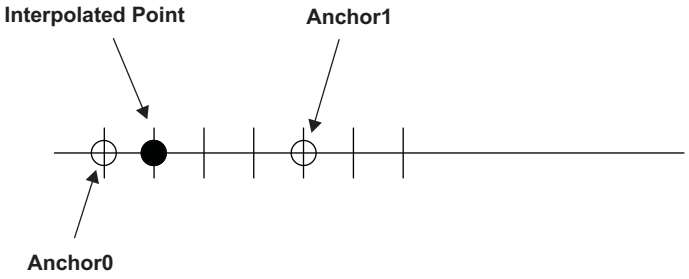
The upsampling is performed by an interpolation filter which uses Catmull-Rom algorithm. The Catmull-Rom Filter is based on four anchor pixels representing a four tap filter. The general 4-tap filter Catmull-Rom filter is defined in Figure 1-17.

Figure 1-17. Catmull-Rom Filter Definition

$$[\,1 \quad x \quad x^2 \quad x^3\,] * \begin{bmatrix} 0 & 1 & 0 & 0 \\ -a & 0 & a & 0 \\ 2a & -3+a & 3-2a & -a \\ -a & 2-a & -(2-a) & a \end{bmatrix}$$

In the previous figure, x is the distance to the interpolated point between the two anchor points. In Figure 1-18, the example shows the desired interpolated point to be ¼ of the distance between Anchor0 and Anchor1. Thus, x = ¼.

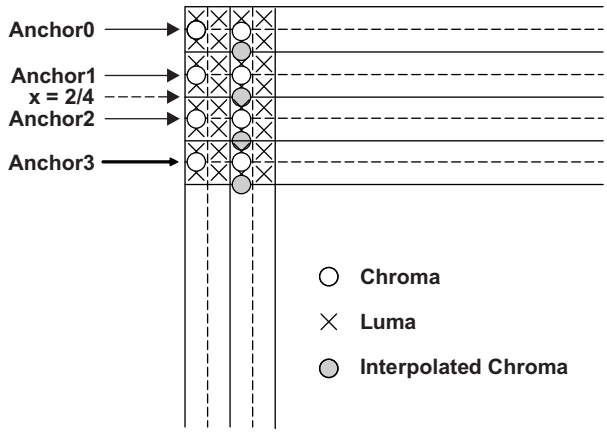
Figure 1-18. Definition of 'X'



The variable 'a' determines the characteristics of the filter. a = ½ is generally used because the filter will produce an interpolated output that is an exact match to a linear input curve. In the literature, some people have noted that a=0.75 or a=1.0 may be more pleasing to the eye. In the implementation, the filter coefficients are programmable through MMR.

For the interpolated pixel, the variable x defines the positional offset relative to anchor pixel1. Figure 1-19 shows four anchor pixels with Anchor0 being near the top of the image and Anchor3 near the bottom. x is relative to Anchor1. Positive values of x goes down towards Anchor3. Negative x values imply a direction towards Anchor0. For example, if we want to interpolate a pixel midway between Anchor1 and Anchor2, x would be 2/4=1/2. There are four half pels between Anchor1 and Anchor2. Midway is two pels, so x=2/4.

Figure 1-19. Anchor Pixels



In the implementation, we need to interpolate the anchor pixel to get it on-grid. Then, we also need to interpolate a completely new pixel for YPrPb 4:2:2.

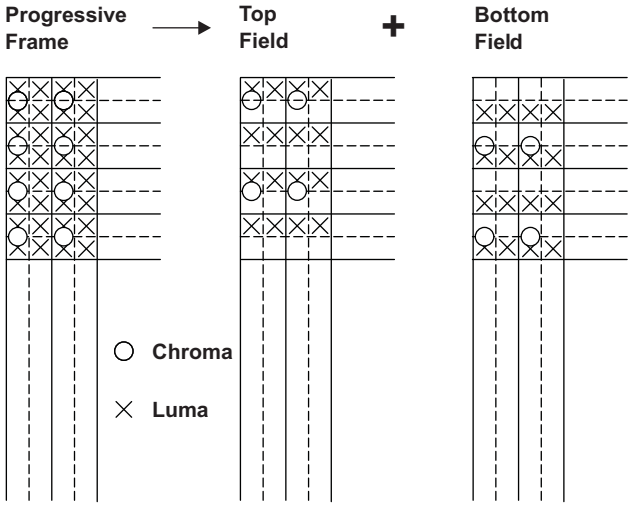
For a progressive input, x = -1/4 for getting the anchor pixel on-grid. x = 1/4 for generating the new pixel.

Lines are scanned from the top of the picture to the bottom.

1.2.1.2.1 For Interlaced YUV420 Input Data

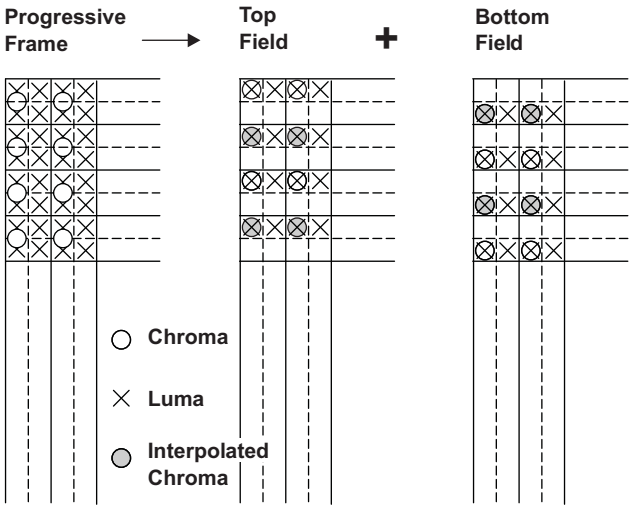
Figure 1-20 shows how 4:2:0 video is split into top and bottom fields in interlaced format. Chroma is attached to alternating Luma lines in the top and bottom fields such that color is equally spread out between the top field and the bottom field. This 4:2:0 interlaced chroma representation is shown in the following figure.

Figure 1-20. 4:2:0 Interlaced Scan



In each interlaced field, the chroma anchor points are separated by 4 pixel lines, or 8 half pels. The 4:2:2 chroma interpolated color space representation of interlaced pictures is shown in Figure 1-21.

Figure 1-21. Ideal 4:2:2 Chroma Upsampling for Interlaced Scan



Following interpolation, the chroma samples lie on a 4:2:2 grid.

Anchor pixels for the top field have been sited up by half a pel (x = -1/8). The new interpolated pixel is sited 3 half pels (x=3/8) down. Samples from the top field are distinct from samples in the bottom field.

For the bottom field, anchor pixels are sited 3 half pels up (x = -3/8). The new interpolated pixel is sited 1 half pel down (x=1/8).

The chroma upsampling filter accepts different coefficients for the top field and the bottom field. In the case of progressive input, the coefficients for the top field and bottom field must be the same.

It should be noted that a different implementation could have been chosen to use the same coefficients for the top and bottom fields. Instead of pushing pixels from the top to bottom of a picture, it can be shown that pushing the bottom field through the upsampling filter from the bottom to the top of the picture permits using the same values for x as in the top field case.

1.2.1.2.2 Edge Effects

Several methods with increasing levels of difficulty resulting in increasing quality can be employed to deal with chroma pixels near the edges. In this module, the edge pixels can be mathematically approximated using the same filter as the rest of the picture. Edge pixels are duplicated going into the filter.

1.2.1.2.3 Modes of Operation (VPDMA)

In both primary (PRI) and auxiliary (AUX) paths, the mode in which the VPDMA needs to be operated depends whether the chroma upsampler and de-interlacers are enabled or not. Table 1-12 shows the modes of operation.

Table 1-12. VPDMA Modes of Operation

Input data is 4:2:0	Input data is 4:2:2
Mode A	Mode B

These modes need to be set in the following register bit-fields of particular instances being used:

CHR_US_reg0.cfg_mode

Line_mode bitfield in VPDMA registers of format RD_LB_CLIENT_CTL_STATUS need to configured as follows:

Mode A corresponds to MMR value 0
Mode B corresponds to MMR value 1

The following are the VPDMA client related bit-fields that need to be configured:

VPDMA_pri_chroma_cstat.line_mode
VPDMA_aux_chroma_cstat.line_mode
VPDMA_sec0_chroma_cstat.line_mode
VPDMA_sec1_chroma_cstat.line_mode
VPDMA_pri_luma_cstat.line_mode
VPDMA_aux_luma_cstat.line_mode
VPDMA_sec0_luma_cstat.line_mode
VPDMA_sec1_luma_cstat.line_mode

Important Notes:

1. For VPDMA luma clients, Mode B should always be used.
2. For VPDMA chroma clients, Mode A is used for 420 data and Mode B is used for 422 data.

1.2.1.2.4 Coefficient Configuration

The filter coefficients are left-aligned 14-bit binary values in signed Q4.10 format. The decimal point is between bits 9 and 10 using the convention of the least significant bit being at position zero. The most significant bit, 13, is the sign bit.

In the register map, the most significant nibble of the coefficient is the sign and the integer portion of the value. The next 10 bits represent the fractional portion of the coefficient value.

Chroma upsampling requires two sets of coefficients. Each coefficient set is comprised of four 14-bit Q4.10 values. One set is used for the top field of an interlaced picture, and the other set is used for the bottom field of an interlaced picture. For a progressive picture, both sets must be identical.

The coefficients and settings should be used for the following video source types:

4:2:2 input (progressive or interlaced input)

VPDMA line mode = 1

CHR_US_reg0.cfg_mode = 0x1 (mode B)

CHR_US coefficients are not used in this mode, so values are "don't care"

4:2:0 input (interlaced input):

VPDMA line mode = 0

CHR_US_reg0.cfg_mode = 0x0 (mode A)
CHR_US_reg0.anchor_fid0_c0 = 0x51
CHR_US_reg0.anchor_fid0_c1 = 0x3d5
CHR_US_reg1.anchor_fid0_c2 = 0x3fe3
CHR_US_reg1.anchor_fid0_c3 = 0x3ff7
CHR_US_reg2.interp_fid0_c0 = 0x3fb5
CHR_US_reg2.interp_fid0_c1 = 0x2e9
CHR_US_reg3.interp_fid0_c2 = 0x18f
CHR_US_reg3.interp_fid0_c3 = 0x3fd3
CHR_US_reg4.anchor_fid1_c0 = 0x16b
CHR_US_reg4.anchor_fid1_c1 = 0x247
CHR_US_reg5.anchor_fid1_c2 = 0xb1
CHR_US_reg5.anchor_fid1_c3 = 0x3f9d
CHR_US_reg6.interp_fid1_c0 = 0x3fcf
CHR_US_reg6.interp_fid1_c1 = 0x3db
CHR_US_reg7.interp_fid1_c2 = 0x5d
CHR_US_reg7.interp_fid1_c3 = 0x3ff9

4:2:0 input (progressive input):

VPDMA line mode = 0

CHR_US_reg0.cfg_mode = 0x0 (mode A)
CHR_US_reg0.anchor_fid0_c0 = 0x00C8
CHR_US_reg0.anchor_fid0_c1 = 0x0348
CHR_US_reg1.anchor_fid0_c2 = 0x0018
CHR_US_reg1.anchor_fid0_c3 = 0x3fd8
CHR_US_reg2.interp_fid0_c0 = 0x3fb8
CHR_US_reg2.interp_fid0_c1 = 0x0378
CHR_US_reg3.interp_fid0_c2 = 0x00e8
CHR_US_reg3.interp_fid0_c3 = 0x3fe8
CHR_US_reg4 to CHR_US_reg7 are not used so their values are "don't care".

1.2.2 Color Space Converter (CSC)

The color space converter (CSC) module is used to convert video data from one color space to another with nine programmable integer multipliers.

1.2.2.1 Features

- All parameters are programmable
- Each parameter is configurable in signed 13-bits
- Support for Bypass Mode

1.2.2.2 Functional Description

The conversion between the different color spaces requires addition and multiplication operations on color and intensity components. The mathematical expression of the conversion can be written as:

```
Y   = A0*R + B0*G + C0*B + D0
Cb  = A1*R + B1*G + C1*B + D1
Cr  = A2*R + B2*G + C2*B + D2
```

Using YUV to RGB conversion as an example: YUV represents one color space and RGB represents another color space. The conversion can be written in the matrix format shown in Figure 1-22.

Figure 1-22. Matrix Format

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} A0 & B0 & C0 \\ A1 & B1 & C1 \\ A2 & B2 & C2 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} D0 \\ D1 \\ D2 \end{bmatrix}$$

Since HDTV and SDTV have different conversion requirements, both conversions of RGB-to-YCbCr and YCbCr-to-RGB are described. The details of derivations of these matrixes will be given in the following subsections.

1.2.2.2.1 HDTV Application

1.2.2.2.1.1 HDTV Application with Video Data Range

The two equations presented in this section are for the HDTV application. The chromaticity parameters are defined by ITU-R709 standard.

The input video data for these equations should be within the range that is defined for video application.

In an 8-bit system:

- Rd, Gd, Bd, and Yd will be in the range [16-235]
- Cb and Cr will be the range [16-240]
- D = 1

In a 10-bit system:

- Rd, Gd, Bd, and Yd will be in the range [64-940]
- Cb and Cr will be in the range [64-960]
- D = 4

Conversion from RGB to YCbCr:

Figure 1-23. Conversion from RGB to YCbCr

$$\begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.2126 & 0.7152 & 0.0722 \\ -0.1172 & -0.3942 & 0.5114 \\ 0.5114 & -0.4646 & -0.0468 \end{bmatrix} \begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix} D$$

Conversion from YCbCr to RGB:

Figure 1-24. Conversion from YCbCr to RGB

$$\begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.5396 \\ 1 & -0.1831 & -0.4577 \\ 1 & 1.8142 & 0 \end{bmatrix} \begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -197 \\ 82 \\ -232 \end{bmatrix} D$$

1.2.2.2.1.2 HDTV Application with Graphics Data Range

The two equations presented in this section are for the HDTV application with graphics range data input. The main application is for computer graphics display. The chromaticity parameters are defined by ITU-R709 standard.

The input data ranges for these equations are as follows.

In an 8-bit system:

- Rd, Gd, Bd, Yd, Cb and Cr will be the range [0-255]
- D = 1

In a 10-bit system:

- Rd, Gd, Bd, Yd, Cb and Cr will be in the range [0-1023]
- D = 4

Conversion from RGB to YCbCr:

Figure 1-25. Conversion from RGB to YCbCr

$$\begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.1826 & 0.6142 & 0.0620 \\ -0.1006 & -0.3385 & 0.4392 \\ 0.4392 & -0.3990 & -0.0402 \end{bmatrix} \begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} + \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix} D$$

Conversion from YCbCr to RGB:

Figure 1-26. Conversion from YCbCr to RGB

$$\begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} = \begin{bmatrix} 1.1644 & -0.0003 & 1.7927 \\ 1.1644 & -0.2132 & -0.5329 \\ 1.1642 & 2.1125 & -0.0001 \end{bmatrix} \begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -248 \\ 77 \\ -289 \end{bmatrix} D$$

1.2.2.2.1.3 Quantized Coefficients for Color Space Converter in HDTV

This section quantizes all the coefficients of color space conversion based on a 10-bit system for HDTV application. These coefficients can be input to the registers of programmable color space converter. Refer to register section for the corresponding register setting.

Table 1-13. Quantized Coefficients of HDTV Application with Video Data Range

Conversion from RGB to YCbCr				Conversion from YCbCr to RGB			
Coefficient Names	Real Number Format	Quantized Format	Hex Format	Coefficient Names	Real Number Format	Quantized Format	Hex Format
A0(13-bit)	0.2126	218	0x00DA	A0(13-bit)	1	1024	0x0400
B0(13-bit)	0.7152	732	0x02DC	B0(13-bit)	0	0	0x0000
C0(13-bit)	0.0722	74	0x004A	C0(13-bit)	1.5396	1577	0x0629
A1(13-bit)	-0.1172	-120	0x1F88	A1(13-bit)	1	1024	0x0400
B1(13-bit)	-0.3942	-404	0x1E6C	B1(13-bit)	-0.1831	-187	0x1F45
C1(13-bit)	0.5114	524	0x020C	C1(13-bit)	-0.4577	-469	0x1E2B
A2(13-bit)	0.5114	524	0x020C	A2(13-bit)	1	1024	0x0400
B2(13-bit)	-0.4646	-476	0x1E24	B2(13-bit)	1.8142	1858	0x0742
C2(13-bit)	-0.0468	-48	0x1FD0	C2(13-bit)	0	0	0x0000
D0(12-bit)	0	0	0x000	D0(12-bit)	-197	-788	0xCEC
D1(12-bit)	128	512	0x200	D1(12-bit)	82	328	0x148
D2(12-bit)	128	512	0x200	D2(12-bit)	-232	-928	0xC60

Table 1-14. Quantized Coefficients of HDTV Application with Graphics Data Range

Conversion from RGB to YCbCr				Conversion from YCbCr to RGB			
Coefficient Names	Real Number Format	Quantized Format	Hex Format	Coefficient Names	Real Number Format	Quantized Format	Hex Format
A0(13-bit)	0.1826	187	0x00BB	A0(13-bit)	1.1644	1192	0x04A8
B0(13-bit)	0.6142	629	0x0275	B0(13-bit)	-0.0003	0	0x0000
C0(13-bit)	0.062	63	0x003F	C0(13-bit)	1.7927	1836	0x072C
A1(13-bit)	-0.1006	-103	0x1F99	A1(13-bit)	1.1644	1192	0x04A8
B1(13-bit)	-0.3385	-347	0x1EA5	B1(13-bit)	-0.2132	-218	0x1F26
C1(13-bit)	0.4392	450	0x01C2	C1(13-bit)	-0.5329	-546	0x1DDE
A2(13-bit)	0.4392	450	0x01C2	A2(13-bit)	1.1642	1192	0x04A8
B2(13-bit)	-0.399	-409	0x1E67	B2(13-bit)	2.1125	2163	0x0873
C2(13-bit)	-0.0402	-41	0x1FD7	C2(13-bit)	-0.0001	0	0x0000
D0(12-bit)	16	64	0x040	D0(12-bit)	-248	-992	0xC20
D1(12-bit)	128	512	0x200	D1(12-bit)	77	308	0x134
D2(12-bit)	128	512	0x200	D2(12-bit)	-289	-1156	0xB7C

1.2.2.2.2 SDTV Application

1.2.2.2.2.1 SDTV Application with Video Data Range

The two equations presented in this section are for the SDTV application. The chromaticity parameters are defined by ITU-R601 standard.

The input video data for these equations should be within the range that is defined for video application.

In an 8-bit system:

- Rd, Gd, Bd, and Yd will be in the range [16-235]
- Cb and Cr will be the range [16-240]
- D = 1

In a 10-bit system:

- Rd, Gd, Bd, and Yd will be in the range [64-940]
- Cb and Cr will be in the range [64-960]
- D = 4

Conversion from RGB to YCbCr:

Figure 1-27. Conversion from RGB to YCbCr

$$\begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.172 & -0.339 & 0.511 \\ 0.511 & -0.428 & -0.083 \end{bmatrix} \begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} + \begin{bmatrix} 0 \\ 128 \\ 128 \end{bmatrix} D$$

Conversion from YCbCr to RGB:

Figure 1-28. Conversion from YCbCr to RGB

$$\begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} = \begin{bmatrix} 1 & -0.0003 & 1.3717 \\ 1 & -0.3365 & -0.6984 \\ 1 & 1.7336 & -0.0016 \end{bmatrix} \begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -176 \\ 132 \\ -222 \end{bmatrix} D$$

1.2.2.2.2.2 SDTV Application with Graphics Data Range

The two equations presented in this section are for the SDTV application with graphics range data input. The main application is for computer graphics display. The chromaticity parameters are defined by ITU-R601 standard.

The input data ranges for these equations are as following.

In an 8-bit system:

- Rd, Gd, Bd, Yd, Cb and Cr will be the range [0-255]
- D = 1

In a 10-bit system:

- Rd, Gd, Bd, Yd, Cb and Cr will be in the range [0-1023]
- D = 4

Conversion from RGB to YCbCr:

Figure 1-29. Conversion from RGB to YCbCr

$$\begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 0.257 & 0.504 & 0.098 \\ -0.148 & -0.291 & 0.439 \\ 0.439 & -0.368 & -0.071 \end{bmatrix} \begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} + \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix} D$$

Conversion from YCbCr to RGB:

Figure 1-30. Conversion from YCbCr to RGB

$$\begin{bmatrix} Rd \\ Gd \\ Bd \end{bmatrix} = \begin{bmatrix} 1.1641 & -0.0018 & 1.5958 \\ 1.1641 & -0.3914 & -0.8135 \\ 1.1641 & 2.0178 & -0.0012 \end{bmatrix} \begin{bmatrix} Yd \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -223 \\ 136 \\ -277 \end{bmatrix} D$$

1.2.2.2.2.3 Quantized Coefficients for Color Space Converter in SDTV

This section quantizes all the coefficients of color space conversion based on a 10-bit system for SDTV application. These coefficients can be input to the registers of programmable color space converter. Refer to register section for the corresponding register setting.

Table 1-15. Quantized Coefficients of SDTV Application with Video Data Range

Conversion from RGB to YCbCr				Conversion from YCbCr to RGB			
Coefficient Names	Real Number Format	Quantized Format	Hex Format	Coefficient Names	Real Number Format	Quantized Format	Hex Format
A0(13-bit)	0.299	306	0x0132	A0(13-bit)	1	1024	0x0400
B0(13-bit)	0.587	601	0x0259	B0(13-bit)	-0.0003	0	0x0000
C0(13-bit)	0.114	117	0x0075	C0(13-bit)	1.3717	1405	0x057D
A1(13-bit)	-0.172	-176	0x1F50	A1(13-bit)	1	1024	0x0400
B1(13-bit)	-0.339	-347	0x1EA5	B1(13-bit)	-0.3365	-345	0x1EA7
C1(13-bit)	0.511	523	0x020B	C1(13-bit)	-0.6984	-715	0x1D35
A2(13-bit)	0.511	523	0x020B	A2(13-bit)	1	1024	0x0400
B2(13-bit)	-0.428	-438	0x1E4A	B2(13-bit)	1.7336	1775	0x06EF
C2(13-bit)	-0.083	-85	0x1FAB	C2(13-bit)	-0.0016	-2	0x1FFE
D0(12-bit)	0	0	0x000	D0(12-bit)	-176	-704	0xD40
D1(12-bit)	128	512	0x200	D1(12-bit)	132	528	0x210
D2(12-bit)	128	512	0x200	D2(12-bit)	-222	-888	0xC88

Table 1-16. Quantized Coefficients of SDTV Application with Graphics Data Range

Conversion from RGB to YCbCr				Conversion from YCbCr to RGB			
Coefficient Names	Real Number Format	Quantized Format	Hex Format	Coefficient Names	Real Number Format	Quantized Format	Hex Format
A0(13-bit)	0.257	263	0x0107	A0(13-bit)	1.1641	1192	0x04A8
B0(13-bit)	0.504	516	0x0204	B0(13-bit)	-0.0018	-2	0x1FFE
C0(13-bit)	0.098	100	0x0064	C0(13-bit)	1.5958	1634	0x0662
A1(13-bit)	-0.148	-152	0x1F68	A1(13-bit)	1.1641	1192	0x04A8
B1(13-bit)	-0.291	-298	0x1ED6	B1(13-bit)	-0.3914	-401	0x1E6F
C1(13-bit)	0.439	450	0x01C2	C1(13-bit)	-0.8135	-833	0x1CBF
A2(13-bit)	0.439	450	0x01C2	A2(13-bit)	1.1641	1192	0x04A8
B2(13-bit)	-0.368	-377	0x1E87	B2(13-bit)	2.0178	2066	0x0812
C2(13-bit)	-0.071	-73	0x1FB7	C2(13-bit)	-0.0012	-1	0x1FFF
D0(12-bit)	16	64	0x040	D0(12-bit)	-223	-892	0xC84
D1(12-bit)	128	512	0x200	D1(12-bit)	136	544	0x220
D2(12-bit)	128	512	0x200	D2(12-bit)	-277	-1108	0xBAC

1.2.2.3 Bypass Mode

CSC module can be bypassed by setting the following bit-field to 1:

CSC→CSC05.Bypass

1.2.3 Compositor Module

The Compositor (COMP) module is used to blend the input video and graphics sources into a single stream to drive video encoders.

1.2.3.1 Features Supported

COMP supports the following features:

- Four displays: 3 HDs and 1 SD
- Up to five input layers for each HD display: two videos and three graphics
- Up to four input layers for the SD display: one video and three graphics
- Cascade alpha blending for two input layers first and graphic blending later
- Blended outputs to memory from two of the blenders

1.2.3.2 Functional Description

The COMP module has four independently controlled blenders (compositors): three for HD output and one for SD output. Each HD blender can take up to five input layers (two videos and three graphics) to generate one composite output layer. The SD blender can take up to four input layers (one video and three graphics) to generate one composite output layer. This is shown in Figure 1-31

Each blender is associated with one of the four VENCs to drive the display data as shown.

Blender0 → HDMI/DVO1

Blender1 → DVO2

Blender2 → HDCOMP

Blender3 → SD

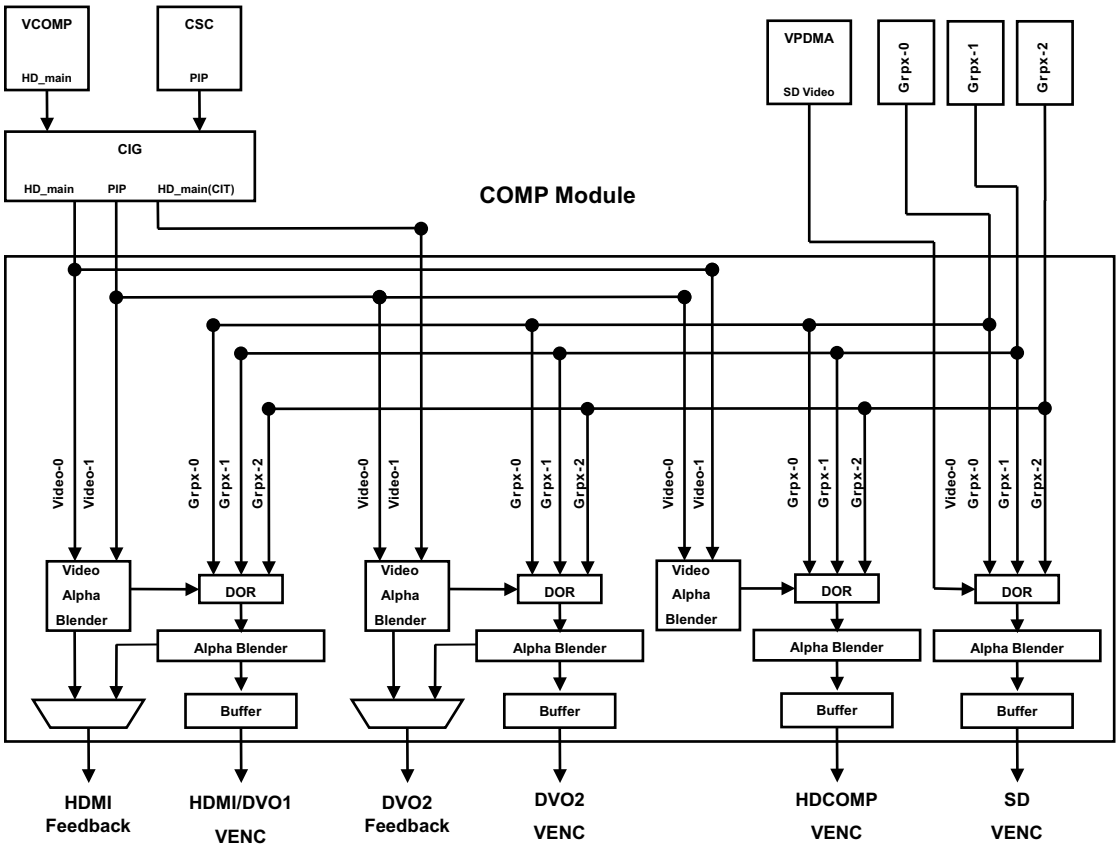
Following are the input layers available:

- HD - Main Video Input
- HD - Main Video Input constrained (CIT)
- HD - PIP Video Input
- SD Video Input
- Graphics0 input (GRPX-0)
- Graphics1 input (GRPX-1)
- Graphics2 input (GRPX-2)

Each of the input layers can be associated to one or more VENCs in HD-VPSS as shown in the above figure. All the input layers associated with a VENC should have the same size and type (progressive or interlaced) of the display. This implies that if an input layer is shared with multiple VENCs, all those VENCs should have the same size, type and frame rate.

For example, if the 1080p HDMI output is desired to have main video input and PIP video input with 1 graphics, then the main and PIP video input must be 1080p, and one of the graphics must be 1080p. If another blender is setup 480i, it cannot use either the main or PIP video inputs, and must use a different graphics input.

Figure 1-31. COMP Module Block Diagram



All graphic sources have both interlaced or progressive formats. Muxes are used for each display to choose the right format. If the graphics module has interlaced input, it can only provide interlaced output through progressive data path. Therefore, the interlaced input data path can not be used in this case.

Input layers associated to a VENC are grouped together, reordered according to the user programmable display priority order list, and blended using embedded alpha values between overlapped layers. Each composed output is then buffered in a memory (inside COMP) from which the associated VENC pulls the data out at its pixel clock rate.

As mentioned above, each blender can take up to five input layers (four for SD) out of the available seven input layers. The accessibility of each blender to the input layer is shown in Table 1-17.

Table 1-17. Input Layers and Associated Blenders

Input layers and Blenders	Blender0	Blender1	Blender2	Blender3
HD main video	YES	NO	YES	NO
HD main video (CIT)	NO	YES	NO	NO
SD video	NO	NO	NO	YES
HD pip video	YES	YES	YES	NO
Grpx-0	YES	YES	YES	YES
Grpx-1	YES	YES	YES	YES
Grpx-2	YES	YES	YES	YES

1.2.3.3 Input Sources

Each blender in COMP module receives up to five input sources (four for SD) to blend and send the composited output to the corresponding VENC. Five input sources to a blender are as follows :

1. Video-0 (HD main video/ HD main video CIT/ SD video)
2. Video-1 (HD pip video; Not available for SD output)
3. Grpx-0
4. Grpx-1
5. Grpx-2

All the inputs that are connected to a single blender should:

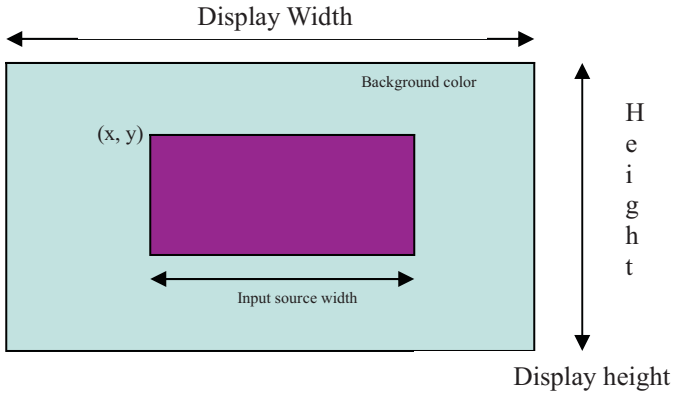
- Have the same size of its corresponding VENC display size. This is done by forming a WINDOW (shown below) in the upstream modules. Please note that it does NOT imply any restriction on the actual input video sizes in external memory to be the same. For example, Video-0 can be 1920x1080 and Video-1 can be 720x480 in the memory.
- Carry their priority levels (if g_reorder =0) to re-order themselves as layers on the final display stream (only for graphic inputs) and
- Carry alpha values used to blend with each other using the above priority levels.

It is necessary to configure upstream modules (to blender) to supply each input of full display size to the blender. If the size of any window is not the same as the display size, background color is inserted in the remaining portion as shown below. The upstream modules include:

1. VCOMP (for HD main video - CIT and non-CIT)
2. CIG (for HD PIP video)
3. VPDMA SD Video (for SD Video)
4. GRPX-0 (for Grpx-0 input)
5. GRPX-1 (for Grpx-1 input)
6. GRPX-2 (for Grpx-2 input)

Display width and display height parameters come from VENC module settings, as shown in Figure 1-32.

Figure 1-32. Display Width and Height Parameters



1.2.3.3.1 HD Main Video Window (CIT or non_CIT)

This window is formed in the VCOMP module with two input sources: main and auxiliary. The composition of the input sources and background color is explained in VCOMP module functional description.

VCOMP→reg6. cfg_dsply_numlines = CIG→CIG_REG1.disp_h = Display_Height of VENC associated with HD main video

VCOMP→reg6. cfg_dsply_numpix_per_line = CIG→CIG_REG1.disp_w = Display_Width of VENC associated with HD main video

Background color for HD main window is selected using following bitfields:

VCOMP→reg9.cfg_dsply_bckgrnd_cr_val

VCOMP→reg9.cfg_dsply_bckgrnd_cb_val

VCOMP→reg9.cfg_dsply_bckgrnd_y_val

The alpha value of HD PIP window is configured using following bit-fields:

CIG→CIG_REG2.bl_enable

CIG→CIG_REG2.bl_level

The layer order of HD video windows (main and pip) is configured in COMP <VENC> settings. The <VENC>_vid_bld_ord bitfield is described in the video alpha blender section.

1.2.3.3.2 HD PIP Video Window

CIG module forms the PIP video window after receiving PIP video source from CSC module

CIG→CIG_REG6.pip_disp_h = Display_Height of VENC associated with PIP video

CIG→CIG_REG6.pip_disp_w = Display_Width of VENC associated with PIP video

Background color for PIP window is transparent and carries an alpha value of zero. It gets the background color set by COMP→back_clr at the time of composition.

The alpha value of HD PIP window is configured using following bit-fields:

CIG→CIG_REG9.bl_enable

CIG→CIG_REG9.bl_level

The priority of HD video windows (both the main and PIP windows) is described in Section 1.2.3.4.1.

1.2.3.3.3 SD Video Window

For the SD video window, the SD video input from the memory needs to be the same as the Display_Width of SD_VENC output display.

For the SD video window:

Input source width = Display_Width

Input source height = Display_Height

x=0

y=0

and hence no background color

The alpha value for SD video is 0xFF.

The priority level used SD video is set in: COMP→SD_setting.vid_order (irrespective of COMP→SD_setting.g_reorder bit-field value).

1.2.3.3.4 Graphics Windows

These windows are formed in the corresponding GPRX modules by configuring below:

GRPX→frame_display_attributes.frame_height = Display_Height of VENC associated with corresponding Grpx

GRPX→frame_display_attributes.frame_width = Display_Width of VENC associated with corresponding Grpx

The origin of a Grpx region input in the window (x,y) is configured as below:

GRPX→region_display_attributes.disp_pos_x = x

GRPX→region_display_attributes.disp_pos_y = y

Background color for Grpx window is transparent and carries an alpha value of zero. It gets the background color set by COMP→back_clr at the time of composition.

The alpha value configuration for blending is explained in GRPX module. Blend type for a region is selected using following bitfield:

GRPX→region_display_attributes.Disp_blend_cfg

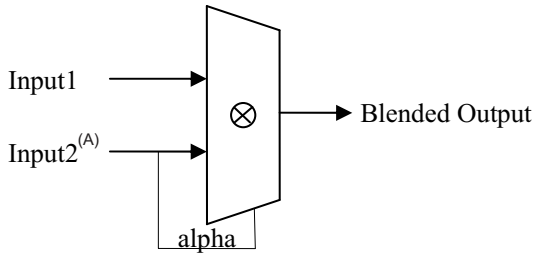
The priority level of a graphics region is set, in corresponding region, using the bitfield mentioned below:

GRPX→region_display_attributes.Disp_prior

1.2.3.4 Blender

A Blender in the COMP module works as mentioned in Figure 1-33:

Figure 1-33. Blender Diagram



A Input2 is tied to 0 for the SD Blender.

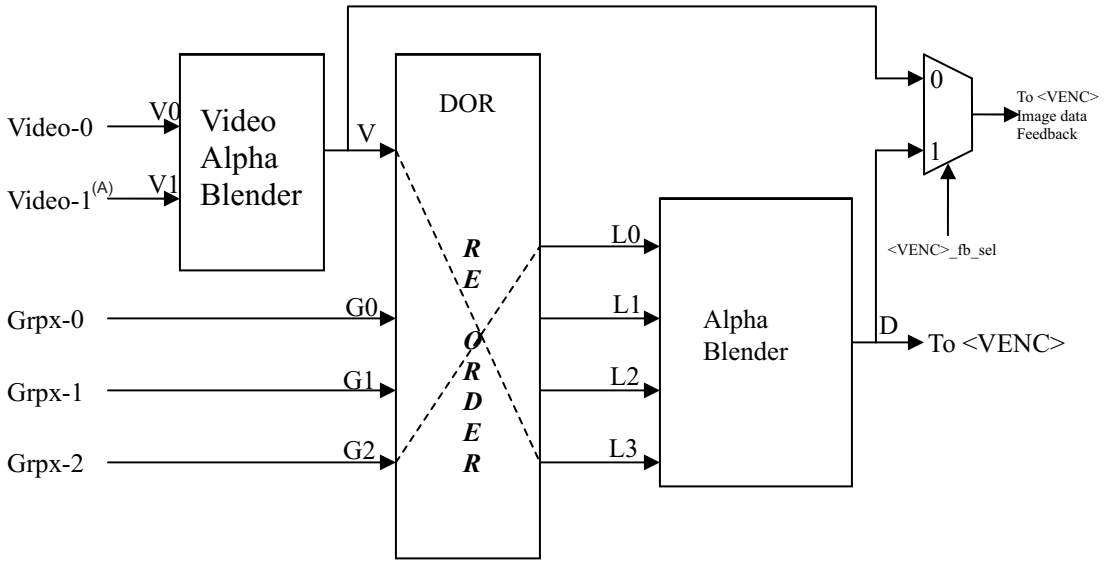
When two input sources, say input1 and input2, are blended, the resulting source is calculated as follows:

Blended Output	=(a)*input1+ (1-a)*input2	if input1 is top layer and input2 is bottom layer
	=(1-b)*input1+ (b)*input2	if input2 is top layer and input1 is bottom layer

Where a and b are alpha values of input1 and input2 windows respectively. The layer order (top or bottom) is decided by priority levels of the two video inputs.

The blending and re-ordering in each blender happens as shown in Figure 1-34

Figure 1-34. Blending and Reordering



A Video-1 is tied to 0 for the SD Blender.

1.2.3.4.1 Video Alpha Blender

Two video inputs, Video-0 and Video-1 (sometimes known as MAIN and PIP windows) are first blended together to generate a single video output as shown in the figure above. The priority level, which determines which video to be on top, is decided by COMP→<VENC> settings. <VENC>_vid.bld_ord bitfield.

The alpha values for both the videos are configured in CIG module as described in the sections above.

The alpha value (blended alpha) of the blended video output is calculated as follows.

Blended alpha	=alpha_bottom video layer	if alpha_top video layer < 0xFF
	=alpha_top video layer	if alpha_top video layer = 0xFF

Blended alpha (calculated above) is used as alpha value for the Video input to the DOR module described below:

The priority of blended video is configured in COMP→<VENC>Settings.vid_order fit field.

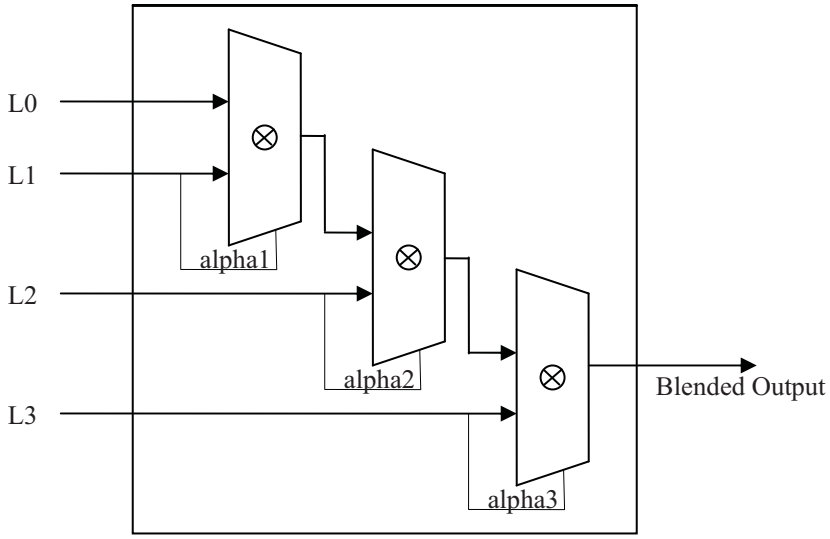
1.2.3.4.2 Display Order Re-shuffling (DOR)

The DOR module is a fully programmable crossbar switch to allow flexible display order change for all input layers. Video layer data is placed in the layer based on its register setting (vid_order bit-field). The graphic data comes with a four-bit priority level configured in the GRPX module. If the global re-order is set (g_reorder=1), the graphics layers are reordered (from top to bottom) based on COMP register settings (g0_order, g1_order, g2_order bit-fields). Otherwise, graphics layers are reordered based on GRPX register (priority) settings as mentioned in the above sections.

1.2.3.4.3 Alpha Blender

The Alpha Blender uses the alpha values of the input layers and blends all of them as per the input order. The block diagram of alpha blender is shown in Figure 1-35.

Figure 1-35. Alpha Blender Block Diagram



In Figure 1-35, L0 is the top layer and L3 is the bottom layer. alpha1, alpha2, alpha3 are the blending levels of layers L1, L2, and L3 respectively.

Note: The total number of pixels per frame/field of any source driving the COMP module should be even.

1.2.3.5 Feedback Output

Blenders 0 and 1 (associated with DVO1 and DVO2) have a feedback output from blended image data. The feedback image data can be selected from video alpha blending or final alpha blending, and sent to external memory. Since feedback path stalls also stall the entire data pipeline, the amount of the stalls in this path can not be such that they will cause an under-flow to the VENC. Hence, the feedback path needs to be given proper high priority in the system for memory access when the corresponding VENC is also functional. Both the paths (feedback path and Venc data path) are optional.

1.2.3.6 Background Color

There is a programmable background color in COMP module. Background color is configured in RGB format with 10-bit in each R, G, and B. Any pixel with an alpha value of 0 will be replaced by this color. If the video bottom layer is disabled, the video top layer will be blended with background color. If both video layers are disabled, the background color is used as output of video alpha blending. For SD channel, only one video stream comes in and it will be blended with the background color.

If the COMP is disabled, or the channel within the COMP driving a particular VENC is disabled, or all inputs to a channel driving particular VENC are disabled, the underflow condition occurs at the VENC. This underflow condition is due to data is not being driven out of the COMP fast enough to keep up with the VENC read rate. Underflow can also happen due to lack of sufficient memory bandwidth or improper VPDMA configuration for any of the input channel. When underflow condition happens, the background color programmed in the COMP module is sent for the underflowed pixels.

1.2.4 Constrained Image Generator (CIG)

The Constrained Image Generator (CIG) module is used to generate a resolution constrained version of the high-quality video to meet the CableCard Copy Protection Specification`s requirement on the handling of Constrained Image Trigger (CIT) information.

1.2.4.1 Features

- Generates both constrained and non-constrained output from a single input video source
  - 1/4x vertical/horizontal resolution reduction using 3-tap vertical/horizontal decimation filters
  - 2x vertical/horizontal resolution restoration using 2-tap average interpolation
  - Video Interlacing to match final scan format
- PIP window framer: Positions a PIP window onto a full display screen.
- Individual Chroma keying and blend value application for all outputs
- Can generate interlaced output on both PIP and main window from a progressive input

1.2.4.2 Functional Description

Copy control information (CCI) is passed from the video service provider across the data channel to inform the Set Top Box of the level of copy protection required. Product shall be able to constrain, when required by the CIT CCI bit, the resolution of content that is High Definition to be output through a connection capable of transmitting content in High Definition Analogue Form, to a Constrained Image. The basic requirement of a constrained image is that it contains the visual equivalent of not more than 520,000 Pixels per frame (e.g. an image with resolution of 540 vertical lines by 960 horizontal lines for a 16:9 aspect ratio). A Constrained Image can be output or displayed using video processing techniques such as line doubling or sharpening to improve the perceived quality of the image.

Although not specifically mentioned in these sources, it is also generally accepted that the degraded video will still need to look better than standard DVDs, which generally are encoded at 720x480.

The CIG module takes in a single non-constrained HD video and generates following two outputs:

- The same non-constrained video which may optionally be interlaced
- The same or constrained version of the source video which may optionally be interlaced

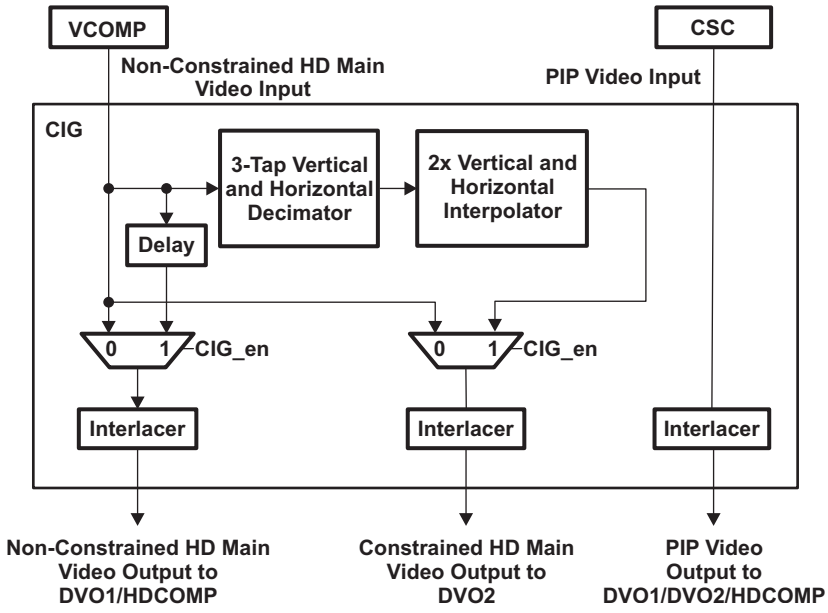
The first output is sent to the DVO1 (HDMI)/ HDCOMP output (via COMP/HD_VENC_A) and the second output is sent to the digital HD output HD_DVO2 (via COMP/HD_VENC_D).

In addition, the CIG module takes in a second video input and positions the video in a full display output screen if the input video is a PIP sized. The PIP video output from CIG module can optionally be interlaced. This path is enabled for following two use cases:

- Displaying un-constrained PIP with constrained/unconstrained main Video (PIP mode)
- Displaying aux video channel output directly on the HD_DVO2 output (Dual-Video Channel mode)

The block diagram of CIG module is shown in Figure 1-36.

Figure 1-36. CIG Block Diagram



1.2.4.2.1 Constrained Video Mode

When the image constraining is required, the CIG requires the incoming unconstrained video to be in progressive scan format in order to apply vertical decimation filter properly. If the output is required to be in interlaced format, the CIG can optionally interlace the outgoing video on both outputs. The PIP video output format (interlaced or progressive) should match the main video output format if it is used as a PIP over the main video.

For the non-constrained video, the output is simply a delayed version (same delay as that of constrained video) of the original video. For the constrained video, ½ decimation filters (3-tap) and 2x interpolation filters (2-tap average) are used to first reduce the overall source resolution by ¼ (½ in vertical ½ in horizontal direction) and to later recover the original display size.

The CIG module performs ½ decimation in both vertical and horizontal directions to achieve the resolution reduction by ¼th (½ in vertical ½ in horizontal direction) on the constrained output and 2x interpolation to restore the total pixel counts. To minimize further filtering of previously optimized image data, a simple 3-taps half-band-filter (¼, ½, ¼) is used for both vertical and horizontal decimation filters while a simple average filter is used for interpolation.

1.2.4.2.2 Interlacer

The CIG module supports interlacing on each output to generate an interlaced output from the progressive input if needed. The interlacing is performed simply by sending only the current field lines and discarding the others. The current field id is passed on from the upstream module (CSC for HD main video and CSC for PIP video).

1.2.4.2.3 Alpha assignment for Chroma Keying (Transparency) and Blending

The CIG module receives RGB data and assigns an alpha value to each pixel data based on programmable transparency and blending configurations. When enabled, the blender block in the COMP module uses the configured 8-bit alpha value for both HD main and PIP video windows. Also, it will force a pixel's alpha value to be 0 if the transparency mode is enabled and pixel's color is same as the user-configured transparency color value. A bit masking feature is provided to ignore bottom 1-3 bits when making comparison for transparency color value. The blending alpha value configured in CIG module is carried onto COMP module.

1.2.4.2.4 PIP Video Path

The CIG module includes PIP windowing logic to support composition of an un-constrained PIP window with the constrained video. (Note that if the VCOMP is used to composite two video sources, the Constrain filter is applied to both main and pip video which may not be desired.)

This path can also be used as a non-PIP datapath logic to simply route a second video source to the COMP module.

The PIP path supports independent PIP_DISP_W and PIP_DISP_H to set the output screen size. PIP_W and PIP_H are used to configure the size of the PIP window. When configured as a “fullsize”, then the incoming video must be same as this output size. i.e PIP_DISP_W = PIP_W and PIP_DISP_H = PIP_H. When configured as a non-fullsize, then PIP_X and PIP_Y will position the incoming video onto the output screen. PIP_X, PIP_Y = (0,0) means the PIP window is positioned at top left corner. Note that PIP_X + PIP_W must be less than or equal to PIP_DISP_W. Similiarly, PIP_Y + PIP_H must be less than or equal to PIP_DISP_H.

As mentioned, output interlacing is also supported on this path just in case the incoming video is in progressive scan mode but it needs to be fed into interlaced output. Note that all W/H/X/Y configurations need to be in FRAME mode.

1.2.4.2.5 CIG Bypass Mode

When the image constraining is not required (CIT bit in the encoded bitstream is not set or the application does not require image constraining), the image constraining should be disabled and the input field or frame data should simply be bypassed to the output as shown in Figure 1-36.

To enable the bypass mode:

CIG->CIG_REG0.cig_en = 0
CIG->CIG_REG1 register needs to be configured with correct HD video image size.

When the image constraining function is bypassed, then the line memories in the CIG module can optionally be turned into a pair of 1920 pixels deep FIFOs by setting CIG_REG0.CIG_BYPASS_FIFO_MODE parameter. When enabled, these FIFOs provide additional tolerance to the DDR bandwidth in the video (main and pip) paths.

To enable the main path FIFO (while cig_en=0):

CIG->CIG_REG0.CIG_BYPASS_FIFO_MODE[8] = 1

To enable the pip path FIFO (while cig_en=0):

CIG->CIG_REG0.CIG_BYPASS_FIFO_MODE[9] = 1
If PIP path is displaying a full size video:
CIG->CIG_REG0.CIG_BYPASS_FIFO_MODE[10] = 0
If PIP path is displaying a none-full size video:
CIG->CIG_REG0.CIG_BYPASS_FIFO_MODE[10] = 1

Note that the chroma keying and alpha assignment for blending feature as well as output interlacing are still available even in the bypass mode.

1.2.5 Graphics Module (GRPX)

The graphics module (GRPX) is a region-based graphics processor that composes one or more graphics regions to create a display plane input for the video compositor (COMP) module. For this device, only one region application is supported.

1.2.5.1 Features

- Input:
  - Supports interlace or progressive input format
  - Supports several input formats like RGB 32/24/16-bit, bitmap data (8/4/2/1-bit) with configurable CLUT
  - Supports optional stenciling (1-bit mask) table for each region
- Output:
  - Output data format is ARGB32
  - Provides both progressive and interlaced outputs through different ports simultaneously when input source is progressive
- Multi-region support. Each region can have:
  - Width, height, placement (X and Y) parameters
  - Display priority
  - Scalar enable/disable
  - Scaling ratio attributes
  - Stenciling enable/disable
  - Support for global color and pixel level blending
  - Configurable chroma keying options
  - Bounding box support to reduce artifacts at region boundaries

1.2.5.2 Functional Description

GRPX module reads a RGB or bitmap image data and applies the frame/region attributes to create a graphics plane for the COMP module. The block diagram of GRPX is shown in Figure 1-37.

Two output ports, progressive and interlaced, are available (as shown in Figure 1-37) at the output of GRPX module to output both progressive and interlaced output data to COMP module when the input source is progressive. If the input source is interlaced format, interlaced output is available on both the ports.

One example of the output frame of GRPX module with three regions is shown in Figure 1-38.

As shown in Figure 1-38, a frame is typically composited by rectangular boxes called as regions. Any two regions should not overlap in vertical direction. There is no limitation on number of regions that can be supported in a frame.

The GRPX module is configured in 128-bit words which are logically divided into three groups:

1. Frame configuration attribute – configures display format/sizes (required during initialization)
2. Region configuration attribute – configures all region specific attributes (required on each frame display regions)
3. Scalar configuration attributes (13 words) – configure scaler specific attributes (only required if scaling is enabled)

Figure 1-37. GRPX Functional Block Diagram

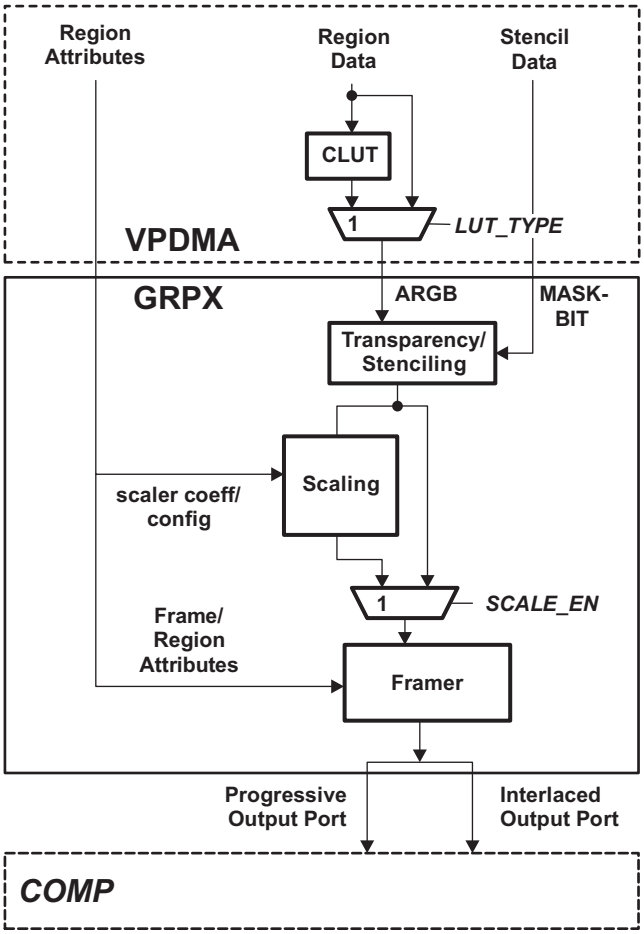
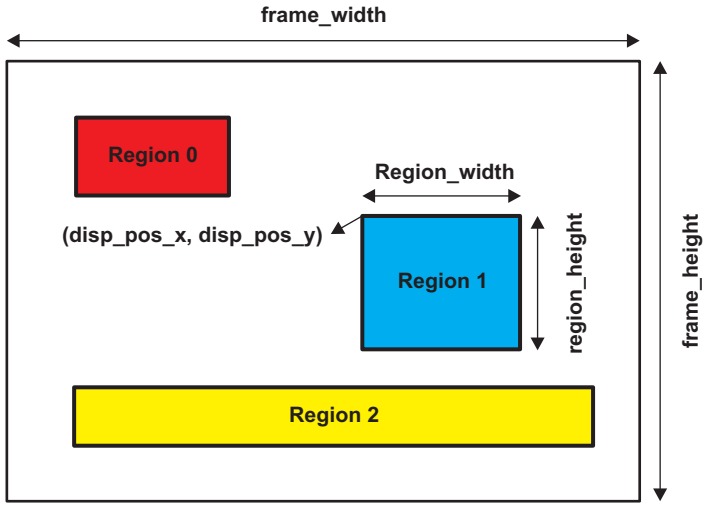


Figure 1-38. GRPX Output



1.2.5.2.1 Frame Configuration Attribute

To enable the graphics output plane, a frame configuration attribute has to be written first (typically during the initialization by using a VPDMA configuration descriptor) to set the frame display size (width, height and input data format).

The size of the frame from GRPX module should match the VENC display output size to which the GRPX output is redirected by COMP module. For example, if GRPX0 output is used in DVO2 display output then GRPX0 frame configuration parameters should be same as DVO2 display output frame size.

Table 1-18. Frame Configuration Attribute (Configuration descriptor payload word 0-3)

Attribute	Bits	Description
Reserved	31-0	Reserved
frame_height	47-32	Frame height (default: 0x0, max 0x7FF) If src_fmt_interlaced is set, frame_height is field_height. (for example, for 480i it should be set to 240). Frame height should be an even number to ensure interlaced outputs are same in height for both fields.
frame_width	63-48	Frame width (default: 0x0, max 0x780)
Reserved	125-64	Reserved
src_fmt_interlaced	126	Format of the source image: 0 = Progressive (default) 1 = Interlaced
Soft reset	127	Software reset of GRPX data pipeline: Writing 1 resets GRPX data pipeline Returns 0 on read always

1.2.5.2.2 Region Configuration Attribute

To display a region, region attribute parameters are set up using the client specific attributes field in the VPDMA data inbound descriptor. Below table shows the details of these parameters.

Table 1-19. Region Configuration Attribute (Inbound data descriptor word 4-7)

Attribute	Bits	Description
Region_height	15-0	Height of the region (number of input region data lines) (max: 0x7FF)
Region_width	31-16	Width of the region (max: 0x780)
disp_pos_y	47-32	Position of region (Y origin) (default: 0x00)
disp_pos_x	63-48	Position of region (X origin) (default: 0x00)
Disp_prior	67-64	Region display priority
Reserved	70-68	Reserved
Disp_first_region	71	1: First region of the frame
Disp_last_region	72	1: First region of the frame
scaler_enable	73	Scaler enable
Reserved	74	Reserved
stenciling_en	75	Stenciling enable for the region
Reserved	78-76	Reserved
bound_box_en	79	0: Bounding box disable 1: Bounding box enable
bb_alpha	87-80	Replace bounding box alpha value when bounding box is enabled. Default value is 0x80.
Disp_blend_cfg	97-88	Blending configuration 95-88: Blending (alpha) value 97-96: Blending Type: 0 = No blending 1 = Region global blending 2 = Color (palette) blending 3 = Pixel (embedded alpha) blending
disp_trans_cfg	127-101	Transparency (color keying enable) configuration bits 103-102: Transparency LSB bit masking 00 = No masking 01 = Mask[0] during pixel data comparison to TRANS_COLOR 10 = Mask[1:0] 11 = Mask[2:0] Example: If TR_LSB_MASK is set to 2'b11, top 5 bits of R/G/B component data are compared to the corresponding 5 bits of TRANS_COLOR R/G/B color. 101: Transparency enable 0 = Disable 1 = Enable transparency for video layer 127-104: Transparency color (RGB24)

1.2.5.2.2.1 Parameter Configuration

Region_height, Region_width, disp_pos_y, disp_pos_x are configured as shown in Figure 1-38.

1.2.5.2.2.1.1 Disp_prior

Each region can be specified to have an inter-graphics-pipeline display priority level which may be used to switch the order between two overlapping regions from two GRPX pipelines. The GRPX simply passes these values along with each pixel data to the COMP module and the COMP uses it to reorder between two GRPX data. This should be used only when both GRPX outputs are tied to the same display output format and rate. The blended output is calculated differently (in the COMP module) for each region based on each its priority level.

1.2.5.2.2.1.2 Disp_first_region

This bit needs to be set to `1` if the region is the first in vertical direction from top of the frame. Region0 in Figure 1-38 is the first region in the frame.

1.2.5.2.2.1.3 Disp_last_region

This bit needs to be set to `1` if the region is the last in vertical direction from top of the frame. Region2 in Figure 1-38 is the last region in the frame.

1.2.5.2.2.1.4 Scaler

The scaler used in GRPX module is consisted of a 5-tap/8-phase horizontal and a 4-tap/8-phase vertical polyphase filters. It supports 0.25x – 4x scaling with a step size of 0.01. Individual regions can have a different set of scaling parameters (coefficients, scale factor, and offset).

The input source format should be progressive if scaling of region is required.

If a region scaling is enabled, the first pixel location (origin) of the region serves as an anchor point for the region display. Since the width and height of the region change after the scaling, application should take care of the correct scaler attributes such that output of the scaler does not go out of the frame display.

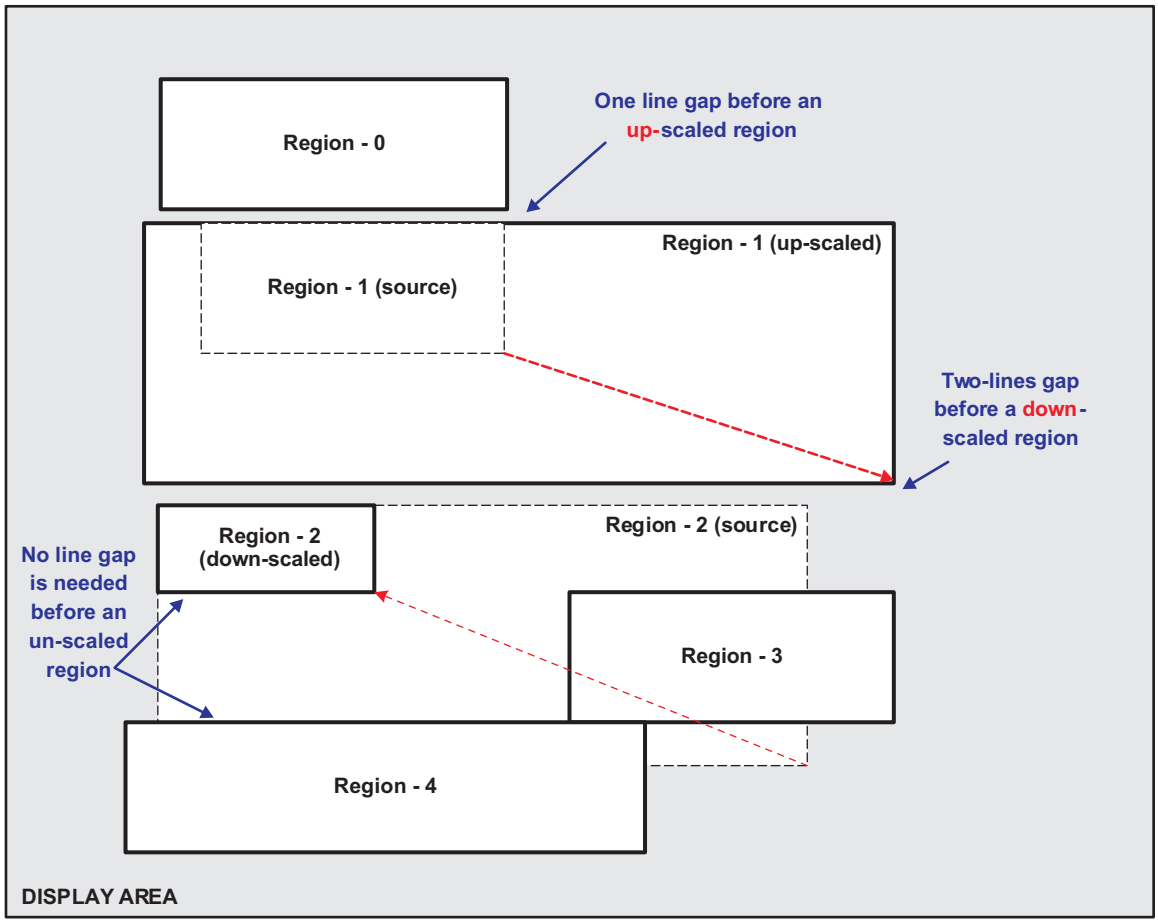
Since the scaler stores one or more input lines before outputting any output lines, the following constraints are imposed when multiple regions are displayed on the screen and scaling is enable:

1. One display line gap is required before a vertically up-scaled region
2. Two display line gap is required before a vertically down-scaled region

These constraints do not apply to the first region on the screen. This is illustrated in Figure 1-39.

The minimum size of vertical region is one line, and no multiple regions on a same line is allowed (nor is possible) per “region” graphics definition.

Figure 1-39. Region Display Position and Gap Requirement Illustration



Scaler configuration attributes (see Section 1.2.5.2.3) are to be filled for a given scaling ratio when scaler is enabled.

1.2.5.2.2.1.4.1 Anti-flicker Filter Implementation

When a region is scaled up or down, the poly-phase vertical filter will inherently provide anti-flicker filtering. Even when a region is not needed to be scaled, the scaler can still be enabled to perform low-pass filtering along the vertical direction with scaling ratio=1. Similarly, when the target display of the GRPX is in an interlaced scan mode, the scaler can be used to perform anti-flicker filtering.

1.2.5.2.2.1.5 Stenciling

The VPDMA sends 1-bit for each pixel (from the region stenciling data buffer) of a region that has “stenciling” feature enabled. This bit is used to force the alpha value of the pixel to ZERO in order to “mask”-off the pixel (i.e., make the pixel transparent). This feature can be used by application to assign an arbitrary mask shape to a rectangular region graphics. Enabling of this feature requires “stenciling_en” bit-field to be set to `1`.

1.2.5.2.2.1.6 Boundary Box Blending

Even with anti-flickering, the flicker around the top and bottom edges of a region may still exists when the anti-flickered region is composed onto the output display in the COMP module. The GRPX supports overwriting alpha values of pixels that make up a 1-pixel wide boundary box of a region with a semi-transparent (alpha) value (default – 0x80) so that the flickering around the edges can be minimized. This feature is enabled when bound_box_en is set to `1`. The alpha value for the boundary box is programmable in the bit-field bb_alpha.

1.2.5.2.3 Blending/Transparency Handling

The GRPX supports four blending modes (no-blending, global, pixel/CLUT, pixel) and a transparency mode for each region to determine how alpha value for each pixel is set. The configuration for blending and transparency are in the region attributes and are shown again in Table 1-20.

Table 1-20. Blending and Transparency Configuration

Attribute	Bits	Description
Disp_blend_cfg	[97:88]	Blending configuration [95:88]: Blending (alpha) value [97:96]: Blending type 0 = No Blending 1 = Region global blending 2 = Color (palette) blending 3 = Pixel (embedded alpha) blending
disp_trans_cfg	[127:101]	Transparency (color keying enable) configuration bits [103:102]: Transparency LSB bit masking 00 = No masking 01 = Mask[0] during pixel data comparison to TRANS_COLOR 10 = Mask[1:0] 11 = Mask[2:0] Example: If TR_LSB_MASK is set to 2'b11, top 5 bits of R/G/B component data are compared to the corresponding 5 bits of TRANS_COLOR R/G/B color. [101]: Transparency enable 0 = Disable 1 = Enable transparency for video layer [127:104]: Transparency color (RGB24)

When no-blending is selected, the GRPX forces each alpha to FFh to make the region total opaque. In region global-blending, a programmed alpha value in bits [95:88] (also called as “global blend” value) is assigned to each pixel similar to the no-blending case.

For color or pixel blending, the VPDMA sets the alpha value with CLUT mapping or with embedded Alpha value (argb format source) respectively. In these two modes, the GRPX simply passes the alpha value from the VPDMA to COMP module. Pixel level blending is performed in the COMP module for both color and pixel blending modes.

When transparency is enabled, each pixel color is compared against the transparency color to determine whether the pixel is to be transparent or not. If the colors match, the alpha value is forced to 00h. Otherwise, the alpha value remains as programmed.

The blending level supported is from 0 (transparent) to 255 (totally opaque).

Because the alpha value is also scaled in the same way the color components (RGB) are scaled, all enabled blending/transparency related tasks are performed in the following order:

1. Application of No-blending (force alpha = FFh) or Global-blending (force alpha=programmed global blend level)
2. Transparency check to force alpha = 0 for transparent pixels
3. Stenciling application to force masked pixels (stencil data = 1) with alpha = 0
4. Scaling of Alpha (if scaling enabled)
5. Box Blending (force alpha = programmed box_blend_level)

1.2.5.2.4 Region Scaler Configuration Attributes

Table 1-21. Region Scaler Configuration Attributes 1

Attribute	Bits	Description
coefh0_p0	[9:0]	Coefficient for Horizontal TAP 0 Phase 0
Reserved	[15:10]	reserved
coefh0_p1	[25:16]	Coefficient for Horizontal TAP 0 Phase 1
Reserved	[31:26]	reserved
coefh0_p2	[41:32]	Coefficient for Horizontal TAP 0 Phase 2
Reserved	[47:42]	reserved
coefh0_p3	[57:48]	Coefficient for Horizontal TAP 0 Phase 3
Reserved	[63:58]	reserved
coefh0_p4	[73:64]	Coefficient for Horizontal TAP 0 Phase 4
Reserved	[79:74]	reserved
coefh0_p5	[89:80]	Coefficient for Horizontal TAP 0 Phase 5
Reserved	[95:90]	reserved
coefh0_p6	[105:96]	Coefficient for Horizontal TAP 0 Phase 6
Reserved	[111:106]	reserved
coefh0_p7	[121:112]	Coefficient for Horizontal TAP 0 Phase 7
Reserved	[127:122]	reserved

Table 1-22. Region Scaler Attributes 2

Attribute	Bits	Description
coefh1_p0	[9:0]	Coefficient for Horizontal TAP 1 Phase 0
Reserved	[15:10]	reserved
coefh1_p1	[25:16]	Coefficient for Horizontal TAP 1 Phase 1
Reserved	[31:26]	reserved
coefh1_p2	[41:32]	Coefficient for Horizontal TAP 1 Phase 2
Reserved	[47:42]	reserved
coefh1_p3	[57:48]	Coefficient for Horizontal TAP 1 Phase 3
Reserved	[63:58]	reserved
coefh1_p4	[73:64]	Coefficient for Horizontal TAP 1 Phase 4
Reserved	[79:74]	reserved
coefh1_p5	[89:80]	Coefficient for Horizontal TAP 1 Phase 5
Reserved	[95:90]	reserved
coefh1_p6	[105:96]	Coefficient for Horizontal TAP 1 Phase 6
Reserved	[111:106]	reserved
coefh1_p7	[121:112]	Coefficient for Horizontal TAP 1 Phase 7
Reserved	[127:122]	reserved

Table 1-23. Region Scaler Attributes 3

Attribute	Bits	Description
coefh2_p0	[9:0]	Coefficient for Horizontal TAP 2 Phase 0
Reserved	[15:10]	reserved
coefh2_p1	[25:16]	Coefficient for Horizontal TAP 2 Phase 1

Table 1-23. Region Scaler Attributes 3 (continued)

Attribute	Bits	Description
Reserved	[31:26]	reserved
coefh2_p2	[41:32]	Coefficient for Horizontal TAP 2 Phase 2
Reserved	[47:42]	reserved
coefh2_p3	[57:48]	Coefficient for Horizontal TAP 2 Phase 3
Reserved	[63:58]	reserved
coefh2_p4	[73:64]	Coefficient for Horizontal TAP 2 Phase 4
Reserved	[79:74]	reserved
coefh2_p5	[89:80]	Coefficient for Horizontal TAP 2 Phase 5
Reserved	[95:90]	reserved
coefh2_p6	[105:96]	Coefficient for Horizontal TAP 2 Phase 6
Reserved	[111:106]	reserved
coefh2_p7	[121:112]	Coefficient for Horizontal TAP 2 Phase 7
Reserved	[127:122]	reserved

Table 1-24. Region Scaler Attributes 4

Attribute	Bits	Description
coefh3_p0	[9:0]	Coefficient for Horizontal TAP 3 Phase 0
Reserved	[15:10]	reserved
coefh3_p1	[25:16]	Coefficient for Horizontal TAP 3 Phase 1
Reserved	[31:26]	reserved
coefh3_p2	[41:32]	Coefficient for Horizontal TAP 3 Phase 2
Reserved	[47:42]	reserved
coefh3_p3	[57:48]	Coefficient for Horizontal TAP 3 Phase 3
Reserved	[63:58]	reserved
coefh3_p4	[73:64]	Coefficient for Horizontal TAP 3 Phase 4
Reserved	[79:74]	reserved
coefh3_p5	[89:80]	Coefficient for Horizontal TAP 3 Phase 5
Reserved	[95:90]	reserved
coefh3_p6	[105:96]	Coefficient for Horizontal TAP 3 Phase 6
Reserved	[111:106]	reserved
coefh3_p7	[121:112]	Coefficient for Horizontal TAP 3 Phase 7
Reserved	[127:122]	reserved

Table 1-25. Region Scaler Attributes 5

Attribute	Bits	Description
coefh4_p0	[9:0]	Coefficient for Horizontal TAP 4 Phase 0
Reserved	[15:10]	Reserved
coefh4_p1	[25:16]	Coefficient for Horizontal TAP 4 Phase 1
Reserved	[31:26]	Reserved
coefh4_p2	[41:32]	Coefficient for Horizontal TAP 4 Phase 2
Reserved	[47:42]	Reserved
coefh4_p3	[57:48]	Coefficient for Horizontal TAP 4 Phase 3
Reserved	[63:58]	Reserved

Table 1-25. Region Scaler Attributes 5 (continued)

Attribute	Bits	Description
coefh4_p4	[73:64]	Coefficient for Horizontal TAP 4 Phase 4
Reserved	[79:74]	Reserved
coefh4_p5	[89:80]	Coefficient for Horizontal TAP 4 Phase 5
Reserved	[95:90]	Reserved
coefh4_p6	[105:96]	Coefficient for Horizontal TAP 4 Phase 6
Reserved	[111:106]	Reserved
coefh4_p7	[121:112]	Coefficient for Horizontal TAP 4 Phase 7
Reserved	[127:122]	reserved

Table 1-26. Region Scaler Attributes 6

Attribute	Bits	Description
countvalhorz	[14:0]	Numerator value for fractional counter countval / 2048 coefv0_p0
Reserved	[15]	Reserved
fineoffsethorz	[30:16]	Count offset for start of line
Reserved	[127:31]	Reserved

Table 1-27. Region Scaler Attributes 7

Attribute	Bits	Description
coefv0_p0	[9:0]	Coefficient for Vertical TAP 0 Phase 0
Reserved	[15:10]	reserved
coefv0_p1	[25:16]	Coefficient for Vertical TAP 0 Phase 1
Reserved	[31:26]	reserved
coefv0_p2	[41:32]	Coefficient for Vertical TAP 0 Phase 2
Reserved	[47:42]	reserved
coefv0_p3	[57:48]	Coefficient for Vertical TAP 0 Phase 3
Reserved	[63:58]	reserved
coefv0_p4	[73:64]	Coefficient for Vertical TAP 0 Phase 4
Reserved	[79:74]	reserved
coefv0_p5	[89:80]	Coefficient for Vertical TAP 0 Phase 5
Reserved	[95:90]	reserved
coefv0_p6	[105:96]	Coefficient for Vertical TAP 0 Phase 6
Reserved	[111:106]	reserved
coefv0_p7	[121:112]	Coefficient for Vertical TAP 0 Phase 7
Reserved	[127:122]	reserved

Table 1-28. Region Scaler Attributes 8

Attribute	Bits	Description
coefv1_p0	[9:0]	Coefficient for Vertical TAP 1 Phase 0
Reserved	[15:10]	reserved
coefv1_p1	[25:16]	Coefficient for Vertical TAP 1 Phase 1

Table 1-28. Region Scaler Attributes 8 (continued)

Attribute	Bits	Description
Reserved	[31:26]	reserved
coefv1_p2	[41:32]	Coefficient for Vertical TAP 1 Phase 2
Reserved	[47:42]	reserved
coefv1_p3	[57:48]	Coefficient for Vertical TAP 1 Phase 3
Reserved	[63:58]	reserved
coefv1_p4	[73:64]	Coefficient for Vertical TAP 1 Phase 4
Reserved	[79:74]	reserved
coefv1_p5	[89:80]	Coefficient for Vertical TAP 1 Phase 5
Reserved	[95:90]	reserved
coefv1_p6	[105:96]	Coefficient for Vertical TAP 1 Phase 6
Reserved	[111:106]	reserved
coefv1_p7	[121:112]	Coefficient for Vertical TAP 1 Phase 7
Reserved	[127:122]	reserved

Table 1-29. Region Scaler Attributes 9

Attribute	Bits	Description
coefv2_p0	[9:0]	Coefficient for Vertical TAP 2 Phase 0
Reserved	[15:10]	reserved
coefv2_p1	[25:16]	Coefficient for Vertical TAP 2 Phase 1
Reserved	[31:26]	reserved
coefv2_p2	[41:32]	Coefficient for Vertical TAP 2 Phase 2
Reserved	[47:42]	reserved
coefv2_p3	[57:48]	Coefficient for Vertical TAP 2 Phase 3
Reserved	[63:58]	reserved
coefv2_p4	[73:64]	Coefficient for Vertical TAP 2 Phase 4
Reserved	[79:74]	reserved
coefv2_p5	[89:80]	Coefficient for Vertical TAP 2 Phase 5
Reserved	[95:90]	reserved
coefv2_p6	[105:96]	Coefficient for Vertical TAP 2 Phase 6
Reserved	[111:106]	reserved
coefv2_p7	[121:112]	Coefficient for Vertical TAP 2 Phase 7
Reserved	[127:122]	reserved

Table 1-30. Region Scaler Attributes 10

Attribute	Bits	Description
coefv3_p0	[9:0]	Coefficient for Vertical TAP 3 Phase 0
Reserved	[15:10]	reserved
coefv3_p1	[25:16]	Coefficient for Vertical TAP 3 Phase 1
Reserved	[31:26]	reserved
coefv3_p2	[41:32]	Coefficient for Vertical TAP 3 Phase 2
Reserved	[47:42]	reserved
coefv3_p3	[57:48]	Coefficient for Vertical TAP 3 Phase 3
Reserved	[63:58]	reserved

Table 1-30. Region Scaler Attributes 10 (continued)

Attribute	Bits	Description
coefv3_p4	[73:64]	Coefficient for Vertical TAP 3 Phase 4
Reserved	[79:74]	reserved
coefv3_p5	[89:80]	Coefficient for Vertical TAP 3 Phase 5
Reserved	[95:90]	reserved
coefv3_p6	[105:96]	Coefficient for Vertical TAP 3 Phase 6
Reserved	[111:106]	reserved
coefv3_p7	[121:112]	Coefficient for Vertical TAP 3 Phase 7
Reserved	[127:122]	reserved

Table 1-31. Region Scaler Attributes 11

Attribute	Bits	Description
countvalvert	[14:0]	Numerator value for fractional counter countval / 248 coefv0_p0
Reserved	[15]	Reserved
fineoffsetvert	[30:16]	Count offset for start of line
Reserved	[127:31]	Reserved

1.2.5.2.5 VPDMA Configuration

VPDMA needs to be setup to configure the GRPX module and input data transfer. The initialization sequence for each frame (assuming frame/region attributes change for every frame) should be as follows:

- Frame Attribute Configuration Descriptor
- Region Scalar Co-efficient/Attribute Configuration Descriptor (if required)
- Region Look-Up table Configuration Descriptor (if required)
- Region Stencil Data Descriptor (if required)
- Region Data Descriptor (different from regular data descriptor and it configures region attributes also)

Some of the previous configuration descriptors can be combined into single configuration descriptor (using class 0 type).

If the configuration in any of the previous configuration descriptors is not changed from region to region or frame to frame, it is not required to set up those configuration descriptors each time in the VPDMA LIST. The configuration of descriptors is explained and illustrated in the *VPDMA* chapter.

1.2.6 Standard-Definition Video Encoder (SD_VENC)

1.2.6.1 Overview

The VENC (video encoder) converts digital component YCbCr/RGB video signals to conform to the various TV standard analog video. CVBS is supported.

1.2.6.1.1 Standards

- SMPTE 170M
  - Composite Analog Video Signal – NTSC for Studio Application
- ITU-R BT.470
  - Conventional television systems
- ITU-R BT.601
  - Studio encoding parameters of digital television for standard 4:3 and wide-screen 16:9 aspect ratios
- ITU-R BT.1119
  - Wide-screen signaling for broadcasting (Signaling for wide-screen and other enhanced television parameters)
- EIAJ CPR-1204
  - Transfer Method of Video ID information using Vertical Blanking Interval (525 line system)
- ETSI EN 300 294
  - Television systems; 625-line television Wide Screen Signaling (WSS)
- EIA/CEA-608-E
  - Line 21 Data Services

1.2.6.1.2 Features

- SDTV Feature
  - Master Clock Input - 27 MHz
  - Support Following TV standard
    - NTSC-M
    - NTSC-J
    - NTSC-4.43
    - PAL-B/D/G/H/K/I
    - PAL-M
    - PAL-N
    - PAL-Nc
    - PAL-60
    - SECAM-B/D/G/H/K/L
  - Composite (CVBS)
  - Macrovision (Rev7.1) Anticopy Protection
  - Non-Interlace
  - CGMS/WSS
  - Line 21 Closed Caption Data Encoding
  - Programmable Sync Amplitude
  - Programmable Color-burst Amplitude
  - Programmable Color Space Converter
  - Programmable Sub-carrier Frequency and SCH phase
  - Programmable Luma Delay

- 24-bit Input Interface (either RGB 4:4:4 or YCbCr 4:4:4)
- One channel 12-bit 2x Over-Sampled DAC Output
- Programmable Sync Output
- Master/Slave Operation
- Internal Color Bar Generation
- Support VBI I/F for the generic VBI data insertion

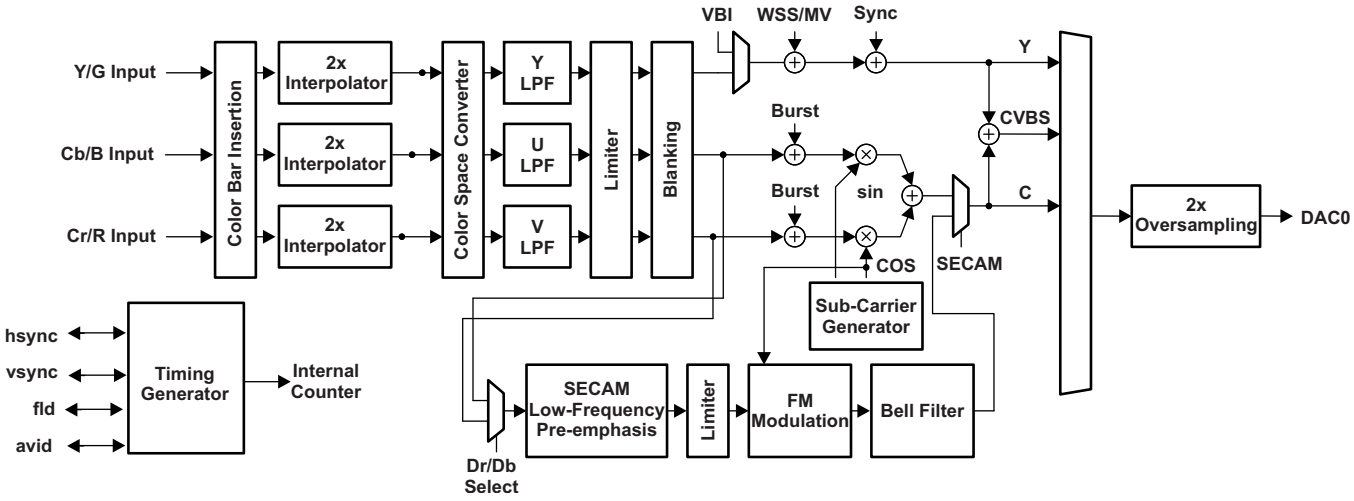
1.2.6.1.3 Features Not Supported

- Square pixel sampling
- Input with embedded sync conforming to ITU-R BT.656
- Analog component video output

1.2.6.2 Functional Description

1.2.6.2.1 Block Diagram

Figure 1-40. VENC Block Diagram



1.2.6.2.2 Operating Modes

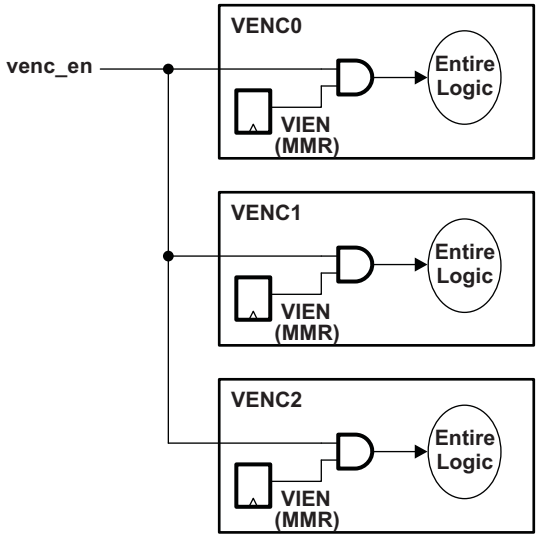
1.2.6.2.2.1 Synchronous Mode

The VENC supports two synchronous modes; master and slave. Each mode can be used in above two video modes.

- Master mode: This mode operates in synchronization with horizontal / vertical sync signals generated in built-in sync signal generator..
- Slave mode: This mode operates in synchronization with sync signals input from outside. Setting the SLV register to 1 enables the slave mode. The external sync inputs are active high by default and their polarity can be independently inverted by registers.

The VENC starts the operation when the external input venc_en is HIGH and the VIEN register is set to 1. The venc_en signal is used for synchronizing multiple video encoders for the multichannel video systems. An external timing manager should take care of the generation of the venc_en signal. When only a single video encoder is used or no synchronization is required among the multiple video encoders, the venc_en can be tied to HIGH. Figure 1-41 provides an example of this synchronization operation.

Figure 1-41. Example of Multiple VENC Synchronization

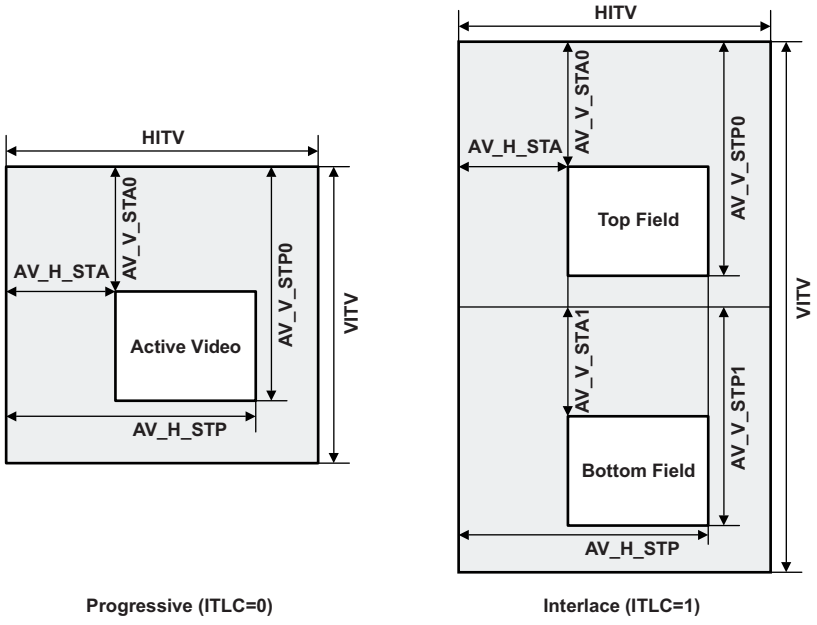


1.2.6.2.3 Timing

1.2.6.2.3.1 Video Timing

The video timing is programmable as shown in Figure 1-42. The HITV and VITV registers set the horizontal and vertical frame sizes. When the target video is interlaced, set ITLC=1. Line per field is VITV/2. Unequal line per field is optionally available. When UEL=1, line per field alternately toggles between (VITV-1)/2 and (VITV+1)/2. The active video position is set by the AV registers.

Figure 1-42. Video Timing



For the analog video output, one of the following TV formats in Table 1-32 also needs to be specified by the FMT register accordingly. The FMT setting specifies the format-dependent timing parameters such as sync rise/fall build-up time, active video rise/fall time, vertical sync and equalizing pulse position, WSS/CC waveform position and so on.

Table 1-32. TV Formats

FMT	Video Format	Type
0	525i	SDTV
1	625i	

For SDTV (525i/625i), composite video (CVBS) and S-video are available. The output combination from two DACs is described in Section 1.2.6.2.14.2.

1.2.6.2.3.2 Input I/F Timing

The input I/F consist of venc_dtv_hs (horizontal sync), venc_dtv_vs (vertical sync), venc_dtv_fid (field ID) and venc_dtv_avid (active video). The timing of each signal is programmable. The timing reference is the internal base counter. The internal base counter starts when VIEN register is set to 1 and the venc_en signal is HIGH. The phase between clk1x and the internal base counter is maintained so that the horizontal counter begins increment at phase1x = 1 as shown in Figure 1-43.

The horizontal timing of each signal is configured in unit of clk2x. The AVID timing should be configured considering the input latency of one cycle of clk1x.

Vertical timing resolution is 1/2H. Independent AVID timings are available for each field for an interlaced format. VS and FID have a unique configuration for both fields

For progressive or non-interlaced formats, the internal base FID is fixed to low. However, it is possible to force toggling venc_dtv_fid at the specified line by setting DTV_FID_F_STA0 register to 1.

Figure 1-43 and Figure 1-44 show the input I/F timing chart with example settings.

Figure 1-43. Input I/F Horizontal Timing

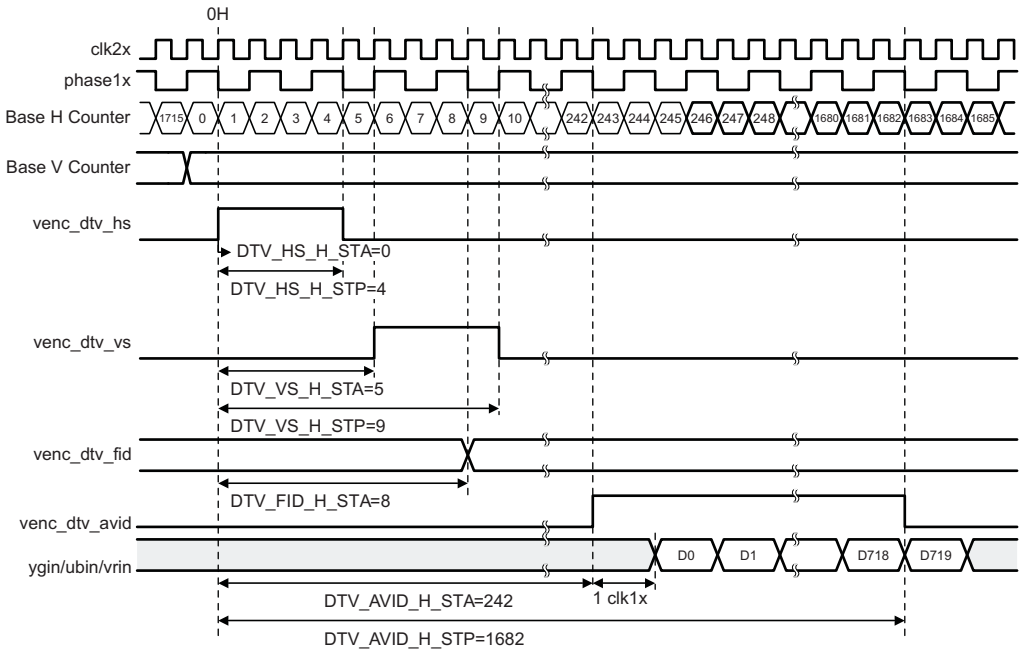
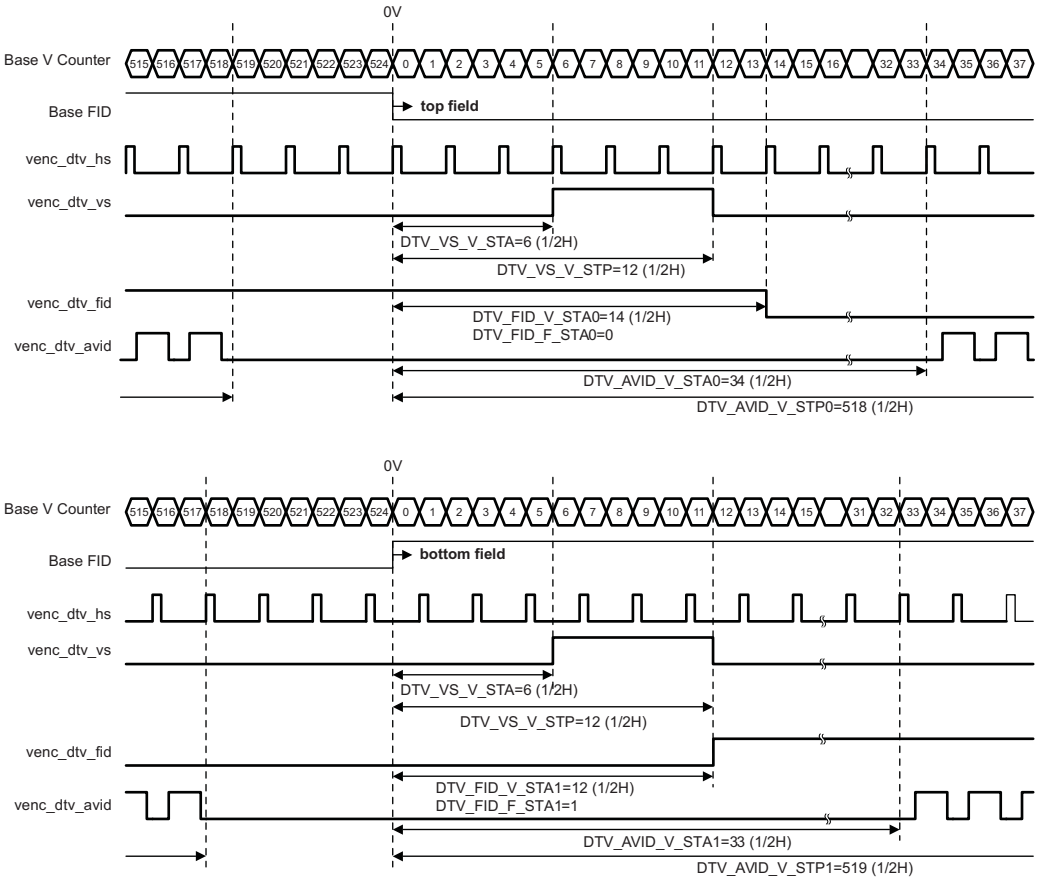


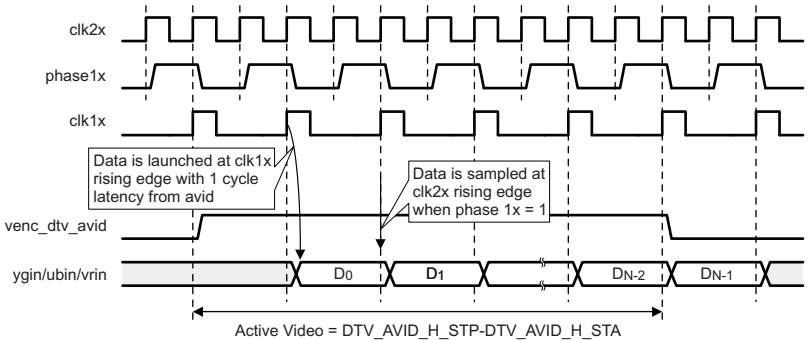
Figure 1-44. Input I/F Vertical Timing



The VENC generates a venc_dtv_avid signal for data request purpose for the upstream module. Input data is expected to arrive at the VENC one clk1x cycle (two clk2x cycles) after an avid assertion. The supported input data format is RGB 4:4:4 or YCbCr 4:4:4. Input data is sampled at clk2x rising edge at phase1x=1. Figure 1-45 shows the timing chart of the input interface.

It is possible to sample the input data with an inversion. When the DIIV register is 1, the input data is inverted before sampling.

Figure 1-45. Input Data Timing



1.2.6.2.3.3 Interrupt Timing

An interrupt pulse is output from the venc_irq port with a single clk2x cycle pulse width every field. Its horizontal and vertical assert position is configured by IRQ_H_STA and IRQ_V_STA registers, respectively.

Figure 1-46. Interrupt Horizontal Timing

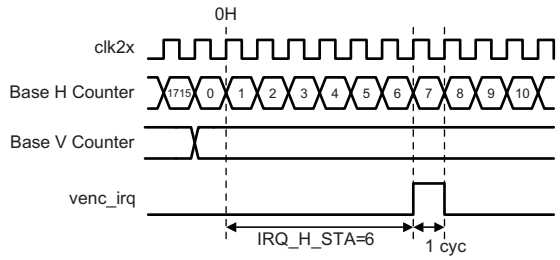
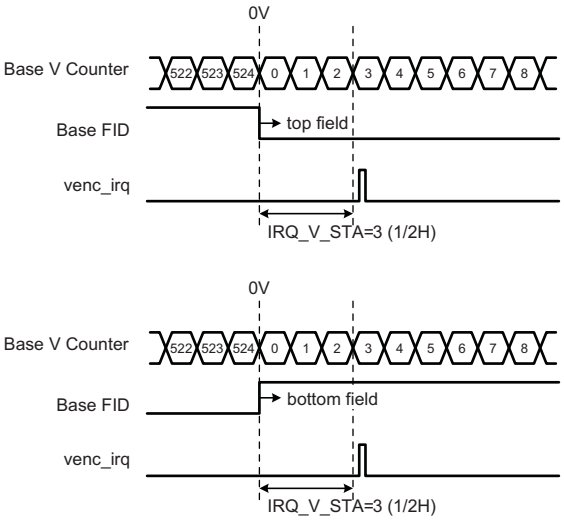


Figure 1-47. Interrupt Vertical Timing



1.2.6.2.3.4 TV Detection Pulse Timing

The VENC supports a TVDET gate pulse generation to connect with the DAC which has the TV detect feature. Its horizontal timing (see Figure 1-48) is configured by TVDETGP_H_STAand TVDETGP_H_STP registers, and vertical timing (see Figure 1-49) is configured by TVDETGP_V_STA and TVDETGP_V_STP registers.

Figure 1-48. TVDETGP Horizontal Timing

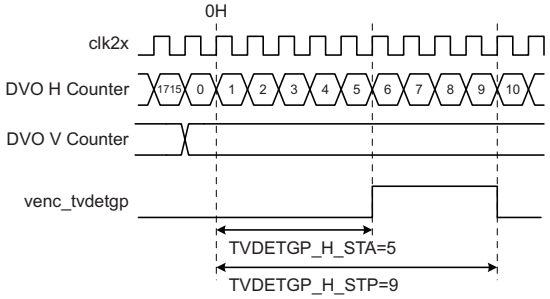
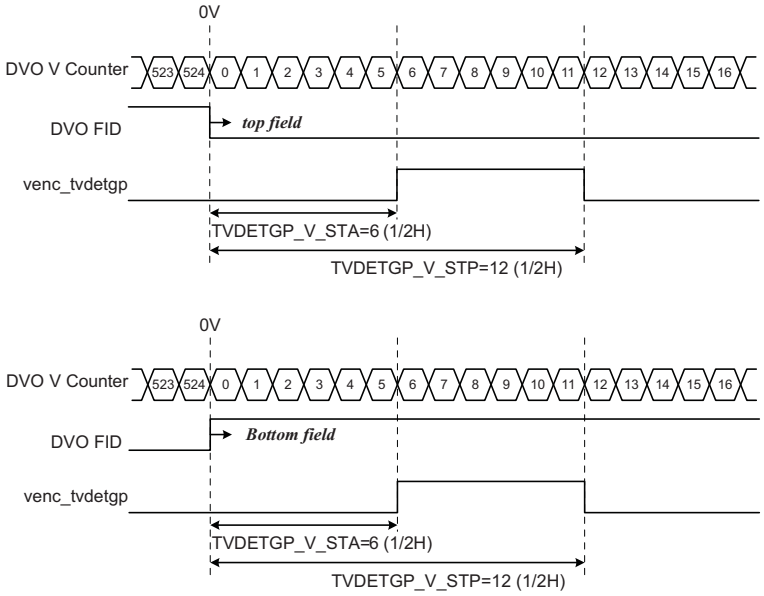


Figure 1-49. TVDETGP Vertical Timing



1.2.6.2.3.5 DAC Video Output Timing

1.2.6.2.3.5.1 SDTV Timing

Figure 1-50 shows horizontal timing characteristics of the SDTV DAC video output. The number of pixels per line is determined by the TV scan format register FMT. The horizontal sync pulse width is also fixed depending on the FMT setting. The color burst start/end positions are specified by BST_H_STA and BST_H_STP registers, and the active video start/end positions are specified by AV_H_STA and AV_H_STP registers. The timing reference of these registers is the internal TV counter.

The AV_H registers specify the window position for the active video. There are similar registers to specify the AVID timing which controls the input video timing. They are independent.

Serration and equalization pulses are inserted on the appropriate lines defined in the standard. Color burst is automatically inserted on the appropriate lines defined in the standard. Figure 1-51 and Figure 1-52 show the vertical timing characteristics of NTSC and PAL. The vertical sync duration is selectable from either 3H or 2.5H by the SVSW register. Typically, 3H VSYNC is used for 525i and 2.5H VSYNC is used for 625i, but this is not always the case. For example, PAL-N has 3H VSYNC even though it is a 625i system.

The color burst is not indicated in these figures but its sequence is managed by hardware. The PAL meander sequence is supported for PAL mode.

Figure 1-50. SDTV Horizontal Timing

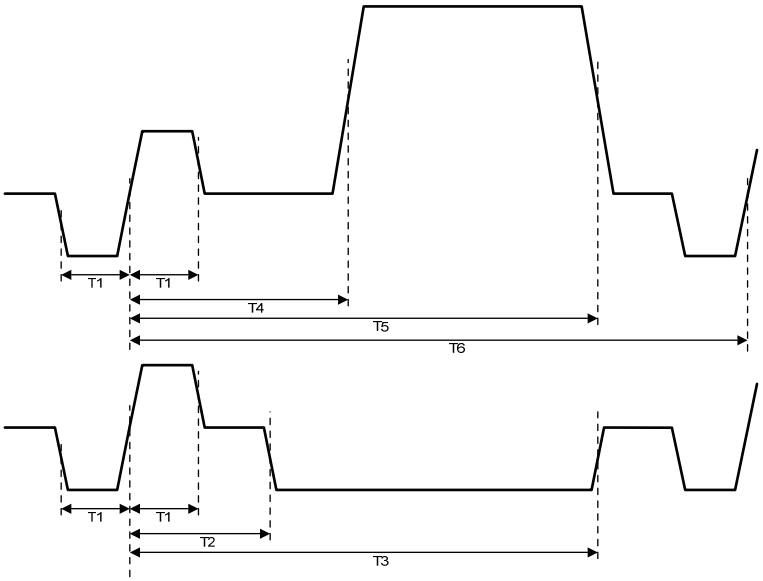


Table 1-33. SDTV Horizontal Timing Parameter

Parameter	Item	525I (FMT = 0)	625I (FMT = 1)	Unit
T1	Horizontal Sync Pulse Width	127		clk2x
T2	H Ref to Burst Start	BST_H_STA		
T3	H Ref to Burst End	BST_H_STP		
T4	H ref to H Blanking End	AV_H_STA		
T5	H ref to H Blanking Start	AV_H_STP		
T6	1H	HITV		
T7	Equalizing Pulse Width	62	63	
T8	Serration Pulse Width	127		
T9	1/2H	HITV/2		

Figure 1-51. 525i Vertical Timing

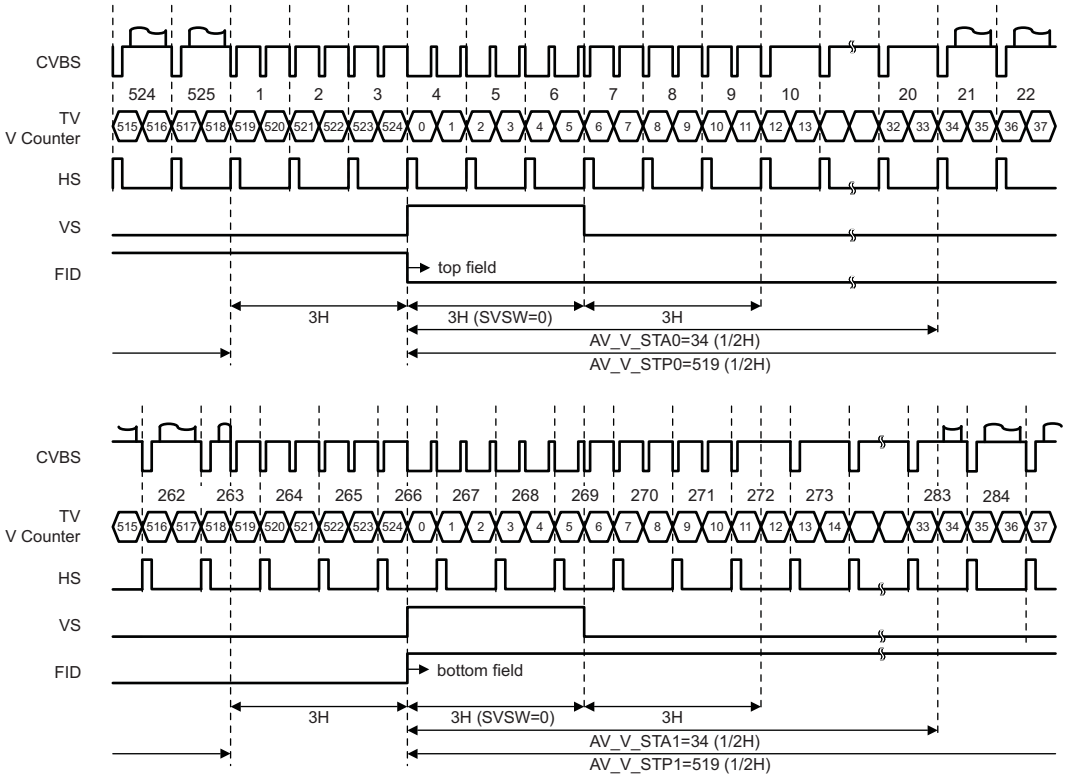


Figure 1-52. 625i Vertical Timing

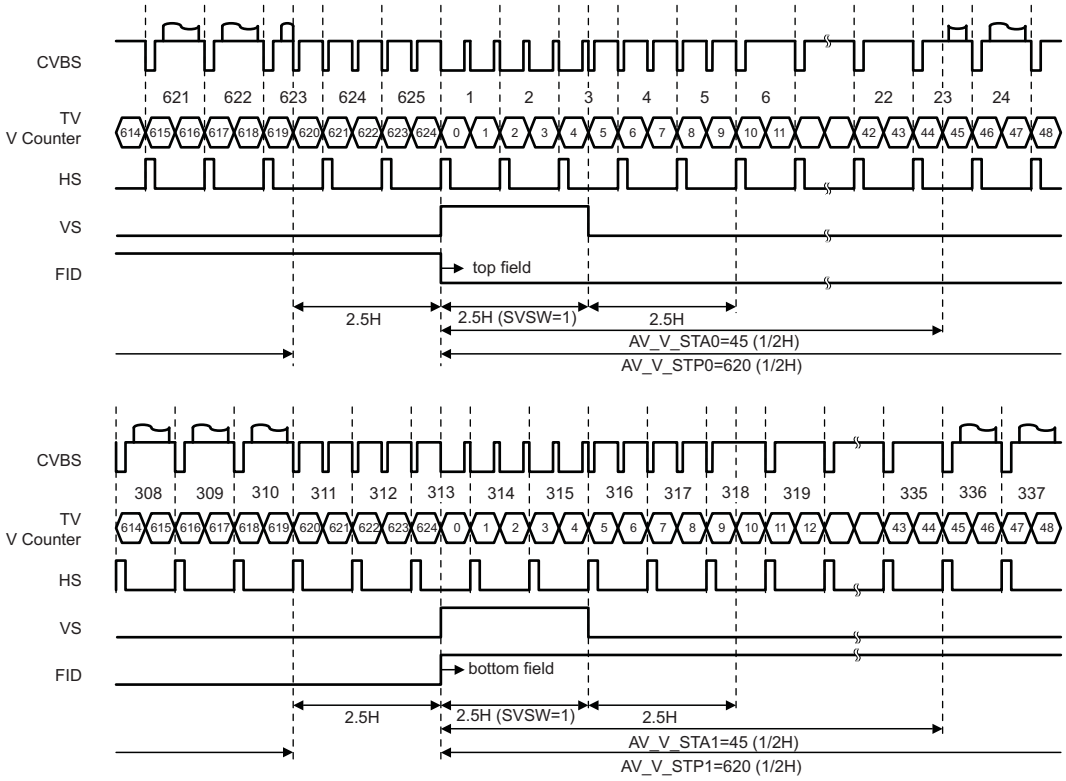


Figure 1-53 and Figure 1-54 show the DAC video output pipeline delay against the internal base counter. The pipeline delay latency is determined by the input pixel rate. The input pixel rate is specified by the PXLR register. The SDTV input pixel rate is typically 13.5 MHz, which is half of clk2x (PXLR = 0). However, some unusual systems may apply the 27 MHz input pixel rate. It is possible to set PXLR = 1.

Figure 1-53. SDTV DAC Video Output Pipeline Delay (PXLR = 0)

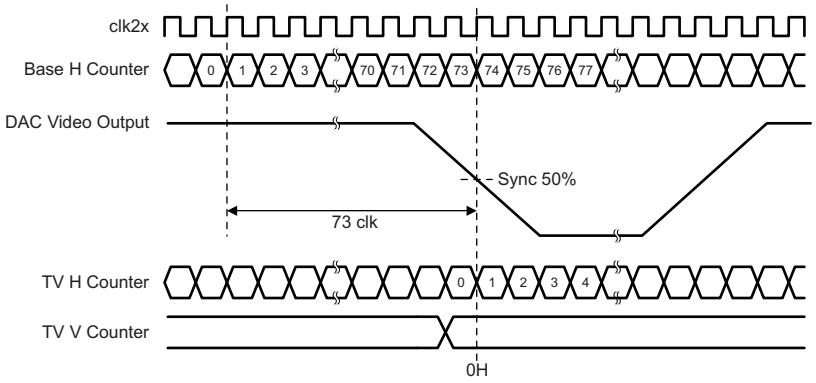


Figure 1-54. SDTV DAC Video Output Pipeline Delay (PXLR = 1)

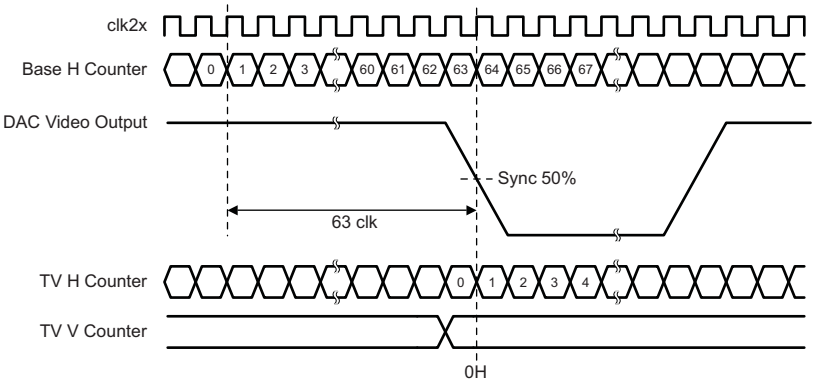


Figure 1-55 and Figure 1-56 show the non-interlaced operation for 262p and 312p. Table 1-34 shows the register setting for the non-interlaced format. Although it is progressive scan, the ITLC register has to be 1 because the internal hardware still relies on the interlaced timing control. Note that the FID is forced to low for non-interlaced mode.

Figure 1-55. 262p (Non-Interlaced NTSC) Vertical Timing

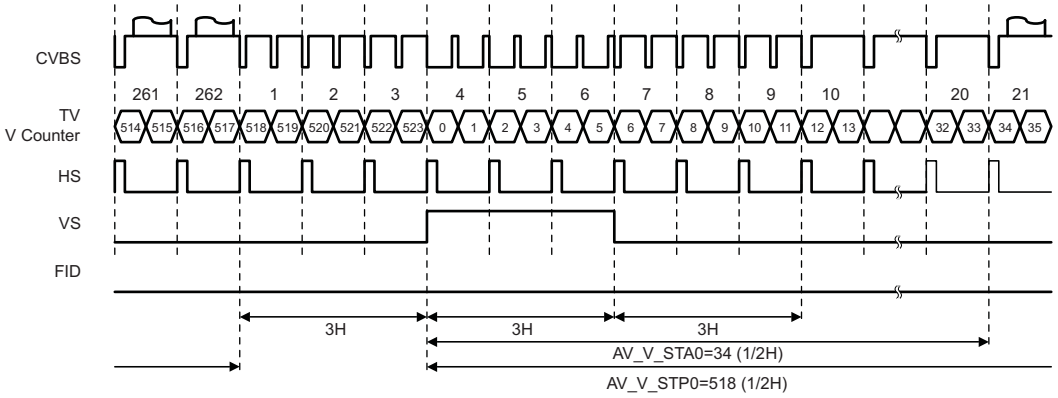


Figure 1-56. 312p (Non-Interlaced PAL) Vertical Timing

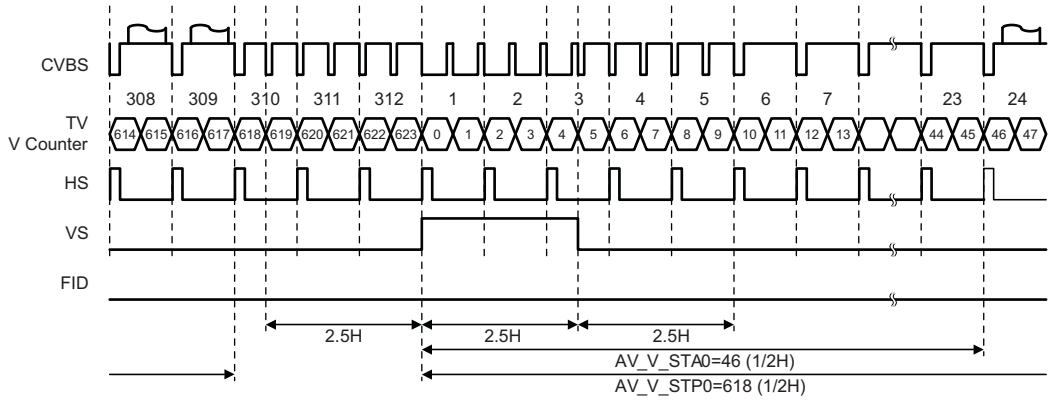


Table 1-34. Non-Interlaced Format

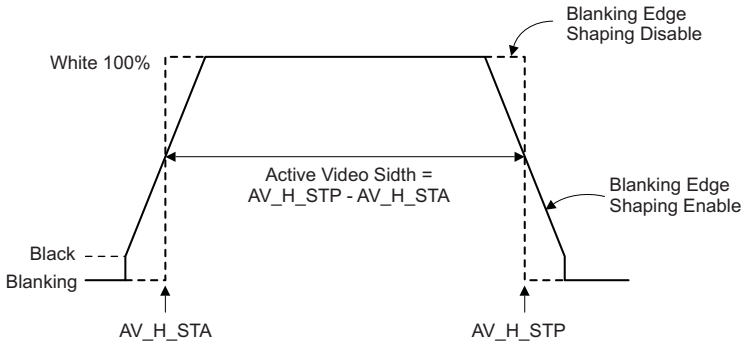
FMT	HITV	VITV	ITLC	UEL	Derived Format
0	1716	525	1	0	525i
		524			262H Non-Interlace
		526			263H Non-Interlace
		525		1	262H, 263H Non-Interlace
1	1728	625	1	0	625i
		624			312H Non-Interlace
		626			313H Non-Interlace
		625		1	312H, 313H Non-Interlace

1.2.6.2.3.6 Horizontal Blanking Edge Shaping

Horizontal video blanking edge is shaped so that the output video has the proper blanking transition.

This feature is enabled by default but can be disabled by setting 1 to the BLS register. Figure 1-57 shows the waveforms when blanking edge shaping is enabled and disabled.

Figure 1-57. Horizontal Blanking Shaping

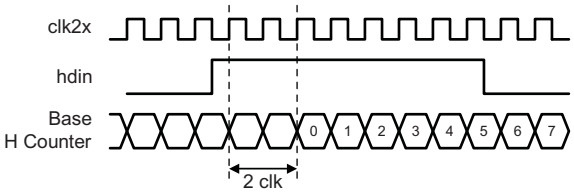


1.2.6.2.3.7 Slave Mode Timings

1.2.6.2.3.7.1 Slave Mode Horizontal Timing

Figure 1-58 shows slave mode horizontal timing. The hdin acts as a horizontal sync input. The internal base horizontal counter is reset after two clk2x cycles upon detecting a rising edge of hdin. The polarity of hdin can be inverted by the HIP register.

Figure 1-58. Slave Mode Horizontal Timing



1.2.6.2.3.7.2 Slave Mode Vertical Timings

Figure 1-59, Figure 1-60, and Figure 1-61 show the slave mode vertical timing. The vdin acts as a vertical sync input. The internal base vertical counter is reset when vdin rise transition is detected at hdin rising edge or 0.5H position for the interlaced mode. If vdin is behind hdin assertion. Vertical reset is suspended until the next hdin rise edge or the next 0.5H for the interlaced mode.

Figure 1-59. Interlaced Slave Vertical Timing (FMD = 0,1)

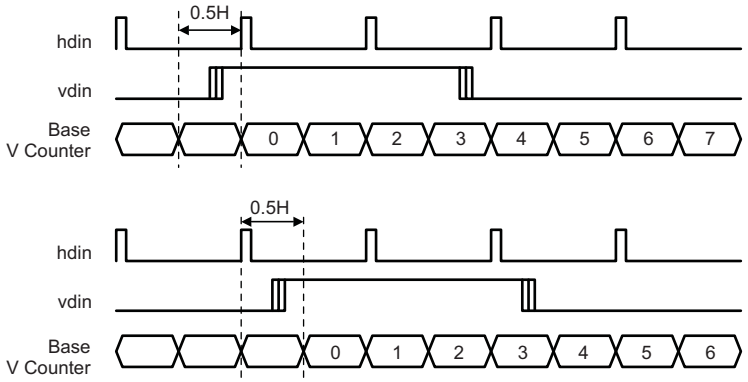


Figure 1-60. Interlaced Slave Vertical Timing (FMD = 2)

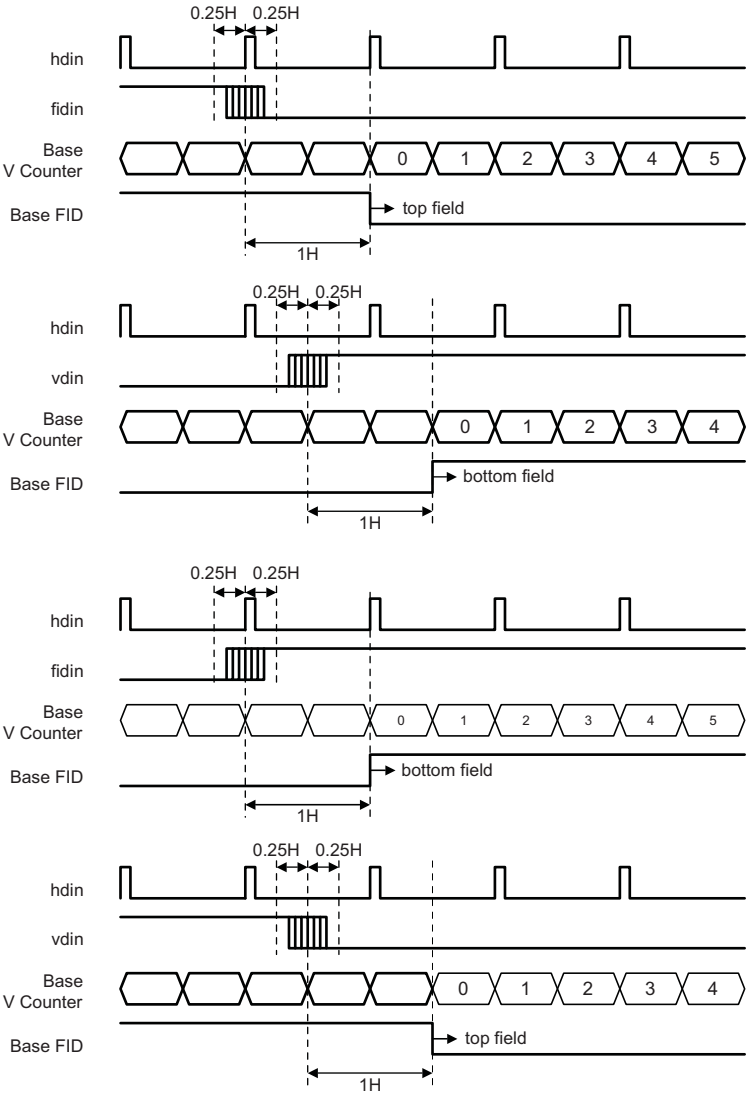
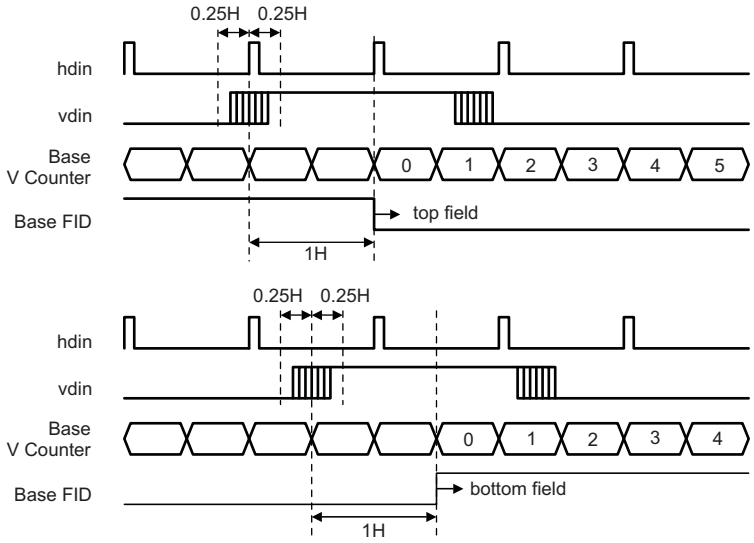


Figure 1-61. Interlaced Slave Vertical Timing (FMD = 3)



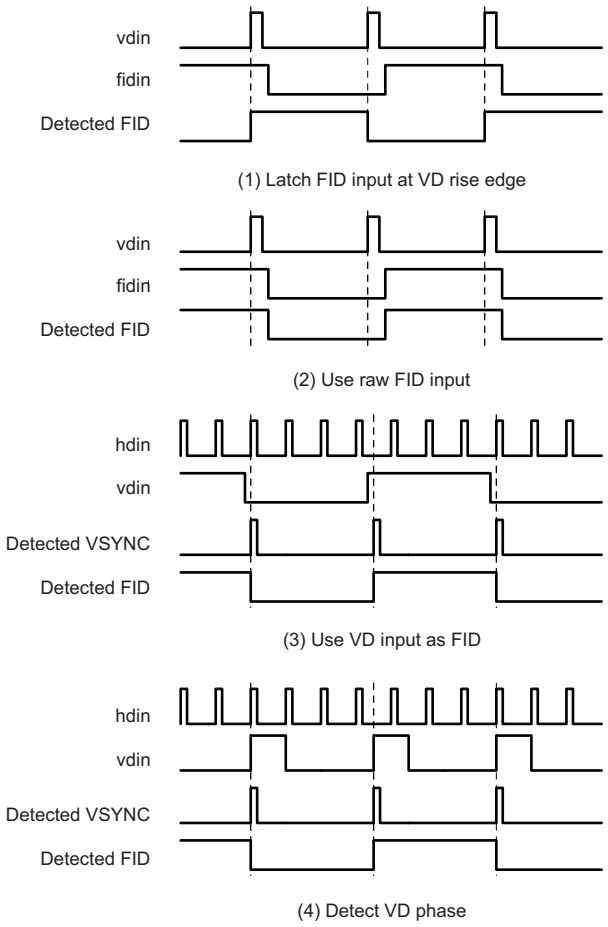
1.2.6.2.3.7.3 Slave Mode Field Detection

For slave interface mode, the field ID is detected by one of the following methods:

1. Latch FID input at VD rise edge
2. Use raw FID input
3. Use VD input as FID
4. Detect VD phase

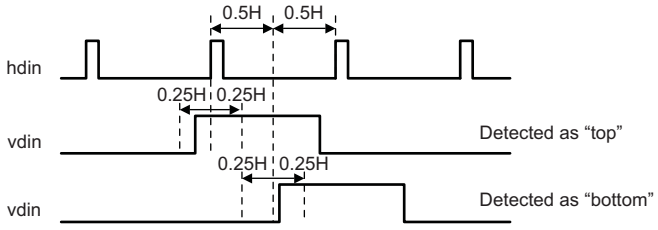
These four modes can be selected by the FMD register. Figure 1-62 shows the timing of each mode.

Figure 1-62. Field Detection Mode



In option4 (Detect VD phase), the timing generator detects VD asserted position in a line. When vdin occurs within 0.25H around hdin, the fid is detected as “top.” Otherwise, the fid is detected as “bottom.” Figure 1-63 shows this detection scheme. When in non-standard mode, field id is always detected as “top” in option4.

Figure 1-63. Field Detection by VD Phase (FMD=3)



1.2.6.2.4 Color Bar Insertion

When the CBAR register is set to 1, the input pixel data is replaced by the predefined color bar data. The data format of the inserted color bar is 8-bit RGB as shown in Table 1-35. Although the color bar data is generated internally, its timing is based on the AVID signal so it is required to configure the DTV_AVID_STA and DTV_AVID_STP registers appropriately.

When color bar mode is used, the color space conversion matrix should be appropriately programmed so that it can convert the full-range RGB to the desired color format.

Table 1-35. Color Bar Table

Color	G	B	R
White	255	255	255
Yellow	255	0	255
Cyan	255	255	0
Green	255	0	0
Magenta	0	255	255
Red	0	0	255
Blue	0	255	0
Black	0	0	0

1.2.6.2.5 2× Interpolation

Three pixel components, YG, UB and VR, are applied to 2x interpolators. The interpolation is intended to interpolate the SD input pixel which is 1x pixel rate (13.5 MHz) to the 2× clock rate (27 MHz). The interpolator consists of 27 tap symmetric FIR with programmable coefficients. The coefficient register format is s(0.7). The transfer function is expressed as:

$$H(z) = \sum_{n=0}^{26} h(n)\, z^{-n}$$

Table 1-36. 2× Interpolation Filter Coefficients

Coefficients	Value	Default
h(0), h(26)	UPFC0	0
h(1), h(25)	0	0
h(2), h(24)	UPFC1	0
h(3), h(23)	0	0
h(4), h(22)	UPFC2	0
h(5), h(21)	0	0
h(6), h(20)	UPFC3	0
h(7), h(19)	0	0
h(8), h(18)	UPFC4	6/128
h(9), h(17)	0	0
h(10), h(16)	UPFC5	-20/128
h(11), h(15)	0	0
h(12), h(14)	UPFC6	78/128
h(13)	1	1

The interpolation is disabled by default and can be enabled by the UPS register.

The interpolator takes 8-bit input (8.0) and generates 12-bit output that has 8-bit integer and 4-bit fractional parts (8.4). After the 2x interpolation, the data processing is done in 12-bit throughout the data pipe. When the interpolation is disabled, the zeros are inserted on 4 LSBs.

1.2.6.2.6 Color Space Converter

The 2x interpolated data then comes into a color space converter (CSC) to be converted into the desired color format. Two independent color space converters are available for CVBS and S-Video paths.

The CSC is implemented based on following equation:

$$\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \end{bmatrix} = \frac{1}{64} \begin{bmatrix} A_1 & B_1 & C_1 \\ A_2 & B_2 & C_2 \\ A_3 & B_3 & C_3 \end{bmatrix} \begin{bmatrix} X_1 + D_1 \\ X_2 + D_2 \\ X_3 + D_3 \end{bmatrix} + \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}$$

The input is X (8.4) and the output is Y s(12.0). The 3x3 matrix coefficients A, B and C are 13 bit s(6.6). The input offset D is 13 bit s(8.4) and the output offset E is 13 bit s(12.0). The parameters in the equation, A, B, C, D and E, are programmable.

Since the CSC output directly contributes the output video amplitude, the coefficients should be determined considering the final video amplitude. In other words, the CSC can also perform amplification for the video output. The output gain should be included in the matrix coefficients. The input offset D should be applied when input data has an offset like BT601. The output offset E should be used to put pedestal level which is needed for NTSC-M.

Following the above CSC conversion, a limiter is available to constrain the output data to the upper and lower bounds.

The programming example of the CSC will be described later in the sections for each targeted system.

1.2.6.2.7 CVBS Encoding

1.2.6.2.7.1 Color Systems

Targeted color modulation system of SDTV is specified by the CCM register. Table 1-37 shows the supported color systems. Quadrature AM modulation is used for NTSC or PAL systems while FM modulation is used for SECAM. Independent programmability of the timing and color systems enables to generate variant TV formats such as PAL-M, PAL-60 and so on.

Table 1-37. Color Systems

CCM	Color System
0	NTSC
1	PAL
2	SECAM
3	Reserved

1.2.6.2.7.2 NTSC/PAL Encoding

1.2.6.2.7.2.1 YUV Generation

First, YUV data should be generated by an appropriate color space conversion. The input color format could be YCbCr or RGB. The CSC can convert either format to YUV.

The fundamental YUV formula is defined in the standard as follows:

$$E'_Y = 0.587E'_G + 0.114E'_B + 0.299E'_R$$
$$E'_U = K_b\left(E'_B - E'_Y\right)$$
$$E'_V = K_r\left(E'_R - E'_Y\right)$$

where K_b and K_r are kell factors which have the following values:

$$K_b = \frac{1}{3}\sqrt{\frac{209556997}{96146491}} = 0.492111$$
$$K_r = \sqrt{\frac{221990474}{288439473}} = 0.877283$$

$E_B{}' - E_Y{}'$ and $E_R{}' - E_Y{}'$ are derived using the following equation:

$$\begin{bmatrix} E'_Y \\ E'_B - E'_Y \\ E'_R - E'_Y \end{bmatrix} = \begin{bmatrix} 0.587 & 0.114 & 0.299 \\ -0.587 & 0.886 & -0.299 \\ -0.587 & -0.114 & 0.701 \end{bmatrix} \begin{bmatrix} E'_G \\ E'_B \\ E'_R \end{bmatrix} \equiv \mathbf{M_0} \begin{bmatrix} E'_G \\ E'_B \\ E'_R \end{bmatrix}$$

Using M_0, the fundamental YUV formula can be rewritten as follows.

$$\begin{bmatrix} E'_Y \\ E'_U \\ E'_V \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & K_b & 0 \\ 0 & 0 & K_r \end{bmatrix} \bullet \mathbf{M_0} \bullet \begin{bmatrix} E'_G \\ E'_B \\ E'_R \end{bmatrix} \equiv \mathbf{M} \begin{bmatrix} E'_G \\ E'_B \\ E'_R \end{bmatrix}$$

The following are examples of CSC programming for various input and output combinations.

Example 1-1. Full-range RGB [0…255] to YUV 10:4 Picture Sync Ratio with 7.5% Setup

In this example, it is assumed that DAC is configured to have maximum amplitude of 1400 mV.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = A \bullet \mathbf{M} \bullet \frac{1}{255} \begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} S_Y \\ 0 \\ 0 \end{bmatrix}$$

$$= \frac{1}{64} \begin{bmatrix} 285 & 55 & 145 \\ -140 & 211 & -71 \\ -250 & -48 & 298 \end{bmatrix} \begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} 157 \\ 0 \\ 0 \end{bmatrix}$$

$$A = \frac{10}{14} \times 1000(mV) \times 92.5\% \times \frac{4095(LSB)}{1400(mV)} = 1932.6$$

$$S_Y = \frac{10}{14} \times 1000(mV) \times 7.5\% \times \frac{4095(LSB)}{1400(mV)} = 157$$

$$Sync = \frac{4}{14} \times 1000(mV) \times \frac{4095(LSB)}{1400(mV)} = 836$$

This coefficient set is preset by default for the CVBS CSC registers.

Example 1-2. Full-range RGB to YUV 10:4 Picture Sync Ratio with Zero Setup

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = A \bullet \mathbf{M} \bullet \frac{1}{255} \begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} S_Y \\ 0 \\ 0 \end{bmatrix}$$

$$= \frac{1}{64} \begin{bmatrix} 308 & 60 & 157 \\ -152 & 229 & -77 \\ -270 & -52 & 322 \end{bmatrix} \begin{bmatrix} G \\ B \\ R \end{bmatrix}$$

$$A = \frac{10}{14} \times 1000(mV) \times \frac{4095(LSB)}{1400(mV)} = 2089$$

$$S_Y = 0$$

Example 1-3. Studio RGB [0…219] to YUV 10:4 Picture Sync Ratio with 7.5% Setup

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = A \bullet \mathbf{M} \bullet \frac{1}{219}\begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} S_Y \\ 0 \\ 0 \end{bmatrix}$$

$$= \frac{1}{64}\begin{bmatrix} 332 & 64 & 169 \\ -163 & 246 & -83 \\ -291 & -56 & 347 \end{bmatrix}\begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} 157 \\ 0 \\ 0 \end{bmatrix}$$

$$A = \frac{10}{14} \times 1000(mV) \times 92.5\% \times \frac{4095(LSB)}{1400(mV)} = 1932.6$$

$$S_Y = \frac{10}{14} \times 1000(mV) \times 7.5\% \times \frac{4095(LSB)}{1400(mV)} = 157$$

Example 1-4. Studio RGB [0…219] to YUV 10:4 Picture Sync Ratio with Zero Setup

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = A \bullet \mathbf{M} \bullet \frac{1}{219}\begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} S_Y \\ 0 \\ 0 \end{bmatrix}$$

$$= \frac{1}{64}\begin{bmatrix} 358 & 70 & 183 \\ -176 & 266 & -90 \\ -314 & -61 & 375 \end{bmatrix}\begin{bmatrix} G \\ B \\ R \end{bmatrix}$$

$$A = \frac{10}{14} \times 1000(mV) \times \frac{4095(LSB)}{1400(mV)} = 2089$$

$$S_Y = 0$$

Example 1-5. Full-range RGB [0…255] to YUV 7:3 Picture Sync Ratio with Zero Setup

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = A \bullet \mathbf{M} \bullet \frac{1}{255}\begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} S_Y \\ 0 \\ 0 \end{bmatrix}$$

$$= \frac{1}{64}\begin{bmatrix} 351 & 68 & 179 \\ -173 & 261 & -88 \\ -308 & -60 & 368 \end{bmatrix}\begin{bmatrix} G \\ B \\ R \end{bmatrix}$$

$$A = \frac{7}{10} \times 1000(mV) \times \frac{4095(LSB)}{1400(mV)} = 2047.5$$

$$S_Y = 0$$

$$Sync = \frac{3}{10} \times 1000(mV) \times \frac{4095(LSB)}{1400(mV)} = 878$$

Example 1-6. ITU-R BT.601 YCbCr to YUV 10:4 Picture Sync Ratio with 7.5% Setup

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = A\begin{bmatrix} 1 & 0 & 0 \\ 0 & K_b & 0 \\ 0 & 0 & K_r \end{bmatrix}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0.886 & 0 \\ 0 & 0 & 0.701 \end{bmatrix}\begin{bmatrix} 1/219 & 0 & 0 \\ 0 & 1/112 & 0 \\ 0 & 0 & 1/112 \end{bmatrix}\begin{bmatrix} Y-16 \\ C_b-128 \\ C_r-128 \end{bmatrix} + \begin{bmatrix} S_Y \\ 0 \\ 0 \end{bmatrix}$$

$$= \frac{1}{64}\begin{bmatrix} 565 & 0 & 0 \\ 0 & 482 & 0 \\ 0 & 0 & 679 \end{bmatrix}\begin{bmatrix} Y-16 \\ C_b-128 \\ C_r-128 \end{bmatrix} + \begin{bmatrix} 157 \\ 0 \\ 0 \end{bmatrix}$$

$$A = \frac{10}{14} \times 1000(mV) \times 92.5\% \times \frac{4095(LSB)}{1400(mV)} = 1932.6$$

$$S_Y = \frac{10}{14} \times 1000(mV) \times 7.5\% \times \frac{4095(LSB)}{1400(mV)} = 157$$

Example 1-7. Full-range RGB to YUV 10:4 Picture Sync Ratio with Zero Setup (DAC Full-swing)

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = A \bullet \mathbf{M} \bullet \frac{1}{255} \begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} S_Y \\ 0 \\ 0 \end{bmatrix}$$

$$= \frac{1}{64} \begin{bmatrix} 326 & 63 & 166 \\ -160 & 242 & -82 \\ -286 & -56 & 342 \end{bmatrix} \begin{bmatrix} G \\ B \\ R \end{bmatrix} + \begin{bmatrix} 180 \\ 0 \\ 0 \end{bmatrix}$$

Maximum excursion occurs at yellow of the 100% color bar whose amplitude is calculated as follows:

$$\begin{bmatrix} E'_{yellow} \\ E'_{yellow} \\ E'_{yellow} \end{bmatrix} = \mathbf{M} \begin{bmatrix} E'_G = 100 \\ E'_B = 0 \\ E'_R = 100 \end{bmatrix}$$

$$= \begin{bmatrix} 88.6 \\ -88.6Kb \\ 11.4Kr \end{bmatrix}$$

$$MaxAmp_{yellow} = 0.925\left(Y_{yellow} + \sqrt{U_{yellow}{}^2 + V_{yellow}{}^2}\right) + 7.5$$

$$= 130.83(IRE)$$

$$A = \frac{100(IRE)}{40(IRE) + 131(IRE)} \times 0.925 \times 4095(LSB) = 2215$$

$$S_Y = \frac{100(IRE)}{40(IRE) + 131(IRE)} \times 0.075 \times 4095(LSB) = 180$$

$$Sync = \frac{40(IRE)}{40(IRE) + 131(IRE)} \times 4095(LSB) = 958$$

1.2.6.2.7.2.2 LPF

The YUV data from color space converter is applied to the LPF. The LPF is used to bandlimit the signal to conform to the standard. The LPF comprises of 11 tap symmetric FIR with the programmable coefficients. Independent coefficients are available for luma and chroma. The luma LPF takes the input from CSC in s(12.0) and outputs s(12.0). The chroma LPF takes s(11.0) from the CSC (MSB thrown away) and output s(11.0). The coefficient register format is s(0.7). The sampling rate of the FIR filter is half of clk2x clock. The LPFs are disabled by default and can be activated by YLPF and CLPF registers. LPF is available only for the CVBS generation.

Table 1-38. Luma LPF Filter Coefficient

Coefficients		Value	Default
h(0)	h(10)	YLPFC0	0
h(1)	h(9)	YLPFC1	0
h(2)	h(8)	YLPFC2	0
h(3)	h(7)	YLPFC3	0
h(4)	h(6)	YLPFC4	32/128
h(5)		YLPFC5	64/128

Table 1-39. Chroma LPF Filter Coefficient

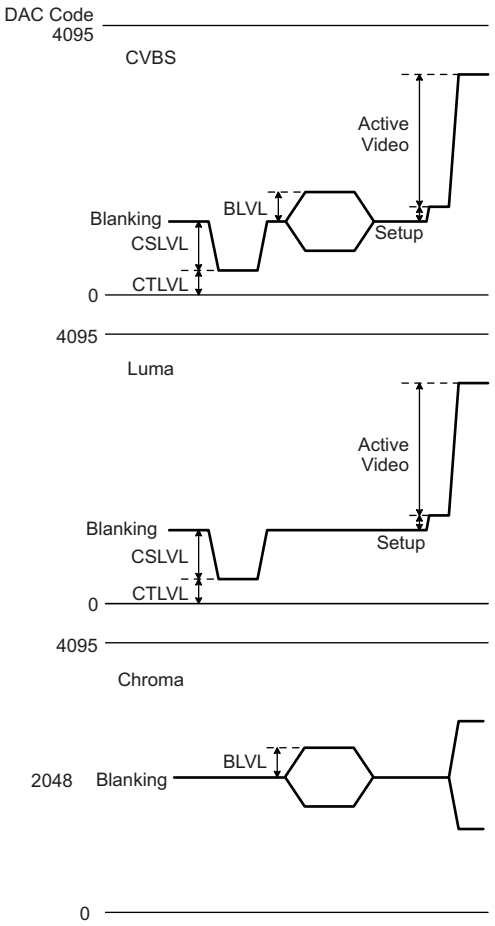
Coefficients		Value	Default
h(0)	h(10)	CLPFC0	0
h(1)	h(9)	CLPFC1	0
h(2)	h(8)	CLPFC2	0
h(3)	h(7)	CLPFC3	12/128
h(4)	h(6)	CLPFC4	32/128
h(5)		CLPFC5	40/128

1.2.6.2.7.2.3 Sync/Burst Insertion

Following LPF, sync waveform is inserted onto the luma. The sync tip level and the sync amplitude are programmable as shown in Figure 1-64. The color burst is inserted onto the chroma. The amplitude of the color burst is specified by CBLVL register as follows:

$$ColorBurst = \begin{cases} CBLVL & \ldots \quad NTSC\ (CCM = 0) \\ \sqrt{2} \times CBLVL & \ldots \quad PAL\ (CCM = 1) \end{cases}$$

Figure 1-64. CVBS Video Amplitude



Closed caption and WSS signals are also inserted onto the appropriate lines of luma. The pulse amplitude of CC/WSS bit stream is automatically calculated based on the sync amplitude and the picture sync ratio setting. White 100% level is calculated by the following equation:

$$White_{100\%} = \begin{cases} CSLVL \times 10/4 & \ldots \quad CPSR = 0 \\ CSLVL \times 7/3 & \ldots \quad CPSR = 1 \end{cases}$$

The pulse amplitude of CC/WSS is calculated using the ratio of the white level defined in each standard.

The generic VBI-data is also inserted when used. The detail of the VBI-data insertion is described in Section 1.2.6.2.11.

1.2.6.2.7.2.4 QAM Modulation

The VENC generates the sub-carrier by internal direct digital synthesizer (DDS). The frequency of sub-carrier is determined by three increment parameters, SCP0, SCP1 and SCP2 as follows:

$$f_{sc} = \frac{1}{1024} \times \left(SCP0 + \frac{SCP1}{SCP2} \right) \times 27MHz$$

Typical settings of these parameters are shown in Table 1-40.

Table 1-40. Sub-carrier Increment Parameters

TV Format	SCP0	SCP1	SCP2	Frequency
NTSC-M/J	135	25	33	3.579545454… MHz
NTSC-4.43	168	2516	16875	4.433618749… MHz
PAL-B/D/G/H/K/I	168	2516	16875	4.433618749… MHz
PAL-M	135	87	143	3.575611888… MHz
PAL-N	168	2516	16875	4.433618749… MHz
PAL-Nc	135	14391	16875	3.58205625 MHz
PAL-60	168	2516	16875	4.433618749… MHz

The sub-carrier to horizontal (SC-H) phase can be controlled by the user. Writing the SCSD register automatically initializes the sub-carrier phase as the value specified in SCSD. The initialization is occurred at the line 4 in the color field 1 for NTSC and the line 1 in the color field 1 for PAL. The phase resolution of DDS is (1/1024)*360°.

Chroma modulation is performed as expressed by:

$$C = \begin{cases} U\sin(2\pi f_{sc}) + V\cos(2\pi f_{sc}) & \ldots \quad NTSC \\ U\sin(2\pi f_{sc}) \pm V\cos(2\pi f_{sc}) & \ldots \quad PAL \end{cases}$$

1.2.6.2.7.3 SECAM Encoding

1.2.6.2.7.3.1 DbDr Generation

First, SECAM YDbDr need to be generated using the CSC. In this example, the input is assumed to be full-range RGB [0…255] and the output is assumed to have 7:3 picture sync ratio with zero setup.

The fundamental SECAM YDbDr equation is expressed as follows:

$$\begin{bmatrix} E'_Y \\ D'_b \\ D'_r \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1.505 & 0 \\ 0 & 0 & -1.902 \end{bmatrix} \bullet \mathbf{M_0} \bullet \begin{bmatrix} E'_G \\ E'_B \\ E'_R \end{bmatrix}$$

Where D'_b has a range of 0 to ±1.33343 and D'_r has a range of 0 to ±1.333302 and needs to be scaled so that the resulted values have the corresponding deviation for the FM modulation.

The deviation calculation is explained in Section 1.2.6.2.7.3.3.

$$\begin{bmatrix} Y \\ D_b \\ D_r \end{bmatrix} = \begin{bmatrix} A_Y & 0 & 0 \\ 0 & A_{D_b} & 0 \\ 0 & 0 & A_{D_r} \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1.505 & 0 \\ 0 & 0 & -1.902 \end{bmatrix} \bullet \mathbf{M_0} \bullet \frac{1}{255} \begin{bmatrix} G \\ B \\ R \end{bmatrix}$$

$$= \frac{1}{64} \begin{bmatrix} 302 & 59 & 154 \\ -186 & 280 & -94 \\ 286 & 55 & -341 \end{bmatrix} \begin{bmatrix} G \\ B \\ R \end{bmatrix}$$

$$A_Y = \frac{7}{10} \times 1000(mV) \times \frac{4095(LSB)}{1400(mV)} = 2047.5$$

$$A_{D_b} = \frac{0.230(MHz)}{27(MHz)} \times 1024 \times 128 \times \frac{1}{1.33343} = 837.3$$

$$A_{D_r} = \frac{0.280(MHz)}{27(MHz)} \times 1024 \times 128 \times \frac{1}{1.333302} = 1019.4$$

$$Sync = \frac{3}{10} \times 1000(mV) \times \frac{4095(LSB)}{1400(mV)} = 878$$

Where D_b has a range of 0 to ±1117 and D_r has a range of 0 to ±1359.

1.2.6.2.7.3.2 Low-Frequency Pre-Emphasis

The YDbDr from CSC is applied to the LPF for a proper attenuation. The LPF function is already described in Section 1.2.6.2.7.2.2. The low-pass filtered Dr and Db are then applied to low-frequency pre-emphasis. The pre-emphasis is implemented by an IIR filter whose transfer function is expressed by:

$$H(z) = \frac{2.75 - 2.5z^{-6}}{1 - 0.75z^{-6}}$$

Then, a limiter clips the DbDr to conform to the maximum deviation requirement specified in SECAM standard. Figure 1-65 shows an example of the limiter configuration.

Figure 1-65. Limiter Configuration

$$-350kHz \le \Delta f_{OB} \le 506kHz$$

$$\text{CULCLP} = -\frac{0.35(MHz)}{27(MHz)} \times 1024 \times 128 = -1699$$

$$\text{CUUCLP} = +\frac{0.506(MHz)}{27(MHz)} \times 1024 \times 128 = +2456$$

$$-506kHz \le \Delta f_{OR} \le 350kHz$$

$$\text{CVLCLP} = -\frac{0.506(MHz)}{27(MHz)} \times 1024 \times 128 = -2456$$

$$\text{CVUCLP} = +\frac{0.35(MHz)}{27(MHz)} \times 1024 \times 128 = +1699$$

1.2.6.2.7.3.3 FM Modulation

The low-frequency, pre-emphasized DbDr is then applied to FM modulation. The frequency of the FM modulated sub-carrier is determined by the following equation:

$$f_{FM} = \frac{1}{1024} \times \frac{D_x}{128} \times 27MHz$$

Prior to the modulation, the offsets corresponding to the nominal subcarrier frequency of Db and Dr are added to the low-frequency, pre-emphasized DbDr. The Db and Dr offsets are set by the sub-carrier parameter register SCP1 and SCP2, respectively, as shown in Figure 1-66.

Figure 1-66. Sub-carrier Parameter Registers

$$f_{OB} = 4.25MHz$$

$$\text{SCP1} = \frac{4.25(MHz)}{27(MHz)} \times 1024 \times 128 = 20632$$

$$f_{OR} = 4.40625MHz$$

$$\text{SCP2} = \frac{4.40625(MHz)}{27(MHz)} \times 1024 \times 128 = 21390$$

The amplitude of the FM modulated sub-carrier is specified by the CBLVL register. While the CBLVL register specifies the burst amplitude for NTSC/PAL mode, it works differently in SECAM as the sub-carrier amplitude.

For color synchronization, the VENC does not support field identification, but line identification.

The phase of the sub-carrier is reset every line.

1.2.6.2.7.3.4 Bell Filter

A high-frequency pre-emphasis is performed on the FM modulated sub-carrier. The filter has a bell characteristic expressed by:

$$H(z) = \frac{8 - 2.25z^{-4} - 5.5z^{-6}}{1 - 0.5z^{-2}}$$

Finally, SECAM chroma is available from the bell filter output.

1.2.6.2.7.4 Luma Delay

The Y signal delay on the CVBS path can be adjusted by the CYDLY register. It adjusts the Y delay right before mixing Y and C to generate CVBS. The adjustable range is from –8 to 7 cycle of clk2x. S-Video Y is not affected.

1.2.6.2.8 WSS

The VENC can insert 14-bit video information (WSS) on line 23 of every frame to conform to the ITU-R BT.1119-2 (ETSI EN 300 294) Wide Screen Signaling specification for the 625i system. The 14-bit transmitted data is specified in the 20-bit WSS_DATA register. The WSS_EN register enables attribute insertion. Figure 1-67 shows the WSS_DATA register usage.

Figure 1-67. WSS_Data Register Usage

19 14	13 11	10 8	7 4	3 0
Unused	GROUP4	GROUP3	GROUP2	GROUP1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Transmission order is LSB first, that is, WSS_DATA[0] is transmitted first then WSS_DATA[1] follows.

The amplitude of the WSS symbol is automatically determined as five-seventh (5/7) of white 100%. As described earlier, the white level is calculated by the sync amplitude and picture-sync ratio registers (CSLVL and CPSR for CVBS).

1.2.6.2.9 CGMS

The VENC can insert 14-bit CGMS data on line 20 and line 283 to conform to the EIAJ CPR-1024 for 525i. The 14-bit VID data and the corresponding 6-bit CRC are set in the 20-bit WSS_DATA register. The CRC should be calculated by user based on the following equation.

$G(x) = x^6 + x + 1$, where x^6, x are preset to 1

The WSS_EN register enables attribute insertion. Figure 1-68 shows the WSS_DATA register usage.

Figure 1-68. WSS_Data Register Usage

19 14	13 6	5 2	1 0
CRC	WORD2	WORD1	WORD0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Transmission order is LSB first, that is, WSS_DATA[0] is transmitted first and then WSS_DATA[1] follows. WSS_DATA and WSS_EN registers are exclusively used for WSS and CGMS insertion depending on the timing format.

The amplitude of CGMS data is automatically determined as 70% of white (70IRE).

1.2.6.2.10 Closed Caption

The VENC supports closed caption encoding. Closed caption data is transmitted on the line 21 of the odd (top) field and the line 284 of the even (bottom) field in 525i mode. It is possible to specify the fields on which closed captioning is enabled by L21EN register.

Closed caption encoding for 625i system is also supported. Closed caption is inserted on line 22 of the odd field and line 335 of the even field for 625i systems.

The data should be written to the L21DO or L21DE register for odd or even fields, respectively. When data is written to L21DO, CAOST read status bit is changed to 1. When data is written to L21DE, CAEST becomes 1. These bits are automatically cleared to 0 when a caption data transmission is completed on the line 21 in odd field or the line 284 in even field (line 22 and 335 for 625i).

When the caption data register (L21DO or L21DE) is not written before the caption data transmission timing of the corresponding field, an ASCII code specified by L21DF register is used for transmission. A null character should be typically set to L21DF register.

The width of each data register is 8 bits, which consists of 7-bit data and the parity bit. It is your responsibility to calculate the parity bit. The amplitude of closed caption pulse is automatically determined as 50% of white (50IRE).

1.2.6.2.11 Raw VBI-data Insertion Mode

The VBI waveform which is not supported by VENC hardware can be inserted using raw VBI-data insertion mode. In this mode, the VBI waveform is synthesized by software according to the waveform requirements of the selected data type. The VBI_IF module sends VBI waveform to the VENC at the specified VBI lines.

The raw VBI-data insertion mode is enabled VBIEN register is set to 1. Otherwise, the VBI_IF module is basically in a reset state.

The VENC asserts venc_vbi_req pulses to the VBI_IF module during VBI period. The horizontal timing of venc_vbi_req can be configured by VBI_H_STA and VBI_H_STP registers. The reference timing of these registers is the internal TV counter. The vertical timing is determined by the AV window position which is specified by AV_V_STA and AV_V_STP registers. The timing is shown in Figure 1-69 and Figure 1-70.

The VBI_IF module keeps tracks of VBI line numbers by counting the number of venc_vbi_req pulses. On the specified VBI line number, the VBI_IF will send the samples from the payload to the VENC with vbi_venc_val set to HIGH. The data width of vbi_venc_data is only 8bit so zeros are padded to the 4 LSBs when inserted.

Note that CC/WSS and Macrovision have the priority over the VBI data when VBI data insertion is activated on the lines which have these pulses. The vbi_venc_val is disregarded at the lines CC/WSS and Macrovision are enabled.

1.2.6.2.12 Macrovision

The VENC supports analog copy protection Macrovision Rev7.1 to the SDTV CVBS and S-Video output. Due to strict security control by Macrovision, any information such as Macrovision register map, usage, and so on, are not directly distributed to the customers. These information are supposed to be given by Macrovision upon a certain certification.

1.2.6.2.13 Register Setting for Various Video Standards

Table 1-41 is a list of the typical register setting for various video standards.

Figure 1-69. VBI I/F Horizontal Timing

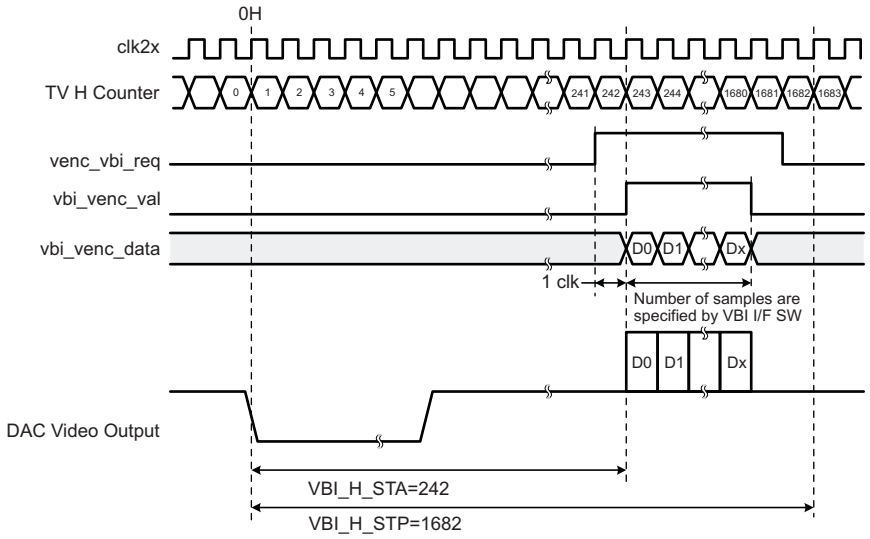


Figure 1-70. VBI I/F Vertical Timing

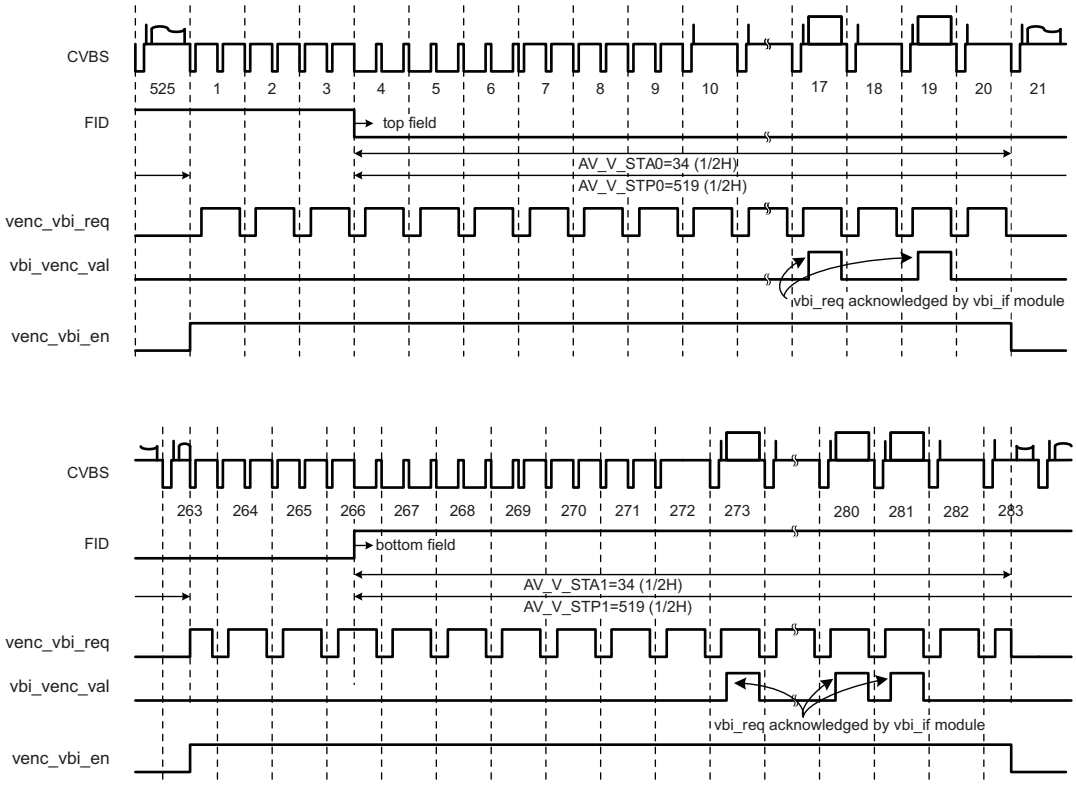


Table 1-41. Typical Register Setting for Various Video Standards

Parameter	Register Name	Location	SDTV							
			NTSC-M	NTSC-4.43	PAL	PAL-M	PAL-N	PAL-Nc	PAL-60	SECAM
Horizontal Interval	HITV	0x12[12:0]	1716	1716	1728	1716	1728	1728	1716	1728
Vertical Interval	VITV	0X12[28:16]	525	525	625	525	625	625	525	625
Scan Mode	ITLC	0x4[2]	1	1	1	1	1	1	1	1
Scan Format	FMT	0x84[11:8]	0	0	1	0	1	1	0	1
SDTV Vertical Sync Width	SVSW	0x84[3]	0	0	1	0	0	1	0	1
Horizontal Start of Active Video	AV_H_STA	0x88[12:0]	244	244	264	244	265	265	244	265
Horizontal Stop of Active Video	AV_H_STP	0x88[28:16]	1684	1684	1704	1684	1704	1704	1684	1704
Vertical Start Line of Active Video	AV_V_STA0	0x8c[12:0]	34	34	45	34	45	45	34	45
Vertical Stop Line of Active Video	AV_V_STP0	0x8c[28:16]	519	519	620	519	620	620	519	620
Vertical Start Line of Active Video	AV_V_STA1	0x90[12:0]	34	34	45	34	45	45	34	45
Vertical Stop Line of Active Video	AV_V_STP1	0x90[28:16]	519	519	620	519	620	620	519	620
Horizontal Burst Start	BST_H_STA	0x94[8:0]	143	143	151	156	151	151	143	157
Horizontal Burst Stop	BST_H_STP	0x94[24:16]	211	211	212	225	212	219	211	264
CVBS Sync Tip Level	CTLVL	0x9c[11:0]	188	188	148	188	188	148	148	148
CVBS Sync Amplitude	CSLVL	0x9c[27:16]	836	836	878	836	836	878	878	878
CVBS Picture Sync Ratio	CPSR	0xa0[0]	0	0	1	0	0	1	1	1
Color Modulation Mode	CCM	0xa0[5:4]	0	0	1	1	1	1	1	2
Burst Level	CBLVL	0xa0[27:16]	418	418	310	295	295	310	310	480
Sub-carrier Increment Integer	SCP0	0x148[23:16]	135	168	168	135	168	135	168	-
Sub-carrier Increment Numerator	SCP1	0x14C[15:0]	25	2516	2516	87	2516	14391	2516	20632
Sub-carrier Increment Denominator	SCP2	0x14C[31:16]	33	16875	16875	143	16875	16875	16875	21390

1.2.6.2.14 DAC Output

1.2.6.2.14.1 DAC Output Level

The VENC has one channel 12-bit digital outputs for DAC input. The DAC output code can be optionally inverted by the DAIV register.

1.2.6.2.14.2 DAC Output Configuration

It is your choice to specify which DAC outputs which video signal. DA0S-DA1S registers specify the DAC output signal as shown in Table 1-42.

Table 1-42. DAC Output Select

DAxS	DAC Output
0	CVBS
-15	Reserved

1.2.6.2.14.3 DAC Oversampling

The VENC is capable of 2x oversampling for the final DAC output. The 2x DAC oversampling eases the external analog filter cost as it can eliminate the unwanted image around the sampling frequency of clk2x. Setting DAUPS enables 2x oversampling. The oversampling filter is comprised of a 27 tap symmetric FIR filter with the programmable coefficients. The transfer function is expressed as:

$$H(z) = \sum_{n=0}^{26} h(n)\ z^{-n}$$

The clk4x is used in the oversampler as a DAC sampling clock. Its frequency should be double of clk2x if the hardware is configured to support 2x oversampling. Otherwise, the clk4x should be identical to clk2x. Whether or not to support 2x oversampling can be configured by INC_DUPS parameter in the Verilog HDL.

Table 1-43. DAC 2x Oversampling Filter Coefficients

Coefficients	Value	Default
h(0), h(26)	DUPFC0	0
h(1), h(25)	0	0
h(2), h(24)	DUPFC1	0
h(3), h(23)	0	0
h(4), h(22)	DUPFC2	0
h(5), h(21)	0	0
h(6), h(20)	DUPFC3	0
h(7), h(19)	0	0
h(8), h(18)	DUPFC4	6/128
h(9), h(17)	0	0
h(10), h(16)	DUPFC5	-20/128
h(11), h(15)	0	0
h(12), h(14)	DUPFC6	78/128
h(13)	1	1

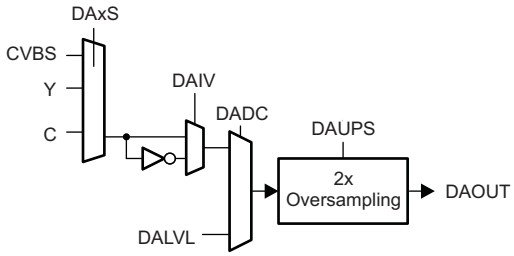
1.2.6.2.14.4 DAC Power Down

DAC power down is managed by the DA0E-DA1E registers. The corresponding DAC should be enabled by setting these registers to 1. Otherwise, DAC should be in power down state. Both DACs can be power down independently. By default, these registers are set to 0 to disable all DACs.

1.2.6.2.14.5 DAC DC Output Mode

A test mode to output the specified DC level on the DAC output pins is available. Setting DADC register to 1 switches DAC output from normal video signal to DALVL register. In this mode, both DACs have same DC output of DALVL D/A converted value.

Figure 1-71. DAC I/F Logic



1.2.7 High-Definition Video Encoder (HD_VENC)

The HD VENC module encodes the active video data from COMP module and sends it to 30-bit wide DVO (Digital Video Output) port by generating timing signals to control the data flow.

1.2.7.1 Features Supported

- The DVO port will support the output data rate up to 1080p formats (148.5 MHz × 30bits)
- The DVO support 10/20/30-bit wide output with embedded sync or discrete sync
- Fully programmable DVO timing generation (VS,HS,FID) to support any format flat display panel
- Fully programmable internal timing generation - VS, HS, FID, HBI, VBI, and ACT_VID for internal video compositor
- Programmable Color Space Converter: 10-bit data path.
- Gamma correction table
- A triple channel 10-bit current-steering DAC to support both Component and VGA output.

1.2.7.2 Functional Overview

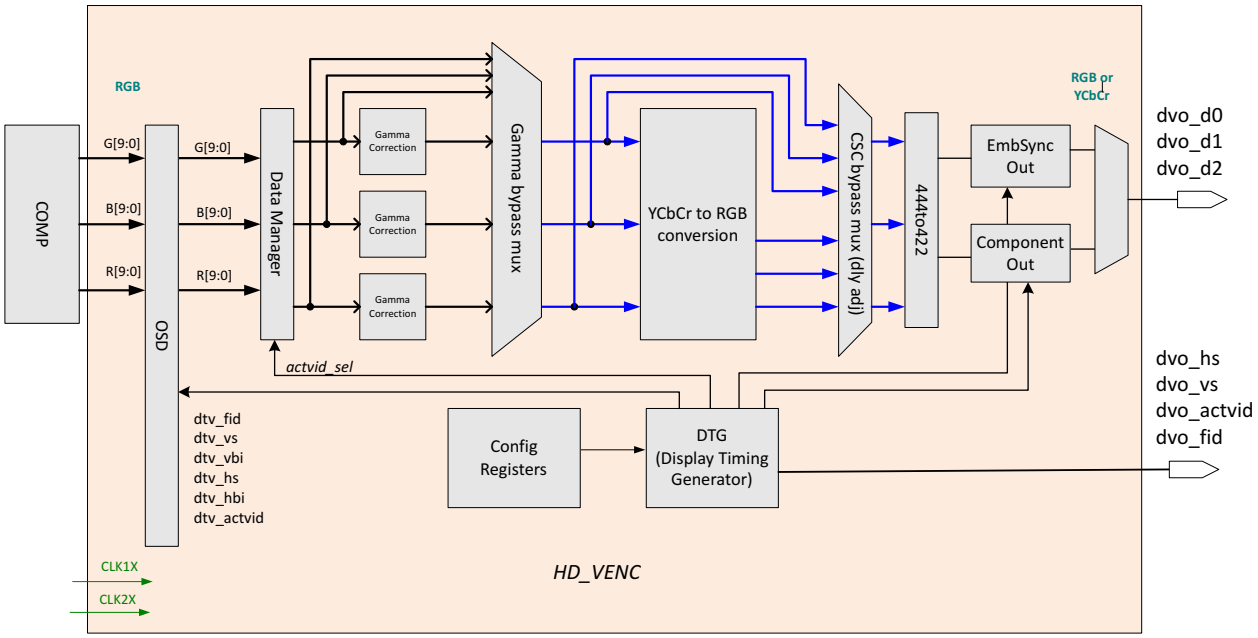
HD VENC primarily has two blocks: OSD and encoder. The OSD module is used to get the data from the COMP module using the sync signals generated by encoder module. In the device, HD VENC supports either digital (HD_VENC_D [HDMI/DVO1] and HD_VENC_D[DVO2]) or HD_VENC_A[HDCOMP].

Table 1-44 lists the possible display ports and corresponding VENC names. The basic block diagram of HD VENC module is shown in Figure 1-72.

Table 1-44. Display Ports and VENC Names

Display Port Name	Type	HDVENC Used	Port Name for PINMUX	Features Supported
HDMI/DVO1	Digital	HD_VENC_D	VOUT1	All features in digital data flow path
DVO2	Digital	HD_VENC_D	VOUT0	All features in digital data flow path
SDVENC	Analog	SD_VENC	Not Applicable	Please check SD VENC userguide for details.
HDCOMP	Analog	HD_VENC_A	Not applicable	All features in analog data flow path.

Figure 1-72. HD VENC Block Diagram



1.2.7.3 Video Data Interface to OSD

1.2.7.3.1 OSD Interface Overview

The interface between OSD and video display encoder are consisting of a 30-bit data bus, a pixel clock and five sync signals. By default 30-bit RGB video data will be passed from OSD to encoders on every rising edge of the pixel clock during active video period. The maximum frequency of the pixel clock is 148.5 MHz.

Table 1-45 lists all the control signals of this interface.

Table 1-45. OSD Interface Signals

Signal Names	Descriptions
dtv_fid	Field ID signal. This signal will toggle between “1” and “0” on every field in interlace mode. It will toggle between “1” and “0” on every frame in progressive mode. Programmability: controlled by register CFG13 (END_F1) and CFG10 (LINES).
dtv_vs	Vertical sync signal. This signal is a one-line long pulse. This pulse indicates the first line of each field in interlace mode. In progressive mode, it indicates the first line of each frame. Programmability: location of this signal is controlled V_BLANK1, VBLANK2, and FD1.
dtv_vbi	Vertical blank interval signal. This signal goes to “1” during non-active video period; it stays at “0” during active video period. Programmability: controlled by register CFG16/17. (For OSD interface only)
dtv_hs	Horizontal sync signal. This is the horizontal sync signal. Programmability; the start location and width of this signal are both programmable. They are controlled by CFG17. (For OSD interface only)
dtv_hbi	This is a four-pixels-wide and active-high signal. It appears once every video line. Programmability: The location of this pulse is programmable. (For OSD interface only)
dtv_actvid	This is active-video qualification signal. When this signal is high, encoder is expecting active video data output from OSD after one clock delay. Programmability: The fully programmable. (For OSD interface only)

Note: The dtv_vs, dtv_vbi, dtv_hs and dtv_hbi signals are generated by the encoder but are not used by the HDVPSS design. Therefore, all parameters related to these signals do not need to be specified.

The following figures illustrate the protocol of this interface. Figure 1-73 illustrates all the signals that are related to frame/field sync.

Figure 1-73. Vertical Sync Signals for OSD

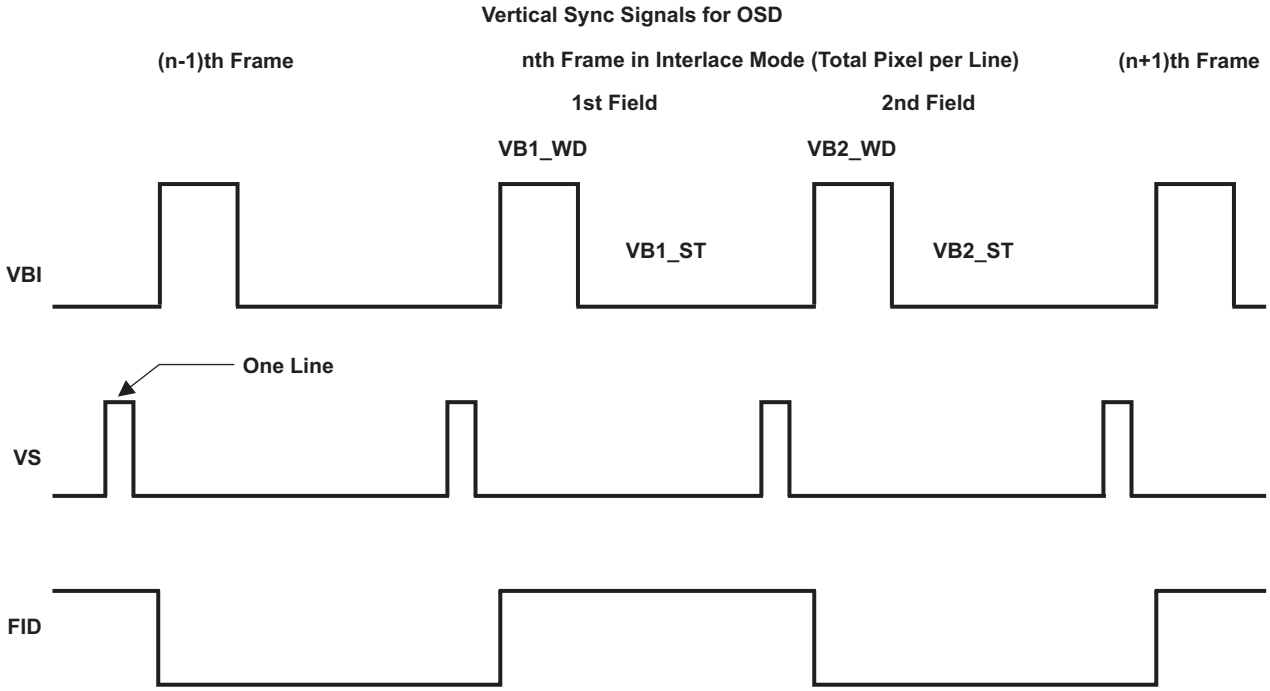


Figure 1-74 illustrates all the signals that are related to line sync. The programmable parameters with corresponding register names are indicated in the diagram.

Figure 1-74. Horizontal Sync-related Signal for OSD

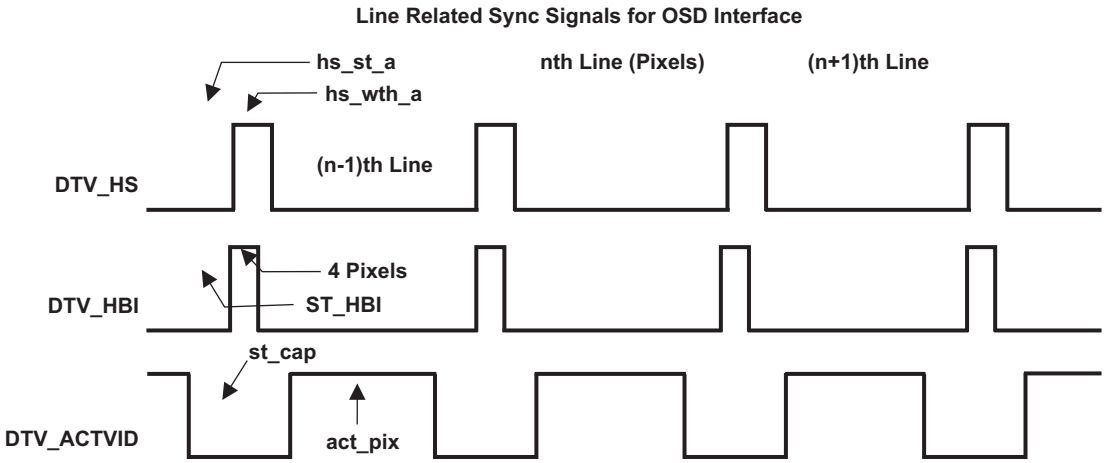
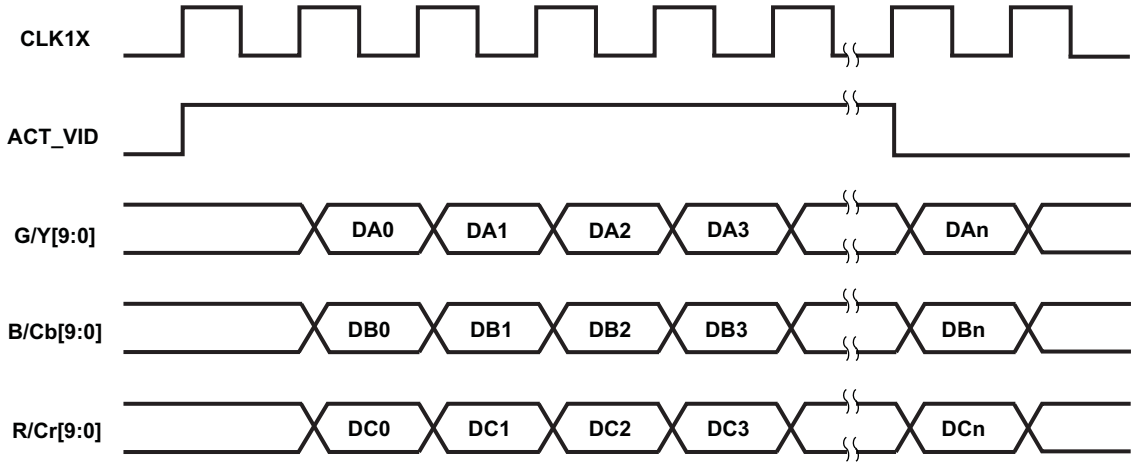


Figure 1-75 is the OSD-to-encoder data bus timing diagram. ACT_VID is the active video data qualification signal. Encoder will capture data from OSD after one clock delay when the ACT_VID goes to “high”.

The input 30-bit video data can also be in YCbCr 444 format. On chip processor will set the register bit “Y_RGBn” in CFG0 register to select RGB or YCbCr color spaces.

Figure 1-75. Video Data Interface Between OSD and Encoder



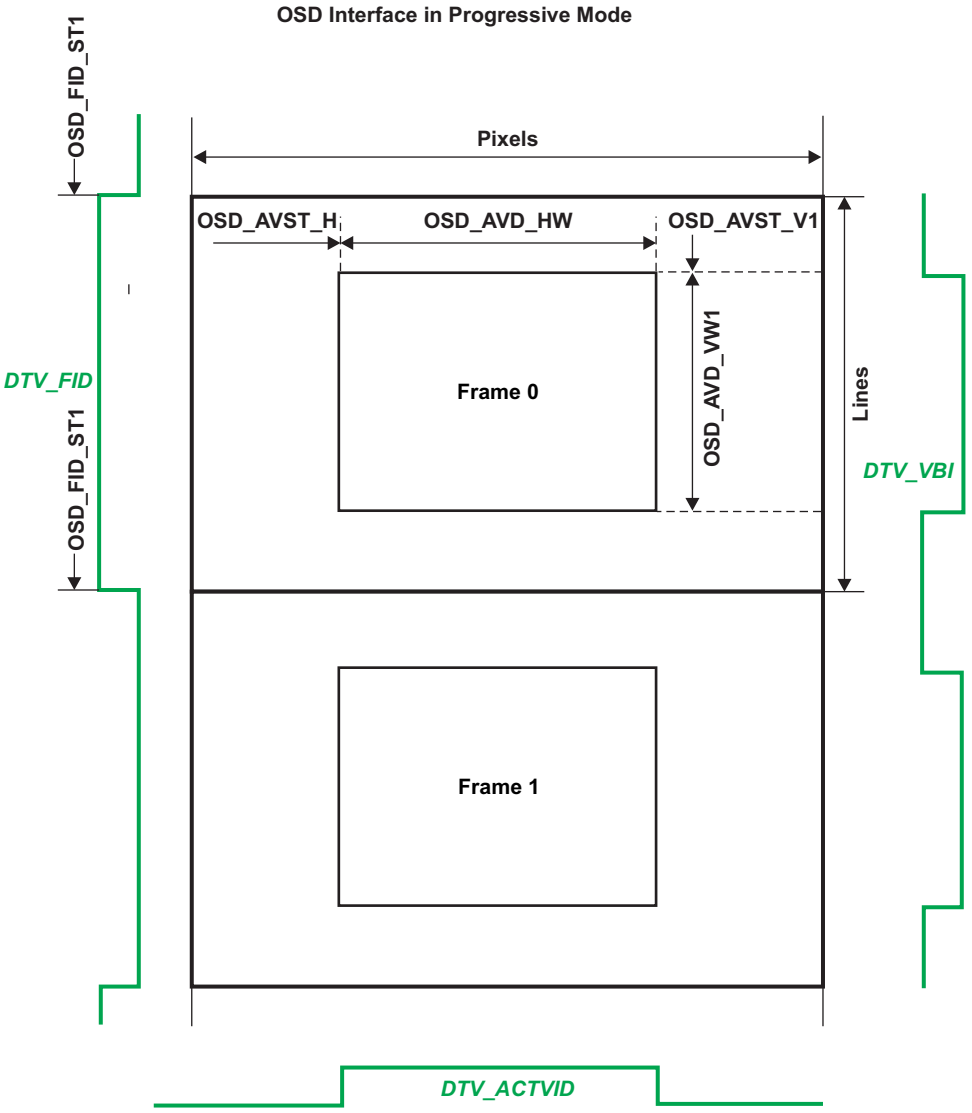
1.2.7.3.2 OSD Interface Configuration for Progressive Display

Figure 1-76 illustrates the OSD interface in the configuration for progressive display mode.

The corresponding register settings are described in the register section.

The green color signals are the signals outputting to OSD.

Figure 1-76. OSD Interface in Progressive Mode



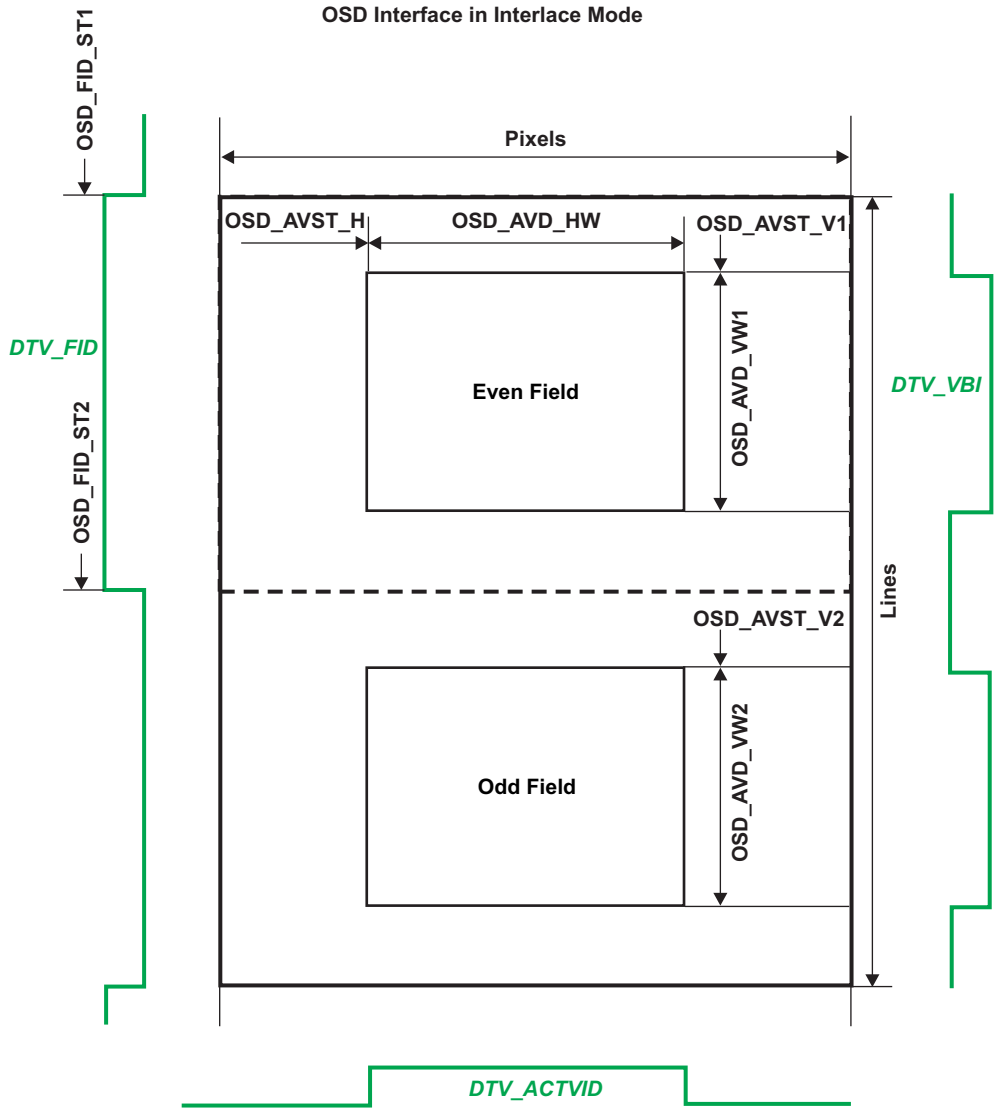
1.2.7.3.3 OSD Interface Configuration for Interlace Display

Figure 1-77 illustrates the OSD interface in the configuration for interlace display mode.

The corresponding register settings are described in the register section.

The green color signals are the signals outputting to OSD.

Figure 1-77. OSD Interface in Interlace Mode



1.2.7.4 Display Timing Generation (DTG)

The DTG (Display Timing Generator) block will generate all the sync and display timing signals for both OSD interface and DVO interface.

Due to the fast development of display panel technology and lack of the interface standard, the sync timing for DVO will be designed highly flexible. This will make sure that the device can interface to the most panels used by digital TV industry; meanwhile, maintains the simplicity for the software programming.

The details of OSD interface and DVO interface are described in the corresponding sections.

1.2.7.5 DVO (Digital Video Output)

1.2.7.5.1 Output Formats of DVO

Table 1-46 lists all formats that the DVO supports.

Table 1-46. DVO Formats

Formats	DVO_D0	DVO_D1	DVO_D2
Single-stream 656	YCbCr	(Unused)	(Unused)
Dual-stream 656	Y	CbCr	(Unused)
Tri-stream 656	Y/G	Cb/B	Cr/R
YUV422 20bit output with discrete sync	Y	CbCr	(Unused)
30bit output with discrete sync	Y/G	Cb/B	Cr/R

During the two discrete sync modes, following are the sync signals that DVO outputs:

1. DVO_HS
2. DVO_VS
3. DVO_ACTVID
4. DVO_FID

1.2.7.5.2 Embedded Sync Word Definitions of DVO

DVO of the device supports single/dual/tri stream with embedded sync (SAV/EAV).

The active video data in single/dual stream formats are in 4:2:2 YCbCr format.

DVO of the device also supports 10-bit video, the embedded sync SAV/EAV in 10bit format as: 3FF, 000, 000, XXX. All the possible values for XXX are listed in Table 1-47.

Table 1-47. Definition of SAV and EAV words

BITS	9	8	7	6	5	4	3	2	1	0	SAV/EAV	Hex
Function	1	F	V	H	P3	P2	P1	P0	x	x		
0	1	0	0	0	0	0	0	0	0	0	SAV	200
1	1	0	0	1	1	1	0	1	0	0	EAV	276
2	1	0	1	0	1	0	1	1	0	0	SAV	2AC
3	1	0	1	1	0	1	1	0	0	0	EAV	2D8
4	1	1	0	0	0	1	1	1	0	0	SAV	31C
5	1	1	0	1	1	0	1	0	0	0	EAV	368
6	1	1	1	0	1	1	0	0	0	0	SAV	3B0
7	1	1	1	1	0	0	0	1	0	0	EAV	3C4

1.2.7.5.3 DVO Interface Configuration

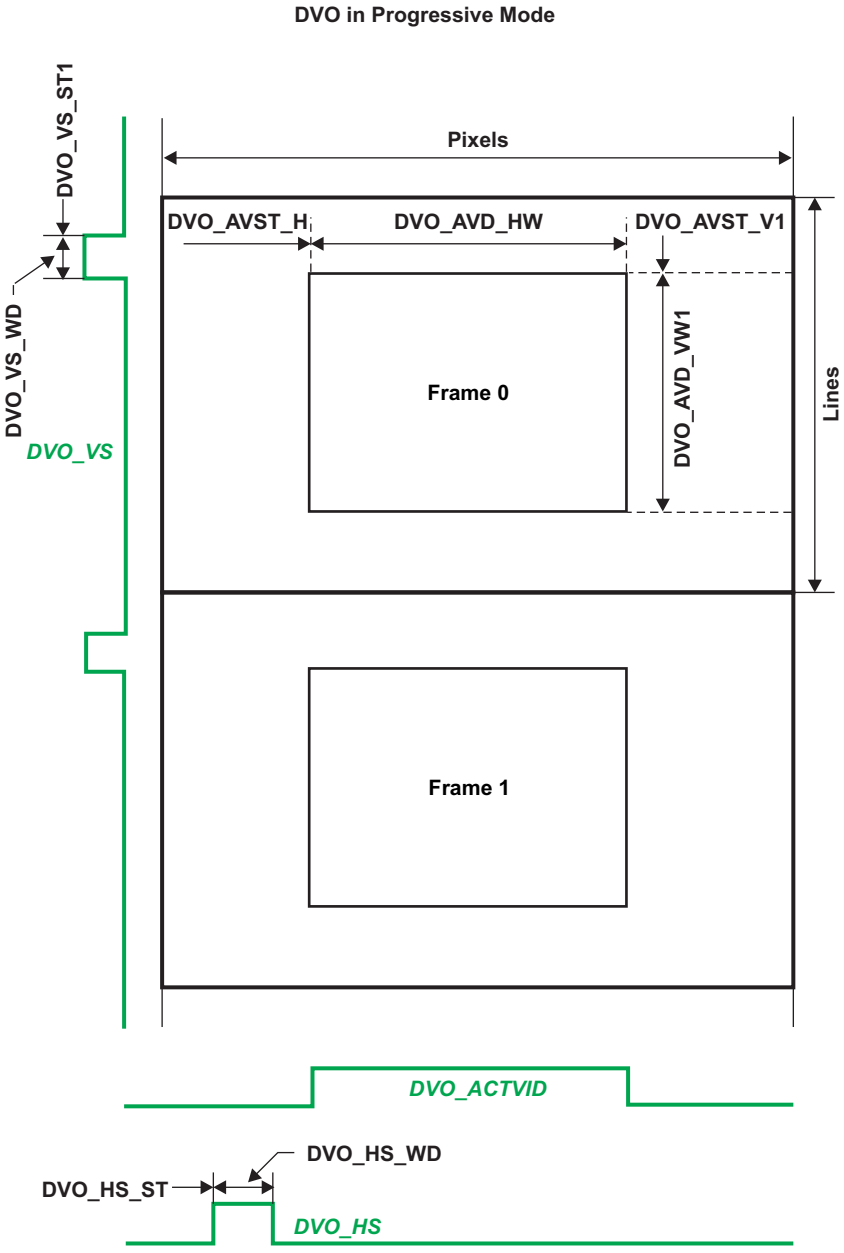
The design goal of the DVO of the device is to interface to all standard and non-standard panels seamlessly. To archive this goal, the DVO of the device has been refined with ultimate flexibility; meanwhile maintaining simplicity for the software programming. Following subsections present all the interface signals for both progressive and interface display devices.

1.2.7.5.3.1 DVO Interface for Progressive Display

The progressive display format is the display format for most flat panel display devices, such LCD, Plasma, and DLP. Figure 1-78 illustrates the progressive configuration of DVO port. The configuration register settings are described in the register section.

The green color signals are the signals outputting from the DVO port.

Figure 1-78. Progressive Configuration of DVO

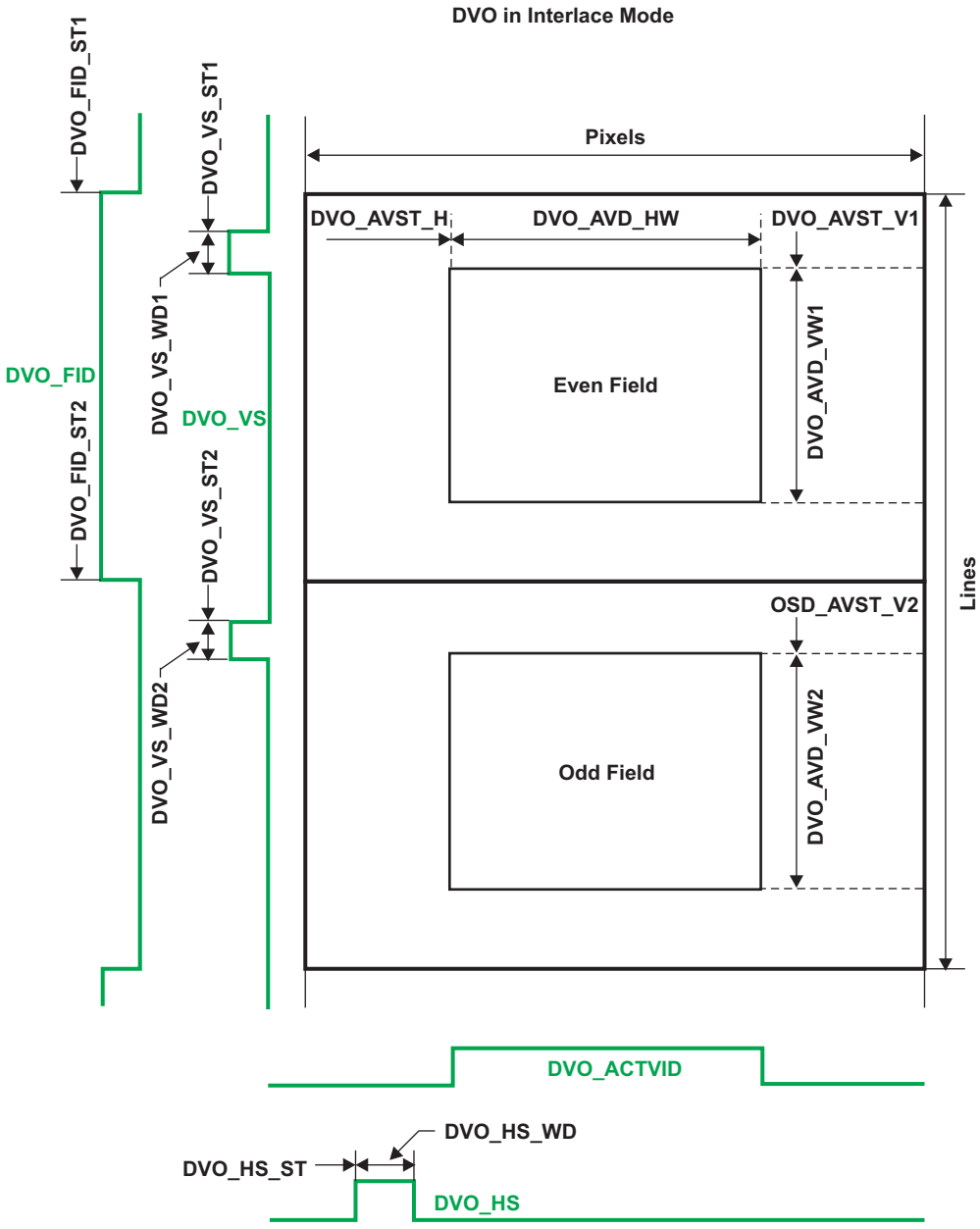


1.2.7.5.3.2 DVO Interface for Interlace Display

Figure 1-79 illustrates the interlace configuration of DVO port. The configuration register settings are described in the register section.

The green color signals are the signals outputting from the DVO port.

Figure 1-79. Interlace Configuration of DVO



1.2.7.6 JEIDA Format of DVO

A new output format of DVO has been added and a corresponding control bit “JED” has also been added.

This bit is used to make DVO interfacing to certain LCD panels seamlessly. Table 1-48 illustrates the JEIDA and VESA (the normal/default format we use) format.

Table 1-48. JEIDA and VESA Format

VESA Mode		JEIDA Mode	
RGB Data	**DVO Port**	**RGB Data**	**DVO Port**
G/B/R[9]	DV_OUT0/1/2[9]	G/B/R[3]	DV_OUT0/1/2[9]
G/B/R[8]	DV_OUT0/1/2[8]	G/B/R[2]	DV_OUT0/1/2[8]
G/B/R[7]	DV_OUT0/1/2[7]	G/B/R[9]	DV_OUT0/1/2[7]
G/B/R[6]	DV_OUT0/1/2[6]	G/B/R[8]	DV_OUT0/1/2[6]
G/B/R[5]	DV_OUT0/1/2[5]	G/B/R[7]	DV_OUT0/1/2[5]
G/B/R[4]	DV_OUT0/1/2[4]	G/B/R[6]	DV_OUT0/1/2[4]
G/B/R[3]	DV_OUT0/1/2[3]	G/B/R[5]	DV_OUT0/1/2[3]
G/B/R[2]	DV_OUT0/1/2[2]	G/B/R[4]	DV_OUT0/1/2[2]
G/B/R[1]	DV_OUT0/1/2[1]	G/B/R[1]	DV_OUT0/1/2[1]
G/B/R[0]	DV_OUT0/1/2[0]	G/B/R[0]	DV_OUT0/1/2[0]

The JEIDA mode is only used in three-channel RGB with discrete sync output format.

1.2.7.7 VBI Data Service

Following are the commonly used VBI-data-services on analog component video interface, these functions are supported by the hardware inside the encoder.

- Type-A and Type-B data packets based on CEA-805-A standard, which include CGMS-A/APS(Analog Protection System)/AFD(Active Format Description)/RCI(Re-distribution Control Information)
- International VBI data support based on the international standard IEC-62375, which is mainly for the applications outside of north-American.

A typical VBI data package usually consists of three segments, they are illustrated in Figure 1-80.

Figure 1-80. Typical VBI Data Package

Each segment has its-own programmable symbol. Number of symbol for each segment is also programmable. The minimum element of a symbol is one pixel clock. For different display formats, different pixel clocks have been used. All of these require the VBI data encoder can be used for different display interface formats.

Two programmable VBI data encoders have been designed to service all the above functional requirement. These VBI data line encoders are symbol based, it can accommodate different symbol modulations.

- The first VBI line will be used for type-A data packet of CEA-805-A standard or IEC-62375 standard.
- The second VBI line will be used for type-B data packet of CEA-805-A standard

Table 1-49 shows the first line encoder's programmable capacity. The payload symbol can be programed in the phase-modulation representation. It can be used for type-A VBI data service of CEA-805-A or IEC-62375.

Table 1-49. Programmable Capacity of First Line Encoder

Start Symbol	Header Symbol	Payload Symbol
Max. = 64	Max. = 64	Max. = 128

Table 1-50 shows the second line encoder's programmable capacity, it can be used for type-B VBI data service of CEA-805-A. The payload has been increased to accommodate large data packets.

Table 1-50. Programmable Capacity of Second Line Encoder

Start Symbol	Header Symbol	Payload Symbol
Max. = 64	Max. = 64	Max. = 128

Although these two line encoders are targeting to some specific VBI applications, but they are flexible enough to be used by some other applications. For example, both encoder data-lines can be transmitted on any line in a frame or a field (by set the line number to register VBI_L1).

These VBI data line encoders can support up to two VBI lines in a frame or a field. If the host-CPU updates the VBI data registers at the frame rate (or field rate), the encoders are able to send out two VBI lines per frame or per field.

1.2.7.8 Processing Blocks

The main processing blocks in encoder module are:

- Gamma Correction (Gamm)
- Color Space Conversion (CSC)

1.2.7.8.1 Gamma Correction (Gamm)

The gamma correction modules perform a gamma or color correction independently for each color in RGB color space by using configurable LUT (Look-Up Table) in RAM. Each Gamm module reads 10-bit input and outputs 10-bit value from its corresponding Look-up Table entry. The RAM has 1024 32-bit words and contains three LUTs for each color as shown in Table 1-51.

Table 1-51. Gamma Correction LUT

	bit[9:0]	bit[19:10]	bit[29:20]	bit[31:30]
Address at 0x0000	LUT_G[0]	LUT_B[0]	LUT_R[0]	reserved, return 0 during read
Address at 0x0004	LUT_G[1]	LUT_B[1]	LUT_R[1]	reserved, return 0 during read
Address at 0x0008	LUT_G[2]	LUT_B[2]	LUT_R[2]	reserved, return 0 during read
...	...	...	...	...
Address at 0x0FFC	LUT_G[1023]	LUT_B[1023]	LUT_R[1023]	reserved, return 0 during read

- If CFG0.RD_MEM = '1', processor can read and write these LUTs as regular memory.
- If CFG0.RD_MEM = '0', processor can only write to these LUTs as regular memory.

Table 1-52 shows the memory map address of configuration register and the LUT memories.

Table 1-52. Memory Map Addresses for Configuration Register and LUT Memories

Descriptions	Start Address[12:0]	End Address[12:0]
HD VENC MMR	0x0000	0x0FFF
LUT RAM	0x1000	0x1FFF

Gamm module can be bypassed by setting CFG0.BYPS_GC bit-field to 1.

1.2.7.8.2 Color Space Conversion (CSC)

The color space conversion (CSC) module is used to convert the input data from one color space to another by using a programmable 3 × 3 matrix. See the *Color Space Converter* section for more details. The CSC module can be bypassed by setting CFG0.BYPS_CS bit-field to 1.

1.2.8 VIP Parser

The VIP Parser module is used to capture the video data into the HDVPSS module.

1.2.8.1 Features

The device has two identical instances of the VIP subsystem. Each VIP instance has one VIP parser.

For one VIP Parser instance, the video capture requirements include:

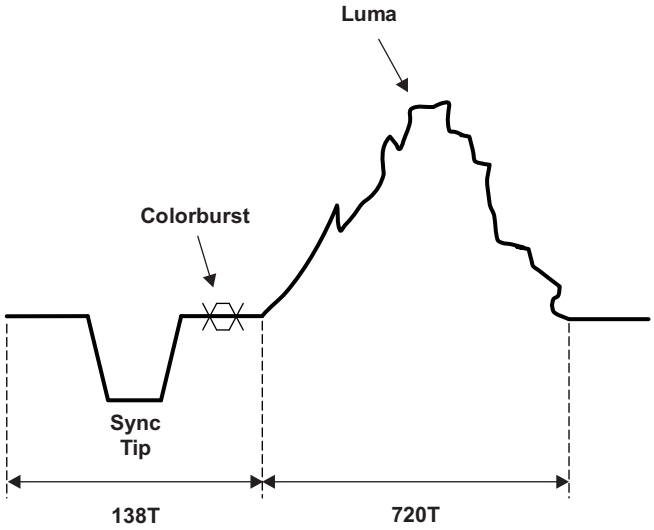
- Two Pixel Clock Input Domains are supported (Port A and Port B)
  - Each Pixel Clock Input Domain has separate clock and framing signals.
  - Each Pixel Clock Input Domain can support embedded (BT.656 style) or discrete (BT.601 style) sync.
  - Pixel Clock Input Domain Port A supports up to one 24-bit input data bus, including BT.1120 style embedded sync for 16 and 24 bit data.
  - Pixel Clock Input Domain Port B supports one 8-bit input data bus. At the SOC level, the same device pins may be shared between Ports A and B. One 24 bit chip level set of device pins is shared. Port A has access to all 24 bits. Port B only has access to 8 bits.
- Embedded Sync data interface mode supports single or multiplexed sources
- Discrete Sync data interface mode supports only single source input
- The two Pixel Clock Input Domains can be individually configured in any combination of Embedded or Discrete Sync
- Vertical ancillary data is supported for each input source. For discrete sync modes where vertical ancillary data is not specified using signals, vertical ancillary data will appear in active video buffer.
- A maximum of 8 + 1 (8 normal line sources + 1 split-line source) multiplexed sources are supported for a single Pixel Clock Input Domain using TI Line Mux Mode
- Multiplexed data can only appear in embedded sync mode
- Where possible, blanking pixels that may contain embedded vertical ancillary data will be stored in a dedicated buffer per each video source
- Optional selection of channel (Luma or Chroma or both) from which Vertical Ancillary data is extracted for YUV422 source
- For RGB source, Vertical Ancillary data can be found in one of the R, G, or B channels. The VIP Parser can select the channel from which Vertical Ancillary data is extracted.
- Ancillary Data can appear in the Horizontal Blanking as well as the Vertical Blanking. Typically, only Vertical Blanking Ancillary Data is captured. However, Horizontal Blanking Ancillary Data can be captured as well using HSYNC style discrete sync capture mode.
- Video up to WUXGA (1920 × 1200) can be supported using Port A in 16- or 24-bit mode.

1.2.8.2 Functional Description

1.2.8.2.1 Analog Video

A digital interface stream is based on analog video. The waveform for a line of NTSC analog video is shown in Figure 1-81.

Figure 1-81. NTSC Analog Video Waveform for One Horizontal Line



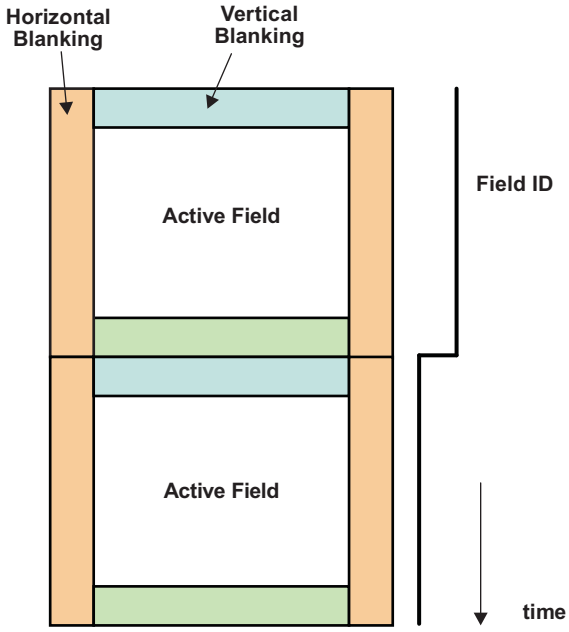
T is a time constant. For NTSC, T=1/13.5 MHz = 74ns.

1.2.8.2.2 Digitized Video

Digitized video is based on scan lines in found in analog video. BT.601 uses various sync signals to specify when a new field and a new line starts. BT.656 and BT.1120 uses sync words embedded in the data stream to specify start of field and start of line.

An image can be digitized into regions shown in Figure 1-82.

Figure 1-82. Digitized Video



With the capability to encode sync words inside the data stream, there is more flexibility for adding non-video related data, called Ancillary Data. Also, code words embedded in the digital stream can be used as a type of identifier for multiplexing several sources of video into one data stream. Such a multi-camera multiplex is useful in the digital security markets.

Figure 1-83 shows End-of-Active-Video (EAV) and Start-of-Active-Video (SAV) code words added to a video transmission. The period between the EAV and SAV is equivalent to Horizontal Blanking. The period between the SAV to the next EAV is active video or vertical blanking.

In the BT.656 or BT.1120 embedded code word scheme, three bits of the EAV/SAV code word are important: F (field), H (horizontal blanking), and V (vertical blanking).

Figure 1-83. Code Word Embedded Video Format

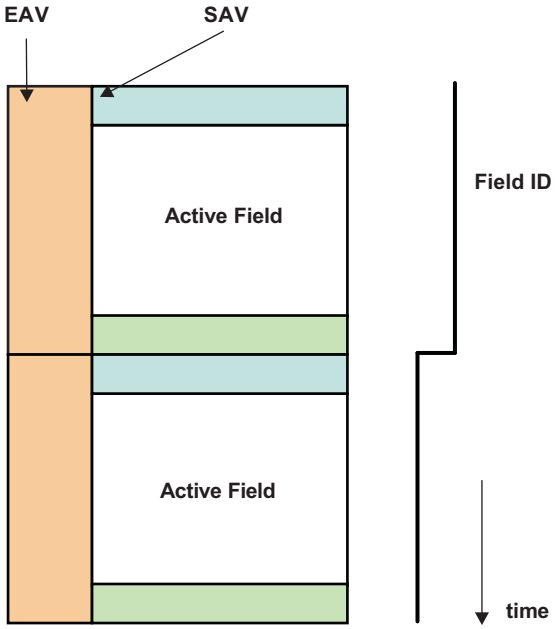
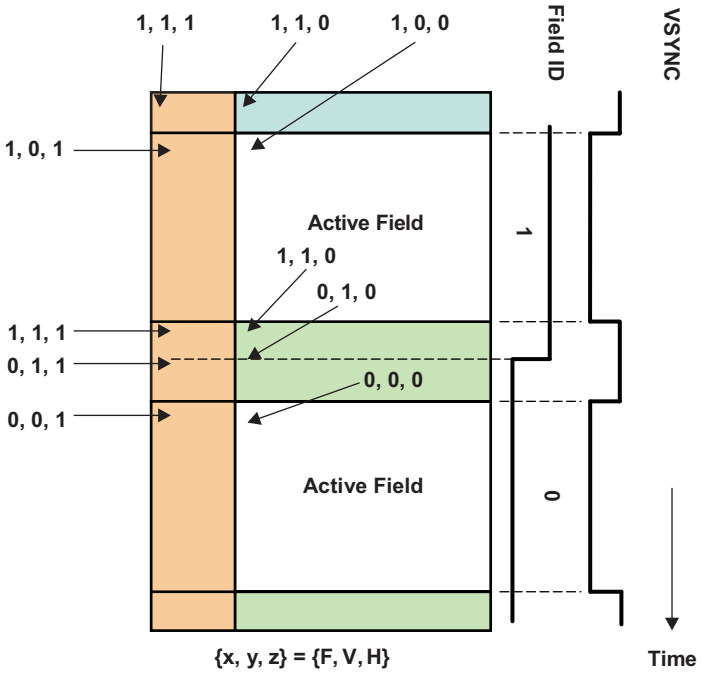


Figure 1-84 shows the values of F, V, and H flags at different locations in the picture. The Field flag represents the state of the Field ID for the picture. For progressive frames, F is always '0.' The V flag specifies vertical blanking areas. The H flag specifies horizontal blanking portions of the picture.

Figure 1-84. Digitized Video with F, V, and H Flags in EAV/SAV



1.2.8.2.3 Frame Buffers

The VIP/VPDMA supports Frame Buffers in DDR for Active Video and Ancillary Data.

4:2:2 data is always saved in packed pixel buffers.

4:2:0 data is saved in Planar Luma buffers and Planar CbCr pair buffers.

A Luma Frame Buffer is a Planar storage area. Each line is the width in pixels (1Byte/pixel) of the output picture size format. The frame buffer contains the number of active video lines in the output picture size format.

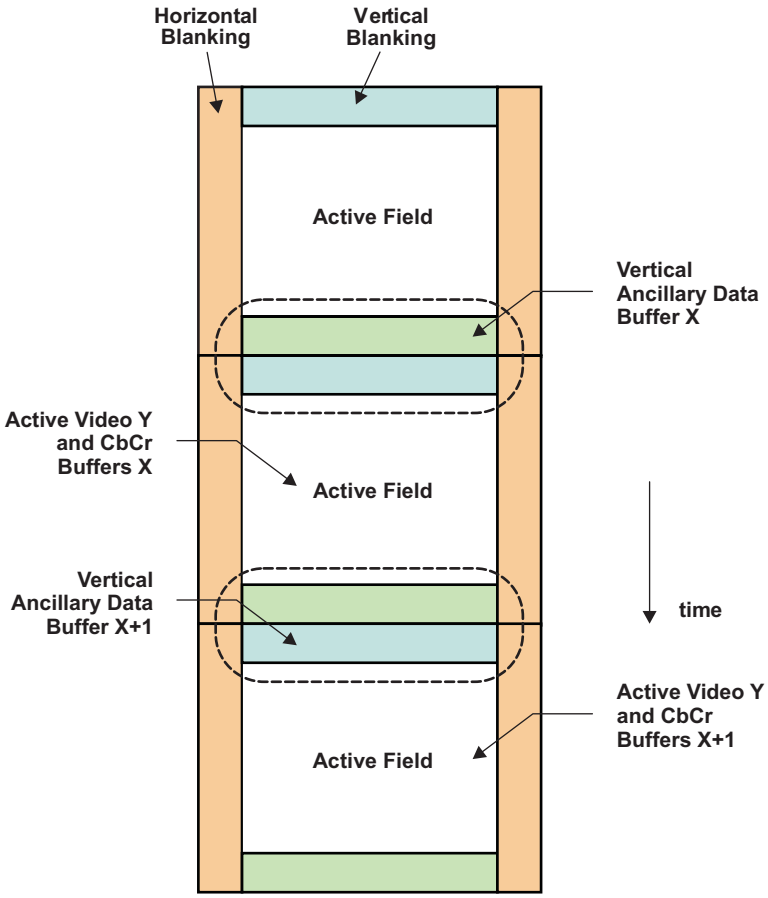
A Chroma Pair Frame Buffer is Planar storage of CbCr pixel pairs, with each pixel being a byte. For 4:2:0 storage, N lines in the output picture active video results in N/2 lines of CbCr pairs being stored.

The Ancillary Data buffer is different than the Active Video Frame Buffers. The Ancillary Data buffer only stores Vertical Blanking Ancillary Data. The number of lines in the Ancillary Data buffer is the same as the number of Vertical Blanking lines. Typically, only one channel is extracted from the Vertical Blanking data, so the width of the Ancillary Data buffer is the same as the width of the Luma Buffer.

In 8-bit input mode, it is possible for both Luma and Chroma sites to be extracted for Vertical Ancillary data. Each color component is strobed on separate input clock cycles. In this case, the line width of the Ancillary data is twice the Luma line width of the picture. Both Luma and Chroma sites cannot be extracted for 16-bit input mode because both Luma and Chroma are sent on the same input clock cycle and the Ancillary port to the VPDMA VPI is only 8 bits wide.

Figure 1-85 shows how the planar data regions are stored in DDR. The vertical blanking data is stored in a set of Planar Buffers. Note that the bottom of the Vertical Ancillary Data from the previous field or frame is stored in the same buffer as the top of the Vertical Ancillary Data from the current field or frame.

Figure 1-85. Planar Buffer Storage Description



The Luma representing Active Video is stored in a set of Planar Buffers. The CbCr Chroma Pairs are stored in a set of Planar Buffers.

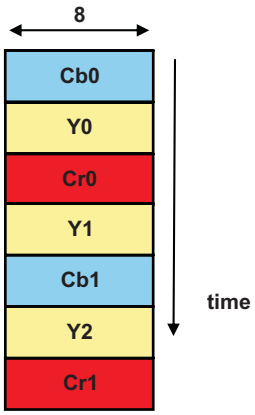
1.2.8.2.4 Input Data Interface

This section describes how the data (luma and chroma data for YUV422 format capture & R,G and B data for RGB888 format capture) is muxed for the interface modes described below.

1.2.8.2.4.1 8b Interface Mode

In 8b data interface mode, the input pixels are multiplexed according to Figure 1-86. The Chroma Format is 4:2:2. Sites with Cb/Cr pixels are known as Chroma sites. Those sites with Y pixels are known as Luma sites.

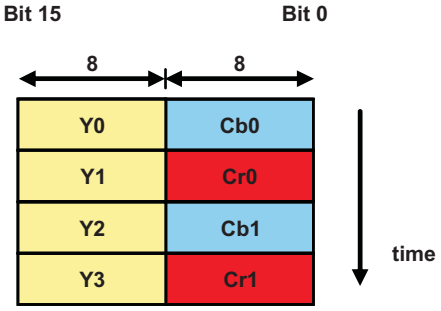
Figure 1-86. 8b Interface Discrete Sync Pixel Multiplexing



1.2.8.2.4.2 16b Interface Mode

In 16b interface mode, Luma is on 8 bits of the data bus and Cb/Cr chroma pixels alternate on the other 8 bits of the data bus as shown in Figure 1-87.

Figure 1-87. 16b Interface Discrete Sync Pixel Multiplexing

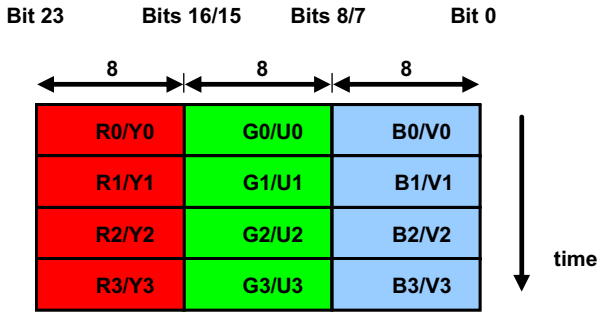


1.2.8.2.4.3 24b Interface Mode

RGB or YUV444 data is sent in 24b Interface Mode. The three components are packed into the data bus and sent to the VPDMA. The 24-bit Luma VPI client to the VPDMA carries all three components. This data is saved to the DDR in packed mode. That is, the three components are not separated by hardware. The 24-bit data bus is shown in Figure 1-88.

Ancillary data is saved in the Ancillary Data buffer. The ctrl_chan_sel configuration register is used to select whether the ancillary data is from the R/Y, G/U, or B/V channels.

Figure 1-88. 24b Interface RGB or YUV444 Discrete Sync

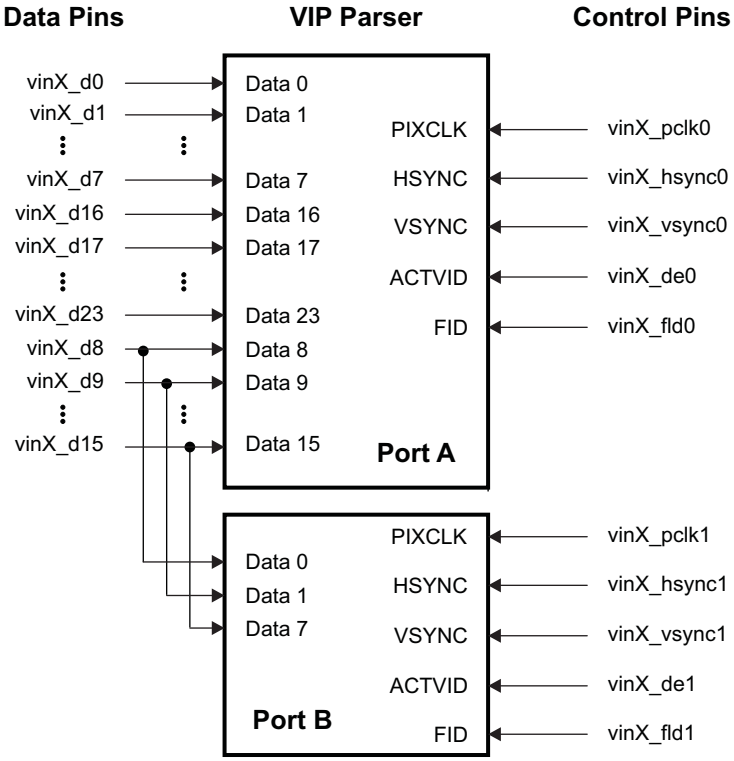


1.2.8.2.5 Input Ports and Sharing of the 24 Bit Data Bus

The VIP Parser supports two independent Pixel Clock Input Domains, which shall be called Port A and Port B. Port A supports a single 24-bit data bus at the instance level and Port B supports a single 8-bit data bus at the instance level.

For the device, a single set of 24 device pins are used to drive both Ports A and B, as shown in the following figure.

Figure 1-89. 24 Device Pins for Ports A and B



The configuration for each device input port is described in Table 1-53.

Table 1-53. Valid Input Port Configurations

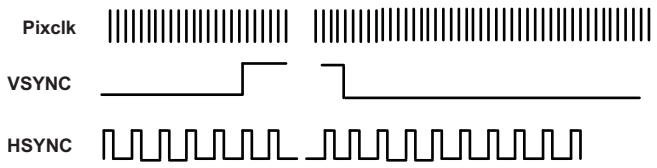
Port A	Port B
8 Bit	Off
16 Bit	Off
24 Bit	Off
8 Bit	8 Bit
16 Bit	8 Bit
Off	8 Bit

Each Port can individually be configured as Discrete Sync or Embedded Sync.

1.2.8.2.5.1 Signal Relationships

A digital representation of video can be realized by using HSYNC and VSYNC signals to identify frame start and line start. Suppose HSYNC and VSYNC are active high, Figure 1-90 shows the general relationship of these signals.

Figure 1-90. Discrete Sync Signals



Every Pixclk cycle carries either an active pixel or a blanking pixel. VSYNC pulses between two fields (or frames, in the case of progressive video). HSYNC pulses to signify the beginning of every line. An ACTVID signal can be used as a data valid to specify active video.

Discrete Sync cannot be used with any multi-camera multiplexed stream inputs. In the device, if Port A is configured for 24 bit discrete sync, then Port B must be disabled since there are no more data input pins left over for Port B.

If Port A is not 24 bits, then the 8-bit Port B can be configured and enabled for either discrete or embedded sync.

Discrete sync basic mode is used to determine the type of vertical blanking signal. DISCRETE_BASIC_MODE='0' means that the vertical blanking interval is specified by the signaling. In the cases where there is no awareness of vertical blanking start and end, vertical blanking data is saved in the Active Video Buffer (DISCRETE_BASIC_MODE='1').

1.2.8.2.5.2 General 5 Pin Interfaces

Discrete Sync signal handling varies among different sending devices. The information that must be conveyed includes the pixel data value, field ID, horizontal blanking, and vertical blanking. Many devices can be configured to adjust the timing of the signals relative to each other.

In this section, DATA will be depicted as 8 bits. However, discrete sync does optionally support 16b and 24b data input. Type 1 is named after a generic five pin interface between the sending and receiving devices.

In Figure 1-91, P0 represents the first pixel in the horizontal blanking interval following the last vertical blanking line of the previous field or frame. HSYNC specifies the horizontal blanking region and VSYNC specifies that the P0 pixel is in the vertical sync area. HSYNC can be a strobe that is active one or more cycles and can deassert before the actual end of horizontal blanking or HSYNC may be active for the full duration of horizontal blanking.

Likewise, VSYNC can be a strobe that is active one or more cycles and can deassert before the actual end of vertical blanking or VSYNC may be active for the full duration of vertical blanking.

FID can change at this pixel or it may change later. For interlaced source, though, the FID will be inverted for this pixel at the same time point in the next field. So, it does not really matter when FID is captured. Many sending devices allow the location of FID changes to be programmable.

In this diagram and all others in this document, the active polarities of the interface signals can be either high or low. For the sake of uniformity in this document, all polarities are drawn active high. Also, different vendors have different datasheet names for the interface signals.

Figure 1-91. Type 1, First Horizontal Blanking Pixel

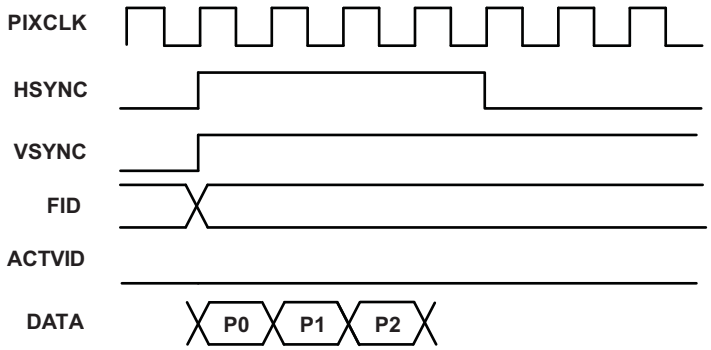
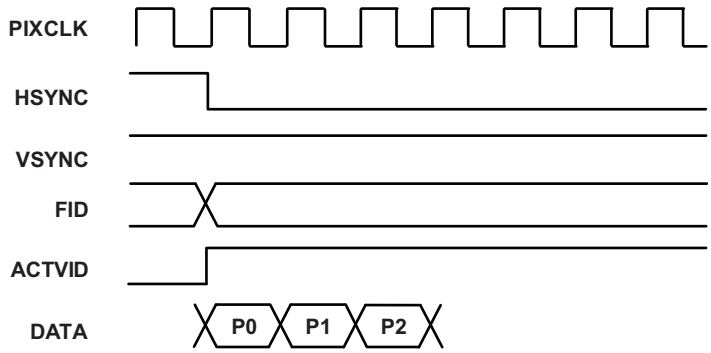


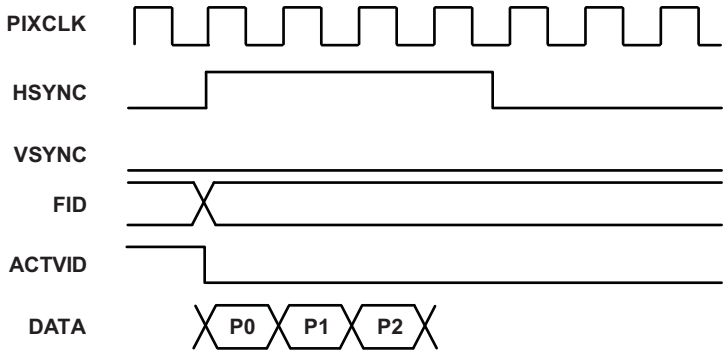
Figure 1-92 shows the P0 pixel being the first Chroma Channel data value in the Vertical Ancillary Data region. HSYNC is definitely de-asserted by now since P0 is no longer in horizontal blanking. ACTVID may or may not be active for Vertical Ancillary Data. Some devices consider these pixels to be Active (as in non-horizontal blanking). Other devices consider only video to be ACTIVE Video.

Figure 1-92. Type 1, First Vertical Ancillary Data Pixel



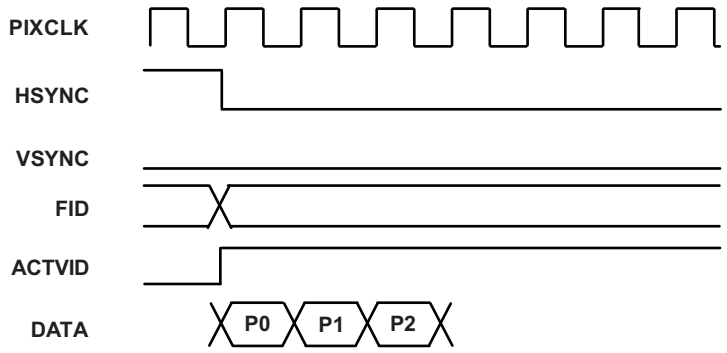
Following the vertical blanking region, the video portion of the field or frame starts. Figure 1-93 shows the horizontal blanking area in this video portion of the field or frame. P0 is the first pixel in the horizontal blanking. HSYNC is active for one or more pixel clocks. VSYNC is inactive in this video area. FID can change here. ACTVID is low since P0 is horizontal blanking.

Figure 1-93. Type 1, Horizontal Blanking in Video Region



In Figure 1-94, P0 represents the first Chroma pixel in the Active video line. HSYNC is inactive, since P0 is in the active video region. Likewise, VSYNC is inactive. FID may or may not change here. ACTVID is high to signal capturing of video pixels.

Figure 1-94. Type 1, First Video Pixel



1.2.8.2.5.3 Signal Subsets—4 Pin VSYNC, ACTVID, and FID

A sending device may use only a subset of the signals described in Section 1.2.8.2.5.1. The sending device just needs to convey important signals required to capture the field or frame. It can be shown that various selections of four pins can be used to satisfy all Type 1 conditions.

Three pins, VSYNC, ACTVID, and FID, plus a pixel clock can be used to support discrete sync. VSYNC would bump the capture buffer. An inactive to active level of ACTVID specifies a line of data to capture. FID determines the field ID polarity. The scenario in which the sending device wants the receiving end to capture Vertical Ancillary Data using 4-pin signaling is shown in Figure 1-95.

Figure 1-95. 4-Pin Reduced ACTVID Signaling with Vertical Ancillary Data

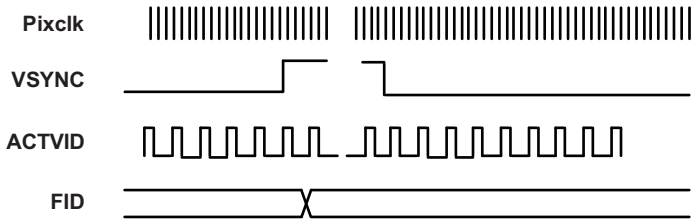
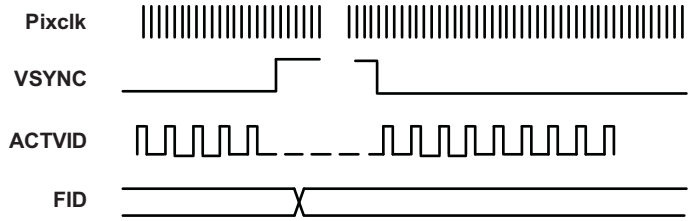


Figure 1-96 describes the case using the 4-pin interface in which the sending device does not send Vertical Ancillary Data.

Figure 1-96. 4-Pin Reduced ACTVID Signaling with No Vertical Ancillary Data

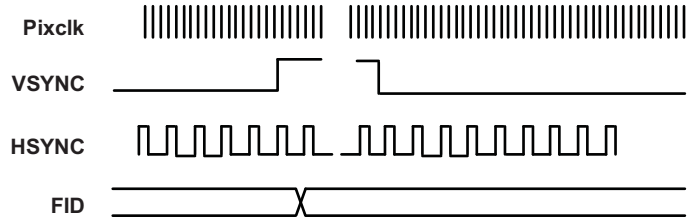


1.2.8.2.5.4 Signal Subsets—4 Pin VSYNC, HSYNC, and FID

In this style of Discrete Sync, as shown in Figure 1-97, four pins are used including the Pixel Clock. HSYNC signals the beginning of the line. All data in the line is captured, including Horizontal Blanking Data. In fact, this signaling mode is the only one that allows Horizontal Blanking Data to be captured.

Of course, by capturing the horizontal blanking pixels in the frame buffers, there is no way to be certain exactly where the blanking ends and the active video starts. One would have to rely solely on video format specs to find the active video inside the frame buffer.

Figure 1-97. 4-Pin Reduced HSYNC Signaling with Vertical Ancillary Data



1.2.8.2.5.5 Vertical Sync

Vertical Sync is used to indicate lines that are in the vertical blanking interval. The VSYNC also separates fields or frames. To be spec compliant, VSYNC should be active for a few lines at the bottom of the picture. The exact number of vertical blanking lines at the bottom depends on the specification for the picture format (480i, 480p, 720p, 1080i, 1080p).

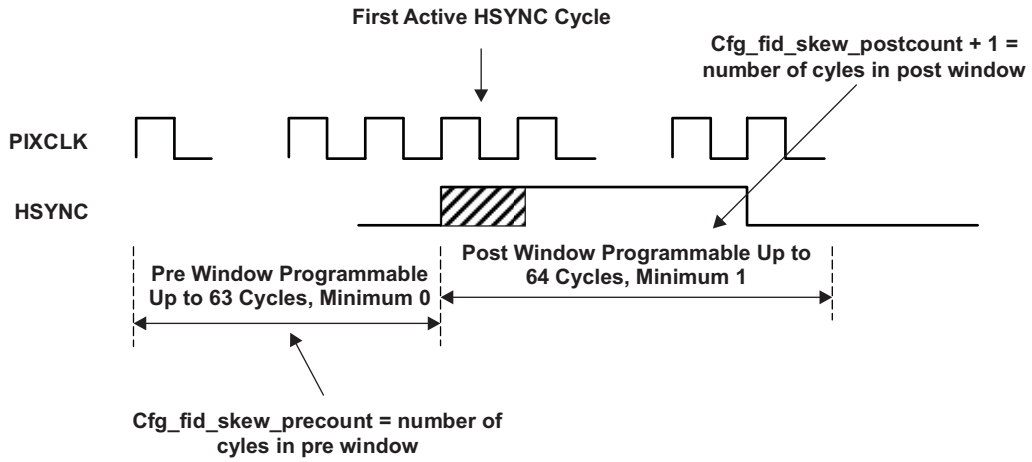
Likewise, the number of vertical blanking lines at the top of the picture depends on the video format specification corresponding to the incoming picture.

In the VIP parser, lines associated with an Active VSYNC are stored in the vertical ancillary data buffers using the ANC VPI port to the VPDMA. Lines without an Active VSYNC are stored in the active video Luma and Chroma-pair buffers using the Y and UV VPI ports, respectively, to the VPDMA.

When using HSYNC signaling instead of ACTVID, the VSYNC signal may be derived from an analog source such as an NTSC/PAL decoder. In this case, VSYNC may not transition on the exact cycle as HSYNC. Thus, the VIP Parser supports a window region around HSYNC in which VSYNC transitions will be detected. A VSYNC transition occurring within the window is identified the same way as if VSYNC transitioned on the same cycle as HSYNC going active.

The window is defined by a pre-window, which is determined by the cfg_fid_skew_precount register. There is also a post-window that is defined by cfg_fid_skew_postcount. Note that although the configuration registers are named fid_skew, they are also used for defining the VSYNC transition window. The window region definition is shown in Figure 1-98.

Figure 1-98. VSYNC Pre and Post Window



The results of VSYNC behavior in the transition window are shown in Figure 1-99. A low to high transition in the window is equivalent to VSYNC going low to high on the active HSYNC cycle.

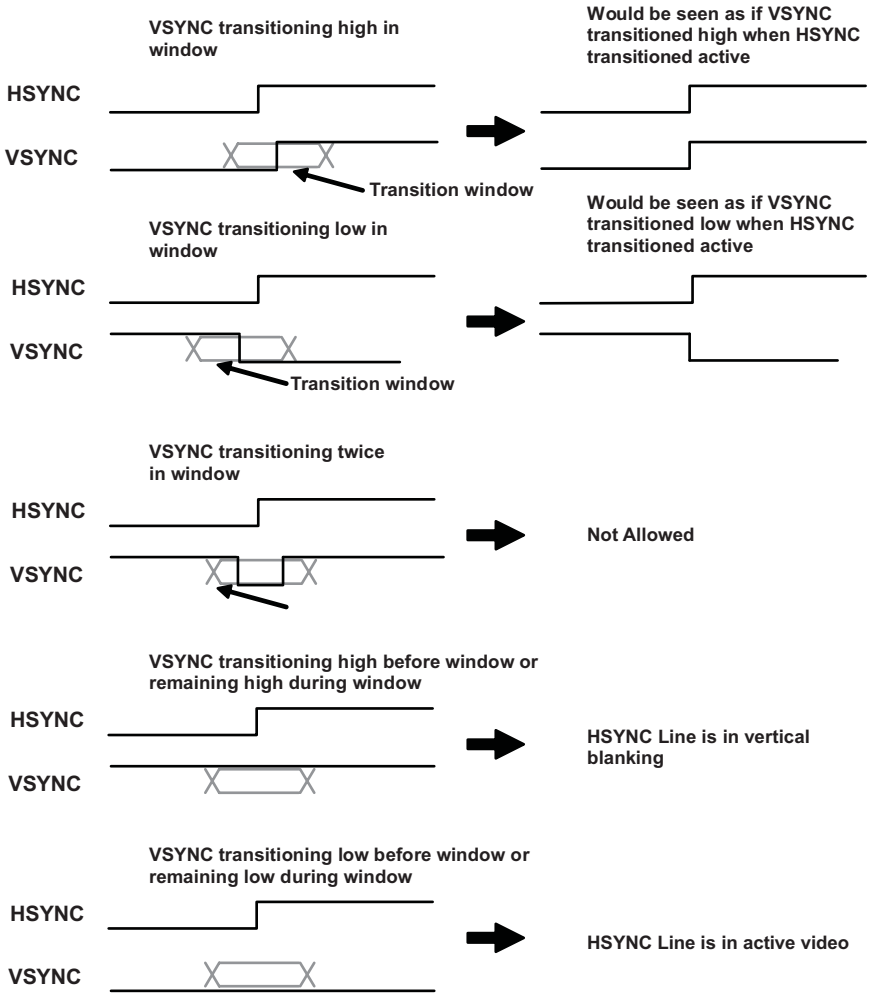
Likewise, a high to low transition in the window is equivalent to VSYNC going high to low on the active HSYNC cycle.

Two transitions of VSYNC within the VSYNC window is not allow and is undefined behavior.

If VSYNC is high throughout the transition window, then the HSYNC line is in vertical blanking.

If VSYNC is low throughout the transition window, then the HSYNC line is in active video.

Figure 1-99. VSYNC Equivalence When Using Transition Window



Note that VSYNC skew generally only applies to input signals that have been sampled from an analog source, as in a NTSC/PAL decoder. If the VSYNC is a VBLANK-type signal or if the sending device is another all-digital IC such as another device or Davinci part, then the VSYNC signal does not have a skew since VSYNC will be aligned to HSYNC. In this case, setting cfg_fid_skew_precount = '0' and cfg_fid_skew_postcount = '0' defines a minimum size window which will capture the value of VSYNC on the same cycle that HSYNC goes active.

1.2.8.2.5.6 Field ID Determination Using Dedicated Signal

For Progressive Source, FIELD ID is always '0.'

For Interlace Source, we need to extract FIELD ID consistently.

In some cases, vertical sync is active on the first pixel of a line in the vertical blanking period and it stays active until the last line in the vertical blanking period.

However, the pixel where the FIELD ID signal transitions can be quite variable and depends on the external chip driving the VIP Parser. Many parts that generate digitized raw video have a programmable feature to specify when FIELD ID changes. From our standpoint, the good news is that FIELD ID is valid at the same point for every field. That is, if FIELD ID is read at one particular place in a field, the polarity of the signal will be reversed at the same location in the next field. So, FIELD ID can be corrected with a programmable polarity configuration bit that is XORed with the captured value.

For discrete sync mode, FIELD ID will be registered on the first active pixel capture cycle of each line in both styles of HSYNC and ACTVID usage as specified in Figure 1-100 and Figure 1-101.

Figure 1-100. FID Registering When Using HSYNC

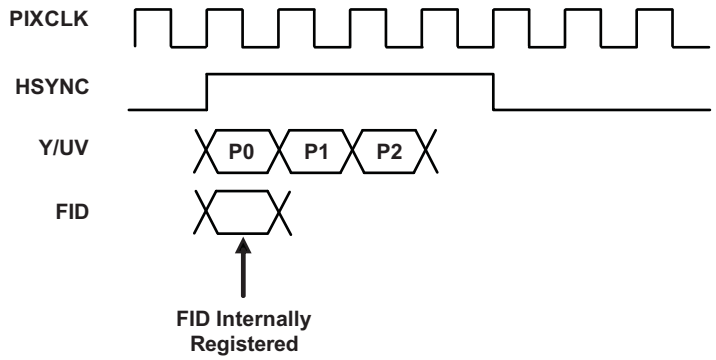
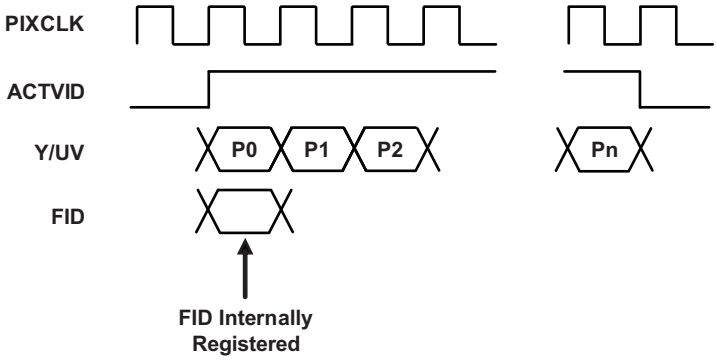


Figure 1-101. FID Registering When Using ACTVID

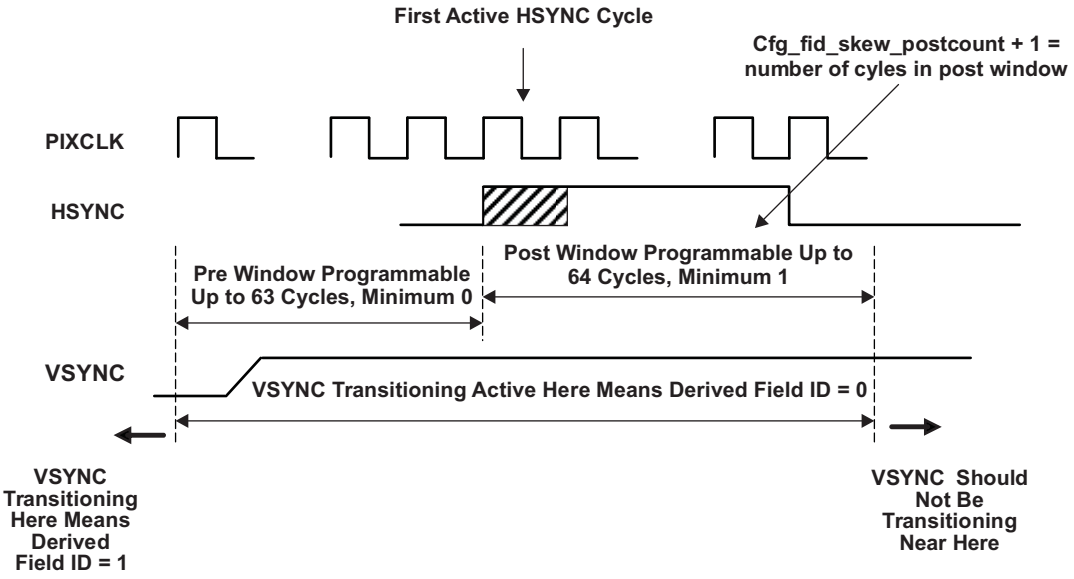


1.2.8.2.5.7 Field ID Determination Using VSYNC Skew

In order to save a device pin, there is a case where a skew may be inserted into VSYNC (with respect to HSYNC) when HSYNC is used as a start of line indicator as described in Figure 1-97. In this case, no FIELD ID signal is sent by the source chip. A description of Field ID determination by VSYNC skew is shown in Figure 1-102.

The active polarity of VSYNC falling within n pixel clock cycles of the first active cycle of HSYNC indicates the field id. If VSYNC is active before this time window, then the field_id = '1' for the next picture. If VSYNC becomes active within this window, then field_id = '0' for the next picture.

Figure 1-102. Field ID Determination By VSYNC Skew



When using FID determination by VSYNC skew, the value for VSYNC is also determined by transitions in the window as shown in Figure 1-99.

The VIP Parser supports a configuration FID polarity bit. For FID determination by VSYNC Skew, the fid determination functions as described in Table 1-54.

Table 1-54. Polarity Table for FID Determination By VSYNC Skew

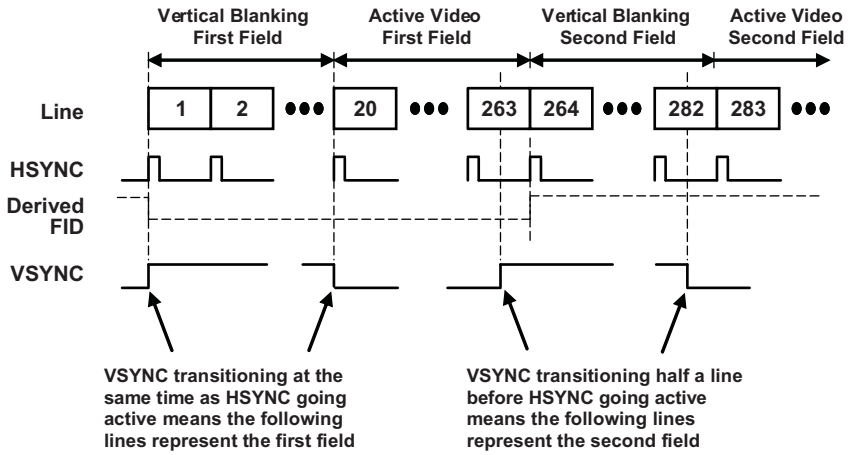
Cfg_fid_polarity	Transition in Pre/Post Range	FID Determination
0	No	1
0	Yes	0
1	No	0
1	Yes	1

1.2.8.2.5.8 Rationale for FID Determination By VSYNC Skew

FID determination by VSYNC skew is a method for field ID determination derived from the analog NTSC and PAL interlaced specifications. Under this method, the sending device will not be providing a FID signal. NTSC has 525 total lines split between two fields. PAL has 625 total lines split between two fields. Each of these interlaced standards support an odd number of lines.

Let's consider just the 525 active line NTSC signal. For the sake of consistency, let's call Line 1 the first line of the 2-field pair and Line 525 the last line of the 2-field pair.

Figure 1-103. Example of 525-line FID Determination By VSYNC Skew



A waveform is shown in Figure 1-103. VSYNC is defined to go active at the same time as HSYNC for the first line of the first field in a two-field picture pair. For this first field, VSYNC will go inactive after Line 20.

For the second field, VSYNC will go active in the middle of Line 263 to signal that Line 264 is the start of a vertical blanking interval. When HSYNC for Line 264 arrives, coinciding with the vertical blanking interval for the beginning of the second field, VSYNC has already been active for half of Line 263. For the second field, VSYNC will go inactive midway through Line 282 to indicate that Line 283 is active video. When HSYNC for Line 283 appears, VSYNC has already been inactive for half a line.

By seeing whether VSYNC transitions at the beginning of a line or whether it transitions at the midway point of a line, one can determine whether the upcoming group of lines represents the first field or the second field. The derived FID is shown in dashed lines.

The analog NTSC specification defines the field ID changing part way into the vertical blanking. That is, the first few lines of vertical blanking belong to the previous field and the next several lines of vertical blanking belong to the upcoming field. The VIP Parser saves one channel of the entire vertical blanking interval between two active video fields into a single buffer. The hardware does not discriminate between whether the vertical blanking lines belong to the bottom of the previous field or those belonging to the start of the next field. This usage model is consistent with vertical ancillary data capture for embedded sync mode of operation.

Obviously, FID Determination by VSYNC skew cannot be used when framing does not use the VSYNC signal but rather relies on the ACTVID signal instead.

1.2.8.2.5.9 ACTVID Framing

Instead of an HSYNC signal, the VIP Parser can use ACTVID framing as described in Figure 1-96. Under ACTVID Framing, VSYNC is used to separate vertical blanking lines from active video lines.

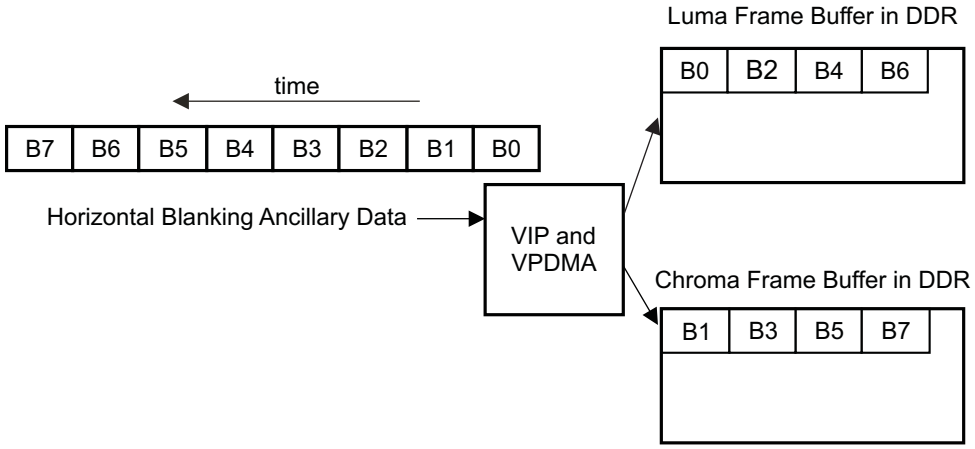
FID determination by VSYNC Skew is not allowed for ACTVID framing because there is no HSYNC input signal in this mode. Also, the VSYNC transition window is not employed. VSYNC is captured at the first pixel of each ACTVID grouping of pixels. Lines are separated by ACTVID transitioning inactive.

1.2.8.2.5.10 Ancillary Data Storage in Descrete Sync Mode

Ancillary data appearing in horizontal blanking is called Horizontal Blanking Ancillary Data. Ancillary Data in vertical blanking is called Vertical Blanking Ancillary Data.

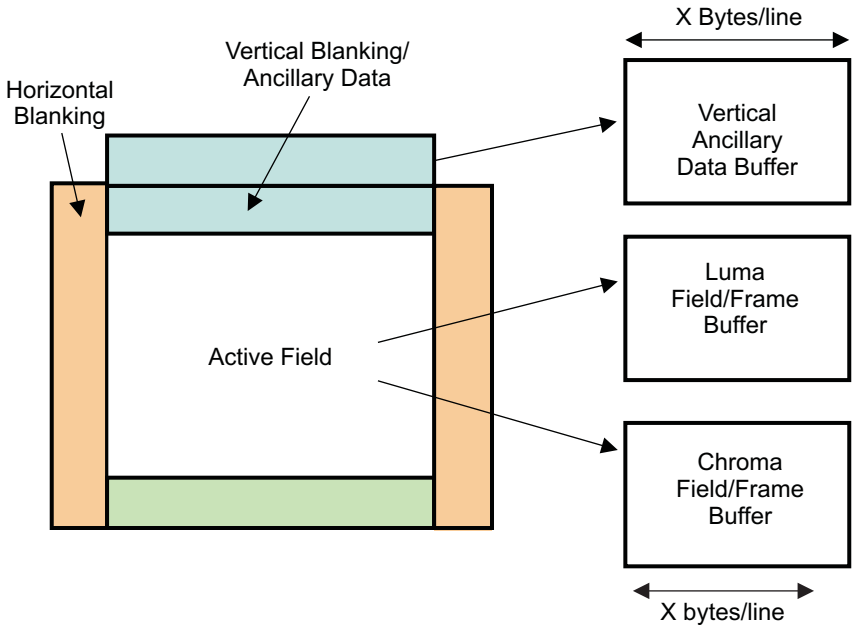
Horizontal Blanking Ancillary Data is not commonly used. For the ACTVID data valid mode described in Figure 1-95, there is no way to capture Horizontal Blanking Ancillary Data. Using the HSYNC mode in Figure 1-97, all blanking pixels are captured. However, the horizontal ancillary data is byte-by-byte distributed between the Luma and Chroma frame buffers. Chroma sited bytes are saved in the Chroma frame buffer and Luma sited bytes are saved in the Luma frame buffer. Some CPU effort would be needed in order to extract ancillary data from the desired Luma or Chroma channel frame buffers. Also, the video on each line starts after the horizontal blanking period. This situation is shown in Figure 1-104.

Figure 1-104. Horizontal Ancillary Data Packing When HSYNC Used as Sync Signal



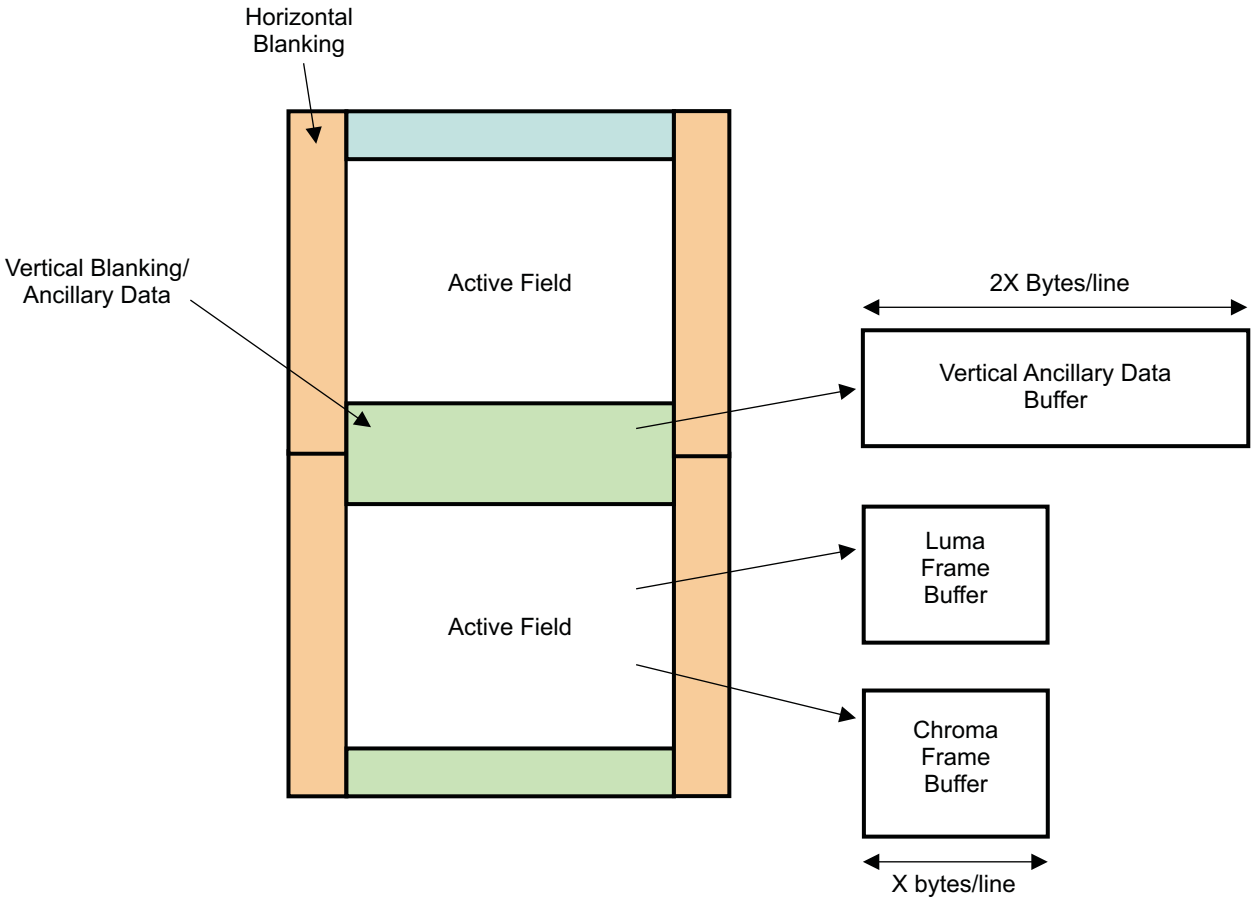
With Interlaced source material, Vertical Blanking Ancillary data will be stored in a separate Vertical Ancillary Data Buffer as shown in Figure 1-105. The Channel from which vertical ancillary data is extracted is a configuration option. For an input image of x active pixels per line, each line of Vertical Blanking Ancillary Data will have x bytes. Unlike the horizontal case, the CPU parsing this Ancillary Data will see a contiguous section of Vertical Ancillary Data that is not intermixed with Video data.

Figure 1-105. Interlaced Field Vertical Blanking Ancillary Data Storage



For Progressive source video, the FIELD ID does not change. So, the Vertical Ancillary Data Buffer will contain all the information beginning from the vertical blanking of the previous frame. This situation is shown in Figure 1-106.

Figure 1-106. Progressive Frame Vertical Blanking Ancillary Data Storage

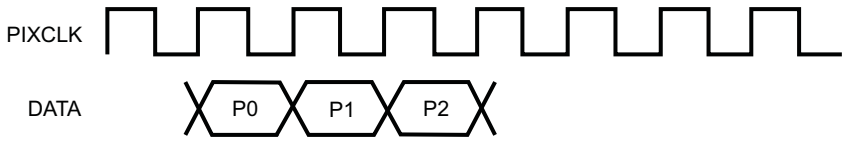


1.2.8.2.6 BT.656 Style Embedded Sync

1.2.8.2.6.1 Data Input

Like Discrete Sync Input, Embedded Sync mode takes data from the 24b input bus. Input data can be 8, 16, or 24 bits wide. A sample is retrieved each and every Pixel Clock cycle. There is no valid signal gating data entry. Figure 1-107 shows a valid data sample each Pixel Clock period.

Figure 1-107. Embedded Sync Data Entry



1.2.8.2.6.2 Sync Words

In embedded sync mode, code words are inserted into the stream at pixel clock rates. For external devices that send out 10 bits (single pixel interface) or 20 bits (parallel Y-Cb/Cr interface) of data, only the 8 (single pixel interface) or 16 (parallel 8bY-8bCb/Cr interface) most significant bits of each pixel are used.

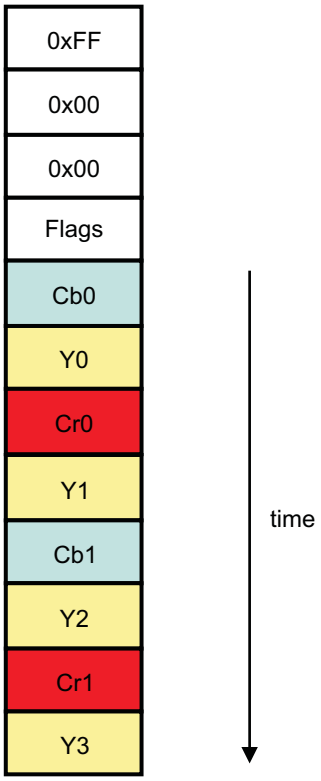
The key code words are Start of Active Video (SAV) and End of Active Video (EAV). Three flags are found in these code words: F (field), V (vertical sync), and H (horizontal sync). These flags signify the position in the frame corresponding to the data immediately following the codeword. The flags determine whether the code is EAV or SAV and where they lie in the picture. The first byte of the code word is 0xFF. The second and third bytes are 0x00. The bit ordering of the fourth byte is detailed in Table 1-55.

Table 1-55. Fourth Byte of EAV/SAV Code Word

7 (fixed)	6 (F)	5 (V)	4 (H)	3 (P3=V^H)	2 (P2=F^H)	1 (P1=F^V)	0 (P0=F^V^H)	Description
1	0	0	0	0	0	0	0	SAV, Field 0, Active Video
1	0	0	1	1	1	0	1	EAV. Field 0, Horizontal Blanking
1	0	1	0	1	0	1	1	SAV, Field 0, Vertical Blanking
1	0	1	1	0	1	1	0	EAV, Field 0, Horizontal Blanking in Vertical Blanking Region
1	1	0	0	0	1	1	1	SAV, Field 1, Active Video
1	1	0	1	1	0	1	0	EAV, Field 1, Horizontal Blanking
1	1	1	0	1	1	0	0	SAV, Field 1, Vertical Blanking
1	1	1	1	0	0	0	1	EAV, Field 1, Horizontal Blanking in Vertical Blanking Region

An example of the input ordering of the embedded code word, followed by active video, is shown in Figure 1-108. The input data mode is 8 bits for the example.

Figure 1-108. Code Word Format Example Followed by Video Data



1.2.8.2.6.3 Error Correction

The FVH flags are sent with four protection bits to support double error detection, single error correction. A non-correctable detected error is simply ignored. An option exists for the protection bits to correct a single bit error in the FVH flags. The correction table is shown in Table 1-56. n/c means that the error condition is detected, but it is non-correctable.

Table 1-56. Error Correction Matrix

P3, P2, P1, P0	F, V, and H Flags							
	000	001	010	011	100	101	110	111
0000	000	000	000	n/c	000	n/c	n/c	111
0001	000	n/c	n/c	111	n/c	111	111	111
0010	000	n/c	n/c	011	n/c	101	n/c	n/c
0011	n/c	n/c	010	n/c	100	n/c	n/c	111
0100	000	n/c	n/c	011	n/c	n/c	110	n/c
0101	n/c	001	n/c	n/c	100	n/c	n/c	111
0110	n/c	011	011	011	100	n/c	n/c	011
0111	100	n/c	n/c	011	100	100	100	n/c
1000	000	n/c	n/c	n/c	n/c	101	110	n/c
1001	n/c	001	010	n/c	n/c	n/c	n/c	111
1010	n/c	101	010	n/c	101	101	n/c	101
1011	010	n/c	010	010	n/c	101	010	n/c
1100	n/c	001	110	n/c	110	n/c	110	110
1101	001	001	n/c	001	n/c	001	110	n/c
1110	n/c	n/c	n/c	011	n/c	101	110	n/c
1111	n/c	001	010	n/c	100	n/c	n/c	n/c

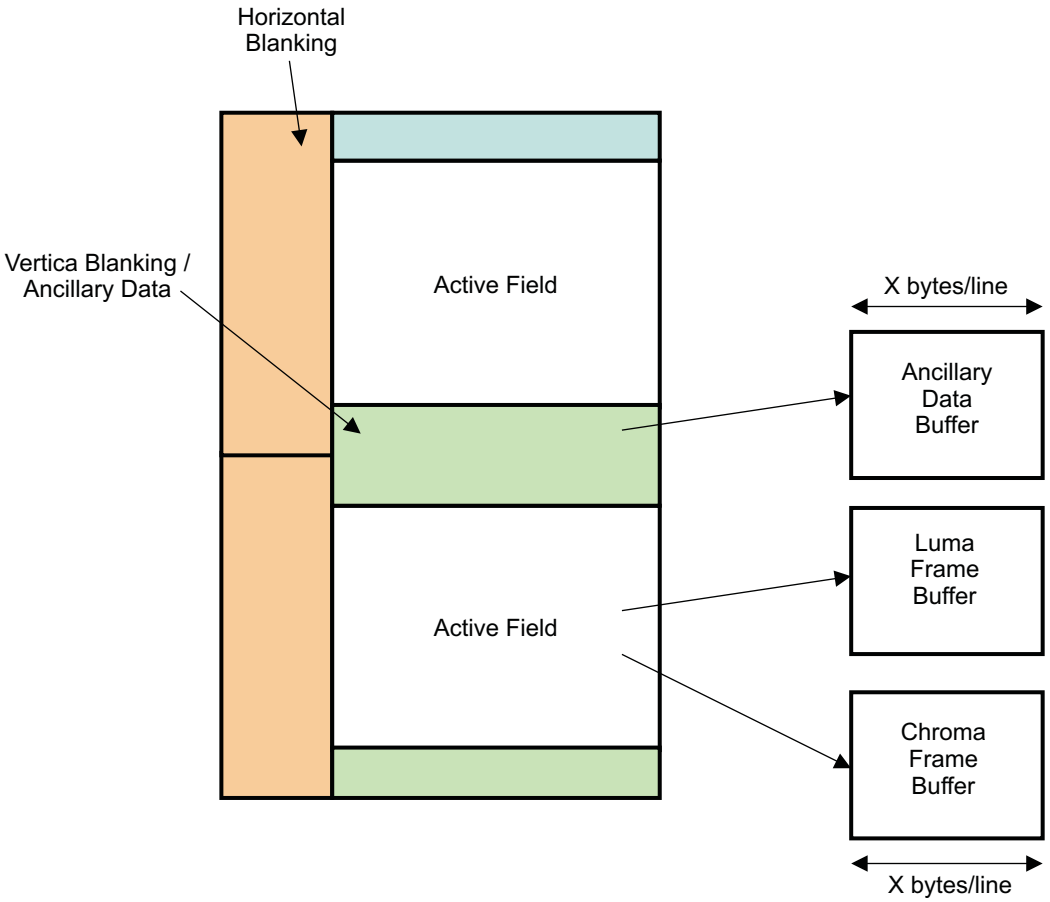
1.2.8.2.6.4 Embedded Sync Ancillary Data

With Embedded Sync streams, only Vertical Ancillary Data can be extracted. The Vertical Ancillary Data buffer is the same width as the corresponding Luma and Chroma buffers. The channel from which Vertical Ancillary Data is extracted is a configuration option.

Horizontal Ancillary data cannot be extracted using embedded sync mode.

The Vertical Ancillary Data is captured starting from the end of the previous active video. See Figure 1-109 for a more detailed description of embedded sync packing.

Figure 1-109. Embedded Sync Packing

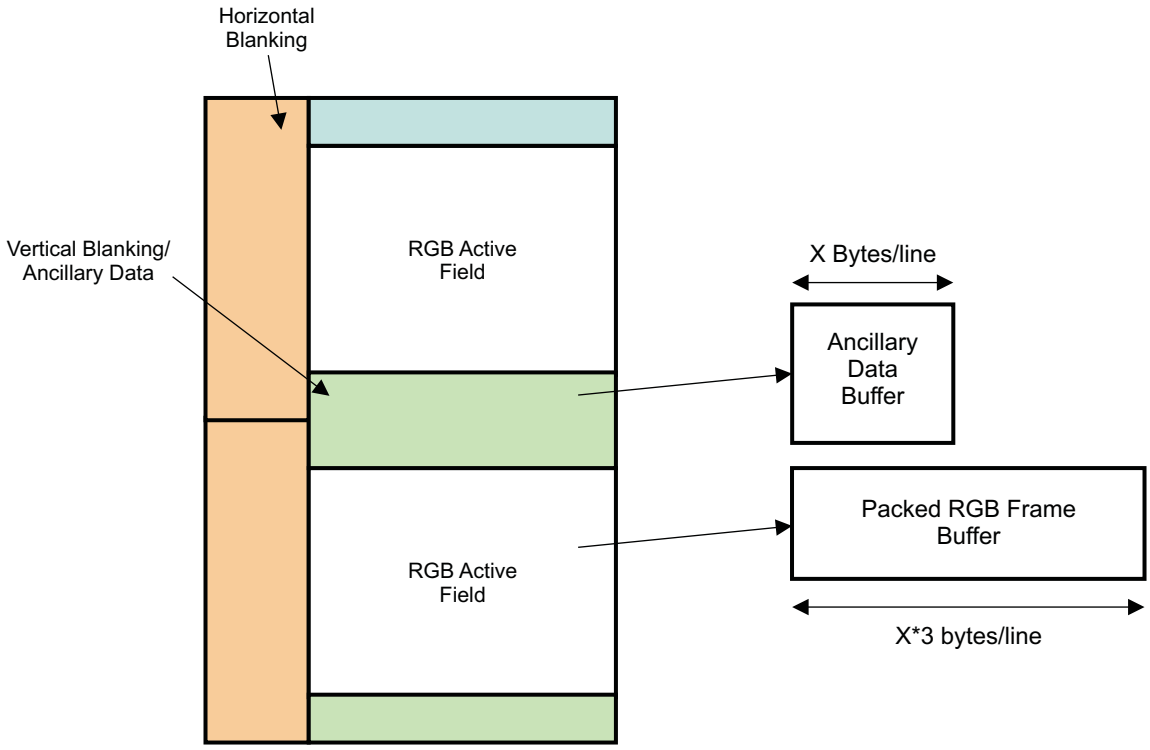


1.2.8.2.6.5 Embedded Sync RGB 24-bit Data

YUV streams are separated into a planar Luma buffer, a planar Chroma Pair (CbCr) buffer, and a planar Vertical Ancillary Data buffer. RGB streams, on the other hand, are stored in a packed R-G-B format, as shown in Figure 1-110.

The BT.1120 standard defines a method of carrying RGB streams. After the SAV code, 8 bits of R, 8 bits of G, and 8 bits of B data are clocked in one cycle. A 24 bit data bus is required. The channel in which to search for the embedded sync codes and the FVH control code is determined by a configuration selection. Only vertical ancillary data from one channel (R, G, or B), which happens to be the channel where control codes are found, are captured. Vertical ancillary data in the other two channels are ignored.

Figure 1-110. RGB Frame Storage



1.2.8.2.7 Source Multiplexing

1.2.8.2.7.1 Multiplexing Scenarios

Some applications require multiple camera sources to be used at the same time. For example, video surveillance systems can record and display multiple camera sources. For this type of device, one solution would be to support N 8b or 16b data interfaces for each of N cameras. However, this solution does not efficiently minimize pin count. One set of 8b or 16b interfaces has the bandwidth to support more than one video source, depending on the resolution of the video. Table 1-57 is explanatory only and shows the number of sources that can be multiplexed in one VIP for 8b and 16b interface modes. Note that it does not reflect the capabilities of the VIP Parser design. In addition, the interface pixel clock rates are shown. The VPDMA limits 16 camera sources to be saved to DDR per Pixel Clock Input Domain.

Table 1-57. Multiplexing Configurations and Pixel Clock Rates

	Max Channels In Single 16b Data Interface Mode	Max Channels In Dual 8b Data Interface Mode - Interleaved Channels per Single 8b Port. One 16b VIP can be configured to support two such 8b ports.	Interface Clock Rate (MHz)
HD Interlaced	2	1	148.5
D1 Interlaced	8	4	108.1
CIF Interlaced	n/a	n/a	n/a
HD Progressive	1	n/a	148.5
D1 Progressive	4	2	108.1
CIF Progressive (1)	32	16	162.2

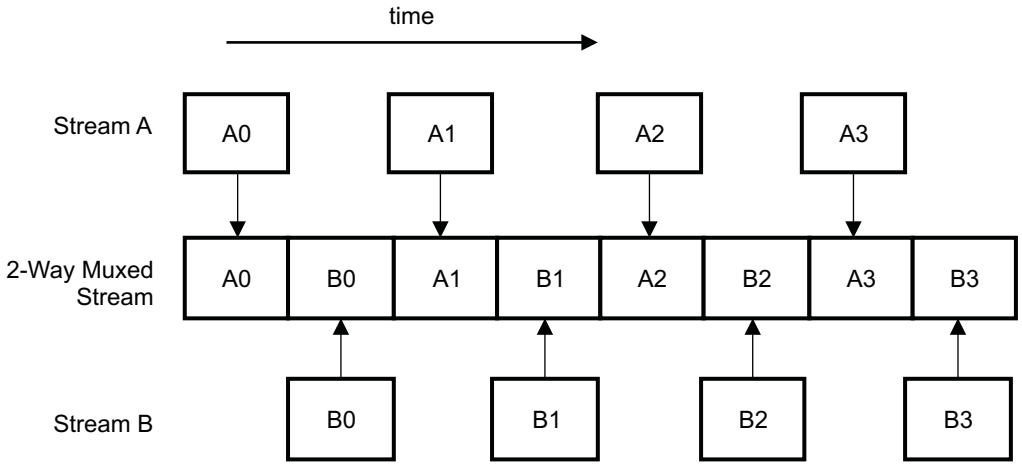
(1) Blanking pixels are not used in the CIF clock rate calculations. Addition of blanking pixels would require a slightly higher clock rate.

NOTE: These Channel Density values reflect 1 VIP subsystem.

1.2.8.2.7.2 2-Way Multiplexing

For 2-Way Multiplexing, two embedded sync streams are interleaved a pixel at a time as shown in Figure 1-111.

Figure 1-111. 2-Way Multiplexing



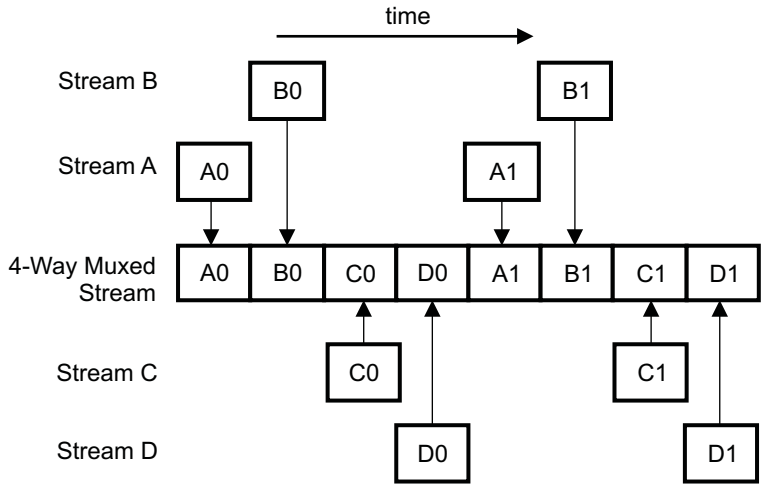
The sync codeword, FF-00-00-XY, is replicated in both source streams. In 2-Way Multiplexing, the sizes of both camera sources must be the same. Likewise, the Vertical Ancillary Data size for both sources must be identical. However, the two streams are not necessarily sending the same pixel site in adjacent clock cycles.

1.2.8.2.7.3 4-Way Multiplexing

For 4-Way Multiplexing, four embedded sync streams are multiplexed into one as seen in Figure 1-112.

Again, the sync codeword is in all four sources. Like 2-Way Multiplexing, the sizes of the four camera sources are the same and the sizes of the Vertical Ancillary Data regions are the same. The four streams are not necessarily sending the same pixel site in adjacent clock cycles.

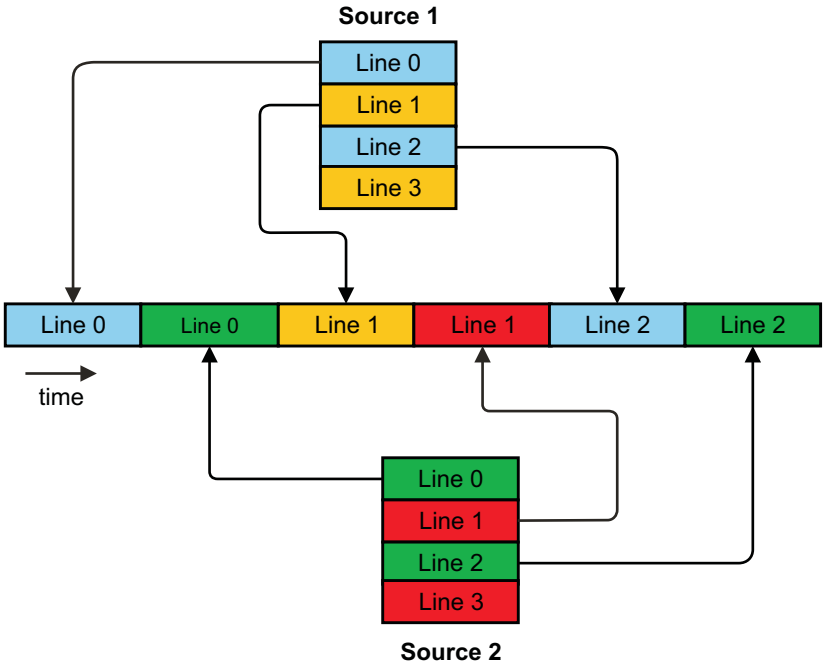
Figure 1-112. Example of 4-Way Multiplexing



1.2.8.2.7.4 Line Multiplexing

In Line Multiplexing, n-different sources are sent into the VIP a complete line at a time using a modified version of embedded sync. An example of Line Multiplexing for two sources is shown in Figure 1-113.

Figure 1-113. Example of Line Multiplexing



The width and height of each source in Line Multiplexed data can be different. For instance, one source can be PAL while another one can be NTSC. A line is comprised of YUV422 pixels in repeating patterns of CbYCrY.

1.2.8.2.7.5 Super Frame Concept in Line Multiplexing

Older TI DSPs do not natively support Line Multiplexing, which is thus far proprietary to the TVP5158 video decoder. When connected to older DSPs, the CPU must parse through the pixel data and in order to create frame buffers. Hence, the '5158 team came up with the concept of a super frame. Different camera sources are interleaved on a line-by-line basis. The beginning of each line carries a Metadata tag that provides key information about that line.

This Metadata tag is preceded by a SAV codeword in which F=0, V=0, and H=0. In other words, the older DSPs would see this line as a normal active video line.

At the end of the line, an EAV code is inserted with an appropriate number of padding pixels following it. This EAV code has F=0, V=0, and H=1.

In older DSPs, a set of like sized buffers are defined to store raw video frames. When a line's V bit changes, the current buffer is closed and an interrupt is given to the CPU. An empty buffer is used to store the incoming line's pixels. With the 5158's SAVs and EAVs having the V flag always set to 0, the older DSPs would never advance their buffer pointer.

Hence, there is a dummy vertical blanking line. The external device would insert an artificial vertical blanking line with a SAV having F=0, V=1, and H=0. It also inserts a dummy EAV with F=0, V=1, and H=1. This dummy line causes the older DSPs to change input buffer and signals the CPU to parse the captured data and build frame buffers.

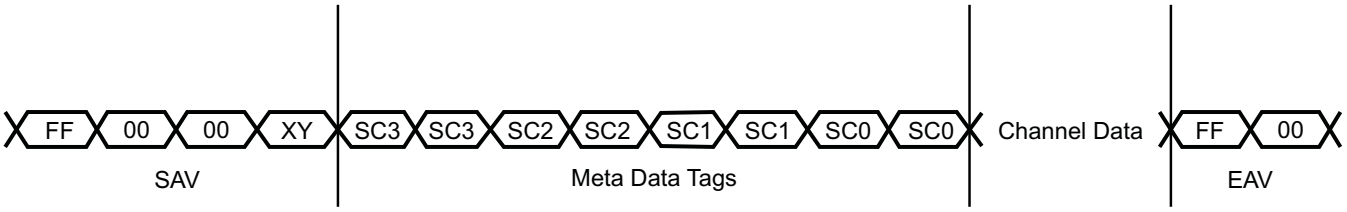
The startcodes used for the Metadata wrapped lines and the dummy lines form the Super Frame.

The dss_vip_parser has logic to parse out the super frame, analyze the Metadata tags, and frame buffer the line contents appropriately.

1.2.8.2.7.6 8-bit Data Interface in Line Multiplexing

Figure 1-114 is an example of an 8-bit line multiplexing interface. Channel Data is the CbYCrY sequence representing a line. Preceding Channel Data is the four byte Meta Data tags. Note that the Meta Data bytes are replicated in both the Luma and the Chroma sites. The entire structure is bounded by a traditional SAV/EAV code in which the V flag is 0.

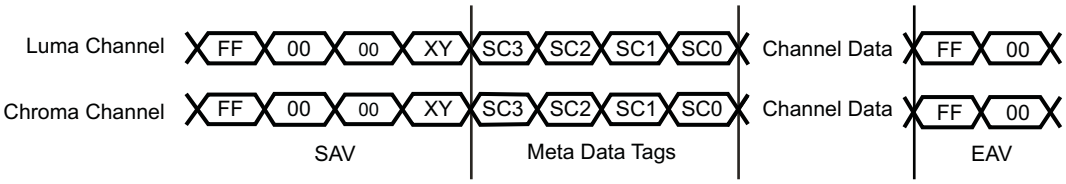
Figure 1-114. 8-bit Line Mux Interface



1.2.8.2.7.7 16-bit Data Interface in Line Multiplexing

Figure 1-115 describes the 16-bit line multiplexing interface. Channel Data is the active line. All the Y pixels are in the Luma Channel. The CbCr pixels are in the Chroma Channel. Each cycle, a 16 bit value representing one Luma sample and one Chroma sample enters the VIP Parser. The Meta Data tags are replicated in both channels. Likewise, the SAV/EAV startcodes are found in both channels. The V flags for the SAV/EAV startcodes are always 0.

Figure 1-115. 16-bit Line Mux Interface



1.2.8.2.7.8 Split Lines in Line Multiplex Mode

Suppose an external device is sending two dissimilar sources in Line Multiplex mode. One narrower source has X pixels per line. The wider source has 2X pixels per line. In an older DSP, the capture buffer for the Super Frame must be configured to be the width of the largest incoming line. So, lines from the narrower source would take up only half of the allocated space in the capture buffer resulting in wasted DDR memory space.

The Meta Data has provisions for the external device to split a line. The Beginning of Line (BOL) and End of Line (EOL) flags tag a split line as described in Table 1-58.

Table 1-58. Split Line Table

BOL	EOL	Function
0	0	Undefined
0	1	Line Segment is the second half of a line
1	0	Line Segment is the first half of a line
1	1	Line has not been segmented into two.

1.2.8.2.7.9 Meta Data

Table 1-59 shows the bitfields in the Meta Data start codes.

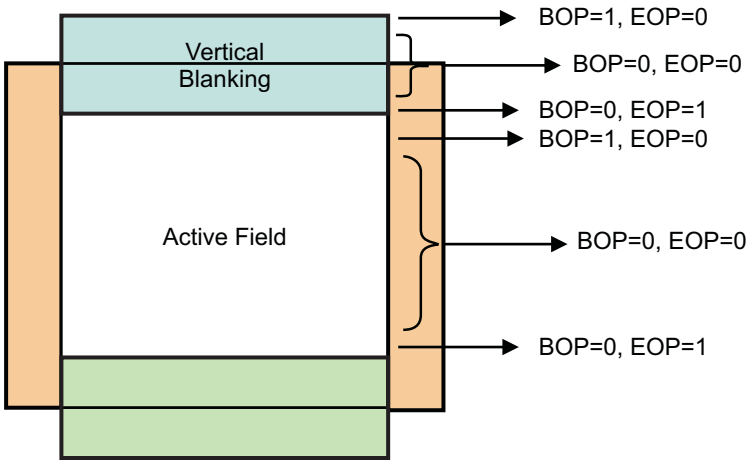
Table 1-59. Meta Data Layout

Byte	7	6	5	4	3	2	1	0
SC3	1	BOP	EOP	RSVD	CH_ID[3:0]			
SC3	1	BOP	EOP	RSVD	CH_ID[3:0]			
SC2	0	BOL	EOL	VDET	LINE_ID[10:7]			
SC1	~LINE_ID[6]	LINE_ID[6:0]						
SC0	PAD	F	V	H	P3	P2	P1	P0

BOP tags the line as a startline in a period. A period is defined as the contiguous lines in a vertical blanking period or the contiguous lines in a field or frame. For the vertical blanking period case, the vertical blanking at the bottom of the previous field or frame combined with the vertical blanking at the top of the current field or frame is combined to create one period.

EOP tags the line as an endline in a period. Figure 1-116 shows the definition of the two types of Periods as outlined by BOP and EOP.

Figure 1-116. BOP/EOP Definition of a Period



For the Split Line at the top of a Period, the BOP bit is set for both halves of the split line. Likewise, for the Split Line at the bottom of a Period, the EOP bit is set for both halves of the split line.

CH_ID is the channel ID, which tags the camera source that generated the incoming line. A maximum of 16 camera sources are support per Pixel Input Clock Domain.

LINE_ID is the line number, starting from 0 and incrementing by one for each subsequent line from the same source. The TVP5158 only supports SD sources or smaller, so only 9 bits of the line ID (bits 8:7) will be used by this external device.

PAD is a flag which tags the line as an artificially inserted padding line. When PAD is '0', the line should be discarded.

F, V, H, P3, P2, P1, and P0 are the bits representing the normal XY code. F is the Field ID associated with line, V signals when the line is in the vertical blanking, H specifies that the line is in the Horizontal Blanking, and P3:P0 are the protection bits.

Since only active video and vertical ancillary data lines are encapsulated in the Meta Data, the H bit in the SC0 byte should never be '1'.

1.2.8.2.7.10 TI Line Mux Mode, Split Lines, and Channel ID Remapping

The VIP Parser supports a maximum of 8 different Channel IDs per Port. The Channel IDs must be in the range {0:7} (3 bits). In the source multiplex, only one source can be a split line source and have the same Channel ID as one of the non-split line sources.

This scenario involves an external NTSC decoder which supports 8 D1 cameras. The external NTSC decoder will downscale the 8 sources to SIF format. However, one camera source will be sent in the multiplex as both the downscaled version and the original D1 sized version. They will both have the same Channel ID. However, the D1 version will be sent as a split-line. The source multiplex will thus have 9 maximum streams.

The dss_vip_parser, for TI Line Mux Mode only, will left shift the Channel ID by one. Bit 0 is used as an indicator whether the Source is a split-line source or a normal non-split line source. Only one of the nine inputs can be a split line source.

Table 1-60. TI Line Mux Mode Channel ID Remapping

Source Input Channel ID	Channel ID Sent to VPDMA	
	Non-split Line	Split Line
0x0	0x0	0x1
0x1	0x2	0x3
0x2	0x4	0x5
0x3	0x6	0x7
0x4	0x8	0x9
0x5	0xA	0xB
0x6	0xC	0xD
0x7	0xE	0xF

All subsequent references to the Camera Source, such as in a VPDMA return descriptor, will reference the remapped Channel ID.

The SrcIDx size status registers and the Source FID status registers reflect the remapped Channel ID when the port is in TI Line Mux mode.

1.2.8.2.8 Channel ID Extraction for 2x/4x Multiplexed Source

1.2.8.2.8.1 Channel ID Extraction Overview

For 2-way and 4-way multiplexed source, the Channel ID is either embedded in the four protection bits inside the EAV/SAV code words or in the horizontal blanking pixel data. A configuration setting determines where the VIP Parser would search for the Channel ID.

1.2.8.2.8.2 Channel ID Embedded in Protection Bits for 2- and 4-Way Multiplexing

The four-bit channel ID is an identifier corresponding with the source number (camera) of the incoming video. As shown in Table 1-61, the Channel ID is placed in the code fourth byte of the EAV/SAV code words normally used for protection bits. With 4 bits, the maximum number of sources that can be defined in this range is 16. However, only Channel IDs in the range {0:7} are supported. Obviously, error correction cannot be performed on the FVH flags since the protection bits are no longer there.

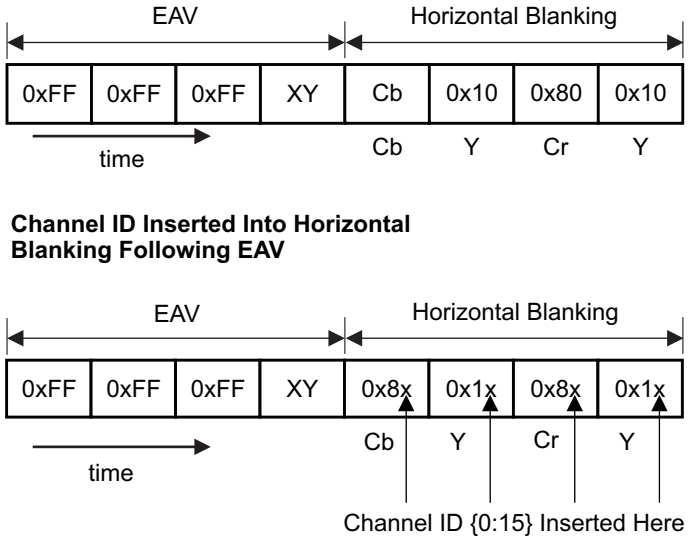
Table 1-61. Channel ID Embedded in EAV/SAV

7 (fixed)	6 (F)	5 (V)	4 (H)	3 (ch_id[3])	2 (ch_id[2])	1 (ch_id[1])	0 (ch_id[0])	Description
1	0	0	0	Ch_id = {0:15}				SAV, Field 0, Active Video
1	0	0	1	Ch_id = {0:15}				EAV, Field 0, Horizontal Blanking
1	0	1	0	Ch_id = {0:15}				SAV, Field 0, Vertical Blanking
1	0	1	1	Ch_id = {0:15}				EAV, Field 0, Horizontal Blanking in Vertical Blanking Region
1	1	0	0	Ch_id = {0:15}				SAV, Field 1, Active Video
1	1	0	1	Ch_id = {0:15}				EAV, Field 1, Horizontal Blanking
1	1	1	0	Ch_id = {0:15}				SAV, Field 1, Vertical Blanking
1	1	1	1	Ch_id = {0:15}				EAV, Field 1, Horizontal Blanking in Vertical Blanking Region

1.2.8.2.8.3 Channel ID Embedded in Horizontal Blanking Pixel Data for 2- and 4-Way Multiplexing

In Horizontal Blanking and Vertical Blanking, non-ancillary data pixels should be Y=0x10 and Cb=Cr=0x80. When the Channel ID is embedded in the Horizontal Blanking for 2 and 4-way multiplexing, the lower nibbles of all Luma and Chroma pixels are replaced by the 4 bit Channel ID. This scenario is shown in Figure 1-117. The maximum number of values defined by this 4-bit range is $2^4 = 16$. However, only Channel IDs in the range {0:7} are supported.

Figure 1-117. Channel ID Inserted Into Horizontal Blanking



1.2.8.2.9 Embedded Sync Mux Modes and Data Bus Widths

Legal combinations of Embedded Sync Mux Modes and Data Bus Widths are described in Table 1-62.

Table 1-62. Valid Embedded Sync Mux Mode and Data Bus Width Combinations

	1x Mux	2x Mux	4x Mux	Line Mux
8 Bit	√	√	√	√
16 Bit	√	n/a	n/a	√
24 Bit	√	n/a	n/a	n/a

1.2.8.2.10 Interrupts

The VIP parser provides one interrupt line to the HDVPSS. The source for this interrupt can be one or more of 22 events.

When an interrupt occurs and is determined to be from the VIP parser, VIP parser level of masks, clears, and status registers must be checked and updated first.

The VIP Parser Interrupt Mask, Interrupt Clear, and Interrupt Status register layout is shown in Table 1-63.

Table 1-63. Register Layout

21	20	19	18	17	16	15	14	13	12	11
PrtB Disable Comple	PrtA Disable Complete	PrtB Anc ProtoVio	PrtB YUV ProtoVio	PrtA Anc ProtoVio	PrtA YUV ProtoVio	PrtB Src0Size	PrtA Src0Size	PrtB DisConn	PrtB Conn	PrtA Disconn
10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PrtA Conn	OpPrtB Anc		OpPrtB YUV	OpPrtA Anc		OpPrtA YUV	InPrtB	InPrtA	PrtB Vdet	PrtAV det

Table 1-64 describes each of the interrupts supported by the VIP Parser.

Table 1-64. VIP Parser Interrupts

Interrupt	Description
PrtBDisableComplete	When Port B is disabled in the middle of the frame, this interrupt is activated when complete frame is sent out of Port B following disable.
PrtADisableComplete	When Port A is disabled in the middle of the frame, this interrupt is activated when complete frame is sent out of Port A following disable.
PrtBANCProtocolVio	This interrupt is enabled when the protocol checker on the output of the dss_vip_parser encounters a violation on the Ancillary VPI of Port B.
PrtBYUVProtocolVio	This interrupt is enabled when the protocol checker on the output of the dss_vip_parser encounters a violation on the Active Video VPI of Port B.
PrtAANCProtocolVio	This interrupt is enabled when the protocol checker on the output of the dss_vip_parser encounters a violation on the Ancillary VPI of Port A.
PrtAYUVProtocolVio	This interrupt is enabled when the protocol checker on the output of the dss_vip_parser encounters a violation on the Active Video VPI of Port A.
PrtBSrc0Size	The output size for Srcnum=0 on Port B differs from the SRC0_NUMLINES and SRC0_NUMPIX register settings
PrtASrc0Size	The output size for Srcnum=0 on Port A differs from the SRC0_NUMLINES and SRC0_NUMPIX register settings
PrtBDisConn	Port B Link Disconnect for Srcnum 0
PrtBConn	Port B Link Connect for Srcnum 0
PrtADisConn	Port A Link Disconnect for Srcnum 0
PrtAConn	Port A Link Connect for Srcnum 0
OpPrtBAnc	Overflow at Ancillary Data VPDMA interface for the Port B
OpPrtBYUV	Overflow at Luma VPDMA interface for Port B
OpPrtAAnc	Overflow at Ancillary Data VPDMA interface for the Port A
OpPrtAYUV	Overflow at Luma VPDMA interface for Port A
InPrtB	Overflow at Input Async FIFO for Port B
InPrtA	Overflow at Input Async FIFO for Port A
PrtBVdet	Video Detect Interrupt for Port B
PrtAVdet	Video Detect Interrupt for Port A

- A ‘1’ in the Status register associated with an Interrupt source shows that the interrupt source is pending. The Status register is read-only. To clear a bit in the Status register, the associated bit in the Clear register must be written with a ‘1.’
- A ’1’ the bit position of the Mask register associated with an Interrupt source ensures that the hardware interrupt will never be passed on to the DSS interrupt controller. A ‘0’ in the bit position of the Mask register associated with an Interrupt source will cause the DSS interrupt controller to see a VIP Parser interrupt in the event the hardware in the parser triggers it.
- A ‘1’ in the bit position of the Clear register associated with an Interrupt source clears the hardware interrupt status register until the next time the hardware triggers it. After a Clear, the CPU should set the bit back to a ‘0.’ Otherwise, the hardware would not be able to set any subsequent interrupts of the same type.

1.2.8.2.11 VDET Interrupt

For Line Multiplexing Embedded Sync mode only, the Meta Data Header includes a Video Detect (VDET) flag. The TVP5158 sets this VDET flag whenever NTSC or PAL sync is found. Some other external devices using Line Multiplexing mode may not use VDET. However, when VDET changes, a VDET interrupt is issued to the DSS interrupt controller. Each Pixel Clock Input Domain has a separate VDET interrupt.

The VDET status register is comprised of 32 bits, each bit representing the value of the VDET flag found in the Meta Data of the Channel ID. Bit 0 is the VDET value from Channel ID 0, Bit 1is is VDET value from Channel ID 1, etc. There is a separate status register for each Pixel Input Clock Domain.

In Line Mux mode, the meta-data field defining the srcnum is 5 bits wide. The TVP5158 spec only defines the last three bits of this field and the upper two bits are reserved. When set to ‘1’, the cfg_tvp5158_chan_id_type register tells the VIP Parser to ignore the top two bits of the field any only use the lower three bits, giving a maximum of eight srcnums. This bit should always be set to '1' in TI Line Mux mode.

1.2.8.2.12 Source Video Size

These status registers provide the size of the last active video frame in 16 different input sources per port. There is no interrupt activated on the change in the source size in any of the input sources. These read-only registers only inform the application of the width and the height of the last active field or frame associated with each channel ID.

1.2.8.2.13 Clipping

The source for the clipping feature can be either embedded sync or discrete sync. Embedded sync streams use 2 reserved codewords as sync codes, 0x00 and 0xFF. These sync codes define different regions in the incoming data. Discrete sync streams have no limitation on the allowed quantization values. All 8 bits, from 0x00 to 0xFF are legal quantization values.

Suppose the input is discrete sync and the device converts the discrete sync raw video into a embedded sync stream (by adding appropriate embedded sync headers) and stores it on the network or hard disk. In this case, the processor checks every raw video byte to ensure that the reserved 0x00 and 0xFF codewords are not used in the raw video before the stream is saved. Otherwise, when the stored stream is read back by some device as an embedded sync stream, illegal codes are found.

The hardware has the capability to clip illegal codewords into legal ones. This clipping is only needed for discrete sync sourced inputs to the HDVPSS VIP module.

Embedded sync sourced input streams do not need to be clipped as they are presumably already following the rules for embedded sync.

For the embedded sync interface, input values 0x00 and 0xFF are reserved for the sync detection, so these values cannot be used in the rest of the system. The VIP Parser supports one configuration bit that, when enabled, changes all 0x00 to 0x01 and 0xFF to 0xFE in the vertical ancillary data. Another configuration bit, when enabled, changes all 0x00 to 0x01 and 0xFF to 0xFE in the active video portion of the input picture.

Note that if the clipping is enabled for ancillary data, the post processing software will never be able to find a data packet sync header, since the 00-FF-FF sequence will be changed to 01-FE-FE.

For 24- bit YUV, clipping is done on each 8 bit channel. If data[23:16]==0xFF, the clipped value will be 0xFE. If data[23:16]==0x00, the clipped value will be 0x01. Likewise, clipping is done for data bit ranges 15:8 and 7:0

1.2.8.2.14 Current and Last FID Value

The FID values for the current field or frame are reported in the Status Registers. When a new field or frame enters, the current FID values are saved into the previous FID status registers and the new FID value is loaded into the current FID register

Following a reset, the previous and current FID status registers are set to '1.' The first two fields or frames are ignored. On the third input field or frame after a reset, the previous FID is loaded with the current FID ('1'), and the current FID is loaded with the actual FID. By the fourth field or frame after a reset, both the previous and current FID values should represent the values found in the input stream.

The FID values are reported for each camera source in both Pixel Input Clock Domains.

1.2.8.2.15 Disable Handling

When the VIP port is used in single-channel embedded or discrete sync interface, output of the VIP can be connected to the scalar or other modules. When connected with these modules, it may be required to work on frame boundary or it may cause lock up without reset. This feature makes sure that VIP is always disabled at the frame boundary.

In a scenario, assume that the VIP Parser has been processing a single input stream. Then, VIP port is disabled by setting ENABLE to '0'. The VIP Parser will continue to output data downstream until it sends out an end frame pixel and the downstream module accepts the end frame pixel.

1.2.8.2.16 Picture Size Interrupt

Each VIP port can be set up to trigger an interrupt if the picture size varies from a pre-programmed expected picture size. This interrupt is supported only for the Active Video portion of the input video and not for the Vertical Ancillary portion. Also this interrupt is only support for source number 0 in multi channel capture.

The interrupts are named PrtASrc0Size and PrtBSrc0Size. They are described in Table 1-64.

For Port A, the expected active video picture size values are programmed in SRC0_NUMLINES and SRC0_NUMPIX in the VIP_PARSER_xtra_port_a register. For Port B, the expected active video picture size values are programmed in SRC0_NUMLINES and SRC0_NUMPIX in VIP_PARSER_xtra_port_b register.

Note that the Picture Size Interrupt reflects the Active Video size going out of the VIP port. If cropping is enabled for Srcnum=0, the Picture Size is the post-cropped size.

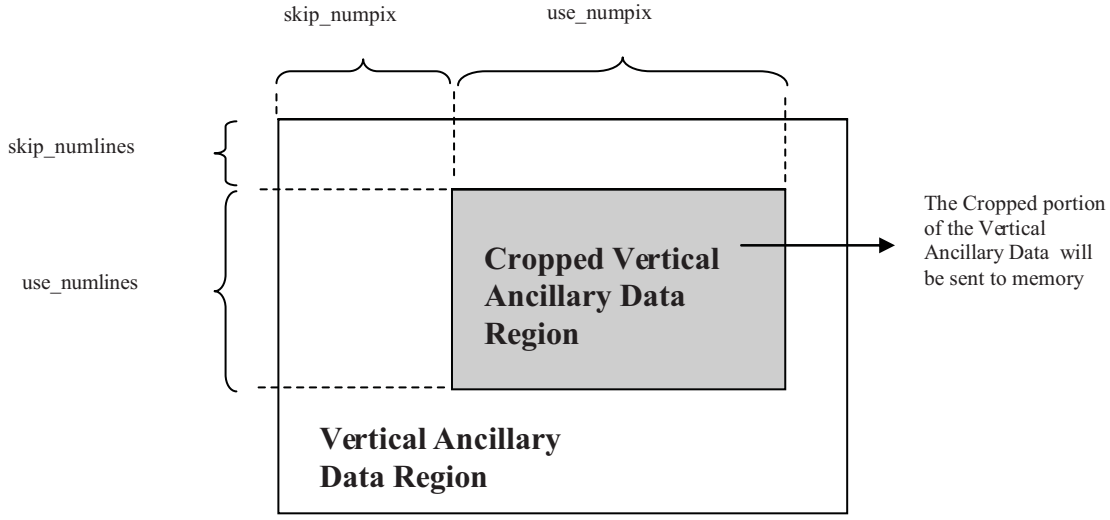
1.2.8.2.17 Ancillary and Video Data Cropping

Each VIP port supports cropping of video and ancillary data. The size of the cropping window for video and ancillary data can be configured independently. This feature is supported for only one source number in a VIP port.

For the Vertical Ancillary Data from Port A, cropping is enabled by setting the ANC_BYPASS_N bit in VIP_PARSER_xtra2_port_a register. The Source Number from Port A that gets cropped is defined by the ANC_TARGET_SRCNUM in VIP_PARSER_xtra2_port_a register.

ANC_SKIP_NUMPIX, ANC_USE_NUMPIX, ANC_SKIP_NUMLINES, and ANC_USE_NUMLINES define the region of the selected Source Number that is cropped and sent to memory. The Vertical Ancillary Data Cropping region is described in Figure 1-118.

Figure 1-118. Vertical Ancillary Data Cropping Region

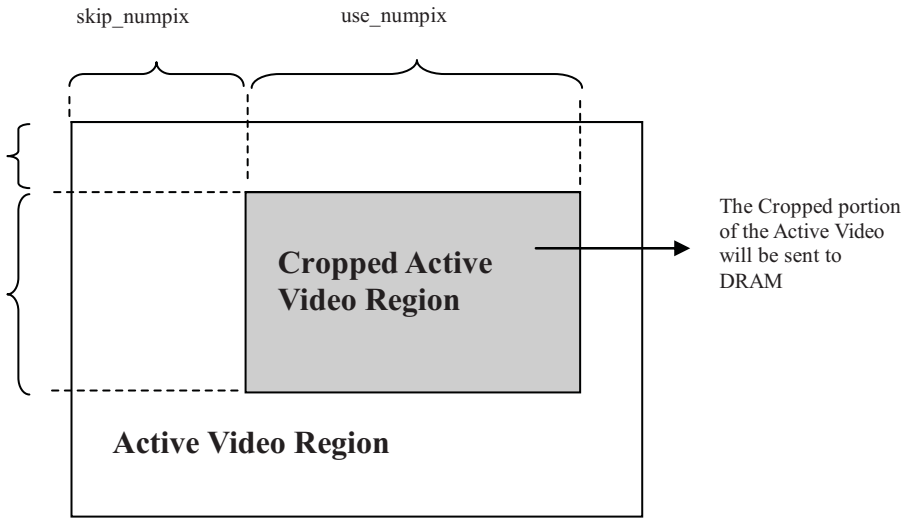


Note that when the VIP is configured to receive data over 8-bit interface, ancillary data from both Luma and Chroma can be captured by configuring ANC_CHAN_SEL_8b to '1x'. Thus, the number of data elements per line in this case is twice the equivalent number of Luma pixels per line. In other words, for this particular dual channel capture example, if there are 720 Luma pixels per line, then the total number of Vertical Ancillary Data Pixels in the source picture can be 2x720=1440 pixels.

For Active Video from Port A, cropping is enabled by setting the ACT_BYPASS_N bit in VIP_PARSER_xtra4_port_a register. The Source Number from Port A that gets cropped is defined by the ACT_TARGET_SRCNUM in VIP_PARSER_xtra2_port_b register.

ACT_SKIP_NUMPIX, ACT_USE_NUMPIX, ACT_SKIP_NUMLINES, and USE_NUMLINES define the region of the selected Source Number that is cropped and sent to memory. The Cropped Active Video region is described in Figure 1-119.

Figure 1-119. Active Video Region

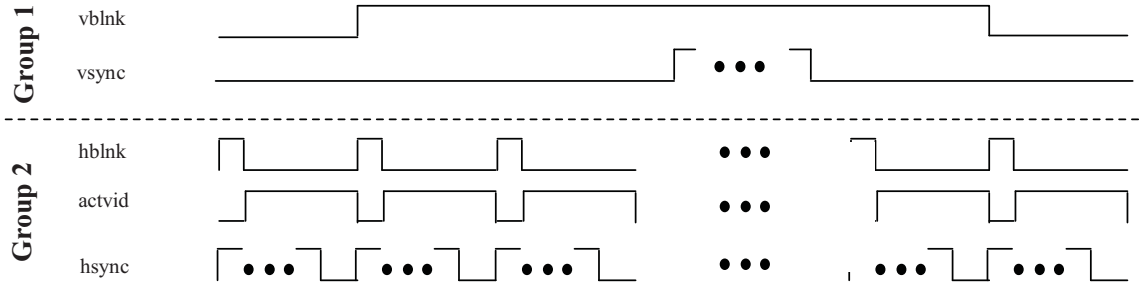


Cropping for Port B works in a similar way to Port A. Since picture data is in 4:2:2 format, SKIP_NUMPIX and USE_NUMPIX must be evenly divisible by 2. If the output of vip_parser is sent to a 4:2:2 to 4:2:0 converter, then USE_NUMLINES must also be evenly divisible by 2.

1.2.8.2.18 Discrete Sync Signals

External ICs generally produce discrete sync interface signals seen in Figure 1-120.

Figure 1-120. Discrete Sync Interface Signals



vbnk represents the vertical blanking interval. Generally, vertical blanking is at the top of a NTSC/PAL field. In certain standards, the last few lines of a field or frame are in vertical blanking in addition to the beginning few lines in the following field or frame.

v**sync** is the vertical sync indicator. vsync is active during a portion of the vertical blanking. Generally, vsync is defined to transition from inactive to active sometime during vertical blanking. This signal then transitions to an inactive state before the end of vertical blanking. Certain standards define the line numbers where vsync transitions.

hblank is the horizontal blanking interval for each line. The horizontal blanking is the same number of pixels whether the line is in the active video region or in the vertical blanking region of the scan.

actvid is the region of a line that is active video. It is exactly inverse of the hblank signal. The number of pixels in the actvid region is the same for a line in vertical blanking as a line in active video.

hsync transitions from inactive to active for the first pixel of each line, which is a horizontal blanking pixel. hsync will transition to the inactive state before the end of the line.

Group 1 signals define the vertical separation between fields or frames. Group 2 signals define the separation between lines. Note that the VIP module defines three discrete sync control signals: Actvid, Hsync, and Vsync. One of the Group 1 signals can be tied to the Vsync input. The Actvid signal from Group 2 is tied to the Actvid input. One of the other two Group 2 signals, hblank or hsync, can be tied to the Hsync input.

USE_ACTVID_HSYNC_N defines whether the line separation method uses the signal from the ACTVID or the HSYNC input of the VIP module. DISCRETE_BASIC_MODE determines whether discrete sync works as described in Section 1.2.8.2.5.1. In summary, choose one signal from Group 1 and one signal from Group 2. There should be a way to capture the external data.

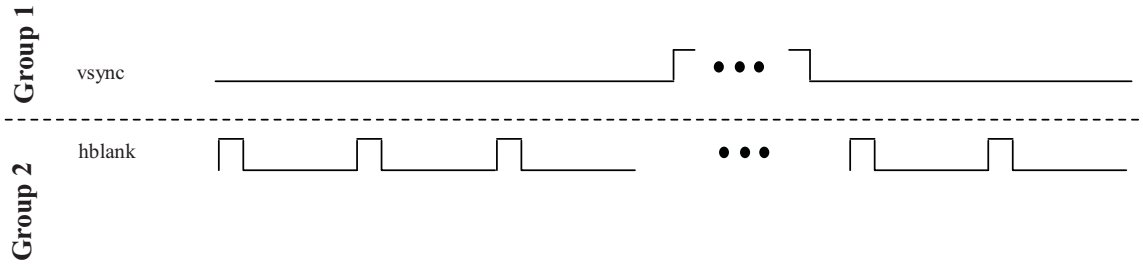
1.2.8.2.18.1 vsync and hblank Input Signals

Figure 1-121 shows vsync from Group 1 and hblank from Group 2 being used. Set USE_ACTVID_HSYNC_N='0' and DISCRETE_BASIC_MODE='1'.

Also, since VIP is not aware of vertical blanking interval start and end, all lines, including both vertical ancillary and active video, will appear in the memory. Lines starting after an inactive to active transition on vsync will delineate a start of frame. Every data element on the Pixel clock's active edge will be stored in the Active Video Buffer.

Note that the vsync signal cannot transition active on the same cycle that hsync transitions active for fast pixel clock rates, since a system clock cycle is needed to insert a new frame indicator into the frame buffer.

Figure 1-121. vsync and hblank Input Signals

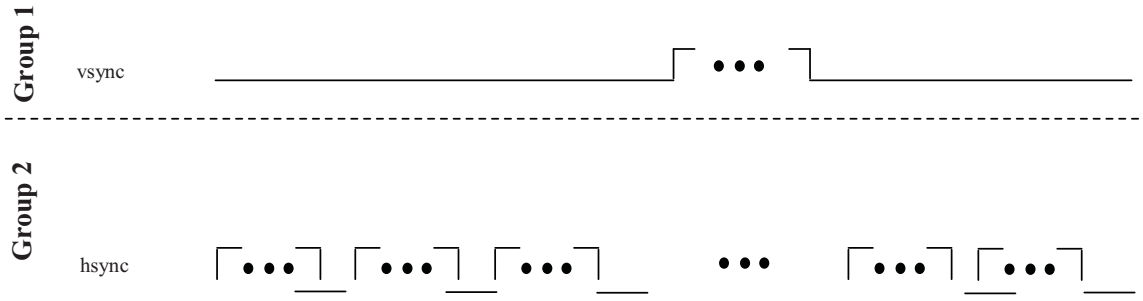


1.2.8.2.18.2 vsync and hsync Input Signals

Figure 1-122 shows vsync from Group 1 and hsync from Group 2 being used. Set USE_ACTVID_HSYNC_N='0' and DISCRETE_BASIC_MODE='1'. Since the VIP is not aware of when VBI data starts and ends, all lines, including both vertical ancillary and active video, will appear in the memory. Lines starting after an inactive to active transition on vsync will delineate a start of frame. Every data element on the Pixel clock's active edge will be stored in the Active Video Buffer. Note that this scenario is the same as the vsync and hblank.

Like the vsync and hblank case, it also holds true that the vsync signal cannot transition active on the same cycle that hsync transitions active for fast pixelclock rates since a system clock cycle is needed to insert a new frame indicator into the framebuffer.

Figure 1-122. vsync and hsync Input Signals

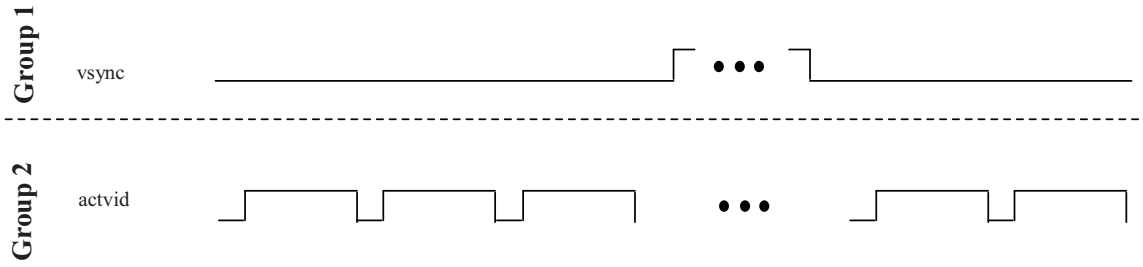


1.2.8.2.18.3 vsync and actvid Input Signals

Figure 1-123 shows vsync from Group 1 and actvid from Group 2 being used. Set USE_ACTVID_HSYNC_N='1' and DISCRETE_BASIC_MODE='1'. Again, since VIP is not aware of when VBI data starts and ends, all lines, including both vertical ancillary and active video, will appear in the memory. Lines starting after an inactive to active transition on vsync will delineate a start of frame. Lines are denoted by an inactive to active transition of actvid. Pixel will be saved only when actvid is active.

Note that vsync must transition active between the actvid delineated data. vsync cannot transition active when actvid is active.

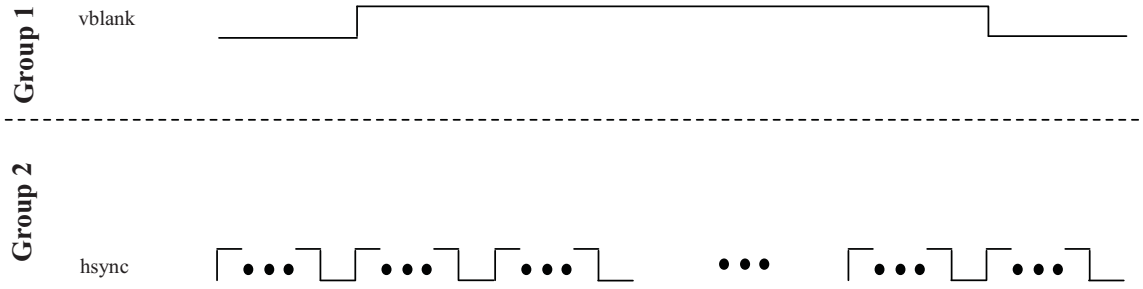
Figure 1-123. vsync and actvid Input Signals



1.2.8.2.18.4 vblank and hsync Input Signals

Figure 1-124 shows vblank from Group 1 and hsync from Group 2 being used. In this scenario, set USE_ACTVID_HSYNC_N='0' and DISCRETE_BASIC_MODE='0'. Again, since VIP is aware of the start and end of vertical blanking interval start and end, vertical ancillary and active video data will appear in different memory buffers. Lines starting from inactive to active transition on vblank will delineate a start of the frame. When vblank is active, all data elements on pixel clock's active edge will appear in ancillary data buffer and when vblank is inactive, all data elements on pixel clock's active edge will appear in video data buffer.

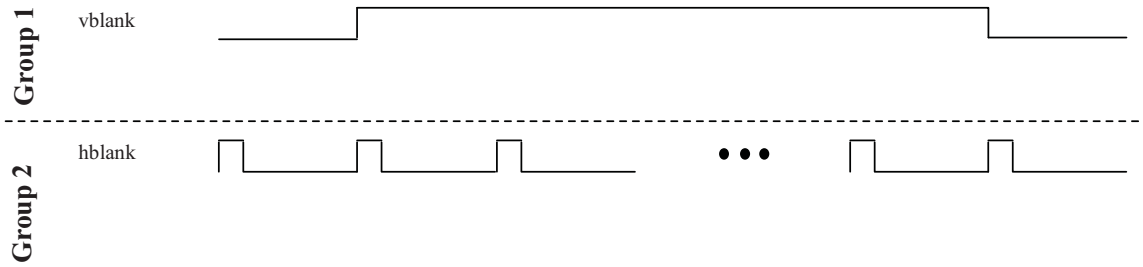
Figure 1-124. vblank and hsync Input Signals



1.2.8.2.18.5 vblank and hblank Input Signals

Figure 1-125 shows the vblank from group1 and hblank from group2 signals being used. In this case, set USE_ACTVID_HSYNC_N='0' and DISCRETE_BASIC_MODE='0'. Again, since VIP is aware of the start and end of vertical blanking interval start and end, vertical ancillary and active video data will appear in different memory buffers. Lines starting from inactive to active transition on vblank will delineate a start of the frame. When vblank is active, all data elements on pixel clock's active edge will appear in ancillary data buffer and when vblank is inactive, all data elements on pixel clock's active edge will appear in video data buffer.

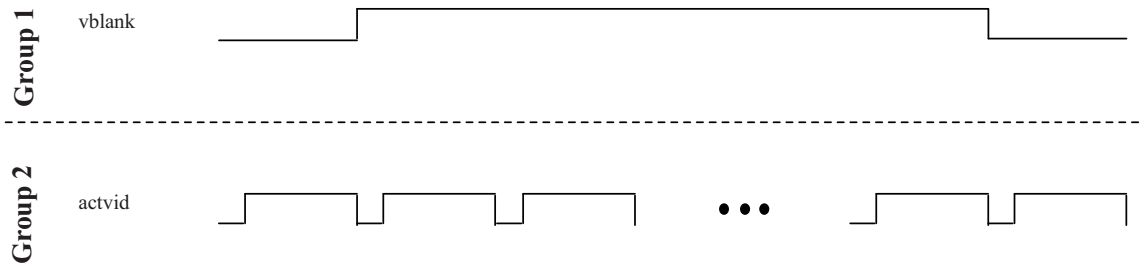
Figure 1-125. vblank and hblank Input Signals



1.2.8.2.18.6 vblank and actvid Input Signals

Figure 1-126 shows vblank from Group 1 and actvid from Group 2 being used. Set USE_ACTVID_HSYNC_N='1' and DISCRETE_BASIC_MODE='0'. Again, since VIP is aware of the start and end of vertical blanking interval start and end, vertical ancillary and active video data will appear in different memory buffers. Lines starting from inactive to active transition on vblank will delineate a start of the frame. When vblank and actvid are active, all data elements on pixel clock's active edge will appear in ancillary data buffer and when vblank is inactive and active is active, all data elements on pixel clock's active edge will appear in video data buffer.

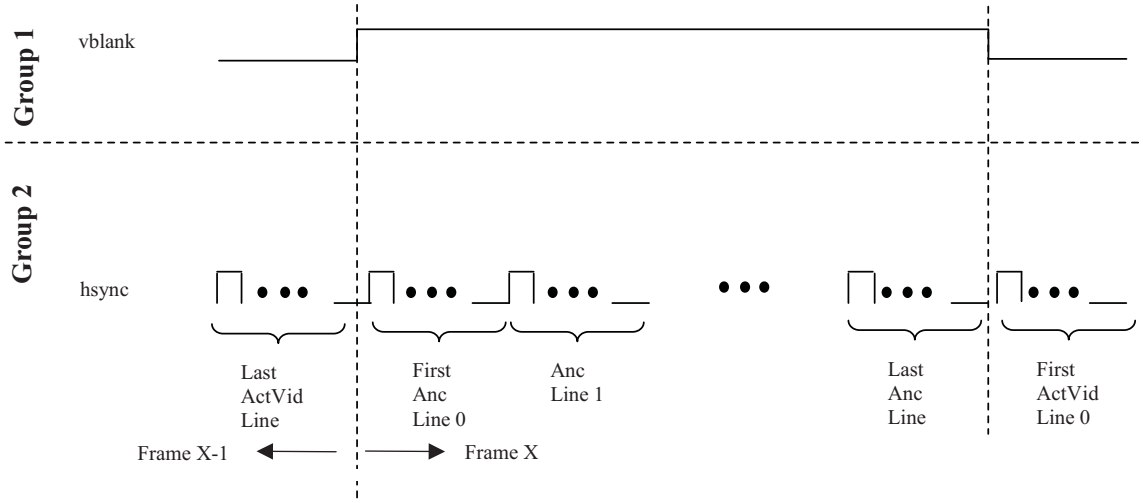
Figure 1-126. vblank and actvid Input Signals



1.2.8.2.18.7 Line and Pixel Capture Examples

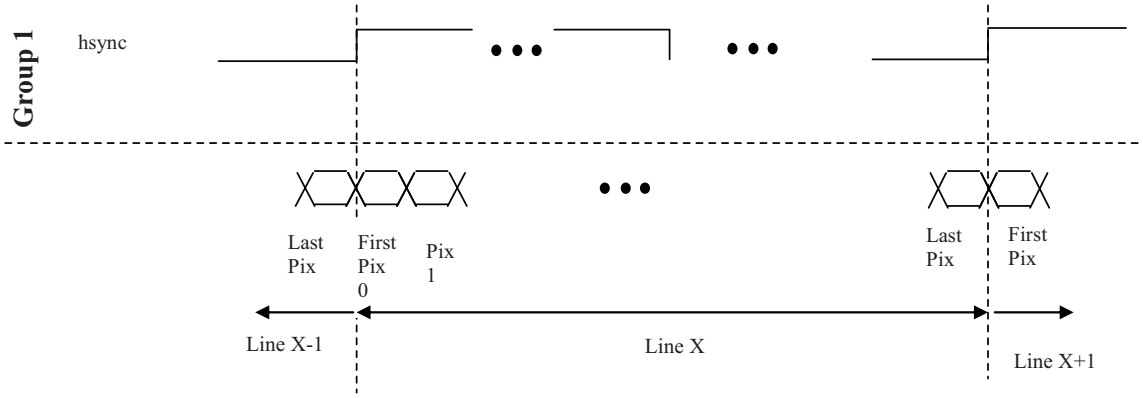
When DISCRETE_BASIC_MODE = '0', vblank is used. All the lines where the start of line is under an active vblank are sent to the Ancillary Data buffer. All the lines where the start of line is not under an active vblank are sent to the Active Video framebuffer. This situation is shown in Figure 1-127.

Figure 1-127. Line and Pixel Capture, vblank and hsync



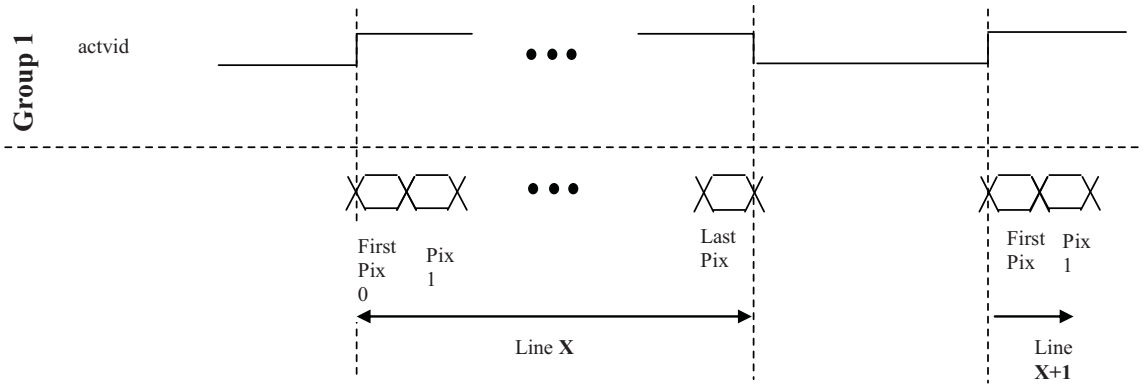
The start of line is the pixel represented by the inactive to active transition on Hsync when USE_ACTVID_HSYNC_N = '1'. Figure 1-128 illustrates the delineation of a line when using USE_ACTVID_HSYNC_N = '1.'

Figure 1-128. Line and Pixel Capture, hsync



The start of line is the pixel represented by the inactive to active transition on actvid when USE_ACTVID_HSYNC_N = '0.' Note that actvid stays active for the entire duration of active video portion of the line. This scenario is shown in Figure 1-129.

Figure 1-129. Line and Pixel Capture, actvid



In 8-bit mode, note that the 4:2:2 YUV input color component order is Cb, Y followed by Cr and Y. For 16 and 24-bit input modes, all the components are sent in the same cycle.

1.2.8.2.19 VIP Overflow Detection and Recovery

It is possible that an overflow can occur in the VIP_PARSER. Overflow detection is determined by reading the VIP_PARSER_fiq_status register and checking for bits 8, 7, 5, 4, 3 and 2. If video is being captured, and any of these bits are set, it indicates that not all of the incoming video data was sent to DDR. VIP Overflow can be caused by one of the following:

1. External pixel clock is faster than processing clock
2. DDR bandwidth is temporarily over-consumed
3. VIP scaler is being used inline with external video input, and is upscaling.
   - VIP scaler in this use case can only be used for downscaling
4. VIP scaler is being used inline with external video input, but has not been configured with scaler coefficients
   - VIP scaler will not accept video input if it is not first configured with scaler coefficients. This will cause overflow
5. VIP scaler is being used inline, but has not been enabled
6. External cables are connected or disconnected while the system is running, resulting in corrupted video streams going into the VIP
7. Bad external video cable, which causes corrupted video streams going into the VIP

Items 6 and 7 are typically seen as noise events, where it is likely that multiple horizontal syncs per line and/or multiple vertical syncs per frame will be observed. These result in high peak throughput requirements, leading to DDR bandwidth being temporarily over-consumed, and thus VIP overflow.

The high level recovery method for VIP Overflow on port a is outlined below. Port b is similar :

1. Set yuv_srcnum_stop_immediately = 0xFFFF_FFFF
2. Set anc_srcnum_stop_immediately = 0xFFFF_FFFF
3. Set ENABLE = 0
4. Set CLR_ASYNC_FIFO_RD and CLR_ASYNC_FIFO_WR to 1
5. Set SW_RESET to 1
6. Reset Other VIP modules
   - For each module used downstream of VIP_PARSER, write 1 to the bit location of the clkc_rst register which is connected to VIP_PARSER (will be bits 20-23 and 25-28)
7. Abort VPDMA channels
   - Write to list attribute to stop list 0
   - Write to list address register location of abort list
   - Write to list attribute register list 0 and size of abort list
8. Set SW_RESET to 0
9. Un-reset Other VIP modules
   - For each module used downstream of VIP_PARSER, write 0 to the bit location of the clkc_rst register which is connected to VIP_PARSER (will be bits 20-23 and 25
10. (Delay)
11. SC coeff downloaded (if VIP_SCALER is being used)
12. (Delay)
13. Set yuv_srcnum_stop_immediately = 0x0000_0000
14. Set anc_srcnum_stop_immediately = 0x0000_0000
15. Set ENABLE = 1
16. Set CLR_ASYNC_FIFO_RD and CLR_ASYNC_FIFO_WR to 0

1.2.9 De-Interlacer (DEI) Module

The de-interlacer (DEI) module is used to generate progressive data output from interlaced input format (also known as, deinterlacing).

1.2.9.1 Features

- Motion-adaptive deinterlacing
  - Supports 4-field Motion detection
  - Motion sensitivity adaptive to the frequency of luma texture
- Edge-Directed Interpolation (EDI)
  - Edge detection using luma pixels in a 2x7 window
  - Half-pixel resolution edge vectors
  - Edge-directed luma and chroma interpolation
  - Soft-switch between edge directed interpolation and vertical interpolation depending on the confidence factor
- Film Mode Detection (FMD)
  - 3-2 pull down detection
  - 2-2 pull down detection
  - Hysteresis controls how fast FMD can enter/exit film mode (software function)
- Bad Edit Detection (BED)
- The module can pass the inputs data directly to the outputs in a bypass configuration. No internal processing is performed.

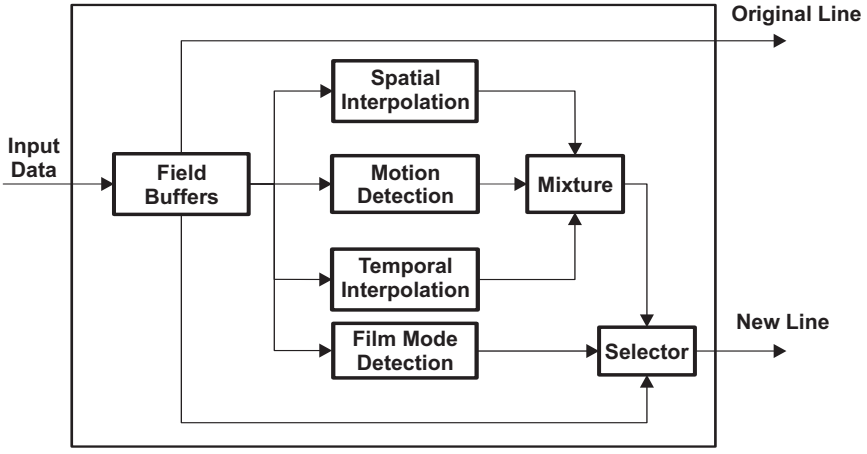
1.2.9.2 Functional Description

The following figure illustrates the block-diagram of motion-adaptive Deinterlacer. The general concept behind motion adaptive deinterlacing is that spatial filtering works very well for images with motion, while temporal filtering works very well for static images. So, the intuitive way is to combine them together. Motion detection is used to switch or fade between the use of spatial deinterlacing and temporal deinterlacing, as shown in the following formula.

$$\hat{y}(j, i, n) = \alpha y_{spat}(j, i, n) + (1 - \alpha) y_{temp}(j, i, n)$$

where $y_{spat}(j, i, n)$ is the spatial interpolation output, $y_{temp}(j, i, n)$ is temporal interpolation output, α is the motion detection output ranging from 0 to 1, $\hat{y}(j, i, n)$ is the final output from deinterlacer, and j, i, n are the vertical, horizontal, and temporal indexes, respectively. From the previous formula, the final output is controlled by the motion detector output, α. The higher the motion, the higher value of α, and the output favors spatial interpolation. If the motion is absent or very low, the temporal interpolation has higher weight.

Figure 1-130. Block Diagram of Motion-Adaptive Deinterlacer



Temporal interpolation can be disabled by programmable control registers. In that case we have:

$\hat{y}(j, i, n) = y_{spat}(j, i, n)$

Chroma interpolation is handled in the same manner as luma with regards to the above equations. There is a separate control for disabling temporal interpolation for chroma, such that luma can perform the full mixture, and chroma can only be spatial. If luma temporal interpolation is disabled, chroma temporal interpolation is also disabled.

The Figure 1-130 provides a simple description of how a motion-adaptive deinterlacer operates. The actual interpolation used is edge directed interpolation. Edge directed interpolation is only performed spatially prior to the output mixing.

1.2.9.2.1 Modes of Operation

The DEI can be operated in bypass mode and deinterlacer mode.

1.2.9.2.1.1 Bypass Mode

In the bypass mode, input luma and chroma are buffered and sent to the stage after DEI without processing.

To set DEI in the bypass mode, the bypass bit must be set accordingly in the configuration register.

1.2.9.2.1.2 Film Mode Detection (FMD)

Film mode detection is performed by both hardware and software. In every field, the hardware accumulates difference between two neighboring frames (two top fields or two bottom fields), difference between two adjacent fields, and combing artifact. At the end of DEI data processing, an interrupt will be sent to the processor. The processor needs to read three status registers from DEI, calculate whether the film mode has been entered or existed, and update film mode lock and jam direction (fmd_cfg0) MMR of DEI before the next field starts. Since it is a time sensitive processing, the FMD interrupt has to be a high priority interrupt to the processor.

Film mode detection can be performed on a full picture size or a smaller window specified by a few MMR registers. The interrupt is always asserted at the end of the entire DEI data processing and is not affected by the window size and location.

Implementing film mode detection algorithm in software allows more flexibility at the cost of timing critical interface between DEI and the processor. For example, customers may find later that supporting 3-2-2-3 pull down is needed. This feature can be easily added by upgrading only the FMD software.

FMD feature is supported by the DEI module. More details about FMD mode, they are discussed in the DEI_H section.

See the appendix for configuration details on FMD.

1.2.9.2.1.3 Deinterlacer Mode

In the deinterlacer mode, DEI takes in alternative field YUV data and sends out a sequential frame YUV data by interpolation techniques mentioned below.

DEI supports four interpolation modes when converting interlaced pictures to progressive pictures.

1.2.9.2.2 Modes of Interpolation

1.2.9.2.2.1 Interpolation Mode 0

In mode 0, the interpolated field is created by simple line averaging from the original YUV data. That is, the interpolated line is created by averaging its top and bottom line. Setting of MDT mode has no effect on output pictures.

1.2.9.2.2.2 Interpolation Mode 1

In mode 1, the interpolated field is created by averaging pixels from fields before and after the current field. In other words, if the current field is a top field, the interpolated bottom field picture is created by averaging pixels from bottom field pictures before and after the current field. MDT setting has no effect on the result.

1.2.9.2.2.3 Interpolation Mode 2 (EDI)

Mode 2 is an edge assisted interlace mode with edges detected from the luma information of a 2 × 7 (H × W) frame window. It detects seven possible edges between 45 and 135 degrees. Edges with slopes greater than 135 degrees are treated as 135 degree lines, and edges with slopes less than 45 degrees are treated as 45 degree lines.

Luma for missing lines are interpolated using original luma along the detected edge.

Motion value (MV) from the MDT module is used to select coefficients from a look up table on how 2D interpolation from the current field and 3D interpolation from two fields adjacent to the current fields are blended. The way to perform blending for chroma is slightly different than for luma, because the MV is based on luma and extra care needs to be taken when blending is applied to chroma.

At this mode, edge-directed interpolation is applied to luma only. Vertical interpolation is performed for chroma data.

1.2.9.2.2.4 Interpolation Mode 3 (EDI)

The edge detection method used in this mode is similar to interpolation mode 2. The only difference is that the edge-directed interpolation is performed on both Luma and Chroma. Chroma is interpolated similarly according to the edge vectors obtained based on luma information. The reason chroma is interpolated slightly different is because of the down-sampled chroma data.

1.2.9.2.3 Motion Detection (MDT)

Motion values from the MDT module are calculated only based on luma information. The motion value is used to determine how 2D and 3D interpolated results should be blended. The motion value is also used in the Film Mode Detection (FMD) module to determine field and frame differences between frames, which are in turn used in film mode detection.

The motion detection module in DEI supports 4-field mode.

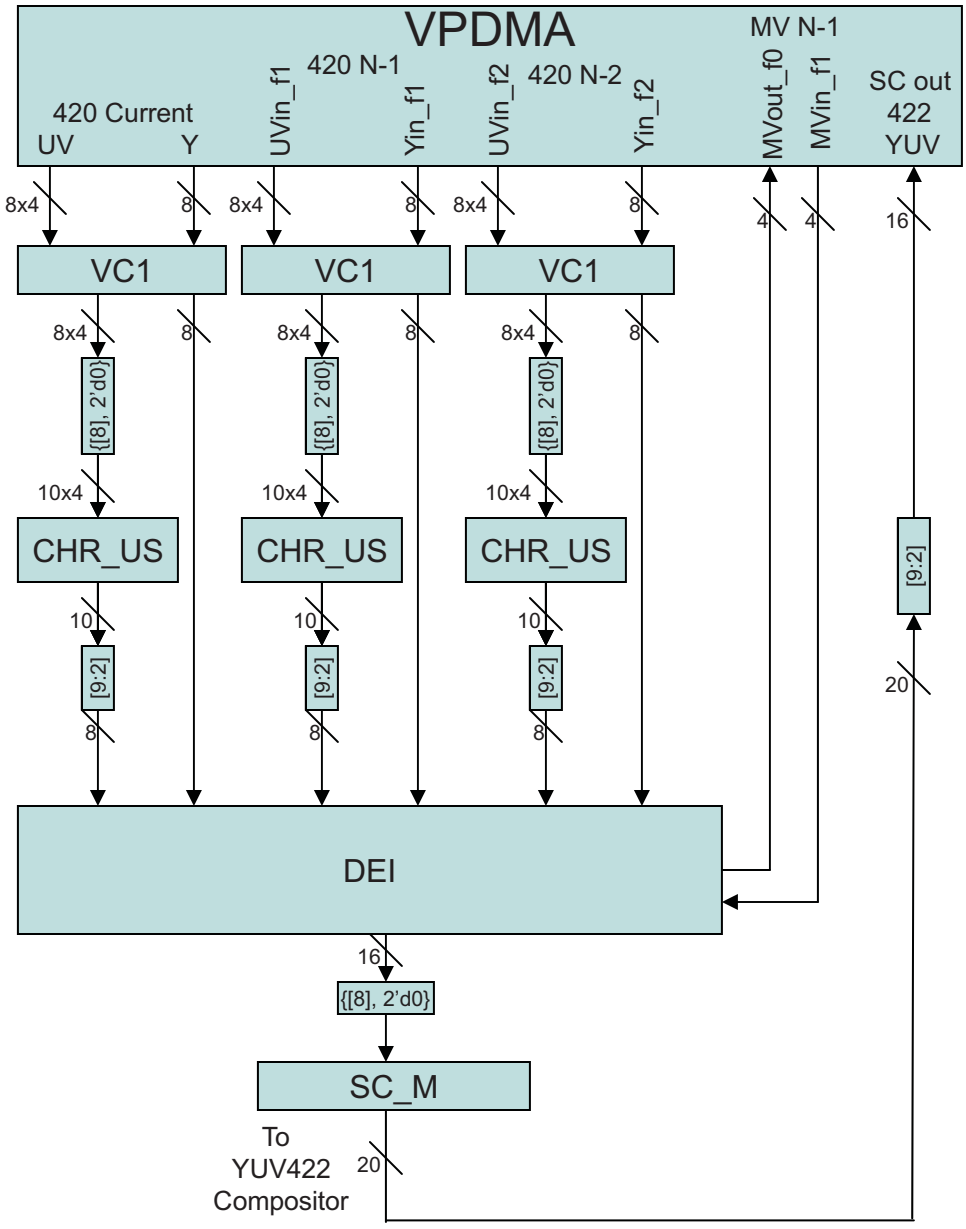
Motion value (MV) is first estimated from y_f0 and y_f2 (current and two field delayed Y). The max value of MV and one field delayed data of MV, MV_f1, is used to create the overall MV per pixel. Since this motion detection method utilizes three fields of luma data and one field delayed MV, it is called 4-field mode as MVs come from four fields of luma data.

There is one field delay between the YUV inputs and the YUV outputs. The “current_field” that the interpolator works on is the YUV_f1 data.

1.2.9.2.4 Data Buffer Management

VPDMA is used to transfer the data in and out of DEI as shown in the following figure.

Figure 1-131. VPDMA Transfer Ports



The following are the VPDMA ports (from DEI to memory) available:

- Inputs
  - Current (N)
    - Y (current Luma)
    - UV (current Chroma
  - One field delay (N-1)
    - Yin_f1 (1-field delayed Luma)
    - UVin_f1 (1-field delayed Chroma)
    - MVin_f1 (1-field delayed Motion Vectors)
  - Two field delay (N-2)
    - Yin_f2 (2-field delayed Luma)
    - UVin_f2 (2-field delayed Chroma)

- Outputs
  - Current
    - Scalar output (422 interleaved output from scalar)
    - MVout_f0 (Motion vectors)

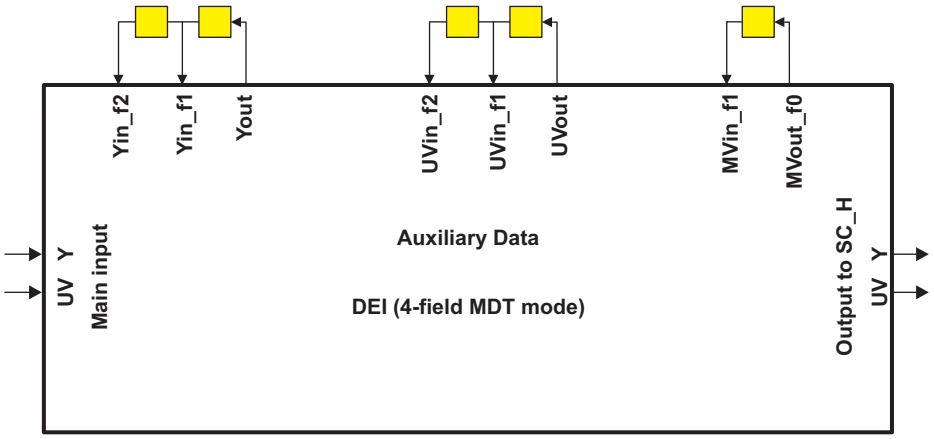
In the previously listed ports, except Y and UV (current) and Scalar output (current) (referred to as main data), all the other ports directly interact with DEI through VPDMA and are referred to as auxiliary data for DEI module. All the Y and UV ports in auxiliary data require 8 bits/pixel while MV port requires 4 bits/pixel.

1.2.9.2.4.1 4-field MDT-based Interpolation Mode

In this mode, the required external memories are three fields of Luma input, three fields of chroma input, and two fields of 4-bit MV.

- Inputs
  - Y
  - UV
  - Yin_f1
  - Yin_f2
  - UVin_f1
  - UVin_f2
  - MVin_f1
- Outputs
  - MVout_f0
  - Output Scalar

Figure 1-132. Auxiliary Data



1.2.9.3 Interrupts

The following two interrupts are generated by the module.

Table 1-65. Module Interrupts

Interrupt	Description
dei_fm_int	Interrupt indicating film mode is enabled and software needs to read Film Mode statistics registers and update the Film Mode lock and jam direction configuration registers. This is required to be a high priority interrupt.
dei_error_int	Interrupt indicating an error condition has occurred

1.2.9.3.1 Interrupt Description

Two interrupts from DEI module are mapped to HD-VPSS level interrupt handler. Those are discussed below.

1.2.9.3.1.1 dei_fm_int

This interrupt is controlled by enabling film mode detection. Once enabled, this interrupt will occur on every input field and tells software that it needs to read the fmd_reset, fmd_frame_diff, fmd_field_diff and fmd_caf registers and execute the Film Mode software program to determine whether to lock film mode and the jamming direction.

This interrupt needs to be serviced as a high priority interrupt. The position the interrupt is generated within a field can be controlled through configuration registers (fmd_window_enable, fmd_window_minx, fmd_window_miny, fmd_window_maxx and fmd_window_maxy). If the window is enabled, the statitics will be gathered over the window bounded by the other register settings, and the interrupt will be generated at the bottom of the window, meaning, the window can be set at the top of the field to generate the interrupt as soon as possible. This interrupt needs to be serviced before the next field is input to the deinterlacer.

The interrupt is fired at the end of the defined film mode window. If the FMD window is not enabled, the entire frame size is used, and the interrupt will occur at the end of the field. Software services the interrupt and then applies “lock and jam” MMR controls to put the design in film mode. This must occur before the next field input. If the entire window is used, there is very little time to perform this servicing and register setting when the design is used in a memory to memory mode. When in a memory to memory mode, and particularly if the “field_flush” control bit is low, the film mode window must be used, and set to provide as much time as possible between the end of the film window and the end of the actual input field. Generally speaking, the film window should end 1 or 2 lines from the bottom of the real field to provide 1 or 2 line times to service the interrupt and apply the lock and jam registers for the next input field. While this means that the entire window is not used for calculating film mode statistics, excluding the last 1 or 2 lines should have negligible impact.

1.2.9.3.1.2 dei_error_int

This interrupt will occur under the following conditions:

(a) The field ID of the current input frame is the same as the field ID of the last frame. The field ID corresponds to whether the input field is the “top” (all even lines) or “bottom” (all odd lines) field. Two subsequent input frames must have opposite field IDs.

(b) An end of frame input has occurred on the input field data (VPI end of frame for current field), but the internal counters have not counted to either the programmed width or height. This indicates that the input data to the Deinterlacer does not match the programmed width and height the Deinterlacer is expecting.

(c) A start of frame input has occurred on the input field data (VPI start of frame for current field), but the internal counters are not at 0. This indicates that a new video field was started before the last video field was completed.

In any of these cases, the input video data is not matching what the deinterlacer programming is expecting. Software should reconfigure the deinterlacer to match the proper input video timing.

1.2.10 Noise Filter (NF)

1.2.10.1 Overview

Noise is one of the most important factors affecting video quality. Random noise can be sensor noise, A/D conversion noise, analog transmission noise, etc. Since human eyes are very sensitive to oscillating signals, the visual quality degenerates significantly even when the noise level is small. Video coding efficiency also suffers from noise because the video encoder has trouble in matching noisy blocks and has to spend extra bits to encode useless noise. Noise reduction plays a fundamental role in improving visual quality and coding efficiency.

There are normally two types of noise reduction techniques – spatial filter and temporal filter. Spatial filter processes each frame individually. Even though each frame becomes clean, the video may still look noisy due to frame-to-frame intensity changing. Temporal filter can remove the frame-to-frame intensity changing. But for moving areas, ghosting artifacts may occur because the pixel-to-pixel correspondence between two consecutive frames is impacted due to the processing. In the noise reduction algorithm of the NF module, a combination of spatial and temporal filter is applied to overcome the shortcomings of both techniques.

It is desirable to have the spatial and temporal filters adaptive to the noise level of the video. If the filters are too weak, the noise may be still obvious. If the filters are too strong, edges and details may be blurred and ghosting artifacts may appear. Noise levels may vary a lot within a video sequence. Automated noise estimation is necessary to measure the noise level of each video clip and adjust the parameters of the filters properly.

This document describes the Video Noise Filter (NF) which is used to reduce noise in a video sequence in order to improve video image quality and compression efficiency.

1.2.10.2 Features

The NF module has the following features:

- Spatial and temporal video noise filtering
- Built-in noise measurement
- Adaptive to noise and motion
- YCbCr 4:2:0 Video format support

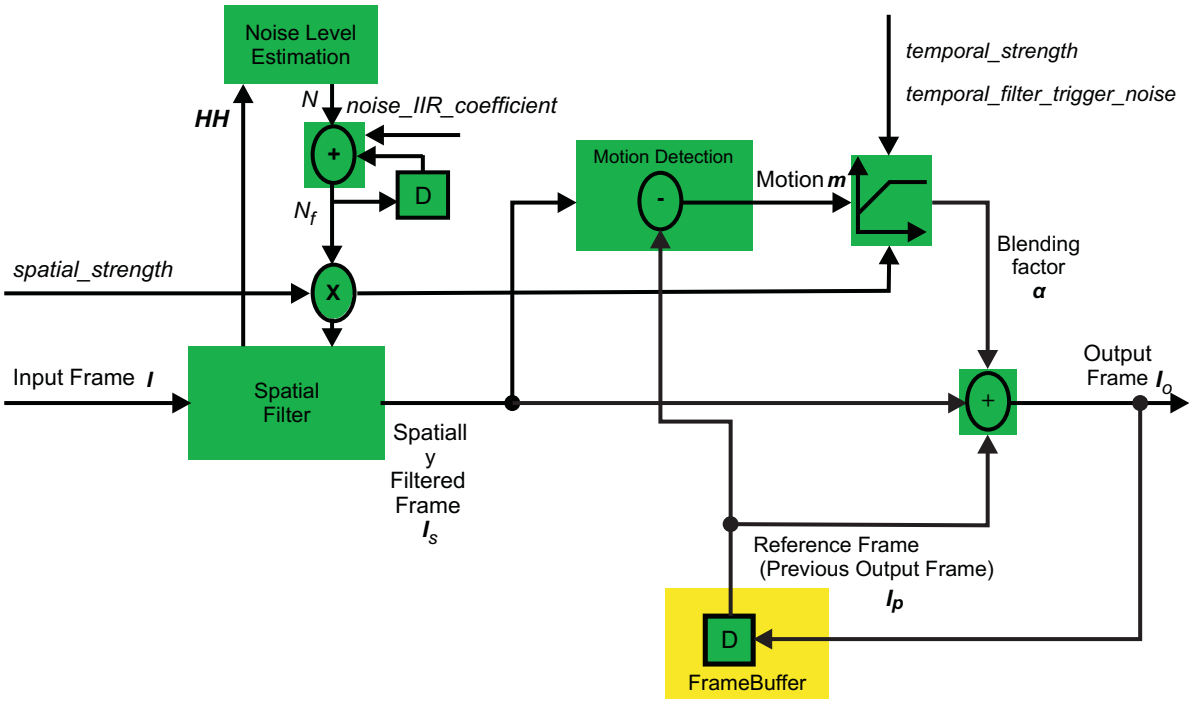
1.2.10.3 Functional Description

The Video Noise Filter implemented in this device is a combination of spatial and temporal IIR filters. The spatial filter is performed with neighboring pixels in the current frame while the temporal filter is performed with a past filtered frame to suppress both spatial and temporal noises.

The spatial and temporal filters are adaptive to the noise level of the video to deal with varying noise levels in different video contents. Noise estimation is performed by the hardware to measure the noise level of each video clip and to automatically adjust the parameters of the filters properly. Figure 1-133 shows the algorithmic block diagram of the noise filter.

The implementation of the video noise filter uses tile-based processing. The algorithm divides a frame into 32x32 tiles and process each of them independently. If the width or height of the frame is not a multiple of 32, 0x0s (for Luma) and 0x80s (for Chroma) will be padded into rightmost and/or bottommost tiles.

Figure 1-133. Noise Filter Architecture Block Diagram



1.2.10.3.1 Spatial Filter

The algorithm kernel size of the spatial filter is 3 (row) x 7 (column). With edge pixels replicated as shown in Figure 1-134, a 3x7 sliding window is used to process the entire 32x32 tile.

Figure 1-134. Top-left Corner of a Tile After the Boundary Replication

00	00	00	00	01	02	03	04	05	06
00	00	00	00	01	02	03	04	05	06
10	10	10	10	11	12	13	14	15	16
20	20	20	20	21	22	23	24	25	26
30	30	30	30	31	32	33	34	35	36
40	40	40	40	41	42	43	44	45	46

For each 3x7 input, one pixel comes out as output as shown in 3x7 Pixel Output.

3x7 Pixel Output

						X
			O			X
						X

For U and V channels, this filtering needs to be performed only at even rows and even columns due to the 4:2:0 format.

1.2.10.3.2 Temporal Filter

The temporal filter is motion- and noise- adaptive. The motion at each pixel is measured as the sum of the absolute differences between the spatially filtered pixel (Ys, Us, Vs) of the current frame and the output pixel (Yp, Up, Vp) of the previous frame.

m = |Ys – Yp|+|Us – Up|+|Vs – Vp|

Figure 1-135. Motion versus Blending Factor Function

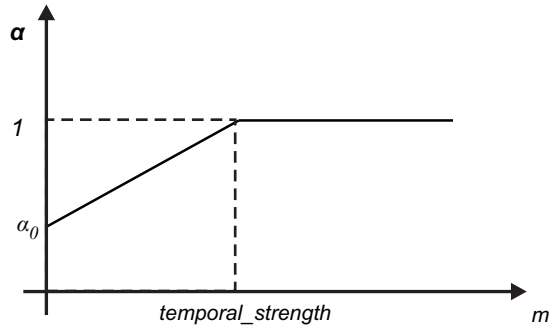


Figure 1-135 shows how the motion value, **m**, translates into the blending factor α. It can be written as:

$\alpha = \alpha_0 + (1 - \alpha_0) * m / temporal\_strength$ if m < temporal strength

=1 if m >= temporal strength

where temporal_strength is a register to control the strength of the temporal filter. Setting it to 0 means the temporal filter is essentially bypassed. The discussions on the parameter α_0 will be detailed in Section 1.2.10.3.4.

The output pixel value of the temporal filter is:

$\mathbf{I_o = \alpha I_s + (1 - \alpha) I_p}$

where $\mathbf{I_s}$ is the spatially filtered pixel value at the current frame and $\mathbf{I_p}$ is the pixel value of previous output frame.

1.2.10.3.3 Noise Estimation

For each tile, the noise level *tileNoise* is the average of absolute pixel differences between the input frame **I** and the previous output frame $\mathbf{I_p}$. In the averaging, the absolute pixel differences which are smaller than *max_noise* are only taken to avoid strong moving edges. The noise level of a frame *Frame_noise* is the average noise level of all *tileNoises* in a frame. Some tiles that contain inaccurate noise level need to be excluded from the averaging calculation. They are:

(a) The boarder tiles on the four edges of a frame. They may contain zeroes that are padded to make the frame size a multiple of 32.

(b) Pure dark or pure white tiles. The max and min Y values of a tile are used to determine if a tile is pure black or pure while one. If maxY<pure_black_threshold, it is a pure black tile. If minY>255 - pure_white_threshold, it is a pure white tile.

Y, U, V channels have their own noise level respectively, denoted as *Frame_noise_Y*, *Frame_noise_U*, *Frame_noise_V*.

1.2.10.3.4 Threshold and α_0

At the end of each frame, the accumulated noise level *Frame_noise_Y*, *Frame_noise_U*, *Frame_noise_V* are processed to generate the thresholds for the spatial filter and the α_0 of the temporal filter. The noise level will first pass an IIR low pass filter as shown in the following example.

```
Frame_noise_filtered=Frame_noise_previous* noise_IIR_coefficient +Frame_noise *(1-
 noise_IIR_coefficient )
```

This IIR low pass filter will make the measured noise level change slowly across frames. The register *noise_IIR_coefficient* controls how fast it changes.

The thresholds of the spatial filter will be the filtered frame noise scaled by *spatial_strength*.

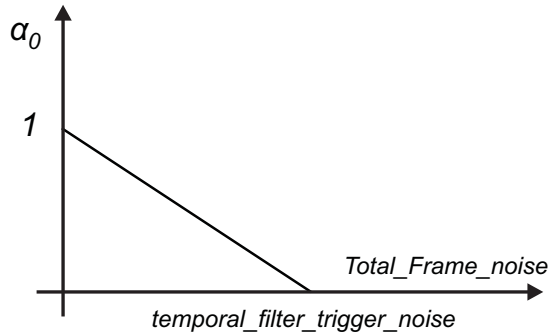
```
Threshold = spatial_strength * Frame_noise_filtered
```

α_0 is the offset of the motion vs blending factor function. It is controlled by the total noise level *Total_Frame_noise* as shown in Figure 1-136. The total noise of all three channels is

```
Total_Frame_noise = Frame_noise_Y + Frame_noise_U + Frame_noise_V
```

where *temporal_filter_trigger_noise* is a register to control the slope of the function in Figure 1-136. This function will make α_0 to be close to 1 if the measured noise level is low, and therefore the temporal filter to be very weak to avoid ghosting artifacts.

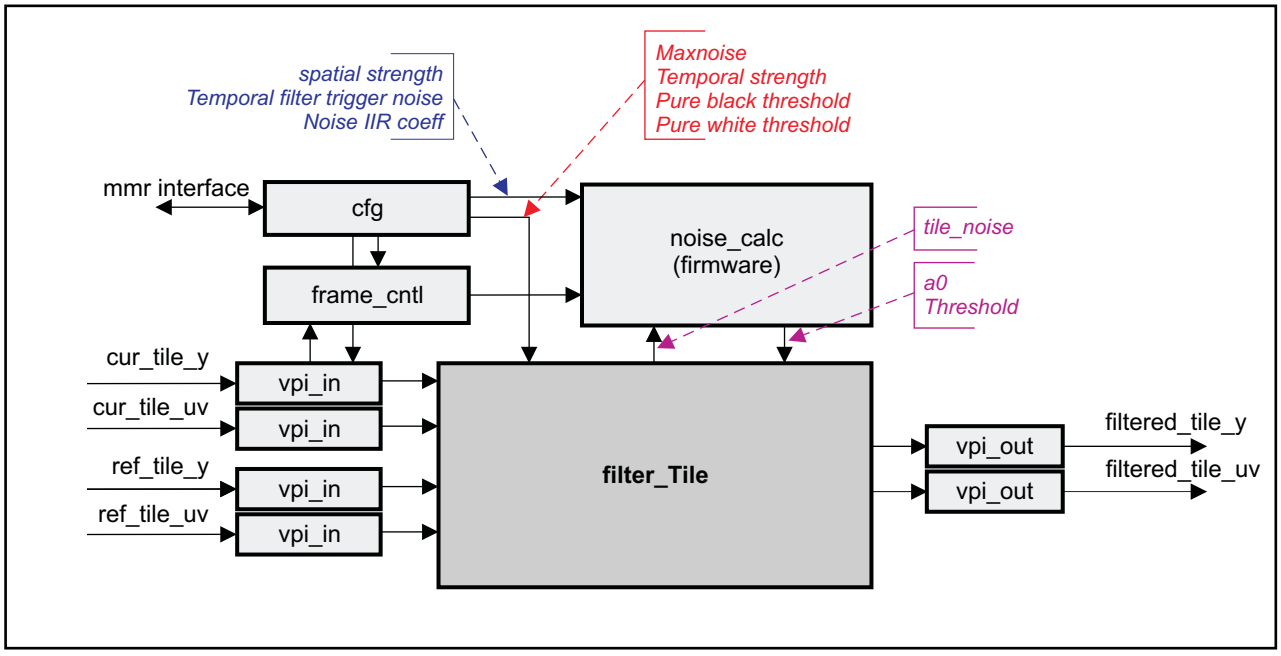
Figure 1-136. α_0 versus *totalFrame_noise* function



1.2.10.3.5 Hardware Implementation

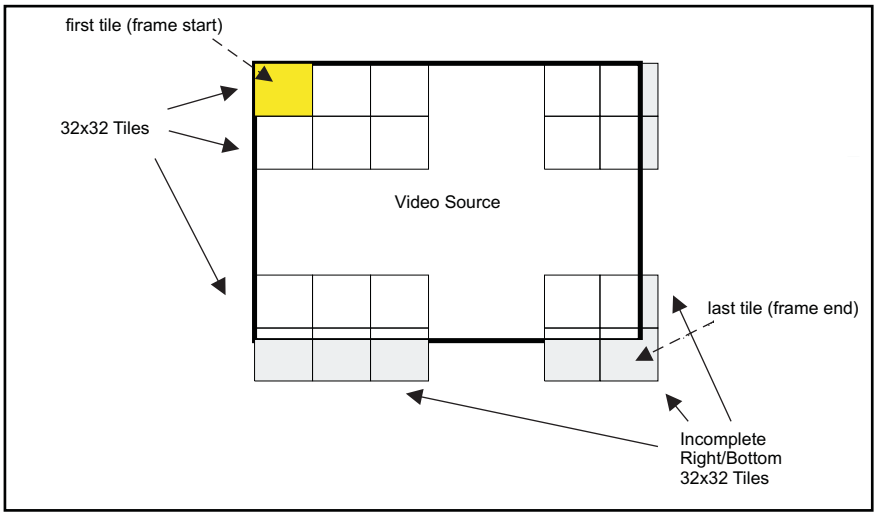
The NF hardware consists of the main filter_Tile processing unit which contains the main spatial and temporal filter logics and a number of support logics which include mainly MMR configuration module, VPI data in and out interface modules, frame noise calculation module (noise_calc) as shown in Figure 1-137.

Figure 1-137. Hardware Implementation Block Diagram



The NF always works on blocks of 32x32 Luma and 32x16 Chroma tiles (U and V channels together). The video source size (width/height) configured in NF_REG1 can be non-multiples of 32. But, the VPDMA/CHR_DS still must send full size tiles to the NF module. Any pixels outside the valid video size (see Figure 1-138) are replaced internally by the vpi_in sub-block with 0x0 for luma and 0x80 for chroma data.

Figure 1-138. Incomplete Boundary Tile Data Masking



Note that ref_tile in the above diagram refers to the (N-1)th output field/frame (previous filtered_tile) while cur_tile refers to the Nth input field/frame.

The arrival of the very first tile of each video frame is used to trigger the frame processing set up and the timing of the last tile sent out is used to trigger the last frame noise calculation and saving.

The noise_calc module (which implements the task of “firmware” described in Section 1.2.10.3.4) keeps track of each tile’s noise output and generates a frame noise at the end of last tile processing.

1.2.10.3.6 Video Source Multiplexing

The hardware has 32 sets of frame noise registers to allow video source switching for up to 32 sources without the software having to read and re-initialize the frame noise values every time the video source is switched. The software simply sets the “nf_video_index” parameter of NF_REG0 register to indicate which stream the NF module is currently processing. The NF then uses the selected frame noise data to generate the threshold for the spatial filter and the α_0 of the temporal filter for next frame processing and updates the frame noise data at the end of the frame.

If more than 32 sets of video sources are to be processed through the NF, then the software needs to manually read the saved frame noise (indexed by “frame_noise_read_index” of NF_REG7) from NF_REG8 and NF_REG9. The read noise values can then be reloaded next time the same video source is to be processed by writing to data to the NF_REG8 and NF_REG9 and also by setting the “nf_frame_noise_init_en” parameter of NF_REG0.

NF_REG0 (nf_frame_noise_update_en) bit can be used to disable the saving of collected Frame noise information in cases where sliced based filtering is used and the same filter setup is desired for all slices. In this case, the update should only be done at the beginning or end of the frame – once per frame.

1.2.10.4 Configuration Examples

1.2.10.4.1 Example of 16-Channel Use Case

For example, when NF is used to process 16 channels, the steps below show how we should configure for channel 12.

Frame 0, Initialization:

1. nf_video_index = 12
2. nf_frame_noise_init_en=1
3. Initialize NF_REG8 and NF_REG9 (Frame_noise_y, Frame_noise_u, Frame_noise_v) with the desired initialization values.
4. nf_frame_noise_update_en =1

Complete frame processing (the steps 1, 2, and 3 above are used to set the initialization values for noise measurement, and step 4 means the measured noise value per field/frame will be updated through the IIR filter.)

Clear the initialization flags at Frame 1:

nf_frame_noise_init_en=0

At this point, to read the measured noise levels:

Set frame_noise_read_index = 12

Read stored Frame_noise_y/u/v through NF_Reg8 and Reg9

1.2.10.4.2 Basic Configurations

NF can be easily configured to perform spatial-temporal filtering, spatial-only filtering, temporal-only filtering, or at by-pass mode. Table 1-66 shows how NF should be configured for each basic mode. Note that the temporal bypass mode here is mainly used for debug purpose, and it is not a true bypass mode.

Table 1-66. NF Configuration for Each Basic Mode

Register Name	Spatial-Temporal	Spatial Only	Temporal Only	Spatial Bypass	Temporal Bypass
nf_en	1	1	1	1	1
nf_ref_cfg	b'00	Any value, but preferred to set as b'10 or b'11 to disable DMA for reference frame	b'00	Any value, but preferred to set as b'10 or b'11 to disable DMA for reference frame	b'00
nf_bypass_cfg	b'00	b'00	b'00	b'01 (or b'11)	b'10
spatial_strength X 6			0		
temporal_strength		0			

1.2.11 Scaler (SC)

The scaler module is used to resize YCbCr422 video images.

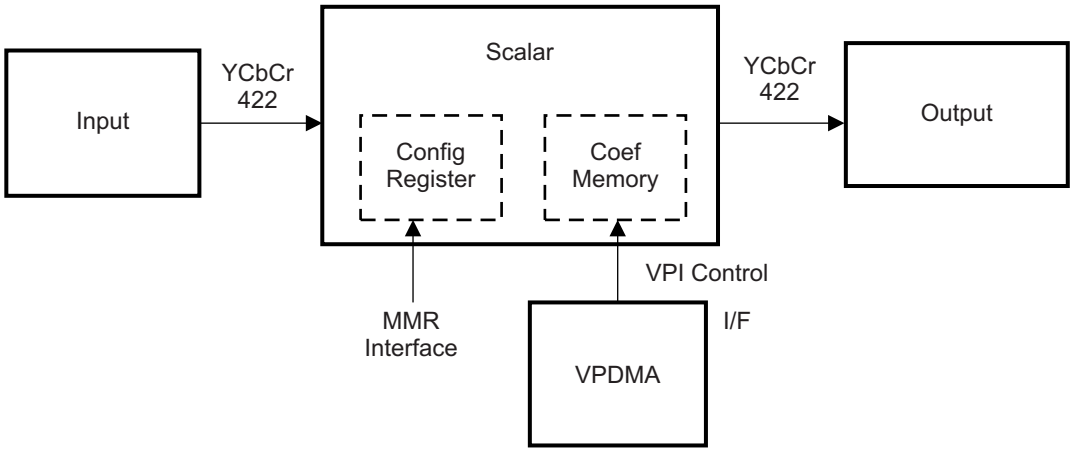
1.2.11.1 Features

- Independent vertical and horizontal up/down scaling
- Polyphase filter vertical up/down scaling
- Running average vertical down scaling for memory optimization
- Decimation and polyphase filtering for horizontal scaling
- Non-linear scaling for stretched/compressed left and right sides
- Input image trimmer for pan/scan support
- Pre-scaling peaking filter for enhanced sharpness
- Scale field as frame
- Interlacing of scaled output
- Full 1080p input and output support
- YCbCr422 input and output
- Maximum horizontal scaling ratio only limited by output line buffer (2047 pixels)
- Scaling filter Coefficient memory download via VPI (Video Port Interface) Control interface

1.2.11.2 Functional Description

Scaler takes in a 10-bit YCbCr 422 video frame from an upstream module, performs vertical/horizontal scaling, and outputs a YCbCr422 scaled image to a next downstream module. All configurations are done via the MMR interface except for the scaler coefficient memory configuration that is done via the common VPI control interface bus by VPDMA. Figure 1-139 shows the high level block diagram of the scaler module.

Figure 1-139. High Level Block Diagram

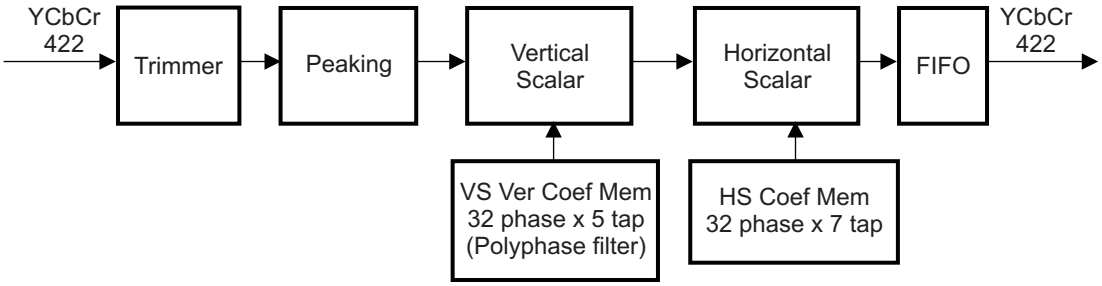


The SC (Figure 1-140) is used in the video path and in all other video write-back data paths in the HDVPSS module.

Scaling is performed in following three steps:

1. Trimming and Pre-peaking filtering
2. Vertical Scaling (Polyphase/Running Average Filter)
3. Horizontal polyphase scaling

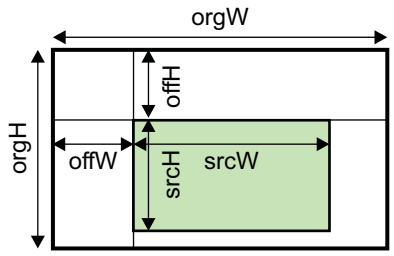
Figure 1-140. SC Block Diagram



1.2.11.2.1 Trimmer

The trimmer can be programmed to re-define a new source image within the input video frame sent from an upstream module before it is sent to the scaling sub-modules. This feature enables small area zoom out, source pan/scan, or removal of unwanted area in the video (such as black box/curtains/noisy line-21 video) without modifying the VPDMA parameters.

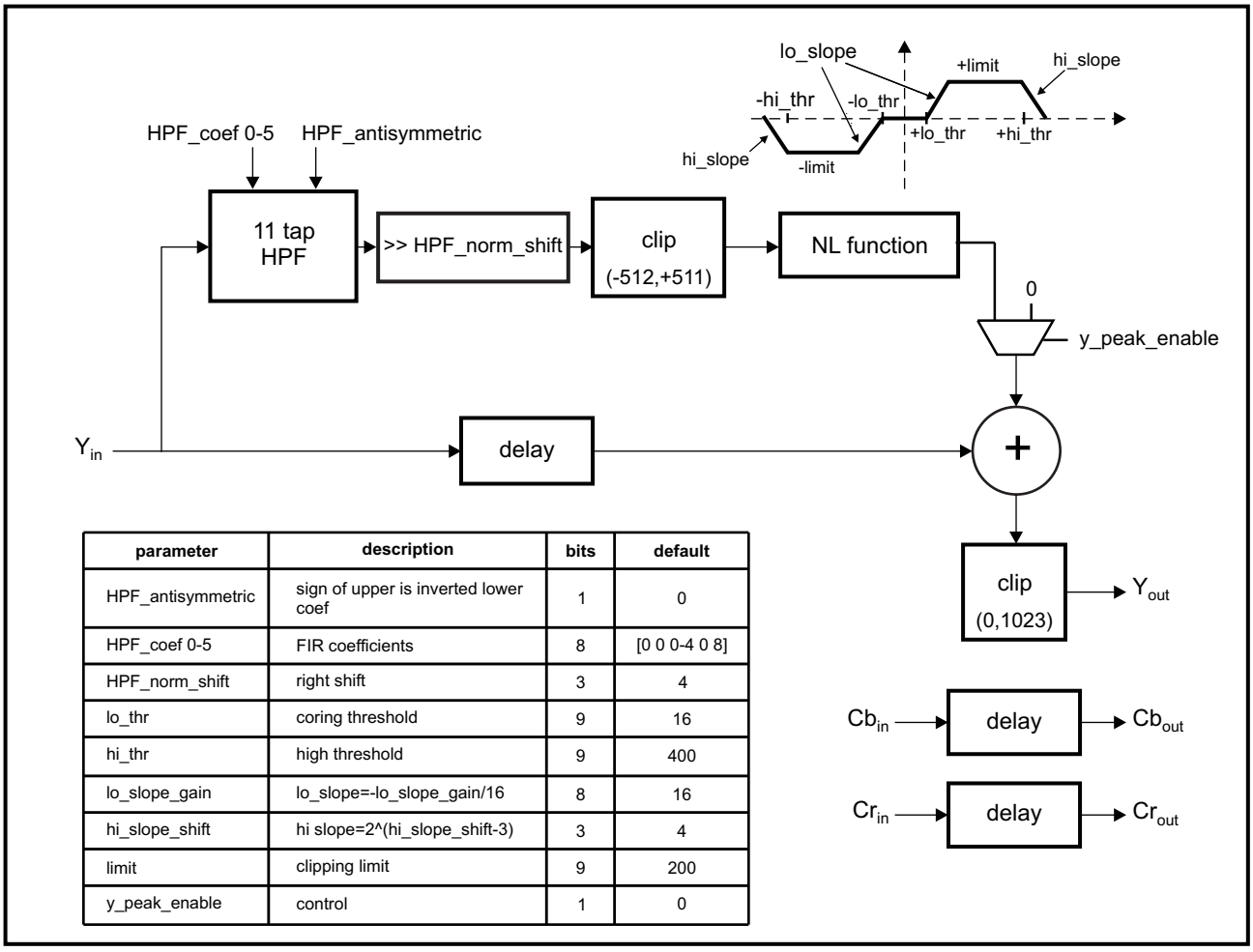
Figure 1-141. Input Image Trimming



1.2.11.2.2 Peaking

The peaking block increases the amplitude of high frequency luminance information in horizontal direction to increase the sharpness of a video image before it is scaled. As shown in Figure 1-142, the high-frequency luminance is increased using an 11-tap High-Pass filter with adjustable gain. The non-linear coring function removes low-level noise and the modified luminance is then added to the original luminance signal. The implementation details are shown in Figure 1-142.

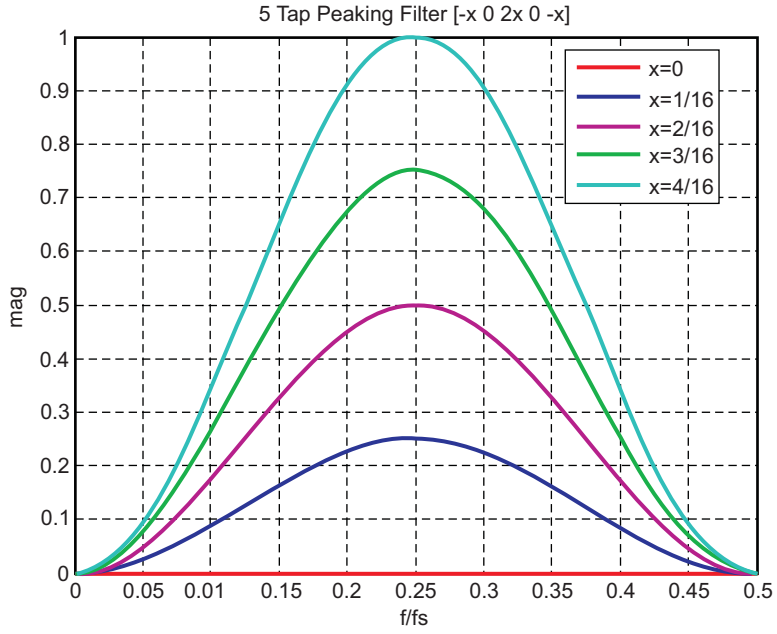
Figure 1-142. Filter Implementation and Parameter Description



parameter	description	bits	default
HPF_antisymmetric	sign of upper is inverted lower coef	1	0
HPF_coef 0-5	FIR coefficients	8	[0 0 0-4 0 8]
HPF_norm_shift	right shift	3	4
lo_thr	coring threshold	9	16
hi_thr	high threshold	9	400
lo_slope_gain	lo_slope=-lo_slope_gain/16	8	16
hi_slope_shift	hi slope=2^(hi_slope_shift-3)	3	4
limit	clipping limit	9	200
y_peak_enable	control	1	0

Parameters for the Peaking filters are defined in CFG_SC19-22. The frequency responses of the peaking-filter with different sets of coefficients are shown in Figure 1-143. If the source of the input video is NTSC or PAL format, the peaking filter can be configured to reject the color subcarrier frequency.

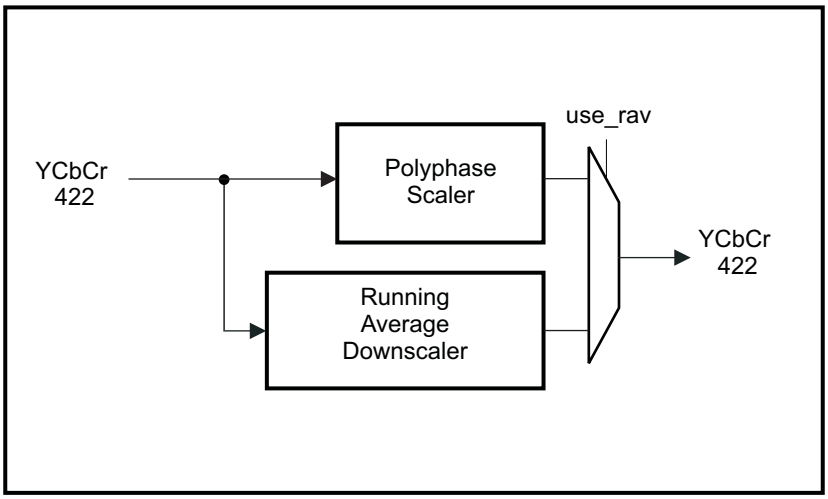
Figure 1-143. Peaking Filter at fs/4



1.2.11.2.3 Vertical Scaler

The vertical scaler has a poly-phase and a running average filter as shown in Figure 1-144. While the poly-phase filter can be used for any up-scaling and preferably downscaling to 3/16 scale factor, the running average filter is used only for downscaling to a ½ or less size. Selection between these two scalers is based on the user setting of “use_rav” parameter, according to the user preference of the tradeoff between sharpness preserving and introduced artifacts.

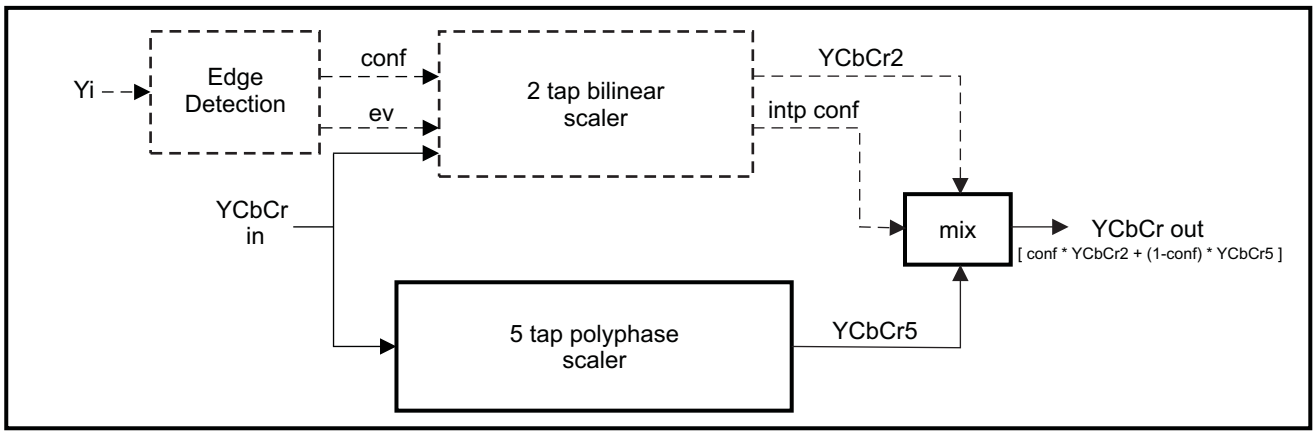
Figure 1-144. Vertical Scaler Block Diagram



1.2.11.2.3.1 Polyphase Scaler (in Vertical Scaler)

The vertical polyphase scaler is mainly implemented using a 32-phase 5-tap polyphase filter.

Figure 1-145. Mixed 2-tap and 5-tap vertical interpolation

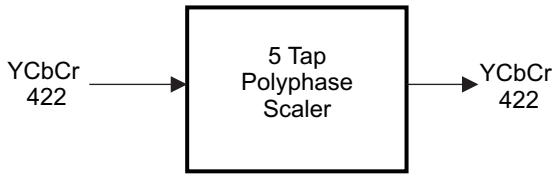


NOTE: In SC_M modules present in this device, edge detection and 2-tap bilinear filter modules are not available.

1.2.11.2.3.1.1 Polyphase Filter Selection

The scaler (SC) uses 5-tap polyphase filtering for vertical up-scaling.

Figure 1-146. Vertical Polyphase Scaler Block Diagram (SC)



1.2.11.2.3.2 Running Average Filter

When a poly-phase filter is used, usually it has to have many taps in order to achieve acceptable quality for very small downscaling ratio, which requires the use of many line buffers. In HDVPSS, we have a weighted Running Average filter for downscaling when the scaling factor is small (for example, when the scaling ratio is less than 0.5). This highly optimized design requires only one line buffer for luma and one for chroma, which still achieving acceptable quality. The output of the running average filter is based on weighted average of pixels in the current and previous rows in vertical direction. Initializations of accumulators affect the weights.

1.2.11.2.3.3 Vertical Scaler Configuration Parameters

Table 1-67. Vertical Scaler Configuration Parameters

Parameter	Bits	Typical	Controls	Description
interlace_in	1		Frame or Field	0 = progressive, 1 = interlace
interlace_out	1			0 = progressive 1 = interlace
invt_fid	1			Invert field ID input
use_rav	1		Scaler Mode	0 = use polyphase scaler 1 = use running average scaler
row_acc_inc	11.16		Bilinear & Polyphase Scalers	round(2^16*(srcH)/(tarH))
row_acc_offset	11.16	0		Initial row accumulator value for progressive frame and top field
row_acc_offset_b	11.16	0		Initial row accumulator value for bottom field
ev_thr	3.2	0xC	Bilinear Scaler	Edge vector threshold used in luma soft switch
delta_ev_thr	4	1		Range of luma soft switch based on edge vector
delta_luma_thr	4	4		Range for luma soft switch based on pixel differences (max limit = 8)
delta_chroma_thr	4	4		Range for chroma soft switch based on pixel differences (max limit = 8)
chroma_intp_thr	10	64		Threshold used in chroma soft switch based on pixel differences
luma polyphase filter coefficients	s1.11			32 phases × 7 taps × 13 bits array (interpolation only: scale factor = 1)
chroma polyphase filter coefficients	s1.11			32 phases × 7 taps × 13 bits array (interpolation only: scale factor = 1)
sc_factor_rav	10		Running Average Scaler	Scale factor = round(1024 × tarH/srcH)
row_acc_init_rav	10			Initial row accumulator value for progressive frame and top field
row_acc_init_rav_b	10			Initial row accumulator value for bottom field
luma polyphase filter coefficients	s1.11		Polyphase Scaler	32 phases × 5 taps × 13 bits array (dependent on scale factor)
chroma polyphase filter coefficients	s1.11			32 phases × 5 taps × 13 bits array (dependent on scale factor)

Note: Bi-linear scaler is not present in this device.

1.2.11.2.4 Horizontal Scaler

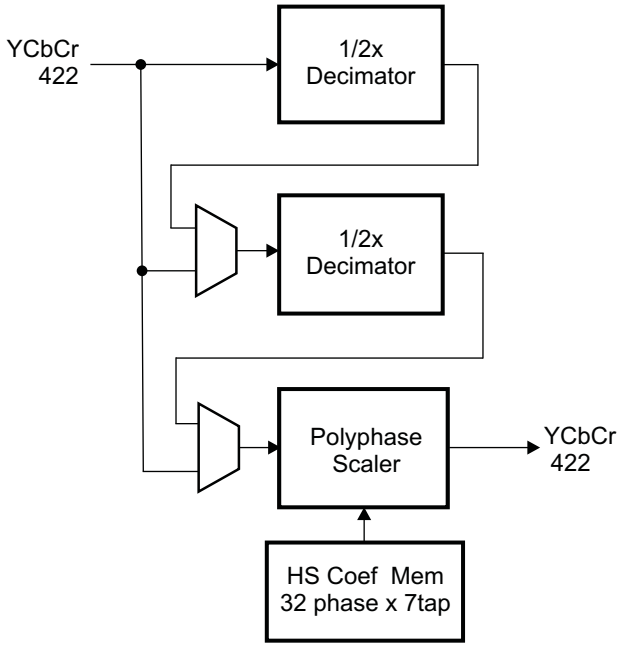
The horizontal scaler is implemented using a 32-phase × 7-tap polyphase filter preceded by two sets of x1/2 decimators. The general configuration of the Horizontal scaler is performed as follows:

- For up scaling, the input video is interpolated using the polyphase scaler.
- For downscaling, it is recommended that input video is decimated by 2 until the modified scale factor falls between 1/2 and 1. Then, a polyphase filter is configured with coefficients selected based on the mod_scale_factor calculated as shown below from one of nine different sets of coefficients: (8,9,10,11,12,13,14,15,16)/16.

```
if (scale_factor>=1/2) {
    dcm_2x=0;
    dcm_4x=0;
    mod_scale_factor=scale factor;
} else if (scale_factor>=1/4) {
    dcm_2x=1;
    dcm_4x=0;
    mod_scale_factor=2*scale_factor;
} else {
    dcm_2x=0;
    dcm_4x=1;
    mod_scale_factor=4*scale_factor;
}
```

In auto mode (auto_hs == 1), scaler will operate as per above recommendation. In addition to this, for (auto_hs==1), polyphase filtering will be bypassed when (scale_factor == 1) or (scale_factor == ½) or (scale_factor == ¼). If (auto_hs==0) is used, user must provide proper values for dcm_2x, dcm_4x, proper values for all inputs to polyphase filter in the registers as well as appropriate coefficient sets. There is no constraint on polyphase filtering in terms of scaling ratio. However, there are constraints on input and output image width for scaler. Frame dimensions are limited from 64x64 to 2047x2047.

Figure 1-147. Horizontal Scaler Block Diagram



1.2.11.2.4.1 Half Decimation Filter

The half-decimation filter is an 11-tap filter with following coefficients – (14, 0, -29, 0, 79, 128, 79, 0, -29, 0, 14). For processing left and right edge pixels, the first and last data are repeated to pre-fill and extend the filter data pipeline respectively.

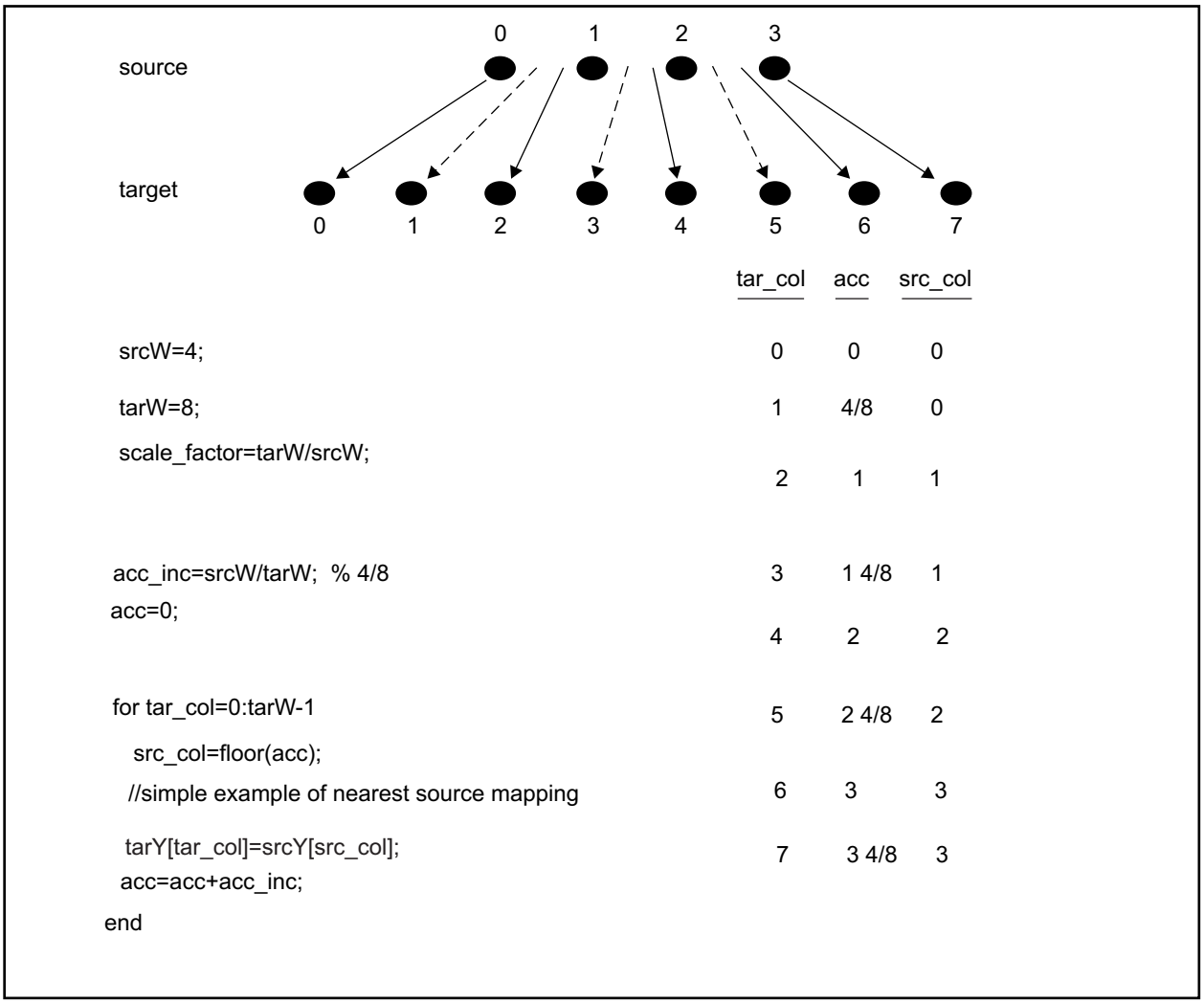
These coefficients are hard-coded into scaler design and user cannot modify these.

1.2.11.2.4.2 Polyphase Filter

The horizontal scaling is done by stepping across the target row and interpolating target pixels based on source pixels. Accumulator points to the source pixel that corresponds to the target pixel.

Figure 1-148 shows an up-scaling example.

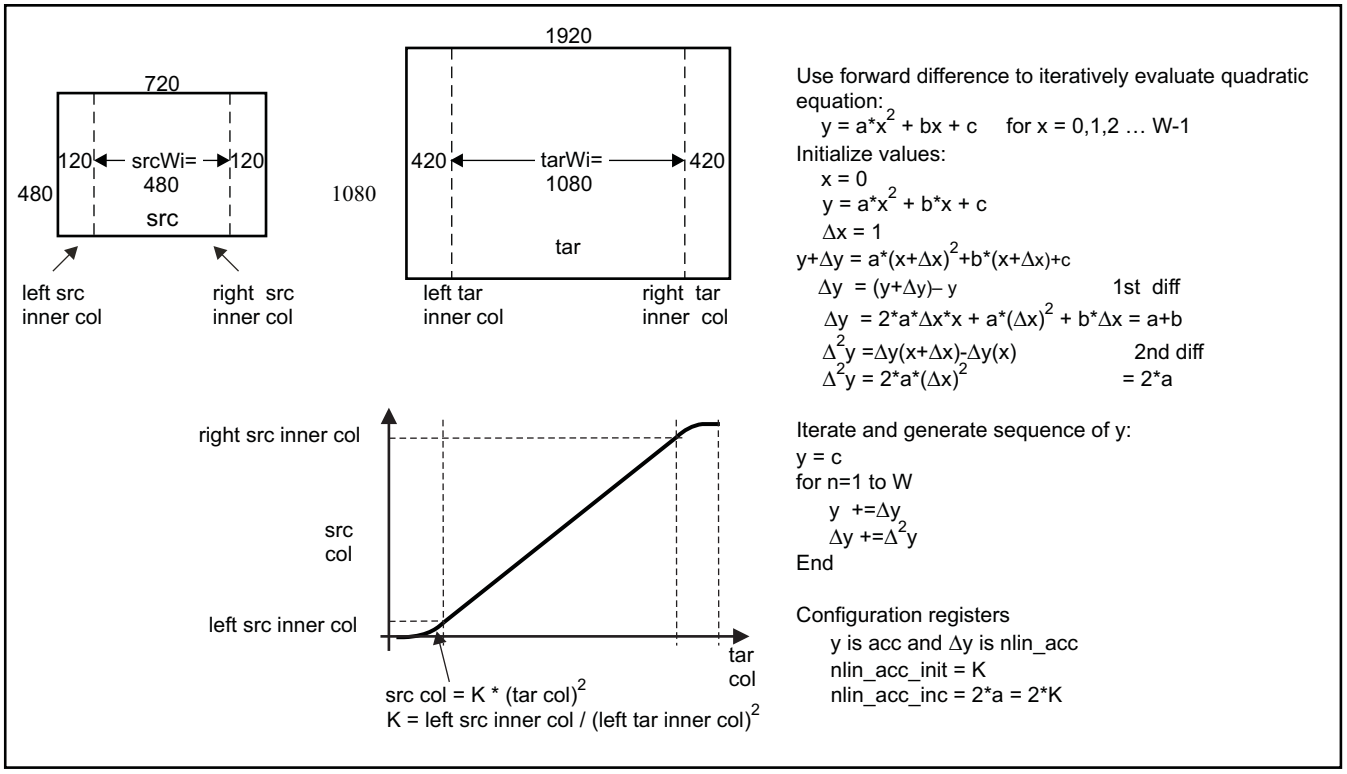
Figure 1-148. Polyphase Filtering Example



1.2.11.2.4.3 Nonlinear Horizontal Scaling

The horizontal scaler supports non-linear scaling to maintain the same aspect ratio for inner picture while stretching picture edges to fill the screen when displaying a 4x3 picture onto a 16x9 display. When setting up a non-linear scaling application, the inner picture is defined as the center square portion of the image with width and height equal to the height of the source image. Remaining side regions are then scaled non-linearly. Figure 1-149 shows a non-linear scaling case:

Figure 1-149. Non-linear Scaling Example



1.2.11.2.4.4 Horizontal Scaler Configuration Registers

Table 1-68. Horizontal Scaler Related Parameter Configuration

Parameter	Bits	Controls	Description			
srcW	11	Image Dimension	Source Width			
tarW	11		Target Width			
linear	1	Scaler Mode	If (linear == 1) srcWi=srcW and tarWi=tarW Else srcWi=srcH and tarWi=tarH			
sc_bypass	1		0 = enable scaler, 1 = bypass scaler			
auto_hs	1		Auto_hs	dcm_2x	dcm_4x	Definition
			0	0	0	Polyphase scaling
dcm_2x	1		0	0	1	Horizontal decimation by 4 and polyphase scaling
			0	1	0	Horizontal decimation by 4 and polyphase scaling
dcm_4x			1	-	-	Automatic (selection of decimation filter is automatic)

Table 1-69. Horizontal Decimation Selection

Scale Factor	Decimation
< ¼	By 4
< 1/4	By 4
== 1/4	By 4
1/4 < and < 1/2	By 2
1/2	By 2
1/2 < and < 1	Bypassed
1	Bypassed
> 1	Bypassed

Table 1-70. Horizontal Polyphase Filter Related Parameter Configuration

Parameter	Bits	Controls	Description
lin_acc_inc	11.24	Polyphase Scaler	if upscaling then lin_acc inc = round(2^24*(srcWi)/(tarWi)) elseif downscaling lin_acc inc = round(2^24*(srcWi/n)/(tarWi)) where n=1 when (cfg_dcm_2x == 0 && cfg_dcm_4x == 0) n=2 when (cfg_dcm_2x == 1 && cfg_dcm_4x == 0) n=4 when (cfg_dcm_2x == 0 && cfg_dcm_4x == 1)
nlin_left (Ltar)	11		if linear==1 nlin_right = tarW-1 else nlin_right = Ltar + tarWi – 1
nlin_right (Rtar)	11		if linear==1 nlin_left = 0

nlin_acc_inc	11.24		if tarW/srcW>=1 then
			d = 0
			if Ltar!=0 K = round[2^24*Lsrc/(Ltar*Ltar)] where Lsrc= (srcW-srcWi)/2
			else K = 0
			else
			d = (tarW-1)/2
			if Ltar!=0 K = round[2^24 * Lsrc / (Ltar*(Ltar-2d))]
			where Lsrc= (srcW-srcWi)/(2n) and n=1,2 or 4
			else K = 0
			nlin_acc_inc = 2*K (negative for downscaling)

nlin_acc_int	11.24		nlin_acc_init = K*(1-2*d)
luma polyphase filter coefficients	s1.11		32 phases × 7 taps × 13 bits array
chroma polyphase coefficients	s1.11		32 phases × 7 taps × 13 bits array

Note: Source width and height variables for the polyphase filter are internally set with trimmer and decimation filter adjusted values.

1.2.11.2.5 Coefficient Memory

1.2.11.2.5.1 Overview

The scaler requires initialization of eight coefficient SRAMS prior to processing a video frame. These coefficients are stored in the external DDR memories and downloaded by the VPDMA. The VPDMA writes the coefficient data through the VPI Control Interface bus.

The eight coefficient SRAMs are:

- HS horizontal polyphase scaler, Luma and Chroma (7tap)
- VS vertical polyphase scaler, Luma and Chroma (5tap or 3tap)
- VS vertical bilinear scaler, top line Luma and Chroma (7tap)
- VS vertical bilinear scaler, bottom line Luma and Chroma (7tap)

Only the SC_H requires the VS vertical bilinear scaler coefficients and has the memories to store them. Nevertheless, SC will accept the VPI Write command to these memories although it does not store the data.

1.2.11.2.5.2 Physical Coefficient SRAM Layout

Each of the six legacy coefficient SRAMs is 32 phases × 91 bits. A single coefficient value is 13 bits. Therefore, one word of the SRAM contains 7 coefficient values as shown in Figure 1-150, and 224 coefficient values are stored in each SRAM.

Figure 1-150. SRAM Layout for 7tap Coefficient

Phase 0	C6	C5	C4	C3	C2	C1	C0
Phase 31	C223	C222	C221	C220	C219	C218	C217

The two vertical polyphase SRAMs are 32 phases × 65 bits. A single coefficient is 13 bits. Therefore, one word of SRAM contains 5 coefficient values as shown in Figure 1-151.

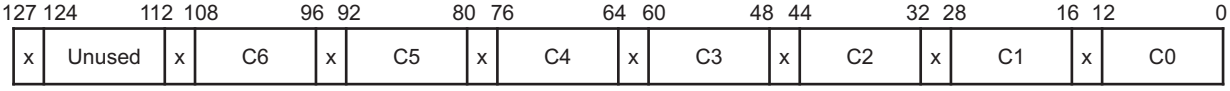
Figure 1-151. SRAM Layout for 5tap Coefficient

Phase 0	C4	C3	C2	C1	C0
Phase 31	C221	C220	C219	C218	C217

1.2.11.2.5.3 Scaler Coefficients Packing on 128-bit VPI Control I/F

A coefficient value is 13 bits wide and takes a single half word. Thus, one VPI Control write carries one phase's worth of coefficients. The last half-word in a quad-word is not used for 7tap coefficients.

Figure 1-152. VPI Control I/F Coef Data Format (7tap)



The Vertical Polyphase scaler coefficients have only five or three values per phase, so the last three (or five) entries are unused. The Vertical Polyphase coefficient packing is shown in Figure 1-153 and Figure 1-154.

Figure 1-153. VPI Control I/F Coef Data Format (5tap)

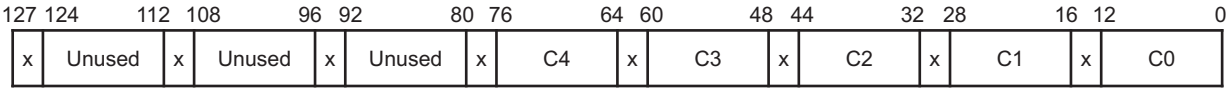
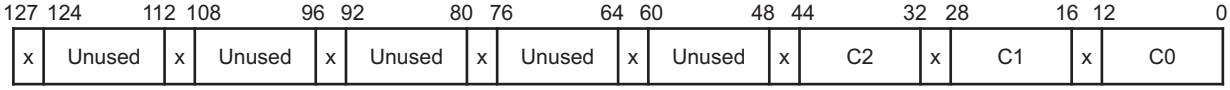


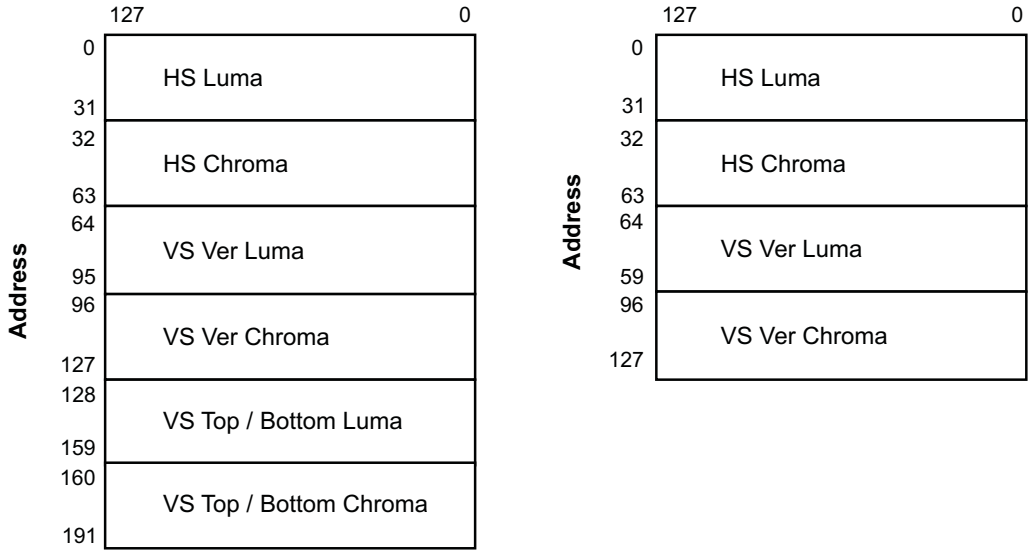
Figure 1-154. VPI Control I/F Coef Data Format (3tap)



1.2.11.2.5.4 VPI Control I/F Memory Map for Scaler Coefficients

The memory map of the VPI Control I/F for the Scaler coefficients is shown in Figure 1-155. All coefficients can be filled up by a single VPI Control write command. The update address feature of VPI Control I/F enables individual access to a certain location of memories. The VS top and bottom coefficients of SC_H are written concurrently through VPI Control Write.

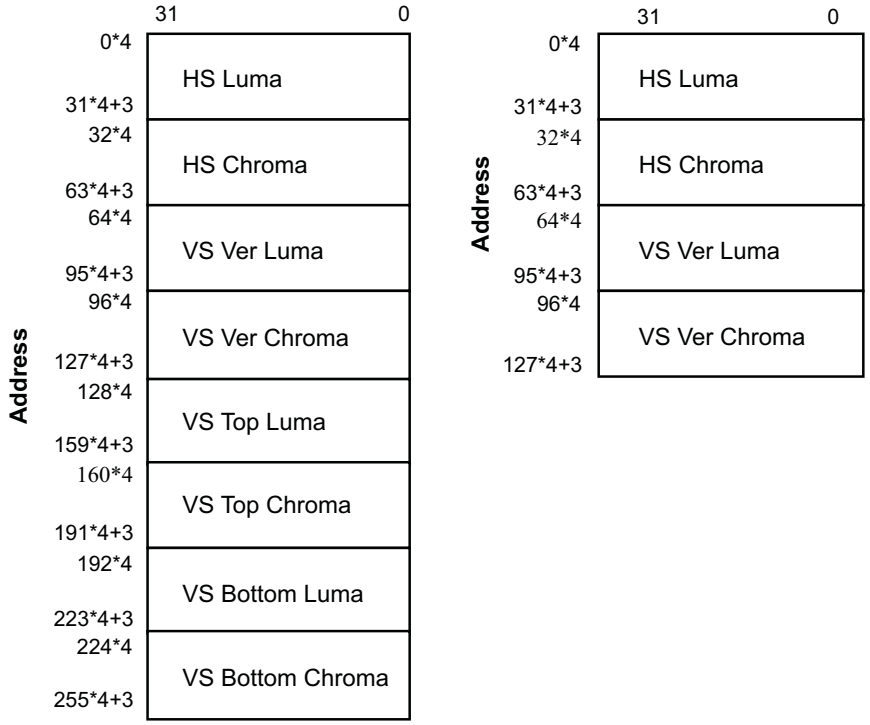
Figure 1-155. VPI Control I/F Memory Map (Write)



(a) sc_h **(b) sc_m**

The module supports the VPI Control Read to read back the contents in the coefficient memories for debug purpose. Figure 1-156 shows the memory map of the VPI Control Read. As the VPI Control Read has only 32 bit data bus, it requires the word addressing while the write does the quad-word addressing. The VS top and bottom coefficients can be accessed separately for the read.

Figure 1-156. VPI Control I/F Memory Map (Read)



1.2.11.2.5.5 VPI Control Interface

VPDMA is used to configure the coefficient memories of scaler through VPI control interface. Since the coefficient memories are not shadowed (unlike the MMR registers), VPI control write access needs to be done only during the gap between video frame processing times. If a write request is made while the Scaler is active, the access will be held off by the hardware until the last data of the currently processed frame is sent out. Care must be given to the order of the DMA descriptors so that blocking of VPI control bus does not occur.

1.2.11.2.5.6 Coefficient Table Selection Guide

The scaler filter coefficient tables are pre-generated using a Matlab program for various scaling factor ranges. Table 1-71 is a general selection guide table for coefficient data files.

Table 1-71. Coefficient Data Files

Scaler	Scale Factor	Coeff table
HS Polyphase Filter	All upscaling	ppfcoef_scale_eq_1_32_phases_flip.dat
HS Polyphase Filter	All upscaling	ppfcoef_scale_eq_1_32_hases_flip.dat
	½ or ¼ down scaling	ppfcoef_scale_eq_1_32_phases_flip.dat
	> 15/16	ppfcoef_scale_eq_15div16_32_phases_flip.dat
	> 14/16	ppfcoef_scale_eq_14div16_32_phases_flip.dat
	> 13/16	ppfcoef_scale_eq_13div16_32_phases_flip.dat
	> 12/16	ppfcoef_scale_eq_12div16_32_phases_flip.dat
	> 11/16	ppfcoef_scale_eq_11div16_32_phases_flip.dat
	> 10/16	ppfcoef_scale_eq_10div16_32_phases_flip.dat
	> 9/16	ppfcoef_scale_eq_9div16_32_phases_flip.dat
	> 8/16	ppfcoef_scale_eq_8div16_32_phases_flip.dat(1)
VS Polyphase Filter	Upscaling	ppfcoef_scale_eq_1_32_phases_ver_5tap_flip.dat
	> 15/16	ppfcoef_scale_eq_15div16_32_phases_ver_5tap_flip.dat
	> 14/16	ppfcoef_scale_eq_14div16_32_phases_ver_5tap_flip.dat
	> 13/16	ppfcoef_scale_eq_13div16_32_phases_ver_5tap_flip.dat
	> 12/16	ppfcoef_scale_eq_12div16_32_phases_ver_5tap_flip.dat
	> 11/16	ppfcoef_scale_eq_11div16_32_phases_ver_5tap_flip.dat
	> 10/16	ppfcoef_scale_eq_10div16_32_phases_ver_5tap_flip.dat
	> 9/16	ppfcoef_scale_eq_9div16_32_phases_ver_5tap_flip.dat
	> 8/16	ppfcoef_scale_eq_8div16_32_phases_ver_5tap_flip.dat
	else	For down-scaling <8/16, RAV filter is recommended. In this case, coefficients for vertical scaling need not be loaded.

(1) HS Scaler has two sets of ½-decimator to perform downscaling ratios below ½ and ¼.

The above mentioned .dat files are available in Section 1.2.11.4.

1.2.11.3 Code

1.2.11.3.1 Generate Coefficient Memory Image

The following Perl script is used to generate a coefficient memory image for a given set of scaling factors.

```
#!/usr/local/bin/perl

#$dir="coef/";                    # directory which contains the coef files
#$cfg_file="sc_config1.cfg";      # configuration file name
#$spl_file="sc_config_supl.cfg";  # supplemental configuration file name $cfg_file=$ARGV[0];  #
configuration file name $spl_file=$ARGV[1];  # supplemental configuration file name
$dir=$ARGV[2];       # directory which contains the coef files

$coef_width=13;  # coef bit width
$coef_ntap=7;    # coef tap
$coef_nphase=32; # coef phase
$coef_norm=11;   # coef norm

#-----------------------------------------------------------
# read config file to get srcH/tarH/interlace_i/interlace_o
#-----------------------------------------------------------
open(INFILE, "<$cfg_file") or die "### ERROR: Cannot open $cfg_file";
```

```
while(<INFILE>){
  if (m/([-0-9]+) +\/\/ +srcW/) {
    $srcW = $1;
  } elsif (m/([-0-9]+) +\/\/ +srcH/) {
    $srcH = $1;
  } elsif (m/([-0-9]+) +\/\/ +tarW/) {
    $tarW = $1;
  } elsif (m/([-0-9]+) +\/\/ +tarH/) {
    $tarH = $1;
  } elsif (m/([-0-9]+) +\/\/ +interlace_in/) {
    $interlace_i = $1;
  } elsif (m/([-0-9]+) +\/\/ +interlace_out/) {
    $interlace_o = $1;
}
}
close(INFILE);

#-------------------------------------------------------------
# read supplemental config file to get srcWi/tarWi from
#-------------------------------------------------------------
open(INFILE,"<$spl_file") or die "### ERROR: Cannot open $spl_file";
while(<INFILE>){
  if (m/([-0-9]+) +\/\/ +srcWi/) {
    $srcWi = $1;
  } elsif (m/([-0-9]+) +\/\/ +tarWi/) {
    $tarWi = $1;
  } elsif (m/([-0-9]+) +\/\/ +profile/) {
    $profile = $1; # 0:HIGH,1:MEDIUM,2:LOW
  }
}
close(INFILE);
#-------------------------------------------------------------
# determine coef file based on the width/height
#-------------------------------------------------------------
# VS
#$vsc_file0 = "mod_ppfcoef_scale_eq_1_32_phases_flip.dat";
$vsc_file0 = "ppfcoef_scale_eq_1_32_phases_flip_PPF3_peak5_gain_eq_1_25.dat";
# VS VER
$mod_tarH = ($interlace_i == 0 && $interlace_o == 1) ? $tarH<<1 : $tarH; if ($profile==2) {
  # LOW profile
  if ($mod_tarH >= $srcH) {
    $vsc_ver_file0 = "ppfcoef_scale_eq_1_32_phases_ver_3tap_flip.dat";
} else {
    if ($mod_tarH >=($srcH>>1)) {
      $n = int(16.0*$mod_tarH/$srcH);
      $vsc_ver_file0 = sprintf("ppfcoef_scale_eq_%ddiv16_32_phases_ver_3tap_flip.dat",$n);
    } else {
      $n = 0;
      $vsc_ver_file0 = "ppfcoef_scale_eq_1_32_phases_ver_3tap_flip.dat";
    }
  }
} else {
  if ($mod_tarH >= $srcH) {
    $vsc_ver_file0 = "ppfcoef_scale_eq_1_32_phases_ver_5tap_flip.dat";
  } else {
      $n = int(16.0*$mod_tarH/$srcH);
      $vsc_ver_file0 = sprintf("ppfcoef_scale_eq_%ddiv16_32_phases_ver_5tap_flip.dat",$n);
  }
}

# HS
if ($tarWi >= $srcWi) {
  $hsc_file0 = "ppfcoef_scale_eq_1_32_phases_flip.dat";
} elsif ( ($tarWi == ($srcWi>>1)) || ($tarWi == ($srcWi>>2)) ) {
  $hsc_file0 = "ppfcoef_scale_eq_1_32_phases_flip.dat";
} else {
```

```
if ($tarWi > ($srcWi>>1)) {
    $n = int(16.0*$tarWi/$srcWi);
  } elsif ($tarWi > ($srcWi>>2)) {
    $n = int(16.0*$tarWi/($srcWi>>1));
  } elsif ($tarWi >=($srcWi>>3)) {
    $n = int(16.0*$tarWi/($srcWi>>2));
  } else {
    $n = 0;
  }
  $hsc_file0 = sprintf("ppfcoef_scale_eq_%ddiv16_32_phases_flip.dat",$n);
}
#-----------------------------------------------------------
# write out the coef hex file
#-----------------------------------------------------------
&write_coef($hsc_file0);
&write_coef($hsc_file0);
&write_coef($vsc_ver_file0);
&write_coef($vsc_ver_file0);
&write_coef($vsc_file0);
&write_coef($vsc_file0);
sub write_coef {

  my ($filename) = @_;

  open(INFILE, "<$dir/$filename") or die "### ERROR: Cannot open $dir/$filename";

  $line=<INFILE>;
@val=split(' ',$line);
  $ntap=$val[0];
  $nphase=$val[1];
  $norm=$val[2];
for ($p=0;$p<$nphase;$p++) {
    $line=<INFILE>;@val=split(' ',$line);
    for($i=0;$i<$ntap;$i++) {
      if ($val[$i]<0) {
        $val[$i]+=(1<<$coef_width);
      }
    }
    undef(@coef);
    unshift(@coef, sprintf("%04x",$val[0]));
    unshift(@coef, sprintf("%04x",$val[1]));
    unshift(@coef, sprintf("%04x",$val[2]));
    unshift(@coef, sprintf("%04x",$val[3]));
    unshift(@coef, sprintf("%04x",$val[4]));
    unshift(@coef, sprintf("%04x",$val[5]));
    unshift(@coef, sprintf("%04x",$val[6]));
    unshift(@coef, sprintf("%04x",0));
    $coef=join("",@coef);
    print "$coef\n";
  }

  close(INFILE);
}
```

1.2.11.3.2 Scaler Configuration Calculation

The following C-code shows how configuration parameters are calculated:

```
// ======================================
// Required Input Parameter
// ======================================
//   srcW, srcH, tarW, tarH, srcWi, tarWi
//   input/output scan modes


pixel_scale_factor=4;  // 10 bit pixel
hor_pixel_offset =0.0

  // ============================================================================================
  // Peaking Filter Configuration
  // ============================================================================================
  // ------------------------------------------------------------
  // HPF Coef
  // ------------------------------------------------------------
    y_peak_enable     =   0;

    peak_select=0; // 0=peak at fs/4  1=NTSC  2=PAL
    switch(peak_select) {
    case 0: {// peak at fs/4 and gain = 1
             HPF_coef0         =   0;
             HPF_coef1         =   0;
             HPF_coef2         =   0;
             HPF_coef3         =  -4;
             HPF_coef4         =   0;
             HPF_coef5         =   8; // mid tap
             HPF_norm_shift    =   4;
         break;
}
    case 1: {// NTSC: peak at 0.133*fs and gain=1
             HPF_coef0         =  -2;
             HPF_coef1         =  -8;
             HPF_coef2         =  -8;
             HPF_coef3         =  -2;
             HPF_coef4         =  12;
             HPF_coef5         =  16; // mid tap
             HPF_norm_shift    =   6;
             break;
    }
    case 2: {// PAL: peak at 0.163*fs and gain=1
             HPF_coef0         =   2;
             HPF_coef1         =  -4;
             HPF_coef2         = -11;
             HPF_coef3         =  -7;
             HPF_coef4         =   9;
             HPF_coef5         =  22; // mid tap
             HPF_norm_shift    =   6;
             break;
    }
    }

  // ------------------------------------------------------------
  // NonLinear Coring Function typical values
  // ------------------------------------------------------------
    NL_coring_thr     =  16;
    NL_limit          = 200;
    NL_lo_slope       =  16;
    NL_hi_thr         = 400;
    NL_hi_slope_shift =   4;
```

```
  // ================================================================================================
  // Edge Detection Configuration
  // ================================================================================================
    // edge detection
    confidence_default = 0; // 0  =use 5 tap polyphase filter for SC or sc_h with ev_enable =0

    min_Gy_thr         =  64; // 64
    min_Gy_thr_range   =   3; // 3 power of 2
    gradient_thr       = 200; // 200
gradient_thr_range =   6; // 6 power of 2

    ev_thr = int(4.0*3.111+0.5); // edge vector soft switch threshold (3.2)


// ============================================================================
// vertical scaler configuration
// ============================================================================
//srcH/tarH is field height for interlaced data //srcH/tarH is frame height for progressive data

// ----------------------------------------------------------------
// vertical scaler typical parameters
// ----------------------------------------------------------------
invert_field_ID  = 0;   // invert field ID input
ver_pixel_offset = 0.0; // User may modify this is required
uv_intp_thr      = pixel_scale_factor*16;
delta_y_thr      = 4;   // luma soft switch range
delta_uv_thr     = 4;   // chroma soft switch range

// ----------------------------------------------------------------
// Vertical Scaler Mode Determination
// ----------------------------------------------------------------
if((interlace_in == 0) && (interlace_out == 1)) {
    if(2*tarH > (srcH/2))
        use_rav = 0;  // 1=use RAV scaler 0=use polyphase scaler
    else
        use_rav = 1;
}
else
{
    if(tarH > (srcH/2))
        use_rav = 0;  // 1=use RAV scaler 0=use polyphase scaler
    else
        use_rav = 1;
}

// ----------------------------------------------------------------
// RAV or Polyphase parameters
// ----------------------------------------------------------------
if(use_rav) // downscale only
{
    // ------------
    // --- RAV ----
    // ------------
    if(use_internal_defaults)
        enable_edge_detection = 0;

    if((interlace_in == 0) && (interlace_out == 1))
    {
        scale = double(2*tarH)/double(srcH);
    }
    else
    {
        scale = double(tarH)/double(srcH);
    }
    sc_factor_rav = int(1024.0*scale+0.5);
```

```
    // Peter's method
    delta = (1.0/scale-1.0)/2.0;
    int_part         = floor(delta);
    frac_part        = delta-int_part;
    row_acc_init_rav = int(1024*(scale+(1.0-scale)/2.0)+0.5); // top field

    // bottom field
    tmp1 = (1.0-2.0*frac_part);
    tmp2 = (1.0- (1.0+2.0*int_part)*scale);
    row_acc_init_b_rav = int(1024*(scale + tmp1*tmp2/2.0) + 0.5);

    row_acc_inc      = 0; // polyphasescaler
    row_acc_offset   = 0; // polyphasescaler
    row_acc_offset_b = 0; // polyphasescaler } else {
    //upscale using polyphase scaler
    // ------------
    // --- PPF ----
    // ------------
    if(use_internal_defaults)
        enable_edge_detection = 1;
    sc_factor_rav      = 0;
    delta_rav          = 0;
    row_acc_init_rav   = 0;
    row_acc_init_b_rav = 0;

    // progressive or top field
    row_acc_offset = int(65536.0*ver_pixel_offset +0.5);
    row_acc_inc    = int(65536.0*double(srcH)/double(tarH)+0.5);

    //bottom field
    if((interlace_in == 1) ampamp (interlace_out == 0))
    {
        if((-0.5+row_acc_offset) < 0.0)
            round_factor = -0.5;
        else
            round_factor = 0.5;
        row_acc_offset_b = int(65536.0*(-0.5)+round_factor)+row_acc_offset;
    }
    if((interlace_in == 0) && (interlace_out == 1))
    {
        row_acc_offset_b =
            int(65536.0*double(srcH)/double(tarH)+0.5)+row_acc_offset;
    }
    if((interlace_in == 1) ampamp (interlace_out == 1))
    {
        row_acc_offset_b =
            (int(65536.0/2.0*(double(srcH)/(double(tarH))-1.0)+0.5))+
            row_acc_offset;
    }
}


// ================================================================================================
  // Horizontal Scaler configuration
  // ================================================================================================
  // ----------------------------------------------------------------
  // horizontal scaler mode determination
  // ----------------------------------------------------------------
  auto_hs                = 1;
  dcm_2x                 = 0;
  dcm_4x                 = 0;
  hp_bypass              = 0;
  if (srcWi==srcW) linear = 1;
  else             linear = 0;

  // hor scaler parameters
```

```
  if (tarW>srcW) {              // upscale
    mod_srcW  = srcW;
    mod_srcWi = srcWi;
} else if (tarW<=(srcW>>2)) {  // downscale by <=1/4
    mod_srcW  = srcW>>2;
    mod_srcWi = srcWi>>2;
  } else if (tarW<=(srcW>>1)) {  // downscale by <=1/2
    mod_srcW  = srcW>>1;
    mod_srcWi = srcWi>>1;
  } else {                      // downscale by <=1
    mod_srcW  = srcW;
    mod_srcWi = srcWi;
  }

  // Not used any more:
  // hs_factor       = int(16.0*double(tarWi)/double(mod_srcWi)+0.5);  // hor scale factor (6.4)

  // ---------------------------------------------------------------
  // Horizontal PolyPhase Settings  --
  // ---------------------------------------------------------------
  lin_acc_inc     = int(16777216.0*double(mod_srcWi-1)/double(tarWi-1)+0.5);
  col_acc_offset  = int(16777216.0*hor_pixel_offset +0.5);
  nlin_left       = (tarW-tarWi)>>1;
  nlin_right      = nlin_left+tarWi-1;
  if (linear) {
    nlin_acc_inc    = 0;
    nlin_acc_init   = 0;
  } else {
     // ---------------------------------
     // Non-linear scaling configuration
     // ---------------------------------
    nlin_left_src   = (mod_srcW-mod_srcWi)>>1;

       if (tarWi>=srcWi) {    // upscale
      d             =  0.0;
      round_factor  =  0.5;
       } else {                 // downscale
      d             = (double(tarW)-1.0)/2.0;
      round_factor  = -0.5;
    }

      K             = 16777216.0*double(nlin_left_src)/(double(nlin_left)*double(nlin_left-
2.0*d));
    nlin_acc_inc  = int(2.0*K+round_factor);
    nlin_acc_init = int(K*(1.0-2.0*d)+0.5);
  }
nlin_left_tar  = nlin_left;
  nlin_right_tar = nlin_right;

  // ============================================================================================
  // Bypass Determination
  // ============================================================================================
  // bypass
  if ((srcW==tarW)&&(srcWi==tarWi)&&(mod_srcH==mod_tarH)) sc_bypass = 1;
  else                                                   sc_bypass = 0;
  //

}
```

1.2.11.3.3 Typical Configuration Values

The following is the list of all scaler register fields that are set to constant values by the software – representing typical settings:

CFG_SC0 : InvertFieldId = 0
CFG_SC0 : EnableEdgeDetection = 1
CFG_SC0 : AutoHorizontalScaling = 1
CFG_SC0 : Decimation2x = 0
CFG_SC0 : Decimation4x = 0
CFG_SC0 : EnableSin2VerticalInterpolation = 1
CFG_SC0 : EnableLumaPeaking = 0
CFG_SC0 : EnableTrimming= 1
CFG_SC12 : ColumnAccumulatorOffset = 0
CFG_SC13 : ChromaInterpolationThreshold = 64
CFG_SC13 : DeltaChromaThreshold = 4
CFG_SC17 : EdgeVectorThreshold = 12 (3.111 in 8.2 format)
CFG_SC17 : DeltaLumaThreshold = 4
CFG_SC17 : DeltaEdgeVectorThreshold = 1
CFG_SC18 : ConfidenceFactorDefault = 0x100
CFG_SC19 = 0xFC000000
CFG_SC20 = 0x0C840800
CFG_SC21 = 0x00100010
CFG_SC22 = 0x00040190

1.2.11.4 Coefficient Data Files

1.2.11.4.1 HS Polyphase Filter Coefficients

1.2.11.4.1.1 ppfcoef_scale_eq_1_32_phases_flip.dat

```
 7  32 11
31 -112  210 1790  210 -112   31
28  -98  159 1787  264 -126   34
25  -84  111 1779  320 -140   37
22  -71   65 1767  379 -154   40
19  -58   23 1750  439 -168   43
16  -45  -17 1728  502 -181   45
14  -33  -53 1701  565 -193   47
11  -22  -86 1670  631 -205   49
 9  -11 -116 1635  696 -216   51
 7   -1 -142 1594  763 -225   52
 5    8 -166 1551  830 -233   53
 3   16 -186 1504  898 -240   53
 2   23 -204 1455  965 -245   52
 1   30 -218 1401 1031 -248   51
 0   35 -230 1345 1097 -249   50
-1   40 -238 1286 1162 -248   47
44 -244 1224 1224 -244   44    0
47 -248 1162 1286 -238   40   -1
50 -249 1097 1345 -230   35    0
51 -248 1031 1401 -218   30    1
52 -245  965 1455 -204   23    2
53 -240  898 1504 -186   16    3
53 -233  830 1551 -166    8    5
52 -225  763 1594 -142   -1    7
51 -216  696 1635 -116  -11    9
49 -205  631 1670  -86  -22   11
47 -193  565 1701  -53  -33   14
```

```
  45 -181  502 1728  -17  -45   16
  43 -168  439 1750   23  -58   19
  40 -154  379 1767   65  -71   22
  37 -140  320 1779  111  -84   25
  34 -126  264 1787  159  -98   28
```

1.2.11.4.1.2 ppfcoef_scale_eq_8div16_32_phases_flip.dat

```
7  32 11
  -28   61  542  898  542   61  -28
  -27   52  523  899  560   70  -29
  -26   44  505  898  578   79  -30
  -25   37  487  895  595   89  -30
  -24   30  468  892  613  100  -31
  -22   23  450  887  630  111  -31
  -21   17  432  883  647  122  -32
  -20   11  414  877  664  134  -32
  -19    6  396  871  680  146  -32
  -18    1  378  864  695  159  -31
  -16   -4  360  856  711  172  -31
  -15   -8  343  847  726  185  -30
  -14  -12  325  838  740  200  -29
  -13  -15  308  828  754  214  -28
  -12  -18  292  816  768  229  -27
  -10  -21  275  805  780  244  -25
  -23  258  789  789  258  -23    0
  -25  244  780  805  275  -21  -10
  -27  229  768  816  292  -18  -12
  -28  214  754  828  308  -15  -13
  -29  200  740  838  325  -12  -14
  -30  185  726  847  343   -8  -15
  -31  172  711  856  360   -4  -16
  -31  159  695  864  378    1  -18
  -32  146  680  871  396    6  -19
  -32  134  664  877  414   11  -20
  -32  122  647  883  432   17  -21
  -31  111  630  887  450   23  -22
  -31  100  613  892  468   30  -24
  -30   89  595  895  487   37  -25
  -30   79  578  898  505   44  -26
  -29   70  560  899  523   52  -27
```

1.2.11.4.1.3 ppfcoef_scale_eq_9div16_32_phases_flip.dat

```
7  32 11
  -33    8  547 1004  547    8  -33
  -31    0  525 1003  570   16  -35
  -29   -7  503 1001  592   25  -37
  -27  -13  481  998  614   34  -39
  -26  -19  459  995  636   44  -41
  -24  -25  437  990  658   55  -43
  -22  -29  414  983  679   67  -44
  -20  -34  393  976  700   79  -46
  -18  -38  371  968  721   91  -47
  -17  -41  350  959  742  104  -49
  -15  -44  330  948  761  118  -50
  -13  -46  309  936  780  133  -51
  -12  -48  289  924  799  148  -52
  -11  -50  270  911  817  163  -52
   -9  -51  250  897  833  180  -52
   -8  -52  232  882  850  196  -52
  -52  213  863  863  213  -52    0
  -52  196  850  882  232  -52   -8
  -52  180  833  897  250  -51   -9
  -52  163  817  911  270  -50  -11
```

```
  -52  148  799  924  289  -48  -12
  -51  133  780  936  309  -46  -13
  -50  118  761  948  330  -44  -15
  -49  104  742  959  350  -41  -17
  -47   91  721  968  371  -38  -18
  -46   79  700  976  393  -34  -20
  -44   67  679  983  414  -29  -22
  -43   55  658  990  437  -25  -24
  -41   44  636  995  459  -19  -26
  -39   34  614  998  481  -13  -27
  -37   25  592 1001  503   -7  -29
  -35   16  570 1003  525    0  -31
```

1.2.11.4.1.4 ppfcoef_scale_eq_10div16_32_phases_flip.dat

```
7  32 11
  -30  -46  542 1116  542  -46  -30
  -28  -52  515 1115  570  -39  -33
  -25  -57  488 1113  597  -32  -36
  -23  -62  462 1109  624  -24  -38
  -20  -65  435 1104  650  -15  -41
  -18  -69  409 1097  678   -5  -44
  -16  -71  383 1089  704    6  -47
  -14  -74  358 1081  730   17  -50
  -12  -75  333 1070  756   29  -53
  -11  -76  309 1058  782   42  -56
   -9  -77  285 1045  806   56  -58
   -8  -77  262 1030  831   71  -61
   -6  -77  239 1015  855   86  -64
   -5  -76  218  997  877  103  -66
   -4  -75  196  980  899  120  -68
   -3  -74  176  961  920  138  -70
  -72  156  940  940  156  -72    0
  -70  138  920  961  176  -74   -3
  -68  120  899  980  196  -75   -4
  -66  103  877  997  218  -76   -5
  -64   86  855 1015  239  -77   -6
  -61   71  831 1030  262  -77   -8
  -58   56  806 1045  285  -77   -9
  -56   42  782 1058  309  -76  -11
  -53   29  756 1070  333  -75  -12
  -50   17  730 1081  358  -74  -14
  -47    6  704 1089  383  -71  -16
  -44   -5  678 1097  409  -69  -18
  -41  -15  650 1104  435  -65  -20
  -38  -24  624 1109  462  -62  -23
  -36  -32  597 1113  488  -57  -25
  -33  -39  570 1115  515  -52  -28
```

1.2.11.4.1.5 ppfcoef_scale_eq_11div16_32_phases_flip.dat

```
7  32 11
  -19  -94  522 1230  522  -94  -19
  -17  -98  490 1230  555  -90  -22
  -14 -100  458 1227  587  -85  -25
  -12 -102  427 1223  620  -79  -29
  -10 -103  397 1217  652  -73  -32
   -8 -104  367 1209  685  -65  -36
   -6 -104  337 1199  717  -56  -39
   -4 -103  309 1187  749  -47  -43
   -3 -102  281 1174  781  -36  -47
   -1 -100  253 1159  812  -24  -51
    0  -98  227 1142  843  -11  -55
    1  -96  201 1124  874    3  -59
    1  -93  177 1105  903   18  -63
```

```
   2  -90  153 1084  932   34  -67
   2  -87  131 1062  961   51  -72
   3  -83  109 1038  987   69  -75
 -79   89 1014 1014   89  -79    0
 -75   69  987 1038  109  -83    3
 -72   51  961 1062  131  -87    2
 -67   34  932 1084  153  -90    2
 -63   18  903 1105  177  -93    1
 -59    3  874 1124  201  -96    1
 -55  -11  843 1142  227  -98    0
 -51  -24  812 1159  253 -100   -1
 -47  -36  781 1174  281 -102   -3
 -43  -47  749 1187  309 -103   -4
 -39  -56  717 1199  337 -104   -6
 -36  -65  685 1209  367 -104   -8
 -32  -73  652 1217  397 -103  -10
 -29  -79  620 1223  427 -102  -12
 -25  -85  587 1227  458 -100  -14
 -22  -90  555 1230  490  -98  -17
```

1.2.11.4.1.6 ppfcoef_scale_eq_12div16_32_phases_flip.dat

```
7  32 11
   -3 -132  486 1346  486 -132   -3
   -1 -132  449 1345  524 -131   -6
    1 -131  413 1342  562 -130   -9
    3 -130  378 1336  600 -127  -12
    4 -128  343 1328  639 -123  -15
    5 -125  309 1319  677 -119  -18
    6 -122  277 1306  716 -113  -22
    7 -118  245 1292  754 -106  -26
    8 -114  214 1276  793  -98  -31
    8 -109  185 1257  831  -89  -35
    9 -105  156 1237  869  -78  -40
    9 -100  130 1214  906  -66  -45
    9  -94  104 1190  942  -53  -50
    9  -89   79 1165  978  -38  -56
    8  -83   56 1138 1012  -22  -61
    8  -78   35 1108 1046   -4  -67
  -72   15 1081 1081   15  -72    0
  -67   -4 1046 1108   35  -78    8
  -61  -22 1012 1138   56  -83    8
  -56  -38  978 1165   79  -89    9
  -50  -53  942 1190  104  -94    9
  -45  -66  906 1214  130 -100    9
  -40  -78  869 1237  156 -105    9
  -35  -89  831 1257  185 -109    8
  -31  -98  793 1276  214 -114    8
  -26 -106  754 1292  245 -118    7
  -22 -113  716 1306  277 -122    6
  -18 -119  677 1319  309 -125    5
  -15 -123  639 1328  343 -128    4
  -12 -127  600 1336  378 -130    3
   -9 -130  562 1342  413 -131    1
   -6 -131  524 1345  449 -132   -1
```

1.2.11.4.1.7 ppfcoef_scale_eq_13div16_32_phases_flip.dat

```
7  32 11
   14 -154  435 1458  435 -154   14
   15 -150  393 1458  477 -157   12
   16 -146  353 1454  521 -160   10
   16 -141  314 1447  565 -161    8
   17 -135  276 1436  609 -161    6
   17 -129  239 1425  654 -161    3
```

```
  17 -123  204 1410  699 -159    0
  16 -116  170 1393  745 -156   -4
  16 -109  137 1373  790 -151   -8
  16 -102  107 1350  835 -146  -12
  15  -94   77 1325  879 -138  -16
  14  -87   50 1298  924 -130  -21
  13  -80   24 1269  968 -119  -27
  12  -72    0 1238 1010 -107  -33
  11  -65  -22 1204 1053  -94  -39
  10  -58  -43 1169 1093  -78  -45
 -52  -62 1138 1138  -62  -52    0
 -45  -78 1093 1169  -43  -58   10
 -39  -94 1053 1204  -22  -65   11
 -33 -107 1010 1238    0  -72   12
 -27 -119  968 1269   24  -80   13
 -21 -130  924 1298   50  -87   14
 -16 -138  879 1325   77  -94   15
 -12 -146  835 1350  107 -102   16
  -8 -151  790 1373  137 -109   16
  -4 -156  745 1393  170 -116   16
   0 -159  699 1410  204 -123   17
   3 -161  654 1425  239 -129   17
   6 -161  609 1436  276 -135   17
   8 -161  565 1447  314 -141   16
  10 -160  521 1454  353 -146   16
  12 -157  477 1458  393 -150   15
```

1.2.11.4.1.8 ppfcoef_scale_eq_14div16_32_phases_flip.dat

```
7  32 11
  27 -158  370 1570  370 -158   27
  27 -150  324 1568  417 -165   27
  26 -142  281 1563  465 -172   27
  25 -133  238 1555  515 -178   26
  24 -124  198 1543  565 -183   25
  23 -115  159 1527  616 -186   24
  22 -106  122 1510  667 -189   22
  21  -97   87 1489  719 -191   20
  19  -87   54 1464  772 -191   17
  18  -78   23 1437  824 -190   14
  16  -69   -6 1407  876 -187   11
  15  -60  -32 1373  927 -182    7
  13  -52  -57 1339  979 -176    2
  12  -44  -79 1300 1030 -168   -3
  11  -36  -99 1261 1079 -159   -9
   9  -28 -117 1218 1128 -147  -15
 -21 -134 1179 1179 -134  -21    0
 -15 -147 1128 1218 -117  -28    9
  -9 -159 1079 1261  -99  -36   11
  -3 -168 1030 1300  -79  -44   12
   2 -176  979 1339  -57  -52   13
   7 -182  927 1373  -32  -60   15
  11 -187  876 1407   -6  -69   16
  14 -190  824 1437   23  -78   18
  17 -191  772 1464   54  -87   19
  20 -191  719 1489   87  -97   21
  22 -189  667 1510  122 -106   22
  24 -186  616 1527  159 -115   23
  25 -183  565 1543  198 -124   24
  26 -178  515 1555  238 -133   25
  27 -172  465 1563  281 -142   26
  27 -165  417 1568  324 -150   27
```

1.2.11.4.1.9 ppfcoef_scale_eq_15div16_32_phases_flip.dat

```
7  32 11
   33 -143  294 1680  294 -143   33
   31 -132  246 1678  345 -155   35
   30 -121  199 1671  398 -165   36
   27 -109  154 1661  452 -175   38
   25  -97  112 1647  508 -185   38
   23  -86   72 1629  564 -193   39
   21  -75   35 1607  622 -201   39
   19  -64    0 1580  681 -207   39
   17  -53  -32 1551  740 -213   38
   15  -43  -61 1518  799 -217   37
   13  -33  -88 1481  859 -219   35
   11  -24 -113 1442  919 -220   33
    9  -15 -134 1399  978 -219   30
    8   -7 -153 1354 1036 -217   27
    6    0 -170 1307 1094 -212   23
    5    7 -184 1257 1150 -205   18
   13 -196 1207 1207 -196   13    0
   18 -205 1150 1257 -184    7    5
   23 -212 1094 1307 -170    0    6
   27 -217 1036 1354 -153   -7    8
   30 -219  978 1399 -134  -15    9
   33 -220  919 1442 -113  -24   11
   35 -219  859 1481  -88  -33   13
   37 -217  799 1518  -61  -43   15
   38 -213  740 1551  -32  -53   17
   39 -207  681 1580    0  -64   19
   39 -201  622 1607   35  -75   21
   39 -193  564 1629   72  -86   23
   38 -185  508 1647  112  -97   25
   38 -175  452 1661  154 -109   27
   36 -165  398 1671  199 -121   30
   35 -155  345 1678  246 -132   31
```

1.2.11.4.2 VS Polyphase Filter Coefficients

1.2.11.4.2.1 ppfcoef_scale_eq_1_32_phases_ver_5tap_flip.dat

```
5  32 11
  -47  177 1788  177  -47
  -40  133 1785  225  -55
  -33   91 1778  276  -64
  -27   53 1765  330  -73
  -21   18 1747  386  -82
  -15  -13 1722  445  -91
  -11  -41 1693  507 -100
   -7  -66 1660  570 -109
   -3  -88 1622  635 -118
    0 -107 1579  703 -127
    2 -122 1532  771 -135
    4 -135 1482  839 -142
    5 -145 1428  909 -149
    6 -153 1371  978 -154
    7 -158 1310 1047 -158
    7 -161 1247 1116 -161
 -162 1186 1186 -162    0
 -161 1116 1247 -161    7
 -158 1047 1310 -158    7
 -154  978 1371 -153    6
 -149  909 1428 -145    5
 -142  839 1482 -135    4
 -135  771 1532 -122    2
 -127  703 1579 -107    0
```

```
 -118  635 1622  -88   -3
 -109  570 1660  -66   -7
 -100  507 1693  -41  -11
  -91  445 1722  -13  -15
  -82  386 1747   18  -21
  -73  330 1765   53  -27
  -64  276 1778   91  -33
  -55  225 1785  133  -40
```

1.2.11.4.2.2 ppfcoef_scale_eq_3_32_phases_flip.dat

```
5,   32,   11,
  130,  515,  758,  515,  130,
  121,  503,  757,  528,  139,
  113,  490,  756,  541,  148,
  105,  477,  755,  553,  158,
   97,  464,  753,  566,  168,
   90,  451,  751,  578,  178,
   83,  437,  749,  590,  189,
   76,  424,  746,  602,  200,
   69,  411,  743,  614,  211,
   63,  398,  739,  626,  222,
   57,  386,  734,  637,  234,
   52,  373,  729,  648,  246,
   46,  360,  725,  659,  258,
   41,  347,  719,  670,  271,
   37,  335,  713,  680,  283,
   32,  322,  707,  690,  297,
  314,  710,  710,  314,    0,
  297,  690,  707,  322,   32,
  283,  680,  713,  335,   37,
  271,  670,  719,  347,   41,
  258,  659,  725,  360,   46,
  246,  648,  729,  373,   52,
  234,  637,  734,  386,   57,
  222,  626,  739,  398,   63,
  211,  614,  743,  411,   69,
  200,  602,  746,  424,   76,
  189,  590,  749,  437,   83,
  178,  578,  751,  451,   90,
  168,  566,  753,  464,   97,
  158,  553,  755,  477,  105,
  148,  541,  756,  490,  113,
  139,  528,  757,  503,  121};
```

1.2.11.4.2.3 ppfcoef_scale_eq_4_32_phases_flip.dat

```
5,   32,   11,
  116,  515,  786,  515,  116,
  107,  502,  785,  530,  124,
   99,  488,  784,  544,  133,
   92,  473,  783,  557,  143,
   85,  459,  781,  571,  152,
   78,  445,  778,  585,  162,
   71,  431,  775,  598,  173,
   65,  417,  772,  611,  183,
   59,  403,  767,  624,  195,
   53,  389,  763,  637,  206,
   48,  375,  758,  649,  218,
   43,  362,  752,  661,  230,
   38,  348,  747,  673,  242,
   34,  334,  740,  685,  255,
   30,  321,  733,  696,  268,
   26,  308,  726,  707,  281,
  298,  726,  726,  298,    0,
```

```
  281,  707,  726,  308,   26,
  268,  696,  733,  321,   30,
  255,  685,  740,  334,   34,
  242,  673,  747,  348,   38,
  230,  661,  752,  362,   43,
  218,  649,  758,  375,   48,
  206,  637,  763,  389,   53,
  195,  624,  767,  403,   59,
  183,  611,  772,  417,   65,
  173,  598,  775,  431,   71,
  162,  585,  778,  445,   78,
  152,  571,  781,  459,   85,
  143,  557,  783,  473,   92,
  133,  544,  784,  488,   99,
  124,  530,  785,  502,  107};
```

1.2.11.4.2.4 ppfcoef_scale_eq_5_32_phases_flip.dat

```
5,   32,   11,
   98,  515,  822,  515,   98,
   90,  500,  821,  531,  106,
   83,  484,  820,  547,  114,
   75,  469,  819,  562,  123,
   69,  453,  816,  577,  133,
   63,  438,  813,  592,  142,
   57,  422,  809,  607,  153,
   51,  407,  805,  622,  163,
   46,  391,  801,  636,  174,
   41,  376,  795,  650,  186,
   37,  361,  789,  664,  197,
   32,  347,  782,  678,  209,
   28,  332,  775,  691,  222,
   25,  317,  767,  704,  235,
   22,  303,  759,  716,  248,
   18,  289,  750,  729,  262,
  278,  746,  746,  278,    0,
  262,  729,  750,  289,   18,
  248,  716,  759,  303,   22,
  235,  704,  767,  317,   25,
  222,  691,  775,  332,   28,
  209,  678,  782,  347,   32,
  197,  664,  789,  361,   37,
  186,  650,  795,  376,   41,
  174,  636,  801,  391,   46,
  163,  622,  805,  407,   51,
  153,  607,  809,  422,   57,
  142,  592,  813,  438,   63,
  133,  577,  816,  453,   69,
  123,  562,  819,  469,   75,
  114,  547,  820,  484,   83,
  106,  531,  821,  500,   90};
```

1.2.11.4.2.5 ppfcoef_scale_eq_6_32_phases_flip.dat

```
5,   32,   11,
   77,  513,  868,  513,   77,
   70,  496,  867,  531,   84,
   63,  479,  866,  548,   92,
   57,  461,  864,  566,  100,
   51,  444,  861,  583,  109,
   46,  427,  857,  600,  118,
   41,  409,  853,  617,  128,
   36,  393,  847,  633,  139,
   32,  376,  841,  650,  149,
   28,  359,  835,  666,  160,
```

```
  24,  343,  827,  682,  172,
  21,  327,  819,  697,  184,
  18,  311,  810,  712,  197,
  15,  296,  800,  727,  210,
  13,  281,  790,  741,  223,
  11,  266,  779,  755,  237,
 253,  771,  771,  253,    0,
 237,  755,  779,  266,   11,
 223,  741,  790,  281,   13,
 210,  727,  800,  296,   15,
 197,  712,  810,  311,   18,
 184,  697,  819,  327,   21,
 172,  682,  827,  343,   24,
 160,  666,  835,  359,   28,
 149,  650,  841,  376,   32,
 139,  633,  847,  393,   36,
 128,  617,  853,  409,   41,
 118,  600,  857,  427,   46,
 109,  583,  861,  444,   51,
 100,  566,  864,  461,   57,
  92,  548,  866,  479,   63,
  84,  531,  867,  496,   70};
```

1.2.11.4.2.6 ppfcoef_scale_eq_7_32_phases_flip.dat

```
5,   32,   11,
   53,  510,  922,  510,   53,
   47,  490,  922,  529,   60,
   41,  470,  921,  549,   67,
   36,  451,  918,  569,   74,
   32,  431,  915,  588,   82,
   27,  412,  910,  608,   91,
   23,  393,  905,  627,  100,
   20,  374,  898,  646,  110,
   17,  356,  890,  665,  120,
   14,  337,  882,  684,  131,
   11,  320,  873,  702,  142,
    9,  302,  863,  720,  154,
    7,  285,  852,  737,  167,
    6,  269,  840,  753,  180,
    4,  253,  827,  770,  194,
    3,  237,  815,  785,  208,
  223,  801,  801,  223,    0,
  208,  785,  815,  237,    3,
  194,  770,  827,  253,    4,
  180,  753,  840,  269,    6,
  167,  737,  852,  285,    7,
  154,  720,  863,  302,    9,
  142,  702,  873,  320,   11,
  131,  684,  882,  337,   14,
  120,  665,  890,  356,   17,
  110,  646,  898,  374,   20,
  100,  627,  905,  393,   23,
   91,  608,  910,  412,   27,
   82,  588,  915,  431,   32,
   74,  569,  918,  451,   36,
   67,  549,  921,  470,   41,
   60,  529,  922,  490,   47};
```

1.2.11.4.2.6.1 ppfcoef_scale_eq_8div16_32_phases_ver_5tap_flip.dat

```
5  32 11
   28  502  988  502   28
   24  479  987  524   34
   19  457  985  547   40
```

```
  15  435  982  570   46
  12  413  978  592   53
   9  392  972  614   61
   6  371  965  637   69
   4  350  957  659   78
   2  330  948  680   88
   0  310  938  702   98
  -1  291  926  723  109
  -2  272  914  744  120
  -3  254  900  764  133
  -3  237  886  783  145
  -4  220  871  802  159
  -4  204  855  820  173
 188  836  836  188    0
 173  820  855  204   -4
 159  802  871  220   -4
 145  783  886  237   -3
 133  764  900  254   -3
 120  744  914  272   -2
 109  723  926  291   -1
  98  702  938  310    0
  88  680  948  330    2
  78  659  957  350    4
  69  637  965  371    6
  61  614  972  392    9
  53  592  978  413   12
  46  570  982  435   15
  40  547  985  457   19
  34  524  987  479   24
```

1.2.11.4.2.6.2 ppfcoef_scale_eq_9div16_32_phases_ver_5tap_flip.dat

```
5  32 11
    3  489 1064  489    3
    0  464 1062  515    7
   -3  439 1060  540   12
   -5  414 1056  566   17
   -7  390 1050  592   23
   -9  366 1044  618   29
  -10  343 1035  644   36
  -11  320 1025  670   44
  -12  298 1014  695   53
  -12  277 1001  720   62
  -12  256  987  745   72
  -12  236  972  769   83
  -12  217  956  792   95
  -11  199  938  815  107
  -10  181  920  837  120
  -10  165  900  859  134
  148  876  876  148    0
  134  859  900  165  -10
  120  837  920  181  -10
  107  815  938  199  -11
   95  792  956  217  -12
   83  769  972  236  -12
   72  745  987  256  -12
   62  720 1001  277  -12
   53  695 1014  298  -12
   44  670 1025  320  -11
   36  644 1035  343  -10
   29  618 1044  366   -9
   23  592 1050  390   -7
   17  566 1056  414   -5
   12  540 1060  439   -3
    7  515 1062  464    0
```

1.2.11.4.2.6.3 ppfcoef_scale_eq_10div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -20  470 1148  470  -20
  -22  442 1147  499  -18
  -23  413 1144  529  -15
  -24  386 1139  558  -11
  -24  359 1132  588   -7
  -24  333 1124  618   -3
  -24  308 1113  648    3
  -23  283 1101  678    9
  -23  260 1088  707   16
  -22  237 1072  737   24
  -21  215 1056  765   33
  -19  194 1037  793   43
  -18  174 1017  822   53
  -16  156  995  848   65
  -15  138  973  875   77
  -13  121  949  900   91
  105  919  919  105    0
   91  900  949  121  -13
   77  875  973  138  -15
   65  848  995  156  -16
   53  822 1017  174  -18
   43  793 1037  194  -19
   33  765 1056  215  -21
   24  737 1072  237  -22
   16  707 1088  260  -23
    9  678 1101  283  -23
    3  648 1113  308  -24
   -3  618 1124  333  -24
   -7  588 1132  359  -24
  -11  558 1139  386  -24
  -15  529 1144  413  -23
  -18  499 1147  442  -22
```

1.2.11.4.2.6.4 ppfcoef_scale_eq_11div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -40  444 1240  444  -40
  -40  412 1240  476  -40
  -40  381 1236  510  -39
  -39  350 1231  544  -38
  -37  321 1223  577  -36
  -36  293 1212  612  -33
  -34  265 1200  646  -29
  -32  239 1185  681  -25
  -30  214 1169  715  -20
  -28  190 1150  750  -14
  -26  167 1130  783   -6
  -23  146 1107  816    2
  -21  126 1083  849   11
  -19  107 1057  882   21
  -17   90 1030  913   32
  -15   73 1002  943   45
   58  966  966   58    0
   45  943 1002   73  -15
   32  913 1030   90  -17
   21  882 1057  107  -19
   11  849 1083  126  -21
    2  816 1107  146  -23
   -6  783 1130  167  -26
  -14  750 1150  190  -28
  -20  715 1169  214  -30
  -25  681 1185  239  -32
  -29  646 1200  265  -34
```

```
  -33  612 1212  293  -36
  -36  577 1223  321  -37
  -38  544 1231  350  -39
  -39  510 1236  381  -40
  -40  476 1240  412  -40
```

1.2.11.4.2.6.5 ppfcoef_scale_eq_12div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -56  409 1342  409  -56
  -54  373 1342  445  -58
  -51  339 1337  482  -59
  -49  306 1330  521  -60
  -46  274 1321  559  -60
  -43  244 1308  598  -59
  -40  215 1293  638  -58
  -36  187 1275  678  -56
  -33  161 1255  718  -53
  -30  137 1233  757  -49
  -27  114 1208  797  -44
  -24   93 1182  836  -39
  -21   73 1152  875  -31
  -18   55 1122  912  -23
  -16   38 1090  950  -14
  -14   23 1056  986   -3
    9 1015 1015    9    0
   -3  986 1056   23  -14
  -14  950 1090   38  -16
  -23  912 1122   55  -18
  -31  875 1152   73  -21
  -39  836 1182   93  -24
  -44  797 1208  114  -27
  -49  757 1233  137  -30
  -53  718 1255  161  -33
  -56  678 1275  187  -36
  -58  638 1293  215  -40
  -59  598 1308  244  -43
  -60  559 1321  274  -46
  -60  521 1330  306  -49
  -59  482 1337  339  -51
  -58  445 1342  373  -54
```

1.2.11.4.2.6.6 ppfcoef_scale_eq_13div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -65  364 1450  364  -65
  -61  326 1448  404  -69
  -57  289 1443  445  -72
  -53  253 1435  488  -75
  -48  220 1423  531  -78
  -44  188 1408  576  -80
  -40  158 1390  621  -81
  -36  130 1370  666  -82
  -32  103 1346  713  -82
  -28   79 1320  758  -81
  -24   56 1290  805  -79
  -21   36 1259  850  -76
  -18   17 1224  896  -71
  -15    0 1188  940  -65
  -12  -15 1149  984  -58
  -10  -28 1109 1027  -50
  -40 1064 1064  -40    0
  -50 1027 1109  -28  -10
  -58  984 1149  -15  -12
  -65  940 1188    0  -15
```

```
  -71  896 1224   17  -18
  -76  850 1259   36  -21
  -79  805 1290   56  -24
  -81  758 1320   79  -28
  -82  713 1346  103  -32
  -82  666 1370  130  -36
  -81  621 1390  158  -40
  -80  576 1408  188  -44
  -78  531 1423  220  -48
  -75  488 1435  253  -53
  -72  445 1443  289  -57
  -69  404 1448  326  -61
```

1.2.11.4.2.6.7 ppfcoef_scale_eq_14div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -67  310 1562  310  -67
  -61  269 1559  353  -72
  -55  230 1553  398  -78
  -50  193 1543  445  -83
  -44  158 1529  493  -88
  -39  125 1512  543  -93
  -34   94 1491  594  -97
  -30   66 1468  645 -101
  -25   41 1439  697 -104
  -22   17 1408  751 -106
  -18   -4 1373  804 -107
  -15  -23 1336  857 -107
  -12  -40 1296  910 -106
   -9  -55 1253  962 -103
   -7  -67 1208 1013  -99
   -5  -78 1161 1064  -94
  -86 1110 1110  -86    0
  -94 1064 1161  -78   -5
  -99 1013 1208  -67   -7
 -103  962 1253  -55   -9
 -106  910 1296  -40  -12
 -107  857 1336  -23  -15
 -107  804 1373   -4  -18
 -106  751 1408   17  -22
 -104  697 1439   41  -25
 -101  645 1468   66  -30
  -97  594 1491   94  -34
  -93  543 1512  125  -39
  -88  493 1529  158  -44
  -83  445 1543  193  -50
  -78  398 1553  230  -55
  -72  353 1559  269  -61
```

1.2.11.4.2.6.8 ppfcoef_scale_eq_15div16_32_phases_ver_5tap_flip.dat

```
5  32 11
  -61  248 1674  248  -61
  -54  204 1673  293  -68
  -47  163 1665  342  -75
  -41  125 1654  392  -82
  -35   90 1638  445  -90
  -29   57 1618  499  -97
  -24   27 1593  556 -104
  -20    0 1565  613 -110
  -16  -24 1532  672 -116
  -12  -46 1495  732 -121
   -9  -65 1455  793 -126
   -6  -81 1411  854 -130
   -4  -95 1364  915 -132
```

```
  -2 -107 1315  975 -133
   0 -116 1262 1035 -133
   1 -123 1208 1094 -132
-128 1152 1152 -128    0
-132 1094 1208 -123    1
-133 1035 1262 -116    0
-133  975 1315 -107   -2
-132  915 1364  -95   -4
-130  854 1411  -81   -6
-126  793 1455  -65   -9
-121  732 1495  -46  -12
-116  672 1532  -24  -16
-110  613 1565    0  -20
-104  556 1593   27  -24
 -97  499 1618   57  -29
 -90  445 1638   90  -35
 -82  392 1654  125  -41
 -75  342 1665  163  -47
 -68  293 1673  204  -54
```

ppcoef_scale_1x_ver_5tap.dat

```
5    32    11
      0       0    2048       0       0
    -40     133    1785     225     -55
    -33      91    1778     276     -64
    -27      53    1765     330     -73
    -21      18    1747     386     -82
    -15     -13    1722     445     -91
    -11     -41    1693     507    -100
     -7     -66    1660     570    -109
     -3     -88    1622     635    -118
      0    -107    1579     703    -127
      2    -122    1532     771    -135
      4    -135    1482     839    -142
      5    -145    1428     909    -149
      6    -153    1371     978    -154
      7    -158    1310    1047    -158
      7    -161    1247    1116    -161
    162    1186    1186    -162       0
    161    1116    1247    -161       7
    158    1047    1310    -158       7
    154     978    1371    -153       6
    149     909    1428    -145       5
    142     839    1482    -135       4
    135     771    1532    -122       2
    127     703    1579    -107       0
    118     635    1622     -88      -3
    109     570    1660     -66      -7
    100     507    1693     -41     -11
    -91     445    1722     -13     -15
    -82     386    1747      18     -21
    -73     330    1765      53     -27
    -64     276    1778      91     -33
    -55     225    1785     133     -40
```

1.2.11.4.3 VS (Bilinear Filter Coefficients)

1.2.11.4.3.1 ppfcoef_scale_eq_1_32_phases_flip_PPF3_peak5_gain_eq_1_25.dat

This is not applicable for this device.

```
7  32 11
  -11 -106  190 1902  190 -106  -11
   -9 -105  153 1897  230 -105  -13
   -8 -105  121 1887  274 -105  -16
   -6 -104   91 1869  320 -104  -18
   -5 -102   65 1843  370 -102  -21
   -4 -101   42 1812  424 -101  -24
   -3  -99   20 1776  480  -99  -27
   -2  -96    3 1730  539  -96  -30
   -1  -93  -12 1679  602  -93  -34
   -1  -90  -26 1627  665  -90  -37
    0  -87  -37 1568  732  -87  -41
    0  -84  -46 1506  801  -84  -45
    0  -80  -54 1439  871  -80  -48
    0  -76  -60 1371  941  -76  -52
    1  -72  -65 1299 1013  -72  -56
    1  -68  -69 1227 1085  -68  -60
  -64  -64 1152 1152  -64  -64    0
  -60  -68 1085 1227  -69  -68    1
  -56  -72 1013 1299  -65  -72    1
  -52  -76  941 1371  -60  -76    0
  -48  -80  871 1439  -54  -80    0
  -45  -84  801 1506  -46  -84    0
  -41  -87  732 1568  -37  -87    0
  -37  -90  665 1627  -26  -90   -1
  -34  -93  602 1679  -12  -93   -1
  -30  -96  539 1730    3  -96   -2
  -27  -99  480 1776   20  -99   -3
  -24 -101  424 1812   42 -101   -4
  -21 -102  370 1843   65 -102   -5
  -18 -104  320 1869   91 -104   -6
  -16 -105  274 1887  121 -105   -8
  -13 -105  230 1897  153 -105   -9
```

1.2.12 Video Compositer (VCOMP)

1.2.12.1 Overview

The Video Compositor module composites two sources of input video over a background color layer. Both input sources are in 4:2:2 YUV format. The output of the module is also 4:2:2 YUV.

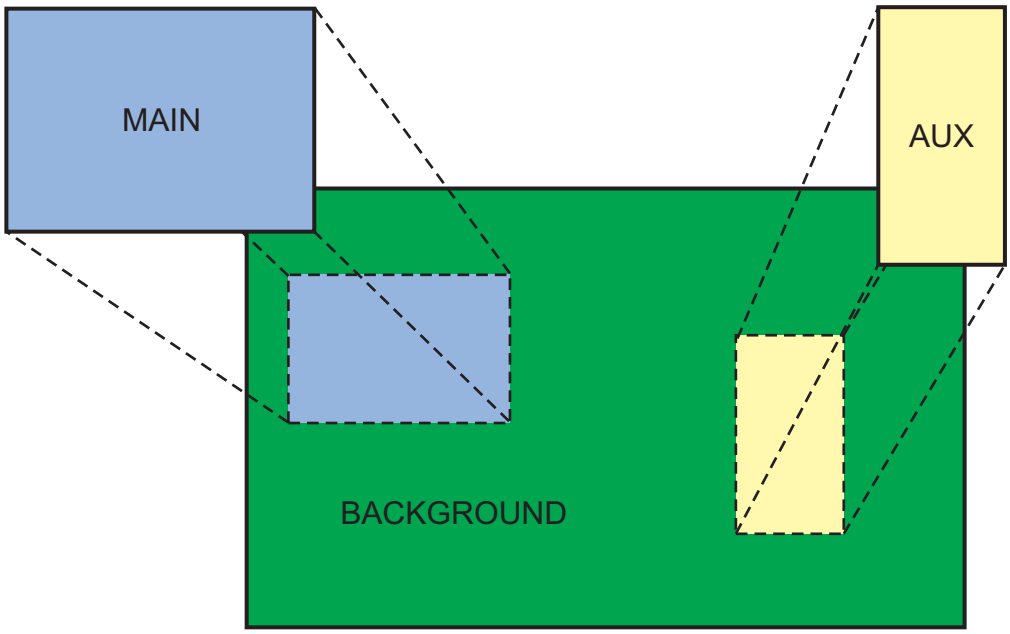
1.2.12.2 Features Supported

- Flexible placement of Main and Auxiliary layers on the background color
- Main and Auxiliary layers can be cropped in both horizontal and vertical directions
- Configurable background color in YUV422
- Optional disabling of Main or Auxiliary or both layers
- Alternate color selection when the input is disabled

1.2.12.3 Functional Description

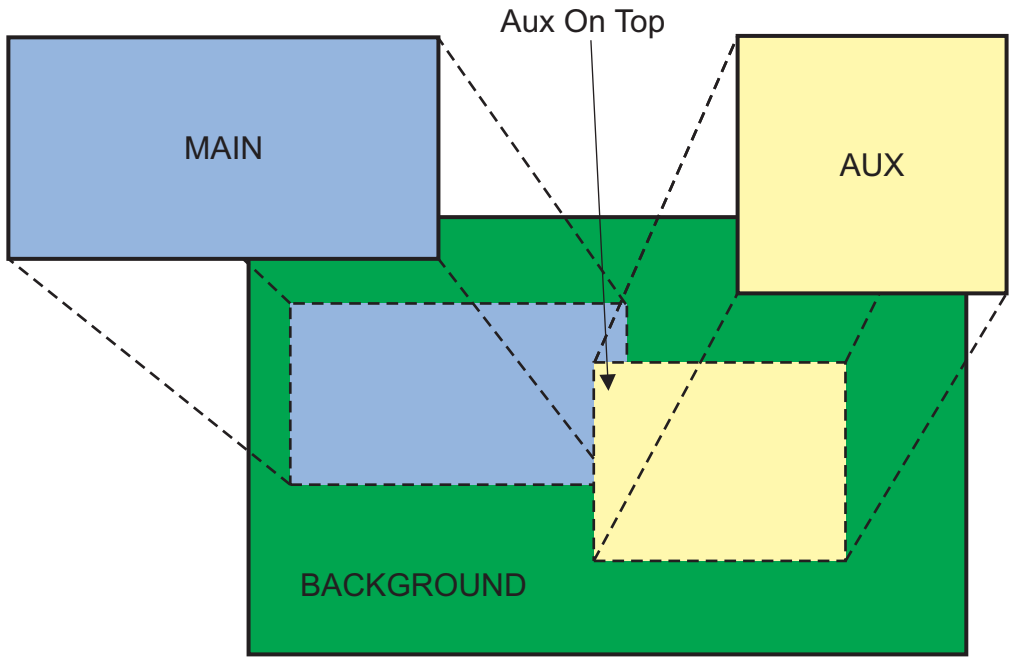
The VCOMP module takes 4:2:2 YUV input from two sources called Main (Main) and Auxiliary (Aux) layers. The VCOMP has a default background color layer that is the size of the output. As shown in Figure 1-157, the Main and Aux layers are composited over the background color.

Figure 1-157. Main and Auxiliary Layers Over Background



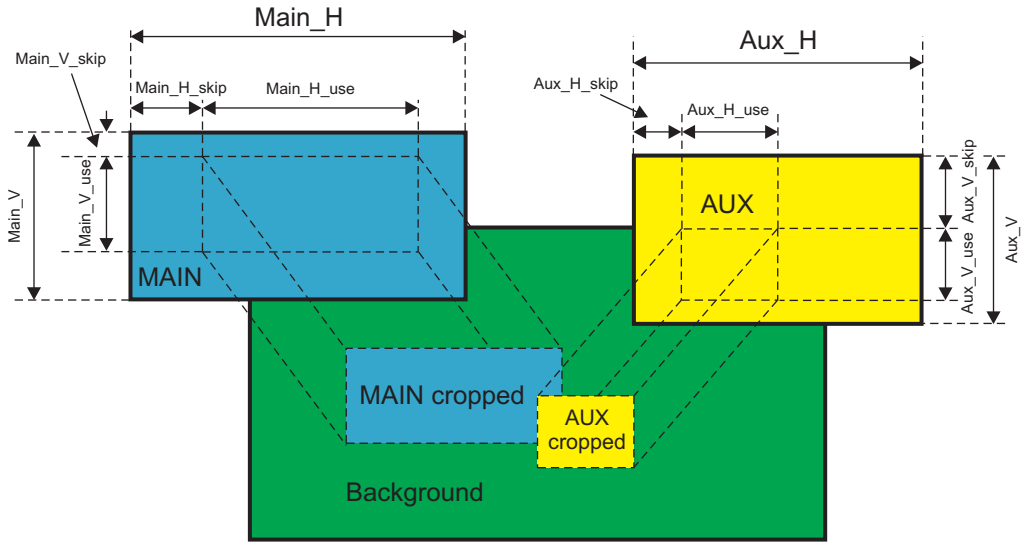
Pixels where the Main and Aux overlap are controlled by a global configuration bit (VCOMP→reg9.cfg_main_aux_n_ontop) that determines whether the Main or the Aux is on top. An example of the config bit set for Aux on Top is shown in Figure 1-158.

Figure 1-158. Overlap Region



The Main and Aux layers can be positioned anywhere over the background layer. The Main and Aux layers can optionally be cropped in the horizontal and vertical directions as shown in Figure 1-159.

Figure 1-159. Cropping of Input Layers

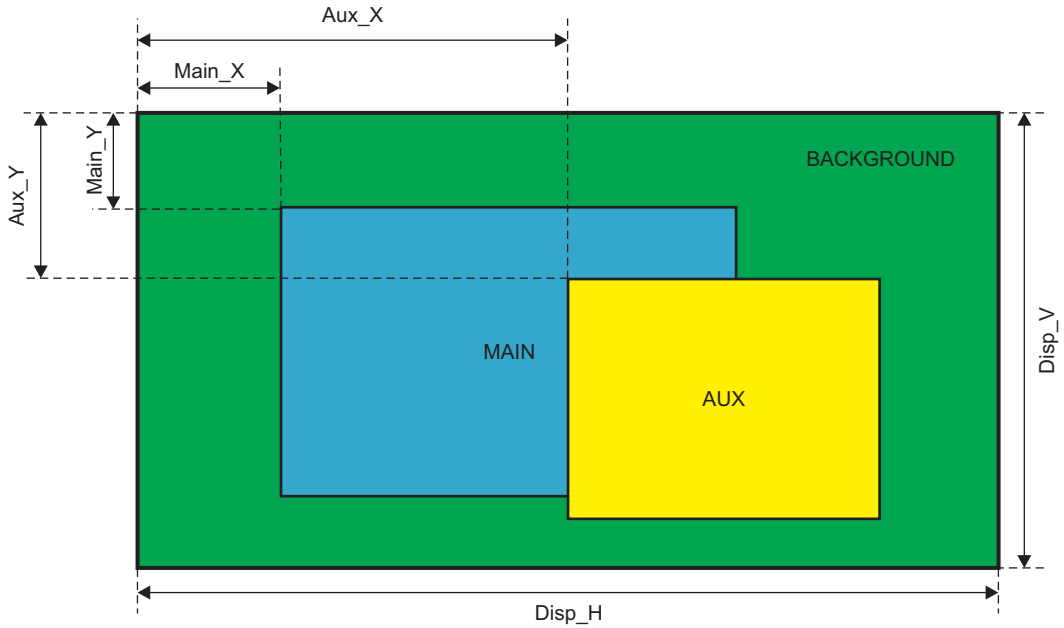


The configuration of parameters shown in Figure 1-159 is done using the following register fields:

```
Main_H          = VCOMP->reg0.cfg_main_native_numpix_per_line
Main_H_skip     = VCOMP->reg1.cfg_main_skip_numpix
Main_H_use      = VCOMP->reg1.cfg_main_use_numpix
Man_V           = VCOMP->reg0.cfg_main_native_numlines
Main_V_skip     = VCOMP->reg2.cfg_main_skip_numlines
Main_V_use      = VCOMP->reg2.cfg_main_use_numlines
Aux_H           = VCOMP->reg3.cfg_aux_native_numpix_per_line
Aux_H_skip      = VCOMP->reg4.cfg_aux_skip_numpix
Aux_H_use       = VCOMP->reg4.cfg_aux_use_numpix
Aux_V           = VCOMP->reg3.cfg_aux_native_numlines
Aux_V_skip      = VCOMP->reg5.cfg_aux_skip_numlines
Aux_V_use       = VCOMP->reg5.cfg_aux_use_numlines
```

The output of the VCOMP is a single 4:2:2 YUV plane, as shown in Figure 1-160.

Figure 1-160. Single Plane Output



The configuration of parameters shown in Figure 1-160 is done using the following register fields:

```
Disp_H    = VCOMP->reg6.cfg_dsply_numpix_per_line
Disp_V    = VCOMP->reg6. cfg_dsply_numlines
Main_X    = VCOMP->reg7.cfg_dsply_main_x_origin
Main_Y    = VCOMP->reg7.cfg_dsply_main_y_origin
Aux_X     = VCOMP->reg8.cfg_dsply_aux_x_origin
Aux_Y     = VCOMP->reg8.cfg_dsply_aux_y_origin
```

Background color configuration:

```
Y         = VCOMP->reg8.cfg_dsply_bckgrnd_y_val
Cb        = VCOMP->reg8.cfg_dsply_bckgrnd_cb_val
Cr        = VCOMP->reg8.cfg_dsply_bckgrnd_cr_val
```

In the previous examples, both Main and Aux are active. However, Main can be the only source (Figure 1-161), Aux can be the only source (Figure 1-162), or both Main and Aux can be disabled and only the Background is sent out (Figure 1-163). In the last case, either the Main or the Aux inputs must still be sending data into the VCOMP even though the picture data is not used.

Figure 1-161. Main Layer Only

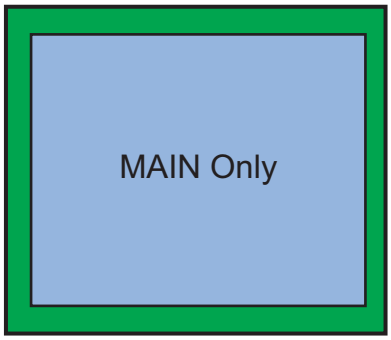


Figure 1-162. Aux Layer Only

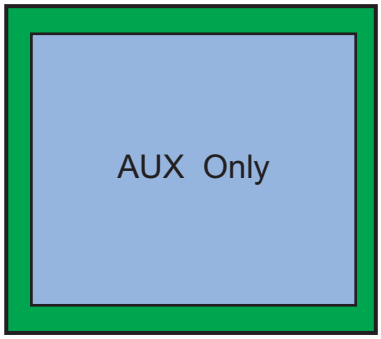
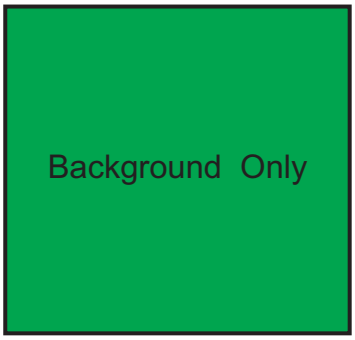


Figure 1-163. No Layer Enabled



To enable/disable Layers, the following register bitfields are used:

```
Main Layer    VCOMP->reg0.cfg_main_enable
Aux Layer     VCOMP->reg3.cfg_aux_enable
```

The Main and Aux sources, single or together, can completely cover the Background layer.

Alternate fixed color can be selected for main and aux layers when needed as shown below.

Main layer Fixed data enable/disable VCOMP→reg0.cfg_main_fixed_data_send

Fixed data:

```
Y        = VCOMP->reg11.cfg_dsply_alt_main_y_val
Cb       = VCOMP->reg11.cfg_dsply_alt_main_cb_val
Cr       = VCOMP->reg11.cfg_dsply_alt_main_cr_val
```

Aux layer Fixed data enable/disable VCOMP→reg3.cfg_aux_fixed_data_send

Fixed data:

```
Y        = VCOMP->reg12.cfg_dsply_alt_aux_y_val
Cb       = VCOMP->reg12.cfg_dsply_alt_aux_cb_val
Cr       = VCOMP->reg12.cfg_dsply_alt_aux_cr_val
```

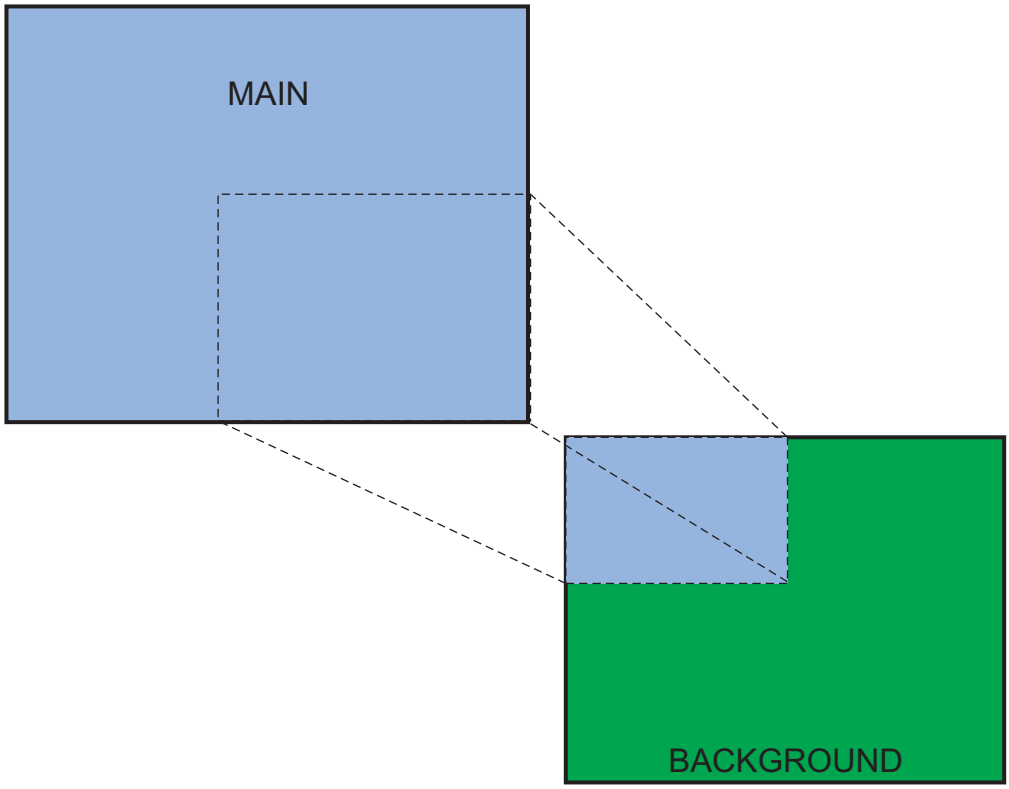
1.2.12.4 Exceptions

1.2.12.4.1 Exception with Respect to Timing

The VCOMP gets data from external memory and is generally used to setup HD Main Video Window for display operations through VENC. A VENC with a timebase generator determines the VCOMP's output timing requirements for when it needs to have pixel data ready. The VCOMP may not have pixel data ready for display if the input pixels have yet to arrive. The following is one scenario which can possibly create an issue.

In this case, the lower right quadrant of the Main layer is to be cropped and displayed on the top left corner of the output. This situation is shown in Figure 1-164. When the first pixel of the output is needed, the first pixel of the cropped region may not have entered the VCOMP yet. In this case, the configuration does not work for the device even though it is conceptually valid.

Figure 1-164. Conditions Where Valid Configurations May Not Work in a System



1.2.12.4.2 Exception with Respect to Placement

Figure 1-165 contains examples that show if the placement of Aux layer with respect to Main Layer is supported or not.

Exception1: Do not start or end an inserted Main or Aux window at an odd horizontal pixel location. Item “pip034” shown in Figure 1-165 is not supported because it starts and ends at odd pixel number.

Figure 1-165. Example

1.2.13 Video Port Direct Memory Access (VPDMA)

1.2.13.1 Introduction

1.2.13.1.1 Overview

The primary function of the Video Port Direct Memory Access (VPDMA) is to move data between external memory and HD-VPSS processing modules that source or sink data. The modules that source or sink data are referred to as "clients". The physical interface between the processing module and external memory is called a client. A "channel (software mechanism)" is set up inside the VPDMA to connect a specific memory buffer to a specific client. The VPDMA centralizes the Direct Memory Access (DMA) control functions and buffering required to allow all the clients to minimize the effect of long latency.

The VPDMA supports descriptor based mode where lists of descriptors can be set up to configure all the channels as they become available.

1.2.13.1.2 Basic Definitions

1.2.13.1.2.1 Firmware

All the DMA transfers are controlled by List Manager module inside VPDMA. List Manager needs to be loaded with **FIRMWARE**, before any DMA transfer from memory, after the VPDMA reset.

The first MMR write to LIST_ADDR register after VPDMA reset should be the address of the memory buffer(128-bit aligned, that is, last four bits of the buffer address should be zero) where the firmware is stored. List Manager then schedules a DMA transaction to fetch the firmware and sets the list_attr.rdy bit after the firmware loading is complete.

The followingcode is required to be included after the VPDMA clock is enabled in HD-VPSS:

```
*(volatile Uint32*)0x4810D004 = (Uint32)(firmware_buffer_address
      & 0xFFFFFFF0); // Write buffer address of the firmware to register VPDMA-
>List_addr (offset:0x4)
while(*(volatile Uint32*)0x4810D008 != 0x00080000); // Wait for firmware to complete loading.
Wait on bit-field VPDMA->List_attr->rdy (offset: 0x4, bit 19)
```

1.2.13.1.2.2 Client

The clients of the VPDMA are the physical connection to the HD-VPSS processing modules that source or sinks of the data and control when the channel can be updated. Each client can be configured to have specific start event which allows for the channel data to start flowing to or from the external client. The start event can be selected from one of the signals specified by bitfield RD_LB_CLIENT_CTL_STATUS.frame_start or RD_CLIENT_CTL_STATUS.frame_start or WR_CLIENT_CTL_STATUS.frame_start according to the type of the client. MMR of this type are mentioned in the address offset range 0x300 - 0x3f4.

1.2.13.1.2.3 Channel

The VPDMA requires a channel to be setup for each group of transfers. The VPDMA supports four types of channels: YUV, RGB, Miscellaneous and Free. The type of channels is based on the client that the channel can be connected to as each client is expected to provide a specific type of data.All the channels are described through a Data Transfer Descriptor that has a common format. The client that the channel is mapped to interprets the information in the descriptor to perform the requested data transfer.

1.2.13.1.2.4 Descriptor

The VPDMA needs to be programmed through DESCRIPTORS(A pre-defined structure of eight or four 32-bit words depending on type of descriptors) other than VPDMA Memory Mapped Registers (MMR). Descriptors are of three types:

1. Data Transfer Descriptors - A memory structure used to describe a desired memory transaction to or from a client.
2. Control Descriptors - A memory structure used to perform a control operation inside the DMA controller
3. Configuration Descriptors - A memory structure used to described a setup that should be applied to an processing modules like MMR write, scalar coefficient write etc.

1.2.13.1.2.5 List

A list is a group of descriptors that makes up a set of DMA transfers that need to be completed.

The Regular List is just a single list that the VPDMA will execute each descriptor once and initiate an interrupt when the list has completed. A regular list can contain any kind of descriptor without limitation and be of any size.

The VPDMA Controller works on lists of descriptors. In this mode the processor writes the lists of descriptors in the order it wants them executed. It then writes the location of the list to the LIST_ADDR register, followed by writing the size, type of list and list number to the LIST_ATTR register. The List Manager module will then schedule a DMA transfer to pull in the portion of the list that it can store in internal VPDMA memory. The List Manager will sequentially process the active list of descriptors until either the descriptor requires the use of a client that is currently active or if it is waiting for the next portion of the list to be transferred from a DMA request. If there is no active list to process the list manager will go into an IDLE mode waiting for any client that is blocking a list or a list DMA transfer to complete.

1.2.13.1.2.6 Data Formats Supported

Following are the data formats supported in the VPDMA:

- RGB Data Types:
  - RGB16-565
  - ARGB-1555
  - ARGB-4444
  - RGBA-5551
  - RGBA-4444
  - ARGB24-6666
  - RGB24-888
  - ARGB32-8888
  - RGBA24-6666
  - RGBA32-8888
  - Bitmap-8
  - Bitmap-4 Lower
  - Bitmap-4 Upper
  - Bitmap-2 Offset0
  - Bitmap-2 Offset1
  - Bitmap-2 Offset2
  - Bitmap-2 Offset3
  - Bitmap-1 Offset0
  - Bitmap-1 Offset1
  - Bitmap-1 Offset2
  - Bitmap-1 Offset3

  - Bitmap-1 Offset4
  - Bitmap-1 Offset5
  - Bitmap-1 Offset6
  - Bitmap-1 Offset7
- YUV Data Types:
  - Y 4:4:4
  - Y 4:2:2
  - Y 4:2:0
  - C 4:4:4
  - C 4:2:2
  - C 4:2:0
  - YC 4:2:2
  - YC4:4:4
  - Cb 4:4:4
  - Cb 4:2:2
  - Cb 4:2:0
  - CbY 4:2:2
  - YC 4:2:2
  - YCb 4:2:2

1.2.13.2 Memory Databus Write Order

The VPDMA L3 master port interfaces with the memory controller via a Quad Word (128 bit) data bus. Words are placed in the Quad Word data bus in little endian order. Table 1-72 shows the beginning or a burst on the quad word data bus and the arrangement of each word address within the burst.

Table 1-72. Memory Databus Write Order

	127 96	95 64	63 32	31 0
Quadword Addr 0	Word Addr 0x3	Word Addr 0x2	Word Addr 0x1	Word Addr 0x0
Quadword Addr 1	Word Addr 0x7	Word Addr 0x6	Word Addr 0x5	Word Addr 0x4
.....				
.....				

1.2.13.3 Descriptor

1.2.13.3.1 Data Transfer Descriptors

In order to set up data transfers from the VPDMA, a data transfer descriptor is added into a list. The fields used for an Inbound and Outbound descriptor vary slightly. An outbound transfer can have two different outbound transfers. The two transfers are the main data transfer and a write of an Inbound Descriptor. The created inbound descriptor is formatted so it can be read back in directly to the next channel specified in the original descriptor.

Figure 1-166. Inbound Data Transfer Descriptor Format

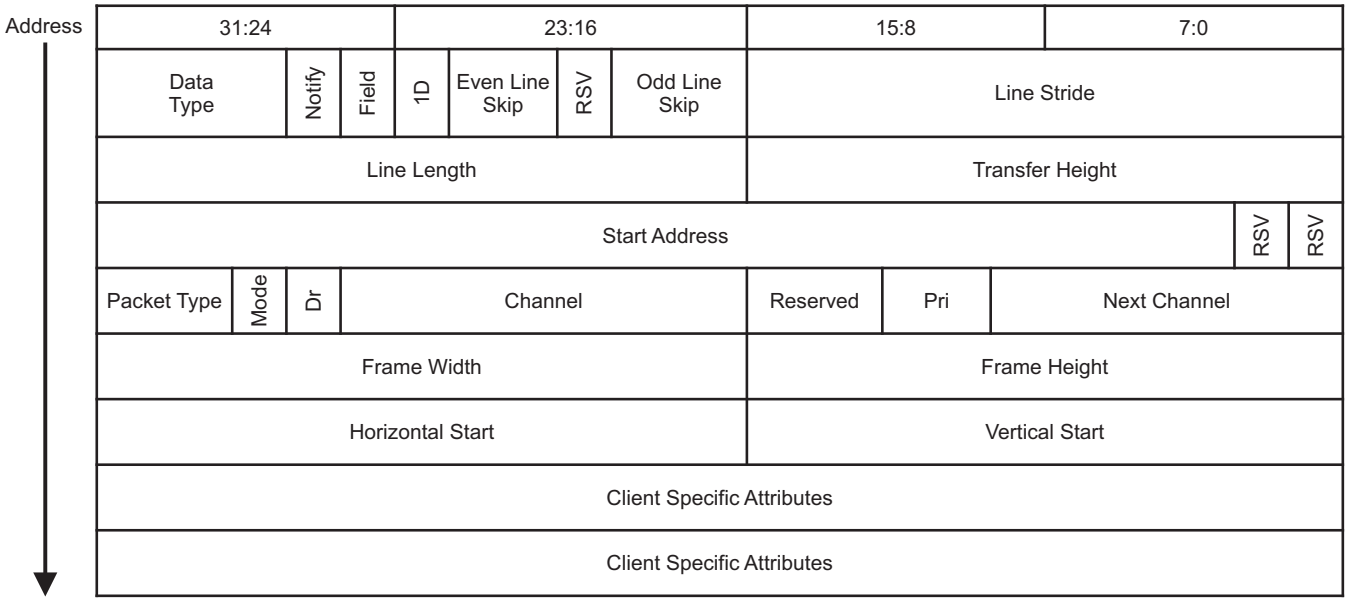
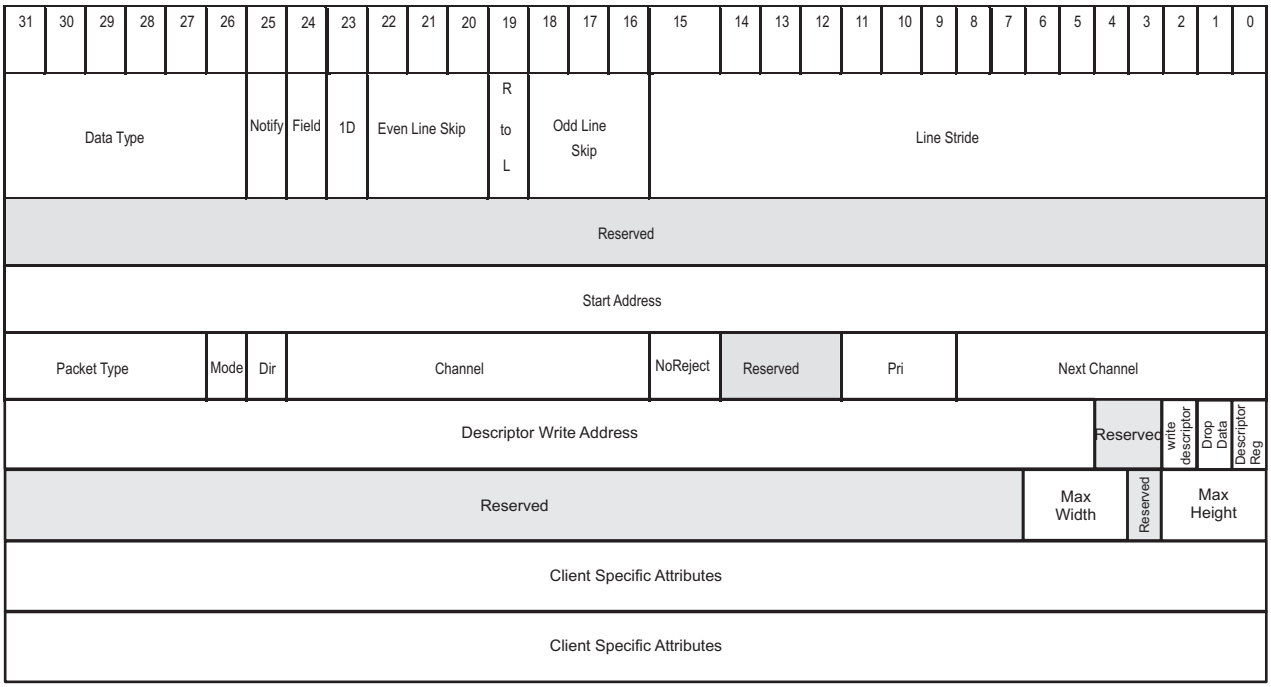


Figure 1-167. Outbound Data Transfer Descriptor Format



The general data transfer Descriptor formats can be seen in the above figures. The descriptor consists of 8 32 bit words. A Data Transfer Descriptor will be removed from the list when the resource specified by the Channel field is free. If the Channel is not free when the list reaches a data transfer descriptor then the list will stall until the current transfer on the channel has completed.

1.2.13.3.1.1 Data Packet Descriptor Word 0 (Data)

Table 1-73. Data Packet Descriptor Word 0 Field Descriptions

Bit	Field	Value	Description
31-26	Data Type		Miscellaneous Channel
			Sets the pixel size in bits plus 1
			RGB Channel
		0	RGB16-565
		1h	ARGB-1555
		2h	ARGB-4444
		3h	RGBA-5551
		4h	RGBA-4444
		5h	ARGB24-6666
		6h	RGB24-888
		7h	ARGB32-8888
		8h	RGBA24-6666
		9h	RGBA32-8888
		20h	Bitmap-8
		22h	Bitmap-4 Lower
		23h	Bitmap-4 Upper
		24h	Bitmap-2 Offset0
		25h	Bitmap-2 Offset1
		26h	Bitmap-2 Offset2
		27h	Bitmap-2 Offset3
		28h	Bitmap-1 Offset0
		29h	Bitmap-1 Offset1
		2Ah	Bitmap-1 Offset2
		2Bh	Bitmap-1 Offset3
		2Ch	Bitmap-1 Offset4
		2Dh	Bitmap-1 Offset5
		2Eh	Bitmap-1 Offset6
		2Fh	Bitmap-1 Offset7
			YUV Channel
		0	Y 4:4:4
		1	Y 4:2:2
		2	Y 4:2:0
		4	C 4:4:4
		5	C 4:2:2
		6	C 4:2:0
		7	YC 4:2:2
		8	YC 4:4:4
		14h	Cb 4:4:4
		15h	Cb 4:2:2
		16h	Cb 4:2:0
		17h	CbY 4:2:2
		27h	YC 4:2:2
		37h	YCb 4:2:2 The formats 14h, 15h, 16h, 17h, 27h, 37h are referred to as swap formats in this specification.
25	Notify	0-1	Send List Notification Interrupt upon last transfer of this channel
24	Field	0-1	Field Value

Table 1-73. Data Packet Descriptor Word 0 Field Descriptions (continued)

Bit	Field	Value	Description
23	1D	0-1	The transfer is one dimensional. The transfer and frame sizes are combined to make a single 32-bit transfer size. For writes this value is passed to the generated descriptor.
22-20	Even Line Skip		Field Value
		0	+1 line
		1h	+2 lines
		2h-7h	Reserved
18-16	Odd Line Skip		Field Value
		0	+1 line
		1h	+2 lines
		2h-7h	Reserved
15-0	Line Stride	0-FFFFh	Address stride between lines in bytes

1.2.13.3.1.1.1 Data Type

Bits 31-26 indicate the type of data that is to be transferred. This value is used to compute the number of bytes per pixel so that transactions may be made for the appropriate amount of data. The types of data are dependent on the type of channel. The VPDMA descriptor data types RGB or YUV are defined associated with the VPDMA channel assignment. This helps the engine to distinguish between the overlapping values of the descriptor data types for RGB and YUV data. For more information about VPDMA channels see Table 1-105.

1.2.13.3.1.1.1.1 Miscellaneous Data Type

The Data Type selects the size in bits of the data for the Miscellaneous channel. The range is from 0 to 63 to represent the sizes from 1 to 64 bits.

MV and MVSTM clients for DEI and DEI_H use 4 bits for each pixel. Data type 3 needs to be selected for this.

1.2.13.3.1.1.1.2 RGB Data Type

The most-significant bit selects if the data uses the CLUT table to generate the final RGB data. The data in this case is used as an address to a 256 entry table that generates the final data. If the Bitmap used is less then 8 bits then the lower bits of the data type are used to generate the upper address bits of the lookup table. If the CLUT table is not used then

1.2.13.3.1.1.1.3 YUV Data Type

The Data Type for a YUV channel determines if the data channel is interleaved or color space separate. If color spaced separate it is still assumed that the two chroma pixels are interleaved.

1.2.13.3.1.1.2 Notify

The Notify bit is used in conjunction with the Notify interrupts and when the channel has completed the DMA transfer the Notify Interrupt for the list that contains the descriptor will fire. The last Notify bit set for a specific list will be used so only a single Notify should be set in a list.

1.2.13.3.1.1.3 Field

The Field bit is the field value of the data that will be passed down to the clients. If the data is interlaced, then this value should be cleared to 0.

1.2.13.3.1.1.4 1D

This bit is set if a large one dimensional frame needs to be sent to the client. In this case, the stride is ignored and for the write the stride the generated descriptor will always be 0. If this bit is set, then the transfer length and transfer height and frame width and frame height fields are combined to form one 32-bit field with the upper 8 bits reserved and the lower 24 bits being the size of the frame in pixels.

CAUTION

Make sure the 1D bit is always cleared to 0 for expected functioning of the VPDMA.

1.2.13.3.1.1.5 Even Line Skip

The Even Line skip is used with Line Stride to generate the next line address on an even line. All frames start on line 0. This value allows for the DMA controller to skip lines for interlaced data in a progressive frame buffer.

1.2.13.3.1.1.6 Odd Line Skip

The Odd Line skip is used with Line Stride to generate the next line address on an odd line. All frames start on line 0, so this will apply starting with the second line. This value allows for the DMA controller to skip lines for interlaced data in a progressive frame buffer.

1.2.13.3.1.1.7 Line Stride

Bits 15-0 are the stride between lines in bytes at the external address. This value is added or subtracted based upon an adjustment using the current skip value. Operation of the external address pointer shall load the Source Address upon start of the transfer, then at the end of each line increment or decrement by the value computed using the Line Stride and Skip value for the line. The line stride must be aligned to an 128-bit bus width i.e The lower 4 bits of the line stride (in hexa decimal) should be zero.

1.2.13.3.1.2 Data Packet Descriptor Word 1

Table 1-74. Data Packet Descriptor Word 1 Field Description

Bits	Name	Description
31-16	Line Length	Line Length in Pixels
15-0	Transfer Height	Number of rows in transfer.

1.2.13.3.1.2.1 Line Length

Bits 31-16 are the line length in pixels of the current channel. This is ignored for the outbound transfer as the client will provide the line length with the end of line signal on the client interface. The maximum supported line length is currently 4096.

1.2.13.3.1.2.2 Transfer Height

Bits 15-0 are the number of lines to be transferred in the current channel. This is ignored for outbound transfers as the client will provide the line length with the end of frame signal on the client interface. The maximum supported transfer size is currently 2048.

1.2.13.3.1.3 Data Packet Descriptor Word 2

Table 1-75. Data Packet Descriptor Word 2 Field Descriptions

Bit	Field	Value	Description
31-0	Start Address		32-bit data source address [31:0]
			If Mode is TILED, then TILER specific ADDRESS Map is used:
			Bits 31-29:
		0	0-degree view
		1h	180-degree view + mirroring
		2h	0-degree view + mirroring
		3h	180-degree view
		4h	270-degree view + mirroring
		5h	270-degree view
		6h	90-degree view
		7h	90-degree view + mirroring
			Bits 28-27:
		0	8-bit container
		1h	16-bit container
		2h	32-bit container
		3h	Page Mode
			If Mode is NORMAL, then bits 31-26 are the upper bits of the address.

1.2.13.3.1.3.1 Start Address

This is the byte aligned address for the first data transfer. It should be set to the leftmost address fetch if the R to L field is not set in the descriptor. If the R to L field is set then the address for the right most pixel should be specified. The lower bits will be used by the client to determine where to grab the first pixel. The address on the OCP bus will always be word aligned.

1.2.13.3.1.4 Data Packet Descriptor Word 3

Table 1-76. Data Packet Descriptor Word 3 Field Descriptions

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = 0xa
26	Mode	0= Normal, 1=TILED
25	Direction	Inbound = 0, Outbound = 1
24-16	Channel	Channel for which this descriptor describes
15	Reserved	Reserved for future use
11-9	Priority	Only Bit 9 and Bit 11 are used to set the priority. Bit 10 is ignored. Highest = 0, Lowest = 3 By default, hardware assigns priority = 3. This priority level is used in the arbitration between the masters at EMIF level (for DDR access). See Section 1.2.13.3.1.4.5 for more details.
8-0	Next Channel	Next Channel to execute on a line or the channel to use in the generated write descriptor.

1.2.13.3.1.4.1 Packet Type

Bits 31:27 are a unique code which indicates that this Descriptor is a VPDMA descriptor. This value should be 0xA for data transfer descriptor.

1.2.13.3.1.4.2 Mode

Bit 26 is used to indicate if the transfer is to regular memory space or to 2D TILED memory space. The VPDMA will use this to determine if it does standard raster based addressing or if it assumes that the data is stored in TILER format. If data is stored in TILER format then the buffer is turned into 2 or 4 line buffers depending on the container type. For shared clients, such as the ancillary data and the VIP port, that use the memory only one can be active if the mode field is set.

1.2.13.3.1.4.3 Direction

Bit 25 is used to indicate the direction of transfer. This bit indicates that the data flow is from an external source to an internal buffer (inbound) or data transfers form an internal buffer to an external location (outbound).

1.2.13.3.1.4.4 Channel

Bits 24:16 are the Channels which is supported by the descriptor. This is the identification of the specific Channel that is controlled by the contents of the descriptor. The channel assignments can be found in the channel table.

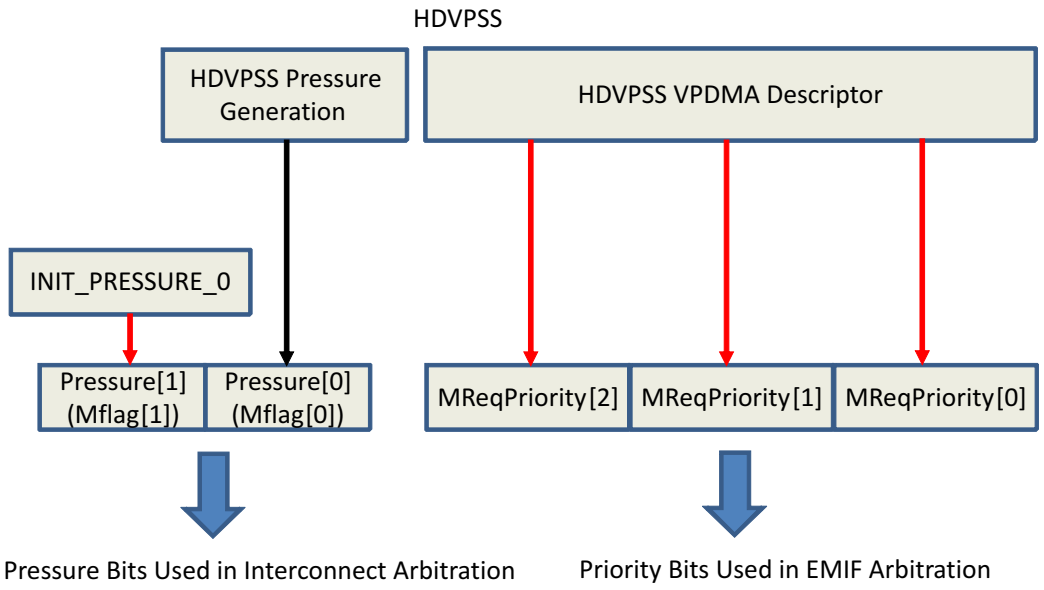
1.2.13.3.1.4.5 Priority

The priority bits (Bits 11, 10 and 9) are used to set the priority at the EMIF level.

VPDMA has two master ports (mst0 and mst1) to transfer the data to external and internal memories.

The priority level for the VPDMA masters can be at two different levels: L3 level (for all the transfers), and EMIF level (only for DDR transfers), as shown in Figure 1-168.

Figure 1-168. HDVPSS Pressure and Priority Settings



1.2.13.3.1.4.5.1 Priority Level Control at L3 Level

Four priority levels are supported at L3 level for all VPMDA transfers that use two bits (Pressure[1] and Pressure[0], shown in Figure 1-168). Pressure[0] is auto-controlled by VPDMA based on buffer levels. Pressure[1] can be configured in the chip level register: Bit 8 of 0x48140608 is used to set the Pressure[1] bit of the VPDMA master port0 (mst0); Bit 10 of 0x48140608 is used to set the Pressure[1] bit of the VPDMA master port1 (mst1).

It is recommended to use the same priority for both VPDMA masters.

NOTE: The higher the value, the higher the priority; that is, a priority level of 3 is prioritized over a priority level of 2.

1.2.13.3.1.4.5.2 Priority Level Control at EMIF Level

Eight levels of priority can be set at the EMIF level using three bits (MReqPriority[2:0]).

Table 1-77. Priority Bit Fields

Priority[11]	Priority[10]	Priority[9]	Priority [11:9]	Priority at EMIF
0	0	0	0	0
0	0	1	1	1
0	1	0	2	2
0	1	1	3	3
1	0	0	4	4
1	0	1	5	5
1	1	0	6	6
1	1	1	7	7

As shown in Table 1-77, Bit 10 of priority bit-field is ignored. Bits 9 and 11 are used to set the priority at EMIF level.

NOTE: The higher the value, the lower the priority; that is, a priority level of 2 is prioritized over a priority level of 3.

1.2.13.3.1.4.6 Next Channel

Bits 8:0 give the next channel to use. This value MUST be the same as the channel.

1.2.13.3.1.5 Data Packet Descriptor Word 4

1.2.13.3.1.5.1 Inbound data

Table 1-78. Data Packet Descriptor Word 4 Inbound Data Field Descriptions

Bits	Name	Description
31-16	Frame Width	Width of the client frame.
15-0	Frame Height	Height of the client frame

1.2.13.3.1.5.1.1 Frame Width

Bits 31:16 indicate the width in pixels of the frame. This is the width of the entire frame and not just the width of the data represented by the current channel unless this channel fills the entire frame. This allows for the VPDMA to present a larger frame of data to the client while only fetching the required data. The currently supported maximum width is 4096.

1.2.13.3.1.5.1.2 Frame Height

Bits 15:0 indicate the height in pixels of the entire frame. This is the height of the entire frame and not just the height of the data represented by the current channel unless this channel fills the entire frame. This allows for the VPDMA to present a larger frame of data to the client while only fetching the required data. The currently supported maximum height is 2048.

1.2.13.3.1.5.2 Outbound data

Table 1-79. Data Packet Descriptor Word 4 Outbound Data Field Descriptions

Bits	Name	Description
31-5	Descriptor Write Address	The 32 byte aligned location to write an inbound descriptor
2	Write Descriptor	If set to 1, a descriptor will be generated when the client completes a frame.
1	Drop Data	If set to 1, the data will not be written out. Also, if this is set, the write descriptor bit MUST be set.This allows for descriptors to only be written out so that software can determine the size of the required buffer before data is written out.
0	Use Descriptor Register	If set to 1, the CURRENT_DESCRIPTOR register will be used for the write address location. If set to 0, the Descriptor Write Address field in this word will be used for the Descriptor Write Address.

1.2.13.3.1.5.2.1 Descriptor Write Address

Bits 31:5 set the 32 byte address to write the generated descriptor. This address is only used if the Write Descriptor bit is set to 1 and the Use Descriptor Register bit is set to 0. If this case is met when the channel is complete a descriptor that meets the inbound descriptor format will be written to the location specified by this field. This allows for software to have a specific channel write its descriptor to a specific address no matter what order the channel completes compared to other outbound channels.

1.2.13.3.1.5.2.2 Write Descriptor

Bit 2 determines if a descriptor should be written out when the client is completed. If this bit is set the descriptor will be written. The format of the descriptor will be of an Inbound Data Transfer descriptor with the LINE LENGTH and TRANSFER HEIGHT fields determined by the counters in the clients. This means that the direction bit will be the opposite of the inbound descriptor. The FRAME WIDTH and FRAME HEIGHT values will match the LINE LENGTH and TRANSFER HEIGHT fields. The CHANNEL and NEXT CHANNEL fields will match the NEXT CHANNEL field of the original descriptor. The FIELD bit will match the source field captured by the client. The NOTIFY bit will always be 0. All other fields will match the original outbound descriptor. If the Outbound descriptor MODE is set to TILED data then the descriptor address used will be in TILED data space and software must ensure that the address is in page mode for the address of the descriptor.

1.2.13.3.1.5.2.3 Drop Data

Bit 1 determines if the data should be written out or not. In some cases software might only want to write the descriptor out to determine the size of the buffer that will be required to store incoming data. By setting this bit,no data will be written out. If this bit is set then the Write Descriptor bit MUST be set.

1.2.13.3.1.5.2.4 Use Descriptor Register

Bit 0 determines where the descriptor should be written. This bit MUST be set to 0.

1.2.13.3.1.6 Data Packet Descriptor Word 5

1.2.13.3.1.6.1 Inbound data

Table 1-80. Data Packet Descriptor Word 5 Inbound Data Field Descriptions

Bits	Name	Description
31-16	Horizontal Start	Data field start location for channel data insertion into frame/field.
15-0	Vertical Start	Horizontal displacement to start of window within the frame.

1.2.13.3.1.6.1.1 Horizontal Start

Bits 31:16 are the horizontal start location for the channel data. This value is used to control where the data starts for a channel so that blank segments may be inserted into the row. This is used for region based graphics. This field is reserved for outbound data. For non-graphics clients this MUST be set to 0.

1.2.13.3.1.6.1.2 Vertical Start

Bits 15:0 are the vertical start location for the channel which allows the channel to be spaced vertically from the previous channel or the top of the frame. This is used for region-based graphics. This field is reserved for outbound data descriptors. For non-graphics clients, this MUST be set to 0.

1.2.13.3.1.6.2 Outbound data

Table 1-81. Data Packet Descriptor Word 5 Outbound Data Field Descriptions

Bits	Name	Description
6-4	Max Width	The maximum allowable pixels per line. 0: Unlimited Line Size 4: 352 pixels 5: 768 pixels 6: 1280 pixels 7: 1920 pixels Others: Reserved
2-0	Max Height	The maximum allowable lines per frame 0: Unlimited Frame Size 4: 288 lines 5: 576 lines 6: 720 lines 7: 1080 lines Others: Reserved

1.2.13.3.1.6.2.1 Max Width

Bits 6:4 are encoded to set the maximum transferred line size. If the field is not set to unlimited if the client sending data into the VPDMA exceeds the maximum allowed pixels the data will continue to be received from the client but will not be sent to external memory until an end of line is received from the client sending data. The outbound descriptor if created will still have the transmitted size of the last line of the frame which will match the max width. If the frame does not exceed the max width then the actual transmitted size will be placed in the descriptor. Tiled clients such as the noise filter should always set this to 0. If Max Width is 0 and the line size is larger then 4096 pixels then the address counters will overflow and the data at the start of the line will be overwritten.

1.2.13.3.1.6.2.2 Max Height

Bits 2:0 are encoded to set the maximum transferred frame size. If the field is not set to unlimited if the client sending data into the VPDMA exceeds the maximum allowed lines the data will continue to be received from the client but will not be sent to external memory until an end of frame is received from the client sending data. The outbound descriptor if created will still have the transmitted number of lines received which would match the max height. If the frame does not exceed the max height then the actual transmitted size will be placed in the descriptor. . Tiled clients such as the noise filter should always set this to 0.

1.2.13.3.1.7 Data Packet Descriptor Word 6/7 (Data)

The words 4/5 give a 64 bit of configuration that can be passed specifically to the IP that supports it. This is passed directly down to the module through a VPI Control port. Please see the section on the specific clients for the format of this data.

1.2.13.3.2 Configuration Descriptor

The Configuration Descriptor is used in a List to setup a client configuration. The configuration descriptor consists of a header and a payload portion. The payload can either be part of the list that the descriptor is contained in or it can be at a separate location. The VPDMA will pass the payload of the configuration descriptor down to the client over the VPI Control port interface or through the MMR configuration port depending on the destination field. A Configuration Descriptor to any single destination except Destination 0 MUST be on a single list. Configuration Descriptors to different destinations may be on different lists.

The Configuration Descriptor Header is 4 32 bit words. A configuration descriptor is not consumed until the destination specified has received the entire configuration payload. Therefore the list is expected to stall while the configuration takes place. This ensures that all descriptors after a configuration descriptor in the list will occur after the desired configuration.

1.2.13.3.2.1 Configuration Descriptor Header Word0

Table 1-82. Configuration Descriptor Header Word0 Field Descriptions

Bits	Name	Description
31-0	Address Offset of the Destination	This is the address offset location in the destination that the block of data in the payload should be written. This field is only used if the descriptor Class is a block type. Otherwise this field is reserved.

1.2.13.3.2.2 Configuration Descriptor Header Word1

Table 1-83. Configuration Descriptor Header Word1 Field Descriptions

Bits	Name	Description
15-0	Number of Data Words	Length of First Data Packet for Class 1(block).

1.2.13.3.2.2.1 Number of Data Words

Bits 15-0 indicate the length of the first data block if the class is 1 as specified in Configuration Descriptor Header Word3. If the class is not 1 then this field should be set to 0.

1.2.13.3.2.3 Configuration Descriptor Header Word2

Table 1-84. Configuration Descriptor Header Word2 Field Descriptions

Bits	Name	Description
31-0	Payload Location	Pointer to the data payload

1.2.13.3.2.3.1 Payload Location

Bits 31-0 contain the pointer to the data payload if the command packet is an indirect type. This value along with the Payload Length will be combined to issue a DMA transaction that must complete before the List Manager can finish processing this descriptor. The list will be made inactive pending this DMA completion. This address should be on a 16 byte boundary so the lower 4 bits should always be 0.

1.2.13.3.2.4 Configuration Descriptor Header Word3

Table 1-85. Configuration Descriptor Header Word3 Field Descriptions

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = 0xb
26	Direct	0 = Indirect Command 1 = Direct Command
25-24	Class	0 = Address, Data Set 1 = Block 2,3 Reserved for Future Use
23-16	Destination	Destination of the configuration payload
15-0	Payload Length	Length of Payload in Words.

1.2.13.3.2.4.1 Packet Type

Bits 31-27, this field indicates the type of descriptor and should be set 0xB for configuration descriptor.

1.2.13.3.2.4.2 Direct

Bit 26, this field indicates that the descriptor is a direct command or indirect command. A direct command means that the payload is contiguous with the descriptor and will be pulled in by the list manager descriptor control as it processes the list. A direct payload must end on or before a 256 byte boundary in the list. An indirect command is when the Address is located in Word2 is a pointer to the data payload. A DMA transaction will be scheduled to bring the payload into the List Manager to allow for the payload to be sent to the destination.

1.2.13.3.2.4.3 Class

Bits 25-24, this field indicates the type of payload is associated with command descriptor, and thus how to handle the payload.

A 0 indicates that the payload consists of blocks of data with each block having an address and length. The first word after a sub-block contains the next address and length in bytes. This allows for writing to multiple configuration regions in a client. The Configuration Descriptor word1 is the first address and length pair. All addresses used must be larger then the previous address for all destinations except for the MMR destination. If a sub block length is not evenly divisible into 16 then zeroes should be padded in the payload so that the Next Client Address and Length field start on a 16 byte boundary.

1.2.13.3.2.4.3.1 Address Data Block Format

Table 1-86. Address Data Block Format Field Descriptions

Bits	Name	Description
31-0		Next Client Address
31-0		Configuration for Next Client Address
31-0		Configuration for Next Client Address + 4
31-0		Configuration for Next Client Address + 8
31-0		Configuration for Next Client Address + 12
31-0		Configuration for Next Client Address + 16
31-0		Next Client Address 2
15-0		Sub Block Length

A 1 indicates the payload is simply block data. The data is contiguous and starts at the offset of the destination as specified in word1.

1.2.13.3.2.4.4 Destination

The Destination field is used to determine where the configuration payload should be sent. The values for the destination field can be seen in the table below.

Table 1-87. Destination Field Description

Destination Value	Actual Destination	Description
0	mmr_client	Write to MMR registers to setup other modules
1	grpx1	Graphics 0 Frame Configuration and Scaler Coefficients
2	grpx2	Graphics 1 Frame Configuration and Scaler Coefficients
3	grpx3	Graphics 2 Frame Configuration and Scaler Coefficients
4	dei	DEI Scaler Coefficient Tables
5	mq	Mid Quality DEI Scaler Coefficient Tables
6	sc_m_wrbk	Mid Quality Writeback Scaler Coefficient Tables
7	vip1	VIP0 Scaler Coefficient Tables
8	vip2	VIP1 Scaler Coefficient Tables

1.2.13.3.2.4.5 Payload Length

Bits 15-0, this field indicates the size of the payload in words for the command. This is 128 bit words. The maximum number of words is 1023 words in a single payload.

1.2.13.3.3 Control Descriptor

1.2.13.3.3.1 Generic Control Descriptor Format

A control descriptor is the mechanism that is used in a list to give commands to the List Manager. These descriptors are not considered consumed until the List Manager has done the instruction required by the descriptor. All control descriptors are four 32bit words long. All control descriptors have a common Header located at Word 3. But, Word 0, Word 1 and Word 2 are based on the specific control descriptor.

1.2.13.3.3.2 Control Descriptor Header Description

Table 1-88. Control Descriptor Header Description

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = 0xc
26-25	Reserved	Reserved
24-16	Source	Specifies the source used for the control event.
15-4	Reserved	Reserved for future use
3-0	Control	The type of control descriptor that should be run by the List Manager

1.2.13.3.3.2.1 Packet Type

Bits 31-27, this field indicates the type of descriptor and should be set 0xB for configuration descriptor.

1.2.13.3.3.2.2 Source

The source is combined with the control field to determine what the control descriptor should use as the source for its synchronization event.

1.2.13.3.3.2.3 Control

The Control field defines the specific function of the descriptor. The table below lists the different control descriptors.

1.2.13.3.3.3 Control Descriptor Types

Table 1-89. Control Descriptor Types Summary

Control Descriptor	Control Field Value	Description
Sync on Client	0	Wait for the client attached to the channel specified to reach a certain event before proceeding.
Sync on List	1h	Wait for another list(s) to reach its Sync on List Descriptor
Sync on External Event	2h	Wait for a Register write to the LIST_STAT_SYNC bit specified or for an external event.
Sync on Channel	4h	Wait for the channel specified to complete
Change Client Interrupt	5h	Change the interrupt event for a client interrupt but do not wait for the event to occur.
Send Interrupt	6h	Generate an interrupt event on one of the Control Descriptor Interrupts
Reload List	7h	Reload the list from the location and size specified.
Abort Channel	8h	Abort the transfer in the channel specified.
Toggle LM Field	9h	Causes the internal field signal that can be selected by each client to toggle. This can be used so that a group of clients can all start simultaneously and not be tied to one of the specific output ports.

1.2.13.3.3.3.1 Sync on Client

A Sync on Client Control descriptor uses the source field to select a channel to modify the attached clients interrupt generation event. After configuring the interrupt generation event the list will then stall until that event has occurred. Word 0 and Word 2 are reserved.

Table 1-90. Sync on Client Field Descriptions (Word - 1)

Bits	Name	Description
31-16	PIXEL_COUNT	Specify the pixel position on a line specified by LINE_COUNT where a pixel based event would occur.
15-0	LINE_COUNT	Specify the line where a line based event would trigger

Table 1-91. Sync on Client Field Descriptions (Word - 3)

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = Ch
26-24	Reserved	Reserved
23-16	Source	Specifies the source used for the control event.
15-4	Reserved	Reserved for future use
3-0	Control	Control type = 0

1.2.13.3.3.3.2 Sync on List

The Sync on List Control descriptor is a mechanism to ensure that multiple lists have all reached a common point. The Sync on List descriptor uses the Source field as a mask for each list that should be synchronized which must include the list where the control descriptor resides. Once all lists specified in the source field have reached their Sync on List descriptor all lists will resume with the lowest list number resuming first. All Sync on List Control descriptors in each of the lists must have the same source field so that all lists will synchronize upon reaching that point.

If it is desired to synchronize list 0 and list 1 then the source field would be 0x3. If it is desired to synchronize list 1, list 3, and list 4 then the source field would be 0x1a. Word 0, Word 1 and Word 2 are reserved.

Table 1-92. Sync on List Field Descriptions (Word - 3)

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = Ch
26-24	Reserved	Reserved
23-16	Source	Specifies the source used for the control event.
15-4	Reserved	Reserved for future use
3-0	Control	Control type = 1h

1.2.13.3.3.3.3 Sync on External Event

A Sync on External Event descriptor ensures an external event has occurred before proceeding. The external event can be a write to a bit of the LIST_STAT_SYNC register or other external events that are determined at VPDMA elaboration to have occurred. This descriptor can be used to allow for external software to control progression of the list. The descriptor can also be used to select external signals that are brought into the VPDMA. Source values 0-7 are for the respective bits in the LIST_STAT_SYNC register. The processing of a Sync on External Event descriptor will result in a handshake the clears that bit of the LIST_STAT_SYNC register. Word 0, Word 1 and Word 2 are reserved.

Table 1-93. Sync on External Event Field Descriptions (Word - 3)

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = Ch
26-24	Reserved	Reserved
23-16	Source	Specifies the source used for the control event.
15-4	Reserved	Reserved for future use
3-0	Control	Control type = 2h

1.2.13.3.3.3.4 Sync on Channel

A Sync on Channel descriptor stalls the list until the channel specified is free. If the channel is already free then the descriptor will not cause the list to stall. Word 0, Word 1 and Word 2 are reserved.

Table 1-94. Sync on Channel Field Descriptions (Word - 3)

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = Ch
26-24	Reserved	Reserved
23-16	Source	Specifies the source used for the control event.
15-4	Reserved	Reserved for future use
3-0	Control	Control type = 4h

1.2.13.3.3.3.5 Change Client Interrupt

A Change Channel Interrupt Source descriptor uses the source field to select a channel to modify the attached clients interrupt generation event. The list will not stall on this descriptor. The format of the fields is identical to the Sync on Client Descriptor. Word 0 is reserved.

Table 1-95. Change Client Interrupt Field Descriptions (Word - 1)

Bits	Name	Description
31-16	PIXEL_COUNT	Specify the pixel position on a line specified by LINE_COUNT where a pixel based event would occur.
15-0	LINE_COUNT	Specify the line where a line based event would trigger.

Table 1-96. Change Client Interrupt Field Descriptions (Word - 2)

Bits	Name	Description
31-4	Reserved	Reserved
3-0	Event	Specify the event which should trigger the client interrupt.

Table 1-97. Change Client Interrupt Field Descriptions (Word - 3)

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = Ch
26-24	Reserved	Reserved
23-16	Source	Specifies the source used for the control event.
15-4	Reserved	Reserved for future use
3-0	Control	Control type = 5h

1.2.13.3.3.3.6 Send Interrupt

A Send Interrupt descriptor will cause the VPDMA to generate an interrupt on the list manager controlled interrupts as specified by the Source Field. The list will not stall on this descriptor. For example if source is 0 then vpdma_descriptor_interrupt0 will fire. If source is 12 then vpdma_descriptor_interrupt12 will fire. Word 0, Word 1 and Word 2 are reserved.

Table 1-98. Send Interrupt Field Descriptions (Word - 3)

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = Ch
26-24	Reserved	Reserved
23-16	Source	Specifies the source used for the control event.
15-4	Reserved	Reserved for future use
3-0	Control	Control type = 6h

1.2.13.3.3.3.7 Reload List

A Reload List descriptor causes ending descriptors after this descriptor in the original list to be dropped and a new list at the location and of the size specified in the descriptor. This descriptor can be used to allow for linked lists in the VPDMA as the list will continue from this point and fetch the list specified and it does not have to be continuous with the current list. The NULL bit in the first word determines if it is a valid address. If the NULL bit is set then the list will not fetch that address until a doorbell is received. Upon receiving the doorbell the reload list descriptor will be refetched from memory and then the new list address will be used along with list size to fetch the next section of the list. This allows for the list to be dynamically adding new sections of a list.

The procedure to use a reload list descriptor as a mechanism to allow dynamic additions to a list is as follows. A list section is created and the last descriptor in the section is a reload list with a NULL bit set. When a new section of the list is created the last descriptor in the list will be a Reload List with the NULL bit set. The software then updates the address and size in the Reload List descriptor in the previous section and then writes to the LIST_ATTRIBUTE register with the list number and the list type set to doorbell. This will create an immediate pulse that the hardware will latch until it does another list fetch. Software can do this as many times as it wants to keep adding to the list. Word 2 is reserved.

Table 1-99. Reload List Field Descriptions (Word - 0)

Bits	Name	Description
31-1	LIST_ADDRESS	31 most-significant Bits of the memory address where the descriptors to be loaded are stored. Address must be 16 byte aligned.
0	NULL	Specify whether “doorbell” SW trigger is used.

Table 1-100. Reload List Field Descriptions (Word - 1)

Bits	Name	Description
31-16	Reserved	Reserved
15-0	LIST_SIZE	Size of the list to load

Table 1-101. Reload List Field Descriptions (Word - 3)

Bits	Name	Description
31-27	Packet Type	Host Packet Descriptor Type = Ch
26-4	Reserved	Reserved
3-0	Control	Control type = 7h

1.2.13.3.3.3.8 Abort Channel

An Abort Channel descriptor is used to clear a channel. This clears the channel from issuing any more requests. Any outstanding requests for that channel will complete as originally scheduled. All data inside the client will be flushed. For Tiled Clients such as the noise filter it is required to issue two consecutive abort channel descriptors to ensure the channel is aborted for both the current tile and next tile. Word 0, Word 1 and Word 2 are reserved.

Table 1-102. Abort Channel Field Descriptions (Word - 3)

Bit	Name	Description
31-27	Packet Type	Host Packet Descriptor type = 0xC
26-24	Reserved	Reserved
23-16	Source	VPDMA Channel Number whose transfers are to be aborted
15-4	Reserved	Reserved
3-0	Control	Control type = 9h

1.2.13.3.3.3.9 Toggle LM Field

A Toggle LM Field descriptor is used if the clients set their frame source to LM FID. The read clients will start transmitting data upon the FID signal inside the LM changing value. This descriptor will cause the LM to toggle the value of the internal FIDs. The descriptor allows to either toggle the existing value of the FID or to set it. Note that clients wait for changes in FID value to generate the new frame so if the value is set to the current value no event will occur for the client. Word 0 and Word 2 are reserved.

Table 1-103. Toggle LM Field Field Descriptions (Word - 2)

Bit	Name	Description
31-6	Reserved	Reserved
5-4	FID2 CTL	This field controls the behavior of FID2 0h: FID2 remains unchanged 1h: FID2 toggles 2h: FID2 becomes 0 3h: FID2 becomes 1
3-2	FID1 CTL	This field controls the behavior of FID1 0h: FID1 remains unchanged 1h: FID1 toggles 2h: FID1 becomes 0 3h: FID1 becomes 1
1-0	FID0 CTL	This field controls the behavior of FID0 0h: FID0 remains unchanged 1h: FID0 toggles 2h: FID0 becomes 0 3h: FID0 becomes 1

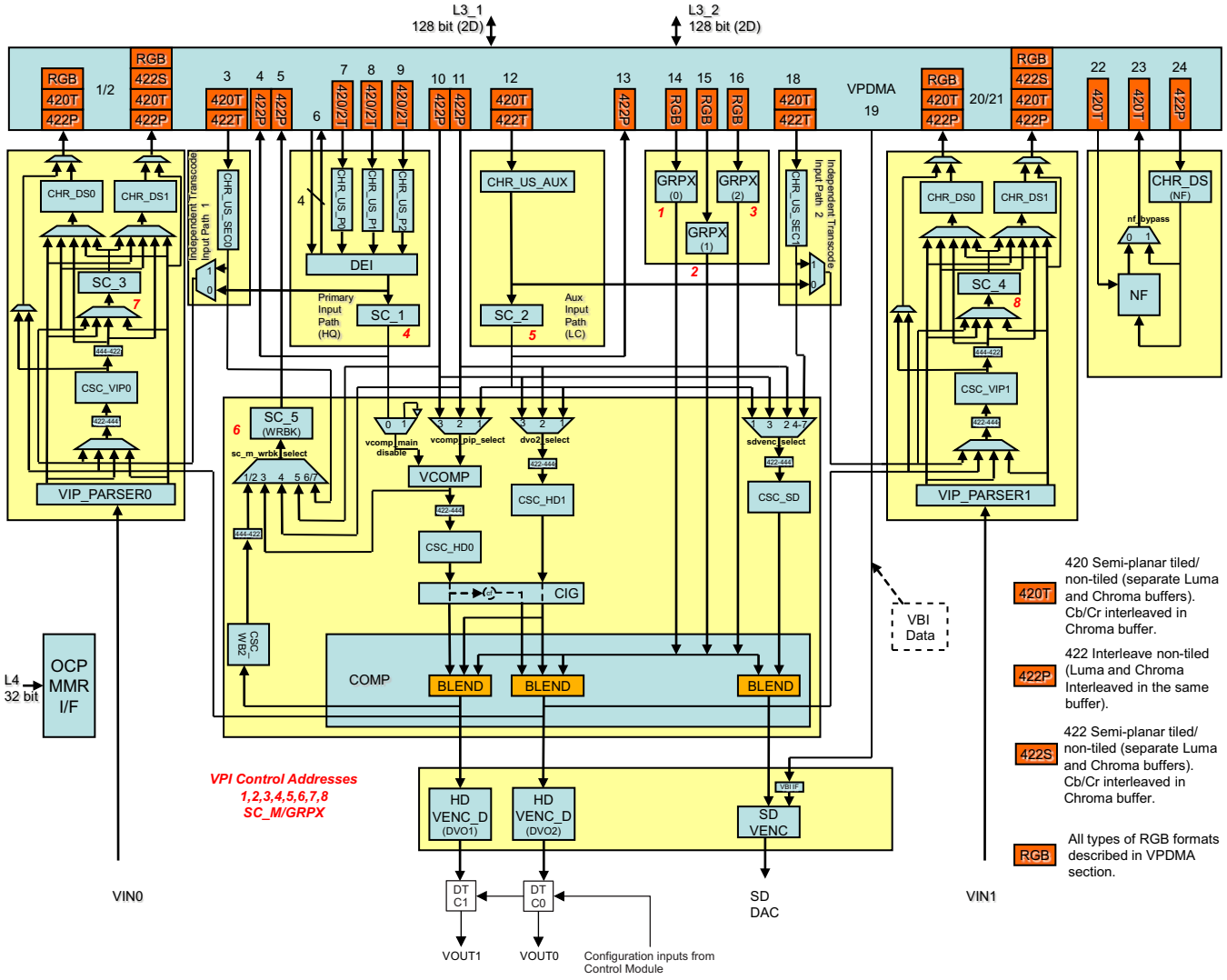
Table 1-104. Toggle LM Field Field Descriptions (Word - 3)

Bit	Field	Description
31-27	Packet Type	Host Packet Descriptor type = 0xC
26-4	Reserved	This field controls the behavior of FID2
3-0	Control	Control type = 9h

1.2.13.4 VPDMA and HDVPSS

The HDVPSS is shown in Figure 1-169 with each of the VPDMA clients numbered at the top.

Figure 1-169. Block Diagram



1.2.13.4.1 VPDMA Channels in HDVPSS

Table 1-105 lists all of the channels in the VPDMA and its base attributes. The Data Type column states what type of data YUV,RGB or OTHER the channel handles and in parentheses are the legal data type values that can be entered into a data transfer descriptor. The Client field states the name of the Client and in parentheses it states the reference number shown in Figure 1-169.

Table 1-105. VPDMA Channels

Channel	Description	Channel Number	Data Type	Client
dei_vid1_luma	DEI Video 420 Luma Data/ 422 Interleaved Data	0	YUV (0x1, 0x2, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	dei_1_luma (7)
dei_vid1_chroma	DEI Video 420 Chroma Data	1	YUV (0x5, 0x6, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	dei_1_chroma (7)
dei_vid2_luma	DEI Field Minus 1420 Luma Data	2	YUV (0x1, 0x2, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	dei_2_luma (8)
dei_vid2_chroma	DEI Field Minus 1 420 Chroma Data	3	YUV (0x5, 0x6, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	dei_2_chroma (8)
dei_vid3_luma	DEI Field Minus 2 420 Luma Data	4	YUV (0x1, 0x2, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	dei_3_luma (9)
dei_vid3_chroma	DEI Field Minus 2 420 Chroma Data	5	YUV (0x5, 0x6, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	dei_3_chroma (9)
dei_mv	DEI Motion Vector	12	OTHER (4)	dei_mv_in (6)
dei_mv_out	DEI Motion Vector Write	15	OTHER (4)	dei_mv_out (6)
dei_scaler	DEI Scaler Write to Memory	17	YUV (0x7)	dei_sc_out (4)
scaler_luma	Scaler In Luma 420/422 Data	18	YUV (0x1, 0x2, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	sc_in_luma (12)
scaler_chroma	Scaler in Chroma 420/422 Data	19	YUV (0x5, 0x6, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	sc_in_chroma (12)
scaler_out	Aux Scaler Write to Memory	28	YUV (0x7)	sc_out (13)
grpx1	Graphics 0 Data	29	RGB (0x0-0x9, 0x20, 0x22-0x2f)	grpx1_data (14)
grpx2	Graphics 1 Data	30	RGB (0x0-0x9, 0x20, 0x22-0x2f)	grpx2_data (15)
grpx3	Graphcis 2 Data	31	RGB (0x0-0x9, 0x20, 0x22-0x2f)	grpx3_data (16)
grpx1_stencil	Graphics 0 Stencil	32	OTHER (1)	grpx1_st (2)
grpx2_stencil	Graphics 1 Stencil	33	OTHER (1)	grpx2_st (2)
grpx3_stencil	Graphics 2 Stencil	34	OTHER (1)	grpx3_st (2)
grpx1_clut	Graphics 0 Color Lookup Table Load from Memory	35	OTHER ()	grpx1_clut_clt (2)
grpx2_clut	Graphics 1 Color Lookup Table Load from Memory	36	OTHER ()	grpx2_clut_clt (2)

Table 1-105. VPDMA Channels (continued)

Channel	Description	Channel Number	Data Type	Client
grpx3_clut	Graphics 2 Color Lookup Table Load from Memory	37	OTHER ()	grpx3_clut_clt (2)
vip1_mult_porta_src0	Video Input 1 Port A Channel 0	38	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src1	Video Input 1 Port A Channel 1	39	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src2	Video Input 1 Port A Channel 2	40	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src3	Video Input 1 Port A Channel 3	41	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src4	Video Input 1 Port A Channel 4	42	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src5	Video Input 1 Port A Channel 5	43	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src6	Video Input 1 Port A Channel 6	44	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src7	Video Input 1 Port A Channel 7	45	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src8	Video Input 1 Port A Channel 8	46	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src9	Video Input 1 Port A Channel 9	47	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src10	Video Input 1 Port A Channel 10	48	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src11	Video Input 1 Port A Channel 11	49	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src12	Video Input 1 Port A Channel 12	50	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src13	Video Input 1 Port A Channel 13	51	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src14	Video Input 1 Port A Channel 14	52	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_porta_src15	Video Input 1 Port A Channel 15	53	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_mult_portb_src0	Video Input 1 Port B Channel 0	54	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src1	Video Input 1 Port B Channel 1	55	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src2	Video Input 1 Port B Channel 2	56	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src3	Video Input 1 Port B Channel 3	57	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src4	Video Input 1 Port B Channel 4	58	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src5	Video Input 1 Port B Channel 5	59	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src6	Video Input 1 Port B Channel 6	60	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src7	Video Input 1 Port B Channel 7	61	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src8	Video Input 1 Port B Channel 8	62	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src9	Video Input 1 Port B Channel 9	63	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src10	Video Input 1 Port B Channel 10	64	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)

Table 1-105. VPDMA Channels (continued)

Channel	Description	Channel Number	Data Type	Client
vip1_mult_portb_src11	Video Input 1 Port B Channel 11	65	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src12	Video Input 1 Port B Channel 12	66	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src13	Video Input 1 Port B Channel 13	67	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src14	Video Input 1 Port B Channel 14	68	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_portb_src15	Video Input 1 Port B Channel 15	69	YUV (0x7, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_mult_anca_src0	Video Input 1 Port A Ancillary Data Channel 0	70	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src1	Video Input 1 Port A Ancillary Data Channel 1	71	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src2	Video Input 1 Port A Ancillary Data Channel 2	72	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src3	Video Input 1 Port A Ancillary Data Channel 3	73	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src4	Video Input 1 Port A Ancillary Data Channel 4	74	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src5	Video Input 1 Port A Ancillary Data Channel 5	75	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src6	Video Input 1 Port A Ancillary Data Channel 6	76	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src7	Video Input 1 Port A Ancillary Data Channel 7	77	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src8	Video Input 1 Port A Ancillary Data Channel 8	78	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src9	Video Input 1 Port A Ancillary Data Channel 9	79	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src10	Video Input 1 Port A Ancillary Data Channel 10	80	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src11	Video Input 1 Port A Ancillary Data Channel 11	81	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src12	Video Input 1 Port A Ancillary Data Channel 12	82	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src13	Video Input 1 Port A Ancillary Data Channel 13	83	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src14	Video Input 1 Port A Ancillary Data Channel 14	84	OTHER (8)	vip1_anc_a (2)
vip1_mult_anca_src15	Video Input 1 Port A Ancillary Data Channel 15	85	OTHER (8)	vip1_anc_a (2)
vip1_mult_ancb_src0	Video Input 1 Port B Ancillary Data Channel 0	86	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src1	Video Input 1 Port B Ancillary Data Channel 1	87	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src2	Video Input 1 Port B Ancillary Data Channel 2	88	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src3	Video Input 1 Port B Ancillary Data Channel 3	89	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src4	Video Input 1 Port B Ancillary Data Channel 4	90	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src5	Video Input 1 Port B Ancillary Data Channel 5	91	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src6	Video Input 1 Port B Ancillary Data Channel 6	92	OTHER (8)	vip1_anc_b (2)

Table 1-105. VPDMA Channels (continued)

Channel	Description	Channel Number	Data Type	Client
vip1_mult_ancb_src7	Video Input 1 Port B Ancillary Data Channel 7	93	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src8	Video Input 1 Port B Ancillary Data Channel 8	94	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src9	Video Input 1 Port B Ancillary Data Channel 9	95	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src10	Video Input 1 Port B Ancillary Data Channel 10	96	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src11	Video Input 1 Port B Ancillary Data Channel 11	97	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src12	Video Input 1 Port B Ancillary Data Channel 12	98	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src13	Video Input 1 Port B Ancillary Data Channel 13	99	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src14	Video Input 1 Port B Ancillary Data Channel 14	100	OTHER (8)	vip1_anc_b (2)
vip1_mult_ancb_src15	Video Input 1 Port B Ancillary Data Channel 15	101	OTHER (8)	vip1_anc_b (2)
vip1_porta_luma	Video Input 1 Port A 420 Data Luma	102	YUV (0x1, 0x2,0x7, 0x17, 0x27, 0x37)	vip1_up_y (1)
vip1_porta_chroma	Video Input 1 Port A 420 Data Chroma	103	YUV (0x5, 0x6, 0x7, 0x15, 0x16, 0x17, 0x27, 0x37)	vip1_up_uv (1)
vip1_portb_luma	Video Input 1 Port B 420 Data Luma	104	YUV (0x1, 0x2,0x7, 0x17, 0x27, 0x37)	vip1_lo_y (2)
vip1_portb_chroma	Video Input 1 Port B 420 Data Chroma	105	YUV (0x5, 0x6, 0x7, 0x15, 0x16, 0x17, 0x27, 0x37)	vip1_lo_uv (1)
vip1_porta_rgb	Video Input 1 Port A RGB Data	106	RGB (0x0-0x19)	vip1_up_y (1)
vip1_portb_rgb	Video Input 1 Port B RGB Data	107	RGB (0x0-0x19)	vip1_lo_y (2)
vip2_mult_porta_src0	Video Input 2 Port A Channel 0	108	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src1	Video Input 2 Port A Channel 1	109	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src2	Video Input 2 Port A Channel 2	110	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src3	Video Input 2 Port A Channel 3	111	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src4	Video Input 2 Port A Channel 4	112	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src5	Video Input 2 Port A Channel 5	113	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src6	Video Input 2 Port A Channel 6	114	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src7	Video Input 2 Port A Channel 7	115	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src8	Video Input 2 Port A Channel 8	116	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src9	Video Input 2 Port A Channel 9	117	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src10	Video Input 2 Port A Channel 10	118	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src11	Video Input 2 Port A Channel 11	119	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)

Table 1-105. VPDMA Channels (continued)

Channel	Description	Channel Number	Data Type	Client
vip2_mult_porta_src12	Video Input 2 Port A Channel 12	120	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src13	Video Input 2 Port A Channel 13	121	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src14	Video Input 2 Port A Channel 14	122	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_porta_src15	Video Input 2 Port A Channel 15	123	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)
vip2_mult_portb_src0	Video Input 2 Port B Channel 0	124	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src1	Video Input 2 Port B Channel 1	125	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src2	Video Input 2 Port B Channel 2	126	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src3	Video Input 2 Port B Channel 3	127	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src4	Video Input 2 Port B Channel 4	128	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src5	Video Input 2 Port B Channel 5	129	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src6	Video Input 2 Port B Channel 6	130	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src7	Video Input 2 Port B Channel 7	131	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src8	Video Input 2 Port B Channel 8	132	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src9	Video Input 2 Port B Channel 9	133	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src10	Video Input 2 Port B Channel 10	134	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src11	Video Input 2 Port B Channel 11	135	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src12	Video Input 2 Port B Channel 12	136	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src13	Video Input 2 Port B Channel 13	137	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src14	Video Input 2 Port B Channel 14	138	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_portb_src15	Video Input 2 Port B Channel 15	139	YUV (0x7, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_mult_anca_src0	Video Input 2 Port A Ancillary Data Channel 0	140	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src1	Video Input 2 Port A Ancillary Data Channel 1	141	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src2	Video Input 2 Port A Ancillary Data Channel 2	142	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src3	Video Input 2 Port A Ancillary Data Channel 3	143	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src4	Video Input 2 Port A Ancillary Data Channel 4	144	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src5	Video Input 2 Port A Ancillary Data Channel 5	145	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src6	Video Input 2 Port A Ancillary Data Channel 6	146	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src7	Video Input 2 Port A Ancillary Data Channel 7	147	OTHER (8)	vip2_anc_a (21)

Table 1-105. VPDMA Channels (continued)

Channel	Description	Channel Number	Data Type	Client
vip2_mult_anca_src8	Video Input 2 Port A Ancillary Data Channel 8	148	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src9	Video Input 2 Port A Ancillary Data Channel 9	149	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src10	Video Input 2 Port A Ancillary Data Channel 10	150	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src11	Video Input 2 Port A Ancillary Data Channel 11	151	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src12	Video Input 2 Port A Ancillary Data Channel 12	152	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src13	Video Input 2 Port A Ancillary Data Channel 13	153	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src14	Video Input 2 Port A Ancillary Data Channel 14	154	OTHER (8)	vip2_anc_a (21)
vip2_mult_anca_src15	Video Input 2 Port A Ancillary Data Channel 15	155	OTHER (8)	vip2_anc_a (21)
vip2_mult_ancb_src0	Video Input 2 Port B Ancillary Data Channel 0	156	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src1	Video Input 2 Port B Ancillary Data Channel 1	157	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src2	Video Input 2 Port B Ancillary Data Channel 2	158	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src3	Video Input 2 Port B Ancillary Data Channel 3	159	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src4	Video Input 2 Port B Ancillary Data Channel 4	160	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src5	Video Input 2 Port B Ancillary Data Channel 5	161	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src6	Video Input 2 Port B Ancillary Data Channel 6	162	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src7	Video Input 2 Port B Ancillary Data Channel 7	163	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src8	Video Input 2 Port B Ancillary Data Channel 8	164	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src9	Video Input 2 Port B Ancillary Data Channel 9	165	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src10	Video Input 2 Port B Ancillary Data Channel 10	166	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src11	Video Input 2 Port B Ancillary Data Channel 11	167	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src12	Video Input 2 Port B Ancillary Data Channel 12	168	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src13	Video Input 2 Port B Ancillary Data Channel 13	169	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src14	Video Input 2 Port B Ancillary Data Channel 14	170	OTHER (8)	vip2_anc_b (21)
vip2_mult_ancb_src15	Video Input 2 Port B Ancillary Data Channel 15	171	OTHER (8)	vip2_anc_b (21)
vip2_porta_luma	Video Input 2 Port A 420 Data Luma	172	YUV (0x1, 0x2, 0x7, 0x17, 0x27, 0x37)	vip2_up_y (20)
vip2_porta_chroma	Video Input 2 Port A 420 Data Chroma	173	YUV (0x5, 0x6, 0x7, 0x15, 0x16, 0x17, 0x27, 0x37)	vip2_up_uv (20)
vip2_portb_luma	Video Input 2 Port B 420 Data Luma	174	YUV (0x1, 0x2, 0x7, 0x17, 0x27, 0x37)	vip2_lo_y (21)

Table 1-105. VPDMA Channels (continued)

Channel	Description	Channel Number	Data Type	Client
vip2_portb_chroma	Video Input 2 Port B 420 Data Chroma	175	YUV (0x5, 0x6, 0x7, 0x15, 0x16, 0x17, 0x27, 0x37)	vip2_lo_uv (20)
vip2_porta_rgb	Video Input 2 Port A RGB Data	176	RGB (0x0-0x19)	vip2_up_y (20)
vip2_portb_rgb	Video Input 2 Port B RGB Data	177	RGB (0x0-0x19)	vip2_lo_y (21)
nf_read	Noise Filter Input Data 422 Interleaved	178	YUV (0x7, 0x17, 0x27, 0x37)	nf_422_in (24)
nf_write_luma	Noise Filter Data Write 420 Luma	179	YUV (0x1, 0x2, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	nf_420_y_out (23)
nf_write_chroma	Noise Filter Data Write 420 Chroma	180	YUV (0x6, 0x5)	nf_420_uv_out (23)
nf_last_luma	Noise Filter Previous Frame 420 Luma	181	YUV (0x2)	nf_420_y_in (22)
nf_last_chroma	Noise Filter Previous Frame 420 Chroma	182	YUV (0x6, 0x5)	nf_420_uv_in (22)
vbi_sd_venc	SD Video Encoder VBI Data	184	OTHER (8)	vbi_sdvenc (19)
post_comp_wr	Scaled Compositor or Transcode Writeback to Memory	185	YUV (0x7)	hdmi_wrbk_out (5)
pip_frame	422I Video Input to Compositor (no scaling)	186	YUV (0x7)	pip_wrbk (10)
aux_in	422I Video Input to Compositor (no scaling)	187	YUV (0x7)	comp_wrbk (11)
transcode1_luma	Independent Transcode Path 0 Luma	188	YUV (0x1, 0x2, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	trans1_luma (3)
transcode1_chroma	Independent Transcode Path 0 Chroma	189	YUV (0x5, 0x6, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	trans1_chroma (3)
transcode2_luma	Independent Transcode Path 0 Luma	190	YUV (0x1, 0x2, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	trans2_luma (18)
transcode2_chroma	Independent Transcode Path 0 Chroma	191	YUV (0x5, 0x6, 0x7 If data type 0x7 is used half the data fetched will be thrown out.)	trans2_chroma (18)

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Table 1-106 lists for each client the channels used, amount of buffering allocated for it, and the shared buffer used for its memory.

Table 1-106. VPDMA Client Buffering

Client	Channel(s)	Buffering	Shared Buffer
dei_hq_1_chroma	hq_vid1_chroma	11520	DEI_MQ_VID
dei_hq_1_luma	hq_vid1_luma	7680	HD_DEI_VID
dei_hq_2_luma	hq_vid2_luma	7680	DEI_MQ_VID
dei_hq_2_chroma	hq_vid2_chroma	11520	HD_DEI_VID
dei_hq_3_luma	hq_vid3_luma	7680	DEI_MQ_VID1
dei_hq_3_chroma	hq_vid3_chroma	11520	HD_DEI_VID1
dei_hq_mv_in	hq_mv	4096	MV
dei_hq_mv_out	hq_mv_out	4096	MV
dei_sc_out	hq_scaler	4096	MEM_TO_MEM
pip_wrbk	pip_frame	4096	MEM_TO_MEM1
sc_in_chroma	scaler_chroma	11520	DEI_MQ_VID1
sc_in_luma	scaler_luma	7680	TRANS_VID0
sc_out	scaler_out	4096	MEM_TO_MEM
comp_wrbk	aux_in	4096	MEM_TO_MEM1
grpx1_data	grpx1	4096	GRPX_BUF
grpx2_data	grpx2	4096	GRPX_BUF1
grpx3_data	grpx3	4096	MV
vip1_lo_y	vip1_mult_porta_src0 vip1_mult_porta_src1 vip1_mult_porta_src2 vip1_mult_porta_src3 vip1_mult_porta_src4 vip1_mult_porta_src5 vip1_mult_porta_src6 vip1_mult_porta_src7 vip1_mult_porta_src8 vip1_mult_porta_src9 vip1_mult_porta_src10 vip1_mult_porta_src11 vip1_mult_porta_src12 vip1_mult_porta_src13 vip1_mult_porta_src14 vip1_mult_porta_src15 vip1_portb_luma vip1_portb_rgb	11520	VP_WR
vip1_lo_uv	vip1_mult_portb_src0 vip1_mult_portb_src1 vip1_mult_portb_src2 vip1_mult_portb_src3 vip1_mult_portb_src4 vip1_mult_portb_src5 vip1_mult_portb_src6 vip1_mult_portb_src7 vip1_mult_portb_src8 vip1_mult_portb_src9 vip1_mult_portb_src10 vip1_mult_portb_src11 vip1_mult_portb_src12 vip1_mult_portb_src13 vip1_mult_portb_src14 vip1_mult_portb_src15 vip1_portb_chroma	11520	VP_WR
vip1_up_y	vip1_porta_luma vip1_porta_rgb	11520	VP_WR
vip1_up_uv	vip1_porta_chroma	11520	VP_WR

Table 1-106. VPDMA Client Buffering (continued)

Client	Channel(s)	Buffering	Shared Buffer
vip2_lo_y	vip2_mult_porta_src0 vip2_mult_porta_src1 vip2_mult_porta_src2 vip2_mult_porta_src3 vip2_mult_porta_src4 vip2_mult_porta_src5 vip2_mult_porta_src6 vip2_mult_porta_src7 vip2_mult_porta_src8 vip2_mult_porta_src9 vip2_mult_porta_src10 vip2_mult_porta_src11 vip2_mult_porta_src12 vip2_mult_porta_src13 vip2_mult_porta_src14 vip2_mult_porta_src15 vip2_portb_luma vip2_portb_rgb	11520	VP_WR2
vip2_lo_uv	vip2_mult_portb_src0 vip2_mult_portb_src1 vip2_mult_portb_src2 vip2_mult_portb_src3 vip2_mult_portb_src4 vip2_mult_portb_src5 vip2_mult_portb_src6 vip2_mult_portb_src7 vip2_mult_portb_src8 vip2_mult_portb_src9 vip2_mult_portb_src10 vip2_mult_portb_src11 vip2_mult_portb_src12 vip2_mult_portb_src13 vip2_mult_portb_src14 vip2_mult_portb_src15 vip2_portb_chroma	11520	VP_WR2
vip2_up_y	vip2_porta_luma vip2_porta_rgb	11520	VP_WR2
vip2_up_uv	vip2_porta_chroma	11520	VP_WR2
grpx1_st	grpx1_stencil	1024	GRPX_BUF
grpx2_st	grpx2_stencil	1024	GRPX_BUF1
grpx3_st	grpx3_stencil	1024	MV
nf_422_in	nf_read	4096	NF_BUF
nf_420_y_in	nf_last_luma	4096	NF_BUF1
nf_420_uv_in	nf_last_chroma	4096	NF_BUF
nf_420_y_out	nf_write_luma	4096	NF_BUF1
nf_420_uv_out	nf_write_chroma	4096	NF_BUF
vbi_sdvenc	vbi_sd_venc	256	MEM_TO_MEM
vpi_ctl		1024	MEM_TO_MEM1
hdmi_wrbk_out	post_comp_wr	4096	MEM_TO_MEM
trans1_chroma	transcode1_chroma	11520	TRANS_VID0
trans1_luma	transcode1_luma	7680	TRANS_VID1
trans2_chroma	transcode2_chroma	11520	TRANS_VID2
trans2_luma	transcode2_luma	7680	TRANS_VID3

Table 1-106. VPDMA Client Buffering (continued)

Client	Channel(s)	Buffering	Shared Buffer
vip1_anc_a	vip1_mult_anca_src0 vip1_mult_anca_src1 vip1_mult_anca_src2 vip1_mult_anca_src3 vip1_mult_anca_src4 vip1_mult_anca_src5 vip1_mult_anca_src6 vip1_mult_anca_src7 vip1_mult_anca_src8 vip1_mult_anca_src9 vip1_mult_anca_src10 vip1_mult_anca_src11 vip1_mult_anca_src12 vip1_mult_anca_src13 vip1_mult_anca_src14 vip1_mult_anca_src15	0	VP_WR
vip1_anc_b	vip1_mult_ancb_src0 vip1_mult_ancb_src1 vip1_mult_ancb_src2 vip1_mult_ancb_src3 vip1_mult_ancb_src4 vip1_mult_ancb_src5 vip1_mult_ancb_src6 vip1_mult_ancb_src7 vip1_mult_ancb_src8 vip1_mult_ancb_src9 vip1_mult_ancb_src10 vip1_mult_ancb_src11 vip1_mult_ancb_src12 vip1_mult_ancb_src13 vip1_mult_ancb_src14 vip1_mult_ancb_src15	0	VP_WR
vip2_anc_a	vip2_mult_anca_src0 vip2_mult_anca_src1 vip2_mult_anca_src2 vip2_mult_anca_src3 vip2_mult_anca_src4 vip2_mult_anca_src5 vip2_mult_anca_src6 vip2_mult_anca_src7 vip2_mult_anca_src8 vip2_mult_anca_src9 vip2_mult_anca_src10 vip2_mult_anca_src11 vip2_mult_anca_src12 vip2_mult_anca_src13 vip2_mult_anca_src14 vip2_mult_anca_src15	0	VP_WR2

1.2.13.4.3 hd_dss_vpdma Client Functionality

Table 1-107 lists for each client the sizes it handles for tiled and non-tiled memory spaces as well as any additional features it supports such as Virtual Video Buffering, 1D descriptor field.

Table 1-107. HDVPSS Client Functionality

Client	Tiled Memory Max Line Size	Non-Tiled Memory Max Line Size	Additional Features
dei_hq_1_chroma	1920	1920	Virtual Video Buffer with line buffer limitations, TILED
dei_hq_1_luma	1920	4096	Virtual Video Buffer, TILED
dei_hq_2_luma	1920	4096	Virtual Video Buffer, TILED
dei_hq_2_chroma	1920	1920	Virtual Video Buffer with line buffer limitations, TILED
dei_hq_3_luma	1920	4096	Virtual Video Buffer, TILED
dei_hq_3_chroma	1920	1920	Virtual Video Buffer with line buffer limitations, TILED
dei_hq_mv_in	Tiled Data Not Supported	4096	
dei_hq_mv_out	Tiled Data Not Supported	4096	
dei_sc_out	Tiled Data Not Supported	4096	
pip_wrbk	Tiled Data Not Supported	4096	Virtual Video Buffer
sc_in_chroma	1920	1920	Virtual Video Buffer with line buffer limitations, TILED
sc_in_luma	1920	4096	Virtual Video Buffer, TILED
sc_out	Tiled Data Not Supported	4096	
comp_wrbk	Tiled Data Not Supported	4096	Virtual Video Buffer
grpx1_data	Tiled Data Not Supported	4096	
grpx2_data	Tiled Data Not Supported	4096	
grpx3_data	Tiled Data Not Supported	4096	
vip1_lo_y	1920	4096	TILED
vip1_lo_uv	1920	4096	TILED
vip1_up_y	1920	4096	TILED
vip1_up_uv	1920	4096	TILED
vip2_lo_y	1920	4096	TILED
vip2_lo_uv	1920	4096	TILED
vip2_up_y	1920	4096	TILED
vip2_up_uv	1920	4096	TILED
grpx1_st	Tiled Data Not Supported	4096	
grpx2_st	Tiled Data Not Supported	4096	
grpx3_st	Tiled Data Not Supported	4096	
nf_422_in	Tiled Data Not Supported	4096	
nf_420_y_in	1920	4096	TILED
nf_420_uv_in	1920	4096	TILED
nf_420_y_out	1920	4096	TILED
nf_420_uv_out	1920	4096	TILED
vbi_sdvenc	Tiled Data Not Supported	4096	
vpi_ctl	Tiled Data Not Supported	4096	
hdmi_wrbk_out	Tiled Data Not Supported	4096	
trans1_chroma	1920	1920	Virtual Video Buffer with line buffer limitations, TILED
trans1_luma	1920	4096	Virtual Video Buffer, TILED
trans2_chroma	1920	1920	Virtual Video Buffer with line buffer limitations, TILED

Table 1-107. HDVPSS Client Functionality (continued)

Client	Tiled Memory Max Line Size	Non-Tiled Memory Max Line Size	Additional Features
trans2_luma	1920	4096	Virtual Video Buffer, TILED
vip1_anc_a	Tiled Data Not Supported	4096	
vip1_anc_b	Tiled Data Not Supported	4096	
vip2_anc_a	Tiled Data Not Supported	4096	

1.2.13.4.4 VPDMA Interrupts to HDVPSS

The VPDMA has 100 interrupts that it provides to the HDVPSS. These 100 interrupts are actually four groups of 25 interrupts, where the interrupts within each group are identical in terms of their contents, but can be masked independently within the HDVPSS to allow different processors to see different interrupts. Each group of 25 interrupts are mapped to each of the four interrupt outputs from the HDVPSS. The interrupts can fire for the completion of a channel, the completion of a client, completion of a list, a list channel notification completion, or a special event received by the List Manager. These 25 interrupts are additionally grouped by the VPDMA from a total of 251 interrupt sources.

Each of these 25 interrupts can have multiple sources within the VPDMA, and within the VPDMA there are separate status and masking controls to provide the additional layer of register reads to determine the exact source of the interrupt.

Table 1-108 shows all interrupt sources received by the HDVPSS from the VPDMA.

Table 1-108. HDVPSS Interrupt from VPDMA

Interrupt	Description
vpdma_int_channel_group0	An unmasked channel interrupt for interrupt group 0 in channel register 0 has fired.
vpdma_int_channel_group1	An unmasked channel interrupt for interrupt group 1 in channel register 0 has fired.
vpdma_int_channel_group2	An unmasked channel interrupt for interrupt group 2 in channel register 0 has fired.
vpdma_int_channel_group3	An unmasked channel interrupt for interrupt group 3 in channel register 0 has fired.
vpdma_int_channel_group4	An unmasked channel interrupt for interrupt group 4 in channel register 0 has fired.
vpdma_int_channel_group5	An unmasked channel interrupt for interrupt group 5 in channel register 0 has fired.
vpdma_int_channel_group6	An unmasked channel interrupt for interrupt group 6 in channel register 0 has fired.
vpdma_int_list0_complete	List 0 has completed
vpdma_int_list0_notify	The data transfer in list 0 with the Notify Field set in the descriptor has completed
vpdma_int_list1_complete	List 1 has completed
vpdma_int_list1_notify	The data transfer in list 1 with the Notify Field set in the descriptor has completed
vpdma_int_list2_complete	List 2 has completed
vpdma_int_list2_notify	The data transfer in list 2 with the Notify Field set in the descriptor has completed
vpdma_int_list3_complete	List 3 has completed
vpdma_int_list3_notify	The data transfer in list 3 with the Notify Field set in the descriptor has completed
vpdma_int_list4_complete	List 4 has completed
vpdma_int_list4_notify	The data transfer in list 4 with the Notify Field set in the descriptor has completed
vpdma_int_list5_complete	List 5 has completed
vpdma_int_list5_notify	The data transfer in list 5 with the Notify Field set in the descriptor has completed
vpdma_int_list6_complete	List 6 has completed
vpdma_int_list6_notify	The data transfer in list 6 with the Notify Field set in the descriptor has completed
vpdma_int_list7_complete	List 7 has completed
vpdma_int_list7_notify	The data transfer in list 7 with the Notify Field set in the descriptor has completed
vpdma_int_client	Client Interrupt
vpdma_int_descriptor	Descriptor Interrupt

As stated, the above 25 interrupts are replicated four times. Each group has a separate mask register and status register (described in Section 1.3.8.13 to Section 1.3.8.92). At HDVPSS level, these four groups are connected to the four external interrupts (described in Section 1.3.7.3 to Section 1.3.7.31). As such, the overall interrupt mechanism for software is two-tierd.

In the previous table, the “channel_group”, “client” and “descriptor” interrupts are actually a set of additional interrupts. When software receives an interrupt from a “channel_group,” “client,” or “descriptor” it must read the appropriate register within the VPDMA (described in Section 1.3.8.13 to Section 1.3.8.92 and use Table 1-109 to determine the actual interrupt.

Table 1-109. HDVPSS Interrupt Sources

Interrupt	Interrupt Group	Description
channel_aux_in	channel_group5	The last read DMA transaction has occurred for channel aux_in and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client comp_wrbk will now accept a new descriptor from the List Manager.
channel_grpx1	channel_group0	The last read DMA transaction has occurred for channel grpx1 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_data will now accept a new descriptor from the List Manager.
channel_grpx1_clut	channel_group1	The last write DMA transaction has completed for channel grpx1_clut. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client grpx1_clut_clt then the client will be fully empty at this point.
channel_grpx1_stencil	channel_group1	The last read DMA transaction has occurred for channel grpx1_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_st will now accept a new descriptor from the List Manager.
channel_grpx2	channel_group0	The last read DMA transaction has occurred for channel grpx2 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_data will now accept a new descriptor from the List Manager.
channel_grpx2_clut	channel_group1	The last write DMA transaction has completed for channel grpx2_clut. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client grpx2_clut_clt then the client will be fully empty at this point.
channel_grpx2_stencil	channel_group1	The last read DMA transaction has occurred for channel grpx2_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_st will now accept a new descriptor from the List Manager.
channel_grpx3	channel_group0	The last read DMA transaction has occurred for channel grpx3 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_data will now accept a new descriptor from the List Manager.
channel_grpx3_clut	channel_group1	The last write DMA transaction has completed for channel grpx3_clut. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client grpx3_clut_clt then the client will be fully empty at this point.
channel_grpx3_stencil	channel_group1	The last read DMA transaction has occurred for channel grpx3_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_st will now accept a new descriptor from the List Manager.
channel_hq_mv	channel_group0	The last read DMA transaction has occurred for channel hq_mv and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_hq_mv_in will now accept a new descriptor from the List Manager.
channel_hq_mv_out	channel_group0	The last write DMA transaction has completed for channel hq_mv_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_hq_mv_out then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_hq_scaler	channel_group0	The last write DMA transaction has completed for channel hq_scaler. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_sc_out then the client will be fully empty at this point.
channel_hq_vid1_chroma	channel_group0	The last write DMA transaction has completed for channel hq_vid1_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_hq_vid1_luma	channel_group0	The last write DMA transaction has completed for channel hq_vid1_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_hq_vid2_chroma	channel_group0	The last write DMA transaction has completed for channel hq_vid2_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_hq_vid2_luma	channel_group0	The last write DMA transaction has completed for channel hq_vid2_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_hq_vid3_chroma	channel_group0	The last write DMA transaction has completed for channel hq_vid3_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_hq_vid3_luma	channel_group0	The last write DMA transaction has completed for channel hq_vid3_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_nf_last_chroma	channel_group5	The last write DMA transaction has completed for channel nf_last_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_nf_last_luma	channel_group5	The last write DMA transaction has completed for channel nf_last_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_nf_read	channel_group5	The last read DMA transaction has occurred for channel nf_read and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_422_in will now accept a new descriptor from the List Manager.
channel_nf_write_chroma	channel_group5	The last write DMA transaction has completed for channel nf_write_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_nf_write_luma	channel_group5	The last write DMA transaction has completed for channel nf_write_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_pip_frame	channel_group5	The last read DMA transaction has occurred for channel pip_frame and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client pip_wrbk will now accept a new descriptor from the List Manager.
channel_post_comp_wr	channel_group5	The last write DMA transaction has completed for channel post_comp_wr. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client hdmi_wrbk_out then the client will be fully empty at this point.
channel_scaler_chroma	channel_group0	The last write DMA transaction has completed for channel scaler_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_scaler_luma	channel_group0	The last write DMA transaction has completed for channel scaler_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_scaler_out	channel_group0	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point.
channel_transcode1_chroma	channel_group5	The last write DMA transaction has completed for channel transcode1_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_transcode1_luma	channel_group5	The last write DMA transaction has completed for channel transcode1_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_transcode2_chroma	channel_group5	The last write DMA transaction has completed for channel transcode2_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_transcode2_luma	channel_group5	The last write DMA transaction has completed for channel transcode2_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vbi_sd_venc	channel_group5	The last read DMA transaction has occurred for channel vbi_sd_venc and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client vbi_sdvenc will now accept a new descriptor from the List Manager.
channel_vip1_mult_anca_src0	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src1	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src10	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src11	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src12	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src13	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src14	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src15	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_anca_src2	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src3	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src4	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src5	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src6	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src7	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src8	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_anca_src9	channel_group2	The last write DMA transaction has completed for channel vip1_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point.
channel_vip1_mult_ancb_src0	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src1	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src10	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src11	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src12	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src13	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src14	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_ancb_src15	channel_group3	The last write DMA transaction has completed for channel vip1_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src2	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src3	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src4	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src5	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src6	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src7	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src8	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_ancb_src9	channel_group2	The last write DMA transaction has completed for channel vip1_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point.
channel_vip1_mult_porta_src0	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src1	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src10	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src11	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src12	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src13	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_porta_src14	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src15	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src2	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src3	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src4	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src5	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src6	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src7	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src8	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_porta_src9	channel_group1	The last write DMA transaction has completed for channel vip1_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip1_mult_portb_src0	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src1	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src10	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src11	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src12	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_mult_portb_src13	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src14	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src15	channel_group2	The last write DMA transaction has completed for channel vip1_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src2	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src3	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src4	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src5	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src6	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src7	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src8	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_mult_portb_src9	channel_group1	The last write DMA transaction has completed for channel vip1_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point.
channel_vip1_porta_chroma	channel_group3	The last write DMA transaction has completed for channel vip1_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip1_porta_luma	channel_group3	The last write DMA transaction has completed for channel vip1_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip1_porta_rgb	channel_group3	The last write DMA transaction has completed for channel vip1_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_up_y then the client will be fully empty at this point.
channel_vip1_portb_chroma	channel_group3	The last write DMA transaction has completed for channel vip1_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip1_portb_luma	channel_group3	The last write DMA transaction has completed for channel vip1_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip1_portb_rgb	channel_group3	The last write DMA transaction has completed for channel vip1_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point.
channel_vip2_mult_anca_src0	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src1	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src10	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src11	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src12	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src13	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src14	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src15	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src2	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src3	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src4	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src5	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src6	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_anca_src7	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src8	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_anca_src9	channel_group4	The last write DMA transaction has completed for channel vip2_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point.
channel_vip2_mult_ancb_src0	channel_group4	The last write DMA transaction has completed for channel vip2_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src1	channel_group4	The last write DMA transaction has completed for channel vip2_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src10	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src11	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src12	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src13	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src14	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src15	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src2	channel_group4	The last write DMA transaction has completed for channel vip2_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src3	channel_group4	The last write DMA transaction has completed for channel vip2_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src4	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src5	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_ancb_src6	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src7	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src8	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_ancb_src9	channel_group5	The last write DMA transaction has completed for channel vip2_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point.
channel_vip2_mult_porta_src0	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src1	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src10	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src11	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src12	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src13	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src14	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src15	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src2	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src3	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src4	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_porta_src5	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src6	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src7	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src8	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_porta_src9	channel_group3	The last write DMA transaction has completed for channel vip2_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
channel_vip2_mult_portb_src0	channel_group3	The last write DMA transaction has completed for channel vip2_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src1	channel_group3	The last write DMA transaction has completed for channel vip2_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src10	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src11	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src12	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src13	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src14	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src15	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src2	channel_group3	The last write DMA transaction has completed for channel vip2_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src3	channel_group3	The last write DMA transaction has completed for channel vip2_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
channel_vip2_mult_portb_src4	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src5	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src6	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src7	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src8	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_mult_portb_src9	channel_group4	The last write DMA transaction has completed for channel vip2_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point.
channel_vip2_porta_chroma	channel_group5	The last write DMA transaction has completed for channel vip2_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip2_porta_luma	channel_group5	The last write DMA transaction has completed for channel vip2_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip2_porta_rgb	channel_group5	The last write DMA transaction has completed for channel vip2_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_up_y then the client will be fully empty at this point.
channel_vip2_portb_chroma	channel_group5	The last write DMA transaction has completed for channel vip2_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip2_portb_luma	channel_group5	The last write DMA transaction has completed for channel vip2_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point.
channel_vip2_portb_rgb	channel_group5	The last write DMA transaction has completed for channel vip2_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point.
client_comp_wrbk	client	The client interface comp_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_dei_hq_1_chroma	client	The client interface dei_hq_1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_dei_hq_1_luma	client	The client interface dei_hq_1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
client_dei_hq_2_chroma	client	The client interface dei_hq_2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_dei_hq_2_luma	client	The client interface dei_hq_2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_dei_hq_3_chroma	client	The client interface dei_hq_3_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_dei_hq_3_luma	client	The client interface dei_hq_3_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_dei_hq_mv_in	client	The client interface dei_hq_mv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_dei_hq_mv_out	client	The client interface dei_hq_mv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_dei_sc_out	client	The client interface dei_sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_grpx1_data	client	The client interface grpx1_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_grpx1_st	client	The client interface grpx1_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_grpx2_data	client	The client interface grpx2_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_grpx2_st	client	The client interface grpx2_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_grpx3_data	client	The client interface grpx3_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_grpx3_st	client	The client interface grpx3_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_hdmi_wrbk_out	client	The client interface hdmi_wrbk_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_nf_420_uv_in	client	The client interface nf_420_uv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
client_nf_420_uv_out	client	The client interface nf_420_uv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_nf_420_y_in	client	The client interface nf_420_y_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_nf_420_y_out	client	The client interface nf_420_y_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_nf_422_in	client	The client interface nf_422_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_pip_wrbk	client	The client interface pip_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_sc_in_chroma	client	The client interface sc_in_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_sc_in_luma	client	The client interface sc_in_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_sc_out	client	The client interface sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_trans1_chroma	client	The client interface trans1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_trans1_luma	client	The client interface trans1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_trans2_chroma	client	The client interface trans2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_trans2_luma	client	The client interface trans2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_vbi_sdvenc	client	The client interface vbi_sdvenc has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
client_vip1_anc_a	client	The client interface vip1_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip1_anc_b	client	The client interface vip1_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
client_vip1_lo_uv	client	The client interface vip1_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip1_lo_y	client	The client interface vip1_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip1_up_uv	client	The client interface vip1_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip1_up_y	client	The client interface vip1_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_anc_a	client	The client interface vip2_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_anc_b	client	The client interface vip2_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_lo_uv	client	The client interface vip2_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_lo_y	client	The client interface vip2_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_up_uv	client	The client interface vip2_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vip2_up_y	client	The client interface vip2_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module.
client_vpi_ctl	client	The client interface vpi_ctl has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module.
control_descriptor_int0	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 0.
control_descriptor_int1	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 1.
control_descriptor_int10	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 10.
control_descriptor_int11	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 11.
control_descriptor_int12	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 12.
control_descriptor_int13	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 13.
control_descriptor_int14	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 14.
control_descriptor_int15	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 15.

Table 1-109. HDVPSS Interrupt Sources (continued)

Interrupt	Interrupt Group	Description
control_descriptor_int2	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 2.
control_descriptor_int3	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 3.
control_descriptor_int4	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 4.
control_descriptor_int5	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 5.
control_descriptor_int6	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 6.
control_descriptor_int7	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 7.
control_descriptor_int8	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 8.
control_descriptor_int9	descriptor	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 9.

1.2.13.5 VPDMA Configuration

The following section describes the different ways of configuring VPDMA for data transfers.

1.2.13.5.1 Regular List

A regular list executes each descriptor in order until the end of the list is reached. When the end of the list is reached an interrupt is sent and the list can be reused by software. A regular list can contain any descriptor types. Software creates the list at some location in external memory. After completing writing the list software then writes the location of the list to the LIST_ADDRESS register and then writes the LIST_ATTRIBUTE register. If the NUMBER in the LIST_ATTRIBUTE is not an active list then the List will be loaded and begin to execute the next time the List Manager gets to IDLE after processing previous loaded lists. If the NUMBER in the LIST_ATTRIBUTE is busy then the LIST_ADDRESS and LIST_ATTRIBUTE registers will be locked until the active list specified by NUMBER completes. Any writes to the LIST_ADDRESS or LIST_ATTRIBUTE will result in mmr_wready being held inactive until the list is freed.

The different ports inside VPDMA requires different list setup.

1.2.13.5.1.1 Video Input Ports

The Video Input Ports (VIP) can be used in multiple ways. Depending on how the input ports are configured will determine how the lists to manage them need to be setup. The ways in which the ports can work are multiplexed data stream, single YUV color separate stream, dual YUV interleaved or single RGB stream. Each port also has an ancillary data port that can run either multiplexed or single data stream and shares the buffering with the main data stream. For all cases the descriptor must be loaded into the client before the vertical sync is received on the VIP port or the entire frame will be dropped. As with all write clients the VIP channels can be shadowed so the next frame/field descriptor can be loaded while the previous frame is running without stalling the list.

1.2.13.5.1.1.1 Multiplexed Data Streams

In the case of a multiplexed data stream input the channels that should be used are VIPX_PORTY_MULT_SRCZ. Where X is the specific VIP port that wants to be used and port Y is the port A or port B that is receiving the data. Finally Z is the channel number. For Split line mux mode the LSB of the channel will determine if the line is a split line or a complete line. This is required so that the data streams do not get mixed when a channel ends without completing a line. In this mode the data will always be sent out as 422 Interleaved data to the destination specified in the descriptor.

1.2.13.5.1.1.2 Single YUV Color Separate

If the port is configured to be used as sending out color separated YUV data then the channels that must be used are VIPX_PORTY_LUMA and VIPX_PORTY_CHROMA for the luma and chroma components respectively. The data type can be either 420 or 422 color separate in this case.

1.2.13.5.1.1.3 Dual YUV Interleaved

If the port is configured to be used to send out 422 interleaved data from a non-multiplexed source then the channels that must be used are VIPX_PORTY_LUMA or VIPX_PORTY_CHROMA depending on if the data stream is connected to the luma or chroma port. The data type must be 422 interleaved in this case.

1.2.13.5.1.1.4 Single RGB Stream

If the port is configured to be used to send out RGB stream then the channel VIPX_PORTY_RGB must be used. The incoming data is then assumed to be RGB 888 data and this is combined with the Background Color Alpha register field to make ARGB8888 data that will then be sent out based on the data type. If the data type uses less then the full 8 bits the lower bits are dropped and just the upper bits are sent to get the correct data format.

1.2.13.5.1.2 De-Interlacers (DEIs)

The DEIs have two areas that require special handling in setting up the descriptors. The first is with the line buffers. The line buffer must be set to match the mode that the chroma upsampler and the DEI expect to receive for chroma and luma respectively. Refer to the Chroma Upsampler specification for the settings for the chroma client. The luma client should use the same settings for the chroma assuming that the data type is 422. The line buffer mode is set by the CSTAT register for the client. This value is not shadowed and must be set before the descriptor is loaded and can not be changed until the client has finished. This can be accomplished by using a Sync on Client Not Active control descriptor prior to a configuration descriptor to change the line mode. The video clients also must have the 1D descriptor field set to 1 if compression and decompression is used for the field data. Also, if the compression and decompression are set then the write channel descriptors must also generate the next inbound descriptor as this is the only way to know the size of the outbound data that will be the inbound data for the next frame.

1.2.13.5.1.3 Transcode Paths

The transcode paths must set the chroma line buffer to match the chroma upsampler in the transcode path. Refer to the Chroma Upsampler specification for the settings for the chroma client. The line buffer mode is set by the CSTAT register for the client. This value is not shadowed and must be set before the descriptor is loaded and can not be changed until the client has finished. This can be accomplished by using a Sync on Client Not Active control descriptor prior to a configuration descriptor to change the line mode.

1.2.13.5.1.4 Noise Filter (NF)

The noise filter clients break the frame into 32 by 32 tiles for 422 data and 420 Luma data. The noise filter clients break 420 chroma data into 32x16 tiles. The incoming 422 frame should be evenly divisible by 32 by 32. The outgoing frame buffers should leave enough space for a frame that is evenly divisible by 32 by 32 for luma and 32 by 16 for chroma.

1.2.13.5.1.5 Graphics

The graphics ports in this device are tightly coupled with the VPDMA clients that service them. Each graphics port expects a list of data descriptors to describe each region that make up the frame.

1.2.13.5.1.5.1 Region Descriptor

The Graphics module uses the standard Inbound data transfer descriptor as all other channel but it has additional information in the Client Specific Attributes field that are passed down to the Graphics processing module.

Table 1-110. Graphics Region Descriptor Format

Attribute	Location	Description
Region_Height	Word 4 Bits 15:0	Height of the region
Region Width	Word 4 Bits 31:16	The number of pixels wide for the region
Vertical Start	Word 5 Bits 15:0	position of region (Y origin) 0 is top of frame
Horizontal Start	Word 5 Bits 31:16	position of region (X origin) 0 is left side of frame
Disp_pri	Word 6 Bits 3:0	Region display priority 0x0 is on the bottom 0xF is on the top
First Region	Word 6 Bit 7	Marks the region as the first region in a new frame. This bit must be set to 1 on the first region only
Last Region	Word 6 Bit 8	Marks the last region in a frame. This bit must be set only on the last region. If only 1 region exists then both this and the First Region bit should be set
Scaler	Word 6 Bit 9	The region should be scaled using the current frames resizer configuration
AF	Word 6 Bit 10	The region should be passed through the scaler to Anti-flicker the data
Stencil	Word 6 Bit 11	The region should use the stencil client applied to this data. A separate data descriptor for the stencil data must be created and should have been the data descriptor in the list prior to the current region descriptor.
Reserved	[76:78]	Reserved
bbox	Word 6 Bit 15	A single pixel bounding box should be applied along the region with the alpha value of the data replaced with the alpha data in the bb_alpha field.
bb_alpha	Word 6 Bit 23:16	The alpha value to use for the bounding box if it is enabled.
blend_alpha	Word 6 Bit 31:24	The alpha value to use if the blend_type field is set for Region global blending.
blend_type	Word 7 Bits 1:0	The type of blending to perform on the region. This is used to replace the alpha value presented to the Graphics module. 0 — no blending 1 — Region global blending 2 — reserved. (color (palette) Blending) 3 — Pixel (embedded alpha) Blending
trans_enable	Word 7 Bit 5	Enable transparency for the region. If this is set the trans_cfg and trans_color fields are used to replace the alpha of a specific color to make it transparent
tr_lsb_mask	Word 7 Bits 7-6	Transparency LSB bit masking 0 0 : No masking 01 : Mask [0] during pixel data comparison to TRANS_COLOR 1 0 : Mask[1:0] 1 1 : Mask[2:0] ex)., if TR_LSB_MASK is set to 2'b11, top 5 bits of R/G/B component data are compared to the corresponding 5 bits of TRANS_COLOR R/G/B color.
trans color	Word 7 Bits 31:8	Transparency Color (RGB24)

1.2.13.5.1.5.2 Frame Configuration Descriptors

The graphics module also requires its configuration through the use of Configuration descriptors. The Graphics module can accept a frame configuration packet with or without the resizer settings. The frame must be configured before starting the graphics port for its first frame but a new configuration descriptor is not required unless either the frame attributes or the resizer attributes are changing from the previous frame.

Table 1-111. Frame Configuration Descriptor Format

Attribute	Location	Value
Packet Type	Header Word 3 Bits 31:27	0xb
Direct	Header Word 3 Bit 26	Direct Command = 1 Indirect Command = 0
Class	Header Word 3 Bits 25:24	1 = Block
Destination	Header Word 3 Bits 23:16	Graphics port that the frame is being configured.
Payload Length	Header Word 3 Bits 15:0	1
Length	Header Word 2 Bits 31:24	1
Address	Header Word 2 Bits 23:0	1
Payload Location	Header Word 1 Bits 31:0	Address of the Payload if Indirect Command
frame_height	Payload Word 1 Bits 15:0	Frame height
frame_width	Payload Word 1 Bits 31:16	Frame width
src_fmt_interlaced	Payload Word 3 Bit 30	Format of the source image: 0 = Progressive 1 = Interlaced
Soft Reset	Payload Word 3 Bit 31	Software reset of GRPX data pipeline

Table 1-112. Frame with Resizer Configuration Descriptor Format

Attribute	Location	Value
Packet Type	Header Word 3 Bits 31:27	0xb
Direct	Header Word 3 Bit 26	Direct Command = 1 Indirect Command = 0
Class	Header Word 3 Bits 25:24	1 = Block
Destination	Header Word 3 Bits 23:16	Graphics port that the frame is being configured.
Payload Length	Header Word 3 Bits 15:0	12
Length	Header Word 2 Bits 31:24	12
Address	Header Word 2 Bits 23:0	1
Payload Location	Header Word 1 Bits 31:0	Address of the Payload if Indirect Command
frame_height	Payload Word 1 Bits 15:0	Frame height
frame_width	Payload Word 1 Bits 31:16	Frame width
src_fmt_interlaced	Payload Word 3 Bit 30	Format of the source image: 0 = Progressive 1 = Interlaced
Soft Reset	Payload Word 3 Bit 31	Software reset of GRPX data pipeline
coefh0_p0	Payload Word 4 Bits 9:0	Coefficient for Horizontal TAP 0 Phase 0
coefh0_p1	Payload Word 4 Bits 25:16	Coefficient for Horizontal TAP 0 Phase 1
coefh0_p2	Payload Word 5 Bits 9:0	Coefficient for Horizontal TAP 0 Phase 2
coefh0_p3	Payload Word 5 Bits 25:16	Coefficient for Horizontal TAP 0 Phase 3
coefh0_p4	Payload Word 6 Bits 9:0	Coefficient for Horizontal TAP 0 Phase 4
coefh0_p5	Payload Word 6 Bits 25:16	Coefficient for Horizontal TAP 0 Phase 5
coefh0_p6	Payload Word 7 Bits 9:0	Coefficient for Horizontal TAP 0 Phase 6
coefh0_p7	Payload Word 7 Bits 25:16	Coefficient for Horizontal TAP 0 Phase 7

Table 1-112. Frame with Resizer Configuration Descriptor Format (continued)

Attribute	Location	Value
coefh1_p0	Payload Word 8 Bits 9:0	Coefficient for Horizontal TAP 1 Phase 0
coefh1_p1	Payload Word 8 Bits 25:16	Coefficient for Horizontal TAP 1 Phase 1
coefh1_p2	Payload Word 9 Bits 9:0	Coefficient for Horizontal TAP 1 Phase 2
coefh1_p3	Payload Word 9 Bits 25:16	Coefficient for Horizontal TAP 1 Phase 3
coefh1_p4	Payload Word 10 Bits 9:0	Coefficient for Horizontal TAP 1 Phase 4
coefh1_p5	Payload Word 10 Bits 25:16	Coefficient for Horizontal TAP 1 Phase 5
coefh1_p6	Payload Word 11 Bits 9:0	Coefficient for Horizontal TAP 1 Phase 6
coefh1_p7	Payload Word 11 Bits 25:16	Coefficient for Horizontal TAP 1 Phase 7
coefh2_p0	Payload Word 12 Bits 9:0	Coefficient for Horizontal TAP 2 Phase 0
coefh2_p1	Payload Word 12 Bits 25:16	Coefficient for Horizontal TAP 2 Phase 1
coefh2_p2	Payload Word 13 Bits 9:0	Coefficient for Horizontal TAP 2 Phase 2
coefh2_p3	Payload Word 13 Bits 25:16	Coefficient for Horizontal TAP 2 Phase 3
coefh2_p4	Payload Word 14 Bits 9:0	Coefficient for Horizontal TAP 2 Phase 4
coefh2_p5	Payload Word 14 Bits 25:16	Coefficient for Horizontal TAP 2 Phase 5
coefh2_p6	Payload Word 15 Bits 9:0	Coefficient for Horizontal TAP 2 Phase 6
coefh2_p7	Payload Word 15 Bits 25:16	Coefficient for Horizontal TAP 2 Phase 7
coefh3_p0	Payload Word 16 Bits 9:0	Coefficient for Horizontal TAP 3 Phase 0
coefh3_p1	Payload Word 16 Bits 25:16	Coefficient for Horizontal TAP 3 Phase 1
coefh3_p2	Payload Word 17 Bits 9:0	Coefficient for Horizontal TAP 3 Phase 2
coefh3_p3	Payload Word 17 Bits 25:16	Coefficient for Horizontal TAP 3 Phase 3
coefh3_p4	Payload Word 18 Bits 9:0	Coefficient for Horizontal TAP 3 Phase 4
coefh3_p5	Payload Word 18 Bits 25:16	Coefficient for Horizontal TAP 3 Phase 5
coefh3_p6	Payload Word 19 Bits 9:0	Coefficient for Horizontal TAP 3 Phase 6
coefh3_p7	Payload Word 19 Bits 25:16	Coefficient for Horizontal TAP 3 Phase 7
coefh4_p0	Payload Word 20 Bits 9:0	Coefficient for Horizontal TAP 4 Phase 0
coefh4_p1	Payload Word 20 Bits 25:16	Coefficient for Horizontal TAP 4 Phase 1
coefh4_p2	Payload Word 21 Bits 9:0	Coefficient for Horizontal TAP 4 Phase 2
coefh4_p3	Payload Word 21 Bits 25:16	Coefficient for Horizontal TAP 4 Phase 3
coefh4_p4	Payload Word 22 Bits 9:0	Coefficient for Horizontal TAP 4 Phase 4
coefh4_p5	Payload Word 22 Bits 25:16	Coefficient for Horizontal TAP 4 Phase 5
coefh4_p6	Payload Word 23 Bits 9:0	Coefficient for Horizontal TAP 4 Phase 6
coefh4_p7	Payload Word 23 Bits 25:16	Coefficient for Horizontal TAP 4 Phase 7
countvalhorz	Payload Word 24 Bits 14:0	Numerator value for fractional counter countval / 2048
fineoffsethorz	Payload Word 24 Bits 30:16	Count offset for start of line
coefv0_p0	Payload Word 25 Bits 9:0	Coefficient for Vertical TAP 0 Phase 0
coefv0_p1	Payload Word 25 Bits 25:16	Coefficient for Vertical TAP 0 Phase 1
coefv0_p2	Payload Word 26 Bits 9:0	Coefficient for Vertical TAP 0 Phase 2
coefv0_p3	Payload Word 26 Bits 25:16	Coefficient for Vertical TAP 0 Phase 3
coefv0_p4	Payload Word 27 Bits 9:0	Coefficient for Vertical TAP 0 Phase 4
coefv0_p5	Payload Word 27 Bits 25:16	Coefficient for Vertical TAP 0 Phase 5
coefv0_p6	Payload Word 28 Bits 9:0	Coefficient for Vertical TAP 0 Phase 6
coefv0_p7	Payload Word 28 Bits 25:16	Coefficient for Vertical TAP 0 Phase 7
coefv1_p0	Payload Word 29 Bits 9:0	Coefficient for Vertical TAP 1 Phase 0
coefv1_p1	Payload Word 29 Bits 25:16	Coefficient for Vertical TAP 1 Phase 1
coefv1_p2	Payload Word 30 Bits 9:0	Coefficient for Vertical TAP 1 Phase 2
coefv1_p3	Payload Word 30 Bits 25:16	Coefficient for Vertical TAP 1 Phase 3
coefv1_p4	Payload Word 31 Bits 9:0	Coefficient for Vertical TAP 1 Phase 4

Table 1-112. Frame with Resizer Configuration Descriptor Format (continued)

Attribute	Location	Value
coefv1_p5	Payload Word 31 Bits 25:16	Coefficient for Vertical TAP 1 Phase 5
coefv1_p6	Payload Word 32 Bits 9:0	Coefficient for Vertical TAP 1 Phase 6
coefv1_p7	Payload Word 32 Bits 25:16	Coefficient for Vertical TAP 1 Phase 7
coefv2_p0	Payload Word 33 Bits 9:0	Coefficient for Vertical TAP 2 Phase 0
coefv2_p1	Payload Word 33 Bits 25:16	Coefficient for Vertical TAP 2 Phase 1
coefv2_p2	Payload Word 34 Bits 9:0	Coefficient for Vertical TAP 2 Phase 2
coefv2_p3	Payload Word 34 Bits 25:16	Coefficient for Vertical TAP 2 Phase 3
coefv2_p4	Payload Word 35 Bits 9:0	Coefficient for Vertical TAP 2 Phase 4
coefv2_p5	Payload Word 35 Bits 25:16	Coefficient for Vertical TAP 2 Phase 5
coefv2_p6	Payload Word 36 Bits 9:0	Coefficient for Vertical TAP 2 Phase 6
coefv2_p7	Payload Word 36 Bits 25:16	Coefficient for Vertical TAP 2 Phase 7
coefv3_p0	Payload Word 37 Bits 9:0	Coefficient for Vertical TAP 3 Phase 0
coefv3_p1	Payload Word 37 Bits 25:16	Coefficient for Vertical TAP 3 Phase 1
coefv3_p2	Payload Word 38 Bits 9:0	Coefficient for Vertical TAP 3 Phase 2
coefv3_p3	Payload Word 38 Bits 25:16	Coefficient for Vertical TAP 3 Phase 3
coefv3_p4	Payload Word 39 Bits 9:0	Coefficient for Vertical TAP 3 Phase 4
coefv3_p5	Payload Word 39 Bits 25:16	Coefficient for Vertical TAP 3 Phase 5
coefv3_p6	Payload Word 40 Bits 9:0	Coefficient for Vertical TAP 3 Phase 6
coefv3_p7	Payload Word 40 Bits 25:16	Coefficient for Vertical TAP 3 Phase 7
countvalvert	Payload Word 41 Bits 14:0	Numerator value for fractional counter countval / 2048 coefv0_p0
fineoffsetvert	Payload Word 41 Bits 30:16	Count offset for start of line
rav_coef	Payload Word 42 Bits 8:0	Average Filter Coefficient
rav_factor	Payload Word 42 Bits 23:16	Average Filter accumulator averaging factor
rav_rowacc	Payload Word 43 Bits 7:0	Average Accumulator value weight

1.2.13.5.1.5.3 Example Graphics List

An example of how a graphics port can be configured will be shown using an example of three frames with the frame size changing. In this example, Figure 1-170 shows the output from the graphics module for the given list. Although in the example it is shown as one list it could just as easily be formatted as one list per frame with each list loaded when the previous list finishes.

Figure 1-170. Example Graphics Output

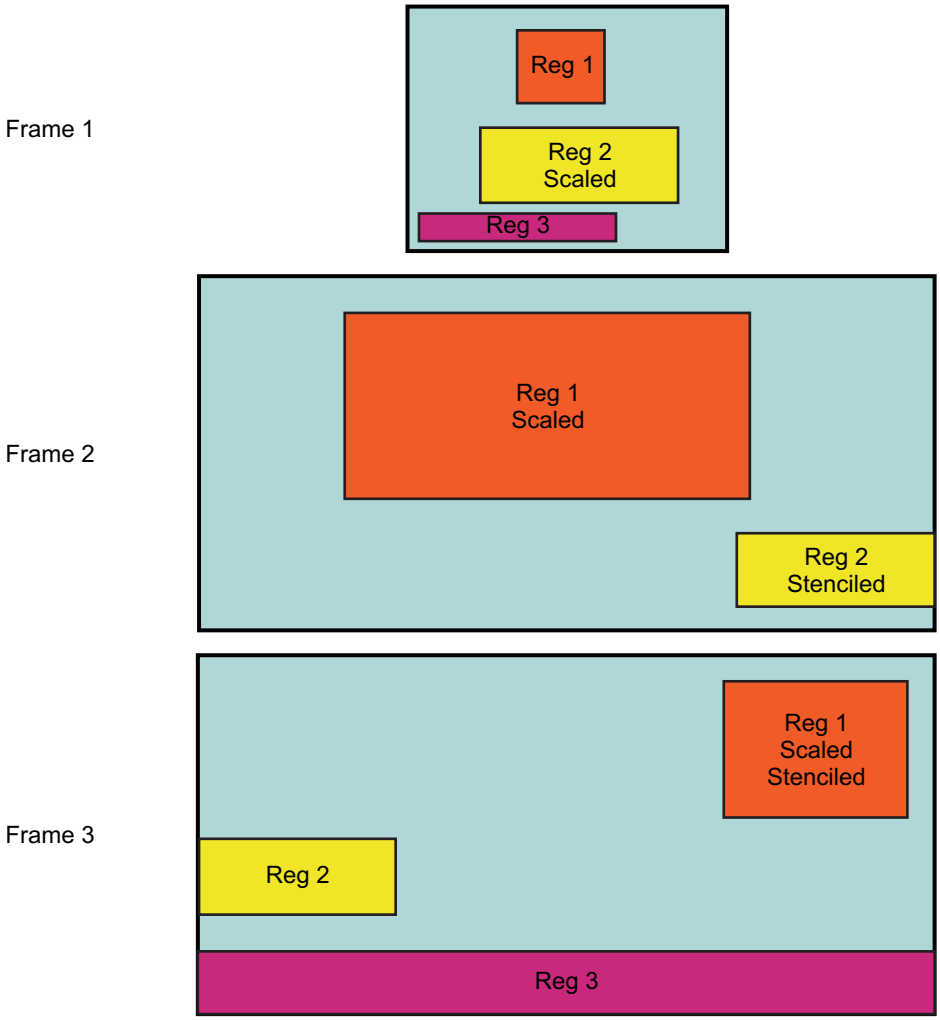


Table 1-113. Example Graphics List Description

Descriptor Type	Description	Size in 128 words
Configuration Descriptor	Sets up Frame 1 size and Scaler Coeficients must be indirect because of the size	1 Payload size 12
Data Transfer Descriptor	Sets up up region 1	2
Data Transfer Descriptor	Sets up up region 2 size is the pre-scaled size	2
Data Transfer Descriptor	Sets up region 3	2
Configuration Descriptor	Sets up Frame size for Frame 2. Assuming scaler setup stays the same so just a frame configuration is load. It can be direct or indirect.	2 (Direct) 1 (Indirect) 1 (Payload Size)
Data transfer descriptor	Sets up the region 1. Size is the pre-scaled size	2
Data transfer descriptor	Sets up the stencil data for region 2.	2
Data transfer descriptor	Sets up the data for region 2	2
Data transfer descriptor	Sets up the stencil data for region 1. Size is the pre-scaled size of region 1	2
Data transfer descriptor	Sets up the data for region 1	2
Data transfer descriptor	Sets up the data for region 2	2
Data transfer descriptor	Sets up the data for region 3	2

After this list is created in memory then the List Address would be written with location of the list. This would be followed with a write to the List Attribute register where a list number and setting the list size to either 23 if the direct list was used for the frame only configuration. If the indirect frame only descriptor is used then the list size would be 22.

1.2.13.5.1.6 List Configuration Example

To exercise different paths in VPSS, lists are to be prepared in memory to be processed by VPDMA. Consider the Transcode path. The input data is to be read in through Client no:8 (Channel 0 for Luma and Channel 1 for Chroma) and output is to be stored back in memory through client no:3 (Channel 102 YUV interleaved output).

The order to keep descriptors is as follows:

1. Configuration descriptors (To configure the Scaler in the path)
2. Outbound Descriptors
3. Inbound Descriptors

1.2.13.6 Data Formats

Each of the channels has a type of data that it can support based upon the client that it services. Also for each channel, the data type will assume that data is packed in memory a certain way and will be prevented to the client in the same manner to the client no matter what the format of the data in memory.

1.2.13.6.1 YUV Data Formats

The YUV formatted channels expect video data that is in YUV color space. The YUV data can be type is for YUV data and it can support both interleaved data where Luma and Chroma are in the same data buffer or it can support co-planar data where the Luma and Chroma are in separate data buffers. The YUV channel also can be given a position to give a different start position for the client instead of the default upper left hand corner of the frame. The storage format for YUV data depends on the data type field. The data type must be set to a data type that the channel can support. All the clients that data are provided too will either accept Luma Only, Chroma Only or Luma and Chroma in a parallel data bus.

1.2.13.6.1.1 Y 4:4:4 (Data Type 0)

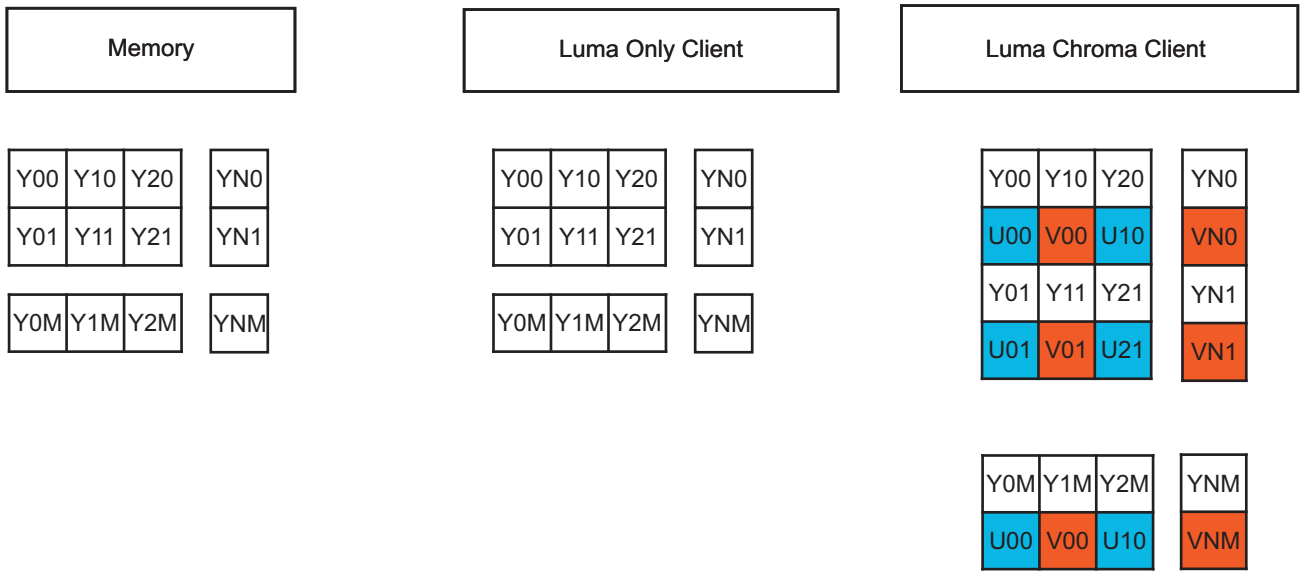
The Y 4:4:4 data type is used for a co-planar 4:4:4 data. In this mode the data is assumed to be a single byte with each pixel is packed in a line. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 8 bit container as described in the TILER specification. This data block should have the width and height set to the desired frame size expected by the receiving client.

Figure 1-171. Y 4:4:4 (Data Type 0)

1.2.13.6.1.2 Y 4:2:2 (Data Type 1)

The Y 4:2:2 data type is used for a co-planar 4:2:2 data. In this mode the data is assumed to be a single byte with each pixel is packed in a line. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 8 bit container as described in the TILER specification. This data block should have the width and the height of the desired frame sent by the VPDMA to the receive client.

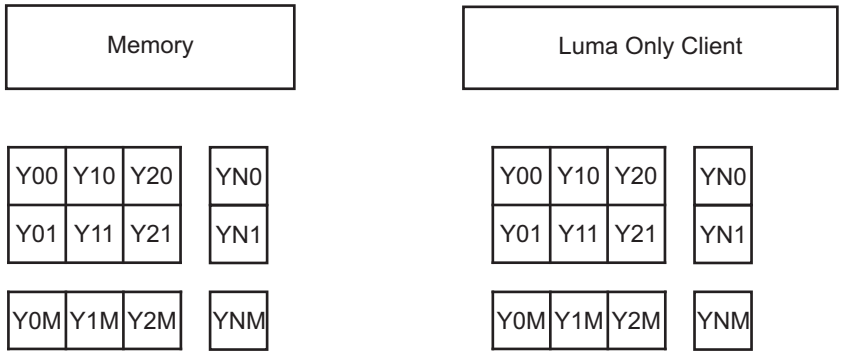
Figure 1-172. Y 4:2:2 (Data Type 1)



1.2.13.6.1.3 Y 4:2:0 (Data Type 2)

The Y 4:2:0 data type is used for a co-planar 4:2:0 data type. In this mode the data is assumed to be a single byte with each pixel is packed in a line. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 8 bit container as described in the TILER specification. This data block should have the width and the height of the expected frame for the client.

Figure 1-173. Y 4:2:0 (Data Type 2)



1.2.13.6.1.4 C 4:4:4 (Data Type 4)

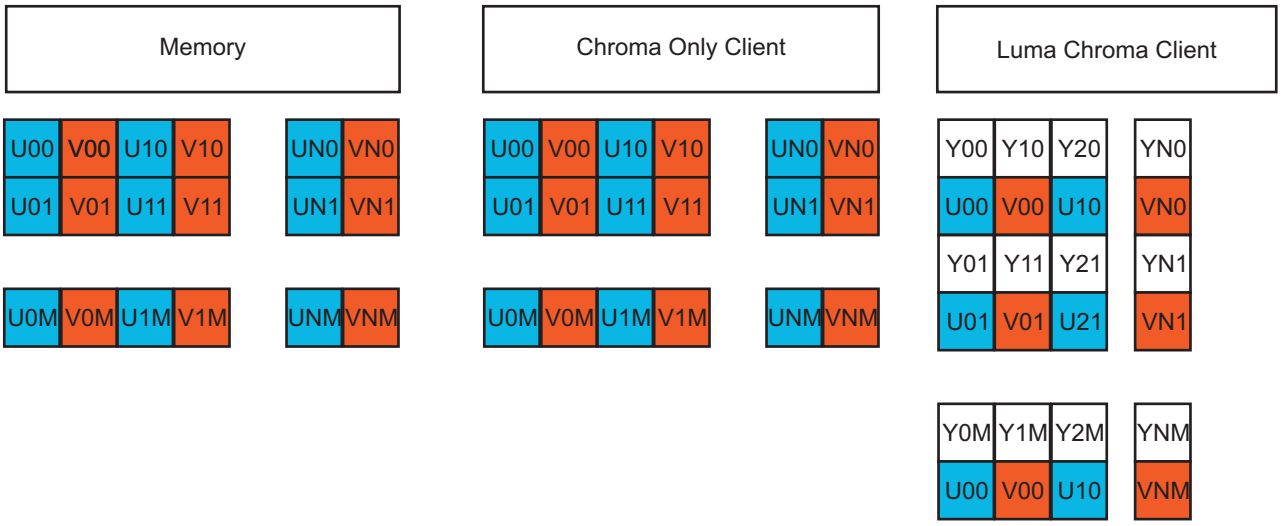
The C 4:4:4 data type is used for a co-planar 4:4:4 data. It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 16 bit container as described in the TILER specification. This data block should have the width and height of the expected client frame.

Figure 1-174. C 4:4:4 (Data Type 4)

1.2.13.6.1.5 C 4:2:2 (Data Type 5)

The C 4:2:2 data type is used for co-planar 4:2:2 data. It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 16 bit container as described in the TILER specification. This data block should have the width and the height of the expected client frame.

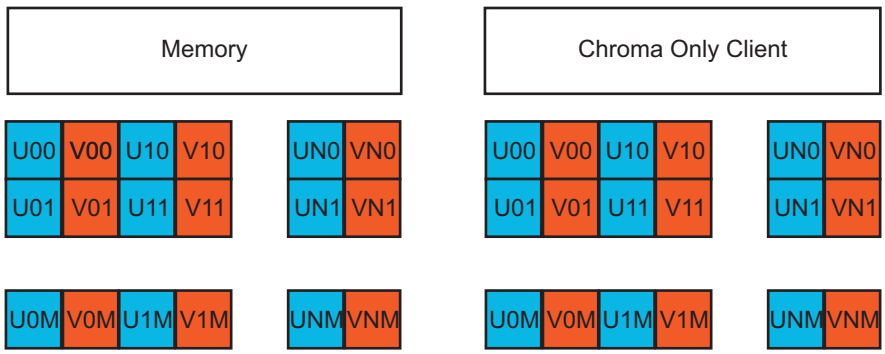
Figure 1-175. C 4:2:2 (Data Type 5)



1.2.13.6.1.6 C 4:2:0 (Data Type 6)

The C 4:2:0 data type is used for a co-planar 4:2:0 data. It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in a 16 bit container as described in the TILER specification. This data block should have the width and half the height of the expected clients frame.

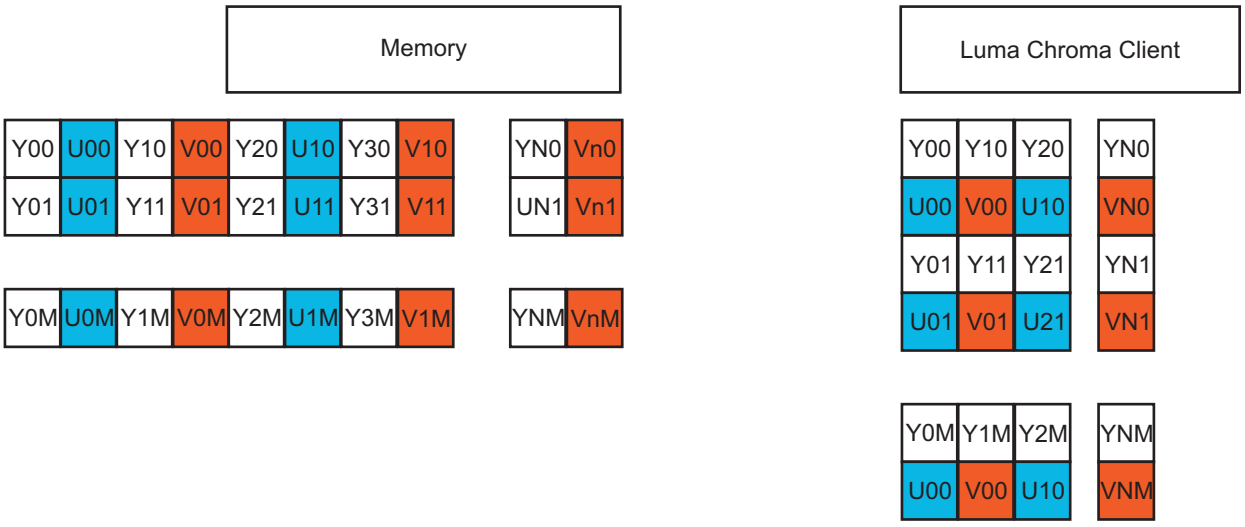
Figure 1-176. C 4:2:0 (Data Type 6)



1.2.13.6.1.7 YC 4:2:2 (Data Type 7)

The YC 4:2:2 data type is used for interleaved 4:2:2 data. It is expected to be packed with Y0 in the lowest byte followed by Cb followed by Y1 finally Cr in the upper most byte. The transfer counts each YC pair in a 16 bit word as a pixel but the number of pixels should be even. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 32 bit container as described in the TILER specification. The data block width and height should be set the same as the expected client.

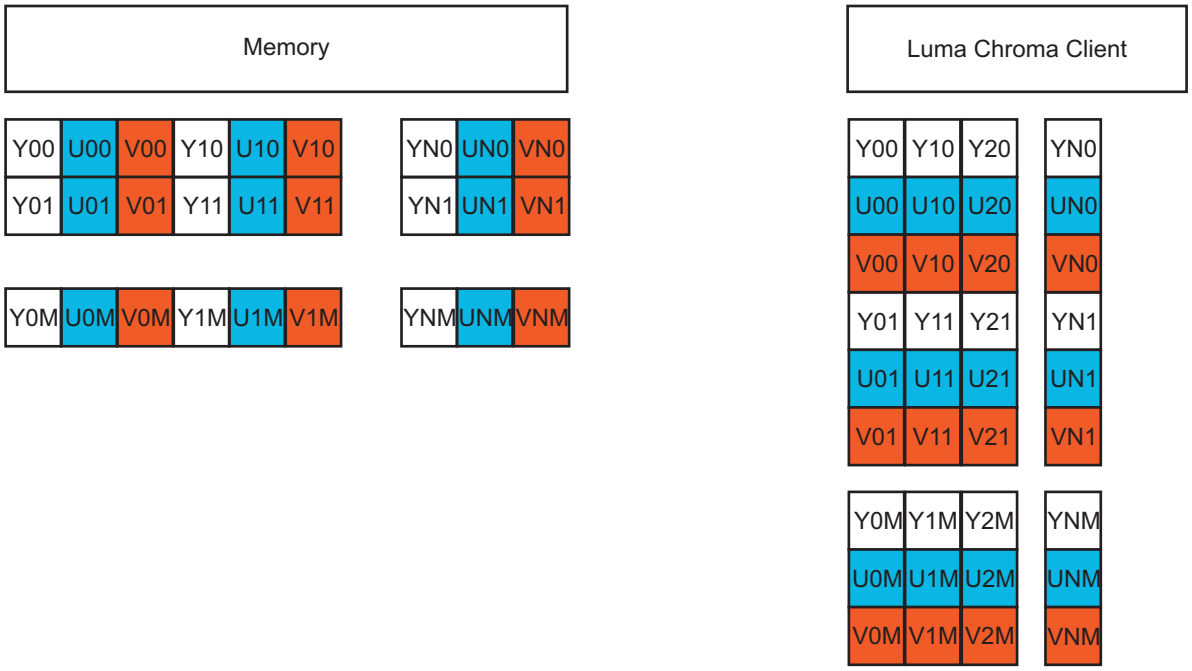
Figure 1-177. YC 4:2:2 (Data Type 7)



1.2.13.6.1.8 YC 4:4:4 (Data Type 8)

The YC 4:4:4 data type is used for interleaved 4:4:4 data. It is expected to be packed with Y0 in the lowest byte followed by Cr followed by Cb. The transfer counts each YCrCb triplet in a 24 bit word as a pixel. A 2D transfer of the data is NOT supported in the VPDMA. The data block width and height should be set to the number of pixels and lines that are expected by the client.

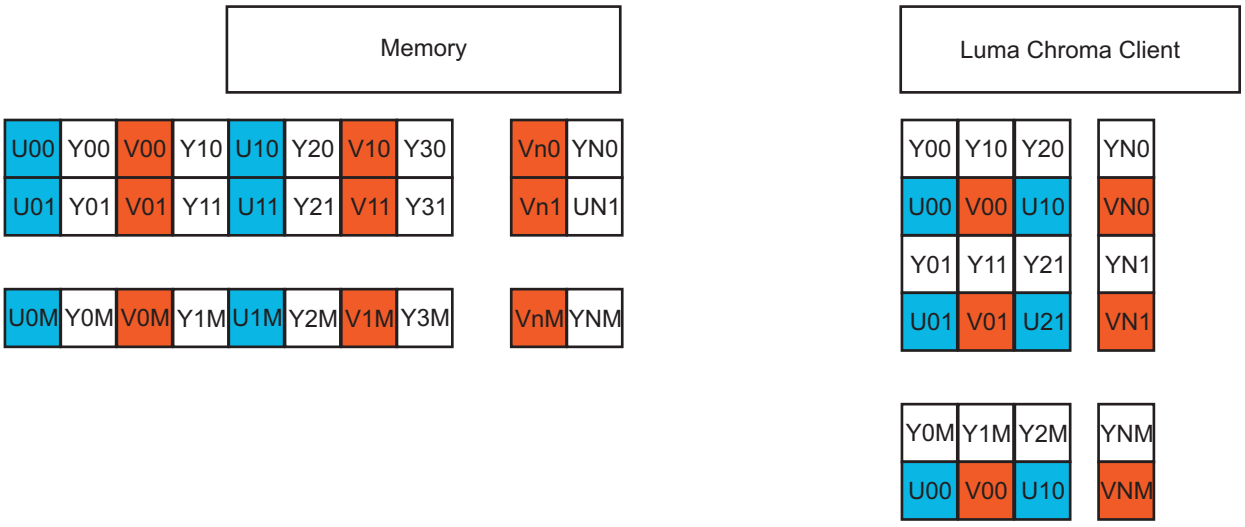
Figure 1-178. YC 4:4:4 (Data Type 8)



1.2.13.6.1.9 CY 4:2:2 (Data Type 23h)

The CY 4:2:2 data type is used for interleaved 4:2:2 data. It is expected to be packed with Cb in the lowest byte followed by Y0 followed by Cr finally Y1 in the upper most byte. The transfer counts each YC pair in a 16 bit word as a pixel but the number of pixels should be even. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 32 bit container as described in the TILER specification. The data block width and height should be set the same as the expected client.

Figure 1-179. CY 4:2:2 (Data Type 23h)



1.2.13.6.1.10 Cb 4:4:4 (Data Type 14h)

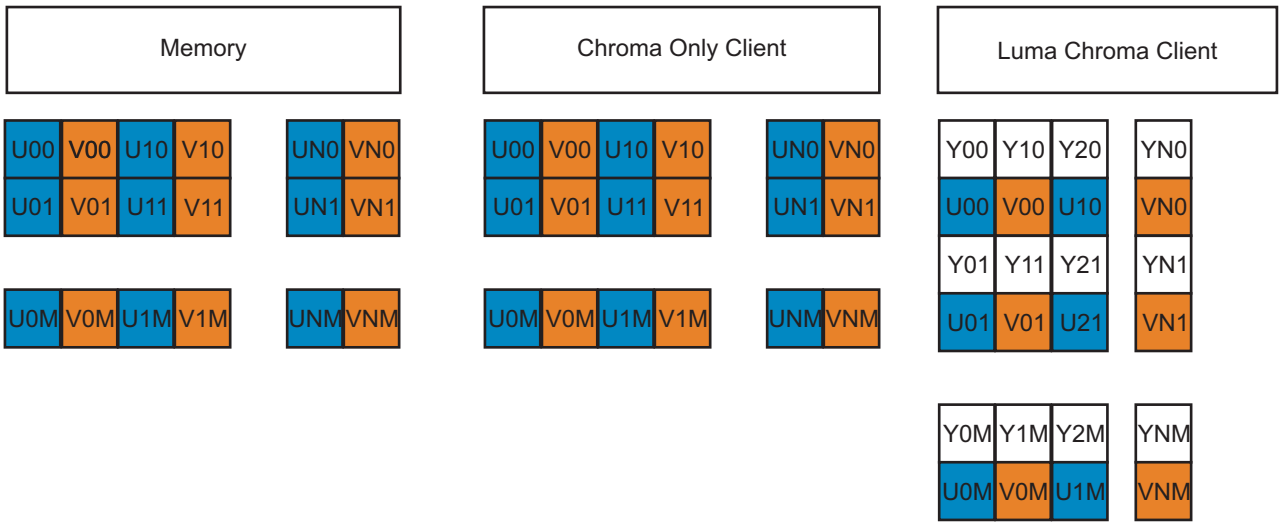
The Cb 4:4:4 data type is used for a co-planar 4:4:4 data. It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 16 bit container as described in the TILER specification. This data block should have the width and height of the expected client frame.

Figure 1-180. Cb 4:4:4 (Data Type 14h)

1.2.13.6.1.11 Cb 4:2:2 (Data Type 15h)

The C 4:2:2 data type is used for co-planar 4:2:2 data. It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 16 bit container as described in the TILER specification. This data block should have the width and the height of the expected client frame.

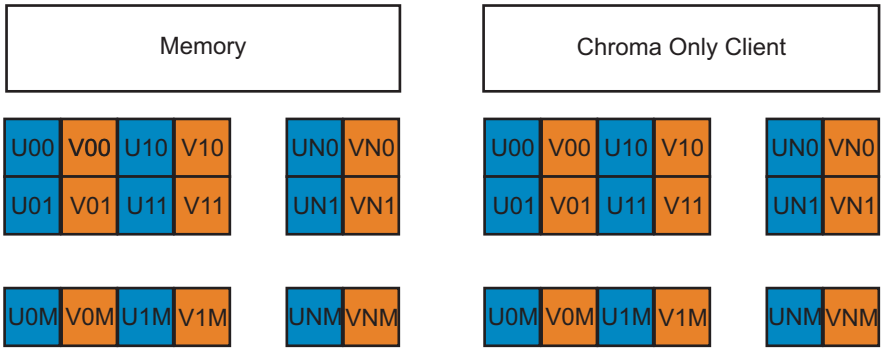
Figure 1-181. Cb 4:2:2 (Data Type 15h)



1.2.13.6.1.12 Cb 4:2:0 (Data Type 16h)

The Cb 4:2:0 data type is used for a co-planar 4:2:0 data. It is expected to be packed Cb in the lower byte and Cr in the upper byte in 16 bit words for each pixel. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in a 16 bit container as described in the TILER specification. This data block should have the width and half the height of the expected clients frame.

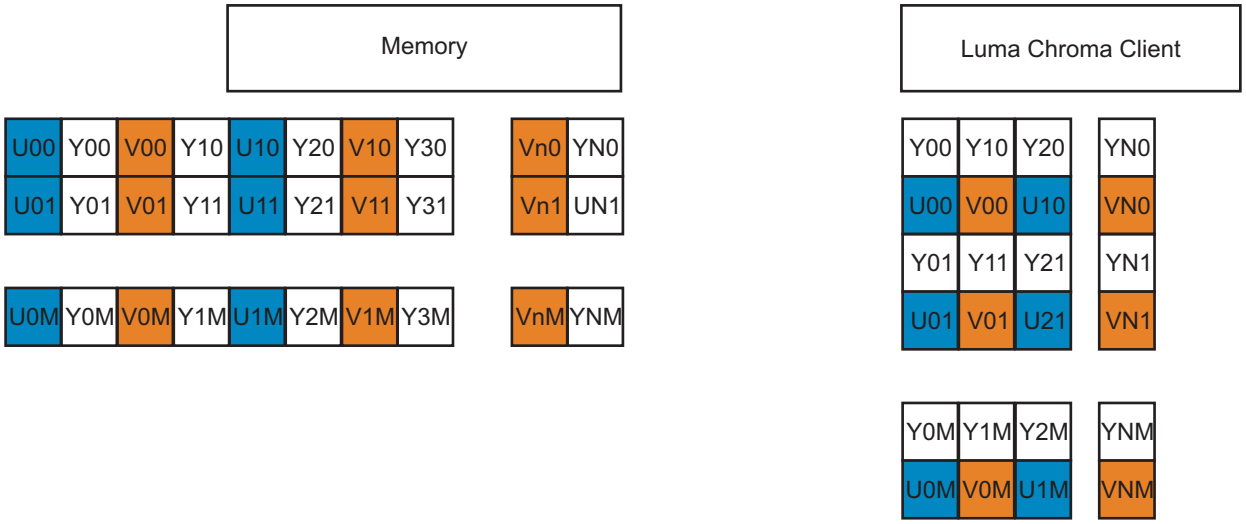
Figure 1-182. Cb 4:2:0 (Data Type 16h)



1.2.13.6.1.13 CbY 4:2:2 (Data Type 17h)

The CY 4:2:2 data type is used for interleaved 4:2:2 data. It is expected to be packed with Cb in the lowest byte followed by Y0 followed by Cr finally Y1 in the upper most byte. The transfer counts each YC pair in a 16 bit word as a pixel but the number of pixels should be even. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 32 bit container as described in the TILER specification. The data block width and height should be set the same as the expected client.

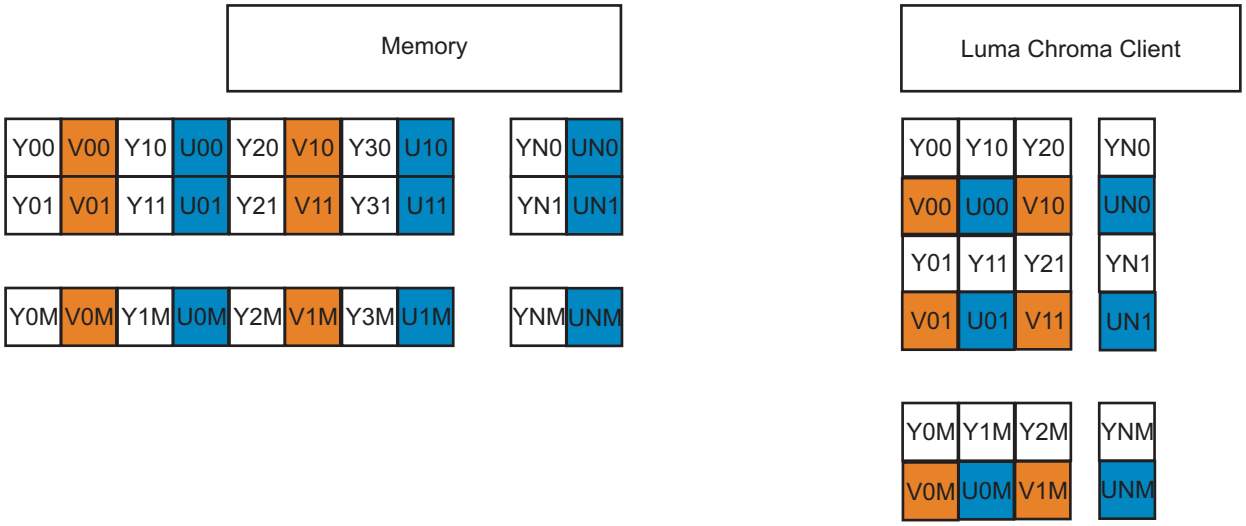
Figure 1-183. CbY 4:2:2 (Data Type 17h)



1.2.13.6.1.14 YC 4:2:2 (Data Type 27h)

The YC 4:2:2 data type is used for interleaved 4:2:2 data. It is expected to be packed with Y0 in the lowest byte followed by Cr followed by Y1 finally Cb in the upper most byte. The transfer counts each YC pair in a 16 bit word as a pixel but the number of pixels should be even. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 32 bit container as described in the TILER specification. The data block width and height should be set the same as the expected client.

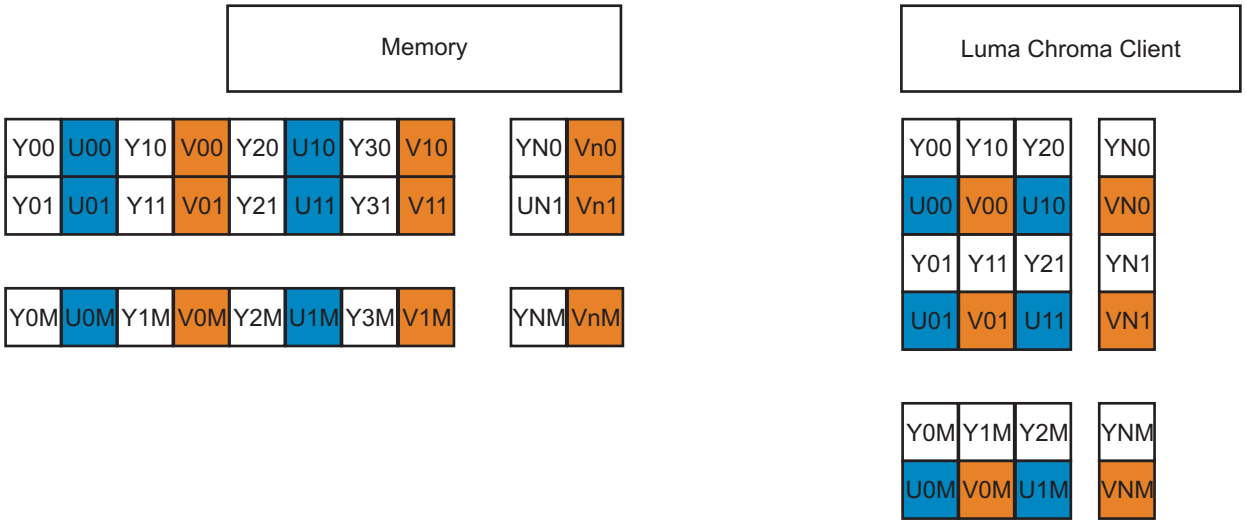
Figure 1-184. YC 4:2:2 (Data Type 27h)



1.2.13.6.1.15 YCb 4:2:2 (Data Type 37h)

The YCb 4:2:2 data type is used for interleaved 4:2:2 data. It is expected to be packed with Y0 in the lowest byte followed by Cb followed by Y1 finally Cr in the upper most byte. The transfer counts each YC pair in a 16 bit word as a pixel but the number of pixels should be even. If a 2D transfer of the data is used the VPDMA will assume this data type is stored in an 32 bit container as described in the TILER specification. The data block width and height should be set the same as the expected client.

Figure 1-185. YC 4:2:2 (Data Type 37h)



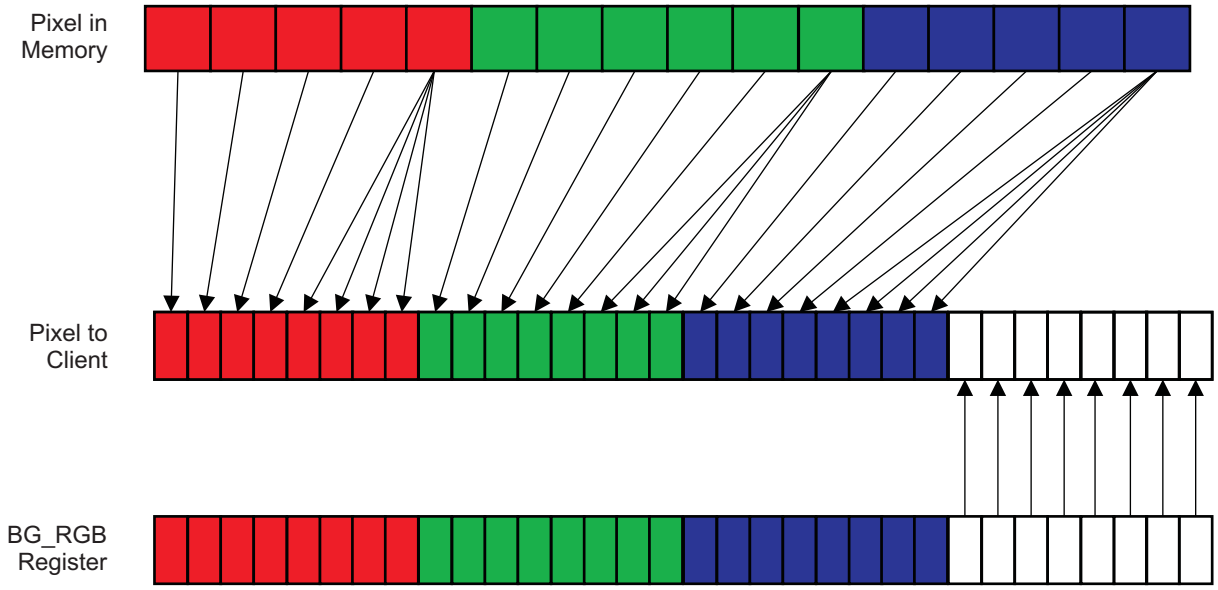
1.2.13.6.2 RGB Data Formats

The RGB channel type is used to provide data for a client that expects to transmit or receive RGB data. If a channel supports it also bit map data can be used where the pixel value of the data can be used as an address for a Color Look-up Table (CLUT) to provide a full 32 bit RGBA data stream to the client. In all modes the client is provided RGBA 8888 data. The lower bits if not provided by the data stream are a replication of the lower bit of the data. For outbound data the input is assumed to be RGB 888 and the Alpha value is taken from the Background Color register to make a full ARGB 8888. The lower bits are dropped from this data if a data type specifies less then the full 8 bits per color.

1.2.13.6.2.1 RGB16-565 (Data Type 0)

In RGB16-565 mode, each pixel is a single RGB pixel with 16 bits of data for each pixel. The 16 bits of data uses the lower 5 bits for blue data, the middle 6 bits for green data and the upper 5 bits for red data.

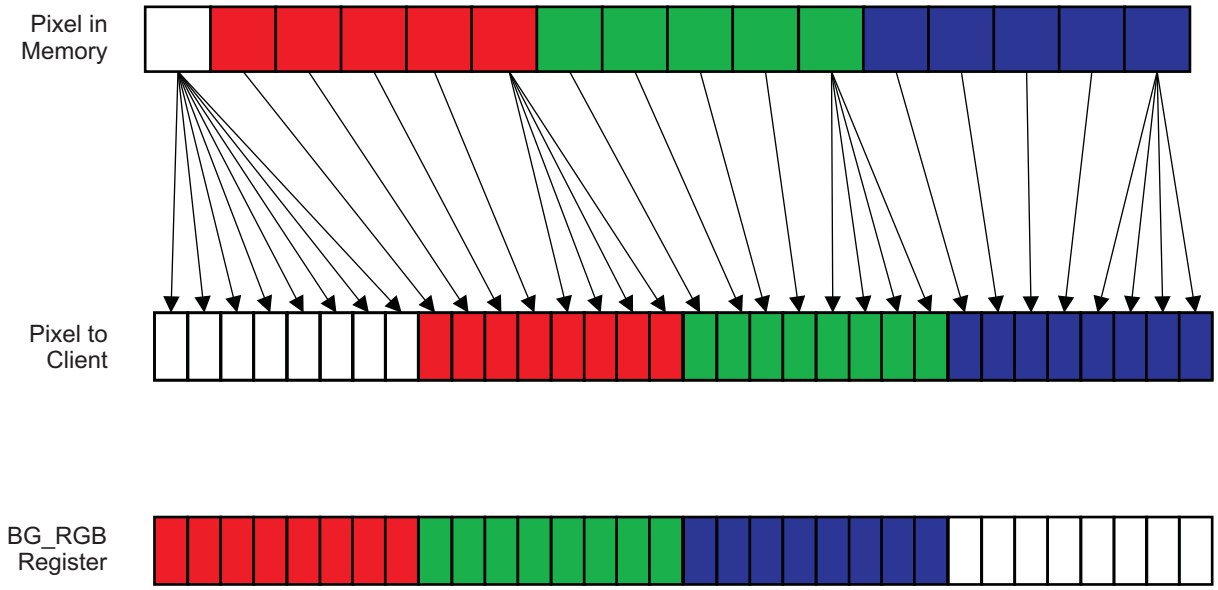
Figure 1-186. RGB16-565 (Data Type 0)



1.2.13.6.2.2 ARGB-1555 (Data Type 1)

In ARGB-1555 mode, each pixel is a single ARGB pixel with 16 bits of data for each pixel. The 16 bits of data uses the lower 5 bits for blue data, the next 5 bits for green data the next 5 bits for red data and the upper most bit for the blend value to use 0 or 0xff.

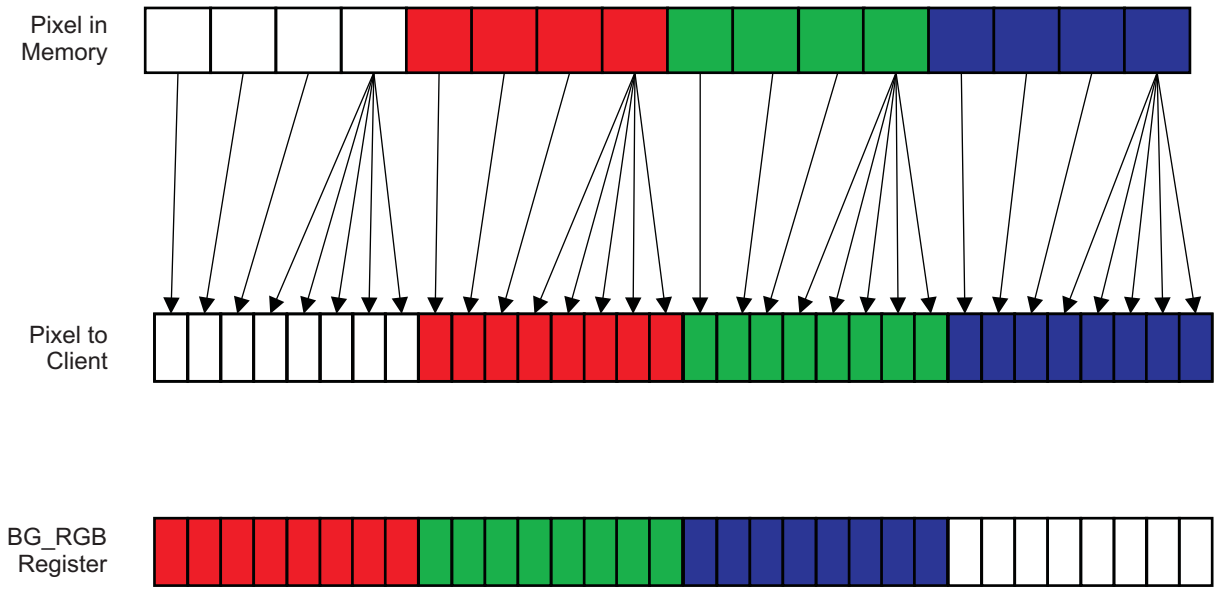
Figure 1-187. ARGB-1555 (Data Type 1)



1.2.13.6.2.3 ARGB-4444 (Data Type 2)

In ARGB16-4444 mode, each pixel is a single RGBA pixel with 16 bits of data for each pixel. The 16 bits of data uses the lowest 4 bits for blue data, the next 4 bits for green data the next 4 bits for red data and the upper most 4 bits for the blend value.

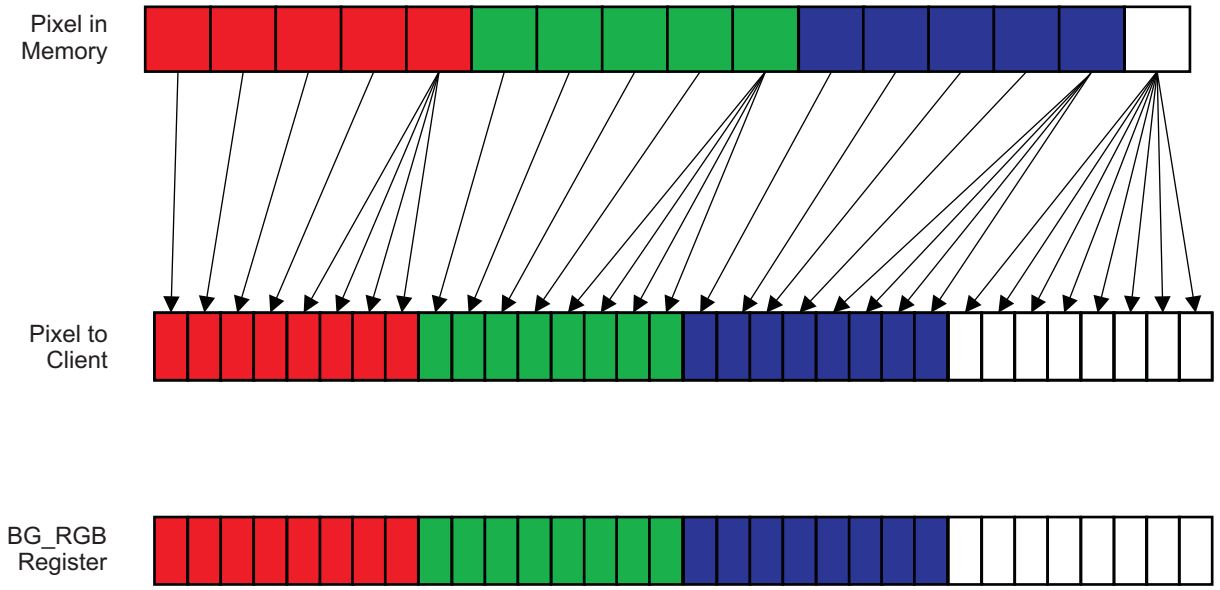
Figure 1-188. ARGB-4444 (Data Type 2)



1.2.13.6.2.4 RGBA-5551 (Data Type 3)

In RGBA-5551 mode, each pixel is a single ARGB pixel with 16 bits of data for each pixel. The 16 bits of data uses the lowest most bit for the blend value to use 0 or 0xff the next 5 bits for blue data, the next 5 bits for green data the next 5 bits for red data.

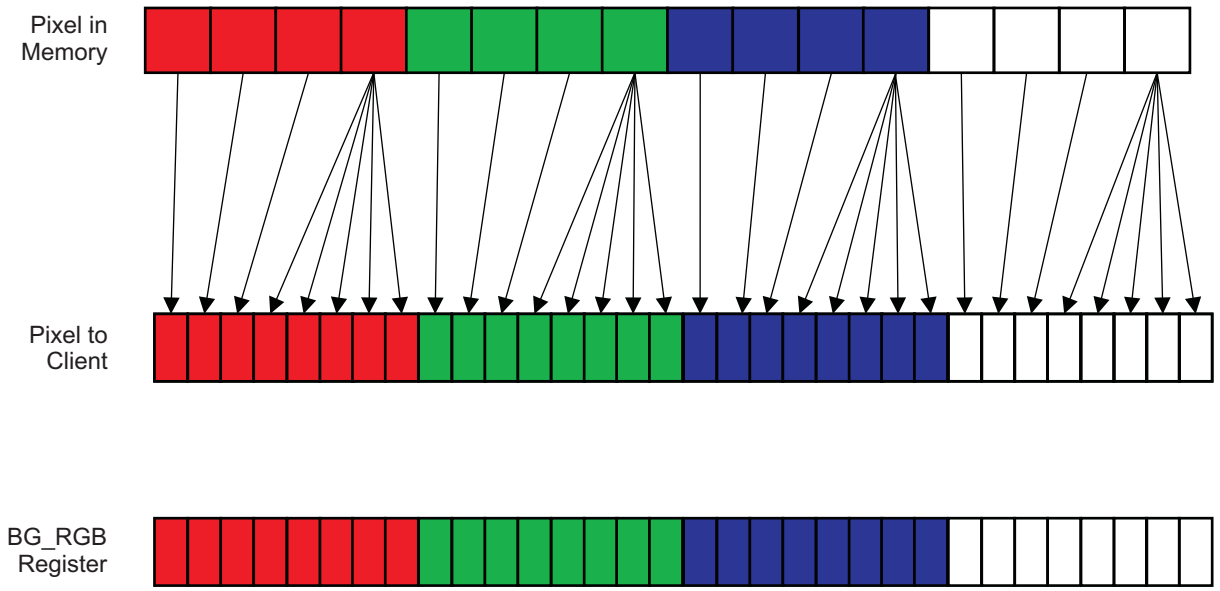
Figure 1-189. RGBA-5551 (Data Type 3)



1.2.13.6.2.5 RGBA-4444 (Data Type 4)

In RGBA-4444 mode, each pixel is a single RGBA pixel with 16 bits of data for each pixel. The 16 bits of data uses the lowest 4 bits for the blend value, the next 4 bits for blue data, the next 4 bits for green data and the upper most 4 bits for red data.

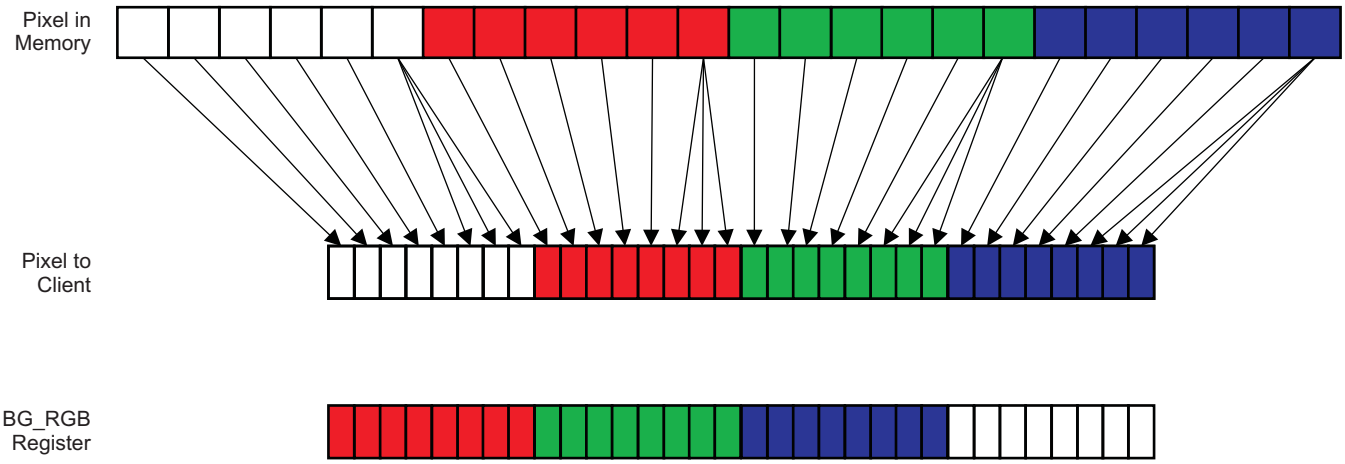
Figure 1-190. RGBA-4444 (Data Type 4)



1.2.13.6.2.6 ARGB24-6666 (Data Type 5)

In ARGB24-6666 mode, each pixel is a single ARGB pixel with 24 bits of data for each pixel. The 24 bits of data uses the lowest 6 bits for the blend value, the next 6 bits for blue data, the next 6 bits for green data and the upper most 6 bits for red data.

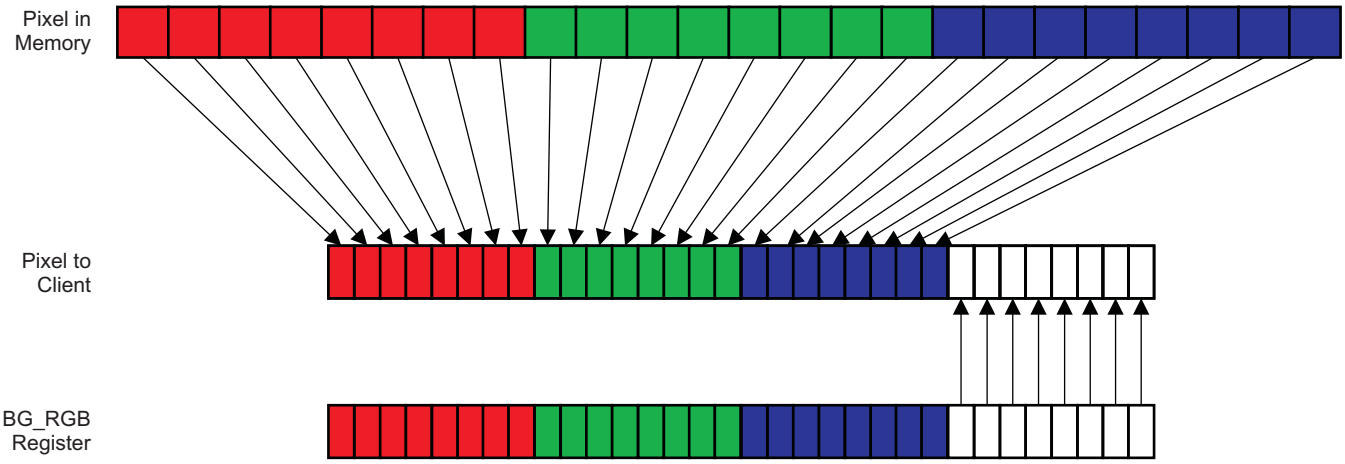
Figure 1-191. ARGB24-6666 (Data Type 5)



1.2.13.6.2.7 RGB24-888 (Data Type 6)

In RGB24-888 mode, each pixel is a single RGB pixel with 24 bits of data for each pixel. The 24 bits of data uses the lowest 8 bits for blue data, the next 8 bits for green data and the upper most 8 bits for red data it uses the BG_RGB Blend value for the Blend value.

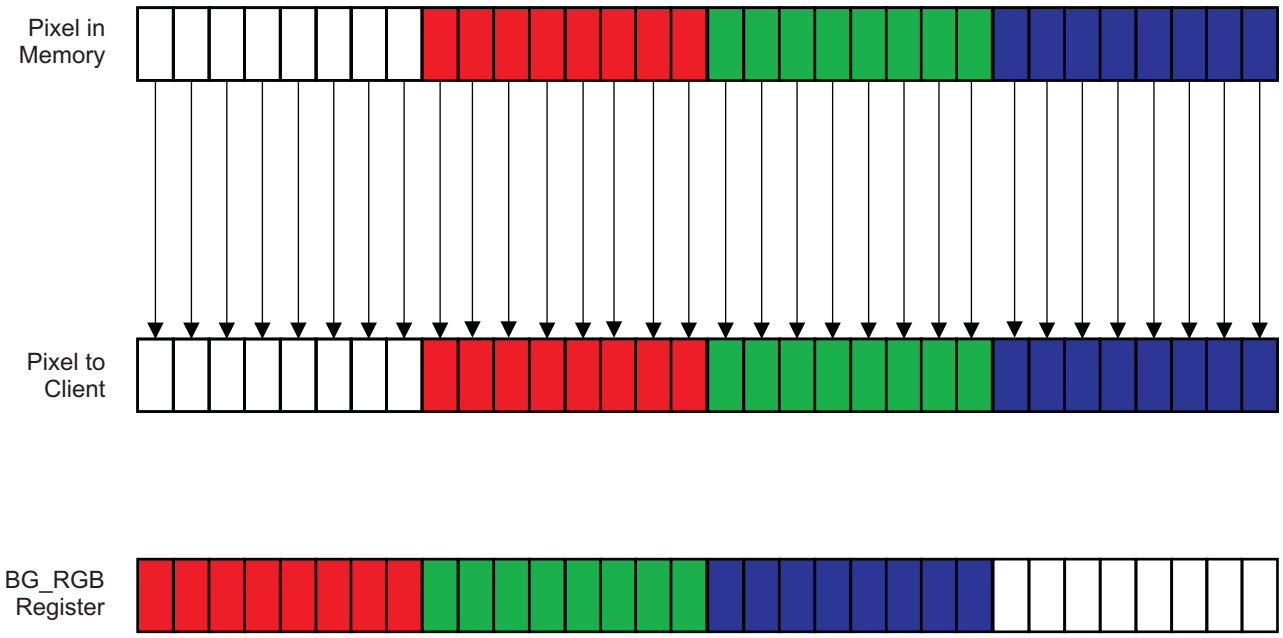
Figure 1-192. RGB24-888 (Data Type 6)



1.2.13.6.2.8 ARGB32-8888 (Data Type 7)

In ARGB32-8888 mode, each pixel is a single ARGB pixel with 32 bits of data for each pixel. The 32 bitsof data uses the lowest 8 bits for blue data, the next 8 bits for green data and the next 8 bits for red data it uses the upper most bits for the blend value.

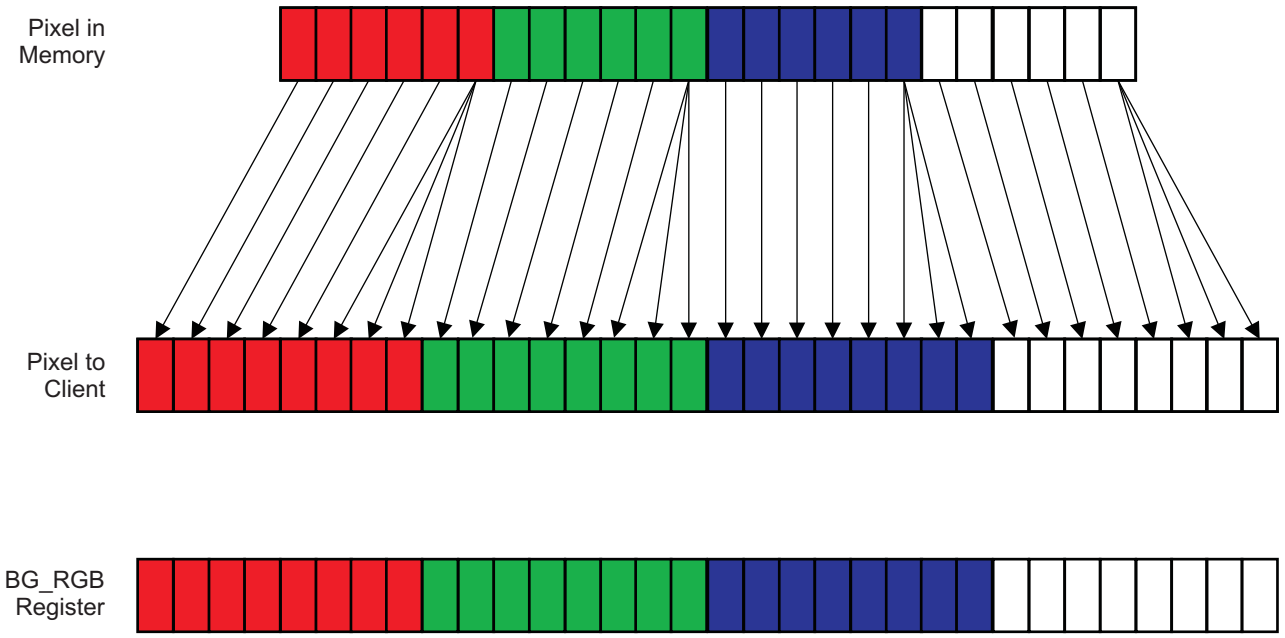
Figure 1-193. ARGB32-8888 (Data Type 7)



1.2.13.6.2.9 RGBA24-6666 (Data Type 8)

In RGBA24-6666 mode, each pixel is a single RGBA pixel with 24 bits of data for each pixel. The 24 bits of data uses the lowest 6 bits for the blend value, the next 6 bits for blue data, the next 6 bits for green data and the upper 6 bits for red data.

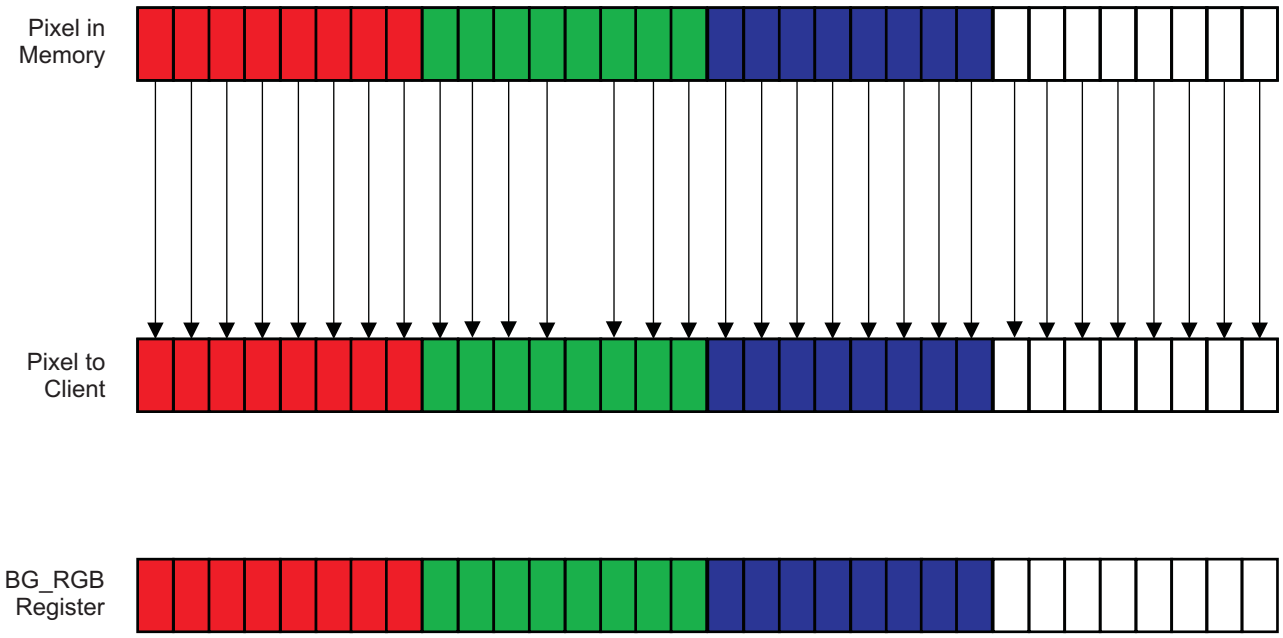
Figure 1-194. RGBA24-6666 (Data Type 8)



1.2.13.6.2.10 RGBA32-8888 (Data Type 9)

In RGBA32-8888 mode, each pixel is a single ARGB pixel with 32 bits of data for each pixel. The 32 bits of data uses the lowest 8 bits for the blend value the next 8 bits for blue data, the next 8 bits for green data and the upper most 8 bits for red data.

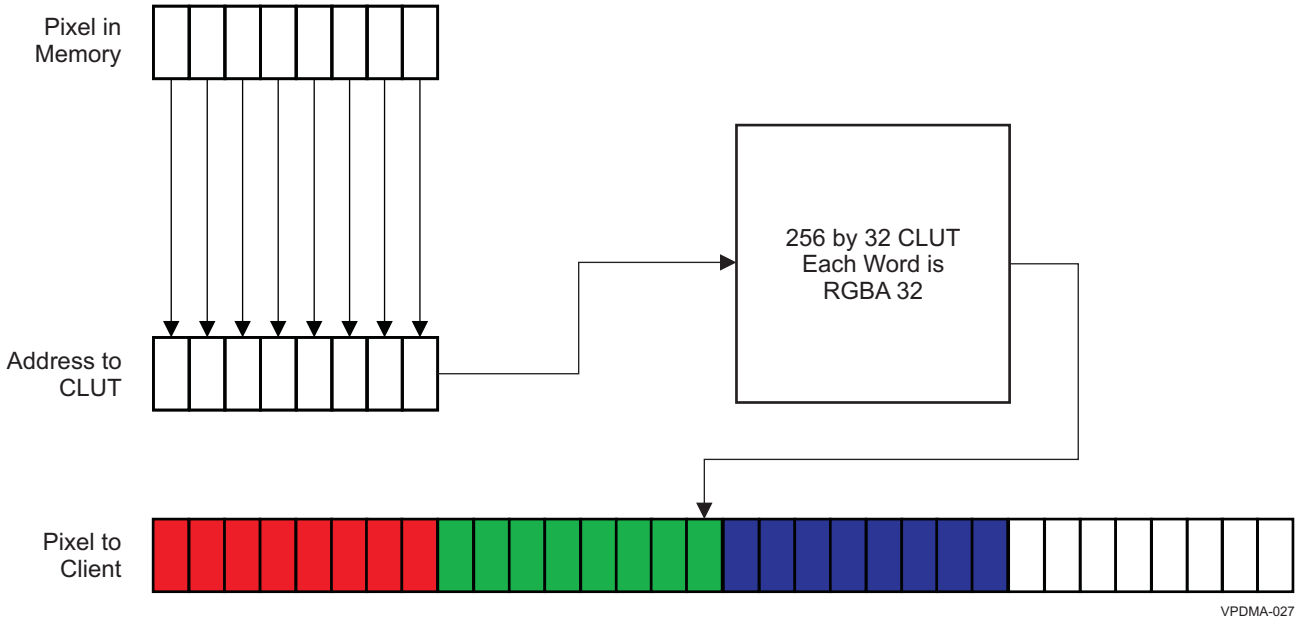
Figure 1-195. RGBA32-8888 (Data Type 9)



1.2.13.6.2.11 Bitmap-8 (Data Type 20h)

In Bitmap-8 data, each pixel is an 8 bit value that is used as an address into a 256 × 32 memory that gives the final RGBA32-8888 data value.

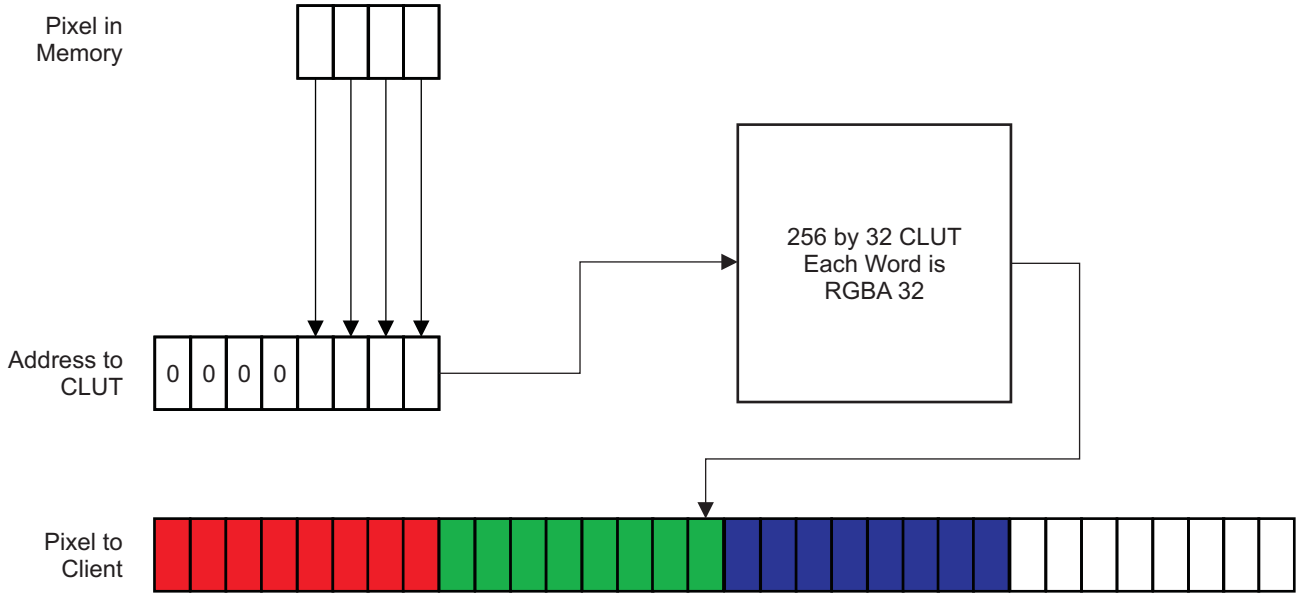
Figure 1-196. Bitmap-8 (Data Type 20h)



1.2.13.6.2.12 Bitmap-4 Lower (Data Type 22h)

In Bitmap-4 Lower data, each pixel is an 4 bit value that is used as the lower 4 bits of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 4 bits in this case are tied to 0.

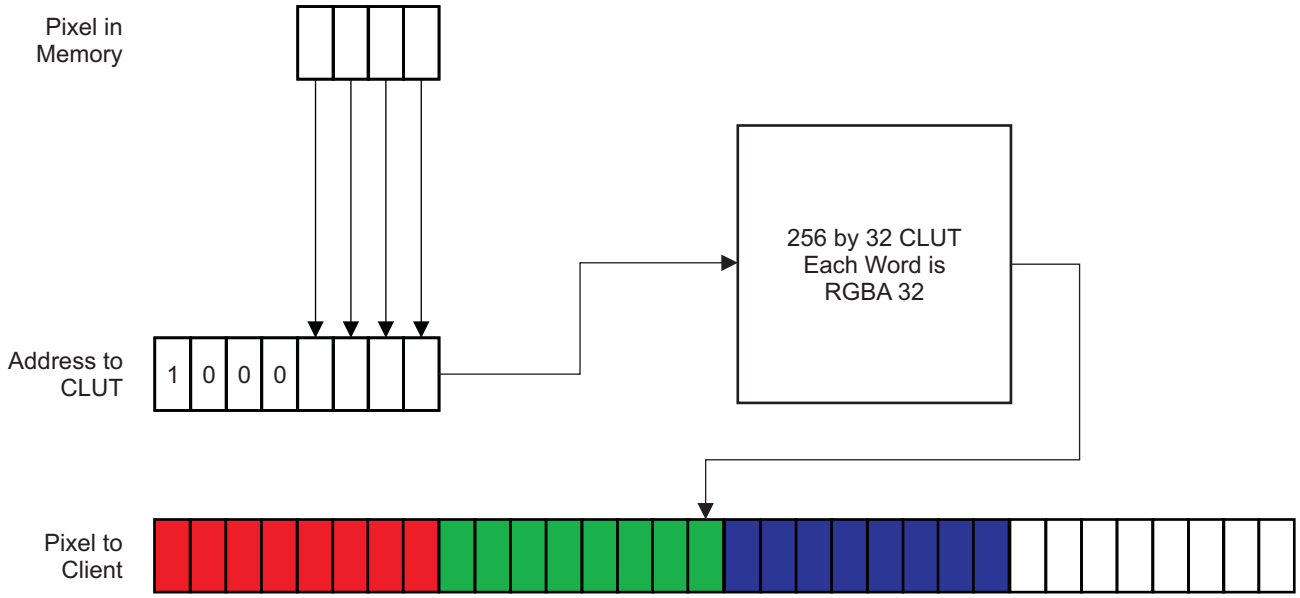
Figure 1-197. Bitmap-4 Lower (Data Type 22h)



1.2.13.6.2.13 Bitmap-4 Upper (Data Type 23h)

In Bitmap-4 Upper data, each pixel is an 4 bit value that is used as the lower 4 bits of address into a 256× 32 memory that gives the final RGBA32-8888 data value. The upper 4 bits in this case are tied to 4'b1000.

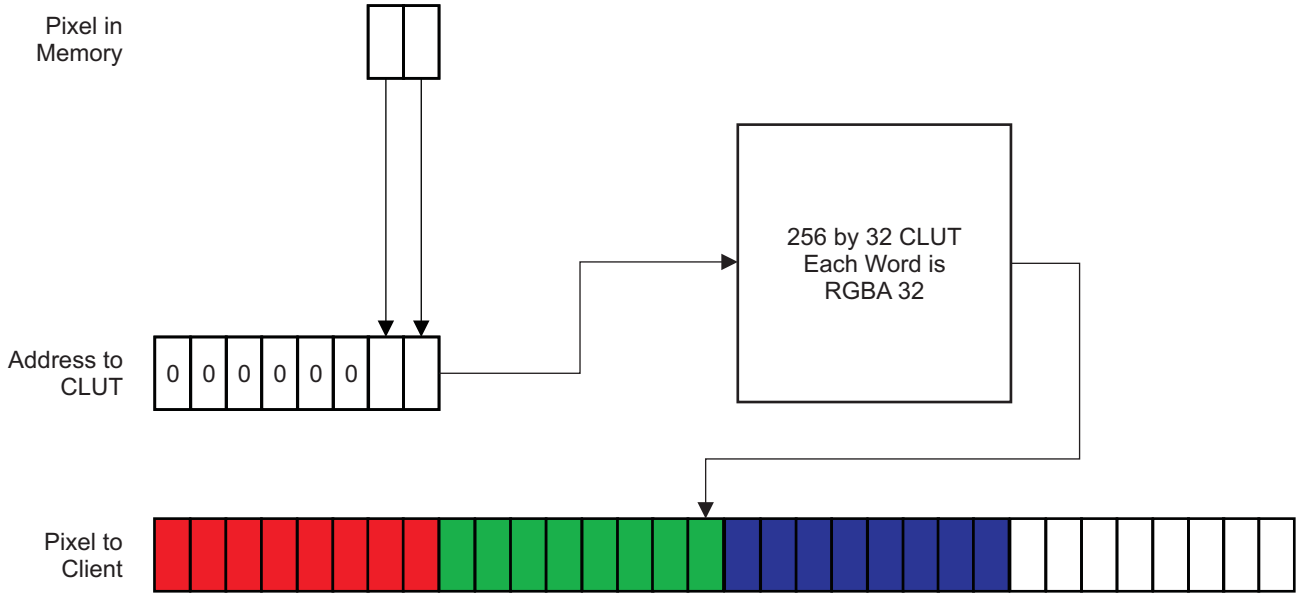
Figure 1-198. Bitmap-4 Upper (Data Type 23h)



1.2.13.6.2.14 Bitmap-2 Offset0 (Data Type 24h)

In Bitmap-2 Offset0 data, each pixel is a 2 bit value that is used as the lower 2 bits of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 2 bits in this case are tied to 0. Bits 2-5 are tied to 0.

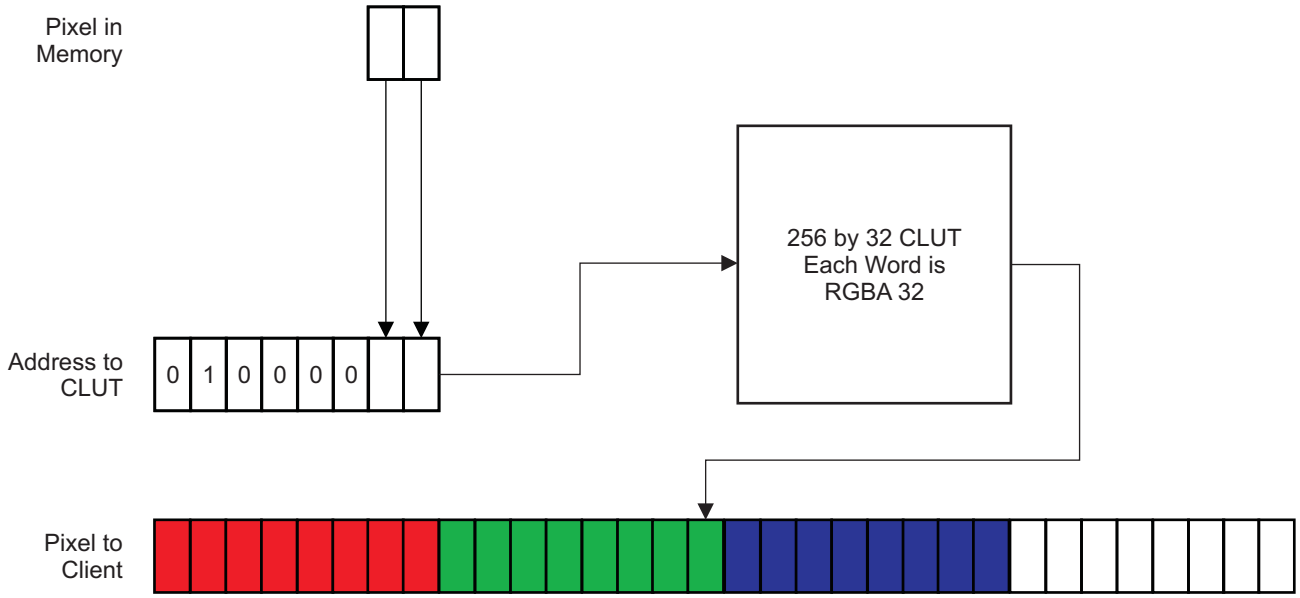
Figure 1-199. Bitmap-2 Offset0 (Data Type 24h)



1.2.13.6.2.15 Bitmap-2 Offset1 (Data Type 25h)

In Bitmap-2 Offset1 data, each pixel is a 2 bit value that is used as the lower 2 bits of address into a 256× 32 memory that gives the final RGBA32-8888 data value. The upper 2 bits in this case are tied to 2'b01. Bits 2-5 are tied to 0.

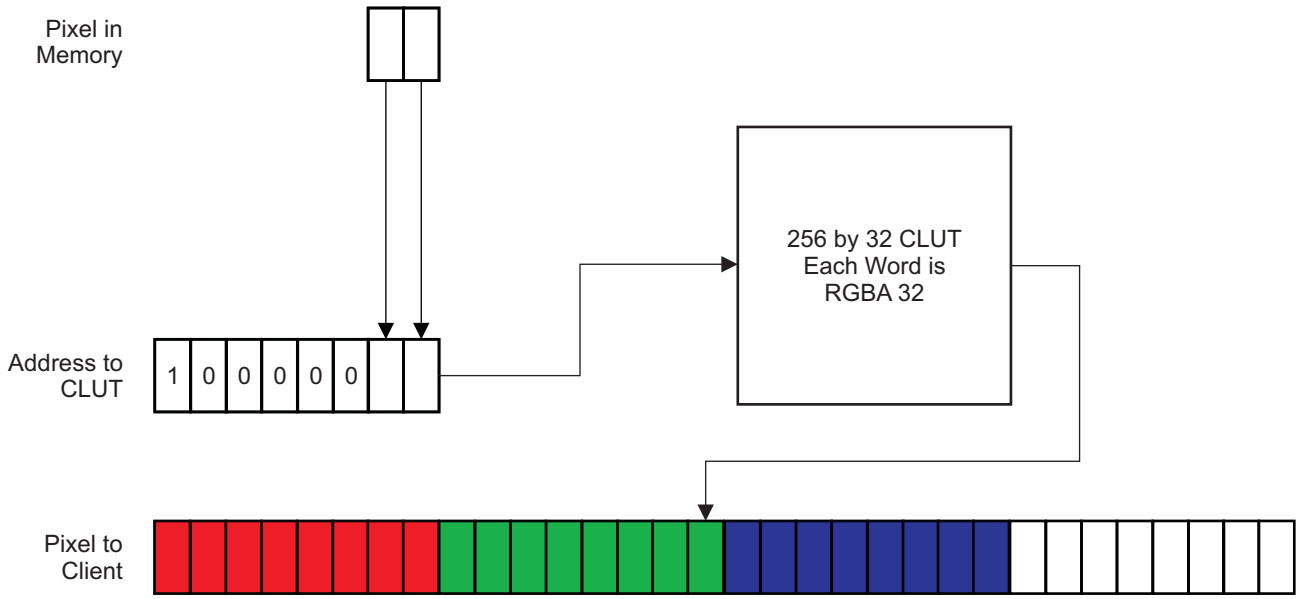
Figure 1-200. Bitmap-2 Offset1 (Data Type 25h)



1.2.13.6.2.16 Bitmap-2 Offset2 (Data Type 26h)

In Bitmap-2 Offset2 data, each pixel is a 2 bit value that is used as the lower 2 bits of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 2 bits in this case are tied to 2'10. Bits 2-5 are tied to 0.

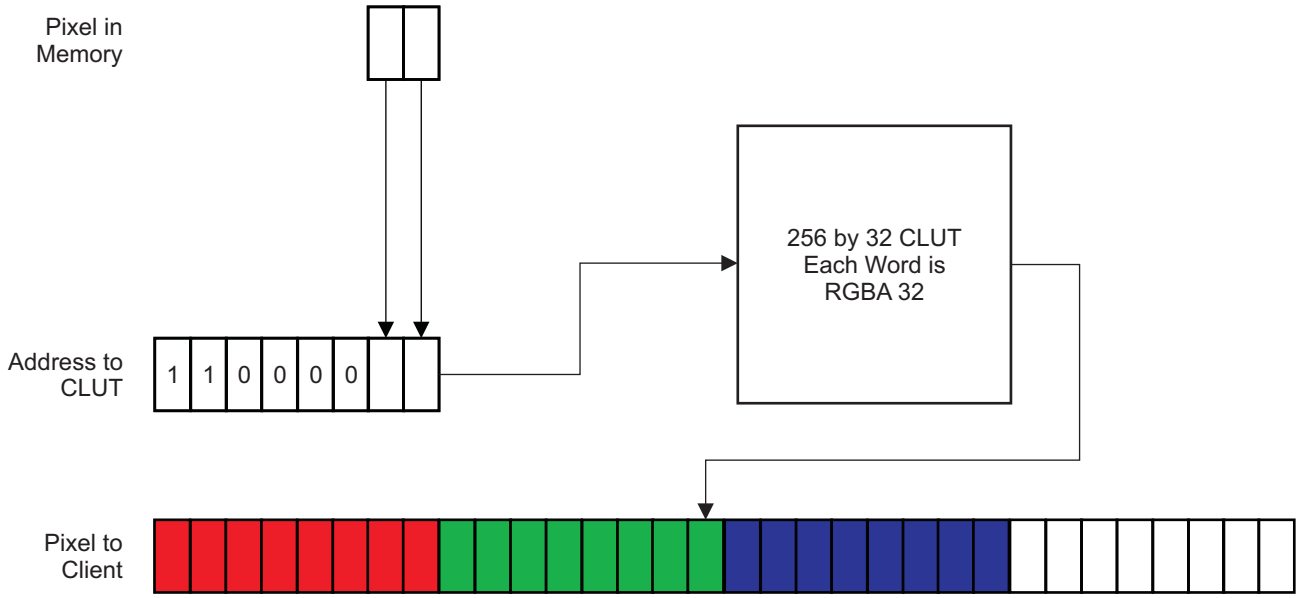
Figure 1-201. Bitmap-2 Offset2 (Data Type 26h)



1.2.13.6.2.17 Bitmap-2 Offset3 (Data Type 27h)

In Bitmap-2 Offset3 data, each pixel is a 2 bit value that is used as the lower 2 bits of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 2 bits in this case are tied to 2'b11. Bits 2-5 are tied to 0.

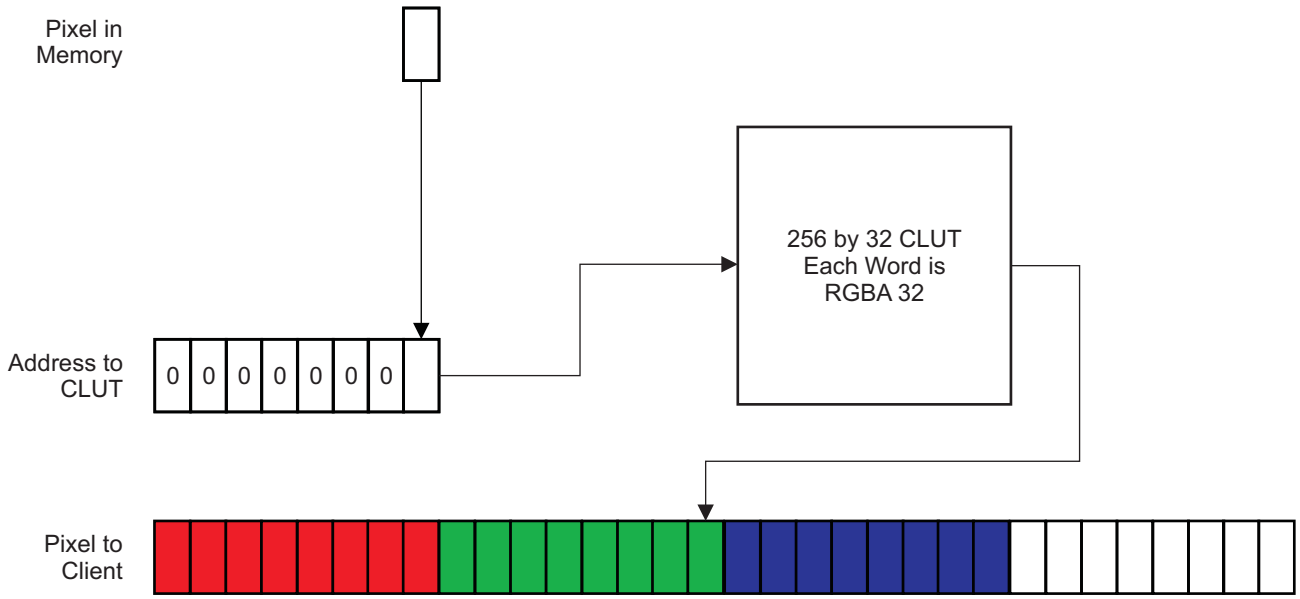
Figure 1-202. Bitmap-2 Offset3 (Data Type 27h)



1.2.13.6.2.18 Bitmap-1 Offset0 (Data Type 28h)

In Bitmap-1 Offset0 data, each pixel is an 1 bit value that is used as the lower bit of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 3 bits in this case are tied to 3'b000. Bits 1-4 are tied to 0.

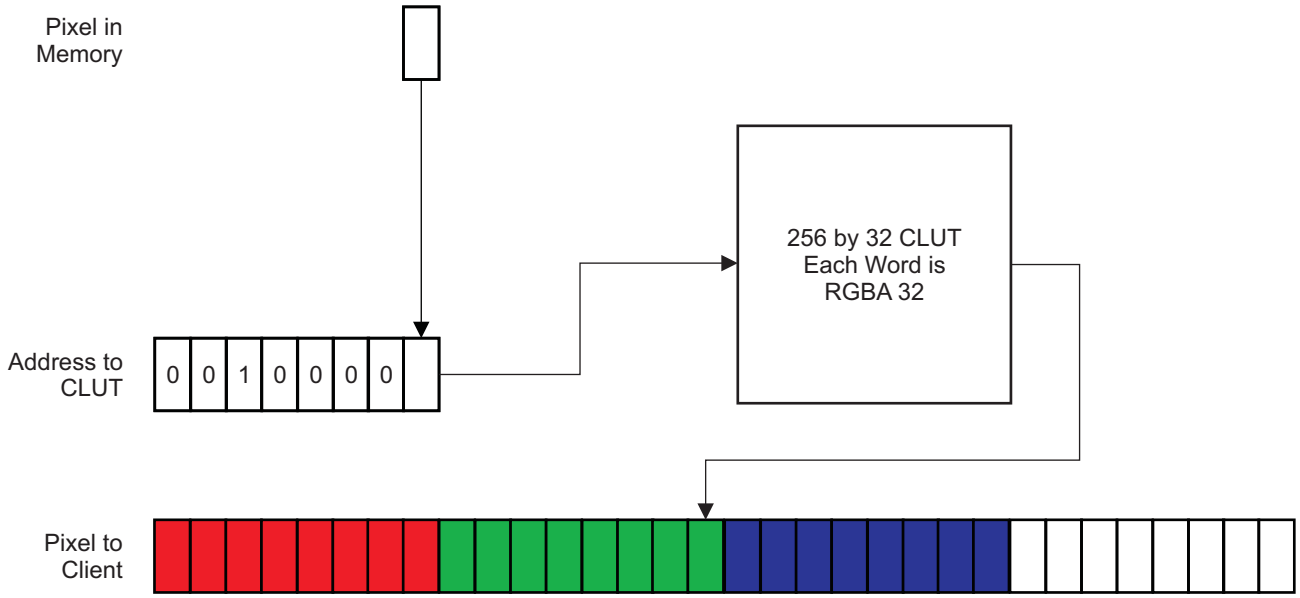
Figure 1-203. Bitmap-1 Offset0 (Data Type 28h)



1.2.13.6.2.19 Bitmap-1 Offset1 (Data Type 29h)

In Bitmap-1 Offset1 data, each pixel is an 1 bit value that is used as the lower bit of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 3 bits in this case are tied to 3'b001. Bits 1-4 are tied to 0.

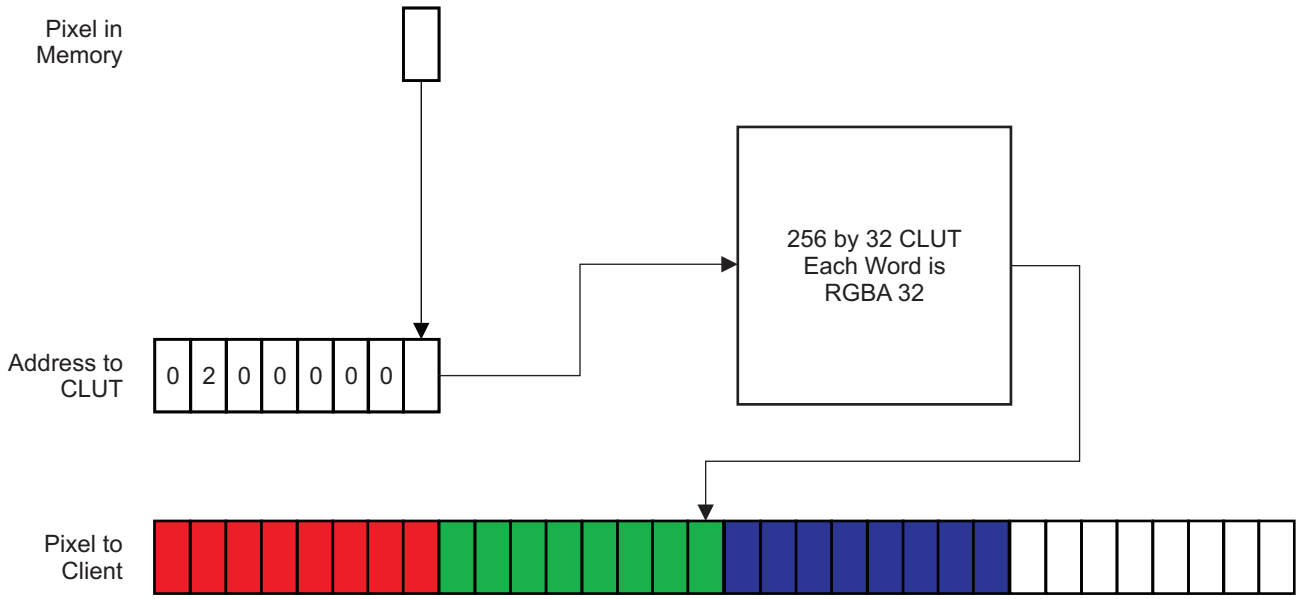
Figure 1-204. Bitmap-1 Offset1 (Data Type 29h)



1.2.13.6.2.20 Bitmap-1 Offset2 (Data Type 2Ah)

In Bitmap-1 Offset2 data, each pixel is an 1 bit value that is used as the lower bit of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 3 bits in this case are tied to 3'b010. Bits 1-4 are tied to 0.

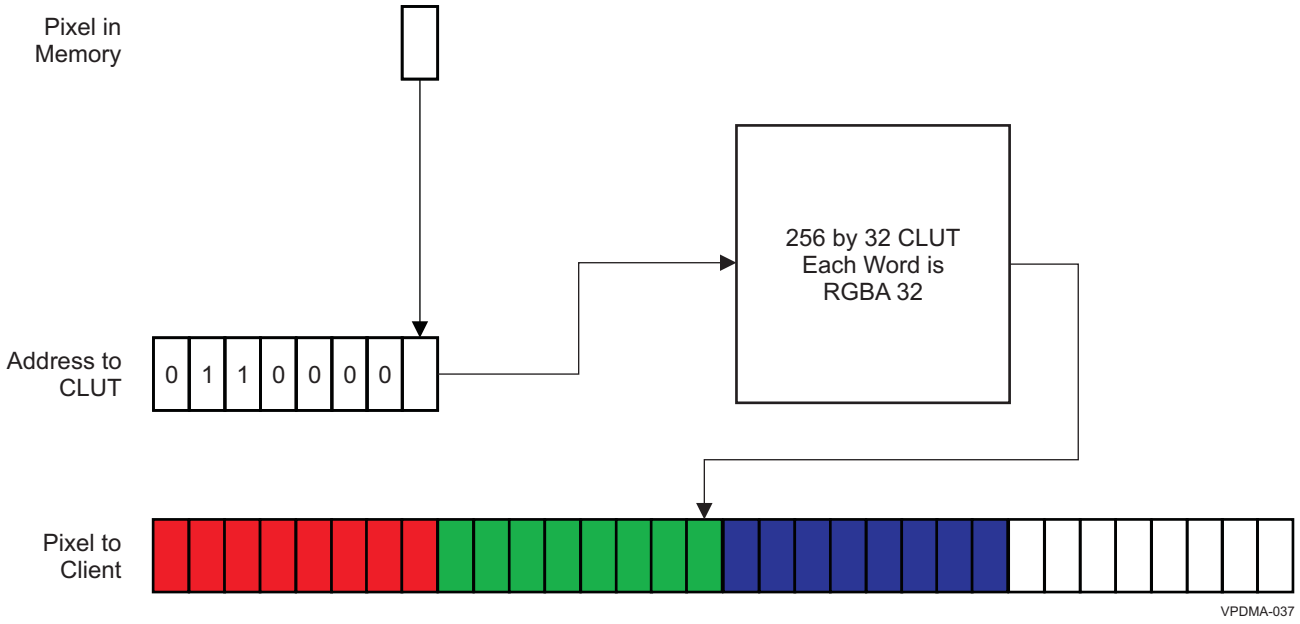
Figure 1-205. Bitmap-1 Offset2 (Data Type 2Ah)



1.2.13.6.2.21 Bitmap-1 Offset3 (Data Type 2Bh)

In Bitmap-1 Offset3 data, each pixel is an 1 bit value that is used as the lower bit of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 3 bits in this case are tied to 3'b000. Bits 1-4 are tied to 0.

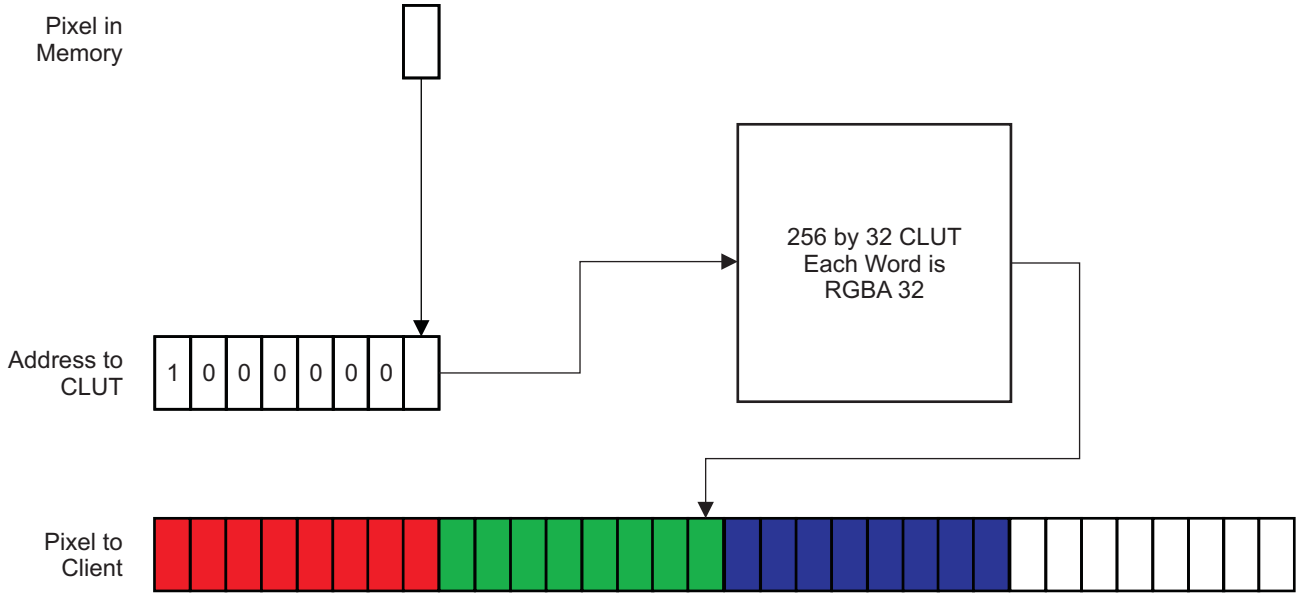
Figure 1-206. Bitmap-1 Offset3 (Data Type 2Bh)



1.2.13.6.2.22 Bitmap-1 Offset4 (Data Type 2Ch)

In Bitmap-1 Offset4 data, each pixel is an 1 bit value that is used as the lower bit of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 3 bits in this case are tied to 3'b000. Bits 1-4 are tied to 0.

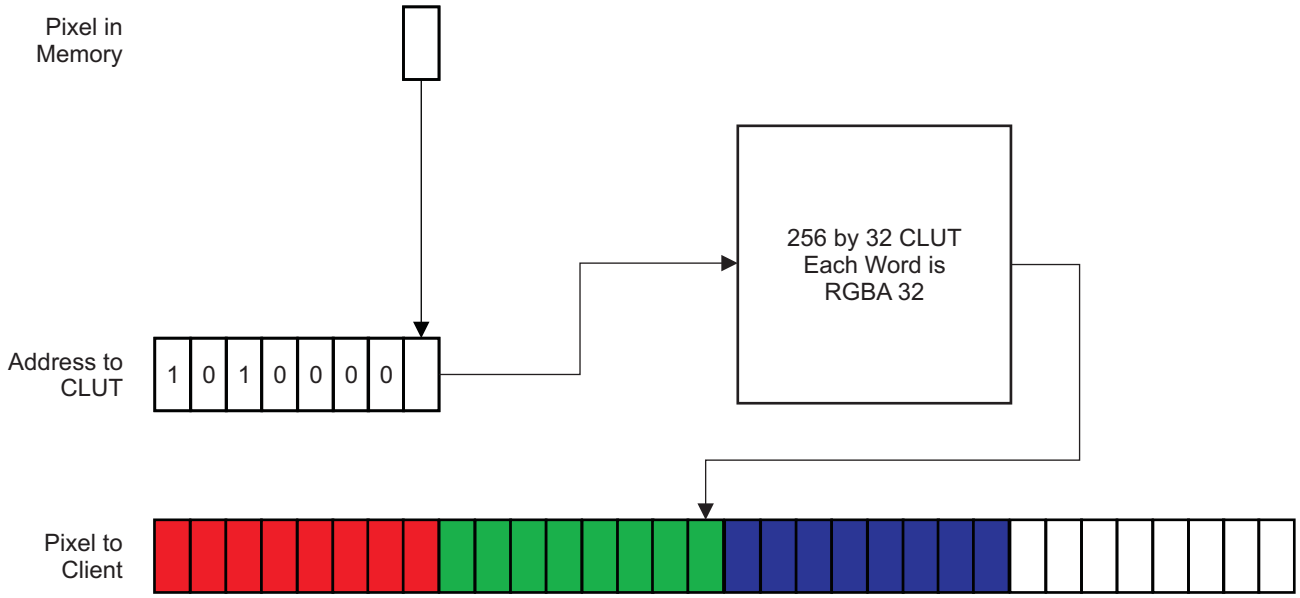
Figure 1-207. Bitmap-1 Offset4 (Data Type 2Ch)



1.2.13.6.2.23 Bitmap-1 Offset5 (Data Type 2Dh)

In Bitmap-1 Offset5 data, each pixel is an 1 bit value that is used as the lower bit of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 3 bits in this case are tied to 3'b101. Bits 1-4 are tied to 0.

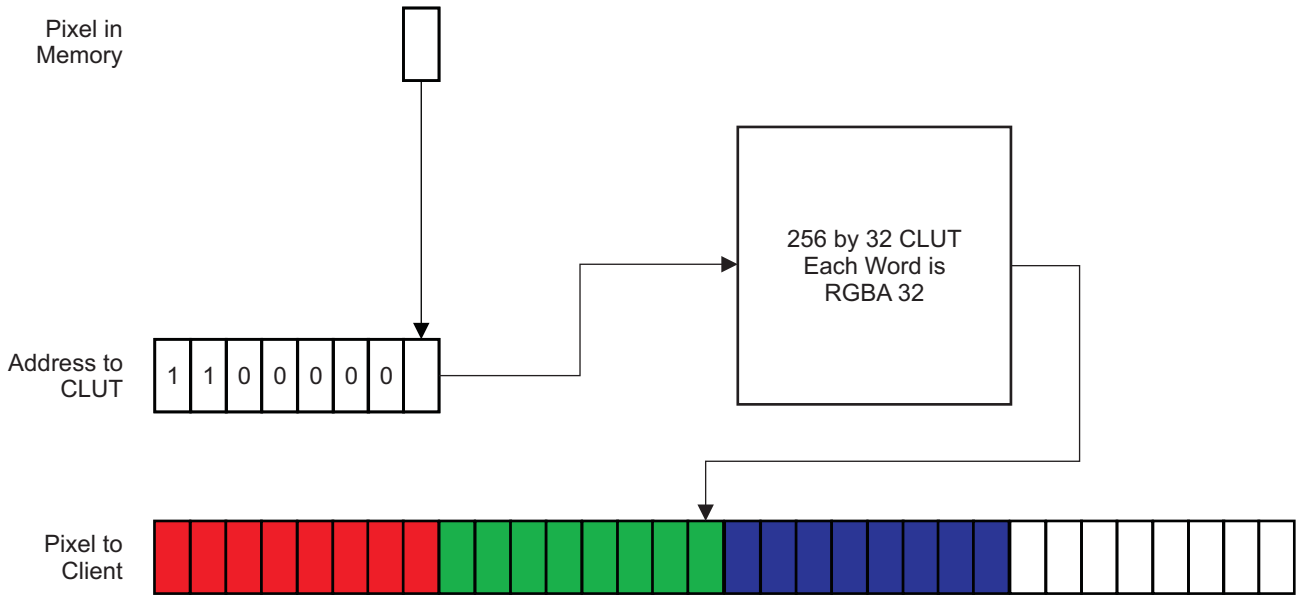
Figure 1-208. Bitmap-1 Offset5 (Data Type 2Dh)



1.2.13.6.2.24 Bitmap-1 Offset6 (Data Type 2Eh)

In Bitmap-1 Offset6 data, each pixel is an 1 bit value that is used as the lower bit of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 3 bits in this case are tied to 3'b110. Bits 1-4 are tied to 0.

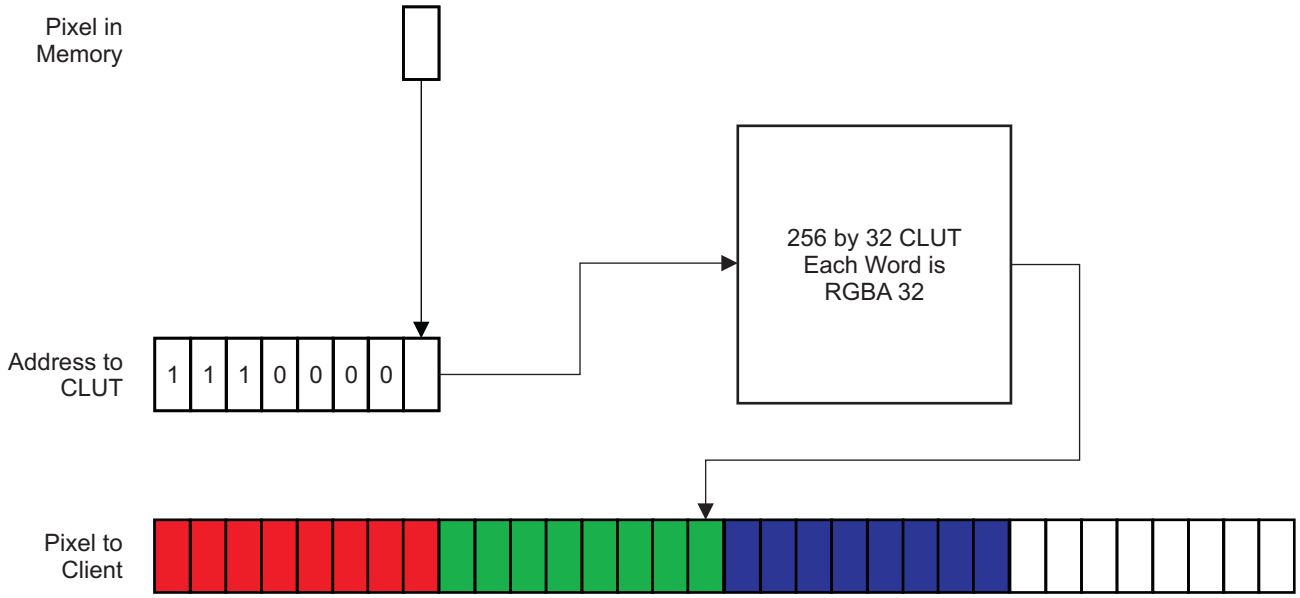
Figure 1-209. Bitmap-1 Offset6 (Data Type 2Eh)



1.2.13.6.2.25 Bitmap-1 Offset7 (Data Type 2Fh)

In Bitmap-1 Offset7 data, each pixel is an 1 bit value that is used as the lower bit of address into a 256 × 32 memory that gives the final RGBA32-8888 data value. The upper 3 bits in this case are tied to 3'b111. Bits 1-4 are tied to 0.

Figure 1-210. Bitmap-1 Offset7 (Data Type 2Fh)



1.2.13.6.3 Miscellaneous Data Type

The Miscellaneous channel type is for any data type that is not a normal video type. The Miscellaneous channel type makes no assumptions on data type and just passes the data to the client and supports a single buffer for the client. The size of the miscellaneous data type is always determined by the Data Type field of the descriptor which specifies the number of bits in the descriptor.

1.2.13.6.4 Free Channel Data Type

The Free channel data type is always ignored as it uses the same data type of the descriptor that first calls the free channel.

1.3 Registers

A register name is comprised of <MODULE_NAME>_<mmr_name> with the MODULE_NAME in upper-case and the mmr_name in that module in lower-case. For example, register name CSC_csc02: where CSC represents the module name (for which registers are specified with offsets in this section) and csc02 represents the MMR name in the module MMR list.

Each module may have multiple instances of it in the subsystem (see Table 1-114). For example, the CSC module has 6 instances with different names: CSC_HD0, CSC_HD1, CSC_SD, CSC_WB2, CSC_VIP0, and CSC_VIP1. See Figure 1-1 for the module instance names and its location in the subsystem. All the instances of a module share the same set of registers mentioned in this section.

Table 1-115 lists the memory map for the HDVPSS registers.

To calculate actual/final address of a specific MMR or register, use this example: register CSC_csc02, for the instance CSC_HD1.

Determine the address of CSC_csc02:	0x4810 0000	(Base Address of HDVPSS)
	+ 0x0000 0C00	(Instance Offset Address: CSC_HD1 from Table 1-115)
	+ 0x0000 0008	(Register Offset Address: CSC_csc02 from , corresponding instance register in this section or search for the register name in this section)
	= 0x4810 0C08	(Actual address of CSC_csc02)

Table 1-114. HDVPSS Module Instances

Module Name	Number of Instances	Instance Names
CHR_US	6	CHR_US_P0, CHR_US_P1, CHR_US_P2, CSC_US_AUX, CHR_US_SEC0, CHR_US_SEC1
CSC	6	CSC_HD0, CSC_HD1, CSC_SD, CSC_WB2, CSC_VIP0, CSC_VIP1
COMP	1	COMP
CIG	1	CIG
GRPX(1)	3	GRPX0, GRPX1, GRPX2
SD_VENC	1	SD_VENC
HD_VENC	3	HDMI/DVO1, DVO2, HDCOMP
VIP_PARSER	2	VIP0_PARSER, VIP1_PARSER
DEI	1	DEI
NF	1	NF
SC	5	SC_1, SC_2, SC_3, SC_4, SC_5
VCOMP	1	VCOMP
VPDMA(2)	1	VPDMA
CHR_DS(3)	5	CHR_DS0_VIP0, CHR_DS1_VIP0, CHR_DS0_VIP1, CHR_DS1_VIP1, CHR_DS_NF

(1) GRPX module does not contain any 32-bit MMRs. The GRPX module is controlled by configuring the attributes mentioned in Section 1.2.5.

(2) CPU and VPDMA (through configuration descriptor) can access all the registers mentioned in this section. The VPDMA can also access GRPX attribute configuration and coefficients of all the scaler instances; however, the CPU can not.

(3) CHR_DS module does not contain any MMRs. The CHR_DS module is enabled by selecting 420 data formatted output in the clkc_vip registers.

NOTE: The block diagram and text sections of this chapter consistently use the instance numbering for the VIP and GRPX submodules as VIP0/VIP1 and GRPX0/GRPX1/GRPX2. However, the register sections use the numbering VIP1/VIP2 and GRPX1/GRPX2/GRPX3. The following list is the convention for submodule naming to register control:

- Submodule VIP0 is controlled by registers VIP1
- Submodule VIP1 is controlled by registers VIP2
- Submodule GRPX0 is controlled by registers GRPX1
- Submodule GRPX1 is controlled by registers GRPX2
- Submodule GRPX2 is controlled by registers GRPX3

Table 1-115. HDVPSS Registers

HDVPSS Submodule	Submodule Base Address
INTC	0000h
CLKC	0100h
CHR_US_P0	0300h
CHR_US_P1	0400h
CHR_US_P2	0500h
DEI	0600h
SC_1	0700h
CHR_US_AUX	0A00h
SC_2	0B00h
CSC_HD1	0C00h
CSC_SD	0D00h
VCOMP	0E00h
CSC_HD0	0F00h
SC_5	5000h
CIG	5100h
COMP	5200h
CSC_WB2	5300h
CHR_US_SEC0	5400h
CHR_US_SEC1	5480h
VIP_PARSER0	5500h
CSC_VIP0	5700h
SC_3	5800h
VIP_PARSER1	5A00h
CSC_VIP1	5C00h
SC_4	5D00h
SD_VENC	5E00h
HD_VENC_D_DVO1	6000h
HD_VENC_A_HDCOMP	8000h
HD_VENC_D_DVO2	A000h
NF	C200h
VPDMA	D000h

1.3.1 CHR_US Registers

Table 1-116 lists the memory-mapped registers for the CHR_US. All register offset addresses not listed in Table 1-116 should be considered as reserved locations and the register contents should not be modified.

Table 1-116. CHR_US REGISTERS

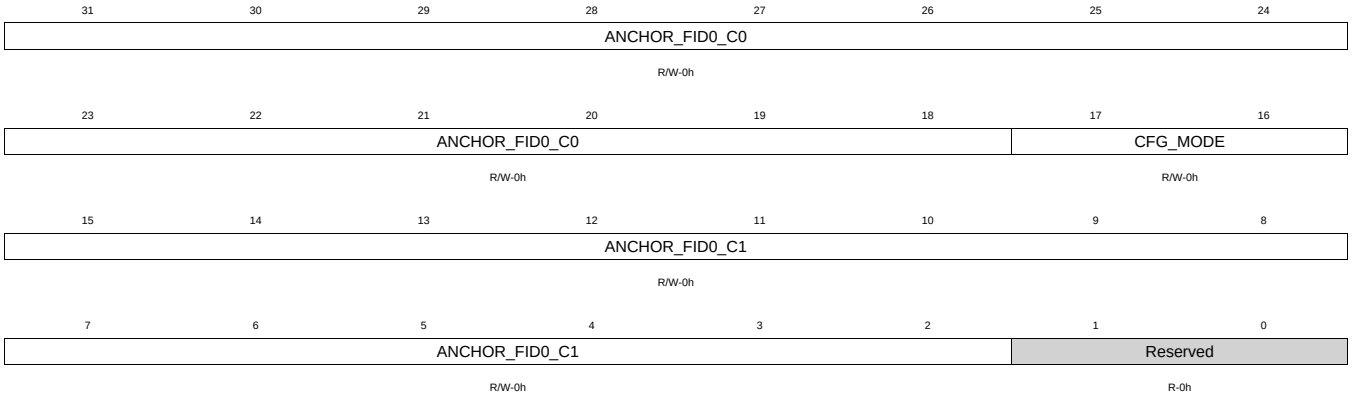
Offset	Acronym	Register Name	Section
4h	CHR_US_reg0	Upsampling Coeffs	Section 1.3.1.1
8h	CHR_US_reg1	Upsampling Coeffs	Section 1.3.1.2
Ch	CHR_US_reg2	Upsampling Coeffs	Section 1.3.1.3
10h	CHR_US_reg3	Upsampling Coeffs	Section 1.3.1.4
14h	CHR_US_reg4	Upsampling Coeffs	Section 1.3.1.5
18h	CHR_US_reg5	Upsampling Coeffs	Section 1.3.1.6
1Ch	CHR_US_reg6	Upsampling Coeffs	Section 1.3.1.7
20h	CHR_US_reg7	Upsampling Coeffs	Section 1.3.1.8

1.3.1.1 CHR_US_reg0 Register (offset = 4h) [reset = 0h]

CHR_US_reg0 is shown in Figure 1-211 and described in Table 1-117.

Upsampling Coeffs

Figure 1-211. CHR_US_reg0 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-117. CHR_US_reg0 Register Field Descriptions

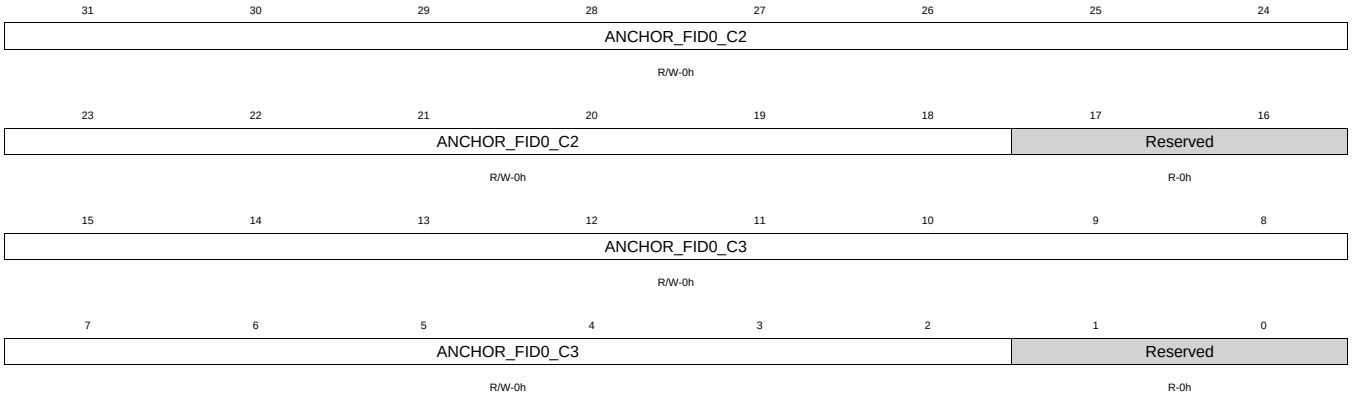
Bit	Field	Type	Reset	Description
31-18	ANCHOR_FID0_C0	R/W	0h	C0 coefficient for Anchor Pixel. Used when field_id = 0
17-16	CFG_MODE	R/W	0h	00 = Mode A 01 = Mode B
15-2	ANCHOR_FID0_C1	R/W	0h	C1 coefficient for Anchor Pixel. Used when field_id = 0
1-0	Reserved	R	0h	Reserved

1.3.1.2 CHR_US_reg1 Register (offset = 8h) [reset = 0h]

CHR_US_reg1 is shown in Figure 1-212 and described in Table 1-118.

Upsampling Coeffs

Figure 1-212. CHR_US_reg1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-118. CHR_US_reg1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	ANCHOR_FID0_C2	R/W	0h	C2 coefficient for Anchor Pixel. Used when field_id = 0
17-16	Reserved	R	0h	Reserved
15-2	ANCHOR_FID0_C3	R/W	0h	C3 coefficient for Anchor Pixel. Used when field_id = 0
1-0	Reserved	R	0h	Reserved

1.3.1.3 CHR_US_reg2 Register (offset = Ch) [reset = 0h]

CHR_US_reg2 is shown in Figure 1-213 and described in Table 1-119.

Upsampling Coeffs

Figure 1-213. CHR_US_reg2 Register

31	30	29	28	27	26	25	24
INTERP_FID0_C0							
R/W-0h							

23	22	21	20	19	18	17	16
INTERP_FID0_C0						Reserved	
R/W-0h						R-0h	

15	14	13	12	11	10	9	8
INTERP_FID0_C1							
R/W-0h							

7	6	5	4	3	2	1	0
INTERP_FID0_C1						Reserved	
R/W-0h						R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-119. CHR_US_reg2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	INTERP_FID0_C0	R/W	0h	C0 coefficient for Interpolated Pixel. Used when field_id = 0
17-16	Reserved	R	0h	Reserved
15-2	INTERP_FID0_C1	R/W	0h	C1 coefficient for Interpolated Pixel. Used when field_id = 0
1-0	Reserved	R	0h	Reserved

1.3.1.4 CHR_US_reg3 Register (offset = 10h) [reset = 0h]

CHR_US_reg3 is shown in Figure 1-214 and described in Table 1-120.

Upsampling Coeffs

Figure 1-214. CHR_US_reg3 Register

31	30	29	28	27	26	25	24
INTERP_FID0_C2							
R/W-0h							

23	22	21	20	19	18	17	16
INTERP_FID0_C2						Reserved	
R/W-0h						R-0h	

15	14	13	12	11	10	9	8
INTERP_FID0_C3							
R/W-0h							

7	6	5	4	3	2	1	0
INTERP_FID0_C3						Reserved	
R/W-0h						R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-120. CHR_US_reg3 Register Field Descriptions

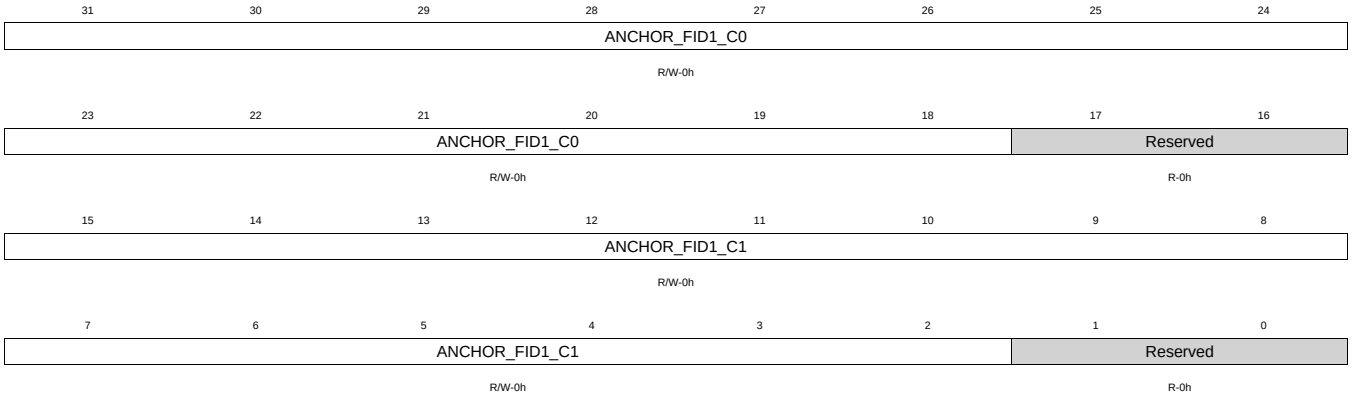
Bit	Field	Type	Reset	Description
31-18	INTERP_FID0_C2	R/W	0h	C2 coefficient for Interpolated Pixel. Used when field_id = 0
17-16	Reserved	R	0h	Reserved
15-2	INTERP_FID0_C3	R/W	0h	C3 coefficient for Interpolated Pixel. Used when field_id = 0
1-0	Reserved	R	0h	Reserved

1.3.1.5 CHR_US_reg4 Register (offset = 14h) [reset = 0h]

CHR_US_reg4 is shown in Figure 1-215 and described in Table 1-121.

Upsampling Coeffs

Figure 1-215. CHR_US_reg4 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-121. CHR_US_reg4 Register Field Descriptions

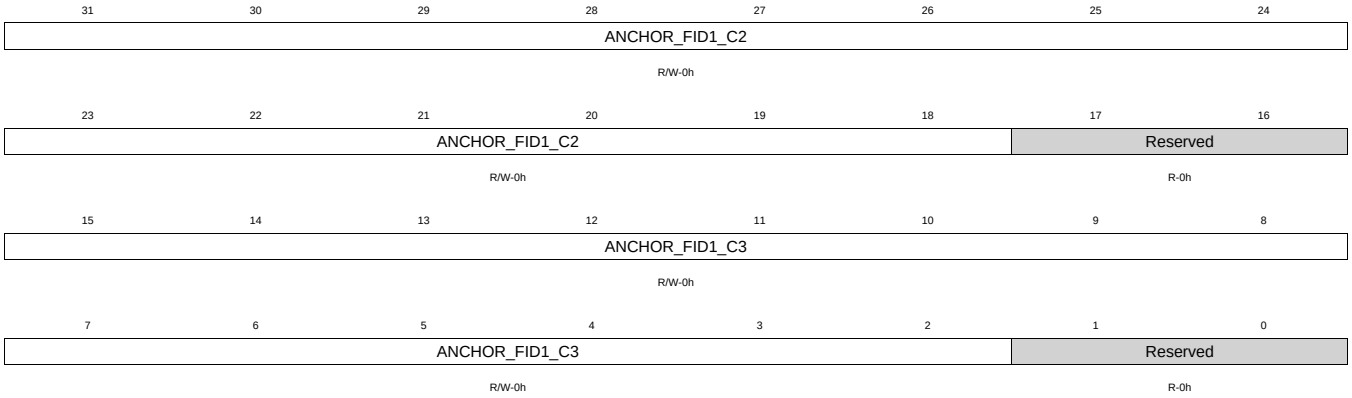
Bit	Field	Type	Reset	Description
31-18	ANCHOR_FID1_C0	R/W	0h	C0 coefficient for Anchor Pixel. Used when field_id = 1
17-16	Reserved	R	0h	Reserved
15-2	ANCHOR_FID1_C1	R/W	0h	C1 coefficient for Anchor Pixel. Used when field_id = 1
1-0	Reserved	R	0h	Reserved

1.3.1.6 CHR_US_reg5 Register (offset = 18h) [reset = 0h]

CHR_US_reg5 is shown in Figure 1-216 and described in Table 1-122.

Upsampling Coeffs

Figure 1-216. CHR_US_reg5 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-122. CHR_US_reg5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	ANCHOR_FID1_C2	R/W	0h	C2 coefficient for Anchor Pixel. Used when field_id = 1
17-16	Reserved	R	0h	Reserved
15-2	ANCHOR_FID1_C3	R/W	0h	C3 coefficient for Anchor Pixel. Used when field_id = 1
1-0	Reserved	R	0h	Reserved

1.3.1.7 CHR_US_reg6 Register (offset = 1Ch) [reset = 0h]

CHR_US_reg6 is shown in Figure 1-217 and described in Table 1-123.

Upsampling Coeffs

Figure 1-217. CHR_US_reg6 Register

31	30	29	28	27	26	25	24
INTERP_FID1_C0							
R/W-0h							

23	22	21	20	19	18	17	16
INTERP_FID1_C0						Reserved	
R/W-0h						R-0h	

15	14	13	12	11	10	9	8
INTERP_FID1_C1							
R/W-0h							

7	6	5	4	3	2	1	0
INTERP_FID1_C1						Reserved	
R/W-0h						R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-123. CHR_US_reg6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	INTERP_FID1_C0	R/W	0h	C0 coefficient for Interpolated Pixel. Used when field_id = 1
17-16	Reserved	R	0h	Reserved
15-2	INTERP_FID1_C1	R/W	0h	C1 coefficient for Interpolated Pixel. Used when field_id = 1
1-0	Reserved	R	0h	Reserved

1.3.1.8 CHR_US_reg7 Register (offset = 20h) [reset = 0h]

CHR_US_reg7 is shown in Figure 1-218 and described in Table 1-124.

Upsampling Coeffs

Figure 1-218. CHR_US_reg7 Register

31	30	29	28	27	26	25	24
INTERP_FID1_C2							
R/W-0h							

23	22	21	20	19	18	17	16
INTERP_FID1_C2						Reserved	
R/W-0h						R-0h	

15	14	13	12	11	10	9	8
INTERP_FID1_C3							
R/W-0h							

7	6	5	4	3	2	1	0
INTERP_FID1_C3						Reserved	
R/W-0h						R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-124. CHR_US_reg7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	INTERP_FID1_C2	R/W	0h	C2 coefficient for Interpolated Pixel. Used when field_id = 1
17-16	Reserved	R	0h	Reserved
15-2	INTERP_FID1_C3	R/W	0h	C3 coefficient for Interpolated Pixel. Used when field_id = 1
1-0	Reserved	R	0h	Reserved

1.3.2 CIG Registers

Table 1-125 lists the memory-mapped registers for the CIG. All register offset addresses not listed in Table 1-125 should be considered as reserved locations and the register contents should not be modified.

Table 1-125. CIG REGISTERS

Offset	Acronym	Register Name	Section
0h	CIG_reg0	CIG Mode Reg	Section 1.3.2.1
4h	CIG_reg1	CIG Display Config Reg	Section 1.3.2.2
8h	CIG_reg2	CIG HDMI Transparency Config Reg	Section 1.3.2.3
Ch	CIG_reg3	CIG HDMI Transparent Color	Section 1.3.2.4
10h	CIG_reg4	CIG HDCOMP Transparency Config Reg	Section 1.3.2.5
14h	CIG_reg5	CIG HDCOMP Transparent Color	Section 1.3.2.6
18h	CIG_reg6	CIG PIP Display Config Reg	Section 1.3.2.7
1Ch	CIG_reg7	CIG PIP Position Config Reg	Section 1.3.2.8
20h	CIG_reg8	CIG PIP Size Config Reg	Section 1.3.2.9
24h	CIG_reg9	CIG PIP Transparency Config Reg	Section 1.3.2.10
28h	CIG_reg10	CIG PIP Transparent Color	Section 1.3.2.11

1.3.2.1 CIG_reg0 Register (offset = 0h) [reset = 0h]

CIG_reg0 is shown in Figure 1-219 and described in Table 1-126.

CIG Mode Reg

Figure 1-219. CIG_reg0 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
PIP_P2I_EN	PIP_FULLSIZE	PIP_EN	CI_FIELD_RPT_EN	CI_VDEC_EN	CI_P2I_EN	P2I_EN	CIG_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-126. CIG_reg0 Register Field Descriptions

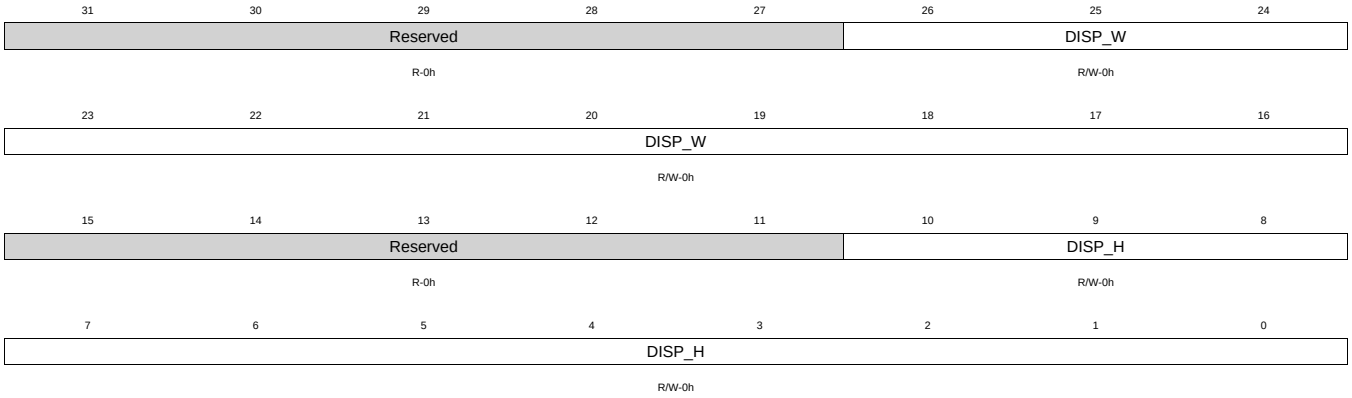
Bit	Field	Type	Reset	Description
31-8	Reserved	R	0h	Reserved
7	PIP_P2I_EN	R/W	0h	Enable Output Interlacing for PIP output 0: Disabled 1: Enabled
6	PIP_FULLSIZE	R/W	0h	CIG PIP window size 0: Sub-window 1: full-size
5	PIP_EN	R/W	0h	CIG PIP path enable 0: Disabled 1: Enabled
4	CI_FIELD_RPT_EN	R/W	0h	CIG filter field drop/repeat option enable for vertical filtering 0 : disable (use the Vertical filter) 1: enable (use field repeat)
3	CI_VDEC_EN	R/W	0h	CIG filter vertical decimation enable 0: Disabled (horizontal decimation only) 1: Enabled (both vertical and horizontal enabled)
2	CI_P2I_EN	R/W	0h	Enable Output Interlacing for Constrained output 0: Disabled 1: Enabled
1	P2I_EN	R/W	0h	Enable Output Interlacing for Non-constrained output 0: Disabled 1: Enabled
0	CIG_EN	R/W	0h	CIG module enable 0: Disabled (Bypass Mode) 1: CIG filter Enabled

1.3.2.2 CIG_reg1 Register (offset = 4h) [reset = 0h]

CIG_reg1 is shown in Figure 1-220 and described in Table 1-127.

CIG Display Config Reg

Figure 1-220. CIG_reg1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-127. CIG_reg1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	Reserved
26-16	DISP_W	R/W	0h	Output display Width (max = 1920)
15-11	Reserved	R	0h	Reserved
10-0	DISP_H	R/W	0h	Output display Height (max = 0x7FF)

1.3.2.3 CIG_reg2 Register (offset = 8h) [reset = 0h]

CIG_reg2 is shown in Figure 1-221 and described in Table 1-128.

CIG HDMI Transparency Config Reg

Figure 1-221. CIG_reg2 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved				BL_LEVEL			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
BL_LEVEL				BL_ENABLE	TR_MODE_MASK		TR_ENABLE
R/W-0h				R/W-0h	R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-128. CIG_reg2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	Reserved	R	0h	Reserved
11-4	BL_LEVEL	R/W	0h	Blending Value Assigned to the video pixel's alpha if blending is enabled.
3	BL_ENABLE	R/W	0h	Blending Enable 0: Disable Blending 1: Apply Blending
2-1	TR_MODE_MASK	R/W	0h	Transparency Color Mask Bit (Number of LSB bits to mask when checking for pixel transparency) 0: No masking 1: Mask 1 LSB bit 2: Mask 2 LSB bits 3: Mask 3 LSB bits
0	TR_ENABLE	R/W	0h	Transparency Enable 0: Disable Transparency 1: Enable Transparency

1.3.2.4 CIG_reg3 Register (offset = Ch) [reset = 0h]

CIG_reg3 is shown in Figure 1-222 and described in Table 1-129.

CIG HDMI Transparent Color

Figure 1-222. CIG_reg3 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
TR_COLOR							
R/W-0h							
15	14	13	12	11	10	9	8
TR_COLOR							
R/W-0h							
7	6	5	4	3	2	1	0
TR_COLOR							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-129. CIG_reg3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-0	TR_COLOR	R/W	0h	Transparency Color 23:16 R 15:8 G 7:0 B (If the video pixel matches this color while transparency is enabled, the alpha value is forced to 0.)

1.3.2.5 CIG_reg4 Register (offset = 10h) [reset = 0h]

CIG_reg4 is shown in Figure 1-223 and described in Table 1-130.

CIG HDCOMP Transparency Config Reg

Figure 1-223. CIG_reg4 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved				BL_LEVEL			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
BL_LEVEL				BL_ENABLE	TR_MODE_MASK		TR_ENABLE
R/W-0h				R/W-0h	R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-130. CIG_reg4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	Reserved	R	0h	Reserved
11-4	BL_LEVEL	R/W	0h	Blending Value Assigned to the video pixel's alpha if blending is enabled.
3	BL_ENABLE	R/W	0h	Blending Enable 0: Disable Blending 1: Apply Blending
2-1	TR_MODE_MASK	R/W	0h	Transparency Color Mask Bit (Number of LSB bits to mask when checking for pixel transparency) 0: No masking 1: Mask 1 LSB bit 2: Mask 2 LSB bits 3: Mask 3 LSB bits
0	TR_ENABLE	R/W	0h	Transparency Enable 0: Disable Transparency 1: Enable Transparency

1.3.2.6 CIG_reg5 Register (offset = 14h) [reset = 0h]

CIG_reg5 is shown in Figure 1-224 and described in Table 1-131.

CIG HDCOMP Transparent Color

Figure 1-224. CIG_reg5 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
TR_COLOR							
R/W-0h							

15	14	13	12	11	10	9	8
TR_COLOR							
R/W-0h							

7	6	5	4	3	2	1	0
TR_COLOR							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-131. CIG_reg5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-0	TR_COLOR	R/W	0h	Transparency Color 23:16 R 15:8 G 7:0 B (If the video pixel matches this color while transparency is enabled, the alpha value is forced to 0.)

1.3.2.7 CIG_reg6 Register (offset = 18h) [reset = 0h]

CIG_reg6 is shown in Figure 1-225 and described in Table 1-132.

CIG PIP Display Config Reg

Figure 1-225. CIG_reg6 Register

31	30	29	28	27	26	25	24
Reserved					PIP_DISP_W		
R-0h					R/W-0h		

23	22	21	20	19	18	17	16
PIP_DISP_W							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved					PIP_DISP_H		
R-0h					R/W-0h		

7	6	5	4	3	2	1	0
PIP_DISP_H							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-132. CIG_reg6 Register Field Descriptions

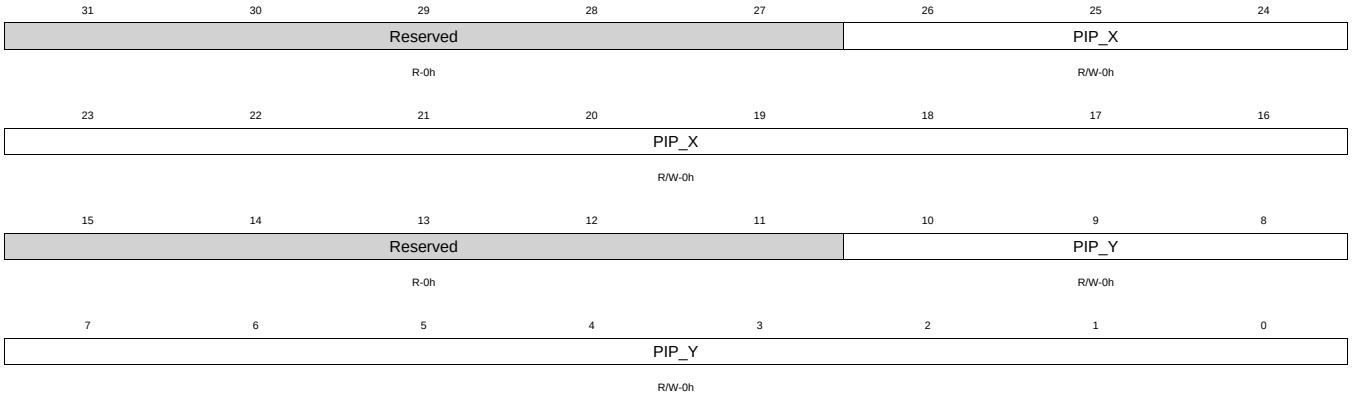
Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	Reserved
26-16	PIP_DISP_W	R/W	0h	PIP Output display Width (max = 1920)
15-11	Reserved	R	0h	Reserved
10-0	PIP_DISP_H	R/W	0h	PIP Output display Height (max = 0x7FF)

1.3.2.8 CIG_reg7 Register (offset = 1Ch) [reset = 0h]

CIG_reg7 is shown in Figure 1-226 and described in Table 1-133.

CIG PIP Position Config Reg

Figure 1-226. CIG_reg7 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-133. CIG_reg7 Register Field Descriptions

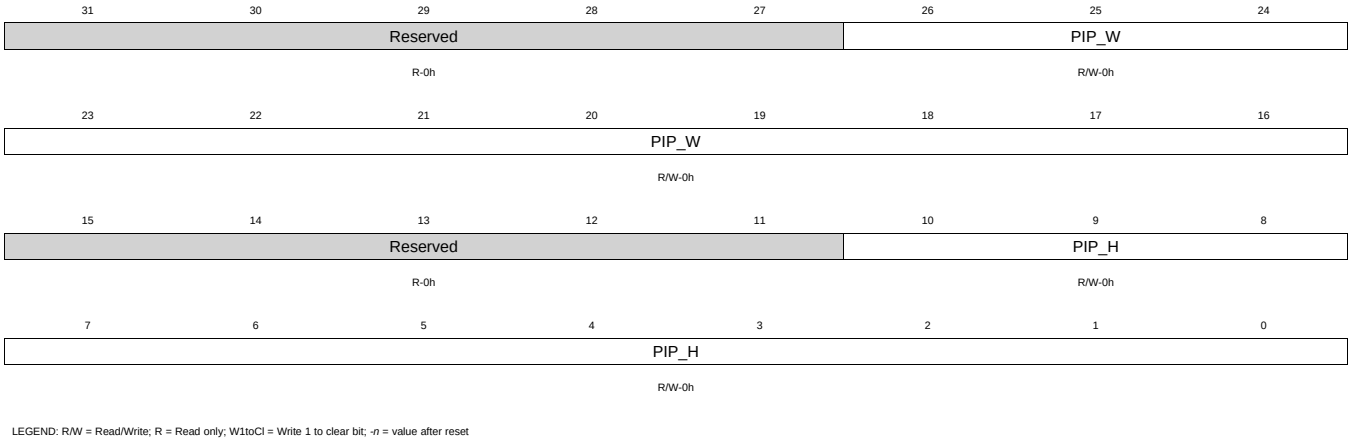
Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	Reserved
26-16	PIP_X	R/W	0h	PIP window X position
15-11	Reserved	R	0h	Reserved
10-0	PIP_Y	R/W	0h	PIP window Y position

1.3.2.9 CIG_reg8 Register (offset = 20h) [reset = 0h]

CIG_reg8 is shown in Figure 1-227 and described in Table 1-134.

CIG PIP Size Config Reg

Figure 1-227. CIG_reg8 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-134. CIG_reg8 Register Field Descriptions

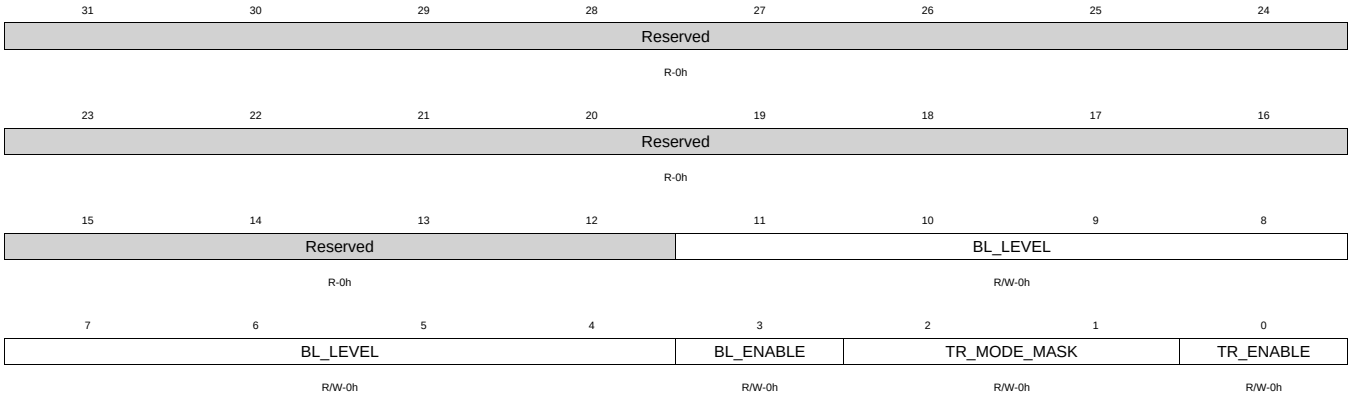
Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	Reserved
26-16	PIP_W	R/W	0h	PIP window Width (pip_x + pip_w must be less than or equal to disp_w)
15-11	Reserved	R	0h	Reserved
10-0	PIP_H	R/W	0h	PIP window Height (pip_y + pip_h must be less than or equal to disp_h)

1.3.2.10 CIG_reg9 Register (offset = 24h) [reset = 0h]

CIG_reg9 is shown in Figure 1-228 and described in Table 1-135.

CIG PIP Transparency Config Reg

Figure 1-228. CIG_reg9 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-135. CIG_reg9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	Reserved	R	0h	Reserved
11-4	BL_LEVEL	R/W	0h	Blending Value Assigned to the video pixel's alpha if blending is enabled.
3	BL_ENABLE	R/W	0h	Blending Enable 0: Disable Blending 1: Apply Blending
2-1	TR_MODE_MASK	R/W	0h	Transparency Color Mask Bit (Number of LSB bits to mask when checking for pixel transparency) 0: No masking 1: Mask 1 LSB bit 2: Mask 2 LSB bits 3: Mask 3 LSB bits
0	TR_ENABLE	R/W	0h	Transparency Enable 0: Disable Transparency 1: Enable Transparency

1.3.2.11 CIG_reg10 Register (offset = 28h) [reset = 0h]

CIG_reg10 is shown in Figure 1-229 and described in Table 1-136.

CIG PIP Transparent Color

Figure 1-229. CIG_reg10 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
TR_COLOR							
R/W-0h							
15	14	13	12	11	10	9	8
TR_COLOR							
R/W-0h							
7	6	5	4	3	2	1	0
TR_COLOR							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-136. CIG_reg10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-0	TR_COLOR	R/W	0h	Transparency Color 23:16 R 15:8 G 7:0 B (If the video pixel matches this color while transparency is enabled, the alpha value is forced to 0.)

1.3.3 COMP Registers

Table 1-137 lists the memory-mapped registers for the COMP. All register offset addresses not listed in Table 1-137 should be considered as reserved locations and the register contents should not be modified.

Table 1-137. COMP REGISTERS

Offset	Acronym	Register Name	Section
0h	COMP_status	Compositor Status	Section 1.3.3.1
4h	COMP_hdmi_settings	COMP HDMI/DVO1 Settings	Section 1.3.3.2
8h	COMP_dvo2_settings	COMP DVO2 Settings	Section 1.3.3.3
Ch	COMP_hdcomp_settings	COMP HDCOMP Settings	Section 1.3.3.4
10h	COMP_sd_settings	COMP SD Settings	Section 1.3.3.5
14h	COMP_back_color_settings	COMP Background Color Settings	Section 1.3.3.6

1.3.3.1 COMP_status Register (offset = 0h) [reset = 0h]

COMP_status is shown in Figure 1-230 and described in Table 1-138.

Compositor Status

Figure 1-230. COMP_status Register

31	30	29	28	27	26	25	24
Reserved	Reserved					SD_FMT	SD_ENABLE
R-0h						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
Reserved	Reserved					HDCOMP_FMT	HDCOMP_ENABLE
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
Reserved	Reserved					DVO2_FMT	DVO2_ENABLE
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
Reserved	Reserved					HDMI_FMT	HDMI_ENABLE
R-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-138. COMP_status Register Field Descriptions

Bit	Field	Type	Reset	Description
30-26	Reserved	R	0h	Reserved
25	SD_FMT	R/W	0h	SD Scan Format 1: interlace format 0: progressive format
24	SD_ENABLE	R/W	0h	SD Blender enable 0 : Disabled 1 : Enabled
22-18	Reserved	R	0h	Reserved
17	HDCOMP_FMT	R/W	0h	HDCOMP Scan Format 1: interlace format 0: progressive format
16	HDCOMP_ENABLE	R/W	0h	HDCOMP Blender enable 0 : Disabled 1 : Enabled
14-10	Reserved	R	0h	Reserved
9	DVO2_FMT	R/W	0h	DVO2 Scan Format 1: interlace format 0: progressive format
8	DVO2_ENABLE	R/W	0h	DVO2 Blender enable 0 : Disabled 1 : Enabled
6-2	Reserved	R	0h	Reserved
1	HDMI_FMT	R/W	0h	HDMI/DVO1 Scan Format 1: interlace format 0: progressive format
0	HDMI_ENABLE	R/W	0h	HDMI/DVO1 Blender enable 0 : Disabled 1 : Enabled

1.3.3.2 COMP_hdmi_settings Register (offset = 4h) [reset = E400h]

COMP_hdmi_settings is shown in Figure 1-231 and described in Table 1-139.

COMP HDMI/DVO1 Settings

Figure 1-231. COMP_hdmi_settings Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							FB_SEL
R-0h							R/W-0h

15	14	13	12	11	10	9	8
G2_ORDER		G1_ORDER		G0_ORDER		VID_ORDER	
R/W-3h		R/W-2h		R/W-1h		R/W-0h	

7	6	5	4	3	2	1	0
G_ORDER	VID_BLD_ORDER	VID_EN	Reserved	PIP_EN	GRPX0_EN	GRPX1_EN	GRPX2_EN
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-139. COMP_hdmi_settings Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	Reserved	R	0h	Reserved
16	FB_SEL	R/W	0h	Feedback data selection 0: select data from video alpha blending 1: select data from final alpha blending
15-14	G2_ORDER	R/W	3h	Graphic2 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
13-12	G1_ORDER	R/W	2h	Graphic1 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
11-10	G0_ORDER	R/W	1h	Graphic0 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
9-8	VID_ORDER	R/W	0h	Video layer display order. From low to high: 00, 01, 10, and 11.
7	G_ORDER	R/W	0h	Global reorder. 1: global reorder is on. The graphic layer priority is based on g0_reorder, g1_reorder, g2_order
6	VID_BLD_ORDER	R/W	0h	Video Build Order 0: Use HD_VID as base (lower) layer for video stream 1: Use HD_PIP as base (lower) layer for video stream
5	VID_EN	R/W	0h	HD VID channel Enable 0 : Disabled 1 : Enabled
4	Reserved	R	0h	Reserved
3	PIP_EN	R/W	0h	HD PIP channel enable 0 : Disabled 1 : Enabled
2	GRPX0_EN	R/W	0h	GRPX2 channel enable 0 : Disabled 1 : Enabled
1	GRPX1_EN	R/W	0h	GRPX1 channel enable 0 : Disabled 1 : Enabled
0	GRPX2_EN	R/W	0h	GRPX2 channel enable 0 : Disabled 1 : Enabled

1.3.3.3 COMP_dvo2_settings Register (offset = 8h) [reset = E400h]

COMP_dvo2_settings is shown in Figure 1-232 and described in Table 1-140.

Figure 1-232. COMP_dvo2_settings Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							FB_SEL
R-0h							R/W-0h

15	14	13	12	11	10	9	8
G2_ORDER		G1_ORDER		G0_ORDER		VID_ORDER	
R/W-3h		R/W-2h		R/W-1h		R/W-0h	

7	6	5	4	3	2	1	0
G_ORDER	VID_BLD_ORDER	VID_EN	Reserved	PIP_EN	GRPX0_EN	GRPX1_EN	GRPX2_EN
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-140. COMP_dvo2_settings Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	Reserved	R	0h	Reserved
16	FB_SEL	R/W	0h	Feedback data selection: 0: select data from video alpha blending 1: select data from final alpha blending
15-14	G2_ORDER	R/W	3h	Graphic2 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
13-12	G1_ORDER	R/W	2h	Graphic1 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
11-10	G0_ORDER	R/W	1h	Graphic0 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
9-8	VID_ORDER	R/W	0h	Video layer display order. From low to high: 00, 01, 10, and 11.
7	G_ORDER	R/W	0h	Global reorder. 1: global reorder is on. The graphic layer priority is based on g0_reorder, g1_reorder, g2_order settings 0: no global reorder. The graphic layer priority is based priority bits [35:32] in the data bus.
6	VID_BLD_ORDER	R/W	0h	Video Build Order 1: Use HD_PIP as base (lower) layer for video stream 0: Use HD_vid as base (lower) layer for video stream
5	VID_EN	R/W	0h	HD VID channel Enable 0 : Disabled 1 : Enabled
4	Reserved	R	0h	Reserved
3	PIP_EN	R/W	0h	HD PIP channel enable 0 : Disabled 1 : Enabled
2	GRPX0_EN	R/W	0h	GRPX0 channel enable 0 : Disabled 1 : Enabled
1	GRPX1_EN	R/W	0h	GRPX1 channel enable 0 : Disabled 1 : Enabled
0	GRPX2_EN	R/W	0h	GRPX2 channel enable 0 : Disabled 1 : Enabled

1.3.3.4 COMP_hdcomp_settings Register (offset = Ch) [reset = E400h]

COMP_hdcomp_settings is shown in Figure 1-233 and described in Table 1-141.

Figure 1-233. COMP_hdcomp_settings Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							FB_SEL
R-0h							R/W-0h

15	14	13	12	11	10	9	8
G2_ORDER		G1_ORDER		G0_ORDER		VID_ORDER	
R/W-3h		R/W-2h		R/W-1h		R/W-0h	

7	6	5	4	3	2	1	0
G_ORDER	VID_BLD_ORDER	VID_EN	Reserved	PIP_EN	GRPX0_EN	GRPX1_EN	GRPX2_EN
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-141. COMP_hdcomp_settings Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	Reserved	R	0h	Reserved
16	FB_SEL	R/W	0h	Feedback data selection: 0: select data from video alpha blending 1: select data from final alpha blending
15-14	G2_ORDER	R/W	3h	Graphic2 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
13-12	G1_ORDER	R/W	2h	Graphic1 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
11-10	G0_ORDER	R/W	1h	Graphic0 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
9-8	VID_ORDER	R/W	0h	Video layer display order. From low to high: 00, 01, 10, and 11.
7	G_ORDER	R/W	0h	Global reorder. 1: global reorder is on. The graphic layer priority is based on g0_reorder, g1_reorder, g2_order settings 0: no global reorder. The graphic layer priority is based priority bits [35:32] in the data bus.
6	VID_BLD_ORDER	R/W	0h	Video Build Order 1: Use HD_PIP as base (lower) layer for video stream 0: Use HD_vid as base (lower) layer for video stream
5	VID_EN	R/W	0h	HD VID channel Enable 0 : Disabled 1 : Enabled
4	Reserved	R	0h	Reserved
3	PIP_EN	R/W	0h	HD PIP channel enable 0 : Disabled 1 : Enabled
2	GRPX0_EN	R/W	0h	GRPX0 channel enable 0 : Disabled 1 : Enabled
1	GRPX1_EN	R/W	0h	GRPX1 channel enable 0 : Disabled 1 : Enabled
0	GRPX2_EN	R/W	0h	GRPX2 channel enable 0 : Disabled 1 : Enabled

1.3.3.5 COMP_sd_settings Register (offset = 10h) [reset = E400h]

COMP_sd_settings is shown in Figure 1-234 and described in Table 1-142.

Figure 1-234. COMP_sd_settings Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							FB_SEL
R-0h							R/W-0h
15	14	13	12	11	10	9	8
G2_ORDER		G1_ORDER		G0_ORDER		VID_ORDER	
R/W-3h		R/W-2h		R/W-1h		R/W-0h	
7	6	5	4	3	2	1	0
G_ORDER	Reserved	VID_EN	Reserved		GRPX0_EN	GRPX1_EN	GRPX2_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-142. COMP_sd_settings Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	Reserved	R	0h	Reserved
16	FB_SEL	R/W	0h	Feedback data selection: 0: select data from video alpha blending 1: select data from final alpha blending
15-14	G2_ORDER	R/W	3h	Graphic2 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
13-12	G1_ORDER	R/W	2h	Graphic1 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
11-10	G0_ORDER	R/W	1h	Graphic0 layer display order when g_order = 1. From low to high: 00, 01, 10, and 11.
9-8	VID_ORDER	R/W	0h	Video layer display order. From low to high: 00, 01, 10, and 11.
7	G_ORDER	R/W	0h	Global reorder. 1: global reorder is on. The graphic layer priority is based on g0_reorder, g1_reorder, g2_order
6	Reserved	R	0h	Reserved
5	VID_EN	R/W	0h	SD VID channel Enable 0 : Disabled 1 : Enabled
4-3	Reserved	R	0h	Reserved
2	GRPX0_EN	R/W	0h	GRPX0 channel enable 0 : Disabled 1 : Enabled
1	GRPX1_EN	R/W	0h	GRPX1 channel enable 0 : Disabled 1 : Enabled
0	GRPX2_EN	R/W	0h	GRPX2 channel enable 0 : Disabled 1 : Enabled

1.3.3.6 COMP_back_color_settings Register (offset = 14h) [reset = 0h]

COMP_back_color_settings is shown in Figure 1-235 and described in Table 1-143.

Figure 1-235. COMP_back_color_settings Register

31	30	29	28	27	26	25	24
Reserved		BACK_CLR					
R-0h		R/W-0h					

23	22	21	20	19	18	17	16
BACK_CLR							
R/W-0h							

15	14	13	12	11	10	9	8
BACK_CLR							
R/W-0h							

7	6	5	4	3	2	1	0
BACK_CLR							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-143. COMP_back_color_settings Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	Reserved
29-0	BACK_CLR	R/W	0h	Background color in RGB format. This color will replace any pixel with alpha value of 0. It is also output to VENCs to be used if channel is not enabled or an underflow occurs

1.3.4 CSC Registers

Table 1-144 lists the memory-mapped registers for the CSC. All register offset addresses not listed in Table 1-144 should be considered as reserved locations and the register contents should not be modified.

Table 1-144. CSC REGISTERS

Offset	Acronym	Register Name	Section
0h	CSC_csc00	Color Space Converter Reg00	Section 1.3.4.1
4h	CSC_csc01	Color Space Converter Reg01	Section 1.3.4.2
8h	CSC_csc02	Color Space Converter Reg02	Section 1.3.4.3
Ch	CSC_csc03	Color Space Converter Reg03	Section 1.3.4.4
10h	CSC_csc04	Color Space Converter Reg04	Section 1.3.4.5
14h	CSC_csc05	Color Space Converter Reg05	Section 1.3.4.6

1.3.4.1 CSC_csc00 Register (offset = 0h) [reset = 0h]

CSC_csc00 is shown in Figure 1-236 and described in Table 1-145.

Color Space Converter Reg00

Figure 1-236. CSC_csc00 Register

31	30	29	28	27	26	25	24
Reserved			B0				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
B0							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			A0				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
A0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-145. CSC_csc00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-16	B0	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in CSC_csc00)
15-13	Reserved	R	0h	Reserved
12-0	A0	R/W	0h	Its is represented as Q3.10 number. So the value ranges from -4 to +4. To convert a decimal number, multiply the number by 1024 and write it in the register in hex format. For example, to program 0.673, 0x2B1 should be written in the register. (round)(0.673 X 1024) = (round)689.152 = 689 = 0x2B1. If the real number is negative, then multiply it by 1024, and convert it to 2's compliment format in 12-bit. For example, if a coefficient is -1.893, 0x186E needs to be written in the register. (round)(-1.893*1024)= -1938 = 0x186E (2'S compliment format of -1938 in 13-bit width)

1.3.4.2 CSC_csc01 Register (offset = 4h) [reset = 0h]

CSC_csc01 is shown in Figure 1-237 and described in Table 1-146.

Color Space Converter Reg01

Figure 1-237. CSC_csc01 Register

31	30	29	28	27	26	25	24
Reserved			A1				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
A1							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			C0				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
C0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-146. CSC_csc01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-16	A1	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in CSC_csc00)
15-13	Reserved	R	0h	Reserved
12-0	C0	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in CSC_csc00)

1.3.4.3 CSC_csc02 Register (offset = 8h) [reset = 0h]

CSC_csc02 is shown in Figure 1-238 and described in Table 1-147.

Color Space Converter Reg02

Figure 1-238. CSC_csc02 Register

31	30	29	28	27	26	25	24
Reserved			C1				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
C1							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			B1				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
B1							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-147. CSC_csc02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-16	C1	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in CSC_csc00)
15-13	Reserved	R	0h	Reserved
12-0	B1	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in CSC_csc00)

1.3.4.4 CSC_csc03 Register (offset = Ch) [reset = 0h]

CSC_csc03 is shown in Figure 1-239 and described in Table 1-148.

Color Space Converter Reg03

Figure 1-239. CSC_csc03 Register

31	30	29	28	27	26	25	24
Reserved			B2				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
B2							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			A2				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
A2							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-148. CSC_csc03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-16	B2	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in CSC_csc00)
15-13	Reserved	R	0h	Reserved
12-0	A2	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in CSC_csc00)

1.3.4.5 CSC_csc04 Register (offset = 10h) [reset = 0h]

CSC_csc04 is shown in Figure 1-240 and described in Table 1-149.

Color Space Converter Reg04

Figure 1-240. CSC_csc04 Register

31	30	29	28	27	26	25	24
Reserved				D0			
R-0h				R/W-0h			

23	22	21	20	19	18	17	16
D0							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved			C2				
R-0h			R/W-0h				

7	6	5	4	3	2	1	0
C2							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-149. CSC_csc04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	Reserved
27-16	D0	R/W	0h	Coefficients of color space converter. This coefficient is an integer number in the range of -2048 to 2047. It is in 12-bit wide 2's compliment format. The MSB is sign bit. For example, if this coefficient is 749, then 0x2ED (hex format) should be assigned to this register. Another example, if this coefficient is -1021, then 0xC03 should be assigned to this register.
15-13	Reserved	R	0h	Reserved
12-0	C2	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in CSC_csc00)

1.3.4.6 CSC_csc05 Register (offset = 14h) [reset = 0h]

CSC_csc05 is shown in Figure 1-241 and described in Table 1-150.

Color Space Converter Reg05

Figure 1-241. CSC_csc05 Register

31	30	29	28	27	26	25	24
Reserved			BYPASS	D2			
R-0h			R/W-0h	R/W-0h			
23	22	21	20	19	18	17	16
D2							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved				D1			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
D1							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-150. CSC_csc05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28	BYPASS	R/W	0h	Full CSC bypass mode
27-16	D2	R/W	0h	Coefficients of color space converter. This coefficient is an integer number in the range of -2048 to 2047. It is in 12-bit wide 2's compliment format. The MSB is sign bit. (Same format conversion as D0 in CSC_csc04)
15-12	Reserved	R	0h	Reserved
11-0	D1	R/W	0h	Coefficients of color space converter. This coefficient is an integer number in the range of -2048 to 2047. It is in 12-bit wide 2's compliment format. The MSB is sign bit. (Same format conversion as D0 in CSC_csc04)

1.3.5 DEI Registers

Table 1-151 lists the memory-mapped registers for the DEI. All register offset addresses not listed in Table 1-151 should be considered as reserved locations and the register contents should not be modified.

Table 1-151. DEI REGISTERS

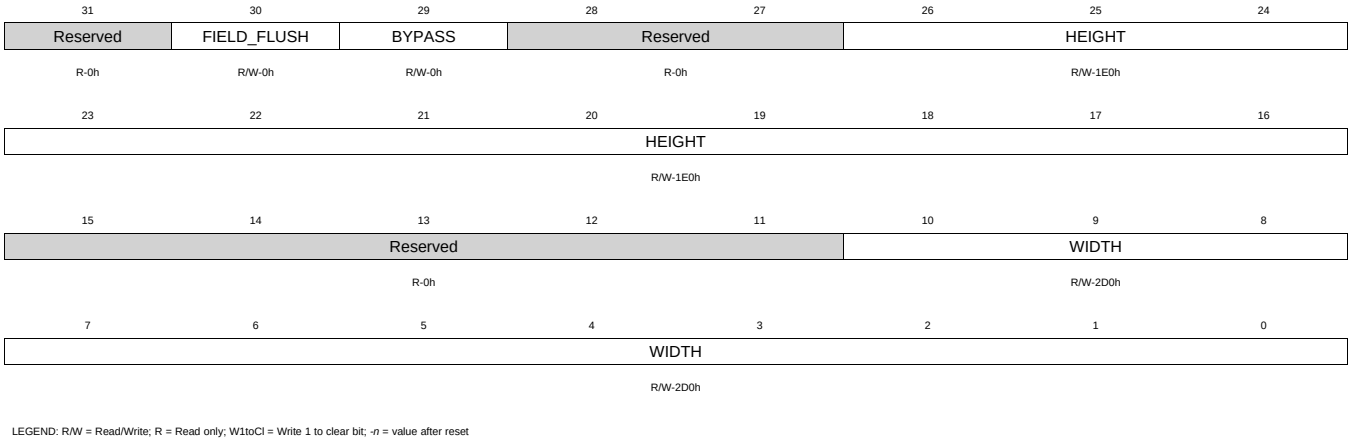
Offset	Acronym	Register Name	Section
0h	dei_reg0	Frame Size Register	Section 1.3.5.1
4h	dei_reg1	MDT Filter Bypass Register	Section 1.3.5.2
8h	dei_reg2	MDT Spatial Frequency Threshold Register	Section 1.3.5.3
Ch	dei_reg3	EDI Configuration Control	Section 1.3.5.4
10h	dei_reg4	EDI Lookup Table Register 0	Section 1.3.5.5
14h	dei_reg5	EDI Lookup Table Register 1	Section 1.3.5.6
18h	dei_reg6	EDI Lookup Table Register 2	Section 1.3.5.7
1Ch	dei_reg7	EDI Lookup Table Register 3	Section 1.3.5.8
20h	dei_reg8	FMD Window Register 0	Section 1.3.5.9
24h	dei_reg9	FMD Window Register 1	Section 1.3.5.10
28h	dei_reg10	FMD Control Register 0	Section 1.3.5.11
2Ch	dei_reg11	FMD Control Register 0	Section 1.3.5.12
30h	dei_reg12	FMD Status Register 0	Section 1.3.5.13
34h	dei_reg13	FMD Status Register 1	Section 1.3.5.14
38h	dei_reg14	FMD Status Register 2	Section 1.3.5.15

1.3.5.1 dei_reg0 Register (offset = 0h) [reset = 01E002D0h]

dei_reg0 is shown in Figure 1-242 and described in Table 1-152.

Frame Size Register

Figure 1-242. dei_reg0 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-152. dei_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Reserved	R	0h	Reserved
30	FIELD_FLUSH	R/W	0h	Field Flush Mode 0: Normal Operation 1: Flush Internal Pipe for Current output Frame
29	BYPASS	R/W	0h	Bypass Mode 0: Normal Deinterlace Mode 1: Input Source bypassed directly to output
28-27	Reserved	R	0h	Reserved
26-16	HEIGHT	R/W	1E0h	Frame height
15-11	Reserved	R	0h	Reserved
10-0	WIDTH	R/W	2D0h	Frame Width

1.3.5.2 dei_reg1 Register (offset = 4h) [reset = 0h]

dei_reg1 is shown in Figure 1-243 and described in Table 1-153.

MDT Filter Bypass Register

Figure 1-243. dei_reg1 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
Reserved						MDT_SPATMAX_BYPASS	MDT_TEMPMAX_BYPASS
R-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-153. dei_reg1 Register Field Descriptions

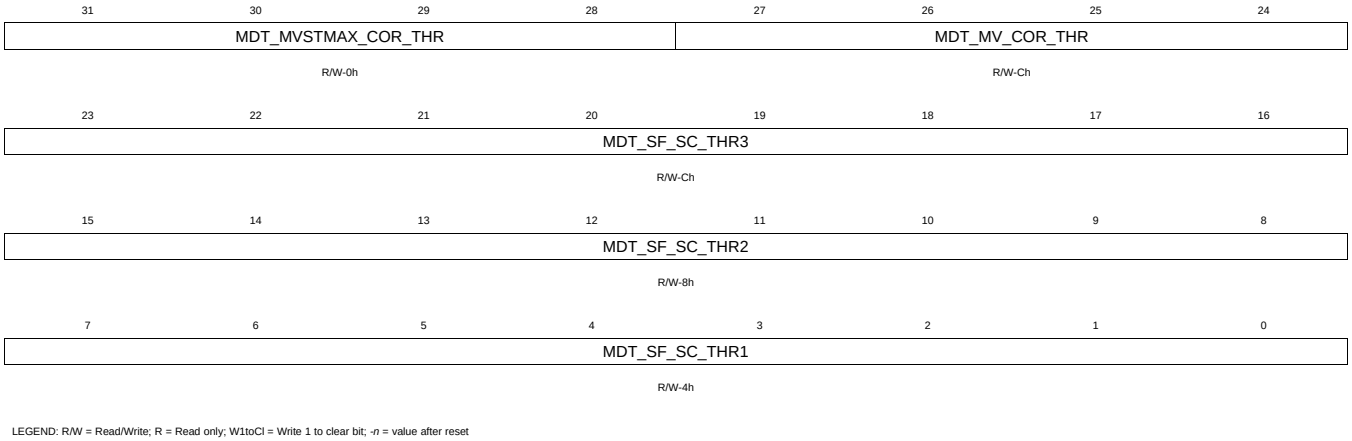
Bit	Field	Type	Reset	Description
31-2	Reserved	R	0h	Reserved
1	MDT_SPATMAX_BYPASS	R/W	0h	Spatial Maximum Filtering Bypass for motion values used in EDI 0: Enable 1: Bypass
0	MDT_TEMPMAX_BYPASS	R/W	0h	Spatio-temporal Maximum Filtering Bypass for motion valued used in EDI 0: Enable 1: Bypass

1.3.5.3 dei_reg2 Register (offset = 8h) [reset = 0C0C0804h]

dei_reg2 is shown in Figure 1-244 and described in Table 1-154.

MDT Spatial Frequency Threshold Register

Figure 1-244. dei_reg2 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-154. dei_reg2 Register Field Descriptions

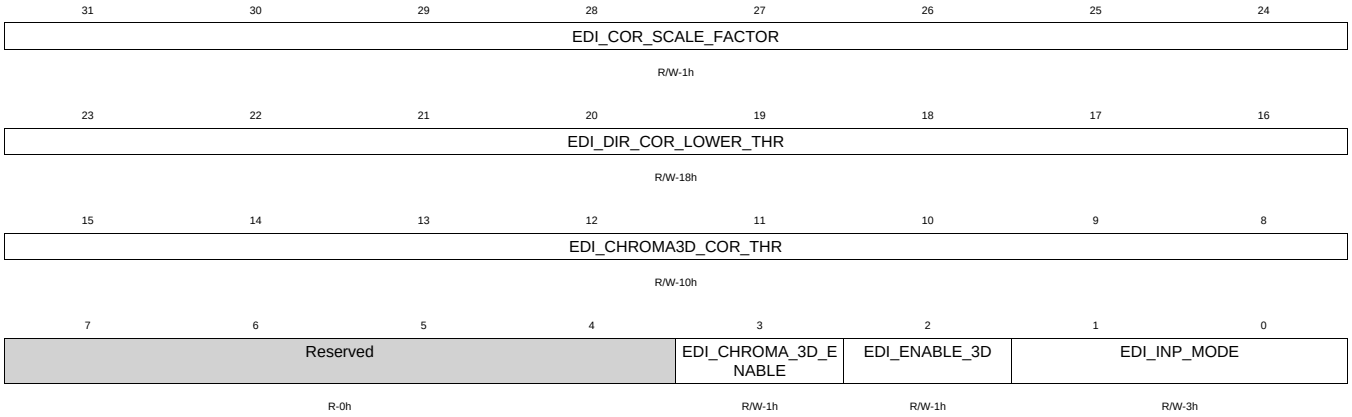
Bit	Field	Type	Reset	Description
31-28	MDT_MVSTMAX_COR_THR	R/W	0h	This is used for increasing noise robustness. Increasing this threshold leads to more robustness to noise, but with the potential of introducing ghosting effect. Note that this threshold is used for motion values for EDI only, and it is in addition mdt_mv_cor_thr.
27-24	MDT_MV_COR_THR	R/W	Ch	This threshold is for the coring for motion value, mv. MDT will become more noise robust if this value increases. But the picture may be washed out if this value is set to high. This threshold can be interpreted as the noise threshold for calculating motion values for all blocks.
23-16	MDT_SF_SC_THR3	R/W	Ch	Spatial frequency threshold 3
15-8	MDT_SF_SC_THR2	R/W	8h	Spatial frequency threshold 2
7-0	MDT_SF_SC_THR1	R/W	4h	Spatial frequency threshold It is used for adaptive scaling of motion values according to how busy the texture is. If the texture is flat, motion values need to be scaled up to reflect the sensitivity of motion values with respect to the detection error. Increasing the thresholds will make the motion value scaling more sensitive to the frequency of the texture. Note: 0 <= mdt_sf_sc_thr1 <= mdt_sf_sc_thr2 <= mdt_sf_sc_thr3

1.3.5.4 dei_reg3 Register (offset = Ch) [reset = 0118100Fh]

dei_reg3 is shown in Figure 1-245 and described in Table 1-155.

EDI Configuration Control

Figure 1-245. dei_reg3 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-155. dei_reg3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	EDI_COR_SCALE_FACTOR	R/W	1h	Scaling factor for correlation along detected edge
23-16	EDI_DIR_COR_LOWER_THR	R/W	18h	Lower threshold used for correlation along detected edge
15-8	EDI_CHROMA3D_COR_THR	R/W	10h	Correlation threshold used in 3D processing for chroma. Because the motion values used for chroma 3D processing are based on luma only. Extra protection is needed. Temporal interpolation is only performed for chroma, when there is strong spatial or temporal correlation for the chroma pixel being processed. When the pixel difference is less than this threshold, it is assumed that there exists strong correlation between these two pixels. Thus, increasing this value leads to more chroma pixels being processed in 3D.
7-4	Reserved	R	0h	Reserved
3	EDI_CHROMA_3D_ENABLE	R/W	1h	3D Chroma Enable 0: Disable 3D processing for chroma 1: Enable 3D processing (temporal interpolation)
2	EDI_ENABLE_3D	R/W	1h	3D Enable 0: Disable 3D processing 1: Enable 3D processing (temporal interpolation)
1-0	EDI_INP_MODE	R/W	3h	Interpolation mode 00: line average 01: field average 10: edge-directed interpolation for luma only 11: edge-directed interpolation for both luma and chroma Note that mode 00 and 01 are used for debug purpose

1.3.5.5 dei_reg4 Register (offset = 10h) [reset = 08040200h]

dei_reg4 is shown in Figure 1-246 and described in Table 1-156.

EDI Lookup Table Register 0

Figure 1-246. dei_reg4 Register

31	30	29	28	27	26	25	24
Reserved			EDI_LUT3				
R-0h			R/W-8h				
23	22	21	20	19	18	17	16
Reserved			EDI_LUT2				
R-0h			R/W-4h				
15	14	13	12	11	10	9	8
Reserved			EDI_LUT1				
R-0h			R/W-2h				
7	6	5	4	3	2	1	0
Reserved			EDI_LUT0				
R-0h			R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-156. dei_reg4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-24	EDI_LUT3	R/W	8h	EDI Lookup Table 3
23-21	Reserved	R	0h	Reserved
20-16	EDI_LUT2	R/W	4h	EDI Lookup Table 2
15-13	Reserved	R	0h	Reserved
12-8	EDI_LUT1	R/W	2h	EDI Lookup Table 1
7-5	Reserved	R	0h	Reserved
4-0	EDI_LUT0	R/W	0h	EDI Lookup Table 0

Note: 0<=EDI_LUT0 <=EDI_LUT1 <=EDI_LUT2 <=EDI_LUT3.....<=EDI_LUT15

1.3.5.6 dei_reg5 Register (offset = 14h) [reset = 1010100Ch]

dei_reg5 is shown in Figure 1-247 and described in Table 1-157.

EDI Lookup Table Register 1

Figure 1-247. dei_reg5 Register

31	30	29	28	27	26	25	24
Reserved			EDI_LUT7				
R-0h			R/W-10h				
23	22	21	20	19	18	17	16
Reserved			EDI_LUT6				
R-0h			R/W-10h				
15	14	13	12	11	10	9	8
Reserved			EDI_LUT5				
R-0h			R/W-10h				
7	6	5	4	3	2	1	0
Reserved			EDI_LUT4				
R-0h			R/W-Ch				

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-157. dei_reg5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-24	EDI_LUT7	R/W	10h	EDI Lookup Table 7
23-21	Reserved	R	0h	Reserved
20-16	EDI_LUT6	R/W	10h	EDI Lookup Table 6
15-13	Reserved	R	0h	Reserved
12-8	EDI_LUT5	R/W	10h	EDI Lookup Table 5
7-5	Reserved	R	0h	Reserved
4-0	EDI_LUT4	R/W	Ch	EDI Lookup Table 4

1.3.5.7 dei_reg6 Register (offset = 18h) [reset = 10101010h]

dei_reg6 is shown in Figure 1-248 and described in Table 1-158.

EDI Lookup Table Register 2

Figure 1-248. dei_reg6 Register

31	30	29	28	27	26	25	24
Reserved			EDI_LUT11				
R-0h			R/W-10h				
23	22	21	20	19	18	17	16
Reserved			EDI_LUT10				
R-0h			R/W-10h				
15	14	13	12	11	10	9	8
Reserved			EDI_LUT9				
R-0h			R/W-10h				
7	6	5	4	3	2	1	0
Reserved			EDI_LUT8				
R-0h			R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-158. dei_reg6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-24	EDI_LUT11	R/W	10h	EDI Lookup Table 11
23-21	Reserved	R	0h	Reserved
20-16	EDI_LUT10	R/W	10h	EDI Lookup Table 10
15-13	Reserved	R	0h	Reserved
12-8	EDI_LUT9	R/W	10h	EDI Lookup Table 9
7-5	Reserved	R	0h	Reserved
4-0	EDI_LUT8	R/W	10h	EDI Lookup Table 8

1.3.5.8 dei_reg7 Register (offset = 1Ch) [reset = 10101010h]

dei_reg7 is shown in Figure 1-249 and described in Table 1-159.

EDI Lookup Table Register 3

Figure 1-249. dei_reg7 Register

31	30	29	28	27	26	25	24
Reserved			EDI_LUT15				
R-0h			R/W-10h				
23	22	21	20	19	18	17	16
Reserved			EDI_LUT14				
R-0h			R/W-10h				
15	14	13	12	11	10	9	8
Reserved			EDI_LUT13				
R-0h			R/W-10h				
7	6	5	4	3	2	1	0
Reserved			EDI_LUT12				
R-0h			R/W-10h				

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-159. dei_reg7 Register Field Descriptions

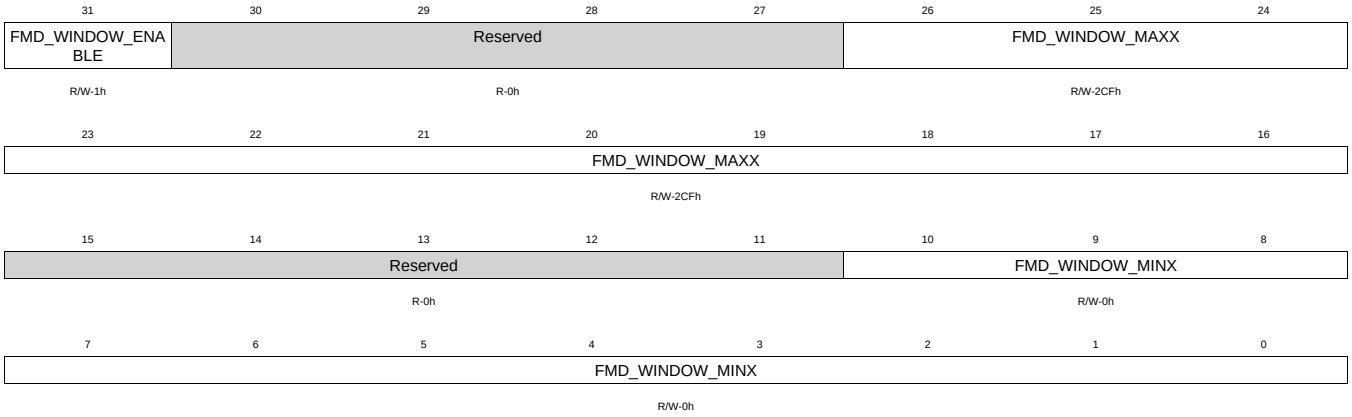
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-24	EDI_LUT15	R/W	10h	EDI Lookup Table 15
23-21	Reserved	R	0h	Reserved
20-16	EDI_LUT14	R/W	10h	EDI Lookup Table 14
15-13	Reserved	R	0h	Reserved
12-8	EDI_LUT13	R/W	10h	EDI Lookup Table 13
7-5	Reserved	R	0h	Reserved
4-0	EDI_LUT12	R/W	10h	EDI Lookup Table 12

1.3.5.9 dei_reg8 Register (offset = 20h) [reset = 82CF0000h]

dei_reg8 is shown in Figure 1-250 and described in Table 1-160.

FMD Window Register 0

Figure 1-250. dei_reg8 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-160. dei_reg8 Register Field Descriptions

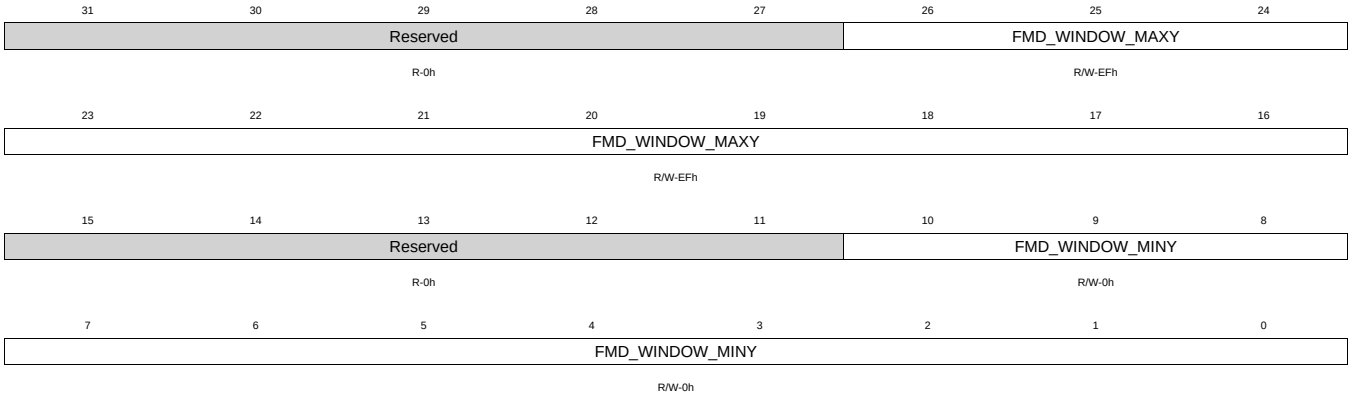
Bit	Field	Type	Reset	Description
31	FMD_WINDOW_ENABLE	R/W	1h	Enable FMD operation window
30-27	Reserved	R	0h	Reserved
26-16	FMD_WINDOW_MAXX	R/W	2CFh	Right boundary of FMD operation window Must be less than width
15-11	Reserved	R	0h	Reserved
10-0	FMD_WINDOW_MINX	R/W	0h	Left boundary of FMD operation window

1.3.5.10 dei_reg9 Register (offset = 24h) [reset = 00EF0000h]

dei_reg9 is shown in Figure 1-251 and described in Table 1-161.

FMD Window Register 1

Figure 1-251. dei_reg9 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-161. dei_reg9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	Reserved
26-16	FMD_WINDOW_MAXY	R/W	EFh	Bottom boundary of FMD operation window Must be less than height/2
15-11	Reserved	R	0h	Reserved
10-0	FMD_WINDOW_MINY	R/W	0h	Top boundary of FMD operation window

1.3.5.11 dei_reg10 Register (offset = 28h) [reset = 080A0000h]

dei_reg10 is shown in Figure 1-252 and described in Table 1-162.

FMD Control Register 0

Figure 1-252. dei_reg10 Register

31	30	29	28	27	26	25	24
FMD_CAF_LINE_THR							
R/W-8h							
23	22	21	20	19	18	17	16
FMD_CAF_FIELD_THR							
R/W-Ah							
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
Reserved				FMD_BED_ENABLE	FMD_JAM_DIR	FMD_LOCK	FMD_ENABLE
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-162. dei_reg10 Register Field Descriptions

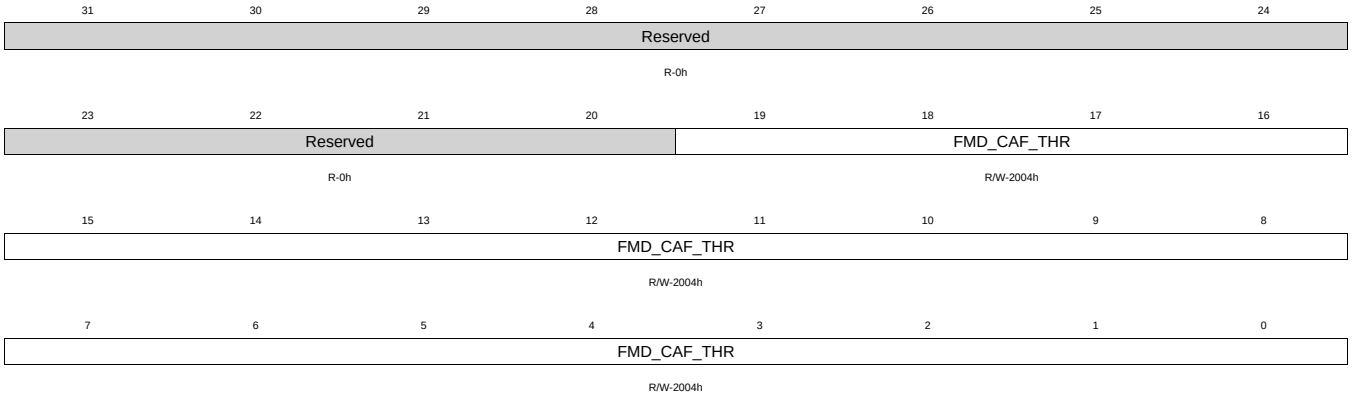
Bit	Field	Type	Reset	Description
31-24	FMD_CAF_LINE_THR	R/W	8h	CAF (Combing Artifacts) threshold used for the pixels from two lines in one field This is the threshold used for combing artifacts detection. The difference of two consecutive lines from the same field (so there is one line in between if two fields are merged into one progressive frame) is compared with this threshold. Decreasing this threshold leads to be more conservative in detecting CAF. Both fmd_caf_field_thr and fmd_caf_line_thr are close the values that two pixels differed by this value is observable.
23-16	FMD_CAF_FIELD_THR	R/W	Ah	CAF (Combing Artifacts) threshold used for the pixels from two fields This is the threshold used for combing artifacts detection. The difference of two consecutive lines (when merging two fields into one progressive frame) is used to compare with this threshold. Increasing this threshold leads to be more conservative in detecting CAF.
15-4	Reserved	R	0h	Reserved
3	FMD_BED_ENABLE	R/W	0h	Film Mode Bad Edit Detection 0: Disable 1: Enable
2	FMD_JAM_DIR	R/W	0h	Film Mode Field Jamming Direction 0: Current field jammed with previous field 1: Current field jammed with next field
1	FMD_LOCK	R/W	0h	Lock Deinterlacer to film mode 0: Standard Deinterlacer Processing 1: Film Mode Deinterlacer Processing
0	FMD_ENABLE	R/W	0h	Enable film mode processing 0: Disable 1: Enable

1.3.5.12 dei_reg11 Register (offset = 2Ch) [reset = 00002004h]

dei_reg11 is shown in Figure 1-253 and described in Table 1-163.

FMD Control Register 0

Figure 1-253. dei_reg11 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-163. dei_reg11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	Reserved	R	0h	Reserved
19-0	FMD_CAF_THR	R/W	2004h	CAF threshold used for leaving film mode as part of bad edit detection (only used if fmd_bed_enable is active): If the combing artifacts is greater than this threshold, CAF is detected and thus the state machine will be forced to leave the film mode. If the user prefers to be more conservative in using film mode, decrease this threshold.

1.3.5.13 dei_reg12 Register (offset = 30h) [reset = 0h]

dei_reg12 is shown in Figure 1-254 and described in Table 1-164.

FMD Status Register 0

Figure 1-254. dei_reg12 Register

31	30	29	28	27	26	25	24
Reserved							FMD_RESET
R-0h							R-0h

23	22	21	20	19	18	17	16
Reserved			FMD_CAF				
R-0h			R-0h				

15	14	13	12	11	10	9	8
FMD_CAF							
R-0h							

7	6	5	4	3	2	1	0
FMD_CAF							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-164. dei_reg12 Register Field Descriptions

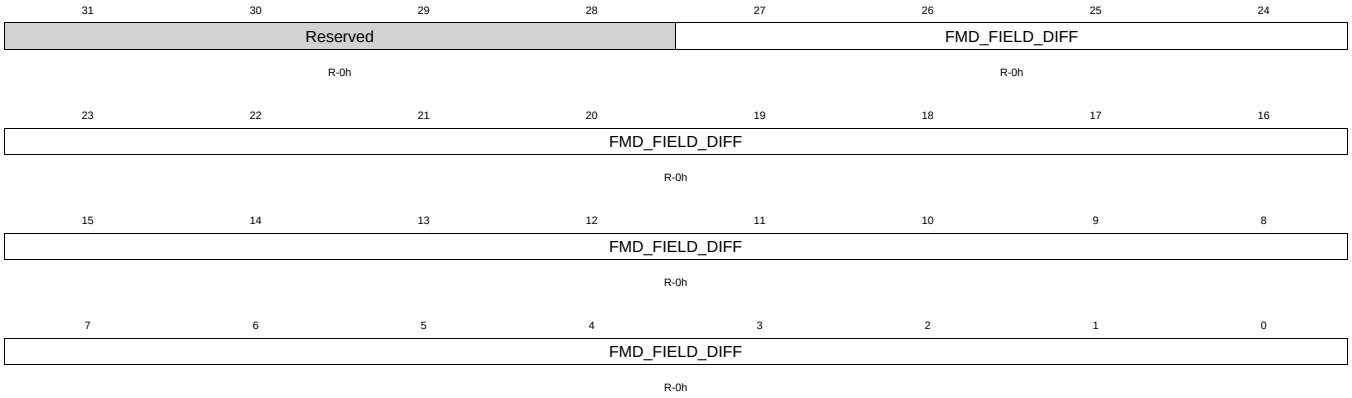
Bit	Field	Type	Reset	Description
31-25	Reserved	R	0h	Reserved
24	FMD_RESET	R	0h	When 1 , the film mode detection module needs to be reset by the software. This bit needs to be checked at each occurrence of the film mode detection interrupt. It will only be active in bad edit detection mode (fmd_bed_enable = 1) and the design is currently locked into film mode.
23-21	Reserved	R	0h	Reserved
20-0	FMD_CAF	R	0h	Detected combing artifacts

1.3.5.14 dei_reg13 Register (offset = 34h) [reset = 0h]

dei_reg13 is shown in Figure 1-255 and described in Table 1-165.

FMD Status Register 1

Figure 1-255. dei_reg13 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-165. dei_reg13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	Reserved
27-0	FMD_FIELD_DIFF	R	0h	Field difference (difference between two neighboring fields, one top and one bottom)

1.3.5.15 dei_reg14 Register (offset = 38h) [reset = 0h]

dei_reg14 is shown in Figure 1-256 and described in Table 1-166.

FMD Status Register 2

Figure 1-256. dei_reg14 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved				FMD_FRAME_DIFF			
R-0h				R-0h			

15	14	13	12	11	10	9	8
FMD_FRAME_DIFF							
R-0h							

7	6	5	4	3	2	1	0
FMD_FRAME_DIFF							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-166. dei_reg14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	Reserved	R	0h	Reserved
19-0	FMD_FRAME_DIFF	R	0h	Frame difference (difference between two top or two bottom fields)

1.3.6 GRPX Registers

The graphics module (GRPX) is configured using VPDMA frame and region descriptors. Please refer to Section 1.2.5 and Section 1.2.13.5.1.5 for instructions on how to configure the graphics module.

1.3.7 INTC_CLKC_CONTROL Registers

Table 1-167 lists the memory-mapped registers for the INTC_CLKC_CONTROL. All register offset addresses not listed in Table 1-167 should be considered as reserved locations and the register contents should not be modified.

Table 1-167. INTC_CLKC_CONTROL REGISTERS

Offset	Acronym	Register Name	Section
0h	pid	PID Register	Section 1.3.7.1
10h	sysconfig	SYS Config Register	Section 1.3.7.2
20h	intc_intr0_status_raw0	Interrupt0 Raw Register 0	Section 1.3.7.3
24h	intc_intr0_status_raw1	Interrupt0 Raw Register 1	Section 1.3.7.4
28h	intc_intr0_status_ena0	Interrupt0 Enabled Register 0	Section 1.3.7.5
2Ch	intc_intr0_status_ena1	Interrupt0 Enabled Register 1	Section 1.3.7.6
30h	intc_intr0_ena_set0	Interrupt0 Enable/Set Register 0	Section 1.3.7.7
34h	intc_intr0_ena_set1	Interrupt0 Enable/Set Register 1	Section 1.3.7.8
38h	intc_intr0_ena_clr0	Interrupt0 Enable/Clear Register 0	Section 1.3.7.9
3Ch	intc_intr0_ena_clr1	Interrupt0 Enable/Clear Register 1	Section 1.3.7.10
40h	intc_intr1_status_raw0	Interrupt1 Raw Register 0	Section 1.3.7.11
44h	intc_intr1_status_raw1	Interrupt1 Raw Register 1	Section 1.3.7.12
48h	intc_intr1_status_ena0	Interrupt1 Enabled Register 0	Section 1.3.7.13
4Ch	intc_intr1_status_ena1	Interrupt1 Enabled Register 1	Section 1.3.7.14
50h	intc_intr1_ena_set0	Interrupt1 Enable/Set Register 0	Section 1.3.7.15
54h	intc_intr1_ena_set1	Interrupt1 Enable/Set Register 1	Section 1.3.7.16
58h	intc_intr1_ena_clr0	Interrupt1 Enable/Clear Register 0	Section 1.3.7.17
5Ch	intc_intr1_ena_clr1	Interrupt1 Enable/Clear Register 1	Section 1.3.7.18
60h	intc_intr2_status_raw0	Interrupt2 Raw Register 0	Section 1.3.7.19
64h	intc_intr2_status_raw1	Interrupt2 Raw Register 1	Section 1.3.7.20
68h	intc_intr2_status_ena0	Interrupt2 Enabled Register 0	Section 1.3.7.21
6Ch	intc_intr2_status_ena1	Interrupt2 Enabled Register 1	Section 1.3.7.22
70h	intc_intr2_ena_set0	Interrupt2 Enable/Set Register 0	Section 1.3.7.23
74h	intc_intr2_ena_set1	Interrupt2 Enable/Set Register 1	Section 1.3.7.24
78h	intc_intr2_ena_clr0	Interrupt2 Enable/Clear Register 0	Section 1.3.7.25
7Ch	intc_intr2_ena_clr1	Interrupt2 Enable/Clear Register 1	Section 1.3.7.26
80h	intc_intr3_status_raw0	Interrupt3 Raw Register 0	Section 1.3.7.27
84h	intc_intr3_status_raw1	Interrupt3 Raw Register 0	Section 1.3.7.28
88h	intc_intr3_status_ena0	Interrupt3 Enabled Register 0	Section 1.3.7.29
8Ch	intc_intr3_status_ena1	Interrupt3 Enabled Register 1	Section 1.3.7.30
90h	intc_intr3_ena_set0	Interrupt3 Enable/Set Register 0	Section 1.3.7.31
94h	intc_intr3_ena_set1	Interrupt3 Enable/Set Register 1	Section 1.3.7.32
98h	intc_intr3_ena_clr0	Interrupt3 Enable/Clear Register 0	Section 1.3.7.33
9Ch	intc_intr3_ena_clr1	Interrupt3 Enable/Clear Register 1	Section 1.3.7.34
A0h	intc_eoi	End of Interrupt Register	Section 1.3.7.35
100h	clkc_clken	Clock Enable Register	Section 1.3.7.36
104h	clkc_rst	Soft Reset Register	Section 1.3.7.37
108h	clkc_dps	Main Datapath Select Register	Section 1.3.7.38
10Ch	clkc_vip1dps	VIP1 Datapath Select Register	Section 1.3.7.39
110h	clkc_vip2dps	VIP2 Datapath Select Register	Section 1.3.7.40
114h	clkc_venc_clksel	VENC Clock Select Register	Section 1.3.7.41
118h	clkc_venc_ena	VENC Enable Register	Section 1.3.7.42
11Ch	clkc_range_map	VC1 Range Map Register	Section 1.3.7.43

Table 1-167. INTC_CLKC_CONTROL REGISTERS (continued)

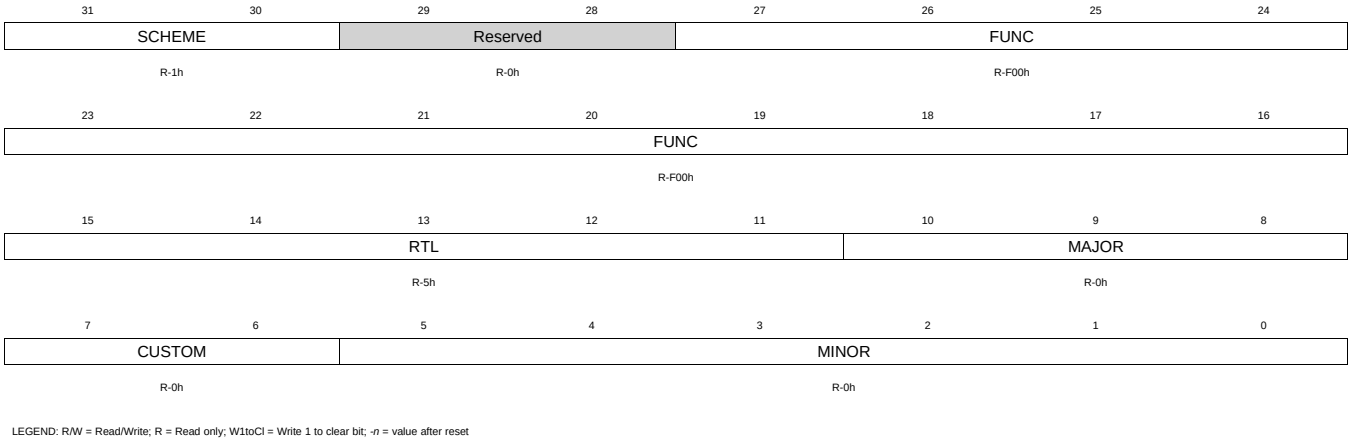
Offset	Acronym	Register Name	Section
120h	clkc_underflow	VENC Underflow Status Register	Section 1.3.7.44

1.3.7.1 pid Register (offset = 0h) [reset = 4F002800h]

pid is shown in Figure 1-257 and described in Table 1-168.

PID Register

Figure 1-257. pid Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-168. pid Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	The scheme of the register used. This indicates the PDR3.5 Method
29-28	Reserved	R	0h	
27-16	FUNC	R	F00h	The function of the module being used
15-11	RTL	R	5h	RTL Release Version The PDR release number of this IP
10-8	MAJOR	R	0h	Major Release Number
7-6	CUSTOM	R	0h	Custom IP
5-0	MINOR	R	0h	Minor Release Number

1.3.7.2 sysconfig Register (offset = 10h) [reset = 28h]

sysconfig is shown in Figure 1-258 and described in Table 1-169.

SYS Config Register

Figure 1-258. sysconfig Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved		STANDBYMODE		IDLEMODE		Reserved	
R-0h		R/W-2h		R/W-2h		R-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-169. sysconfig Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	Reserved	R	0h	
5-4	STANDBYMODE	R/W	2h	Standymode setting for PWRSTNDBY IPGeneric
3-2	IDLEMODE	R/W	2h	Idlemode setting for PWRIDLE IPGenerc
1-0	Reserved	R	0h	

1.3.7.3 intc_intr0_status_raw0 Register (offset = 20h) [reset = 0h]

intc_intr0_status_raw0 is shown in Figure 1-259 and described in Table 1-170.

Interrupt0 Raw Register 0

Figure 1-259. intc_intr0_status_raw0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_RAW	DVO2_INT2_RAW	DVO2_INT1_RAW	DVO2_INT0_RAW	Reserved			DVO1_INT2_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_RAW	DVO1_INT0_RAW	VIP2_PARSER_INT_RAW	VIP1_PARSER_INT_RAW	Reserved	DEI_FMD_INT_RAW	Reserved	VPDMA_INT0_DESCRIPTOR_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT0_LIST7_NOTIFY_RAW	VPDMA_INT0_LIST7_COMPLETE_RAW	VPDMA_INT0_LIST6_NOTIFY_RAW	VPDMA_INT0_LIST6_COMPLETE_RAW	VPDMA_INT0_LIST5_NOTIFY_RAW	VPDMA_INT0_LIST5_COMPLETE_RAW	VPDMA_INT0_LIST4_NOTIFY_RAW	VPDMA_INT0_LIST4_COMPLETE_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT0_LIST3_NOTIFY_RAW	VPDMA_INT0_LIST3_COMPLETE_RAW	VPDMA_INT0_LIST2_NOTIFY_RAW	VPDMA_INT0_LIST2_COMPLETE_RAW	VPDMA_INT0_LIST1_NOTIFY_RAW	VPDMA_INT0_LIST1_COMPLETE_RAW	VPDMA_INT0_LIST0_NOTIFY_RAW	VPDMA_INT0_LIST0_COMPLETE_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-170. intc_intr0_status_raw0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_RAW	R/W	0h	SD VENC Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
30	DVO2_INT2_RAW	R/W	0h	DVO2 Interrupt2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
29	DVO2_INT1_RAW	R/W	0h	DVO2 Interrupt1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
28	DVO2_INT0_RAW	R/W	0h	DVO2 Interrupt0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_RAW	R/W	0h	DVO1 Interrupt2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
23	DVO1_INT1_RAW	R/W	0h	DVO1 Interrupt1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
22	DVO1_INT0_RAW	R/W	0h	DVO1 Interrupt0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
21	VIP2_PARSER_INT_RAW	R/W	0h	VIP2 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
20	VIP1_PARSER_INT_RAW	R/W	0h	VIP1 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_RAW	R/W	0h	DEI Film Mode Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
17	Reserved	R	0h	
16	VPDMA_INT0_DESCRIPTOR_RAW	R/W	0h	VPDMA INT0 Descriptor Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
15	VPDMA_INT0_LIST7_NOTIFY_RAW	R/W	0h	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
14	VPDMA_INT0_LIST7_COMPLETE_RAW	R/W	0h	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

Table 1-170. intc_intr0_status_raw0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	VPDMA_INT0_LIST6_NOTIFY_RAW	R/W	0h	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
12	VPDMA_INT0_LIST6_COMPLETE_RAW	R/W	0h	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
11	VPDMA_INT0_LIST5_NOTIFY_RAW	R/W	0h	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
10	VPDMA_INT0_LIST5_COMPLETE_RAW	R/W	0h	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
9	VPDMA_INT0_LIST4_NOTIFY_RAW	R/W	0h	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
8	VPDMA_INT0_LIST4_COMPLETE_RAW	R/W	0h	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
7	VPDMA_INT0_LIST3_NOTIFY_RAW	R/W	0h	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
6	VPDMA_INT0_LIST3_COMPLETE_RAW	R/W	0h	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT0_LIST2_NOTIFY_RAW	R/W	0h	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT0_LIST2_COMPLETE_RAW	R/W	0h	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT0_LIST1_NOTIFY_RAW	R/W	0h	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT0_LIST1_COMPLETE_RAW	R/W	0h	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT0_LIST0_NOTIFY_RAW	R/W	0h	VPDMA INT0 List0 Notify Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT0_LIST0_COMPLETE_RAW	R/W	0h	VPDMA INT0 List0 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.4 intc_intr0_status_raw1 Register (offset = 24h) [reset = 0h]

intc_intr0_status_raw1 is shown in Figure 1-260 and described in Table 1-171.

Interrupt0 Raw Register 1

Figure 1-260. intc_intr0_status_raw1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_RAW	VIP2_CHR_DS_1_UV_ERR_INT_RAW
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_RAW	VIP1_CHR_DS_1_UV_ERR_INT_RAW	NF_CHR_DS_UV_ERR_INT_RAW	COMP_ERR_INT_RAW	GRPX3_INT_RAW	GRPX2_INT_RAW	GRPX1_INT_RAW	DEI_ERROR_INT_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT0_CLIENT_RAW	VPDMA_INT0_CHANNEL_GROUP6_RAW	VPDMA_INT0_CHANNEL_GROUP5_RAW	VPDMA_INT0_CHANNEL_GROUP4_RAW	VPDMA_INT0_CHANNEL_GROUP3_RAW	VPDMA_INT0_CHANNEL_GROUP2_RAW	VPDMA_INT0_CHANNEL_GROUP1_RAW	VPDMA_INT0_CHANNEL_GROUP0_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-171. intc_intr0_status_raw1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_RAW	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_RAW	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_RAW	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_RAW	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_RAW	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
20	COMP_ERR_INT_RAW	R/W	0h	COMP Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
19	GRPX3_INT_RAW	R/W	0h	GRPX3 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
18	GRPX2_INT_RAW	R/W	0h	GRPX2 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
17	GRPX1_INT_RAW	R/W	0h	GRPX1 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
16	DEI_ERROR_INT_RAW	R/W	0h	DEI Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
15-8	Reserved	R	0h	
7	VPDMA_INT0_CLIENT_RAW	R/W	0h	VPDMA INT0 Client Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

Table 1-171. intc_intr0_status_raw1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	VPDMA_INT0_CHANNEL_GROUP6_RAW	R/W	0h	VPDMA INT0 Channel Group6 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT0_CHANNEL_GROUP5_RAW	R/W	0h	VPDMA INT0 Channel Group5 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT0_CHANNEL_GROUP4_RAW	R/W	0h	VPDMA INT0 Channel Group4 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT0_CHANNEL_GROUP3_RAW	R/W	0h	VPDMA INT0 Channel Group3 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT0_CHANNEL_GROUP2_RAW	R/W	0h	VPDMA INT0 Channel Group2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT0_CHANNEL_GROUP1_RAW	R/W	0h	VPDMA INT0 Channel Group1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT0_CHANNEL_GROUP0_RAW	R/W	0h	VPDMA INT0 Channel Group0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.5 intc_intr0_status_ena0 Register (offset = 28h) [reset = 0h]

intc_intr0_status_ena0 is shown in Figure 1-261 and described in Table 1-172.

Interrupt0 Enabled Register 0

Figure 1-261. intc_intr0_status_ena0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA	DVO2_INT2_ENA	DVO2_INT1_ENA	DVO2_INT0_ENA	Reserved			DVO1_INT2_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA	DVO1_INT0_ENA	VIP2_PARSER_INT_ENA	VIP1_PARSER_INT_ENA	Reserved	DEI_FMD_INT_ENA	Reserved	VPDMA_INT0_DESCRIPTOR_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT0_LIST7_NOTIFY_ENA	VPDMA_INT0_LIST7_COMPLETE_ENA	VPDMA_INT0_LIST6_NOTIFY_ENA	VPDMA_INT0_LIST6_COMPLETE_ENA	VPDMA_INT0_LIST5_NOTIFY_ENA	VPDMA_INT0_LIST5_COMPLETE_ENA	VPDMA_INT0_LIST4_NOTIFY_ENA	VPDMA_INT0_LIST4_COMPLETE_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT0_LIST3_NOTIFY_ENA	VPDMA_INT0_LIST3_COMPLETE_ENA	VPDMA_INT0_LIST2_NOTIFY_ENA	VPDMA_INT0_LIST2_COMPLETE_ENA	VPDMA_INT0_LIST1_NOTIFY_ENA	VPDMA_INT0_LIST1_COMPLETE_ENA	VPDMA_INT0_LIST0_NOTIFY_ENA	VPDMA_INT0_LIST0_COMPLETE_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-172. intc_intr0_status_ena0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA	R/W	0h	SD_VENC Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
30	DVO2_INT2_ENA	R/W	0h	DVO2 Enabled Interrupt2 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
29	DVO2_INT1_ENA	R/W	0h	DVO2 Enabled Interrupt1 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
28	DVO2_INT0_ENA	R/W	0h	DVO2 Enabled Interrupt0 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA	R/W	0h	DVO1 Enabled Interrupt2 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
23	DVO1_INT1_ENA	R/W	0h	DVO1 Enabled Interrupt1 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
22	DVO1_INT0_ENA	R/W	0h	DVO1 Enabled Interrupt0 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
21	VIP2_PARSER_INT_ENA	R/W	0h	VIP2 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
20	VIP1_PARSER_INT_ENA	R/W	0h	VIP1 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
19	Reserved	R	0h	

Table 1-172. intc_intr0_status_ena0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	DEI_FMD_INT_ENA	R/W	0h	DEI Film Mode Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	
16	VPDMA_INT0_DESCRIPTOR_ENA	R/W	0h	VPDMA INT0 Descriptor Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15	VPDMA_INT0_LIST7_NOTIFY_ENA	R/W	0h	VPDMA INT0 List7 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
14	VPDMA_INT0_LIST7_COMPLETE_ENA	R/W	0h	VPDMA INT0 List7 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
13	VPDMA_INT0_LIST6_NOTIFY_ENA	R/W	0h	VPDMA INT0 List6 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
12	VPDMA_INT0_LIST6_COMPLETE_ENA	R/W	0h	VPDMA INT0 List6 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
11	VPDMA_INT0_LIST5_NOTIFY_ENA	R/W	0h	VPDMA INT0 List5 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
10	VPDMA_INT0_LIST5_COMPLETE_ENA	R/W	0h	VPDMA INT0 List5 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
9	VPDMA_INT0_LIST4_NOTIFY_ENA	R/W	0h	VPDMA INT0 List4 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
8	VPDMA_INT0_LIST4_COMPLETE_ENA	R/W	0h	VPDMA INT0 List4 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
7	VPDMA_INT0_LIST3_NOTIFY_ENA	R/W	0h	VPDMA INT0 List3 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
6	VPDMA_INT0_LIST3_COMPLETE_ENA	R/W	0h	VPDMA INT0 List3 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT0_LIST2_NOTIFY_ENA	R/W	0h	VPDMA INT0 List2 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT0_LIST2_COMPLETE_ENA	R/W	0h	VPDMA INT0 List2 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT0_LIST1_NOTIFY_ENA	R/W	0h	VPDMA INT0 List1 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT0_LIST1_COMPLETE_ENA	R/W	0h	VPDMA INT0 List1 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT0_LIST0_NOTIFY_ENA	R/W	0h	VPDMA INT0 List0 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT0_LIST0_COMPLETE_ENA	R/W	0h	VPDMA INT0 List0 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.6 intc_intr0_status_ena1 Register (offset = 2Ch) [reset = 0h]

intc_intr0_status_ena1 is shown in Figure 1-262 and described in Table 1-173.

Interrupt0 Enabled Register 1

Figure 1-262. intc_intr0_status_ena1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA	VIP2_CHR_DS_1_UV_ERR_INT_ENA
R-0h						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA	VIP1_CHR_DS_1_UV_ERR_INT_ENA	NF_CHR_DS_UV_ERR_INT_ENA	COMP_ERR_INT_ENA	GRPX3_INT_ENA	GRPX2_INT_ENA	GRPX1_INT_ENA	DEI_ERROR_INT_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
VPDMA_INT0_CLIENT_ENA	VPDMA_INT0_CHANNEL_GROUP6_ENA	VPDMA_INT0_CHANNEL_GROUP5_ENA	VPDMA_INT0_CHANNEL_GROUP4_ENA	VPDMA_INT0_CHANNEL_GROUP3_ENA	VPDMA_INT0_CHANNEL_GROUP2_ENA	VPDMA_INT0_CHANNEL_GROUP1_ENA	VPDMA_INT0_CHANNEL_GROUP0_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-173. intc_intr0_status_ena1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
20	COMP_ERR_INT_ENA	R/W	0h	COMP Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
19	GRPX3_INT_ENA	R/W	0h	GRPX3 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
18	GRPX2_INT_ENA	R/W	0h	GRPX2 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
17	GRPX1_INT_ENA	R/W	0h	GRPX1 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
16	DEI_ERROR_INT_ENA	R/W	0h	DEI Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect

Table 1-173. intc_intr0_status_ena1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	
7	VPDMA_INT0_CLIENT_ENA	R/W	0h	VPDMA INT0 Client Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
6	VPDMA_INT0_CHANNEL_GROUP6_ENA	R/W	0h	VPDMA INT0 Channel Group6 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT0_CHANNEL_GROUP5_ENA	R/W	0h	VPDMA INT0 Channel Group5 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT0_CHANNEL_GROUP4_ENA	R/W	0h	VPDMA INT0 Channel Group4 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT0_CHANNEL_GROUP3_ENA	R/W	0h	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT0_CHANNEL_GROUP2_ENA	R/W	0h	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT0_CHANNEL_GROUP1_ENA	R/W	0h	VPDMA INT0 Channel Group1 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT0_CHANNEL_GROUP0_ENA	R/W	0h	VPDMA INT0 Channel Group0 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.7 intc_intr0_ena_set0 Register (offset = 30h) [reset = 0h]

intc_intr0_ena_set0 is shown in Figure 1-263 and described in Table 1-174.

Interrupt0 Enable/Set Register 0

Figure 1-263. intc_intr0_ena_set0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA_SET	DVO2_INT2_ENA_SET	DVO2_INT1_ENA_SET	DVO2_INT0_ENA_SET	Reserved			DVO1_INT2_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA_SET	DVO1_INT0_ENA_SET	VIP2_PARSER_INT_ENA_SET	VIP1_PARSER_INT_ENA_SET	Reserved	DEI_FMD_INT_ENA_SET	Reserved	VPDMA_INT0_DESCRIPTOR_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT0_LIST7_NOTIFY_ENA_SET	VPDMA_INT0_LIST7_COMPLETE_ENA_SET	VPDMA_INT0_LIST6_NOTIFY_ENA_SET	VPDMA_INT0_LIST6_COMPLETE_ENA_SET	VPDMA_INT0_LIST5_NOTIFY_ENA_SET	VPDMA_INT0_LIST5_COMPLETE_ENA_SET	VPDMA_INT0_LIST4_NOTIFY_ENA_SET	VPDMA_INT0_LIST4_COMPLETE_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT0_LIST3_NOTIFY_ENA_SET	VPDMA_INT0_LIST3_COMPLETE_ENA_SET	VPDMA_INT0_LIST2_NOTIFY_ENA_SET	VPDMA_INT0_LIST2_COMPLETE_ENA_SET	VPDMA_INT0_LIST1_NOTIFY_ENA_SET	VPDMA_INT0_LIST1_COMPLETE_ENA_SET	VPDMA_INT0_LIST0_NOTIFY_ENA_SET	VPDMA_INT0_LIST0_COMPLETE_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-174. intc_intr0_ena_set0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA_SET	R/W	0h	SD_VENC Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
30	DVO2_INT2_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
29	DVO2_INT1_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
28	DVO2_INT0_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
23	DVO1_INT1_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
22	DVO1_INT0_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
21	VIP2_PARSER_INT_ENA_SET	R/W	0h	VIP2 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
20	VIP1_PARSER_INT_ENA_SET	R/W	0h	VIP1 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_ENA_SET	R/W	0h	DEI Film Mode Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	

Table 1-174. intc_intr0_ena_set0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VPDMA_INT0_DESCRIPTOR_ENA_SET	R/W	0h	VPDMA INT0 Descriptor Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15	VPDMA_INT0_LIST7_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List7 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
14	VPDMA_INT0_LIST7_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List7 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
13	VPDMA_INT0_LIST6_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List6 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
12	VPDMA_INT0_LIST6_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List6 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
11	VPDMA_INT0_LIST5_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List5 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
10	VPDMA_INT0_LIST5_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List5 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
9	VPDMA_INT0_LIST4_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List4 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
8	VPDMA_INT0_LIST4_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List4 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
7	VPDMA_INT0_LIST3_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List3 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
6	VPDMA_INT0_LIST3_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List3 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT0_LIST2_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List2 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT0_LIST2_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List2 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT0_LIST1_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List1 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT0_LIST1_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List1 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT0_LIST0_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List0 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT0_LIST0_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List0 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.8 intc_intr0_ena_set1 Register (offset = 34h) [reset = 0h]

intc_intr0_ena_set1 is shown in Figure 1-264 and described in Table 1-175.

Interrupt0 Enable/Set Register 1

Figure 1-264. intc_intr0_ena_set1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	NF_CHR_DS_UV_ERR_INT_ENA_SET	COMP_ERR_INT_ENA_SET	GRPX3_INT_ENA_SET	GRPX2_INT_ENA_SET	GRPX1_INT_ENA_SET	DEI_ERROR_INT_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT0_CLIENT_ENA_SET	VPDMA_INT0_CHANNEL_GROUP6_ENA_SET	VPDMA_INT0_CHANNEL_GROUP5_ENA_SET	VPDMA_INT0_CHANNEL_GROUP4_ENA_SET	VPDMA_INT0_CHANNEL_GROUP3_ENA_SET	VPDMA_INT0_CHANNEL_GROUP2_ENA_SET	VPDMA_INT0_CHANNEL_GROUP1_ENA_SET	VPDMA_INT0_CHANNEL_GROUP0_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-175. intc_intr0_ena_set1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA_SET	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
20	COMP_ERR_INT_ENA_SET	R/W	0h	COMP Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
19	GRPX3_INT_ENA_SET	R/W	0h	GRPX3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
18	GRPX2_INT_ENA_SET	R/W	0h	GRPX2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	GRPX1_INT_ENA_SET	R/W	0h	GRPX1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
16	DEI_ERROR_INT_ENA_SET	R/W	0h	DEI Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15-8	Reserved	R	0h	
7	VPDMA_INT0_CLIENT_ENA_SET	R/W	0h	VPDMA INT0 Client Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

Table 1-175. intc_intr0_ena_set1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	VPDMA_INT0_CHANNEL_GROUP6_ENA_SET	R/W	0h	VPDMA INT0 Channel Group6 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT0_CHANNEL_GROUP5_ENA_SET	R/W	0h	VPDMA INT0 Channel Group5 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT0_CHANNEL_GROUP4_ENA_SET	R/W	0h	VPDMA INT0 Channel Group4 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT0_CHANNEL_GROUP3_ENA_SET	R/W	0h	VPDMA INT0 Channel Group3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT0_CHANNEL_GROUP2_ENA_SET	R/W	0h	VPDMA INT0 Channel Group2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT0_CHANNEL_GROUP1_ENA_SET	R/W	0h	VPDMA INT0 Channel Group1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT0_CHANNEL_GROUP0_ENA_SET	R/W	0h	VPDMA INT0 Channel Group0 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.9 intc_intr0_ena_clr0 Register (offset = 38h) [reset = 0h]

intc_intr0_ena_clr0 is shown in Figure 1-265 and described in Table 1-176.

Interrupt0 Enable/Clear Register 0

Figure 1-265. intc_intr0_ena_clr0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA_CLR	DVO2_INT2_ENA_CLR	DVO2_INT1_ENA_CLR	DVO2_INT0_ENA_CLR	Reserved			DVO1_INT2_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA_CLR	DVO1_INT0_ENA_CLR	VIP2_PARSER_INT_ENA_CLR	VIP1_PARSER_INT_ENA_CLR	Reserved	DEI_FMD_INT_ENA_CLR	Reserved	VPDMA_INT0_DESCRIPTOR_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT0_LIST7_NOTIFY_ENA_CLR	VPDMA_INT0_LIST7_COMPLETE_ENA_CLR	VPDMA_INT0_LIST6_NOTIFY_ENA_CLR	VPDMA_INT0_LIST6_COMPLETE_ENA_CLR	VPDMA_INT0_LIST5_NOTIFY_ENA_CLR	VPDMA_INT0_LIST5_COMPLETE_ENA_CLR	VPDMA_INT0_LIST4_NOTIFY_ENA_CLR	VPDMA_INT0_LIST4_COMPLETE_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT0_LIST3_NOTIFY_ENA_CLR	VPDMA_INT0_LIST3_COMPLETE_ENA_CLR	VPDMA_INT0_LIST2_NOTIFY_ENA_CLR	VPDMA_INT0_LIST2_COMPLETE_ENA_CLR	VPDMA_INT0_LIST1_NOTIFY_ENA_CLR	VPDMA_INT0_LIST1_COMPLETE_ENA_CLR	VPDMA_INT0_LIST0_NOTIFY_ENA_CLR	VPDMA_INT0_LIST0_COMPLETE_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-176. intc_intr0_ena_clr0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA_CLR	R/W	0h	SD_VENC Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
30	DVO2_INT2_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
29	DVO2_INT1_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
28	DVO2_INT0_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
23	DVO1_INT1_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
22	DVO1_INT0_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
21	VIP2_PARSER_INT_ENA_CLR	R/W	0h	VIP2 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
20	VIP1_PARSER_INT_ENA_CLR	R/W	0h	VIP1 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_ENA_CLR	R/W	0h	DEI Film Mode Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	

Table 1-176. intc_intr0_ena_clr0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VPDMA_INT0_DESCRIPTOR_ENA_CLR	R/W	0h	VPDMA INT0 Descriptor Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
15	VPDMA_INT0_LIST7_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List7 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
14	VPDMA_INT0_LIST7_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List7 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
13	VPDMA_INT0_LIST6_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List6 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
12	VPDMA_INT0_LIST6_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List6 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
11	VPDMA_INT0_LIST5_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List5 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
10	VPDMA_INT0_LIST5_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List5 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
9	VPDMA_INT0_LIST4_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List4 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
8	VPDMA_INT0_LIST4_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List4 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
7	VPDMA_INT0_LIST3_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List3 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
6	VPDMA_INT0_LIST3_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List3 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
5	VPDMA_INT0_LIST2_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List2 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
4	VPDMA_INT0_LIST2_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List2 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
3	VPDMA_INT0_LIST1_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List1 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
2	VPDMA_INT0_LIST1_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List1 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
1	VPDMA_INT0_LIST0_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List0 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
0	VPDMA_INT0_LIST0_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List0 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

1.3.7.10 intc_intr0_ena_clr1 Register (offset = 3Ch) [reset = 0h]

intc_intr0_ena_clr1 is shown in Figure 1-266 and described in Table 1-177.

Interrupt0 Enable/Clear Register 1

Figure 1-266. intc_intr0_ena_clr1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	NF_CHR_DS_UV_ERR_INT_ENA_CLR	COMP_ERR_INT_ENA_CLR	GRPX3_INT_ENA_CLR	GRPX2_INT_ENA_CLR	GRPX1_INT_ENA_CLR	DEI_ERROR_INT_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT0_CLIENT_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP6_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP5_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP4_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP3_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP2_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP1_ENA_CLR	VPDMA_INT0_CHANNEL_GROUP0_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-177. intc_intr0_ena_clr1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA_CLR	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
20	COMP_ERR_INT_ENA_CLR	R/W	0h	COMP Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
19	GRPX3_INT_ENA_CLR	R/W	0h	GRPX3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
18	GRPX2_INT_ENA_CLR	R/W	0h	GRPX2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
17	GRPX1_INT_ENA_CLR	R/W	0h	GRPX1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
16	DEI_ERROR_INT_ENA_CLR	R/W	0h	DEI Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

Table 1-177. intc_intr0_ena_clr1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	
7	VPDMA_INT0_CLIENT_ENA_CLR	R/W	0h	VPDMA INT0 Client Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
6	VPDMA_INT0_CHANNEL_GROUP6_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group6 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
5	VPDMA_INT0_CHANNEL_GROUP5_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group5 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
4	VPDMA_INT0_CHANNEL_GROUP4_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group4 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
3	VPDMA_INT0_CHANNEL_GROUP3_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
2	VPDMA_INT0_CHANNEL_GROUP2_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
1	VPDMA_INT0_CHANNEL_GROUP1_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
0	VPDMA_INT0_CHANNEL_GROUP0_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group0 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

1.3.7.11 intc_intr1_status_raw0 Register (offset = 40h) [reset = 0h]

intc_intr1_status_raw0 is shown in Figure 1-267 and described in Table 1-178.

Interrupt1 Raw Register 0

Figure 1-267. intc_intr1_status_raw0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_RAW	DVO2_INT2_RAW	DVO2_INT1_RAW	DVO2_INT0_RAW	Reserved			DVO1_INT2_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_RAW	DVO1_INT0_RAW	VIP2_PARSER_INT_RAW	VIP1_PARSER_INT_RAW	Reserved	DEI_FMD_INT_RAW	Reserved	VPDMA_INT1_DESCRIPTOR_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT1_LIST7_NOTIFY_RAW	VPDMA_INT1_LIST7_COMPLETE_RAW	VPDMA_INT1_LIST6_NOTIFY_RAW	VPDMA_INT1_LIST6_COMPLETE_RAW	VPDMA_INT1_LIST5_NOTIFY_RAW	VPDMA_INT1_LIST5_COMPLETE_RAW	VPDMA_INT1_LIST4_NOTIFY_RAW	VPDMA_INT1_LIST4_COMPLETE_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT1_LIST3_NOTIFY_RAW	VPDMA_INT1_LIST3_COMPLETE_RAW	VPDMA_INT1_LIST2_NOTIFY_RAW	VPDMA_INT1_LIST2_COMPLETE_RAW	VPDMA_INT1_LIST1_NOTIFY_RAW	VPDMA_INT1_LIST1_COMPLETE_RAW	VPDMA_INT1_LIST0_NOTIFY_RAW	VPDMA_INT1_LIST0_COMPLETE_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-178. intc_intr1_status_raw0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_RAW	R/W	0h	SD VENC Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
30	DVO2_INT2_RAW	R/W	0h	DVO2 Interrupt2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
29	DVO2_INT1_RAW	R/W	0h	DVO2 Interrupt1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
28	DVO2_INT0_RAW	R/W	0h	DVO2 Interrupt0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_RAW	R/W	0h	DVO1 Interrupt2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
23	DVO1_INT1_RAW	R/W	0h	DVO1 Interrupt1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
22	DVO1_INT0_RAW	R/W	0h	DVO1 Interrupt0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
21	VIP2_PARSER_INT_RAW	R/W	0h	VIP2 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
20	VIP1_PARSER_INT_RAW	R/W	0h	VIP1 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_RAW	R/W	0h	DEI Film Mode Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
17	Reserved	R	0h	
16	VPDMA_INT1_DESCRIPTOR_RAW	R/W	0h	VPDMA INT0 Descriptor Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
15	VPDMA_INT1_LIST7_NOTIFY_RAW	R/W	0h	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
14	VPDMA_INT1_LIST7_COMPLETE_RAW	R/W	0h	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

Table 1-178. intc_intr1_status_raw0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	VPDMA_INT1_LIST6_NOTIFY_RAW	R/W	0h	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
12	VPDMA_INT1_LIST6_COMPLETE_RAW	R/W	0h	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
11	VPDMA_INT1_LIST5_NOTIFY_RAW	R/W	0h	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
10	VPDMA_INT1_LIST5_COMPLETE_RAW	R/W	0h	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
9	VPDMA_INT1_LIST4_NOTIFY_RAW	R/W	0h	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
8	VPDMA_INT1_LIST4_COMPLETE_RAW	R/W	0h	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
7	VPDMA_INT1_LIST3_NOTIFY_RAW	R/W	0h	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
6	VPDMA_INT1_LIST3_COMPLETE_RAW	R/W	0h	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT1_LIST2_NOTIFY_RAW	R/W	0h	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT1_LIST2_COMPLETE_RAW	R/W	0h	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT1_LIST1_NOTIFY_RAW	R/W	0h	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT1_LIST1_COMPLETE_RAW	R/W	0h	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT1_LIST0_NOTIFY_RAW	R/W	0h	VPDMA INT0 List0 Notify Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT1_LIST0_COMPLETE_RAW	R/W	0h	VPDMA INT0 List0 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.12 intc_intr1_status_raw1 Register (offset = 44h) [reset = 0h]

intc_intr1_status_raw1 is shown in Figure 1-268 and described in Table 1-179.

Interrupt1 Raw Register 1

Figure 1-268. intc_intr1_status_raw1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_RAW	VIP2_CHR_DS_1_UV_ERR_INT_RAW
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_RAW	VIP1_CHR_DS_1_UV_ERR_INT_RAW	NF_CHR_DS_UV_ERR_INT_RAW	COMP_ERR_INT_RAW	GRPX3_INT_RAW	GRPX2_INT_RAW	GRPX1_INT_RAW	DEI_ERROR_INT_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT1_CLIENT_RAW	VPDMA_INT1_CHANNEL_GROUP6_RAW	VPDMA_INT1_CHANNEL_GROUP5_RAW	VPDMA_INT1_CHANNEL_GROUP4_RAW	VPDMA_INT1_CHANNEL_GROUP3_RAW	VPDMA_INT1_CHANNEL_GROUP2_RAW	VPDMA_INT1_CHANNEL_GROUP1_RAW	VPDMA_INT1_CHANNEL_GROUP0_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-179. intc_intr1_status_raw1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_RAW	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_RAW	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_RAW	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_RAW	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_RAW	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
20	COMP_ERR_INT_RAW	R/W	0h	COMP Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
19	GRPX3_INT_RAW	R/W	0h	GRPX3 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
18	GRPX2_INT_RAW	R/W	0h	GRPX2 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
17	GRPX1_INT_RAW	R/W	0h	GRPX1 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
16	DEI_ERROR_INT_RAW	R/W	0h	DEI Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
15-8	Reserved	R	0h	
7	VPDMA_INT1_CLIENT_RAW	R/W	0h	VPDMA INT0 Client Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

Table 1-179. intc_intr1_status_raw1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	VPDMA_INT1_CHANNEL_GROUP6_RAW	R/W	0h	VPDMA INT0 Channel Group6 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT1_CHANNEL_GROUP5_RAW	R/W	0h	VPDMA INT0 Channel Group5 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT1_CHANNEL_GROUP4_RAW	R/W	0h	VPDMA INT0 Channel Group4 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT1_CHANNEL_GROUP3_RAW	R/W	0h	VPDMA INT0 Channel Group3 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT1_CHANNEL_GROUP2_RAW	R/W	0h	VPDMA INT0 Channel Group2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT1_CHANNEL_GROUP1_RAW	R/W	0h	VPDMA INT0 Channel Group1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT1_CHANNEL_GROUP0_RAW	R/W	0h	VPDMA INT0 Channel Group0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.13 intc_intr1_status_ena0 Register (offset = 48h) [reset = 0h]

intc_intr1_status_ena0 is shown in Figure 1-269 and described in Table 1-180.

Interrupt1 Enabled Register 0

Figure 1-269. intc_intr1_status_ena0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA	DVO2_INT2_ENA	DVO2_INT1_ENA	DVO2_INT0_ENA	Reserved			DVO1_INT2_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA	DVO1_INT0_ENA	VIP2_PARSER_INT_ENA	VIP1_PARSER_INT_ENA	Reserved	DEI_FMD_INT_ENA	Reserved	VPDMA_INT1_DESCRIPTOR_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT1_LIST7_NOTIFY_ENA	VPDMA_INT1_LIST7_COMPLETE_ENA	VPDMA_INT1_LIST6_NOTIFY_ENA	VPDMA_INT1_LIST6_COMPLETE_ENA	VPDMA_INT1_LIST5_NOTIFY_ENA	VPDMA_INT1_LIST5_COMPLETE_ENA	VPDMA_INT1_LIST4_NOTIFY_ENA	VPDMA_INT1_LIST4_COMPLETE_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT1_LIST3_NOTIFY_ENA	VPDMA_INT1_LIST3_COMPLETE_ENA	VPDMA_INT1_LIST2_NOTIFY_ENA	VPDMA_INT1_LIST2_COMPLETE_ENA	VPDMA_INT1_LIST1_NOTIFY_ENA	VPDMA_INT1_LIST1_COMPLETE_ENA	VPDMA_INT1_LIST0_NOTIFY_ENA	VPDMA_INT1_LIST0_COMPLETE_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-180. intc_intr1_status_ena0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA	R/W	0h	SD_VENC Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
30	DVO2_INT2_ENA	R/W	0h	DVO2 Enabled Interrupt2 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
29	DVO2_INT1_ENA	R/W	0h	DVO2 Enabled Interrupt1 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
28	DVO2_INT0_ENA	R/W	0h	DVO2 Enabled Interrupt0 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA	R/W	0h	DVO1 Enabled Interrupt2 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
23	DVO1_INT1_ENA	R/W	0h	DVO1 Enabled Interrupt1 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
22	DVO1_INT0_ENA	R/W	0h	DVO1 Enabled Interrupt0 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
21	VIP2_PARSER_INT_ENA	R/W	0h	VIP2 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
20	VIP1_PARSER_INT_ENA	R/W	0h	VIP1 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
19	Reserved	R	0h	

Table 1-180. intc_intr1_status_ena0 Register Field Descriptions (continued)

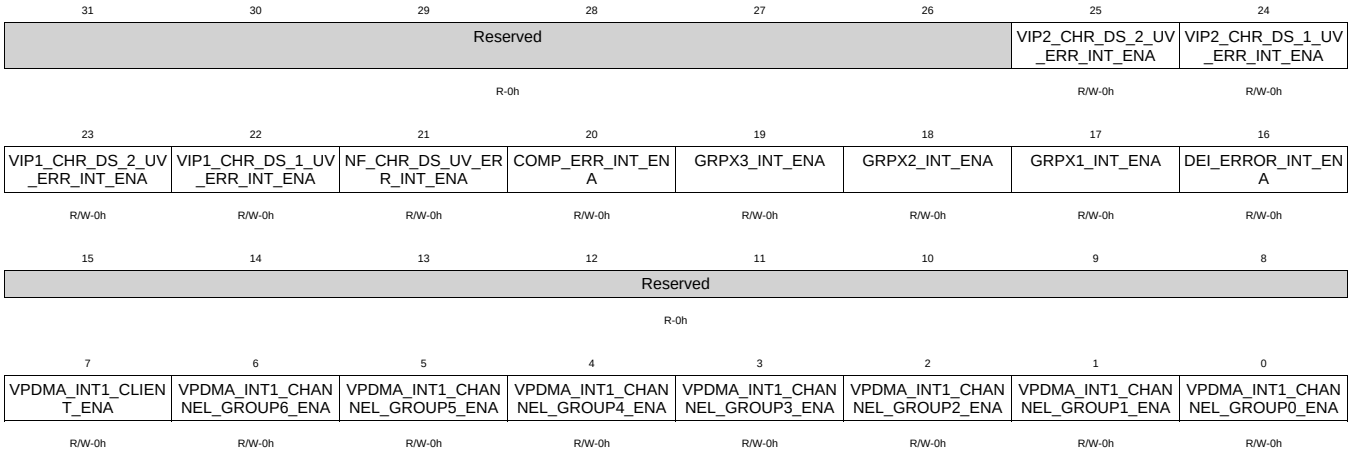
Bit	Field	Type	Reset	Description
18	DEI_FMD_INT_ENA	R/W	0h	DEI Film Mode Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	
16	VPDMA_INT1_DESCRIPTOR_ENA	R/W	0h	VPDMA INT0 Descriptor Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15	VPDMA_INT1_LIST7_NOTIFY_ENA	R/W	0h	VPDMA INT0 List7 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
14	VPDMA_INT1_LIST7_COMPLETE_ENA	R/W	0h	VPDMA INT0 List7 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
13	VPDMA_INT1_LIST6_NOTIFY_ENA	R/W	0h	VPDMA INT0 List6 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
12	VPDMA_INT1_LIST6_COMPLETE_ENA	R/W	0h	VPDMA INT0 List6 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
11	VPDMA_INT1_LIST5_NOTIFY_ENA	R/W	0h	VPDMA INT0 List5 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
10	VPDMA_INT1_LIST5_COMPLETE_ENA	R/W	0h	VPDMA INT0 List5 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
9	VPDMA_INT1_LIST4_NOTIFY_ENA	R/W	0h	VPDMA INT0 List4 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
8	VPDMA_INT1_LIST4_COMPLETE_ENA	R/W	0h	VPDMA INT0 List4 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
7	VPDMA_INT1_LIST3_NOTIFY_ENA	R/W	0h	VPDMA INT0 List3 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
6	VPDMA_INT1_LIST3_COMPLETE_ENA	R/W	0h	VPDMA INT0 List3 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT1_LIST2_NOTIFY_ENA	R/W	0h	VPDMA INT0 List2 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT1_LIST2_COMPLETE_ENA	R/W	0h	VPDMA INT0 List2 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT1_LIST1_NOTIFY_ENA	R/W	0h	VPDMA INT0 List1 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT1_LIST1_COMPLETE_ENA	R/W	0h	VPDMA INT0 List1 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT1_LIST0_NOTIFY_ENA	R/W	0h	VPDMA INT0 List0 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT1_LIST0_COMPLETE_ENA	R/W	0h	VPDMA INT0 List0 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.14 intc_intr1_status_ena1 Register (offset = 4Ch) [reset = 0h]

intc_intr1_status_ena1 is shown in Figure 1-270 and described in Table 1-181.

Interrupt1 Enabled Register 1

Figure 1-270. intc_intr1_status_ena1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-181. intc_intr1_status_ena1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
20	COMP_ERR_INT_ENA	R/W	0h	COMP Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
19	GRPX3_INT_ENA	R/W	0h	GRPX3 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
18	GRPX2_INT_ENA	R/W	0h	GRPX2 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
17	GRPX1_INT_ENA	R/W	0h	GRPX1 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
16	DEI_ERROR_INT_ENA	R/W	0h	DEI Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect

Table 1-181. intc_intr1_status_ena1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	
7	VPDMA_INT1_CLIENT_ENA	R/W	0h	VPDMA INT0 Client Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
6	VPDMA_INT1_CHANNEL_GROUP6_ENA	R/W	0h	VPDMA INT0 Channel Group6 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT1_CHANNEL_GROUP5_ENA	R/W	0h	VPDMA INT0 Channel Group5 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT1_CHANNEL_GROUP4_ENA	R/W	0h	VPDMA INT0 Channel Group4 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT1_CHANNEL_GROUP3_ENA	R/W	0h	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT1_CHANNEL_GROUP2_ENA	R/W	0h	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT1_CHANNEL_GROUP1_ENA	R/W	0h	VPDMA INT0 Channel Group1 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT1_CHANNEL_GROUP0_ENA	R/W	0h	VPDMA INT0 Channel Group0 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.15 intc_intr1_ena_set0 Register (offset = 50h) [reset = 0h]

intc_intr1_ena_set0 is shown in Figure 1-271 and described in Table 1-182.

Interrupt1 Enable/Set Register 0

Figure 1-271. intc_intr1_ena_set0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA_SET	DVO2_INT2_ENA_SET	DVO2_INT1_ENA_SET	DVO2_INT0_ENA_SET	Reserved			DVO1_INT2_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA_SET	DVO1_INT0_ENA_SET	VIP2_PARSER_INT_ENA_SET	VIP1_PARSER_INT_ENA_SET	Reserved	DEI_FMD_INT_ENA_SET	Reserved	VPDMA_INT1_DESCRIPTOR_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT1_LIST7_NOTIFY_ENA_SET	VPDMA_INT1_LIST7_COMPLETE_ENA_SET	VPDMA_INT1_LIST6_NOTIFY_ENA_SET	VPDMA_INT1_LIST6_COMPLETE_ENA_SET	VPDMA_INT1_LIST5_NOTIFY_ENA_SET	VPDMA_INT1_LIST5_COMPLETE_ENA_SET	VPDMA_INT1_LIST4_NOTIFY_ENA_SET	VPDMA_INT1_LIST4_COMPLETE_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT1_LIST3_NOTIFY_ENA_SET	VPDMA_INT1_LIST3_COMPLETE_ENA_SET	VPDMA_INT1_LIST2_NOTIFY_ENA_SET	VPDMA_INT1_LIST2_COMPLETE_ENA_SET	VPDMA_INT1_LIST1_NOTIFY_ENA_SET	VPDMA_INT1_LIST1_COMPLETE_ENA_SET	VPDMA_INT1_LIST0_NOTIFY_ENA_SET	VPDMA_INT1_LIST0_COMPLETE_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-182. intc_intr1_ena_set0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA_SET	R/W	0h	SD_VENC Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
30	DVO2_INT2_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
29	DVO2_INT1_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
28	DVO2_INT0_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
23	DVO1_INT1_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
22	DVO1_INT0_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
21	VIP2_PARSER_INT_ENA_SET	R/W	0h	VIP2 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
20	VIP1_PARSER_INT_ENA_SET	R/W	0h	VIP1 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_ENA_SET	R/W	0h	DEI Film Mode Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	

Table 1-182. intc_intr1_ena_set0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VPDMA_INT1_DESCRIPTOR_ENA_SET	R/W	0h	VPDMA INT0 Descriptor Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15	VPDMA_INT1_LIST7_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List7 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
14	VPDMA_INT1_LIST7_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List7 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
13	VPDMA_INT1_LIST6_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List6 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
12	VPDMA_INT1_LIST6_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List6 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
11	VPDMA_INT1_LIST5_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List5 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
10	VPDMA_INT1_LIST5_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List5 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
9	VPDMA_INT1_LIST4_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List4 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
8	VPDMA_INT1_LIST4_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List4 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
7	VPDMA_INT1_LIST3_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List3 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
6	VPDMA_INT1_LIST3_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List3 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT1_LIST2_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List2 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT1_LIST2_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List2 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT1_LIST1_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List1 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT1_LIST1_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List1 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT1_LIST0_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List0 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT1_LIST0_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List0 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.16 intc_intr1_ena_set1 Register (offset = 54h) [reset = 0h]

intc_intr1_ena_set1 is shown in Figure 1-272 and described in Table 1-183.

Interrupt1 Enable/Set Register 1

Figure 1-272. intc_intr1_ena_set1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	NF_CHR_DS_UV_ERR_INT_ENA_SET	COMP_ERR_INT_ENA_SET	GRPX3_INT_ENA_SET	GRPX2_INT_ENA_SET	GRPX1_INT_ENA_SET	DEI_ERROR_INT_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT1_CLIENT_ENA_SET	VPDMA_INT1_CHANNEL_GROUP6_ENA_SET	VPDMA_INT1_CHANNEL_GROUP5_ENA_SET	VPDMA_INT1_CHANNEL_GROUP4_ENA_SET	VPDMA_INT1_CHANNEL_GROUP3_ENA_SET	VPDMA_INT1_CHANNEL_GROUP2_ENA_SET	VPDMA_INT1_CHANNEL_GROUP1_ENA_SET	VPDMA_INT1_CHANNEL_GROUP0_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-183. intc_intr1_ena_set1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA_SET	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
20	COMP_ERR_INT_ENA_SET	R/W	0h	COMP Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
19	GRPX3_INT_ENA_SET	R/W	0h	GRPX3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
18	GRPX2_INT_ENA_SET	R/W	0h	GRPX2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	GRPX1_INT_ENA_SET	R/W	0h	GRPX1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
16	DEI_ERROR_INT_ENA_SET	R/W	0h	DEI Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15-8	Reserved	R	0h	
7	VPDMA_INT1_CLIENT_ENA_SET	R/W	0h	VPDMA INT0 Client Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

Table 1-183. intc_intr1_ena_set1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	VPDMA_INT1_CHANNEL_GROUP6_ENA_SET	R/W	0h	VPDMA INT0 Channel Group6 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT1_CHANNEL_GROUP5_ENA_SET	R/W	0h	VPDMA INT0 Channel Group5 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT1_CHANNEL_GROUP4_ENA_SET	R/W	0h	VPDMA INT0 Channel Group4 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT1_CHANNEL_GROUP3_ENA_SET	R/W	0h	VPDMA INT0 Channel Group3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT1_CHANNEL_GROUP2_ENA_SET	R/W	0h	VPDMA INT0 Channel Group2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT1_CHANNEL_GROUP1_ENA_SET	R/W	0h	VPDMA INT0 Channel Group1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT1_CHANNEL_GROUP0_ENA_SET	R/W	0h	VPDMA INT0 Channel Group0 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.17 intc_intr1_ena_clr0 Register (offset = 58h) [reset = 0h]

intc_intr1_ena_clr0 is shown in Figure 1-273 and described in Table 1-184.

Interrupt1 Enable/Clear Register 0

Figure 1-273. intc_intr1_ena_clr0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA_CLR	DVO2_INT2_ENA_CLR	DVO2_INT1_ENA_CLR	DVO2_INT0_ENA_CLR	Reserved			DVO1_INT2_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA_CLR	DVO1_INT0_ENA_CLR	VIP2_PARSER_INT_ENA_CLR	VIP1_PARSER_INT_ENA_CLR	Reserved	DEI_FMD_INT_ENA_CLR	Reserved	VPDMA_INT1_DESCRIPTOR_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT1_LIST7_NOTIFY_ENA_CLR	VPDMA_INT1_LIST7_COMPLETE_ENA_CLR	VPDMA_INT1_LIST6_NOTIFY_ENA_CLR	VPDMA_INT1_LIST6_COMPLETE_ENA_CLR	VPDMA_INT1_LIST5_NOTIFY_ENA_CLR	VPDMA_INT1_LIST5_COMPLETE_ENA_CLR	VPDMA_INT1_LIST4_NOTIFY_ENA_CLR	VPDMA_INT1_LIST4_COMPLETE_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT1_LIST3_NOTIFY_ENA_CLR	VPDMA_INT1_LIST3_COMPLETE_ENA_CLR	VPDMA_INT1_LIST2_NOTIFY_ENA_CLR	VPDMA_INT1_LIST2_COMPLETE_ENA_CLR	VPDMA_INT1_LIST1_NOTIFY_ENA_CLR	VPDMA_INT1_LIST1_COMPLETE_ENA_CLR	VPDMA_INT1_LIST0_NOTIFY_ENA_CLR	VPDMA_INT1_LIST0_COMPLETE_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-184. intc_intr1_ena_clr0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA_CLR	R/W	0h	SD_VENC Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
30	DVO2_INT2_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
29	DVO2_INT1_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
28	DVO2_INT0_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
23	DVO1_INT1_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
22	DVO1_INT0_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
21	VIP2_PARSER_INT_ENA_CLR	R/W	0h	VIP2 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
20	VIP1_PARSER_INT_ENA_CLR	R/W	0h	VIP1 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_ENA_CLR	R/W	0h	DEI Film Mode Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	

Table 1-184. intc_intr1_ena_clr0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VPDMA_INT1_DESCRIPTOR_ENA_CLR	R/W	0h	VPDMA INT0 Descriptor Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
15	VPDMA_INT1_LIST7_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List7 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
14	VPDMA_INT1_LIST7_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List7 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
13	VPDMA_INT1_LIST6_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List6 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
12	VPDMA_INT1_LIST6_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List6 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
11	VPDMA_INT1_LIST5_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List5 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
10	VPDMA_INT1_LIST5_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List5 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
9	VPDMA_INT1_LIST4_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List4 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
8	VPDMA_INT1_LIST4_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List4 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
7	VPDMA_INT1_LIST3_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List3 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
6	VPDMA_INT1_LIST3_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List3 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
5	VPDMA_INT1_LIST2_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List2 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
4	VPDMA_INT1_LIST2_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List2 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
3	VPDMA_INT1_LIST1_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List1 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
2	VPDMA_INT1_LIST1_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List1 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
1	VPDMA_INT1_LIST0_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List0 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
0	VPDMA_INT1_LIST0_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List0 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

1.3.7.18 intc_intr1_ena_clr1 Register (offset = 5Ch) [reset = 0h]

intc_intr1_ena_clr1 is shown in Figure 1-274 and described in Table 1-185.

Interrupt1 Enable/Clear Register 1

Figure 1-274. intc_intr1_ena_clr1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	NF_CHR_DS_UV_ERR_INT_ENA_CLR	COMP_ERR_INT_ENA_CLR	GRPX3_INT_ENA_CLR	GRPX2_INT_ENA_CLR	GRPX1_INT_ENA_CLR	DEI_ERROR_INT_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT1_CLIENT_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP6_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP5_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP4_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP3_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP2_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP1_ENA_CLR	VPDMA_INT1_CHANNEL_GROUP0_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-185. intc_intr1_ena_clr1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA_CLR	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
20	COMP_ERR_INT_ENA_CLR	R/W	0h	COMP Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
19	GRPX3_INT_ENA_CLR	R/W	0h	GRPX3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
18	GRPX2_INT_ENA_CLR	R/W	0h	GRPX2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
17	GRPX1_INT_ENA_CLR	R/W	0h	GRPX1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
16	DEI_ERROR_INT_ENA_CLR	R/W	0h	DEI Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

Table 1-185. intc_intr1_ena_clr1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	
7	VPDMA_INT1_CLIENT_ENA_CLR	R/W	0h	VPDMA INT0 Client Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
6	VPDMA_INT1_CHANNEL_GROUP6_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group6 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
5	VPDMA_INT1_CHANNEL_GROUP5_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group5 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
4	VPDMA_INT1_CHANNEL_GROUP4_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group4 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
3	VPDMA_INT1_CHANNEL_GROUP3_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
2	VPDMA_INT1_CHANNEL_GROUP2_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
1	VPDMA_INT1_CHANNEL_GROUP1_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
0	VPDMA_INT1_CHANNEL_GROUP0_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group0 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

1.3.7.19 intc_intr2_status_raw0 Register (offset = 60h) [reset = 0h]

intc_intr2_status_raw0 is shown in Figure 1-275 and described in Table 1-186.

Interrupt2 Raw Register 0

Figure 1-275. intc_intr2_status_raw0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_RAW	DVO2_INT2_RAW	DVO2_INT1_RAW	DVO2_INT0_RAW	Reserved			DVO1_INT2_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_RAW	DVO1_INT0_RAW	VIP2_PARSER_INT_RAW	VIP1_PARSER_INT_RAW	Reserved	DEI_FMD_INT_RAW	Reserved	VPDMA_INT2_DESCRIPTOR_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT2_LIST7_NOTIFY_RAW	VPDMA_INT2_LIST7_COMPLETE_RAW	VPDMA_INT2_LIST6_NOTIFY_RAW	VPDMA_INT2_LIST6_COMPLETE_RAW	VPDMA_INT2_LIST5_NOTIFY_RAW	VPDMA_INT2_LIST5_COMPLETE_RAW	VPDMA_INT2_LIST4_NOTIFY_RAW	VPDMA_INT2_LIST4_COMPLETE_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT2_LIST3_NOTIFY_RAW	VPDMA_INT2_LIST3_COMPLETE_RAW	VPDMA_INT2_LIST2_NOTIFY_RAW	VPDMA_INT2_LIST2_COMPLETE_RAW	VPDMA_INT2_LIST1_NOTIFY_RAW	VPDMA_INT2_LIST1_COMPLETE_RAW	VPDMA_INT2_LIST0_NOTIFY_RAW	VPDMA_INT2_LIST0_COMPLETE_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-186. intc_intr2_status_raw0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_RAW	R/W	0h	SD VENC Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
30	DVO2_INT2_RAW	R/W	0h	DVO2 Interrupt2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
29	DVO2_INT1_RAW	R/W	0h	DVO2 Interrupt1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
28	DVO2_INT0_RAW	R/W	0h	DVO2 Interrupt0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_RAW	R/W	0h	DVO1 Interrupt2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
23	DVO1_INT1_RAW	R/W	0h	DVO1 Interrupt1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
22	DVO1_INT0_RAW	R/W	0h	DVO1 Interrupt0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
21	VIP2_PARSER_INT_RAW	R/W	0h	VIP2 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
20	VIP1_PARSER_INT_RAW	R/W	0h	VIP1 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_RAW	R/W	0h	DEI Film Mode Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
17	Reserved	R	0h	
16	VPDMA_INT2_DESCRIPTOR_RAW	R/W	0h	VPDMA INT0 Descriptor Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
15	VPDMA_INT2_LIST7_NOTIFY_RAW	R/W	0h	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
14	VPDMA_INT2_LIST7_COMPLETE_RAW	R/W	0h	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

Table 1-186. intc_intr2_status_raw0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	VPDMA_INT2_LIST6_NOTIFY_RAW	R/W	0h	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
12	VPDMA_INT2_LIST6_COMPLETE_RAW	R/W	0h	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
11	VPDMA_INT2_LIST5_NOTIFY_RAW	R/W	0h	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
10	VPDMA_INT2_LIST5_COMPLETE_RAW	R/W	0h	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
9	VPDMA_INT2_LIST4_NOTIFY_RAW	R/W	0h	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
8	VPDMA_INT2_LIST4_COMPLETE_RAW	R/W	0h	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
7	VPDMA_INT2_LIST3_NOTIFY_RAW	R/W	0h	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
6	VPDMA_INT2_LIST3_COMPLETE_RAW	R/W	0h	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT2_LIST2_NOTIFY_RAW	R/W	0h	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT2_LIST2_COMPLETE_RAW	R/W	0h	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT2_LIST1_NOTIFY_RAW	R/W	0h	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT2_LIST1_COMPLETE_RAW	R/W	0h	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT2_LIST0_NOTIFY_RAW	R/W	0h	VPDMA INT0 List0 Notify Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT2_LIST0_COMPLETE_RAW	R/W	0h	VPDMA INT0 List0 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.20 intc_intr2_status_raw1 Register (offset = 64h) [reset = 0h]

intc_intr2_status_raw1 is shown in Figure 1-276 and described in Table 1-187.

Interrupt2 Raw Register 1

Figure 1-276. intc_intr2_status_raw1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_RAW	VIP2_CHR_DS_1_UV_ERR_INT_RAW
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_RAW	VIP1_CHR_DS_1_UV_ERR_INT_RAW	NF_CHR_DS_UV_ERR_INT_RAW	COMP_ERR_INT_RAW	GRPX3_INT_RAW	GRPX2_INT_RAW	GRPX1_INT_RAW	DEI_ERROR_INT_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT2_CLIENT_RAW	VPDMA_INT2_CHANNEL_GROUP6_RAW	VPDMA_INT2_CHANNEL_GROUP5_RAW	VPDMA_INT2_CHANNEL_GROUP4_RAW	VPDMA_INT2_CHANNEL_GROUP3_RAW	VPDMA_INT2_CHANNEL_GROUP2_RAW	VPDMA_INT2_CHANNEL_GROUP1_RAW	VPDMA_INT2_CHANNEL_GROUP0_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-187. intc_intr2_status_raw1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_RAW	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_RAW	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_RAW	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_RAW	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_RAW	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
20	COMP_ERR_INT_RAW	R/W	0h	COMP Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
19	GRPX3_INT_RAW	R/W	0h	GRPX3 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
18	GRPX2_INT_RAW	R/W	0h	GRPX2 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
17	GRPX1_INT_RAW	R/W	0h	GRPX1 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
16	DEI_ERROR_INT_RAW	R/W	0h	DEI Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
15-8	Reserved	R	0h	
7	VPDMA_INT2_CLIENT_RAW	R/W	0h	VPDMA INT0 Client Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

Table 1-187. intc_intr2_status_raw1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	VPDMA_INT2_CHANNEL_GROUP6_RAW	R/W	0h	VPDMA INT0 Channel Group6 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT2_CHANNEL_GROUP5_RAW	R/W	0h	VPDMA INT0 Channel Group5 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT2_CHANNEL_GROUP4_RAW	R/W	0h	VPDMA INT0 Channel Group4 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT2_CHANNEL_GROUP3_RAW	R/W	0h	VPDMA INT0 Channel Group3 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT2_CHANNEL_GROUP2_RAW	R/W	0h	VPDMA INT0 Channel Group2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT2_CHANNEL_GROUP1_RAW	R/W	0h	VPDMA INT0 Channel Group1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT2_CHANNEL_GROUP0_RAW	R/W	0h	VPDMA INT0 Channel Group0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.21 intc_intr2_status_ena0 Register (offset = 68h) [reset = 0h]

intc_intr2_status_ena0 is shown in Figure 1-277 and described in Table 1-188.

Interrupt2 Enabled Register 0

Figure 1-277. intc_intr2_status_ena0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA	DVO2_INT2_ENA	DVO2_INT1_ENA	DVO2_INT0_ENA	Reserved			DVO1_INT2_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA	DVO1_INT0_ENA	VIP2_PARSER_INT_ENA	VIP1_PARSER_INT_ENA	Reserved	DEI_FMD_INT_ENA	Reserved	VPDMA_INT2_DESCRIPTOR_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT2_LIST7_NOTIFY_ENA	VPDMA_INT2_LIST7_COMPLETE_ENA	VPDMA_INT2_LIST6_NOTIFY_ENA	VPDMA_INT2_LIST6_COMPLETE_ENA	VPDMA_INT2_LIST5_NOTIFY_ENA	VPDMA_INT2_LIST5_COMPLETE_ENA	VPDMA_INT2_LIST4_NOTIFY_ENA	VPDMA_INT2_LIST4_COMPLETE_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT2_LIST3_NOTIFY_ENA	VPDMA_INT2_LIST3_COMPLETE_ENA	VPDMA_INT2_LIST2_NOTIFY_ENA	VPDMA_INT2_LIST2_COMPLETE_ENA	VPDMA_INT2_LIST1_NOTIFY_ENA	VPDMA_INT2_LIST1_COMPLETE_ENA	VPDMA_INT2_LIST0_NOTIFY_ENA	VPDMA_INT2_LIST0_COMPLETE_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-188. intc_intr2_status_ena0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA	R/W	0h	SD_VENC Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
30	DVO2_INT2_ENA	R/W	0h	DVO2 Enabled Interrupt2 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
29	DVO2_INT1_ENA	R/W	0h	DVO2 Enabled Interrupt1 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
28	DVO2_INT0_ENA	R/W	0h	DVO2 Enabled Interrupt0 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA	R/W	0h	DVO1 Enabled Interrupt2 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
23	DVO1_INT1_ENA	R/W	0h	DVO1 Enabled Interrupt1 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
22	DVO1_INT0_ENA	R/W	0h	DVO1 Enabled Interrupt0 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
21	VIP2_PARSER_INT_ENA	R/W	0h	VIP2 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
20	VIP1_PARSER_INT_ENA	R/W	0h	VIP1 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
19	Reserved	R	0h	

Table 1-188. intc_intr2_status_ena0 Register Field Descriptions (continued)

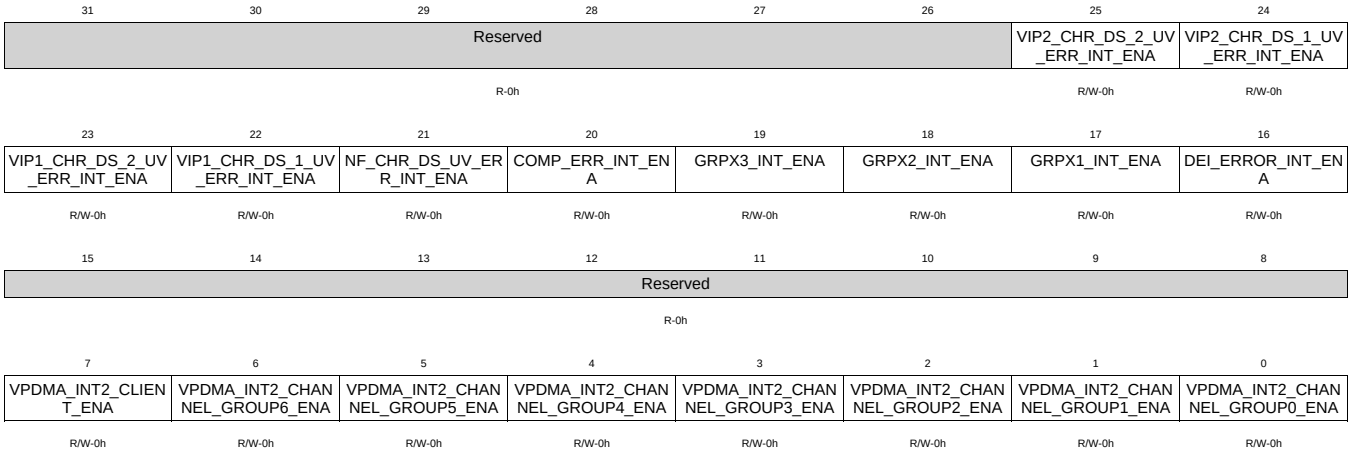
Bit	Field	Type	Reset	Description
18	DEI_FMD_INT_ENA	R/W	0h	DEI Film Mode Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	
16	VPDMA_INT2_DESCRIPTOR_ENA	R/W	0h	VPDMA INT0 Descriptor Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15	VPDMA_INT2_LIST7_NOTIFY_ENA	R/W	0h	VPDMA INT0 List7 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
14	VPDMA_INT2_LIST7_COMPLETE_ENA	R/W	0h	VPDMA INT0 List7 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
13	VPDMA_INT2_LIST6_NOTIFY_ENA	R/W	0h	VPDMA INT0 List6 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
12	VPDMA_INT2_LIST6_COMPLETE_ENA	R/W	0h	VPDMA INT0 List6 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
11	VPDMA_INT2_LIST5_NOTIFY_ENA	R/W	0h	VPDMA INT0 List5 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
10	VPDMA_INT2_LIST5_COMPLETE_ENA	R/W	0h	VPDMA INT0 List5 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
9	VPDMA_INT2_LIST4_NOTIFY_ENA	R/W	0h	VPDMA INT0 List4 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
8	VPDMA_INT2_LIST4_COMPLETE_ENA	R/W	0h	VPDMA INT0 List4 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
7	VPDMA_INT2_LIST3_NOTIFY_ENA	R/W	0h	VPDMA INT0 List3 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
6	VPDMA_INT2_LIST3_COMPLETE_ENA	R/W	0h	VPDMA INT0 List3 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT2_LIST2_NOTIFY_ENA	R/W	0h	VPDMA INT0 List2 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT2_LIST2_COMPLETE_ENA	R/W	0h	VPDMA INT0 List2 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT2_LIST1_NOTIFY_ENA	R/W	0h	VPDMA INT0 List1 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT2_LIST1_COMPLETE_ENA	R/W	0h	VPDMA INT0 List1 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT2_LIST0_NOTIFY_ENA	R/W	0h	VPDMA INT0 List0 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT2_LIST0_COMPLETE_ENA	R/W	0h	VPDMA INT0 List0 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.22 intc_intr2_status_ena1 Register (offset = 6Ch) [reset = 0h]

intc_intr2_status_ena1 is shown in Figure 1-278 and described in Table 1-189.

Interrupt2 Enabled Register 1

Figure 1-278. intc_intr2_status_ena1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-189. intc_intr2_status_ena1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
20	COMP_ERR_INT_ENA	R/W	0h	COMP Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
19	GRPX3_INT_ENA	R/W	0h	GRPX3 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
18	GRPX2_INT_ENA	R/W	0h	GRPX2 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
17	GRPX1_INT_ENA	R/W	0h	GRPX1 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
16	DEI_ERROR_INT_ENA	R/W	0h	DEI Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect

Table 1-189. intc_intr2_status_ena1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	
7	VPDMA_INT2_CLIENT_ENA	R/W	0h	VPDMA INT0 Client Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
6	VPDMA_INT2_CHANNEL_GROUP6_ENA	R/W	0h	VPDMA INT0 Channel Group6 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT2_CHANNEL_GROUP5_ENA	R/W	0h	VPDMA INT0 Channel Group5 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT2_CHANNEL_GROUP4_ENA	R/W	0h	VPDMA INT0 Channel Group4 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT2_CHANNEL_GROUP3_ENA	R/W	0h	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT2_CHANNEL_GROUP2_ENA	R/W	0h	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT2_CHANNEL_GROUP1_ENA	R/W	0h	VPDMA INT0 Channel Group1 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT2_CHANNEL_GROUP0_ENA	R/W	0h	VPDMA INT0 Channel Group0 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.23 intc_intr2_ena_set0 Register (offset = 70h) [reset = 0h]

intc_intr2_ena_set0 is shown in Figure 1-279 and described in Table 1-190.

Interrupt2 Enable/Set Register 0

Figure 1-279. intc_intr2_ena_set0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA_SET	DVO2_INT2_ENA_SET	DVO2_INT1_ENA_SET	DVO2_INT0_ENA_SET	Reserved			DVO1_INT2_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA_SET	DVO1_INT0_ENA_SET	VIP2_PARSER_INT_ENA_SET	VIP1_PARSER_INT_ENA_SET	Reserved	DEI_FMD_INT_ENA_SET	Reserved	VPDMA_INT2_DESCRIPTOR_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT2_LIST7_NOTIFY_ENA_SET	VPDMA_INT2_LIST7_COMPLETE_ENA_SET	VPDMA_INT2_LIST6_NOTIFY_ENA_SET	VPDMA_INT2_LIST6_COMPLETE_ENA_SET	VPDMA_INT2_LIST5_NOTIFY_ENA_SET	VPDMA_INT2_LIST5_COMPLETE_ENA_SET	VPDMA_INT2_LIST4_NOTIFY_ENA_SET	VPDMA_INT2_LIST4_COMPLETE_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT2_LIST3_NOTIFY_ENA_SET	VPDMA_INT2_LIST3_COMPLETE_ENA_SET	VPDMA_INT2_LIST2_NOTIFY_ENA_SET	VPDMA_INT2_LIST2_COMPLETE_ENA_SET	VPDMA_INT2_LIST1_NOTIFY_ENA_SET	VPDMA_INT2_LIST1_COMPLETE_ENA_SET	VPDMA_INT2_LIST0_NOTIFY_ENA_SET	VPDMA_INT2_LIST0_COMPLETE_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-190. intc_intr2_ena_set0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA_SET	R/W	0h	SD_VENC Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
30	DVO2_INT2_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
29	DVO2_INT1_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
28	DVO2_INT0_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
23	DVO1_INT1_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
22	DVO1_INT0_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
21	VIP2_PARSER_INT_ENA_SET	R/W	0h	VIP2 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
20	VIP1_PARSER_INT_ENA_SET	R/W	0h	VIP1 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_ENA_SET	R/W	0h	DEI Film Mode Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	

Table 1-190. intc_intr2_ena_set0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VPDMA_INT2_DESCRIPTOR_ENA_SET	R/W	0h	VPDMA INT0 Descriptor Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15	VPDMA_INT2_LIST7_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List7 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
14	VPDMA_INT2_LIST7_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List7 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
13	VPDMA_INT2_LIST6_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List6 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
12	VPDMA_INT2_LIST6_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List6 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
11	VPDMA_INT2_LIST5_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List5 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
10	VPDMA_INT2_LIST5_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List5 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
9	VPDMA_INT2_LIST4_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List4 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
8	VPDMA_INT2_LIST4_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List4 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
7	VPDMA_INT2_LIST3_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List3 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
6	VPDMA_INT2_LIST3_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List3 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT2_LIST2_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List2 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT2_LIST2_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List2 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT2_LIST1_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List1 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT2_LIST1_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List1 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT2_LIST0_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List0 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT2_LIST0_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List0 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.24 intc_intr2_ena_set1 Register (offset = 74h) [reset = 0h]

intc_intr2_ena_set1 is shown in Figure 1-280 and described in Table 1-191.

Interrupt2 Enable/Set Register 1

Figure 1-280. intc_intr2_ena_set1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	NF_CHR_DS_UV_ERR_INT_ENA_SET	COMP_ERR_INT_ENA_SET	GRPX3_INT_ENA_SET	GRPX2_INT_ENA_SET	GRPX1_INT_ENA_SET	DEI_ERROR_INT_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT2_CLIENT_ENA_SET	VPDMA_INT2_CHANNEL_GROUP6_ENA_SET	VPDMA_INT2_CHANNEL_GROUP5_ENA_SET	VPDMA_INT2_CHANNEL_GROUP4_ENA_SET	VPDMA_INT2_CHANNEL_GROUP3_ENA_SET	VPDMA_INT2_CHANNEL_GROUP2_ENA_SET	VPDMA_INT2_CHANNEL_GROUP1_ENA_SET	VPDMA_INT2_CHANNEL_GROUP0_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-191. intc_intr2_ena_set1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA_SET	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
20	COMP_ERR_INT_ENA_SET	R/W	0h	COMP Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
19	GRPX3_INT_ENA_SET	R/W	0h	GRPX3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
18	GRPX2_INT_ENA_SET	R/W	0h	GRPX2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	GRPX1_INT_ENA_SET	R/W	0h	GRPX1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
16	DEI_ERROR_INT_ENA_SET	R/W	0h	DEI Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15-8	Reserved	R	0h	
7	VPDMA_INT2_CLIENT_ENA_SET	R/W	0h	VPDMA INT0 Client Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

Table 1-191. intc_intr2_ena_set1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	VPDMA_INT2_CHANNEL_GROUP6_ENA_SET	R/W	0h	VPDMA INT0 Channel Group6 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT2_CHANNEL_GROUP5_ENA_SET	R/W	0h	VPDMA INT0 Channel Group5 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT2_CHANNEL_GROUP4_ENA_SET	R/W	0h	VPDMA INT0 Channel Group4 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT2_CHANNEL_GROUP3_ENA_SET	R/W	0h	VPDMA INT0 Channel Group3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT2_CHANNEL_GROUP2_ENA_SET	R/W	0h	VPDMA INT0 Channel Group2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT2_CHANNEL_GROUP1_ENA_SET	R/W	0h	VPDMA INT0 Channel Group1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT2_CHANNEL_GROUP0_ENA_SET	R/W	0h	VPDMA INT0 Channel Group0 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.25 intc_intr2_ena_clr0 Register (offset = 78h) [reset = 0h]

intc_intr2_ena_clr0 is shown in Figure 1-281 and described in Table 1-192.

Interrupt2 Enable/Clear Register 0

Figure 1-281. intc_intr2_ena_clr0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA_CLR	DVO2_INT2_ENA_CLR	DVO2_INT1_ENA_CLR	DVO2_INT0_ENA_CLR	Reserved			DVO1_INT2_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA_CLR	DVO1_INT0_ENA_CLR	VIP2_PARSER_INT_ENA_CLR	VIP1_PARSER_INT_ENA_CLR	Reserved	DEI_FMD_INT_ENA_CLR	Reserved	VPDMA_INT2_DESCRIPTOR_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT2_LIST7_NOTIFY_ENA_CLR	VPDMA_INT2_LIST7_COMPLETE_ENA_CLR	VPDMA_INT2_LIST6_NOTIFY_ENA_CLR	VPDMA_INT2_LIST6_COMPLETE_ENA_CLR	VPDMA_INT2_LIST5_NOTIFY_ENA_CLR	VPDMA_INT2_LIST5_COMPLETE_ENA_CLR	VPDMA_INT2_LIST4_NOTIFY_ENA_CLR	VPDMA_INT2_LIST4_COMPLETE_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT2_LIST3_NOTIFY_ENA_CLR	VPDMA_INT2_LIST3_COMPLETE_ENA_CLR	VPDMA_INT2_LIST2_NOTIFY_ENA_CLR	VPDMA_INT2_LIST2_COMPLETE_ENA_CLR	VPDMA_INT2_LIST1_NOTIFY_ENA_CLR	VPDMA_INT2_LIST1_COMPLETE_ENA_CLR	VPDMA_INT2_LIST0_NOTIFY_ENA_CLR	VPDMA_INT2_LIST0_COMPLETE_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-192. intc_intr2_ena_clr0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA_CLR	R/W	0h	SD_VENC Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
30	DVO2_INT2_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
29	DVO2_INT1_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
28	DVO2_INT0_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
23	DVO1_INT1_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
22	DVO1_INT0_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
21	VIP2_PARSER_INT_ENA_CLR	R/W	0h	VIP2 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
20	VIP1_PARSER_INT_ENA_CLR	R/W	0h	VIP1 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_ENA_CLR	R/W	0h	DEI Film Mode Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	

Table 1-192. intc_intr2_ena_clr0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VPDMA_INT2_DESCRIPTOR_ENA_CLR	R/W	0h	VPDMA INT0 Descriptor Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
15	VPDMA_INT2_LIST7_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List7 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
14	VPDMA_INT2_LIST7_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List7 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
13	VPDMA_INT2_LIST6_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List6 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
12	VPDMA_INT2_LIST6_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List6 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
11	VPDMA_INT2_LIST5_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List5 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
10	VPDMA_INT2_LIST5_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List5 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
9	VPDMA_INT2_LIST4_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List4 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
8	VPDMA_INT2_LIST4_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List4 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
7	VPDMA_INT2_LIST3_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List3 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
6	VPDMA_INT2_LIST3_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List3 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
5	VPDMA_INT2_LIST2_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List2 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
4	VPDMA_INT2_LIST2_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List2 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
3	VPDMA_INT2_LIST1_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List1 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
2	VPDMA_INT2_LIST1_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List1 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
1	VPDMA_INT2_LIST0_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List0 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
0	VPDMA_INT2_LIST0_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List0 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

1.3.7.26 intc_intr2_ena_clr1 Register (offset = 7Ch) [reset = 0h]

intc_intr2_ena_clr1 is shown in Figure 1-282 and described in Table 1-193.

Interrupt2 Enable/Clear Register 1

Figure 1-282. intc_intr2_ena_clr1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	NF_CHR_DS_UV_ERR_INT_ENA_CLR	COMP_ERR_INT_ENA_CLR	GRPX3_INT_ENA_CLR	GRPX2_INT_ENA_CLR	GRPX1_INT_ENA_CLR	DEI_ERROR_INT_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT2_CLIENT_ENA_CLR	VPDMA_INT2_CHANNEL_GROUP6_ENA_CLR	VPDMA_INT2_CHANNEL_GROUP5_ENA_CLR	VPDMA_INT2_CHANNEL_GROUP4_ENA_CLR	VPDMA_INT2_CHANNEL_GROUP3_ENA_CLR	VPDMA_INT2_CHANNEL_GROUP2_ENA_CLR	VPDMA_INT2_CHANNEL_GROUP1_ENA_CLR	VPDMA_INT2_CHANNEL_GROUP0_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-193. intc_intr2_ena_clr1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA_CLR	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
20	COMP_ERR_INT_ENA_CLR	R/W	0h	COMP Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
19	GRPX3_INT_ENA_CLR	R/W	0h	GRPX3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
18	GRPX2_INT_ENA_CLR	R/W	0h	GRPX2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
17	GRPX1_INT_ENA_CLR	R/W	0h	GRPX1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
16	DEI_ERROR_INT_ENA_CLR	R/W	0h	DEI Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

Table 1-193. intc_intr2_ena_clr1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	
7	VPDMA_INT2_CLIENT_ENA_CLR	R/W	0h	VPDMA INT0 Client Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
6	VPDMA_INT2_CHANNEL_GROUP6_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group6 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
5	VPDMA_INT2_CHANNEL_GROUP5_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group5 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
4	VPDMA_INT2_CHANNEL_GROUP4_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group4 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
3	VPDMA_INT2_CHANNEL_GROUP3_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
2	VPDMA_INT2_CHANNEL_GROUP2_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
1	VPDMA_INT2_CHANNEL_GROUP1_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
0	VPDMA_INT2_CHANNEL_GROUP0_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group0 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

1.3.7.27 intc_intr3_status_raw0 Register (offset = 80h) [reset = 0h]

intc_intr3_status_raw0 is shown in Figure 1-283 and described in Table 1-194.

Interrupt3 Raw Register 0

Figure 1-283. intc_intr3_status_raw0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_RAW	DVO2_INT2_RAW	DVO2_INT1_RAW	DVO2_INT0_RAW	Reserved			DVO1_INT2_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_RAW	DVO1_INT0_RAW	VIP2_PARSER_INT_RAW	VIP1_PARSER_INT_RAW	Reserved	DEI_FMD_INT_RAW	Reserved	VPDMA_INT3_DESCRIPTOR_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT3_LIST7_NOTIFY_RAW	VPDMA_INT3_LIST7_COMPLETE_RAW	VPDMA_INT3_LIST6_NOTIFY_RAW	VPDMA_INT3_LIST6_COMPLETE_RAW	VPDMA_INT3_LIST5_NOTIFY_RAW	VPDMA_INT3_LIST5_COMPLETE_RAW	VPDMA_INT3_LIST4_NOTIFY_RAW	VPDMA_INT3_LIST4_COMPLETE_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT3_LIST3_NOTIFY_RAW	VPDMA_INT3_LIST3_COMPLETE_RAW	VPDMA_INT3_LIST2_NOTIFY_RAW	VPDMA_INT3_LIST2_COMPLETE_RAW	VPDMA_INT3_LIST1_NOTIFY_RAW	VPDMA_INT3_LIST1_COMPLETE_RAW	VPDMA_INT3_LIST0_NOTIFY_RAW	VPDMA_INT3_LIST0_COMPLETE_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-194. intc_intr3_status_raw0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_RAW	R/W	0h	SD VENC Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
30	DVO2_INT2_RAW	R/W	0h	DVO2 Interrupt2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
29	DVO2_INT1_RAW	R/W	0h	DVO2 Interrupt1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
28	DVO2_INT0_RAW	R/W	0h	DVO2 Interrupt0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_RAW	R/W	0h	DVO1 Interrupt2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
23	DVO1_INT1_RAW	R/W	0h	DVO1 Interrupt1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
22	DVO1_INT0_RAW	R/W	0h	DVO1 Interrupt0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
21	VIP2_PARSER_INT_RAW	R/W	0h	VIP2 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
20	VIP1_PARSER_INT_RAW	R/W	0h	VIP1 Parser Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_RAW	R/W	0h	DEI Film Mode Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
17	Reserved	R	0h	
16	VPDMA_INT3_DESCRIPTOR_RAW	R/W	0h	VPDMA INT0 Descriptor Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
15	VPDMA_INT3_LIST7_NOTIFY_RAW	R/W	0h	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
14	VPDMA_INT3_LIST7_COMPLETE_RAW	R/W	0h	VPDMA INT0 List7 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

Table 1-194. intc_intr3_status_raw0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	VPDMA_INT3_LIST6_NOTIFY_RAW	R/W	0h	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
12	VPDMA_INT3_LIST6_COMPLETE_RAW	R/W	0h	VPDMA INT0 List6 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
11	VPDMA_INT3_LIST5_NOTIFY_RAW	R/W	0h	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
10	VPDMA_INT3_LIST5_COMPLETE_RAW	R/W	0h	VPDMA INT0 List5 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
9	VPDMA_INT3_LIST4_NOTIFY_RAW	R/W	0h	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
8	VPDMA_INT3_LIST4_COMPLETE_RAW	R/W	0h	VPDMA INT0 List4 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
7	VPDMA_INT3_LIST3_NOTIFY_RAW	R/W	0h	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
6	VPDMA_INT3_LIST3_COMPLETE_RAW	R/W	0h	VPDMA INT0 List3 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT3_LIST2_NOTIFY_RAW	R/W	0h	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT3_LIST2_COMPLETE_RAW	R/W	0h	VPDMA INT0 List2 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT3_LIST1_NOTIFY_RAW	R/W	0h	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT3_LIST1_COMPLETE_RAW	R/W	0h	VPDMA INT0 List1 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT3_LIST0_NOTIFY_RAW	R/W	0h	VPDMA INT0 List0 Notify Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT3_LIST0_COMPLETE_RAW	R/W	0h	VPDMA INT0 List0 Complete Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.28 intc_intr3_status_raw1 Register (offset = 84h) [reset = 0h]

intc_intr3_status_raw1 is shown in Figure 1-284 and described in Table 1-195.

Interrupt3 Raw Register 0

Figure 1-284. intc_intr3_status_raw1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_RAW	VIP2_CHR_DS_1_UV_ERR_INT_RAW
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_RAW	VIP1_CHR_DS_1_UV_ERR_INT_RAW	NF_CHR_DS_UV_ERR_INT_RAW	COMP_ERR_INT_RAW	GRPX3_INT_RAW	GRPX2_INT_RAW	GRPX1_INT_RAW	DEI_ERROR_INT_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT3_CLIENT_RAW	VPDMA_INT3_CHANNEL_GROUP6_RAW	VPDMA_INT3_CHANNEL_GROUP5_RAW	VPDMA_INT3_CHANNEL_GROUP4_RAW	VPDMA_INT3_CHANNEL_GROUP3_RAW	VPDMA_INT3_CHANNEL_GROUP2_RAW	VPDMA_INT3_CHANNEL_GROUP1_RAW	VPDMA_INT3_CHANNEL_GROUP0_RAW
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-195. intc_intr3_status_raw1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_RAW	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_RAW	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_RAW	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_RAW	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_RAW	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
20	COMP_ERR_INT_RAW	R/W	0h	COMP Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
19	GRPX3_INT_RAW	R/W	0h	GRPX3 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
18	GRPX2_INT_RAW	R/W	0h	GRPX2 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
17	GRPX1_INT_RAW	R/W	0h	GRPX1 Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
16	DEI_ERROR_INT_RAW	R/W	0h	DEI Error Interrupt Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
15-8	Reserved	R	0h	
7	VPDMA_INT3_CLIENT_RAW	R/W	0h	VPDMA INT0 Client Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

Table 1-195. intc_intr3_status_raw1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	VPDMA_INT3_CHANNEL_GROUP6_RAW	R/W	0h	VPDMA INT0 Channel Group6 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT3_CHANNEL_GROUP5_RAW	R/W	0h	VPDMA INT0 Channel Group5 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT3_CHANNEL_GROUP4_RAW	R/W	0h	VPDMA INT0 Channel Group4 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT3_CHANNEL_GROUP3_RAW	R/W	0h	VPDMA INT0 Channel Group3 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT3_CHANNEL_GROUP2_RAW	R/W	0h	VPDMA INT0 Channel Group2 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT3_CHANNEL_GROUP1_RAW	R/W	0h	VPDMA INT0 Channel Group1 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT3_CHANNEL_GROUP0_RAW	R/W	0h	VPDMA INT0 Channel Group0 Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.29 intc_intr3_status_ena0 Register (offset = 88h) [reset = 0h]

intc_intr3_status_ena0 is shown in Figure 1-285 and described in Table 1-196.

Interrupt3 Enabled Register 0

Figure 1-285. intc_intr3_status_ena0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA	DVO2_INT2_ENA	DVO2_INT1_ENA	DVO2_INT0_ENA	Reserved			DVO1_INT2_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA	DVO1_INT0_ENA	VIP2_PARSER_INT_ENA	VIP1_PARSER_INT_ENA	Reserved	DEI_FMD_INT_ENA	Reserved	VPDMA_INT3_DESCRIPTOR_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT3_LIST7_NOTIFY_ENA	VPDMA_INT3_LIST7_COMPLETE_ENA	VPDMA_INT3_LIST6_NOTIFY_ENA	VPDMA_INT3_LIST6_COMPLETE_ENA	VPDMA_INT3_LIST5_NOTIFY_ENA	VPDMA_INT3_LIST5_COMPLETE_ENA	VPDMA_INT3_LIST4_NOTIFY_ENA	VPDMA_INT3_LIST4_COMPLETE_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT3_LIST3_NOTIFY_ENA	VPDMA_INT3_LIST3_COMPLETE_ENA	VPDMA_INT3_LIST2_NOTIFY_ENA	VPDMA_INT3_LIST2_COMPLETE_ENA	VPDMA_INT3_LIST1_NOTIFY_ENA	VPDMA_INT3_LIST1_COMPLETE_ENA	VPDMA_INT3_LIST0_NOTIFY_ENA	VPDMA_INT3_LIST0_COMPLETE_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-196. intc_intr3_status_ena0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA	R/W	0h	SD_VENC Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
30	DVO2_INT2_ENA	R/W	0h	DVO2 Enabled Interrupt2 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
29	DVO2_INT1_ENA	R/W	0h	DVO2 Enabled Interrupt1 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
28	DVO2_INT0_ENA	R/W	0h	DVO2 Enabled Interrupt0 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA	R/W	0h	DVO1 Enabled Interrupt2 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
23	DVO1_INT1_ENA	R/W	0h	DVO1 Enabled Interrupt1 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
22	DVO1_INT0_ENA	R/W	0h	DVO1 Enabled Interrupt0 Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
21	VIP2_PARSER_INT_ENA	R/W	0h	VIP2 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
20	VIP1_PARSER_INT_ENA	R/W	0h	VIP1 Parser Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
19	Reserved	R	0h	

Table 1-196. intc_intr3_status_ena0 Register Field Descriptions (continued)

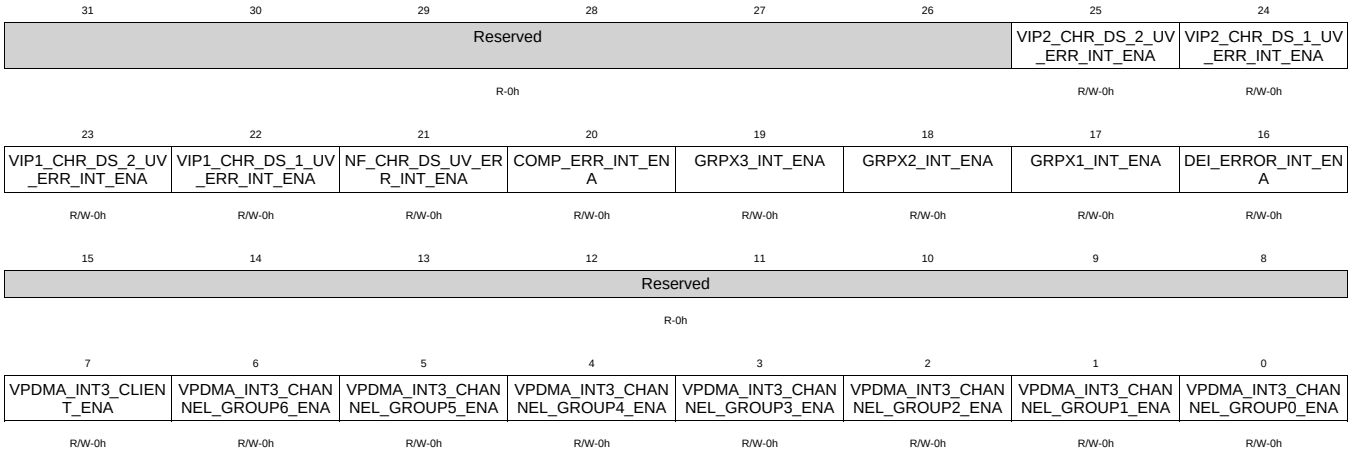
Bit	Field	Type	Reset	Description
18	DEI_FMD_INT_ENA	R/W	0h	DEI Film Mode Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	
16	VPDMA_INT3_DESCRIPTOR_ENA	R/W	0h	VPDMA INT0 Descriptor Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15	VPDMA_INT3_LIST7_NOTIFY_ENA	R/W	0h	VPDMA INT0 List7 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
14	VPDMA_INT3_LIST7_COMPLETE_ENA	R/W	0h	VPDMA INT0 List7 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
13	VPDMA_INT3_LIST6_NOTIFY_ENA	R/W	0h	VPDMA INT0 List6 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
12	VPDMA_INT3_LIST6_COMPLETE_ENA	R/W	0h	VPDMA INT0 List6 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
11	VPDMA_INT3_LIST5_NOTIFY_ENA	R/W	0h	VPDMA INT0 List5 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
10	VPDMA_INT3_LIST5_COMPLETE_ENA	R/W	0h	VPDMA INT0 List5 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
9	VPDMA_INT3_LIST4_NOTIFY_ENA	R/W	0h	VPDMA INT0 List4 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
8	VPDMA_INT3_LIST4_COMPLETE_ENA	R/W	0h	VPDMA INT0 List4 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
7	VPDMA_INT3_LIST3_NOTIFY_ENA	R/W	0h	VPDMA INT0 List3 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
6	VPDMA_INT3_LIST3_COMPLETE_ENA	R/W	0h	VPDMA INT0 List3 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT3_LIST2_NOTIFY_ENA	R/W	0h	VPDMA INT0 List2 Notify Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT3_LIST2_COMPLETE_ENA	R/W	0h	VPDMA INT0 List2 Complete Enabled Statust Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT3_LIST1_NOTIFY_ENA	R/W	0h	VPDMA INT0 List1 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT3_LIST1_COMPLETE_ENA	R/W	0h	VPDMA INT0 List1 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT3_LIST0_NOTIFY_ENA	R/W	0h	VPDMA INT0 List0 Notify Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT3_LIST0_COMPLETE_ENA	R/W	0h	VPDMA INT0 List0 Complete Enabled Status Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.30 intc_intr3_status_ena1 Register (offset = 8Ch) [reset = 0h]

intc_intr3_status_ena1 is shown in Figure 1-286 and described in Table 1-197.

Interrupt3 Enabled Register 1

Figure 1-286. intc_intr3_status_ena1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-197. intc_intr3_status_ena1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enabled Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
20	COMP_ERR_INT_ENA	R/W	0h	COMP Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
19	GRPX3_INT_ENA	R/W	0h	GRPX3 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
18	GRPX2_INT_ENA	R/W	0h	GRPX2 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
17	GRPX1_INT_ENA	R/W	0h	GRPX1 Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect
16	DEI_ERROR_INT_ENA	R/W	0h	DEI Error Enabled Interrupt Status Read indicates enabled status 0 = inactive 1 = active Writing 1 will clear interrupt Writing 0 has no effect

Table 1-197. intc_intr3_status_ena1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	
7	VPDMA_INT3_CLIENT_ENA	R/W	0h	VPDMA INT0 Client Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
6	VPDMA_INT3_CHANNEL_GROUP6_ENA	R/W	0h	VPDMA INT0 Channel Group6 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
5	VPDMA_INT3_CHANNEL_GROUP5_ENA	R/W	0h	VPDMA INT0 Channel Group5 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
4	VPDMA_INT3_CHANNEL_GROUP4_ENA	R/W	0h	VPDMA INT0 Channel Group4 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
3	VPDMA_INT3_CHANNEL_GROUP3_ENA	R/W	0h	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
2	VPDMA_INT3_CHANNEL_GROUP2_ENA	R/W	0h	VPDMA INT0 Channel Group3 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
1	VPDMA_INT3_CHANNEL_GROUP1_ENA	R/W	0h	VPDMA INT0 Channel Group1 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect
0	VPDMA_INT3_CHANNEL_GROUP0_ENA	R/W	0h	VPDMA INT0 Channel Group0 Enabled Status Read indicates raw status 0 = inactive 1 = active Writing 1 will set status Writing 0 has no effect

1.3.7.31 intc_intr3_ena_set0 Register (offset = 90h) [reset = 0h]

intc_intr3_ena_set0 is shown in Figure 1-287 and described in Table 1-198.

Interrupt3 Enable/Set Register 0

Figure 1-287. intc_intr3_ena_set0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA_SET	DVO2_INT2_ENA_SET	DVO2_INT1_ENA_SET	DVO2_INT0_ENA_SET	Reserved			DVO1_INT2_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA_SET	DVO1_INT0_ENA_SET	VIP2_PARSER_INT_ENA_SET	VIP1_PARSER_INT_ENA_SET	Reserved	DEI_FMD_INT_ENA_SET	Reserved	VPDMA_INT3_DESCRIPTOR_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT3_LIST7_NOTIFY_ENA_SET	VPDMA_INT3_LIST7_COMPLETE_ENA_SET	VPDMA_INT3_LIST6_NOTIFY_ENA_SET	VPDMA_INT3_LIST6_COMPLETE_ENA_SET	VPDMA_INT3_LIST5_NOTIFY_ENA_SET	VPDMA_INT3_LIST5_COMPLETE_ENA_SET	VPDMA_INT3_LIST4_NOTIFY_ENA_SET	VPDMA_INT3_LIST4_COMPLETE_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT3_LIST3_NOTIFY_ENA_SET	VPDMA_INT3_LIST3_COMPLETE_ENA_SET	VPDMA_INT3_LIST2_NOTIFY_ENA_SET	VPDMA_INT3_LIST2_COMPLETE_ENA_SET	VPDMA_INT3_LIST1_NOTIFY_ENA_SET	VPDMA_INT3_LIST1_COMPLETE_ENA_SET	VPDMA_INT3_LIST0_NOTIFY_ENA_SET	VPDMA_INT3_LIST0_COMPLETE_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-198. intc_intr3_ena_set0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA_SET	R/W	0h	SD_VENC Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
30	DVO2_INT2_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
29	DVO2_INT1_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
28	DVO2_INT0_ENA_SET	R/W	0h	DVO2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
23	DVO1_INT1_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
22	DVO1_INT0_ENA_SET	R/W	0h	DVO1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
21	VIP2_PARSER_INT_ENA_SET	R/W	0h	VIP2 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
20	VIP1_PARSER_INT_ENA_SET	R/W	0h	VIP1 Parser Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_ENA_SET	R/W	0h	DEI Film Mode Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	

Table 1-198. intc_intr3_ena_set0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VPDMA_INT3_DESCRIPTOR_ENA_SET	R/W	0h	VPDMA INT0 Descriptor Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15	VPDMA_INT3_LIST7_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List7 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
14	VPDMA_INT3_LIST7_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List7 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
13	VPDMA_INT3_LIST6_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List6 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
12	VPDMA_INT3_LIST6_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List6 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
11	VPDMA_INT3_LIST5_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List5 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
10	VPDMA_INT3_LIST5_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List5 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
9	VPDMA_INT3_LIST4_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List4 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
8	VPDMA_INT3_LIST4_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List4 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
7	VPDMA_INT3_LIST3_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List3 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
6	VPDMA_INT3_LIST3_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List3 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT3_LIST2_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List2 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT3_LIST2_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List2 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT3_LIST1_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List1 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT3_LIST1_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List1 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT3_LIST0_NOTIFY_ENA_SET	R/W	0h	VPDMA INT0 List0 Notify Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT3_LIST0_COMPLETE_ENA_SET	R/W	0h	VPDMA INT0 List0 Complete Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.32 intc_intr3_ena_set1 Register (offset = 94h) [reset = 0h]

intc_intr3_ena_set1 is shown in Figure 1-288 and described in Table 1-199.

Interrupt3 Enable/Set Register 1

Figure 1-288. intc_intr3_ena_set1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	NF_CHR_DS_UV_ERR_INT_ENA_SET	COMP_ERR_INT_ENA_SET	GRPX3_INT_ENA_SET	GRPX2_INT_ENA_SET	GRPX1_INT_ENA_SET	DEI_ERROR_INT_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT3_CLIENT_ENA_SET	VPDMA_INT3_CHANNEL_GROUP6_ENA_SET	VPDMA_INT3_CHANNEL_GROUP5_ENA_SET	VPDMA_INT3_CHANNEL_GROUP4_ENA_SET	VPDMA_INT3_CHANNEL_GROUP3_ENA_SET	VPDMA_INT3_CHANNEL_GROUP2_ENA_SET	VPDMA_INT3_CHANNEL_GROUP1_ENA_SET	VPDMA_INT3_CHANNEL_GROUP0_ENA_SET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-199. intc_intr3_ena_set1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_SET	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_SET	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_SET	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_SET	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA_SET	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
20	COMP_ERR_INT_ENA_SET	R/W	0h	COMP Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
19	GRPX3_INT_ENA_SET	R/W	0h	GRPX3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
18	GRPX2_INT_ENA_SET	R/W	0h	GRPX2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
17	GRPX1_INT_ENA_SET	R/W	0h	GRPX1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
16	DEI_ERROR_INT_ENA_SET	R/W	0h	DEI Error Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
15-8	Reserved	R	0h	
7	VPDMA_INT3_CLIENT_ENA_SET	R/W	0h	VPDMA INT0 Client Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

Table 1-199. intc_intr3_ena_set1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	VPDMA_INT3_CHANNEL_GROUP6_ENA_SET	R/W	0h	VPDMA INT0 Channel Group6 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
5	VPDMA_INT3_CHANNEL_GROUP5_ENA_SET	R/W	0h	VPDMA INT0 Channel Group5 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
4	VPDMA_INT3_CHANNEL_GROUP4_ENA_SET	R/W	0h	VPDMA INT0 Channel Group4 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
3	VPDMA_INT3_CHANNEL_GROUP3_ENA_SET	R/W	0h	VPDMA INT0 Channel Group3 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
2	VPDMA_INT3_CHANNEL_GROUP2_ENA_SET	R/W	0h	VPDMA INT0 Channel Group2 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
1	VPDMA_INT3_CHANNEL_GROUP1_ENA_SET	R/W	0h	VPDMA INT0 Channel Group1 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect
0	VPDMA_INT3_CHANNEL_GROUP0_ENA_SET	R/W	0h	VPDMA INT0 Channel Group0 Enable/Set Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will set interrupt enabled Writing 0 has no effect

1.3.7.33 intc_intr3_ena_clr0 Register (offset = 98h) [reset = 0h]

intc_intr3_ena_clr0 is shown in Figure 1-289 and described in Table 1-200.

Interrupt3 Enable/Clear Register 0

Figure 1-289. intc_intr3_ena_clr0 Register

31	30	29	28	27	26	25	24
SDVENC_INT_ENA_CLR	DVO2_INT2_ENA_CLR	DVO2_INT1_ENA_CLR	DVO2_INT0_ENA_CLR	Reserved			DVO1_INT2_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
DVO1_INT1_ENA_CLR	DVO1_INT0_ENA_CLR	VIP2_PARSER_INT_ENA_CLR	VIP1_PARSER_INT_ENA_CLR	Reserved	DEI_FMD_INT_ENA_CLR	Reserved	VPDMA_INT3_DESCRIPTOR_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
VPDMA_INT3_LIST7_NOTIFY_ENA_CLR	VPDMA_INT3_LIST7_COMPLETE_ENA_CLR	VPDMA_INT3_LIST6_NOTIFY_ENA_CLR	VPDMA_INT3_LIST6_COMPLETE_ENA_CLR	VPDMA_INT3_LIST5_NOTIFY_ENA_CLR	VPDMA_INT3_LIST5_COMPLETE_ENA_CLR	VPDMA_INT3_LIST4_NOTIFY_ENA_CLR	VPDMA_INT3_LIST4_COMPLETE_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
VPDMA_INT3_LIST3_NOTIFY_ENA_CLR	VPDMA_INT3_LIST3_COMPLETE_ENA_CLR	VPDMA_INT3_LIST2_NOTIFY_ENA_CLR	VPDMA_INT3_LIST2_COMPLETE_ENA_CLR	VPDMA_INT3_LIST1_NOTIFY_ENA_CLR	VPDMA_INT3_LIST1_COMPLETE_ENA_CLR	VPDMA_INT3_LIST0_NOTIFY_ENA_CLR	VPDMA_INT3_LIST0_COMPLETE_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-200. intc_intr3_ena_clr0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDVENC_INT_ENA_CLR	R/W	0h	SD_VENC Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
30	DVO2_INT2_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
29	DVO2_INT1_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
28	DVO2_INT0_ENA_CLR	R/W	0h	DVO2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
27-25	Reserved	R	0h	
24	DVO1_INT2_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
23	DVO1_INT1_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
22	DVO1_INT0_ENA_CLR	R/W	0h	DVO1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
21	VIP2_PARSER_INT_ENA_CLR	R/W	0h	VIP2 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
20	VIP1_PARSER_INT_ENA_CLR	R/W	0h	VIP1 Parser Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
19	Reserved	R	0h	
18	DEI_FMD_INT_ENA_CLR	R/W	0h	DEI Film Mode Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
17	Reserved	R	0h	

Table 1-200. intc_intr3_ena_clr0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VPDMA_INT3_DESCRIPTOR_ENA_CLR	R/W	0h	VPDMA INT0 Descriptor Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
15	VPDMA_INT3_LIST7_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List7 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
14	VPDMA_INT3_LIST7_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List7 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
13	VPDMA_INT3_LIST6_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List6 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
12	VPDMA_INT3_LIST6_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List6 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
11	VPDMA_INT3_LIST5_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List5 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
10	VPDMA_INT3_LIST5_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List5 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
9	VPDMA_INT3_LIST4_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List4 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
8	VPDMA_INT3_LIST4_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List4 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
7	VPDMA_INT3_LIST3_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List3 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
6	VPDMA_INT3_LIST3_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List3 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
5	VPDMA_INT3_LIST2_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List2 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
4	VPDMA_INT3_LIST2_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List2 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
3	VPDMA_INT3_LIST1_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List1 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
2	VPDMA_INT3_LIST1_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List1 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
1	VPDMA_INT3_LIST0_NOTIFY_ENA_CLR	R/W	0h	VPDMA INT0 List0 Notify Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
0	VPDMA_INT3_LIST0_COMPLETE_ENA_CLR	R/W	0h	VPDMA INT0 List0 Complete Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

1.3.7.34 intc_intr3_ena_clr1 Register (offset = 9Ch) [reset = 0h]

intc_intr3_ena_clr1 is shown in Figure 1-290 and described in Table 1-201.

Interrupt3 Enable/Clear Register 1

Figure 1-290. intc_intr3_ena_clr1 Register

31	30	29	28	27	26	25	24
Reserved						VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	NF_CHR_DS_UV_ERR_INT_ENA_CLR	COMP_ERR_INT_ENA_CLR	GRPX3_INT_ENA_CLR	GRPX2_INT_ENA_CLR	GRPX1_INT_ENA_CLR	DEI_ERROR_INT_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
VPDMA_INT3_CLIENT_ENA_CLR	VPDMA_INT3_CHANNEL_GROUP6_ENA_CLR	VPDMA_INT3_CHANNEL_GROUP5_ENA_CLR	VPDMA_INT3_CHANNEL_GROUP4_ENA_CLR	VPDMA_INT3_CHANNEL_GROUP3_ENA_CLR	VPDMA_INT3_CHANNEL_GROUP2_ENA_CLR	VPDMA_INT3_CHANNEL_GROUP1_ENA_CLR	VPDMA_INT3_CHANNEL_GROUP0_ENA_CLR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-201. intc_intr3_ena_clr1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	VIP2_CHR_DS_2_UV_ERR_INT_ENA_CLR	R/W	0h	VIP2 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
24	VIP2_CHR_DS_1_UV_ERR_INT_ENA_CLR	R/W	0h	VIP2 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
23	VIP1_CHR_DS_2_UV_ERR_INT_ENA_CLR	R/W	0h	VIP1 Chroma Downsampler 2 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
22	VIP1_CHR_DS_1_UV_ERR_INT_ENA_CLR	R/W	0h	VIP1 Chroma Downsampler 1 UV Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
21	NF_CHR_DS_UV_ERR_INT_ENA_CLR	R/W	0h	Noise Filter Chroma Downsampler UV error Interrupt Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
20	COMP_ERR_INT_ENA_CLR	R/W	0h	COMP Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
19	GRPX3_INT_ENA_CLR	R/W	0h	GRPX3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
18	GRPX2_INT_ENA_CLR	R/W	0h	GRPX2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
17	GRPX1_INT_ENA_CLR	R/W	0h	GRPX1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
16	DEI_ERROR_INT_ENA_CLR	R/W	0h	DEI Error Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

Table 1-201. intc_intr3_ena_clr1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	
7	VPDMA_INT3_CLIENT_ENA_CLR	R/W	0h	VPDMA INT0 Client Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
6	VPDMA_INT3_CHANNEL_GROUP6_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group6 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
5	VPDMA_INT3_CHANNEL_GROUP5_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group5 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
4	VPDMA_INT3_CHANNEL_GROUP4_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group4 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
3	VPDMA_INT3_CHANNEL_GROUP3_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group3 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
2	VPDMA_INT3_CHANNEL_GROUP2_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group2 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
1	VPDMA_INT3_CHANNEL_GROUP1_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group1 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect
0	VPDMA_INT3_CHANNEL_GROUP0_ENA_CLR	R/W	0h	VPDMA INT0 Channel Group0 Enable/Clear Read indicates interrupt enable 0 = disabled 1 = enabled Writing 1 will clear interrupt enabled Writing 0 has no effect

1.3.7.35 intc_eoi Register (offset = A0h) [reset = 0h]

intc_eoi is shown in Figure 1-291 and described in Table 1-202.

End of Interrupt Register

Figure 1-291. intc_eoi Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOI_VECTOR																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-202. intc_eoi Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EOI_VECTOR	R/W	0h	Number associated with the ipgenericirq for intr output. There are 4 interrupt outputs Write 0x0 : Write to intr0 IP Generic Write 0x1 : Write to intr1 IP Generic Write 0x2 : Write to intr2 IP Generic Write 0x3 : Write to intr3 IP Generic Any other write value is ignored.

1.3.7.36 clkc_clken Register (offset = 100h) [reset = 0h]

clkc_clken is shown in Figure 1-292 and described in Table 1-203.

Clock Enable Register

Figure 1-292. clkc_clken Register

31	30	29	28	27	26	25	24
Reserved							NF_DP_EN
R-0h							R/W-0h
23	22	21	20	19	18	17	16
Reserved						VIP2_DP_EN	VIP1_DP_EN
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
Reserved			SDVENC_EN	DVO2_EN	HDCOMP_EN	HDMI_DVO1_EN	IND_TRANS2_DP_EN
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
IND_TRANS1_DP_EN	COMP_DP_EN	GRPX3_DP_EN	GRPX2_DP_EN	GRPX1_DP_EN	AUX_DP_EN	PRIM_DP_EN	VPDMA_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-203. clkc_clken Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	Reserved	R	0h	
24	NF_DP_EN	R/W	0h	Noise Filter Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
23-18	Reserved	R	0h	
17	VIP2_DP_EN	R/W	0h	Video Input Port 2 Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
16	VIP1_DP_EN	R/W	0h	Video Input Port 1 Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
15-13	Reserved	R	0h	
12	SDVENC_EN	R/W	0h	SD VENC Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
11	DVO2_EN	R/W	0h	DVO2 VENC Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
10	HDCOMP_EN	R/W	0h	HDCOMP VENC Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
9	HDMI_DVO1_EN	R/W	0h	HDMI/DVO1 VENC Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
8	IND_TRANS2_DP_EN	R/W	0h	Independent Transcode 2 (to VIP1) Data Path Clock .. 1 = Clock Enabled.. 0 = Clock Disabled
7	IND_TRANS1_DP_EN	R/W	0h	Independent Transcode 1 (to VIP2) Data Path Clock .. 1 = Clock Enabled.. 0 = Clock Disabled
6	COMP_DP_EN	R/W	0h	Compositor Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
5	GRPX3_DP_EN	R/W	0h	Graphics 3 Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
4	GRPX2_DP_EN	R/W	0h	Graphics 2 Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
3	GRPX1_DP_EN	R/W	0h	Graphics 1 Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
2	AUX_DP_EN	R/W	0h	Auxiliary Video Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled

Table 1-203. clkc_clken Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PRIM_DP_EN	R/W	0h	Primary Video Data Path Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled
0	VPDMA_EN	R/W	0h	VPDMA Clock Enable.. 1 = Clock Enabled.. 0 = Clock Disabled

1.3.7.37 clkc_rst Register (offset = 104h) [reset = 0h]

clkc_rst is shown in Figure 1-293 and described in Table 1-204.

Soft Reset Register

Figure 1-293. clkc_rst Register

31	30	29	28	27	26	25	24
MAIN_RST	Reserved		VIP2_CHR_DS_2_RST	VIP1_CHR_DS_2_RST	VIP2_CHR_DS_1_RST	VIP1_CHR_DS_1_RST	NF_DP_RST
R-0h	R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
VIP2_SC_RST	VIP1_SC_RST	VIP2_CSC_RST	VIP1_CSC_RST	VIP2_VIP_RST	VIP1_VIP_RST	VIP2_DP_RST	VIP1_DP_RST
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
Reserved			SDVENC_RST	DVO2_RST	HDCOMP_RST	HDMI_DVO1_RST	IND_TRANS2_DP_RST
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
IND_TRANS1_DP_RST	COMP_DP_RST	GRPX3_DP_RST	GRPX2_DP_RST	GRPX1_DP_RST	AUX_DP_RST	PRIM_DP_RST	VPDMA_RST
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-204. clkc_rst Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAIN_RST	R/W	0h	Reset for all modules in DSS Main Data Path
30-29	Reserved	R	0h	Reserved
28	VIP2_CHR_DS_2_RST	R/W	0h	Video Input Port 2 CHR_DS 2 Reset 1 = Reset Enable 0 = Reset Disable
27	VIP1_CHR_DS_2_RST	R/W	0h	Video Input Port 1 CHR_DS 2 Reset 1 = Reset Enable 0 = Reset Disable
26	VIP2_CHR_DS_1_RST	R/W	0h	Video Input Port 2 CHR_DS 1 Reset 1 = Reset Enable 0 = Reset Disable
25	VIP1_CHR_DS_1_RST	R/W	0h	Video Input Port 1 CHR_DS 1 Reset 1 = Reset Enable 0 = Reset Disable
24	NF_DP_RST	R/W	0h	Noise Filter Data Path Reset 1 = Reset Enable 0 = Reset Disable
23	VIP2_SC_RST	R/W	0h	Video Input Port 2 Scaler Reset 1 = Reset Enable 0 = Reset Disable
22	VIP1_SC_RST	R/W	0h	Video Input Port 1 Scaler Reset 1 = Reset Enable 0 = Reset Disable
21	VIP2_CSC_RST	R/W	0h	Video Input Port 2 CSC Reset 1 = Reset Enable 0 = Reset Disable
20	VIP1_CSC_RST	R/W	0h	Video Input Port 1 CSC Reset 1 = Reset Enable 0 = Reset Disable
19	VIP2_VIP_RST	R/W	0h	Video Input Port 2 VIP_PARSER Reset 1 = Reset Enable 0 = Reset Disable
18	VIP1_VIP_RST	R/W	0h	Video Input Port 1 VIP_PARSER Reset 1 = Reset Enable 0 = Reset Disable
17	VIP2_DP_RST	R/W	0h	Video Input Port 2 Data Path Reset 1 = Reset Enable 0 = Reset Disable
16	VIP1_DP_RST	R/W	0h	Video Input Port 1 Data Path Reset 1 = Reset Enable 0 = Reset Disable
15-13	Reserved	R	0h	Reserved
12	SDVENC_RST	R/W	0h	SD Video Encoder/RF Modulator Reset 1 = Reset Enable 0 = Reset Disable
11	DVO2_RST	R/W	0h	DVO2 Video Encoder Reset 1 = Reset Enable 0 = Reset Disable
10	HDCOMP_RST	R/W	0h	HDCOMP (HD_VENC_A) Video Encoder Reset 1 = Reset Enable 0 = Reset Disable

Table 1-204. clkc_rst Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	HDMI_DVO1_RST	R/W	0h	HDMI/DVO1 Video Encoder Reset 1 = Reset Enable 0 = Reset Disable
8	IND_TRANS2_DP_RST	R/W	0h	Independent Transcode 2 (to VIP2) Data Path Reset 1 = Reset Enable 0 = Reset Disable
7	IND_TRANS1_DP_RST	R/W	0h	Independent Transcode 1 (to VIP1) Data Path Reset 1 = Reset Enable 0 = Reset Disable
6	COMP_DP_RST	R/W	0h	Compositor Data Path Reset 1 = Reset Enable 0 = Reset Disable
5	GRPX3_DP_RST	R/W	0h	Graphics 3 Data Path Reset 1 = Reset Enable 0 = Reset Disable
4	GRPX2_DP_RST	R/W	0h	Graphics 2 Data Path Reset 1 = Reset Enable 0 = Reset Disable
3	GRPX1_DP_RST	R/W	0h	Graphics 1 Data Path Reset 1 = Reset Enable 0 = Reset Disable
2	AUX_DP_RST	R/W	0h	Auxiliary Video Data Path Reset 1 = Reset Enable 0 = Reset Disable
1	PRIM_DP_RST	R/W	0h	Primary Video Data Path Reset 1 = Reset Enable 0 = Reset Disable
0	VPDMA_RST	R/W	0h	VPDMA Reset 1 = Reset Enable 0 = Reset Disable

1.3.7.38 clkc_dps Register (offset = 108h) [reset = 0h]

clkc_dps is shown in Figure 1-294 and described in Table 1-205.

Main Datapath Select Register

Figure 1-294. clkc_dps Register

31	30	29	28	27	26	25	24
MAIN_DATAPATH_SELECT				Reserved			
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
Reserved						NF_BYPASS_SELECT	Reserved
R-0h						R/W-0h	R-0h
15	14	13	12	11	10	9	8
Reserved	IND_TRANS2_SELECT	IND_TRANS1_SELECT	Reserved	SC_M_WRBK_SELECT			SDVENC_SELECT
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
SDVENC_SELECT		HDCOMP_DVO2_SELECT			VCOMP_MAIN_DISABLE	VCOMP_PIP_SELECT	
R/W-0h		R/W-0h			R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-205. clkc_dps Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	MAIN_DATAPATH_SELECT	R/W	0h	Main Datapath Register Field Enable 0000 : All fields written 0001 : Only vcomp_pip_select written 0010 : Only vcomp_main_disable written 0011 : Only hdcomp_dvo2_select written 0100 : Only sdvenc_select written 0101 : Only sc_m_wrbk_select written 0110 : Only ind_trans1_select written 0111 : Only ind_trans2_select written 1000 : Only comp_decomp_hq_bypass written 1001 : Only comp_decomp_lc_bypass written 1010 : Only nf_bypass_select written 1011 : Reserved 1100 : Reserved 1101 : Reserved 1110 : Reserved 1111 : Reserved
27-18	Reserved	R	0h	
17	NF_BYPASS_SELECT	R/W	0h	Noise Filter Bypass. 0 : Noise Filter Selected 1 : Noise Filter Bypassed If Noise Filter is bypassed.. 422 Private Data Store data is chroma downsampled and written back out as 420 Tiled Data.
16-15	Reserved	R	0h	
14	IND_TRANS2_SELECT	R/W	0h	Independent Transcode Path Select 0 : DEI_H Path selected for VIP1 Scaler Output 1 : Independent Transcode Path2 selected for VIP2 Scaler Output
13	IND_TRANS1_SELECT	R/W	0h	Independent Transcode Path Select 0 : DEI Path selected for VIP2 Scaler Output 1 : Independent Transcode Path1 selected for VIP1 Scaler Output

Table 1-205. clkc_dps Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	Reserved	R	0h	
11-9	SC_M_WRBK_SELECT	R/W	0h	SC_M_WRBK Path Select 000 : Path Disabled 001 : HDMI Composited Path Input (from COMP) 010 : EDE Path Input (from EDE) 011 : VCOMP Path Input (from VCOMP) 100 : Auxiliary (PIP) Memory Input (from VPDMA) 101 : Primary (HQ) Memory Input (from VPDMA) 110 : Reserved 111 : Reserved
8-6	SDVENC_SELECT	R/W	0h	SD VENC Path Select 000 : Path Disabled 001 : Auxiliary (PIP) Path Input (from SC_M) 010 : Auxiliary (PIP) Memory Input (from VPDMA) 011 : Primary (HQ) Memory Input (from VPDMA) 100 : Independent Transcode Input (from Independent Transcode) 101 : Reserved 110 : Reserved 111 : Reserved
5-3	HDCOMP_DVO2_SELECT	R/W	0h	HDCOMP/DVO2 Path Input Select 000 : Path Disabled 001 : Auxiliary (PIP) Path Input (from SC_M) 010 : Auxiliary (PIP) Memory Input (from VPDMA) 011 : Primary (HQ) Memory Input (from VPDMA) 100 : Reserved 101 : Reserved 110 : Reserved 111 : Reserved
2	VCOMP_MAIN_DISABLE	R/W	0h	VCOMP Main Input Disable (drives main VENC) 0 : Path Enabled 1 : Path Disabled If VCOMP Main Input is disabled.. the VCOMP will not receive input from the main path. Upstream paths would be allowed to run (transcode.. memory to memory). Disabling this input implies VCOMP will not be internally configured to use this input.
1-0	VCOMP_PIP_SELECT	R/W	0h	VCOMP PIP Input Select (drives main VENC) 00 : Path Disabled 01 : Auxiliary (PIP) Path Input (from SC_M) 10 : Auxiliary (PIP) Memory Input (from VPDMA) 11 : Primary (HQ) Memory Input (from VPDMA)

1.3.7.39 clkc_vip1dps Register (offset = 10Ch) [reset = 0h]

clkc_vip1dps is shown in Figure 1-295 and described in Table 1-206.

VIP1 Datapath Select Register

Figure 1-295. clkc_vip1dps Register

31	30	29	28	27	26	25	24
VIP1_DATAPATH_SELECT				Reserved			
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
Reserved						VIP1_CHR_DS_2_BYPASS	VIP1_CHR_DS_1_BYPASS
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
VIP1_MULTI_CHANNEL_SELECT	VIP1_CHR_DS_2_SRC_SELECT			VIP1_CHR_DS_1_SRC_SELECT			VIP1_RGB_OUT_HI_SELECT
R/W-0h	R/W-0h			R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
VIP1_RGB_OUT_LO_SELECT	VIP1_RGB_SRC_SELECT	VIP1_SC_SRC_SELECT			VIP1_CSC_SRC_SELECT		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-206. clkc_vip1dps Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	VIP1_DATAPATH_SELECT	R/W	0h	VIP1 Datapath Register Field Enable 0000 : All fields written 0001 : Only vip1_csc_src_select written 0010 : Only vip1_sc_src_select written 0011 : Only vip1_rgb_src_select written 0100 : Only vip1_rgb_out_lo_select written 0101 : Only vip1_rgb_out_hi_select written 0110 : Only vip1_chr_ds_1_src_select written 0111 : Only vip1_chr_ds_2_src_select written 1000 : Only vip1_multi_channel_select written 1001 : Only vip1_chr_ds_1_bypass written 1010 : Only vip1_chr_ds_2_bypass written 1011 : Reserved 1100 : Reserved 1101 : Reserved 1110 : Reserved 1111 : Reserved
27-18	Reserved	R	0h	
17	VIP1_CHR_DS_2_BYPASS	R/W	0h	Video Input Port 1 Chroma Downsampler 2 Bypass 0 : VIP Chroma Downsampler 1 selected 1 : VIP Chroma Downsampler 1 Bypassed Chroma Downsampler Bypassed means the output format from the VIP will be 422 data. Selected means the output format will be 420
16	VIP1_CHR_DS_1_BYPASS	R/W	0h	Video Input Port 1 Chroma Downsampler 1 Bypass 0 : VIP Chroma Downsampler 1 selected 1 : VIP Chroma Downsampler 1 Bypassed Chroma Downsampler Bypassed means the output format from the VIP will be 422 data. Selected means the output format will be 420

Table 1-206. clkc_vip1dps Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	VIP1_MULTI_CHANNEL_SELECT	R/W	0h	Video Input Port 1 Multi Channel Select 0 : VIP_PARSER A and B channels operate in single channel mode 1 : VIP_PARSER A and B channels directly drive VPDMA (multi-channel case) Multi-Channel means that the A and B sources are from multiple channels and used in a multiplexed stream mode. The VIP Parser extracts the channel ID from each source and outputs this information to VPDMA.. and thus to memory. When operating in a multiplexed stream mode.. this bit must be set to 1 to enable the channel information to be passed to memory. If this is not set.. the channel number (or source number) will be 0 for all streams. If vip1_rgb_out_select = 1.. then VIP_PARSER A port is connected to VPDMA
14-12	VIP1_CHR_DS_2_SRC_SELECT	R/W	0h	Video Input Port 1 Chroma Downsampler 2 Source Select 000 : Path Disabled (no input to CHR_DS) 001 : Source from Scaler (SC_M) 010 : Source from Color Space Converter (CSC) 011 : Source from VIP_PARSER A port 100 : Source from VIP_PARSER B port 101 : Source from Transcode (422) 110 : Reserved 111 : Reserved
11-9	VIP1_CHR_DS_1_SRC_SELECT	R/W	0h	Video Input Port 1 Chroma Downsampler 1 Source Select 000 : Path Disabled (no input to CHR_DS) 001 : Source from Scaler (SC_M) 010 : Source from Color Space Converter (CSC) 011 : Source from VIP_PARSER A port 100 : Source from VIP_PARSER B port 101 : Source from Transcode (422) 110 : Reserved 111 : Reserved
8	VIP1_RGB_OUT_HI_SELECT	R/W	0h	Video Input Port 1 HI RGB Output Select 0 : Output Type is 420/422 1 : Output Type is RGB
7	VIP1_RGB_OUT_LO_SELECT	R/W	0h	Video Input Port 1 LO RGB Output Select 0 : Output Type is 420/422 1 : Output Type is RGB
6	VIP1_RGB_SRC_SELECT	R/W	0h	Video Input Port 1 RGB Output Path Select 0 : Source from Compositor RGB input 1 : Source from CSC
5-3	VIP1_SC_SRC_SELECT	R/W	0h	Video Input Port 1 SC_M Source Select 000 : Path Disabled 001 : Source from Color Space Converter (CSC) 010 : Source from VIP_PARSER A port 011 : Source from VIP_PARSER B port 100 : Source from Transcode (422) 101 : Reserved 110 : Reserved 111 : Reserved

Table 1-206. clkc_vip1dps Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	VIP1_CSC_SRC_SELECT	R/W	0h	Video Input Port 1 CSC Source Select 000 : Path Disabled 001 : Source from VIP_PARSER A (422) port 010 : Source from VIP_PARSER B port 011 : Source from Transcode (422) 100 : Source from VIP_PARSER A (RGB) port 101 : Source from Compositor (RGB) 110 : Reserved 111 : Reserved

1.3.7.40 clkc_vip2dps Register (offset = 110h) [reset = 0h]

clkc_vip2dps is shown in Figure 1-296 and described in Table 1-207.

VIP2 Datapath Select Register

Figure 1-296. clkc_vip2dps Register

31	30	29	28	27	26	25	24
VIP2_DATAPATH_SELECT				Reserved			
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
Reserved						VIP2_CHR_DS_2_BYPASS	VIP2_CHR_DS_1_BYPASS
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
VIP2_MULTI_CHANNEL_SELECT	VIP2_CHR_DS_2_SRC_SELECT			VIP2_CHR_DS_1_SRC_SELECT			VIP2_RGB_OUT_HI_SELECT
R/W-0h	R/W-0h			R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
VIP2_RGB_OUT_LO_SELECT	VIP2_RGB_SRC_SELECT	VIP2_SC_SRC_SELECT			VIP2_CSC_SRC_SELECT		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-207. clkc_vip2dps Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	VIP2_DATAPATH_SELECT	R/W	0h	VIP2 Datapath Register Field Enable 0000 : All fields written 0001 : Only vip2_csc_src_select written 0010 : Only vip2_sc_src_select written 0011 : Only vip2_rgb_src_select written 0100 : Only vip2_rgb_out_lo_select written 0101 : Only vip2_rgb_out_hi_select written 0110 : Only vip2_chr_ds_1_src_select written 0111 : Only vip2_chr_ds_2_src_select written 1000 : Only vip2_multi_channel_select written 1001 : Only vip2_chr_ds_1_bypass written 1010 : Only vip2_chr_ds_2_bypass written 1011 : Reserved 1100 : Reserved 1101 : Reserved 1110 : Reserved 1111 : Reserved
27-18	Reserved	R	0h	
17	VIP2_CHR_DS_2_BYPASS	R/W	0h	Video Input Port 2 Chroma Downsampler 2 Bypass 0 : VIP Chroma Downsampler 1 selected 1 : VIP Chroma Downsampler 1 Bypassed Chroma Downsampler Bypassed means the output format from the VIP will be 422 data. Selected means the output format will be 420
16	VIP2_CHR_DS_1_BYPASS	R/W	0h	Video Input Port 2 Chroma Downsampler 1 Bypass 0 : VIP Chroma Downsampler 1 selected 1 : VIP Chroma Downsampler 1 Bypassed Chroma Downsampler Bypassed means the output format from the VIP will be 422 data. Selected means the output format will be 420

Table 1-207. clkc_vip2dps Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	VIP2_MULTI_CHANNEL_SELECT	R/W	0h	Video Input Port 2 Multi Channel Select 0 : VIP_PARSER A and B channels operate in single channel mode 1 : VIP_PARSER A and B channels directly drive VPDMA (multi-channel case) Multi-Channel means that the A and B sources are from multiple channels and used in a multiplexed stream mode. The VIP Parser extracts the channel ID from each source and outputs this information to VPDMA.. and thus to memory. When operating in a multiplexed stream mode.. this bit must be set to 1 to enable the channel information to be passed to memory. If this is not set.. the channel number (or source number) will be 0 for all streams. If vip2_rgb_out_select = 1.. then VIP_PARSER A port is connected to VPDMA
14-12	VIP2_CHR_DS_2_SRC_SELECT	R/W	0h	Video Input Port 2 Chroma Downsampler 2 Source Select 000 : Path Disabled (no input to CHR_DS) 001 : Source from Scaler (SC_M) 010 : Source from Color Space Converter (CSC) 011 : Source from VIP_PARSER A port 100 : Source from VIP_PARSER B port 101 : Source from Transcode (422) 110 : Reserved 111 : Reserved
11-9	VIP2_CHR_DS_1_SRC_SELECT	R/W	0h	Video Input Port 2 Chroma Downsampler 1 Source Select 000 : Path Disabled (no input to CHR_DS) 001 : Source from Scaler (SC_M) 010 : Source from Color Space Converter (CSC) 011 : Source from VIP_PARSER A port 100 : Source from VIP_PARSER B port 101 : Source from Transcode (422) 110 : Reserved 111 : Reserved
8	VIP2_RGB_OUT_HI_SELECT	R/W	0h	Video Input Port 2 HI RGB Output Select 0 : Output Type is 420/422 1 : Output Type is RGB
7	VIP2_RGB_OUT_LO_SELECT	R/W	0h	Video Input Port 2 LO RGB Output Select 0 : Output Type is 420/422 1 : Output Type is RGB
6	VIP2_RGB_SRC_SELECT	R/W	0h	Video Input Port 2 RGB Output Path Select 0 : Source from Compositor RGB input 1 : Source from CSC
5-3	VIP2_SC_SRC_SELECT	R/W	0h	Video Input Port 2 SC_M Source Select 000 : Path Disabled 001 : Source from Color Space Converter (CSC) 010 : Source from VIP_PARSER A port 011 : Source from VIP_PARSER B port 100 : Source from Transcode (422) 101 : Reserved 110 : Reserved 111 : Reserved

Table 1-207. clkc_vip2dps Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	VIP2_CSC_SRC_SELECT	R/W	0h	Video Input Port 2 CSC Source Select 000 : Path Disabled 001 : Source from VIP_PARSER A (422) port 010 : Source from VIP_PARSER B port 011 : Source from Transcode (422) 100 : Source from VIP_PARSER A (RGB) port 101 : Source from Compositor (RGB) 110 : Reserved 111 : Reserved

1.3.7.41 clkc_venc_clksel Register (offset = 114h) [reset = 0h]

clkc_venc_clksel is shown in Figure 1-297 and described in Table 1-208.

VENC Clock Select Register

Figure 1-297. clkc_venc_clksel Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved				DVO2_CLK_ON	DVO2_CLK_SELECT	Reserved	HD_VENC_G_CLK1X_SELECT
R-0h				R/W-0h	R/W-0h	R-0h	R/W-0h

15	14	13	12	11	10	9	8
Reserved						VBI_HD_CLK_SELECT	HD_VENC_A_CLK1X_SELECT
R-0h						R/W-0	R/W-0

7	6	5	4	3	2	1	0
Reserved				HDMI_CLK_ON	DVO1_CLK_ON	DVO1_CLK_SELECT	HD_VENC_D_CLK1X_SELECT
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-208. clkc_venc_clksel Register Field Descriptions

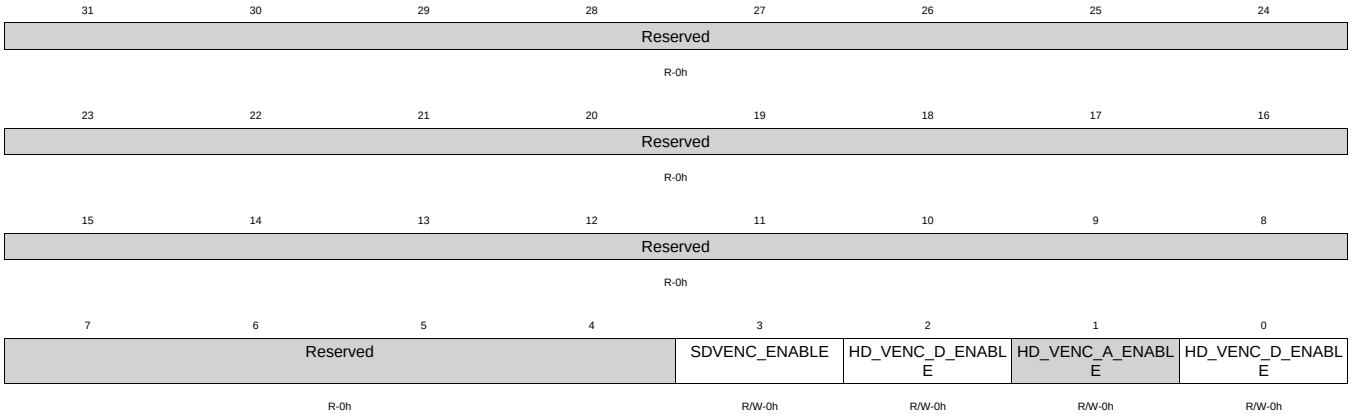
Bit	Field	Type	Reset	Description
31-20	Reserved	R	0h	Reserved
19	DVO2_CLK_ON	R/W	0h	Digital Video Output 2 output clock on 0 : DVO2 output clock is off (0) 1 : DVO2 output clock is on
18	DVO2_CLK_SELECT	R/W	0h	Digital Video Output 2 output clock 0 : hd_venc_a_clk 1 : hd_venc_a_clk/2
17	Reserved	R	0h	Reserved
16	HD_VENC_G_CLK1X_SELECT	R/W	0h	Digital Video Output 2 Clock 2x Select 0 : hd_venc_d_clk/2 1 : hd_venc_a_clk/2
15-10	Reserved	R	0h	Reserved
9	VBI_HD_CLK_SELECT	R/W	0h	VBI HD Clock Select 0: HD_VENC_A VBI clk=hdcomp_clk 1: HD_VENC_A VBI clk=hdcomp_clk /2
8	HD_VENC_A_CLK1X_SELECT	R/W	0h	HD_VENC_A clk1x source clock 0: hdcomp_clk/2 1: hdcomp_clk
7-4	Reserved	R	0h	Reserved
3	HDMI_CLK_ON	R/W	0h	HDMI output clock on 0 : HDMI output clock is off (0) 1 : HDMI output clock is on
2	DVO1_CLK_ON	R/W	0h	Digital Video Output 1 output clock on 0 : DVO1 output clock is off (0) 1 : DVO1 output clock is on
1	DVO1_CLK_SELECT	R/W	0h	Digital Video Output 1 output clock 0 : hd_venc_d_clk 1 : hd_venc_d_clk/2
0	HD_VENC_D_CLK1X_SELECT	R/W	0h	HD_VENC_D_DVO1 clk1x source clock 0 : hd_venc_d_clk/2 1 : hd_venc_d_clk

1.3.7.42 clkc_venc_ena Register (offset = 118h) [reset = 0h]

clkc_venc_ena is shown in Figure 1-298 and described in Table 1-209.

VENC Enable Register

Figure 1-298. clkc_venc_ena Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-209. clkc_venc_ena Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	Reserved	R	0h	
3	SDVENC_ENABLE	R/W	0h	SD VENC Enable 0 : Disabled 1 : Enabled
2	HD_VENC_D_ENABLE	R/W	0h	Digital Video Output 2 VENC Enable 0 : Disabled 1 : Enabled
1	HD_VENC_A_ENABLE	R/W	0h	HDCOMP VENC Enable 0 : Disabled 1 : Enabled
0	HD_VENC_D_ENABLE	R/W	0h	HDMI/Digital Video Output 1 VENC Enable 0 : Disabled 1 : Enabled

1.3.7.43 clkc_range_map Register (offset = 11Ch) [reset = 0h]

clkc_range_map is shown in Figure 1-299 and described in Table 1-210.

VC1 Range Map Register

Figure 1-299. clkc_range_map Register

31	30	29	28	27	26	25	24
RANGE_REDUCTION_IND2_ON	RANGE_REDUCTION_IND1_ON	RANGE_REDUCTION_AUX_ON	RANGE_REDUCTION_PRIM_ON	RANGE_MAP_IND2_ON	RANGE_MAPUV_IND2		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
23	22	21	20	19	18	17	16
RANGE_MAPY_IND2			RANGE_MAP_IND1_ON	RANGE_MAPUV_IND1			RANGE_MAPY_IND1
R/W-0h			R/W-0h	R/W-0h			R/W-0h
15	14	13	12	11	10	9	8
RANGE_MAPY_IND1		RANGE_MAP_AUX_ON	RANGE_MAPUV_AUX			RANGE_MAPY_AUX	
R/W-0h		R/W-0h	R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
RANGE_MAPY_AUX	RANGE_MAP_PRIM_ON	RANGE_MAPUV_PRIM			RANGE_MAPY_PRIM		
R/W-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-210. clkc_range_map Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE_REDUCTION_IND2_ON	R/W	0h	Range Reduction ON for IND2 transcode input
30	RANGE_REDUCTION_IND1_ON	R/W	0h	Range Reduction ON for IND1 transcode input
29	RANGE_REDUCTION_AUX_ON	R/W	0h	Range Reduction ON for Auxiliary input
28	RANGE_REDUCTION_PRIM_ON	R/W	0h	Range Reduction ON for Primary input
27	RANGE_MAP_IND2_ON	R/W	0h	Range Mapping ON for IND2 transcode input
26-24	RANGE_MAPUV_IND2	R/W	0h	Range Map UV for IND2 transcode input
23-21	RANGE_MAPY_IND2	R/W	0h	Range Map Y for IND2 transcode input
20	RANGE_MAP_IND1_ON	R/W	0h	Range Mapping ON for IND1 transcode input
19-17	RANGE_MAPUV_IND1	R/W	0h	Range Map UV for IND1 transcode input
16-14	RANGE_MAPY_IND1	R/W	0h	Range Map Y for IND1 transcode input
13	RANGE_MAP_AUX_ON	R/W	0h	Range Mapping ON for Auxiliary input
12-10	RANGE_MAPUV_AUX	R/W	0h	Range Map UV for Auxiliary input
9-7	RANGE_MAPY_AUX	R/W	0h	Range Map Y for Auxiliary input
6	RANGE_MAP_PRIM_ON	R/W	0h	Range Mapping ON for Primary input
5-3	RANGE_MAPUV_PRIM	R/W	0h	Range Map UV for Primary input
2-0	RANGE_MAPY_PRIM	R/W	0h	Range Map Y for Primary input

1.3.7.44 clkc_underflow Register (offset = 120h) [reset = 0h]

clkc_underflow is shown in Figure 1-300 and described in Table 1-211.

VENC Underflow Status Register

Figure 1-300. clkc_underflow Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved				SD_UNDERFLOW_STAT	DVO2_UNDERFLOW_STAT	HDCOMP_UNDERFLOW_STAT	HDMI_UNDERFLOW_STAT
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-211. clkc_underflow Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	Reserved	R	0h	
3	SD_UNDERFLOW_STAT	R/W	0h	SD VENC Underflow status Read 1 : SD Underflow Read 0 : SD NOT Underflow Write 1 to clear
2	DVO2_UNDERFLOW_STAT	R/W	0h	DVO2 VENC Underflow status Read 1 : DVO2 Underflow Read 0 : DVO2 NOT Underflow Write 1 to clear
1	HDCOMP_UNDERFLOW_STAT	R/W	0h	HDCOMP VENC Underflow status Read 1 : HDCOMP AT Underflow Read 0 : HDCOMP NOT Underflow Write 1 to clear
0	HDMI_UNDERFLOW_STAT	R/W	0h	HDMI/DVO1 VENC Underflow status Read 1 : HDMI/DVO1 Underflow Read 0 : HDMI/DVO1 NOT Underflow Write 1 to clear

1.3.8 VPDMA Registers

Table 1-212 lists the memory-mapped registers for the VPDMA. All register offset addresses not listed in Table 1-212 should be considered as reserved locations and the register contents should not be modified.

Table 1-212. VPDMA REGISTERS

Offset	Acronym	Register Name	Section
0h	VPDMA_pid	VPDMA Peripheral ID Register	Section 1.3.8.1
4h	VPDMA_list_addr	VPDMA List Address Register	Section 1.3.8.2
8h	VPDMA_list_attr	VPDMA List Attribute Register	Section 1.3.8.3
Ch	VPDMA_list_stat_sync	VPDMA List Status Register	Section 1.3.8.4
10h	VPDMA_vpi_ctl_address	VPDMA VPI Control Address Register (Reserved)	Section 1.3.8.5
14h	VPDMA_vpi_ctl_data	VPDMA VPI Control Data Register (Reserved)	Section 1.3.8.6
18h	VPDMA_bg_rgb	VPDMA Background RGB Register	Section 1.3.8.7
1Ch	VPDMA_bg_yuv	VPDMA Background YUV Register	Section 1.3.8.8
20h	VPDMA_descriptor_top	Reserved	Section 1.3.8.9
24h	VPDMA_descriptor_bottom	Reserved	Section 1.3.8.10
28h	VPDMA_current_descriptor	Reserved	Section 1.3.8.11
2Ch	VPDMA_descriptor_status_control	Reserved	Section 1.3.8.12
40h	VPDMA_int0_channel0_int_stat	VPDMA Interrupt 0 Channel 0 Status Register	Section 1.3.8.13
44h	VPDMA_int0_channel0_int_mask	VPDMA Interrupt 0 Channel 0 Mask Register	Section 1.3.8.14
48h	VPDMA_int0_channel1_int_stat	VPDMA Interrupt 0 Channel 1 Status Register	Section 1.3.8.15
4Ch	VPDMA_int0_channel1_int_mask	VPDMA Interrupt 0 Channel 1 Mask Register	Section 1.3.8.16
50h	VPDMA_int0_channel2_int_stat	VPDMA Interrupt 0 Channel 2 Status Register	Section 1.3.8.17
54h	VPDMA_int0_channel2_int_mask	VPDMA Interrupt 0 Channel 2 Mask Register	Section 1.3.8.18
58h	VPDMA_int0_channel3_int_stat	VPDMA Interrupt 0 Channel 3 Status Register	Section 1.3.8.19
5Ch	VPDMA_int0_channel3_int_mask	VPDMA Interrupt 0 Channel 3 Mask Register	Section 1.3.8.20
60h	VPDMA_int0_channel4_int_stat	VPDMA Interrupt 0 Channel 4 Status Register	Section 1.3.8.21
64h	VPDMA_int0_channel4_int_mask	VPDMA Interrupt 0 Channel 4 Mask Register	Section 1.3.8.22
68h	VPDMA_int0_channel5_int_stat	VPDMA Interrupt 0 Channel 5 Status Register	Section 1.3.8.23
6Ch	VPDMA_int0_channel5_int_mask	VPDMA Interrupt 0 Channel 5 Mask Register	Section 1.3.8.24
70h	VPDMA_int0_channel6_int_stat	VPDMA Interrupt 0 Channel 6 Status Register	Section 1.3.8.25
74h	VPDMA_int0_channel6_int_mask	VPDMA Interrupt 0 Channel 6 Mask Register	Section 1.3.8.26
78h	VPDMA_int0_client0_int_stat	VPDMA Interrupt 0 Client 0 Status Register	Section 1.3.8.27
7Ch	VPDMA_int0_client0_int_mask	VPDMA Interrupt 0 Client 0 Mask Register	Section 1.3.8.28
80h	VPDMA_int0_client1_int_stat	VPDMA Interrupt 0 Client 1 Status Register	Section 1.3.8.29
84h	VPDMA_int0_client1_int_mask	VPDMA Interrupt 0 Client 1 Mask Register	Section 1.3.8.30
88h	VPDMA_int0_list0_int_stat	VPDMA Interrupt 0 List 0 Status Register	Section 1.3.8.31
8Ch	VPDMA_int0_list0_int_mask	VPDMA Interrupt 0 List 0 Mask Register	Section 1.3.8.32
90h	VPDMA_int1_channel0_int_stat	VPDMA Interrupt 1 Channel 0 Status Register	Section 1.3.8.33
94h	VPDMA_int1_channel0_int_mask	VPDMA Interrupt 1 Channel 0 Mask Register	Section 1.3.8.34
98h	VPDMA_int1_channel1_int_stat	VPDMA Interrupt 1 Channel 1 Status Register	Section 1.3.8.35
9Ch	VPDMA_int1_channel1_int_mask	VPDMA Interrupt 1 Channel 1 Mask Register	Section 1.3.8.36
A0h	VPDMA_int1_channel2_int_stat	VPDMA Interrupt 1 Channel 2 Status Register	Section 1.3.8.37
A4h	VPDMA_int1_channel2_int_mask	VPDMA Interrupt 1 Channel 2 Mask Register	Section 1.3.8.38
A8h	VPDMA_int1_channel3_int_stat	VPDMA Interrupt 1 Channel 3 Status Register	Section 1.3.8.39
ACh	VPDMA_int1_channel3_int_mask	VPDMA Interrupt 1 Channel 3 Mask Register	Section 1.3.8.40
B0h	VPDMA_int1_channel4_int_stat	VPDMA Interrupt 1 Channel 4 Status Register	Section 1.3.8.41
B4h	VPDMA_int1_channel4_int_mask	VPDMA Interrupt 1 Channel 4 Mask Register	Section 1.3.8.42
B8h	VPDMA_int1_channel5_int_stat	VPDMA Interrupt 1 Channel 5 Status Register	Section 1.3.8.43
BCh	VPDMA_int1_channel5_int_mask	VPDMA Interrupt 1 Channel 5 Mask Register	Section 1.3.8.44

Table 1-212. VPDMA REGISTERS (continued)

Offset	Acronym	Register Name	Section
C0h	VPDMA_int1_channel6_int_stat	VPDMA Interrupt 1 Channel 6 Status Register	Section 1.3.8.45
C4h	VPDMA_int1_channel6_int_mask	VPDMA Interrupt 1 Channel 6 Mask Register	Section 1.3.8.46
C8h	VPDMA_int1_client0_int_stat	VPDMA Interrupt 1 Client 0 Status Register	Section 1.3.8.47
CCh	VPDMA_int1_client0_int_mask	VPDMA Interrupt 1 Client 0 Mask Register	Section 1.3.8.48
D0h	VPDMA_int1_client1_int_stat	VPDMA Interrupt 1 Client 1 Status Register	Section 1.3.8.49
D4h	VPDMA_int1_client1_int_mask	VPDMA Interrupt 1 Client 1 Mask Register	Section 1.3.8.50
D8h	VPDMA_int1_list0_int_stat	VPDMA Interrupt 1 List 0 Status Register	Section 1.3.8.51
DCh	VPDMA_int1_list0_int_mask	VPDMA Interrupt 1 List 0 Mask Register	Section 1.3.8.52
E0h	VPDMA_int2_channel0_int_stat	VPDMA Interrupt 2 Channel 0 Status Register	Section 1.3.8.53
E4h	VPDMA_int2_channel0_int_mask	VPDMA Interrupt 2 Channel 0 Mask Register	Section 1.3.8.54
E8h	VPDMA_int2_channel1_int_stat	VPDMA Interrupt 2 Channel 1 Status Register	Section 1.3.8.55
ECh	VPDMA_int2_channel1_int_mask	VPDMA Interrupt 2 Channel 1 Mask Register	Section 1.3.8.56
F0h	VPDMA_int2_channel2_int_stat	VPDMA Interrupt 2 Channel 2 Status Register	Section 1.3.8.57
F4h	VPDMA_int2_channel2_int_mask	VPDMA Interrupt 2 Channel 2 Mask Register	Section 1.3.8.58
F8h	VPDMA_int2_channel3_int_stat	VPDMA Interrupt 2 Channel 3 Status Register	Section 1.3.8.59
FCh	VPDMA_int2_channel3_int_mask	VPDMA Interrupt 2 Channel 3 Mask Register	Section 1.3.8.60
100h	VPDMA_int2_channel4_int_stat	VPDMA Interrupt 2 Channel 4 Status Register	Section 1.3.8.61
104h	VPDMA_int2_channel4_int_mask	VPDMA Interrupt 2 Channel 4 Mask Register	Section 1.3.8.62
108h	VPDMA_int2_channel5_int_stat	VPDMA Interrupt 2 Channel 5 Status Register	Section 1.3.8.63
10Ch	VPDMA_int2_channel5_int_mask	VPDMA Interrupt 2 Channel 5 Mask Register	Section 1.3.8.64
110h	VPDMA_int2_channel6_int_stat	VPDMA Interrupt 2 Channel 6 Status Register	Section 1.3.8.65
114h	VPDMA_int2_channel6_int_mask	VPDMA Interrupt 2 Channel 6 Mask Register	Section 1.3.8.66
118h	VPDMA_int2_client0_int_stat	VPDMA Interrupt 2 Client 0 Status Register	Section 1.3.8.67
11Ch	VPDMA_int2_client0_int_mask	VPDMA Interrupt 2 Client 0 Mask Register	Section 1.3.8.68
120h	VPDMA_int2_client1_int_stat	VPDMA Interrupt 2 Client 1 Status Register	Section 1.3.8.69
124h	VPDMA_int2_client1_int_mask	VPDMA Interrupt 2 Client 1 Mask Register	Section 1.3.8.70
128h	VPDMA_int2_list0_int_stat	VPDMA Interrupt 2 List 0 Status Register	Section 1.3.8.71
12Ch	VPDMA_int2_list0_int_mask	VPDMA Interrupt 2 List 0 Mask Register	Section 1.3.8.72
130h	VPDMA_int3_channel0_int_stat	VPDMA Interrupt 3 Channel 0 Status Register	Section 1.3.8.73
134h	VPDMA_int3_channel0_int_mask	VPDMA Interrupt 3 Channel 0 Mask Register	Section 1.3.8.74
138h	VPDMA_int3_channel1_int_stat	VPDMA Interrupt 3 Channel 1 Status Register	Section 1.3.8.75
13Ch	VPDMA_int3_channel1_int_mask	VPDMA Interrupt 3 Channel 1 Mask Register	Section 1.3.8.76
140h	VPDMA_int3_channel2_int_stat	VPDMA Interrupt 3 Channel 2 Status Register	Section 1.3.8.77
144h	VPDMA_int3_channel2_int_mask	VPDMA Interrupt 3 Channel 2 Mask Register	Section 1.3.8.78
148h	VPDMA_int3_channel3_int_stat	VPDMA Interrupt 3 Channel 3 Status Register	Section 1.3.8.79
14Ch	VPDMA_int3_channel3_int_mask	VPDMA Interrupt 3 Channel 3 Mask Register	Section 1.3.8.80
150h	VPDMA_int3_channel4_int_stat	VPDMA Interrupt 3 Channel 4 Status Register	Section 1.3.8.81
154h	VPDMA_int3_channel4_int_mask	VPDMA Interrupt 3 Channel 4 Mask Register	Section 1.3.8.82
158h	VPDMA_int3_channel5_int_stat	VPDMA Interrupt 3 Channel 5 Status Register	Section 1.3.8.83
15Ch	VPDMA_int3_channel5_int_mask	VPDMA Interrupt 3 Channel 5 Mask Register	Section 1.3.8.84
160h	VPDMA_int3_channel6_int_stat	VPDMA Interrupt 3 Channel 6 Status Register	Section 1.3.8.85
164h	VPDMA_int3_channel6_int_mask	VPDMA Interrupt 3 Channel 6 Mask Register	Section 1.3.8.86
168h	VPDMA_int3_client0_int_stat	VPDMA Interrupt 3 Client 0 Status Register	Section 1.3.8.87
16Ch	VPDMA_int3_client0_int_mask	VPDMA Interrupt 3 Client 0 Mask Register	Section 1.3.8.88
170h	VPDMA_int3_client1_int_stat	VPDMA Interrupt 3 Client 1 Status Register	Section 1.3.8.89
174h	VPDMA_int3_client1_int_mask	VPDMA Interrupt 3 Client 1 Mask Register	Section 1.3.8.90
178h	VPDMA_int3_list0_int_stat	VPDMA Interrupt 3 List 0 Status Register	Section 1.3.8.91

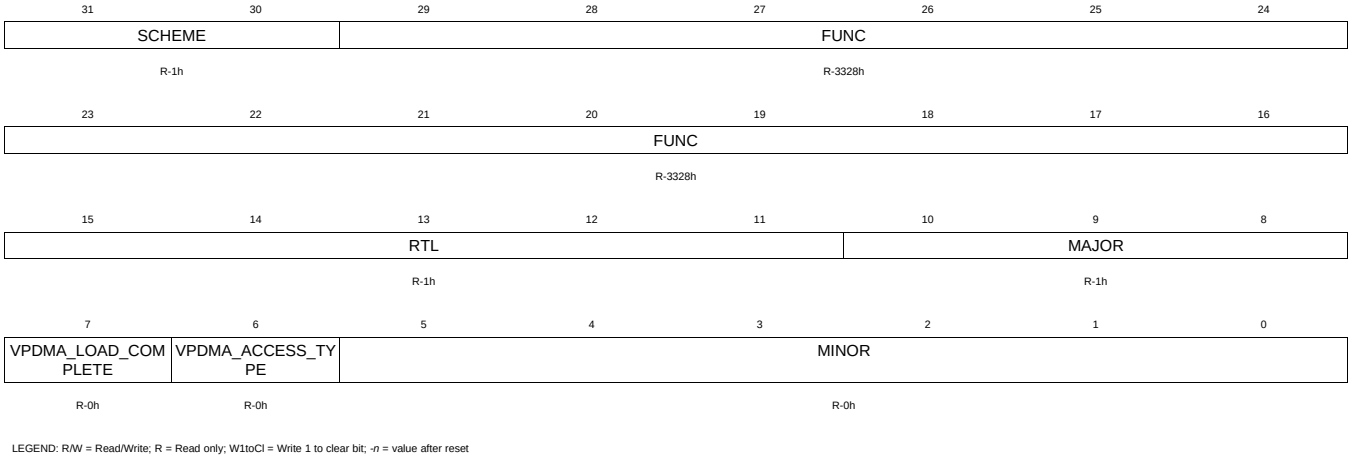
Table 1-212. VPDMA REGISTERS (continued)

Offset	Acronym	Register Name	Section
17Ch	VPDMA_int3_list0_int_mask	VPDMA Interrupt 3 List 0 Mask Register	Section 1.3.8.92
300h	VPDMA_dei_hq_1_chroma_cstat	VPDMA DEI Field 1 Chroma cstat	Section 1.3.8.93
304h	VPDMA_dei_hq_1_luma_cstat	VPDMA DEI Field 1 Luma cstat	Section 1.3.8.94
308h	VPDMA_dei_hq_2_luma_cstat	VPDMA DEI Field 2 Luma cstat	Section 1.3.8.95
30Ch	VPDMA_dei_hq_2_chroma_cstat	VPDMA DEI Field 2 Chroma cstat	Section 1.3.8.96
310h	VPDMA_dei_hq_3_luma_cstat	VPDMA DEI Field 3 Luma cstat	Section 1.3.8.97
314h	VPDMA_dei_hq_3_chroma_cstat	VPDMA DEI Field 3 Chroma cstat	Section 1.3.8.98
330h	VPDMA_dei_hq_mv_in_cstat	VPDMA DEI Motion Vector In cstat	Section 1.3.8.99
33Ch	VPDMA_dei_hq_mv_out_cstat	VPDMA DEI Motion Vector Out cstat	Section 1.3.8.100
344h	VPDMA_dei_sc_out_cstat	VPDMA DEI Scaler (SC_1) Out cstat	Section 1.3.8.101
348h	VPDMA_pip_wrbk_cstat	VPDMA PIP WRBK (BP0) cstat	Section 1.3.8.102
34Ch	VPDMA_sc_in_chroma_cstat	VPDMA Aux (SC_2) Chroma cstat	Section 1.3.8.103
350h	VPDMA_sc_in_luma_cstat	VPDMA Aux (SC_2) Luma cstat	Section 1.3.8.104
374h	VPDMA_sc_out_cstat	VPDMA Aux Scaler (SC_2) Out cstat	Section 1.3.8.105
378h	VPDMA_comp_wrbk_cstat	VPDMA COMP WRBK (BP1) cstat	Section 1.3.8.106
37Ch	VPDMA_grpx1_data_cstat	VPDMA GRPX1 Data cstat	Section 1.3.8.107
380h	VPDMA_grpx2_data_cstat	VPDMA GRPX2 Data cstat	Section 1.3.8.108
384h	VPDMA_grpx3_data_cstat	VPDMA GRPX3 Data cstat	Section 1.3.8.109
388h	VPDMA_vip1_lo_y_cstat	VPDMA VIP1 lo y cstat	Section 1.3.8.110
38Ch	VPDMA_vip1_lo_uv_cstat	VPDMA VIP1 lo uv cstat	Section 1.3.8.111
390h	VPDMA_vip1_up_y_cstat	VPDMA VIP1 up y cstat	Section 1.3.8.112
394h	VPDMA_vip1_up_uv_cstat	VPDMA VIP1 up uv cstat	Section 1.3.8.113
398h	VPDMA_vip2_lo_y_cstat	VPDMA VIP2 lo y cstat	Section 1.3.8.114
39Ch	VPDMA_vip2_lo_uv_cstat	VPDMA VIP2 lo uv cstat	Section 1.3.8.115
3A0h	VPDMA_vip2_up_y_cstat	VPDMA VIP2 up y cstat	Section 1.3.8.116
3A4h	VPDMA_vip2_up_uv_cstat	VPDMA VIP2 up uv cstat	Section 1.3.8.117
3A8h	VPDMA_grpx1_st_cstat	VPDMA GRPX1 Stencil cstat	Section 1.3.8.118
3ACh	VPDMA_grpx2_st_cstat	VPDMA GRPX2 Stencil cstat	Section 1.3.8.119
3B0h	VPDMA_grpx3_st_cstat	VPDMA GRPX3 Stencil cstat	Section 1.3.8.120
3B4h	VPDMA_nf_422_in_cstat	VPDMA NF 422 In cstat	Section 1.3.8.121
3B8h	VPDMA_nf_420_y_in_cstat	VPDMA NF 420 Luma In cstat	Section 1.3.8.122
3BCh	VPDMA_nf_420_uv_in_cstat	VPDMA NF 420 Chroma In cstat	Section 1.3.8.123
3C0h	VPDMA_nf_420_y_out_cstat	VPDMA NF 420 Luma Out cstat	Section 1.3.8.124
3C4h	VPDMA_nf_420_uv_out_cstat	VPDMA NF 420 Chroma Out cstat	Section 1.3.8.125
3CCh	VPDMA_vbi_sdvenc_cstat	VPDMA VBI SDVENC cstat	Section 1.3.8.126
3D0h	VPDMA_vpi_ctl_cstat	VPDMA VPI Control cstat	Section 1.3.8.127
3D4h	VPDMA_hdmi_wrbk_out_cstat	VPDMA HDMI WRBK (SC_5) Out cstat	Section 1.3.8.128
3D8h	VPDMA_trans1_chroma_cstat	VPDMA Transcode 1 Chroma cstat	Section 1.3.8.129
3DCh	VPDMA_trans1_luma_cstat	VPDMA Transcode 1 Luma cstat	Section 1.3.8.130
3E0h	VPDMA_trans2_chroma_cstat	VPDMA Transcode 2 Chroma cstat	Section 1.3.8.131
3E4h	VPDMA_trans2_luma_cstat	VPDMA Transcode 2 Luma cstat	Section 1.3.8.132
3E8h	VPDMA_vip1_anc_a_cstat	VPDMA VIP1 Ancillary A cstat	Section 1.3.8.133
3ECh	VPDMA_vip1_anc_b_cstat	VPDMA VIP1 Ancillary B cstat	Section 1.3.8.134
3F0h	VPDMA_vip2_anc_a_cstat	VPDMA VIP2 Ancillary A cstat	Section 1.3.8.135
3F4h	VPDMA_vip2_anc_b_cstat	VPDMA VIP2 Ancillary B cstat	Section 1.3.8.136

1.3.8.1 VPDMA_pid Register (offset = 0h) [reset = 73280900h]

VPDMA_pid is shown in Figure 1-301 and described in Table 1-213.

Figure 1-301. VPDMA_pid Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-213. VPDMA_pid Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	The scheme of the register used. Currently this is PDR 3.5 Scheme
29-16	FUNC	R	3328h	The funcition of the module being used. The value is for vpdma.
15-11	RTL	R	1h	RTL Release Version The PDR release number of this IP. After Bootup this value becomes the firmware Revision ID
10-8	MAJOR	R	1h	Major Release Number
7	VPDMA_LOAD_COMPLETE	R	0h	This bit will be 1 when the VPDMA state machines image and data image have successfuly been fetched and loaded.
6	VPDMA_ACCESS_TYPE	R	0h	After bootup this bit states how DMA transaction are setup by lists or through register access. 0: Lists 1: Register Access
5-0	MINOR	R	0h	Minor Release Number

1.3.8.2 VPDMA_list_addr Register (offset = 4h) [reset = 0h]

VPDMA_list_addr is shown in Figure 1-302 and described in Table 1-214.

Figure 1-302. VPDMA_list_addr Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIST_ADDR																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-214. VPDMA_list_addr Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LIST_ADDR	R/W	0h	Location of a new list of descriptors. This register must be written with the VPDMA configuration location after reset.

1.3.8.3 VPDMA_list_attr Register (offset = 8h) [reset = 0h]

VPDMA_list_attr is shown in Figure 1-303 and described in Table 1-215.

Figure 1-303. VPDMA_list_attr Register

31	30	29	28	27	26	25	24
Reserved					LIST_NUM		
R-0h					R/W-0h		

23	22	21	20	19	18	17	16
Reserved			STOP	RDY	LIST_TYPE		
R-0h			W-0h	R-0h	R/W-0h		

15	14	13	12	11	10	9	8
LIST_SIZE							
R/W-0h							

7	6	5	4	3	2	1	0
LIST_SIZE							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-215. VPDMA_list_attr Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-24	LIST_NUM	R/W	0h	The list number that should be assigned to the list located at LIST_ADDR. If the list is still active this will block all future list writes until the list is available.
23-21	Reserved	R	0h	
20	STOP	W	0h	This bit is written with the LIST_NUMBER field to stop a list. When this bit is written a one the list specified by the LIST_NUMBER is sent a stop signal and will finish the current frame of transfers and then free the list resources.
19	RDY	R	0h	This bit is low when a new list cannot be written to the LIST_ADDR register. The reasons this bit would be low are at initial startup if the LIST_MANAGER State Machine image has not completed loading. It also would be low if the last write to the LIST_ATTR attempted to start a list that is currently active. When this bit is low any writes to the list address register will cause access to not be accepted until this bit has set by the previous list having completed.
18-16	LIST_TYPE	R/W	0h	The type of list that has been generated. 0: Normal List 1: Self-Modifying List 2: List Doorbell Others Reserved for future use
15-0	LIST_SIZE	R/W	0h	Number of 128 bit word in the new list of descriptors. Writes to this register will activate the list in the list stack of the list manager and begin transfer of the list into VPDMA. This size can not be 0.

1.3.8.4 VPDMA_list_stat_sync Register (offset = Ch) [reset = 0h]

VPDMA_list_stat_sync is shown in Figure 1-304 and described in Table 1-216.

Figure 1-304. VPDMA_list_stat_sync Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
LIST7_BUSY	LIST6_BUSY	LIST5_BUSY	LIST4_BUSY	LIST3_BUSY	LIST2_BUSY	LIST1_BUSY	LIST0_BUSY
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
SYNC_LISTS7	SYNC_LISTS6	SYNC_LISTS5	SYNC_LISTS4	SYNC_LISTS3	SYNC_LISTS2	SYNC_LISTS1	SYNC_LISTS0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-216. VPDMA_list_stat_sync Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	
23	LIST7_BUSY	R	0h	The list 7 is currently running. Any attempt to load a new list to list 7 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.
22	LIST6_BUSY	R	0h	The list 6 is currently running. Any attempt to load a new list to list 6 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.
21	LIST5_BUSY	R	0h	The list 5 is currently running. Any attempt to load a new list to list 5 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.
20	LIST4_BUSY	R	0h	The list 4 is currently running. Any attempt to load a new list to list 4 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.
19	LIST3_BUSY	R	0h	The list 3 is currently running. Any attempt to load a new list to list 3 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.
18	LIST2_BUSY	R	0h	The list 2 is currently running. Any attempt to load a new list to list 2 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.
17	LIST1_BUSY	R	0h	The list 1 is currently running. Any attempt to load a new list to list 1 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.
16	LIST0_BUSY	R	0h	The list 0 is currently running. Any attempt to load a new list to list 0 will result in the LM_ADDR and LM_ATTR registers to be locked until the list is complete and this value goes to 0.
15-8	Reserved	R	0h	
7	SYNC_LISTS7	W	0h	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 7 waiting on it.
6	SYNC_LISTS6	W	0h	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 6 waiting on it.
5	SYNC_LISTS5	W	0h	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 5 waiting on it.
4	SYNC_LISTS4	W	0h	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 4 waiting on it.

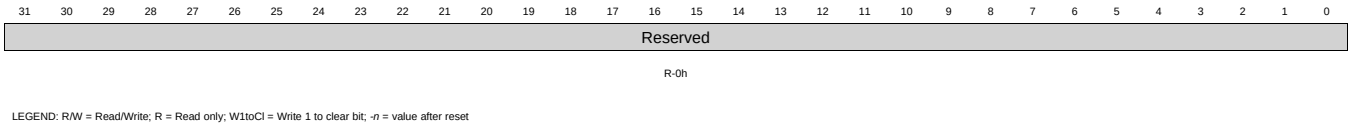
Table 1-216. VPDMA_list_stat_sync Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SYNC_LISTS3	W	0h	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 3 waiting on it.
2	SYNC_LISTS2	W	0h	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 2 waiting on it.
1	SYNC_LISTS1	W	0h	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 1 waiting on it.
0	SYNC_LISTS0	W	0h	Writing a 1 to this field causes a sync event to fire that clears a Control Descriptor in List 0 waiting on it.

1.3.8.5 VPDMA_vpi_ctl_address Register (offset = 10h) [reset = 0h]

VPDMA_vpi_ctl_address is shown in Figure 1-305 and described in Table 1-217.

Figure 1-305. VPDMA_vpi_ctl_address Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

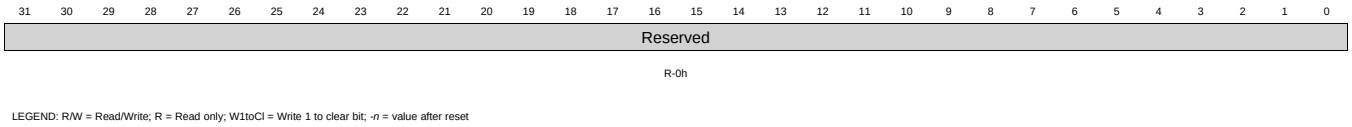
Table 1-217. VPDMA_vpi_ctl_address Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.8.6 VPDMA_vpi_ctl_data Register (offset = 14h) [reset = 0h]

VPDMA_vpi_ctl_data is shown in Figure 1-306 and described in Table 1-218.

Figure 1-306. VPDMA_vpi_ctl_data Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-218. VPDMA_vpi_ctl_data Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.8.7 VPDMA_bg_rgb Register (offset = 18h) [reset = 0h]

VPDMA_bg_rgb is shown in Figure 1-307 and described in Table 1-219.

Figure 1-307. VPDMA_bg_rgb Register

31	30	29	28	27	26	25	24
RED							
R/W-0h							
23	22	21	20	19	18	17	16
GREEN							
R/W-0h							
15	14	13	12	11	10	9	8
BLUE							
R/W-0h							
7	6	5	4	3	2	1	0
BLEND							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-219. VPDMA_bg_rgb Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RED	R/W	0h	The red value to give on an RGB data port for a blank pixel when using virtual video buffering
23-16	GREEN	R/W	0h	The green value to give on an RGB data port for a blank pixel when using virtual video buffering
15-8	BLUE	R/W	0h	The blue value to give on an RGB data port for a blank pixel when using virtual video buffering
7-0	BLEND	R/W	0h	The blend value to give on an RGB data port for a blank pixel when using virtual video buffering

1.3.8.8 VPDMA_bg_yuv Register (offset = 1Ch) [reset = 0h]

VPDMA_bg_yuv is shown in Figure 1-308 and described in Table 1-220.

Figure 1-308. VPDMA_bg_yuv Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Y							
R/W-0h							
15	14	13	12	11	10	9	8
CR							
R/W-0h							
7	6	5	4	3	2	1	0
CB							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-220. VPDMA_bg_yuv Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	
23-16	Y	R/W	0h	The Y value to give on a YUV data port for a blank pixel when using virtual video buffering
15-8	CR	R/W	0h	The Cr value to give on a YUV data port for a blank pixel when using virtual video buffering
7-0	CB	R/W	0h	The Cb value to give on a YUV data port for a blank pixel when using virtual video buffering

1.3.8.9 VPDMA_descriptor_top Register (offset = 20h) [reset = 0h]

VPDMA_descriptor_top is shown in Figure 1-309 and described in Table 1-221.

Figure 1-309. VPDMA_descriptor_top Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-221. VPDMA_descriptor_top Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	

1.3.8.10 VPDMA_descriptor_bottom Register (offset = 24h) [reset = 0h]

VPDMA_descriptor_bottom is shown in Figure 1-310 and described in Table 1-222.

Figure 1-310. VPDMA_descriptor_bottom Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-222. VPDMA_descriptor_bottom Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.8.11 VPDMA_current_descriptor Register (offset = 28h) [reset = 0h]

VPDMA_current_descriptor is shown in Figure 1-311 and described in Table 1-223.

Figure 1-311. VPDMA_current_descriptor Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-223. VPDMA_current_descriptor Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.8.12 VPDMA_descriptor_status_control Register (offset = 2Ch) [reset = 0h]

VPDMA_descriptor_status_control is shown in Figure 1-312 and described in Table 1-224.

Figure 1-312. VPDMA_descriptor_status_control Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

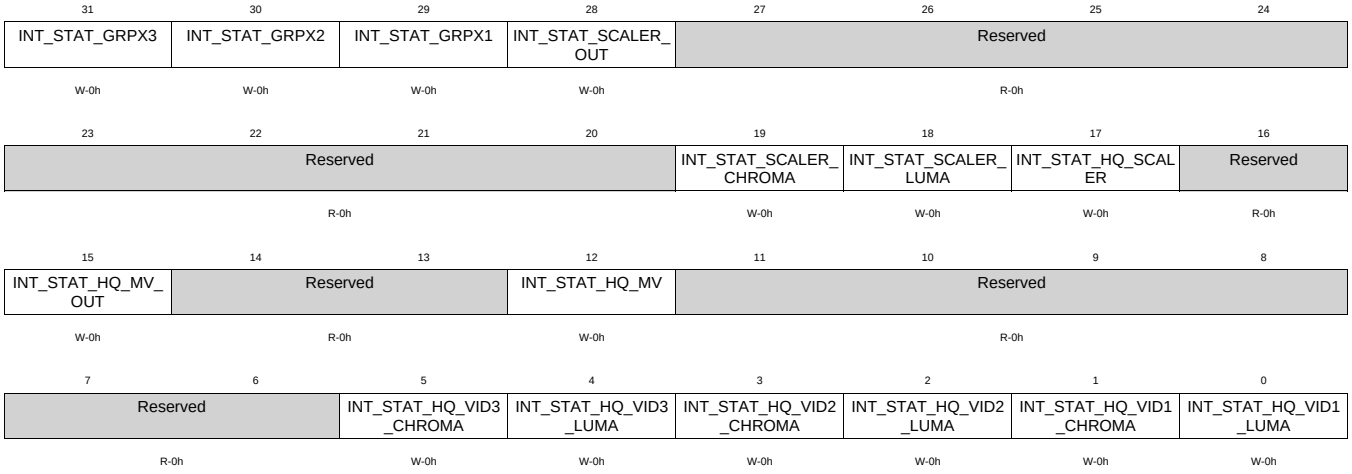
Table 1-224. VPDMA_descriptor_status_control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.8.13 VPDMA_int0_channel0_int_stat Register (offset = 40h) [reset = 0h]

VPDMA_int0_channel0_int_stat is shown in Figure 1-313 and described in Table 1-225.

Figure 1-313. VPDMA_int0_channel0_int_stat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-225. VPDMA_int0_channel0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_GRPX3	W	0h	The last read DMA transaction has occurred for channel grpx3 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_GRPX2	W	0h	The last read DMA transaction has occurred for channel grpx2 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_GRPX1	W	0h	The last read DMA transaction has occurred for channel grpx1 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_SCALER_OUT	W	0h	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27-20	Reserved	R	0h	
19	INT_STAT_SCALER_CHROMA	W	0h	The last write DMA transaction has completed for channel scaler_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-225. VPDMA_int0_channel0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	INT_STAT_SCALER_LUMA	W	0h	The last write DMA transaction has completed for channel scaler_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_HQ_SCALER	W	0h	The last write DMA transaction has completed for channel hq_scaler. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	Reserved	R	0h	
15	INT_STAT_HQ_MV_OUT	W	0h	The last write DMA transaction has completed for channel hq_mv_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_hq_mv_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14-13	Reserved	R	0h	
12	INT_STAT_HQ_MV	W	0h	The last read DMA transaction has occurred for channel hq_mv and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_hq_mv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11-6	Reserved	R	0h	
5	INT_STAT_HQ_VID3_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid3_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_3_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_HQ_VID3_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid3_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_3_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_HQ_VID2_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid2_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_2_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_HQ_VID2_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid2_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_2_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-225. VPDMA_int0_channel0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_STAT_HQ_VID1_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid1_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_1_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_HQ_VID1_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid1_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_1_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.14 VPDMA_int0_channel0_int_mask Register (offset = 44h) [reset = 0h]

VPDMA_int0_channel0_int_mask is shown in Figure 1-314 and described in Table 1-226.

Figure 1-314. VPDMA_int0_channel0_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_GRPX3	INT_MASK_GRPX2	INT_MASK_GRPX1	INT_MASK_SCALER_OUT	Reserved			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
Reserved				INT_MASK_SCALER_CHROMA	INT_MASK_SCALER_LUMA	INT_MASK_HQ_SCALER	Reserved
R-0h				R/W-0h	R/W-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
INT_MASK_HQ_MV_OUT	Reserved		INT_MASK_HQ_MV	Reserved			
R/W-0h	R-0h		R/W-0h	R-0h			
7	6	5	4	3	2	1	0
Reserved		INT_MASK_HQ_VID3_CHROMA	INT_MASK_HQ_VID3_LUMA	INT_MASK_HQ_VID2_CHROMA	INT_MASK_HQ_VID2_LUMA	INT_MASK_HQ_VID1_CHROMA	INT_MASK_HQ_VID1_LUMA
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-226. VPDMA_int0_channel0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_GRPX3	R/W	0h	The interrupt for Graphcis 2 Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_GRPX2	R/W	0h	The interrupt for Graphics 1 Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_GRPX1	R/W	0h	The interrupt for Graphics 0 Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_SCALER_OUT	R/W	0h	The interrupt for Low Cost DEI Scalar Write to Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
27-20	Reserved	R	0h	
19	INT_MASK_SCALER_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_SCALER_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_HQ_SCALER	R/W	0h	The interrupt for High Quality DEI Scaler Write to Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	Reserved	R	0h	
15	INT_MASK_HQ_MV_OUT	R/W	0h	The interrupt for Low Cost DEI Motion Vector Write should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14-13	Reserved	R	0h	
12	INT_MASK_HQ_MV	R/W	0h	The interrupt for Low Cost DEI Motion Vector should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11-6	Reserved	R	0h	

Table 1-226. VPDMA_int0_channel0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_MASK_HQ_VID3_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_HQ_VID3_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_HQ_VID2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_HQ_VID2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_HQ_VID1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_HQ_VID1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.15 VPDMA_int0_channel1_int_stat Register (offset = 48h) [reset = 0h]

VPDMA_int0_channel1_int_stat is shown in Figure 1-315 and described in Table 1-227.

Figure 1-315. VPDMA_int0_channel1_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP1_MULT_PORTB_SRC9	INT_STAT_VIP1_MULT_PORTB_SRC8	INT_STAT_VIP1_MULT_PORTB_SRC7	INT_STAT_VIP1_MULT_PORTB_SRC6	INT_STAT_VIP1_MULT_PORTB_SRC5	INT_STAT_VIP1_MULT_PORTB_SRC4	INT_STAT_VIP1_MULT_PORTB_SRC3	INT_STAT_VIP1_MULT_PORTB_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP1_MULT_PORTB_SRC1	INT_STAT_VIP1_MULT_PORTB_SRC0	INT_STAT_VIP1_MULT_PORTA_SRC15	INT_STAT_VIP1_MULT_PORTA_SRC14	INT_STAT_VIP1_MULT_PORTA_SRC13	INT_STAT_VIP1_MULT_PORTA_SRC12	INT_STAT_VIP1_MULT_PORTA_SRC11	INT_STAT_VIP1_MULT_PORTA_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP1_MULT_PORTA_SRC9	INT_STAT_VIP1_MULT_PORTA_SRC8	INT_STAT_VIP1_MULT_PORTA_SRC7	INT_STAT_VIP1_MULT_PORTA_SRC6	INT_STAT_VIP1_MULT_PORTA_SRC5	INT_STAT_VIP1_MULT_PORTA_SRC4	INT_STAT_VIP1_MULT_PORTA_SRC3	INT_STAT_VIP1_MULT_PORTA_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_PORTA_SRC1	INT_STAT_VIP1_MULT_PORTA_SRC0	INT_STAT_GRPX3_CLUT	INT_STAT_GRPX2_CLUT	INT_STAT_GRPX1_CLUT	INT_STAT_GRPX3_STENCIL	INT_STAT_GRPX2_STENCIL	INT_STAT_GRPX1_STENCIL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-227. VPDMA_int0_channel1_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP1_MULT_PORTB_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP1_MULT_PORTB_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP1_MULT_PORTB_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP1_MULT_PORTB_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_MULT_PORTB_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_MULT_PORTB_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-227. VPDMA_int0_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP1_MULT_PORTB_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP1_MULT_PORTB_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP1_MULT_PORTB_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP1_MULT_PORTB_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP1_MULT_PORTA_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP1_MULT_PORTA_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP1_MULT_PORTA_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP1_MULT_PORTA_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP1_MULT_PORTA_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP1_MULT_PORTA_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-227. VPDMA_int0_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP1_MULT_PORTA_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP1_MULT_PORTA_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP1_MULT_PORTA_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP1_MULT_PORTA_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_MULT_PORTA_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_MULT_PORTA_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_MULT_PORTA_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_MULT_PORTA_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_MULT_PORTA_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_MULT_PORTA_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-227. VPDMA_int0_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_GRPX3_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx3_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_GRPX2_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx2_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_GRPX1_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx1_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_GRPX3_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx3_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_GRPX2_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx2_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_GRPX1_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx1_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.16 VPDMA_int0_channel1_int_mask Register (offset = 4Ch) [reset = 0h]

VPDMA_int0_channel1_int_mask is shown in Figure 1-316 and described in Table 1-228.

Figure 1-316. VPDMA_int0_channel1_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP1_MULT_PORTB_SRC9	INT_MASK_VIP1_MULT_PORTB_SRC8	INT_MASK_VIP1_MULT_PORTB_SRC7	INT_MASK_VIP1_MULT_PORTB_SRC6	INT_MASK_VIP1_MULT_PORTB_SRC5	INT_MASK_VIP1_MULT_PORTB_SRC4	INT_MASK_VIP1_MULT_PORTB_SRC3	INT_MASK_VIP1_MULT_PORTB_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
INT_MASK_VIP1_MULT_PORTB_SRC1	INT_MASK_VIP1_MULT_PORTB_SRC0	INT_MASK_VIP1_MULT_PORTA_SRC15	INT_MASK_VIP1_MULT_PORTA_SRC14	INT_MASK_VIP1_MULT_PORTA_SRC13	INT_MASK_VIP1_MULT_PORTA_SRC12	INT_MASK_VIP1_MULT_PORTA_SRC11	INT_MASK_VIP1_MULT_PORTA_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

15	14	13	12	11	10	9	8
INT_MASK_VIP1_MULT_PORTA_SRC9	INT_MASK_VIP1_MULT_PORTA_SRC8	INT_MASK_VIP1_MULT_PORTA_SRC7	INT_MASK_VIP1_MULT_PORTA_SRC6	INT_MASK_VIP1_MULT_PORTA_SRC5	INT_MASK_VIP1_MULT_PORTA_SRC4	INT_MASK_VIP1_MULT_PORTA_SRC3	INT_MASK_VIP1_MULT_PORTA_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_PORTA_SRC1	INT_MASK_VIP1_MULT_PORTA_SRC0	INT_MASK_GRPX3_CLUT	INT_MASK_GRPX2_CLUT	INT_MASK_GRPX1_CLUT	INT_MASK_GRPX3_STENCIL	INT_MASK_GRPX2_STENCIL	INT_MASK_GRPX1_STENCIL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-228. VPDMA_int0_channel1_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP1_MULT_PORTB_SRC9	R/W	0h	The interrupt for Video Input 1 Port B Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP1_MULT_PORTB_SRC8	R/W	0h	The interrupt for Video Input 1 Port B Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP1_MULT_PORTB_SRC7	R/W	0h	The interrupt for Video Input 1 Port B Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP1_MULT_PORTB_SRC6	R/W	0h	The interrupt for Video Input 1 Port B Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_MULT_PORTB_SRC5	R/W	0h	The interrupt for Video Input 1 Port B Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_MULT_PORTB_SRC4	R/W	0h	The interrupt for Video Input 1 Port B Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP1_MULT_PORTB_SRC3	R/W	0h	The interrupt for Video Input 1 Port B Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP1_MULT_PORTB_SRC2	R/W	0h	The interrupt for Video Input 1 Port B Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP1_MULT_PORTB_SRC1	R/W	0h	The interrupt for Video Input 1 Port B Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP1_MULT_PORTB_SRC0	R/W	0h	The interrupt for Video Input 1 Port B Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP1_MULT_PORTA_SRC15	R/W	0h	The interrupt for Video Input 1 Port A Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-228. VPDMA_int0_channel1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP1_MULT_PORTA_SRC14	R/W	0h	The interrupt for Video Input 1 Port A Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP1_MULT_PORTA_SRC13	R/W	0h	The interrupt for Video Input 1 Port A Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP1_MULT_PORTA_SRC12	R/W	0h	The interrupt for Video Input 1 Port A Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP1_MULT_PORTA_SRC11	R/W	0h	The interrupt for Video Input 1 Port A Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP1_MULT_PORTA_SRC10	R/W	0h	The interrupt for Video Input 1 Port A Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP1_MULT_PORTA_SRC9	R/W	0h	The interrupt for Video Input 1 Port A Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP1_MULT_PORTA_SRC8	R/W	0h	The interrupt for Video Input 1 Port A Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP1_MULT_PORTA_SRC7	R/W	0h	The interrupt for Video Input 1 Port A Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP1_MULT_PORTA_SRC6	R/W	0h	The interrupt for Video Input 1 Port A Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_MULT_PORTA_SRC5	R/W	0h	The interrupt for Video Input 1 Port A Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_MULT_PORTA_SRC4	R/W	0h	The interrupt for Video Input 1 Port A Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_MULT_PORTA_SRC3	R/W	0h	The interrupt for Video Input 1 Port A Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_MULT_PORTA_SRC2	R/W	0h	The interrupt for Video Input 1 Port A Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_MULT_PORTA_SRC1	R/W	0h	The interrupt for Video Input 1 Port A Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_MULT_PORTA_SRC0	R/W	0h	The interrupt for Video Input 1 Port A Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_GRPX3_CLUT	R/W	0h	The interrupt for Graphics 2 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_GRPX2_CLUT	R/W	0h	The interrupt for Graphics 1 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_GRPX1_CLUT	R/W	0h	The interrupt for Graphics 0 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-228. VPDMA_int0_channel1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_GRPX3_STENCIL	R/W	0h	The interrupt for Graphics 2 Stencil should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_GRPX2_STENCIL	R/W	0h	The interrupt for Graphics 1 Stencil should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_GRPX1_STENCIL	R/W	0h	The interrupt for Graphics 0 Stencil should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.17 VPDMA_int0_channel2_int_stat Register (offset = 50h) [reset = 0h]

VPDMA_int0_channel2_int_stat is shown in Figure 1-317 and described in Table 1-229.

Figure 1-317. VPDMA_int0_channel2_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP1_MULT_ANCB_SRC9	INT_STAT_VIP1_MULT_ANCB_SRC8	INT_STAT_VIP1_MULT_ANCB_SRC7	INT_STAT_VIP1_MULT_ANCB_SRC6	INT_STAT_VIP1_MULT_ANCB_SRC5	INT_STAT_VIP1_MULT_ANCB_SRC4	INT_STAT_VIP1_MULT_ANCB_SRC3	INT_STAT_VIP1_MULT_ANCB_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP1_MULT_ANCB_SRC1	INT_STAT_VIP1_MULT_ANCB_SRC0	INT_STAT_VIP1_MULT_ANCA_SRC15	INT_STAT_VIP1_MULT_ANCA_SRC14	INT_STAT_VIP1_MULT_ANCA_SRC13	INT_STAT_VIP1_MULT_ANCA_SRC12	INT_STAT_VIP1_MULT_ANCA_SRC11	INT_STAT_VIP1_MULT_ANCA_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP1_MULT_ANCA_SRC9	INT_STAT_VIP1_MULT_ANCA_SRC8	INT_STAT_VIP1_MULT_ANCA_SRC7	INT_STAT_VIP1_MULT_ANCA_SRC6	INT_STAT_VIP1_MULT_ANCA_SRC5	INT_STAT_VIP1_MULT_ANCA_SRC4	INT_STAT_VIP1_MULT_ANCA_SRC3	INT_STAT_VIP1_MULT_ANCA_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_ANCA_SRC1	INT_STAT_VIP1_MULT_ANCA_SRC0	INT_STAT_VIP1_MULT_PORTB_SRC15	INT_STAT_VIP1_MULT_PORTB_SRC14	INT_STAT_VIP1_MULT_PORTB_SRC13	INT_STAT_VIP1_MULT_PORTB_SRC12	INT_STAT_VIP1_MULT_PORTB_SRC11	INT_STAT_VIP1_MULT_PORTB_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-229. VPDMA_int0_channel2_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP1_MULT_ANCB_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP1_MULT_ANCB_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP1_MULT_ANCB_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP1_MULT_ANCB_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_MULT_ANCB_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_MULT_ANCB_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-229. VPDMA_int0_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP1_MULT_ANCB_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP1_MULT_ANCB_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP1_MULT_ANCB_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP1_MULT_ANCB_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP1_MULT_ANCA_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP1_MULT_ANCA_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP1_MULT_ANCA_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP1_MULT_ANCA_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP1_MULT_ANCA_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP1_MULT_ANCA_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-229. VPDMA_int0_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP1_MULT_ANCA_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP1_MULT_ANCA_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP1_MULT_ANCA_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP1_MULT_ANCA_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_MULT_ANCA_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_MULT_ANCA_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_MULT_ANCA_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_MULT_ANCA_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_MULT_ANCA_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_MULT_ANCA_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-229. VPDMA_int0_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_MULT_PORTB_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_MULT_PORTB_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_MULT_PORTB_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_MULT_PORTB_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP1_MULT_PORTB_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP1_MULT_PORTB_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.18 VPDMA_int0_channel2_int_mask Register (offset = 54h) [reset = 0h]

VPDMA_int0_channel2_int_mask is shown in Figure 1-318 and described in Table 1-230.

Figure 1-318. VPDMA_int0_channel2_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP1_MULT_ANCB_SRC9	INT_MASK_VIP1_MULT_ANCB_SRC8	INT_MASK_VIP1_MULT_ANCB_SRC7	INT_MASK_VIP1_MULT_ANCB_SRC6	INT_MASK_VIP1_MULT_ANCB_SRC5	INT_MASK_VIP1_MULT_ANCB_SRC4	INT_MASK_VIP1_MULT_ANCB_SRC3	INT_MASK_VIP1_MULT_ANCB_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP1_MULT_ANCB_SRC1	INT_MASK_VIP1_MULT_ANCB_SRC0	INT_MASK_VIP1_MULT_ANCA_SRC15	INT_MASK_VIP1_MULT_ANCA_SRC14	INT_MASK_VIP1_MULT_ANCA_SRC13	INT_MASK_VIP1_MULT_ANCA_SRC12	INT_MASK_VIP1_MULT_ANCA_SRC11	INT_MASK_VIP1_MULT_ANCA_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP1_MULT_ANCA_SRC9	INT_MASK_VIP1_MULT_ANCA_SRC8	INT_MASK_VIP1_MULT_ANCA_SRC7	INT_MASK_VIP1_MULT_ANCA_SRC6	INT_MASK_VIP1_MULT_ANCA_SRC5	INT_MASK_VIP1_MULT_ANCA_SRC4	INT_MASK_VIP1_MULT_ANCA_SRC3	INT_MASK_VIP1_MULT_ANCA_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_ANCA_SRC1	INT_MASK_VIP1_MULT_ANCA_SRC0	INT_MASK_VIP1_MULT_PORTB_SRC15	INT_MASK_VIP1_MULT_PORTB_SRC14	INT_MASK_VIP1_MULT_PORTB_SRC13	INT_MASK_VIP1_MULT_PORTB_SRC12	INT_MASK_VIP1_MULT_PORTB_SRC11	INT_MASK_VIP1_MULT_PORTB_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-230. VPDMA_int0_channel2_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP1_MULT_ANCB_SRC9	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP1_MULT_ANCB_SRC8	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP1_MULT_ANCB_SRC7	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP1_MULT_ANCB_SRC6	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_MULT_ANCB_SRC5	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_MULT_ANCB_SRC4	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP1_MULT_ANCB_SRC3	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP1_MULT_ANCB_SRC2	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP1_MULT_ANCB_SRC1	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP1_MULT_ANCB_SRC0	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP1_MULT_ANCA_SRC15	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-230. VPDMA_int0_channel2_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP1_MULT_ANCA_SRC14	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP1_MULT_ANCA_SRC13	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP1_MULT_ANCA_SRC12	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP1_MULT_ANCA_SRC11	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP1_MULT_ANCA_SRC10	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP1_MULT_ANCA_SRC9	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP1_MULT_ANCA_SRC8	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP1_MULT_ANCA_SRC7	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP1_MULT_ANCA_SRC6	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_MULT_ANCA_SRC5	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_MULT_ANCA_SRC4	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_MULT_ANCA_SRC3	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_MULT_ANCA_SRC2	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_MULT_ANCA_SRC1	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_MULT_ANCA_SRC0	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_MULT_PORTB_SRC15	R/W	0h	The interrupt for Video Input 1 Port B Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_MULT_PORTB_SRC14	R/W	0h	The interrupt for Video Input 1 Port B Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_MULT_PORTB_SRC13	R/W	0h	The interrupt for Video Input 1 Port B Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-230. VPDMA_int0_channel2_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP1_MULT_PORTB_SRC12	R/W	0h	The interrupt for Video Input 1 Port B Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP1_MULT_PORTB_SRC11	R/W	0h	The interrupt for Video Input 1 Port B Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP1_MULT_PORTB_SRC10	R/W	0h	The interrupt for Video Input 1 Port B Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.19 VPDMA_int0_channel3_int_stat Register (offset = 58h) [reset = 0h]

VPDMA_int0_channel3_int_stat is shown in Figure 1-319 and described in Table 1-231.

Figure 1-319. VPDMA_int0_channel3_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP2_MULT_PORTB_SRC3	INT_STAT_VIP2_MULT_PORTB_SRC2	INT_STAT_VIP2_MULT_PORTB_SRC1	INT_STAT_VIP2_MULT_PORTB_SRC0	INT_STAT_VIP2_MULT_PORTA_SRC15	INT_STAT_VIP2_MULT_PORTA_SRC14	INT_STAT_VIP2_MULT_PORTA_SRC13	INT_STAT_VIP2_MULT_PORTA_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP2_MULT_PORTA_SRC11	INT_STAT_VIP2_MULT_PORTA_SRC10	INT_STAT_VIP2_MULT_PORTA_SRC9	INT_STAT_VIP2_MULT_PORTA_SRC8	INT_STAT_VIP2_MULT_PORTA_SRC7	INT_STAT_VIP2_MULT_PORTA_SRC6	INT_STAT_VIP2_MULT_PORTA_SRC5	INT_STAT_VIP2_MULT_PORTA_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_MULT_PORTA_SRC3	INT_STAT_VIP2_MULT_PORTA_SRC2	INT_STAT_VIP2_MULT_PORTA_SRC1	INT_STAT_VIP2_MULT_PORTA_SRC0	INT_STAT_VIP1_PORTB_RGB	INT_STAT_VIP1_PORTA_RGB	INT_STAT_VIP1_PORTB_CHROMA	INT_STAT_VIP1_PORTB_LUMA
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_PORTA_CHROMA	INT_STAT_VIP1_PORTA_LUMA	INT_STAT_VIP1_MULT_ANCB_SRC15	INT_STAT_VIP1_MULT_ANCB_SRC14	INT_STAT_VIP1_MULT_ANCB_SRC13	INT_STAT_VIP1_MULT_ANCB_SRC12	INT_STAT_VIP1_MULT_ANCB_SRC11	INT_STAT_VIP1_MULT_ANCB_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-231. VPDMA_int0_channel3_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP2_MULT_PORTB_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP2_MULT_PORTB_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP2_MULT_PORTB_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_MULT_PORTB_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP2_MULT_PORTA_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP2_MULT_PORTA_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-231. VPDMA_int0_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP2_MULT_PORTA_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP2_MULT_PORTA_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP2_MULT_PORTA_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP2_MULT_PORTA_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP2_MULT_PORTA_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP2_MULT_PORTA_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP2_MULT_PORTA_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP2_MULT_PORTA_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_MULT_PORTA_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP2_MULT_PORTA_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-231. VPDMA_int0_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP2_MULT_PORTA_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_MULT_PORTA_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_MULT_PORTA_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_MULT_PORTA_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_PORTB_RGB	W	0h	The last write DMA transaction has completed for channel vip1_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_PORTA_RGB	W	0h	The last write DMA transaction has completed for channel vip1_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_PORTB_CHROMA	W	0h	The last write DMA transaction has completed for channel vip1_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_PORTB_LUMA	W	0h	The last write DMA transaction has completed for channel vip1_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_PORTA_CHROMA	W	0h	The last write DMA transaction has completed for channel vip1_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_PORTA_LUMA	W	0h	The last write DMA transaction has completed for channel vip1_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-231. VPDMA_int0_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_MULT_ANCB_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_MULT_ANCB_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_MULT_ANCB_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_MULT_ANCB_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP1_MULT_ANCB_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP1_MULT_ANCB_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.20 VPDMA_int0_channel3_int_mask Register (offset = 5Ch) [reset = 0h]

VPDMA_int0_channel3_int_mask is shown in Figure 1-320 and described in Table 1-232.

Figure 1-320. VPDMA_int0_channel3_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP2_MULT_PORTB_SRC3	INT_MASK_VIP2_MULT_PORTB_SRC2	INT_MASK_VIP2_MULT_PORTB_SRC1	INT_MASK_VIP2_MULT_PORTB_SRC0	INT_MASK_VIP2_MULT_PORTA_SRC15	INT_MASK_VIP2_MULT_PORTA_SRC14	INT_MASK_VIP2_MULT_PORTA_SRC13	INT_MASK_VIP2_MULT_PORTA_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP2_MULT_PORTA_SRC11	INT_MASK_VIP2_MULT_PORTA_SRC10	INT_MASK_VIP2_MULT_PORTA_SRC9	INT_MASK_VIP2_MULT_PORTA_SRC8	INT_MASK_VIP2_MULT_PORTA_SRC7	INT_MASK_VIP2_MULT_PORTA_SRC6	INT_MASK_VIP2_MULT_PORTA_SRC5	INT_MASK_VIP2_MULT_PORTA_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_MULT_PORTA_SRC3	INT_MASK_VIP2_MULT_PORTA_SRC2	INT_MASK_VIP2_MULT_PORTA_SRC1	INT_MASK_VIP2_MULT_PORTA_SRC0	INT_MASK_VIP1_PORTB_RGB	INT_MASK_VIP1_PORTA_RGB	INT_MASK_VIP1_PORTB_CHROMA	INT_MASK_VIP1_PORTB_LUMA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_PORTA_CHROMA	INT_MASK_VIP1_PORTA_LUMA	INT_MASK_VIP1_MULT_ANCB_SRC15	INT_MASK_VIP1_MULT_ANCB_SRC14	INT_MASK_VIP1_MULT_ANCB_SRC13	INT_MASK_VIP1_MULT_ANCB_SRC12	INT_MASK_VIP1_MULT_ANCB_SRC11	INT_MASK_VIP1_MULT_ANCB_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-232. VPDMA_int0_channel3_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP2_MULT_PORTB_SRC3	R/W	0h	The interrupt for Video Input 2 Port B Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP2_MULT_PORTB_SRC2	R/W	0h	The interrupt for Video Input 2 Port B Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP2_MULT_PORTB_SRC1	R/W	0h	The interrupt for Video Input 2 Port B Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_MULT_PORTB_SRC0	R/W	0h	The interrupt for Video Input 2 Port B Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP2_MULT_PORTA_SRC15	R/W	0h	The interrupt for Video Input 2 Port A Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP2_MULT_PORTA_SRC14	R/W	0h	The interrupt for Video Input 2 Port A Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP2_MULT_PORTA_SRC13	R/W	0h	The interrupt for Video Input 2 Port A Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP2_MULT_PORTA_SRC12	R/W	0h	The interrupt for Video Input 2 Port A Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP2_MULT_PORTA_SRC11	R/W	0h	The interrupt for Video Input 2 Port A Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP2_MULT_PORTA_SRC10	R/W	0h	The interrupt for Video Input 2 Port A Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP2_MULT_PORTA_SRC9	R/W	0h	The interrupt for Video Input 2 Port A Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-232. VPDMA_int0_channel3_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP2_MULT_PORTA_SRC8	R/W	0h	The interrupt for Video Input 2 Port A Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP2_MULT_PORTA_SRC7	R/W	0h	The interrupt for Video Input 2 Port A Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP2_MULT_PORTA_SRC6	R/W	0h	The interrupt for Video Input 2 Port A Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_MULT_PORTA_SRC5	R/W	0h	The interrupt for Video Input 2 Port A Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_MULT_PORTA_SRC4	R/W	0h	The interrupt for Video Input 2 Port A Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_MULT_PORTA_SRC3	R/W	0h	The interrupt for Video Input 2 Port A Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_MULT_PORTA_SRC2	R/W	0h	The interrupt for Video Input 2 Port A Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_MULT_PORTA_SRC1	R/W	0h	The interrupt for Video Input 2 Port A Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_MULT_PORTA_SRC0	R/W	0h	The interrupt for Video Input 2 Port A Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_PORTB_RGB	R/W	0h	The interrupt for Video Input 1 Port B RGB Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_PORTA_RGB	R/W	0h	The interrupt for Video Input 1 Port A RGB Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_PORTB_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_PORTB_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_PORTA_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_PORTA_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_MULT_ANCB_SRC15	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_MULT_ANCB_SRC14	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_MULT_ANCB_SRC13	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-232. VPDMA_int0_channel3_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP1_MULT_ANCB_SRC12	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP1_MULT_ANCB_SRC11	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP1_MULT_ANCB_SRC10	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.21 VPDMA_int0_channel4_int_stat Register (offset = 60h) [reset = 0h]

VPDMA_int0_channel4_int_stat is shown in Figure 1-321 and described in Table 1-233.

Figure 1-321. VPDMA_int0_channel4_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP2_MULT_ANCB_SRC3	INT_STAT_VIP2_MULT_ANCB_SRC2	INT_STAT_VIP2_MULT_ANCB_SRC1	INT_STAT_VIP2_MULT_ANCB_SRC0	INT_STAT_VIP2_MULT_ANCA_SRC15	INT_STAT_VIP2_MULT_ANCA_SRC14	INT_STAT_VIP2_MULT_ANCA_SRC13	INT_STAT_VIP2_MULT_ANCA_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP2_MULT_ANCA_SRC11	INT_STAT_VIP2_MULT_ANCA_SRC10	INT_STAT_VIP2_MULT_ANCA_SRC9	INT_STAT_VIP2_MULT_ANCA_SRC8	INT_STAT_VIP2_MULT_ANCA_SRC7	INT_STAT_VIP2_MULT_ANCA_SRC6	INT_STAT_VIP2_MULT_ANCA_SRC5	INT_STAT_VIP2_MULT_ANCA_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_MULT_ANCA_SRC3	INT_STAT_VIP2_MULT_ANCA_SRC2	INT_STAT_VIP2_MULT_ANCA_SRC1	INT_STAT_VIP2_MULT_ANCA_SRC0	INT_STAT_VIP2_MULT_PORTB_SRC15	INT_STAT_VIP2_MULT_PORTB_SRC14	INT_STAT_VIP2_MULT_PORTB_SRC13	INT_STAT_VIP2_MULT_PORTB_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_PORTB_SRC11	INT_STAT_VIP2_MULT_PORTB_SRC10	INT_STAT_VIP2_MULT_PORTB_SRC9	INT_STAT_VIP2_MULT_PORTB_SRC8	INT_STAT_VIP2_MULT_PORTB_SRC7	INT_STAT_VIP2_MULT_PORTB_SRC6	INT_STAT_VIP2_MULT_PORTB_SRC5	INT_STAT_VIP2_MULT_PORTB_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-233. VPDMA_int0_channel4_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP2_MULT_ANCB_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP2_MULT_ANCB_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP2_MULT_ANCB_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_MULT_ANCB_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP2_MULT_ANCA_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP2_MULT_ANCA_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-233. VPDMA_int0_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP2_MULT_ANCA_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP2_MULT_ANCA_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP2_MULT_ANCA_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP2_MULT_ANCA_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP2_MULT_ANCA_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP2_MULT_ANCA_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP2_MULT_ANCA_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP2_MULT_ANCA_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_MULT_ANCA_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP2_MULT_ANCA_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-233. VPDMA_int0_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP2_MULT_ANCA_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_MULT_ANCA_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_MULT_ANCA_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_MULT_ANCA_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP2_MULT_PORTB_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP2_MULT_PORTB_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_MULT_PORTB_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_MULT_PORTB_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_MULT_PORTB_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP2_MULT_PORTB_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-233. VPDMA_int0_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP2_MULT_PORTB_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP2_MULT_PORTB_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP2_MULT_PORTB_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP2_MULT_PORTB_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP2_MULT_PORTB_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP2_MULT_PORTB_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.22 VPDMA_int0_channel4_int_mask Register (offset = 64h) [reset = 0h]

VPDMA_int0_channel4_int_mask is shown in Figure 1-322 and described in Table 1-234.

Figure 1-322. VPDMA_int0_channel4_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP2_MULT_ANCB_SRC3	INT_MASK_VIP2_MULT_ANCB_SRC2	INT_MASK_VIP2_MULT_ANCB_SRC1	INT_MASK_VIP2_MULT_ANCB_SRC0	INT_MASK_VIP2_MULT_ANCA_SRC15	INT_MASK_VIP2_MULT_ANCA_SRC14	INT_MASK_VIP2_MULT_ANCA_SRC13	INT_MASK_VIP2_MULT_ANCA_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP2_MULT_ANCA_SRC11	INT_MASK_VIP2_MULT_ANCA_SRC10	INT_MASK_VIP2_MULT_ANCA_SRC9	INT_MASK_VIP2_MULT_ANCA_SRC8	INT_MASK_VIP2_MULT_ANCA_SRC7	INT_MASK_VIP2_MULT_ANCA_SRC6	INT_MASK_VIP2_MULT_ANCA_SRC5	INT_MASK_VIP2_MULT_ANCA_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_MULT_ANCA_SRC3	INT_MASK_VIP2_MULT_ANCA_SRC2	INT_MASK_VIP2_MULT_ANCA_SRC1	INT_MASK_VIP2_MULT_ANCA_SRC0	INT_MASK_VIP2_MULT_PORTB_SRC15	INT_MASK_VIP2_MULT_PORTB_SRC14	INT_MASK_VIP2_MULT_PORTB_SRC13	INT_MASK_VIP2_MULT_PORTB_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_PORTB_SRC11	INT_MASK_VIP2_MULT_PORTB_SRC10	INT_MASK_VIP2_MULT_PORTB_SRC9	INT_MASK_VIP2_MULT_PORTB_SRC8	INT_MASK_VIP2_MULT_PORTB_SRC7	INT_MASK_VIP2_MULT_PORTB_SRC6	INT_MASK_VIP2_MULT_PORTB_SRC5	INT_MASK_VIP2_MULT_PORTB_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-234. VPDMA_int0_channel4_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP2_MULT_ANCB_SRC3	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP2_MULT_ANCB_SRC2	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP2_MULT_ANCB_SRC1	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_MULT_ANCB_SRC0	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP2_MULT_ANCA_SRC15	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP2_MULT_ANCA_SRC14	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP2_MULT_ANCA_SRC13	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP2_MULT_ANCA_SRC12	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP2_MULT_ANCA_SRC11	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP2_MULT_ANCA_SRC10	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP2_MULT_ANCA_SRC9	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-234. VPDMA_int0_channel4_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP2_MULT_ANCA_SRC8	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP2_MULT_ANCA_SRC7	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP2_MULT_ANCA_SRC6	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_MULT_ANCA_SRC5	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_MULT_ANCA_SRC4	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_MULT_ANCA_SRC3	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_MULT_ANCA_SRC2	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_MULT_ANCA_SRC1	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_MULT_ANCA_SRC0	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP2_MULT_PORTB_SRC15	R/W	0h	The interrupt for Video Input 2 Port B Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP2_MULT_PORTB_SRC14	R/W	0h	The interrupt for Video Input 2 Port B Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_MULT_PORTB_SRC13	R/W	0h	The interrupt for Video Input 2 Port B Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_MULT_PORTB_SRC12	R/W	0h	The interrupt for Video Input 2 Port B Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_MULT_PORTB_SRC11	R/W	0h	The interrupt for Video Input 2 Port B Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_MULT_PORTB_SRC10	R/W	0h	The interrupt for Video Input 2 Port B Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP2_MULT_PORTB_SRC9	R/W	0h	The interrupt for Video Input 2 Port B Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP2_MULT_PORTB_SRC8	R/W	0h	The interrupt for Video Input 2 Port B Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP2_MULT_PORTB_SRC7	R/W	0h	The interrupt for Video Input 2 Port B Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-234. VPDMA_int0_channel4_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP2_MULT_PORTB_SRC6	R/W	0h	The interrupt for Video Input 2 Port B Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP2_MULT_PORTB_SRC5	R/W	0h	The interrupt for Video Input 2 Port B Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP2_MULT_PORTB_SRC4	R/W	0h	The interrupt for Video Input 2 Port B Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.23 VPDMA_int0_channel5_int_stat Register (offset = 68h) [reset = 0h]

VPDMA_int0_channel5_int_stat is shown in Figure 1-323 and described in Table 1-235.

Figure 1-323. VPDMA_int0_channel5_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_TRANSCODE2_CHROMA	INT_STAT_TRANSCODE2_LUMA	INT_STAT_TRANSCODE1_CHROMA	INT_STAT_TRANSCODE1_LUMA	INT_STAT_AUX_IN	INT_STAT_PIP_FRAME	INT_STAT_POST_COMP_WR	INT_STAT_VBI_SD_VENC
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
Reserved	INT_STAT_NF_LAST_CHROMA	INT_STAT_NF_LAST_LUMA	INT_STAT_NF_WRITE_CHROMA	INT_STAT_NF_WRITE_LUMA	INT_STAT_NF_READ	INT_STAT_VIP2_PORTB_RGB	INT_STAT_VIP2_PORTA_RGB
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_PORTB_CHROMA	INT_STAT_VIP2_PORTB_LUMA	INT_STAT_VIP2_PORTA_CHROMA	INT_STAT_VIP2_PORTA_LUMA	INT_STAT_VIP2_MULT_ANCB_SRC15	INT_STAT_VIP2_MULT_ANCB_SRC14	INT_STAT_VIP2_MULT_ANCB_SRC13	INT_STAT_VIP2_MULT_ANCB_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_ANCB_SRC11	INT_STAT_VIP2_MULT_ANCB_SRC10	INT_STAT_VIP2_MULT_ANCB_SRC9	INT_STAT_VIP2_MULT_ANCB_SRC8	INT_STAT_VIP2_MULT_ANCB_SRC7	INT_STAT_VIP2_MULT_ANCB_SRC6	INT_STAT_VIP2_MULT_ANCB_SRC5	INT_STAT_VIP2_MULT_ANCB_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-235. VPDMA_int0_channel5_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_TRANSCODE2_CHROMA	W	0h	The last read DMA transaction has occurred for channel transcode2_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans2_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_TRANSCODE2_LUMA	W	0h	The last read DMA transaction has occurred for channel transcode2_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans2_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_TRANSCODE1_CHROMA	W	0h	The last read DMA transaction has occurred for channel transcode1_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans1_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_TRANSCODE1_LUMA	W	0h	The last read DMA transaction has occurred for channel transcode1_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans1_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_AUX_IN	W	0h	The last read DMA transaction has occurred for channel aux_in and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client comp_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-235. VPDMA_int0_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	INT_STAT_PIP_FRAME	W	0h	The last read DMA transaction has occurred for channel pip_frame and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client pip_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_POST_COMP_WR	W	0h	The last write DMA transaction has completed for channel post_comp_wr. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client hdmi_wrbk_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VBI_SD_VENC	W	0h	The last read DMA transaction has occurred for channel vbi_sd_venc and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client vbi_sdvenc will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	Reserved	R	0h	
22	INT_STAT_NF_LAST_CHROMA	W	0h	The last read DMA transaction has occurred for channel nf_last_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_420_uv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_NF_LAST_LUMA	W	0h	The last read DMA transaction has occurred for channel nf_last_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_420_y_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_NF_WRITE_CHROMA	W	0h	The last write DMA transaction has completed for channel nf_write_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_NF_WRITE_LUMA	W	0h	The last write DMA transaction has completed for channel nf_write_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_NF_READ	W	0h	The last read DMA transaction has occurred for channel nf_read and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_422_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_PORTB_RGB	W	0h	The last write DMA transaction has completed for channel vip2_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-235. VPDMA_int0_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	INT_STAT_VIP2_PORTA_RGB	W	0h	The last write DMA transaction has completed for channel vip2_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_VIP2_PORTB_CHROMA	W	0h	The last write DMA transaction has completed for channel vip2_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_PORTB_LUMA	W	0h	The last write DMA transaction has completed for channel vip2_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_PORTA_CHROMA	W	0h	The last write DMA transaction has completed for channel vip2_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_PORTA_LUMA	W	0h	The last write DMA transaction has completed for channel vip2_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP2_MULT_ANCB_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP2_MULT_ANCB_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_MULT_ANCB_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_MULT_ANCB_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_MULT_ANCB_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-235. VPDMA_int0_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT_STAT_VIP2_MULT_ANCB_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
5	INT_STAT_VIP2_MULT_ANCB_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP2_MULT_ANCB_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP2_MULT_ANCB_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP2_MULT_ANCB_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP2_MULT_ANCB_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP2_MULT_ANCB_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.24 VPDMA_int0_channel5_int_mask Register (offset = 6Ch) [reset = 0h]

VPDMA_int0_channel5_int_mask is shown in Figure 1-324 and described in Table 1-236.

Figure 1-324. VPDMA_int0_channel5_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_TRANSCODE2_CHROMA	INT_MASK_TRANSCODE2_LUMA	INT_MASK_TRANSCODE1_CHROMA	INT_MASK_TRANSCODE1_LUMA	INT_MASK_AUX_IN	INT_MASK_PIP_FRAME	INT_MASK_POST_COMP_WR	INT_MASK_VBI_SD_VENC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
Reserved	INT_MASK_NF_LAST_CHROMA	INT_MASK_NF_LAST_LUMA	INT_MASK_NF_WRITE_CHROMA	INT_MASK_NF_WRITE_LUMA	INT_MASK_NF_READ	INT_MASK_VIP2_PORTB_RGB	INT_MASK_VIP2_PORTA_RGB
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_PORTB_CHROMA	INT_MASK_VIP2_PORTB_LUMA	INT_MASK_VIP2_PORTA_CHROMA	INT_MASK_VIP2_PORTA_LUMA	INT_MASK_VIP2_MULT_ANCB_SRC15	INT_MASK_VIP2_MULT_ANCB_SRC14	INT_MASK_VIP2_MULT_ANCB_SRC13	INT_MASK_VIP2_MULT_ANCB_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_ANCB_SRC11	INT_MASK_VIP2_MULT_ANCB_SRC10	INT_MASK_VIP2_MULT_ANCB_SRC9	INT_MASK_VIP2_MULT_ANCB_SRC8	INT_MASK_VIP2_MULT_ANCB_SRC7	INT_MASK_VIP2_MULT_ANCB_SRC6	INT_MASK_VIP2_MULT_ANCB_SRC5	INT_MASK_VIP2_MULT_ANCB_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-236. VPDMA_int0_channel5_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_TRANSCODE2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_TRANSCODE2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_TRANSCODE1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_TRANSCODE1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_AUX_IN	R/W	0h	The interrupt for Auxilary Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_PIP_FRAME	R/W	0h	The interrupt for PIP Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_POST_COMP_WR	R/W	0h	The interrupt for Post Compositer Writeback to Memory should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VBI_SD_VENC	R/W	0h	The interrupt for SD Video Encoder VBI Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
23	Reserved	R	0h	
22	INT_MASK_NF_LAST_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_NF_LAST_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-236. VPDMA_int0_channel5_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_NF_WRITE_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_NF_WRITE_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_NF_READ	R/W	0h	The interrupt for Noise Filter Input Data 422 Interleaved should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_PORTB_RGB	R/W	0h	The interrupt for Video Input 2 Port B RGB Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_PORTA_RGB	R/W	0h	The interrupt for Video Input 2 Port A RGB Data should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_PORTB_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_PORTB_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_PORTA_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_PORTA_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP2_MULT_ANCB_SRC15	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP2_MULT_ANCB_SRC14	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_MULT_ANCB_SRC13	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_MULT_ANCB_SRC12	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_MULT_ANCB_SRC11	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_MULT_ANCB_SRC10	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP2_MULT_ANCB_SRC9	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP2_MULT_ANCB_SRC8	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP2_MULT_ANCB_SRC7	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

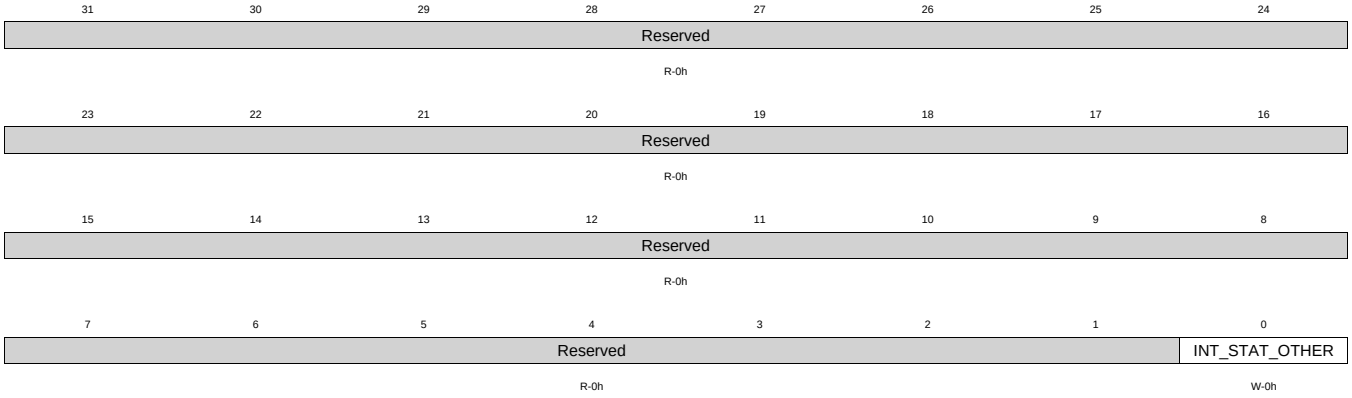
Table 1-236. VPDMA_int0_channel5_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP2_MULT_ANCB_SRC6	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP2_MULT_ANCB_SRC5	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP2_MULT_ANCB_SRC4	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.25 VPDMA_int0_channel6_int_stat Register (offset = 70h) [reset = 0h]

VPDMA_int0_channel6_int_stat is shown in Figure 1-325 and described in Table 1-237.

Figure 1-325. VPDMA_int0_channel6_int_stat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

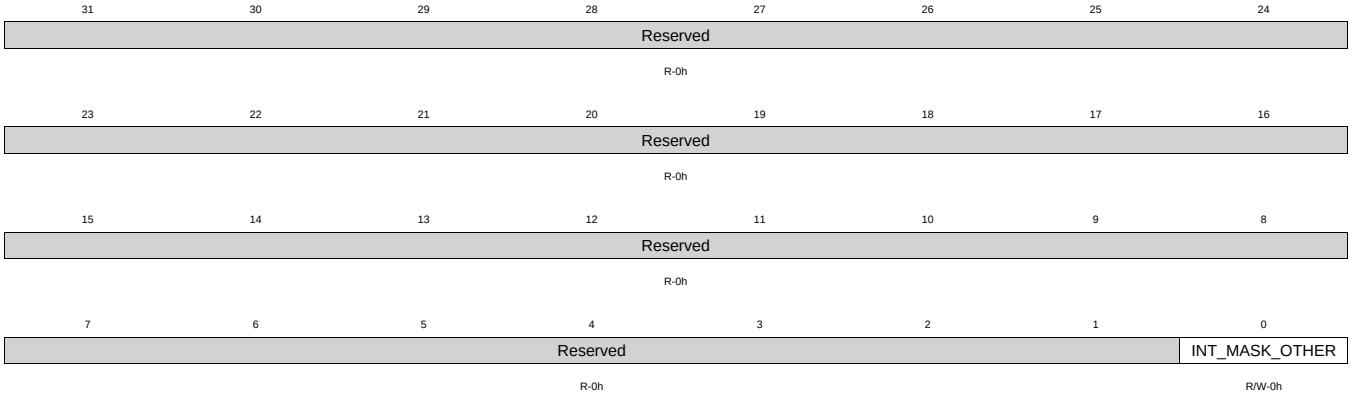
Table 1-237. VPDMA_int0_channel6_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	Reserved	R	0h	
0	INT_STAT_OTHER	W	0h	This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.26 VPDMA_int0_channel6_int_mask Register (offset = 74h) [reset = 0h]

VPDMA_int0_channel6_int_mask is shown in Figure 1-326 and described in Table 1-238.

Figure 1-326. VPDMA_int0_channel6_int_mask Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-238. VPDMA_int0_channel6_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	Reserved	R	0h	
0	INT_MASK_OTHER	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.27 VPDMA_int0_client0_int_stat Register (offset = 78h) [reset = 0h]

VPDMA_int0_client0_int_stat is shown in Figure 1-327 and described in Table 1-239.

Figure 1-327. VPDMA_int0_client0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_GRPX1_DATA	INT_STAT_COMP_WRBK	INT_STAT_SC_OUT	Reserved				
W-0h	W-0h	W-0h	R-0h				
23	22	21	20	19	18	17	16
Reserved			INT_STAT_SC_IN_LUMA	INT_STAT_SC_IN_CHROMA	INT_STAT_PIP_WRBK	INT_STAT_DEI_SC_OUT	Reserved
R-0h			W-0h	W-0h	W-0h	W-0h	R-0h
15	14	13	12	11	10	9	8
INT_STAT_DEI_HQ_MV_OUT	Reserved		INT_STAT_DEI_HQ_MV_IN	Reserved			
W-0h	R-0h		W-0h	R-0h			
7	6	5	4	3	2	1	0
Reserved		INT_STAT_DEI_HQ_3_CHROMA	INT_STAT_DEI_HQ_3_LUMA	INT_STAT_DEI_HQ_2_CHROMA	INT_STAT_DEI_HQ_2_LUMA	INT_STAT_DEI_HQ_1_LUMA	INT_STAT_DEI_HQ_1_CHROMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-239. VPDMA_int0_client0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_GRPX1_DATA	W	0h	The client interface grpx1_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_COMP_WRBK	W	0h	The client interface comp_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_SC_OUT	W	0h	The client interface sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28-21	Reserved	R	0h	
20	INT_STAT_SC_IN_LUMA	W	0h	The client interface sc_in_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_SC_IN_CHROMA	W	0h	The client interface sc_in_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-239. VPDMA_int0_client0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	INT_STAT_PIP_WRBK	W	0h	The client interface pip_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_DEI_SC_OUT	W	0h	The client interface dei_sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	Reserved	R	0h	
15	INT_STAT_DEI_HQ_MV_OUT	W	0h	The client interface dei_hq_mv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14-13	Reserved	R	0h	
12	INT_STAT_DEI_HQ_MV_IN	W	0h	The client interface dei_hq_mv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11-6	Reserved	R	0h	
5	INT_STAT_DEI_HQ_3_CHROMA	W	0h	The client interface dei_hq_3_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_DEI_HQ_3_LUMA	W	0h	The client interface dei_hq_3_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_DEI_HQ_2_CHROMA	W	0h	The client interface dei_hq_2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_DEI_HQ_2_LUMA	W	0h	The client interface dei_hq_2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

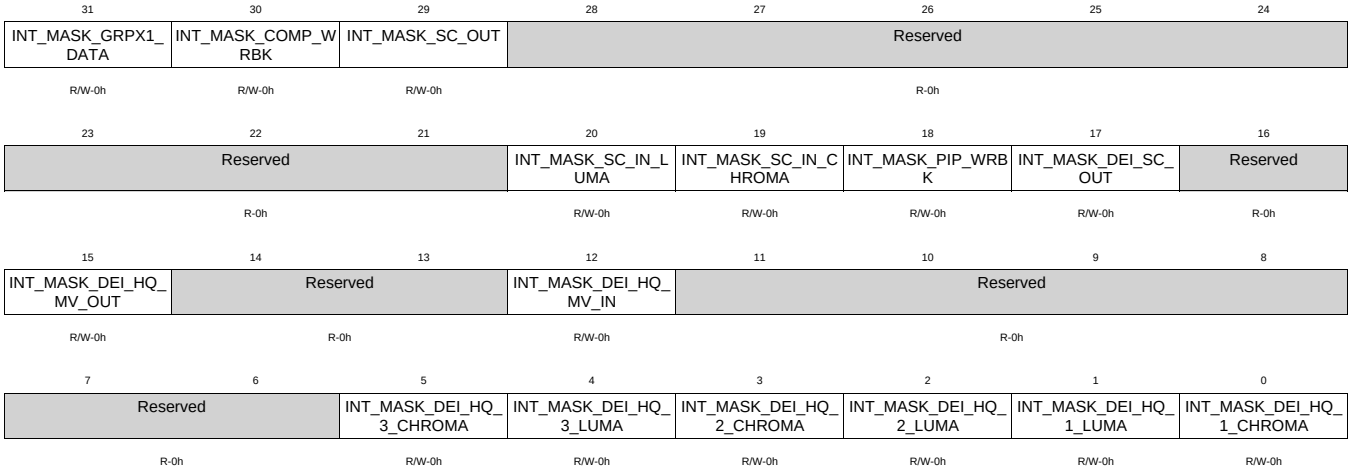
Table 1-239. VPDMA_int0_client0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_STAT_DEI_HQ_1_LUMA	W	0h	The client interface dei_hq_1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_DEI_HQ_1_CHROMA	W	0h	The client interface dei_hq_1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.28 VPDMA_int0_client0_int_mask Register (offset = 7Ch) [reset = 0h]

VPDMA_int0_client0_int_mask is shown in Figure 1-328 and described in Table 1-240.

Figure 1-328. VPDMA_int0_client0_int_mask Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-240. VPDMA_int0_client0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_GRPX1_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_COMP_WRBK	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_SC_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28-21	Reserved	R	0h	
20	INT_MASK_SC_IN_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_SC_IN_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_PIP_WRBK	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_DEI_SC_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	Reserved	R	0h	
15	INT_MASK_DEI_HQ_MV_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14-13	Reserved	R	0h	
12	INT_MASK_DEI_HQ_MV_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11-6	Reserved	R	0h	

Table 1-240. VPDMA_int0_client0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_MASK_DEI_HQ_3_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_DEI_HQ_3_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_DEI_HQ_2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_DEI_HQ_2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_DEI_HQ_1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_DEI_HQ_1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.29 VPDMA_int0_client1_int_stat Register (offset = 80h) [reset = 0h]

VPDMA_int0_client1_int_stat is shown in Figure 1-329 and described in Table 1-241.

Figure 1-329. VPDMA_int0_client1_int_stat Register

31	30	29	28	27	26	25	24
Reserved		INT_STAT_VIP2_ANC_B	INT_STAT_VIP2_ANC_A	INT_STAT_VIP1_ANC_B	INT_STAT_VIP1_ANC_A	INT_STAT_TRANS2_LUMA	INT_STAT_TRANS2_CHROMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_TRANS1_LUMA	INT_STAT_TRANS1_CHROMA	INT_STAT_HDMI_WRBK_OUT	INT_STAT_VPI_CTL	INT_STAT_VBI_SDVENC	Reserved	INT_STAT_NF_420_UV_OUT	INT_STAT_NF_420_Y_OUT
W-0h	W-0h	W-0h	W-0h	W-0h	R-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_NF_420_UV_IN	INT_STAT_NF_420_Y_IN	INT_STAT_NF_422_IN	INT_STAT_GRPX3_ST	INT_STAT_GRPX2_ST	INT_STAT_GRPX1_ST	INT_STAT_VIP2_UP_UV	INT_STAT_VIP2_UP_Y
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_LO_UV	INT_STAT_VIP2_LO_Y	INT_STAT_VIP1_UP_UV	INT_STAT_VIP1_UP_Y	INT_STAT_VIP1_LO_UV	INT_STAT_VIP1_LO_Y	INT_STAT_GRPX3_DATA	INT_STAT_GRPX2_DATA
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-241. VPDMA_int0_client1_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	INT_STAT_VIP2_ANC_B	W	0h	The client interface vip2_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_ANC_A	W	0h	The client interface vip2_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_ANC_B	W	0h	The client interface vip1_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_ANC_A	W	0h	The client interface vip1_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_TRANS2_LUMA	W	0h	The client interface trans2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-241. VPDMA_int0_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	INT_STAT_TRANS2_CHROMA	W	0h	The client interface trans2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_TRANS1_LUMA	W	0h	The client interface trans1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_TRANS1_CHROMA	W	0h	The client interface trans1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_HDMI_WRBK_OUT	W	0h	The client interface hdmi_wrbk_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VPI_CTL	W	0h	The client interface vpi_ctl has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VBI_SDVENC	W	0h	The client interface vbi_sdvenc has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	Reserved	R	0h	
17	INT_STAT_NF_420_UV_OUT	W	0h	The client interface nf_420_uv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_NF_420_Y_OUT	W	0h	The client interface nf_420_y_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_NF_420_UV_IN	W	0h	The client interface nf_420_uv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-241. VPDMA_int0_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	INT_STAT_NF_420_Y_IN	W	0h	The client interface nf_420_y_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_NF_422_IN	W	0h	The client interface nf_422_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_GRPX3_ST	W	0h	The client interface grpx3_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_GRPX2_ST	W	0h	The client interface grpx2_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_GRPX1_ST	W	0h	The client interface grpx1_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_UP_UV	W	0h	The client interface vip2_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_UP_Y	W	0h	The client interface vip2_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_LO_UV	W	0h	The client interface vip2_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP2_LO_Y	W	0h	The client interface vip2_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-241. VPDMA_int0_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_UP_UV	W	0h	The client interface vip1_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_UP_Y	W	0h	The client interface vip1_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_LO_UV	W	0h	The client interface vip1_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_LO_Y	W	0h	The client interface vip1_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_GRPX3_DATA	W	0h	The client interface grpx3_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_GRPX2_DATA	W	0h	The client interface grpx2_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.30 VPDMA_int0_client1_int_mask Register (offset = 84h) [reset = 0h]

VPDMA_int0_client1_int_mask is shown in Figure 1-330 and described in Table 1-242.

Figure 1-330. VPDMA_int0_client1_int_mask Register

31	30	29	28	27	26	25	24
Reserved		INT_MASK_VIP2_ANC_B	INT_MASK_VIP2_ANC_A	INT_MASK_VIP1_ANC_B	INT_MASK_VIP1_ANC_A	INT_MASK_TRANS2_LUMA	INT_MASK_TRANS2_CHROMA
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_TRANS1_LUMA	INT_MASK_TRANS1_CHROMA	INT_MASK_HDMI_WRBK_OUT	INT_MASK_VPI_CTL	INT_MASK_VBI_SDVENC	Reserved	INT_MASK_NF_420_UV_OUT	INT_MASK_NF_420_Y_OUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_NF_420_UV_IN	INT_MASK_NF_420_Y_IN	INT_MASK_NF_422_IN	INT_MASK_GRPX3_ST	INT_MASK_GRPX2_ST	INT_MASK_GRPX1_ST	INT_MASK_VIP2_UP_UV	INT_MASK_VIP2_UP_Y
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_LO_UV	INT_MASK_VIP2_LO_Y	INT_MASK_VIP1_UP_UV	INT_MASK_VIP1_UP_Y	INT_MASK_VIP1_LO_UV	INT_MASK_VIP1_LO_Y	INT_MASK_GRPX3_DATA	INT_MASK_GRPX2_DATA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-242. VPDMA_int0_client1_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	INT_MASK_VIP2_ANC_B	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_ANC_A	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_ANC_B	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_ANC_A	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_TRANS2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_TRANS2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_TRANS1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_TRANS1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_HDMI_WRBK_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
20	INT_MASK_VPI_CTL	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-242. VPDMA_int0_client1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	INT_MASK_VBI_SDVENC	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	Reserved	R	0h	
17	INT_MASK_NF_420_UV_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_NF_420_Y_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_NF_420_UV_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_NF_420_Y_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_NF_422_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_GRPX3_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_GRPX2_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_GRPX1_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_UP_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_UP_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_LO_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_LO_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_UP_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_UP_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_LO_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_VIP1_LO_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_GRPX3_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-242. VPDMA_int0_client1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT_MASK_GRPX2_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.31 VPDMA_int0_list0_int_stat Register (offset = 88h) [reset = 0h]

VPDMA_int0_list0_int_stat is shown in Figure 1-331 and described in Table 1-243.

Figure 1-331. VPDMA_int0_list0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_CONTROL_DESCRIPTOR_INT15	INT_STAT_CONTROL_DESCRIPTOR_INT14	INT_STAT_CONTROL_DESCRIPTOR_INT13	INT_STAT_CONTROL_DESCRIPTOR_INT12	INT_STAT_CONTROL_DESCRIPTOR_INT11	INT_STAT_CONTROL_DESCRIPTOR_INT10	INT_STAT_CONTROL_DESCRIPTOR_INT9	INT_STAT_CONTROL_DESCRIPTOR_INT8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_CONTROL_DESCRIPTOR_INT7	INT_STAT_CONTROL_DESCRIPTOR_INT6	INT_STAT_CONTROL_DESCRIPTOR_INT5	INT_STAT_CONTROL_DESCRIPTOR_INT4	INT_STAT_CONTROL_DESCRIPTOR_INT3	INT_STAT_CONTROL_DESCRIPTOR_INT2	INT_STAT_CONTROL_DESCRIPTOR_INT1	INT_STAT_CONTROL_DESCRIPTOR_INT0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_LIST7_NOTIFY	INT_STAT_LIST7_COMPLETE	INT_STAT_LIST6_NOTIFY	INT_STAT_LIST6_COMPLETE	INT_STAT_LIST5_NOTIFY	INT_STAT_LIST5_COMPLETE	INT_STAT_LIST4_NOTIFY	INT_STAT_LIST4_COMPLETE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_LIST3_NOTIFY	INT_STAT_LIST3_COMPLETE	INT_STAT_LIST2_NOTIFY	INT_STAT_LIST2_COMPLETE	INT_STAT_LIST1_NOTIFY	INT_STAT_LIST1_COMPLETE	INT_STAT_LIST0_NOTIFY	INT_STAT_LIST0_COMPLETE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-243. VPDMA_int0_list0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_CONTROL_DESCRIPTOR_INT15	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 15. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_CONTROL_DESCRIPTOR_INT14	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 14. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_CONTROL_DESCRIPTOR_INT13	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 13. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_CONTROL_DESCRIPTOR_INT12	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 12. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_CONTROL_DESCRIPTOR_INT11	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 11. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_CONTROL_DESCRIPTOR_INT10	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 10. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_CONTROL_DESCRIPTOR_INT9	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 9. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_CONTROL_DESCRIPTOR_INT8	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 8. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-243. VPDMA_int0_list0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	INT_STAT_CONTROL_DESCRIPTOR_INT7	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 7. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_CONTROL_DESCRIPTOR_INT6	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 6. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_CONTROL_DESCRIPTOR_INT5	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 5. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_CONTROL_DESCRIPTOR_INT4	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 4. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_CONTROL_DESCRIPTOR_INT3	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 3. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_CONTROL_DESCRIPTOR_INT2	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 2. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_CONTROL_DESCRIPTOR_INT1	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 1. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_CONTROL_DESCRIPTOR_INT0	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 0. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_LIST7_NOTIFY	W	0h	A channel set by List 7 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_LIST7_COMPLETE	W	0h	List 7 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_LIST6_NOTIFY	W	0h	A channel set by List 6 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_LIST6_COMPLETE	W	0h	List 6 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_LIST5_NOTIFY	W	0h	A channel set by List 5 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_LIST5_COMPLETE	W	0h	List 5 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_LIST4_NOTIFY	W	0h	A channel set by List 4 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-243. VPDMA_int0_list0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT_STAT_LIST4_COMPLETE	W	0h	List 4 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_LIST3_NOTIFY	W	0h	A channel set by List 3 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_LIST3_COMPLETE	W	0h	List 3 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
5	INT_STAT_LIST2_NOTIFY	W	0h	A channel set by List 2 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_LIST2_COMPLETE	W	0h	List 2 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_LIST1_NOTIFY	W	0h	A channel set by List 1 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_LIST1_COMPLETE	W	0h	List 1 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_LIST0_NOTIFY	W	0h	A channel set by List 0 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_LIST0_COMPLETE	W	0h	List 0 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.32 VPDMA_int0_list0_int_mask Register (offset = 8Ch) [reset = 0h]

VPDMA_int0_list0_int_mask is shown in Figure 1-332 and described in Table 1-244.

Figure 1-332. VPDMA_int0_list0_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_CONTROL_DESCRIPTOR_INT15	INT_MASK_CONTROL_DESCRIPTOR_INT14	INT_MASK_CONTROL_DESCRIPTOR_INT13	INT_MASK_CONTROL_DESCRIPTOR_INT12	INT_MASK_CONTROL_DESCRIPTOR_INT11	INT_MASK_CONTROL_DESCRIPTOR_INT10	INT_MASK_CONTROL_DESCRIPTOR_INT9	INT_MASK_CONTROL_DESCRIPTOR_INT8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_CONTROL_DESCRIPTOR_INT7	INT_MASK_CONTROL_DESCRIPTOR_INT6	INT_MASK_CONTROL_DESCRIPTOR_INT5	INT_MASK_CONTROL_DESCRIPTOR_INT4	INT_MASK_CONTROL_DESCRIPTOR_INT3	INT_MASK_CONTROL_DESCRIPTOR_INT2	INT_MASK_CONTROL_DESCRIPTOR_INT1	INT_MASK_CONTROL_DESCRIPTOR_INT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_LIST7_NOTIFY	INT_MASK_LIST7_COMPLETE	INT_MASK_LIST6_NOTIFY	INT_MASK_LIST6_COMPLETE	INT_MASK_LIST5_NOTIFY	INT_MASK_LIST5_COMPLETE	INT_MASK_LIST4_NOTIFY	INT_MASK_LIST4_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_LIST3_NOTIFY	INT_MASK_LIST3_COMPLETE	INT_MASK_LIST2_NOTIFY	INT_MASK_LIST2_COMPLETE	INT_MASK_LIST1_NOTIFY	INT_MASK_LIST1_COMPLETE	INT_MASK_LIST0_NOTIFY	INT_MASK_LIST0_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-244. VPDMA_int0_list0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_CONTROL_DESCRIPTOR_INT15	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_CONTROL_DESCRIPTOR_INT14	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_CONTROL_DESCRIPTOR_INT13	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_CONTROL_DESCRIPTOR_INT12	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_CONTROL_DESCRIPTOR_INT11	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_CONTROL_DESCRIPTOR_INT10	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_CONTROL_DESCRIPTOR_INT9	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_CONTROL_DESCRIPTOR_INT8	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_CONTROL_DESCRIPTOR_INT7	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_CONTROL_DESCRIPTOR_INT6	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-244. VPDMA_int0_list0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	INT_MASK_CONTROL_DESCRIPTOR_INT5	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
20	INT_MASK_CONTROL_DESCRIPTOR_INT4	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_CONTROL_DESCRIPTOR_INT3	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_CONTROL_DESCRIPTOR_INT2	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_CONTROL_DESCRIPTOR_INT1	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_CONTROL_DESCRIPTOR_INT0	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_LIST7_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_LIST7_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_LIST6_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_LIST6_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_LIST5_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_LIST5_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_LIST4_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_LIST4_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_LIST3_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_LIST3_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_LIST2_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_LIST2_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

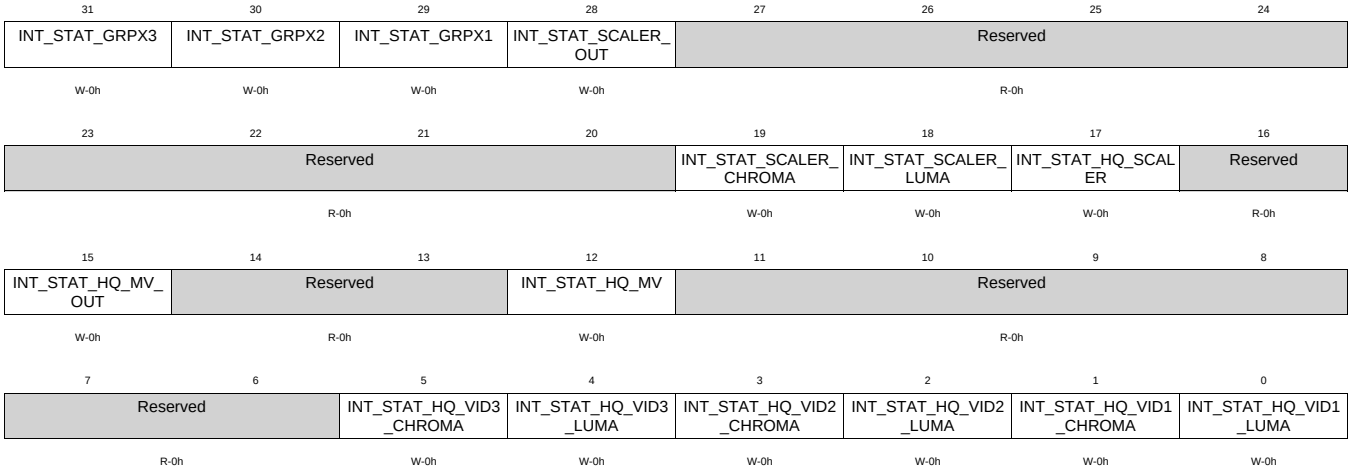
Table 1-244. VPDMA_int0_list0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT_MASK_LIST1_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_LIST1_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_LIST0_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_LIST0_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int0. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.33 VPDMA_int1_channel0_int_stat Register (offset = 90h) [reset = 0h]

VPDMA_int1_channel0_int_stat is shown in Figure 1-333 and described in Table 1-245.

Figure 1-333. VPDMA_int1_channel0_int_stat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-245. VPDMA_int1_channel0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_GRPX3	W	0h	The last read DMA transaction has occurred for channel grpx3 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_GRPX2	W	0h	The last read DMA transaction has occurred for channel grpx2 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_GRPX1	W	0h	The last read DMA transaction has occurred for channel grpx1 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_SCALER_OUT	W	0h	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27-20	Reserved	R	0h	
19	INT_STAT_SCALER_CHROMA	W	0h	The last write DMA transaction has completed for channel scaler_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-245. VPDMA_int1_channel0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	INT_STAT_SCALER_LUMA	W	0h	The last write DMA transaction has completed for channel scaler_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_HQ_SCALER	W	0h	The last write DMA transaction has completed for channel hq_scaler. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	Reserved	R	0h	
15	INT_STAT_HQ_MV_OUT	W	0h	The last write DMA transaction has completed for channel hq_mv_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_hq_mv_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14-13	Reserved	R	0h	
12	INT_STAT_HQ_MV	W	0h	The last read DMA transaction has occurred for channel hq_mv and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_hq_mv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11-6	Reserved	R	0h	
5	INT_STAT_HQ_VID3_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid3_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_3_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_HQ_VID3_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid3_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_3_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_HQ_VID2_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid2_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_2_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_HQ_VID2_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid2_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_2_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-245. VPDMA_int1_channel0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_STAT_HQ_VID1_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid1_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_1_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_HQ_VID1_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid1_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_1_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.34 VPDMA_int1_channel0_int_mask Register (offset = 94h) [reset = 0h]

VPDMA_int1_channel0_int_mask is shown in Figure 1-334 and described in Table 1-246.

Figure 1-334. VPDMA_int1_channel0_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_GRPX3	INT_MASK_GRPX2	INT_MASK_GRPX1	INT_MASK_SCALER_OUT	Reserved			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
Reserved				INT_MASK_SCALER_CHROMA	INT_MASK_SCALER_LUMA	INT_MASK_HQ_SCALER	Reserved
R-0h				R/W-0h	R/W-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
INT_MASK_HQ_MV_OUT	Reserved		INT_MASK_HQ_MV	Reserved			
R/W-0h	R-0h		R/W-0h	R-0h			
7	6	5	4	3	2	1	0
Reserved		INT_MASK_HQ_VID3_CHROMA	INT_MASK_HQ_VID3_LUMA	INT_MASK_HQ_VID2_CHROMA	INT_MASK_HQ_VID2_LUMA	INT_MASK_HQ_VID1_CHROMA	INT_MASK_HQ_VID1_LUMA
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-246. VPDMA_int1_channel0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_GRPX3	R/W	0h	The interrupt for Graphcis 2 Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_GRPX2	R/W	0h	The interrupt for Graphics 1 Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_GRPX1	R/W	0h	The interrupt for Graphics 0 Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_SCALER_OUT	R/W	0h	The interrupt for Low Cost DEI Scalar Write to Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
27-20	Reserved	R	0h	
19	INT_MASK_SCALER_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_SCALER_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_HQ_SCALER	R/W	0h	The interrupt for High Quality DEI Scaler Write to Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	Reserved	R	0h	
15	INT_MASK_HQ_MV_OUT	R/W	0h	The interrupt for Low Cost DEI Motion Vector Write should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14-13	Reserved	R	0h	
12	INT_MASK_HQ_MV	R/W	0h	The interrupt for Low Cost DEI Motion Vector should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11-6	Reserved	R	0h	

Table 1-246. VPDMA_int1_channel0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_MASK_HQ_VID3_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_HQ_VID3_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_HQ_VID2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_HQ_VID2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_HQ_VID1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_HQ_VID1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.35 VPDMA_int1_channel1_int_stat Register (offset = 98h) [reset = 0h]

VPDMA_int1_channel1_int_stat is shown in Figure 1-335 and described in Table 1-247.

Figure 1-335. VPDMA_int1_channel1_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP1_MULT_PORTB_SRC9	INT_STAT_VIP1_MULT_PORTB_SRC8	INT_STAT_VIP1_MULT_PORTB_SRC7	INT_STAT_VIP1_MULT_PORTB_SRC6	INT_STAT_VIP1_MULT_PORTB_SRC5	INT_STAT_VIP1_MULT_PORTB_SRC4	INT_STAT_VIP1_MULT_PORTB_SRC3	INT_STAT_VIP1_MULT_PORTB_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP1_MULT_PORTB_SRC1	INT_STAT_VIP1_MULT_PORTB_SRC0	INT_STAT_VIP1_MULT_PORTA_SRC15	INT_STAT_VIP1_MULT_PORTA_SRC14	INT_STAT_VIP1_MULT_PORTA_SRC13	INT_STAT_VIP1_MULT_PORTA_SRC12	INT_STAT_VIP1_MULT_PORTA_SRC11	INT_STAT_VIP1_MULT_PORTA_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP1_MULT_PORTA_SRC9	INT_STAT_VIP1_MULT_PORTA_SRC8	INT_STAT_VIP1_MULT_PORTA_SRC7	INT_STAT_VIP1_MULT_PORTA_SRC6	INT_STAT_VIP1_MULT_PORTA_SRC5	INT_STAT_VIP1_MULT_PORTA_SRC4	INT_STAT_VIP1_MULT_PORTA_SRC3	INT_STAT_VIP1_MULT_PORTA_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_PORTA_SRC1	INT_STAT_VIP1_MULT_PORTA_SRC0	INT_STAT_GRPX3_CLUT	INT_STAT_GRPX2_CLUT	INT_STAT_GRPX1_CLUT	INT_STAT_GRPX3_STENCIL	INT_STAT_GRPX2_STENCIL	INT_STAT_GRPX1_STENCIL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-247. VPDMA_int1_channel1_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP1_MULT_PORTB_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP1_MULT_PORTB_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP1_MULT_PORTB_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP1_MULT_PORTB_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_MULT_PORTB_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_MULT_PORTB_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-247. VPDMA_int1_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP1_MULT_PORTB_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP1_MULT_PORTB_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP1_MULT_PORTB_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP1_MULT_PORTB_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP1_MULT_PORTA_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP1_MULT_PORTA_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP1_MULT_PORTA_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP1_MULT_PORTA_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP1_MULT_PORTA_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP1_MULT_PORTA_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-247. VPDMA_int1_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP1_MULT_PORTA_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP1_MULT_PORTA_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP1_MULT_PORTA_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP1_MULT_PORTA_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_MULT_PORTA_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_MULT_PORTA_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_MULT_PORTA_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_MULT_PORTA_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_MULT_PORTA_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_MULT_PORTA_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-247. VPDMA_int1_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_GRPX3_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx3_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_GRPX2_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx2_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_GRPX1_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx1_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_GRPX3_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx3_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_GRPX2_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx2_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_GRPX1_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx1_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.36 VPDMA_int1_channel1_int_mask Register (offset = 9Ch) [reset = 0h]

VPDMA_int1_channel1_int_mask is shown in Figure 1-336 and described in Table 1-248.

Figure 1-336. VPDMA_int1_channel1_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP1_MULT_PORTB_SRC9	INT_MASK_VIP1_MULT_PORTB_SRC8	INT_MASK_VIP1_MULT_PORTB_SRC7	INT_MASK_VIP1_MULT_PORTB_SRC6	INT_MASK_VIP1_MULT_PORTB_SRC5	INT_MASK_VIP1_MULT_PORTB_SRC4	INT_MASK_VIP1_MULT_PORTB_SRC3	INT_MASK_VIP1_MULT_PORTB_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP1_MULT_PORTB_SRC1	INT_MASK_VIP1_MULT_PORTB_SRC0	INT_MASK_VIP1_MULT_PORTA_SRC15	INT_MASK_VIP1_MULT_PORTA_SRC14	INT_MASK_VIP1_MULT_PORTA_SRC13	INT_MASK_VIP1_MULT_PORTA_SRC12	INT_MASK_VIP1_MULT_PORTA_SRC11	INT_MASK_VIP1_MULT_PORTA_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP1_MULT_PORTA_SRC9	INT_MASK_VIP1_MULT_PORTA_SRC8	INT_MASK_VIP1_MULT_PORTA_SRC7	INT_MASK_VIP1_MULT_PORTA_SRC6	INT_MASK_VIP1_MULT_PORTA_SRC5	INT_MASK_VIP1_MULT_PORTA_SRC4	INT_MASK_VIP1_MULT_PORTA_SRC3	INT_MASK_VIP1_MULT_PORTA_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_PORTA_SRC1	INT_MASK_VIP1_MULT_PORTA_SRC0	INT_MASK_GRPX3_CLUT	INT_MASK_GRPX2_CLUT	INT_MASK_GRPX1_CLUT	INT_MASK_GRPX3_STENCIL	INT_MASK_GRPX2_STENCIL	INT_MASK_GRPX1_STENCIL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-248. VPDMA_int1_channel1_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP1_MULT_PORTB_SRC9	R/W	0h	The interrupt for Video Input 1 Port B Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP1_MULT_PORTB_SRC8	R/W	0h	The interrupt for Video Input 1 Port B Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP1_MULT_PORTB_SRC7	R/W	0h	The interrupt for Video Input 1 Port B Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP1_MULT_PORTB_SRC6	R/W	0h	The interrupt for Video Input 1 Port B Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_MULT_PORTB_SRC5	R/W	0h	The interrupt for Video Input 1 Port B Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_MULT_PORTB_SRC4	R/W	0h	The interrupt for Video Input 1 Port B Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP1_MULT_PORTB_SRC3	R/W	0h	The interrupt for Video Input 1 Port B Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP1_MULT_PORTB_SRC2	R/W	0h	The interrupt for Video Input 1 Port B Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP1_MULT_PORTB_SRC1	R/W	0h	The interrupt for Video Input 1 Port B Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP1_MULT_PORTB_SRC0	R/W	0h	The interrupt for Video Input 1 Port B Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP1_MULT_PORTA_SRC15	R/W	0h	The interrupt for Video Input 1 Port A Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-248. VPDMA_int1_channel1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP1_MULT_PORTA_SRC14	R/W	0h	The interrupt for Video Input 1 Port A Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP1_MULT_PORTA_SRC13	R/W	0h	The interrupt for Video Input 1 Port A Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP1_MULT_PORTA_SRC12	R/W	0h	The interrupt for Video Input 1 Port A Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP1_MULT_PORTA_SRC11	R/W	0h	The interrupt for Video Input 1 Port A Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP1_MULT_PORTA_SRC10	R/W	0h	The interrupt for Video Input 1 Port A Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP1_MULT_PORTA_SRC9	R/W	0h	The interrupt for Video Input 1 Port A Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP1_MULT_PORTA_SRC8	R/W	0h	The interrupt for Video Input 1 Port A Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP1_MULT_PORTA_SRC7	R/W	0h	The interrupt for Video Input 1 Port A Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP1_MULT_PORTA_SRC6	R/W	0h	The interrupt for Video Input 1 Port A Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_MULT_PORTA_SRC5	R/W	0h	The interrupt for Video Input 1 Port A Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_MULT_PORTA_SRC4	R/W	0h	The interrupt for Video Input 1 Port A Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_MULT_PORTA_SRC3	R/W	0h	The interrupt for Video Input 1 Port A Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_MULT_PORTA_SRC2	R/W	0h	The interrupt for Video Input 1 Port A Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_MULT_PORTA_SRC1	R/W	0h	The interrupt for Video Input 1 Port A Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_MULT_PORTA_SRC0	R/W	0h	The interrupt for Video Input 1 Port A Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_GRPX3_CLUT	R/W	0h	The interrupt for Graphics 2 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_GRPX2_CLUT	R/W	0h	The interrupt for Graphics 1 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_GRPX1_CLUT	R/W	0h	The interrupt for Graphics 0 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-248. VPDMA_int1_channel1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_GRPX3_STENCIL	R/W	0h	The interrupt for Graphics 2 Stencil should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_GRPX2_STENCIL	R/W	0h	The interrupt for Graphics 1 Stencil should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_GRPX1_STENCIL	R/W	0h	The interrupt for Graphics 0 Stencil should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.37 VPDMA_int1_channel2_int_stat Register (offset = A0h) [reset = 0h]

VPDMA_int1_channel2_int_stat is shown in Figure 1-337 and described in Table 1-249.

Figure 1-337. VPDMA_int1_channel2_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP1_MULT_ANCB_SRC9	INT_STAT_VIP1_MULT_ANCB_SRC8	INT_STAT_VIP1_MULT_ANCB_SRC7	INT_STAT_VIP1_MULT_ANCB_SRC6	INT_STAT_VIP1_MULT_ANCB_SRC5	INT_STAT_VIP1_MULT_ANCB_SRC4	INT_STAT_VIP1_MULT_ANCB_SRC3	INT_STAT_VIP1_MULT_ANCB_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP1_MULT_ANCB_SRC1	INT_STAT_VIP1_MULT_ANCB_SRC0	INT_STAT_VIP1_MULT_ANCA_SRC15	INT_STAT_VIP1_MULT_ANCA_SRC14	INT_STAT_VIP1_MULT_ANCA_SRC13	INT_STAT_VIP1_MULT_ANCA_SRC12	INT_STAT_VIP1_MULT_ANCA_SRC11	INT_STAT_VIP1_MULT_ANCA_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP1_MULT_ANCA_SRC9	INT_STAT_VIP1_MULT_ANCA_SRC8	INT_STAT_VIP1_MULT_ANCA_SRC7	INT_STAT_VIP1_MULT_ANCA_SRC6	INT_STAT_VIP1_MULT_ANCA_SRC5	INT_STAT_VIP1_MULT_ANCA_SRC4	INT_STAT_VIP1_MULT_ANCA_SRC3	INT_STAT_VIP1_MULT_ANCA_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_ANCA_SRC1	INT_STAT_VIP1_MULT_ANCA_SRC0	INT_STAT_VIP1_MULT_PORTB_SRC15	INT_STAT_VIP1_MULT_PORTB_SRC14	INT_STAT_VIP1_MULT_PORTB_SRC13	INT_STAT_VIP1_MULT_PORTB_SRC12	INT_STAT_VIP1_MULT_PORTB_SRC11	INT_STAT_VIP1_MULT_PORTB_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-249. VPDMA_int1_channel2_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP1_MULT_ANCB_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP1_MULT_ANCB_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP1_MULT_ANCB_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP1_MULT_ANCB_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_MULT_ANCB_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_MULT_ANCB_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-249. VPDMA_int1_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP1_MULT_ANCB_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP1_MULT_ANCB_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP1_MULT_ANCB_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP1_MULT_ANCB_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP1_MULT_ANCA_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP1_MULT_ANCA_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP1_MULT_ANCA_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP1_MULT_ANCA_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP1_MULT_ANCA_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP1_MULT_ANCA_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-249. VPDMA_int1_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP1_MULT_ANCA_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP1_MULT_ANCA_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP1_MULT_ANCA_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP1_MULT_ANCA_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_MULT_ANCA_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_MULT_ANCA_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_MULT_ANCA_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_MULT_ANCA_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_MULT_ANCA_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_MULT_ANCA_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-249. VPDMA_int1_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_MULT_PORTB_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_MULT_PORTB_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_MULT_PORTB_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_MULT_PORTB_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP1_MULT_PORTB_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP1_MULT_PORTB_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.38 VPDMA_int1_channel2_int_mask Register (offset = A4h) [reset = 0h]

VPDMA_int1_channel2_int_mask is shown in Figure 1-338 and described in Table 1-250.

Figure 1-338. VPDMA_int1_channel2_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP1_MULT_ANCB_SRC9	INT_MASK_VIP1_MULT_ANCB_SRC8	INT_MASK_VIP1_MULT_ANCB_SRC7	INT_MASK_VIP1_MULT_ANCB_SRC6	INT_MASK_VIP1_MULT_ANCB_SRC5	INT_MASK_VIP1_MULT_ANCB_SRC4	INT_MASK_VIP1_MULT_ANCB_SRC3	INT_MASK_VIP1_MULT_ANCB_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP1_MULT_ANCB_SRC1	INT_MASK_VIP1_MULT_ANCB_SRC0	INT_MASK_VIP1_MULT_ANCA_SRC15	INT_MASK_VIP1_MULT_ANCA_SRC14	INT_MASK_VIP1_MULT_ANCA_SRC13	INT_MASK_VIP1_MULT_ANCA_SRC12	INT_MASK_VIP1_MULT_ANCA_SRC11	INT_MASK_VIP1_MULT_ANCA_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP1_MULT_ANCA_SRC9	INT_MASK_VIP1_MULT_ANCA_SRC8	INT_MASK_VIP1_MULT_ANCA_SRC7	INT_MASK_VIP1_MULT_ANCA_SRC6	INT_MASK_VIP1_MULT_ANCA_SRC5	INT_MASK_VIP1_MULT_ANCA_SRC4	INT_MASK_VIP1_MULT_ANCA_SRC3	INT_MASK_VIP1_MULT_ANCA_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_ANCA_SRC1	INT_MASK_VIP1_MULT_ANCA_SRC0	INT_MASK_VIP1_MULT_PORTB_SRC15	INT_MASK_VIP1_MULT_PORTB_SRC14	INT_MASK_VIP1_MULT_PORTB_SRC13	INT_MASK_VIP1_MULT_PORTB_SRC12	INT_MASK_VIP1_MULT_PORTB_SRC11	INT_MASK_VIP1_MULT_PORTB_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-250. VPDMA_int1_channel2_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP1_MULT_ANCB_SRC9	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP1_MULT_ANCB_SRC8	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP1_MULT_ANCB_SRC7	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP1_MULT_ANCB_SRC6	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_MULT_ANCB_SRC5	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_MULT_ANCB_SRC4	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP1_MULT_ANCB_SRC3	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP1_MULT_ANCB_SRC2	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP1_MULT_ANCB_SRC1	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP1_MULT_ANCB_SRC0	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP1_MULT_ANCA_SRC15	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-250. VPDMA_int1_channel2_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP1_MULT_ANCA_SRC14	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP1_MULT_ANCA_SRC13	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP1_MULT_ANCA_SRC12	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP1_MULT_ANCA_SRC11	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP1_MULT_ANCA_SRC10	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP1_MULT_ANCA_SRC9	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP1_MULT_ANCA_SRC8	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP1_MULT_ANCA_SRC7	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP1_MULT_ANCA_SRC6	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_MULT_ANCA_SRC5	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_MULT_ANCA_SRC4	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_MULT_ANCA_SRC3	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_MULT_ANCA_SRC2	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_MULT_ANCA_SRC1	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_MULT_ANCA_SRC0	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_MULT_PORTB_SRC15	R/W	0h	The interrupt for Video Input 1 Port B Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_MULT_PORTB_SRC14	R/W	0h	The interrupt for Video Input 1 Port B Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_MULT_PORTB_SRC13	R/W	0h	The interrupt for Video Input 1 Port B Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-250. VPDMA_int1_channel2_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP1_MULT_PORTB_SRC12	R/W	0h	The interrupt for Video Input 1 Port B Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP1_MULT_PORTB_SRC11	R/W	0h	The interrupt for Video Input 1 Port B Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP1_MULT_PORTB_SRC10	R/W	0h	The interrupt for Video Input 1 Port B Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.39 VPDMA_int1_channel3_int_stat Register (offset = A8h) [reset = 0h]

VPDMA_int1_channel3_int_stat is shown in Figure 1-339 and described in Table 1-251.

Figure 1-339. VPDMA_int1_channel3_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP2_MULT_PORTB_SRC3	INT_STAT_VIP2_MULT_PORTB_SRC2	INT_STAT_VIP2_MULT_PORTB_SRC1	INT_STAT_VIP2_MULT_PORTB_SRC0	INT_STAT_VIP2_MULT_PORTA_SRC15	INT_STAT_VIP2_MULT_PORTA_SRC14	INT_STAT_VIP2_MULT_PORTA_SRC13	INT_STAT_VIP2_MULT_PORTA_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP2_MULT_PORTA_SRC11	INT_STAT_VIP2_MULT_PORTA_SRC10	INT_STAT_VIP2_MULT_PORTA_SRC9	INT_STAT_VIP2_MULT_PORTA_SRC8	INT_STAT_VIP2_MULT_PORTA_SRC7	INT_STAT_VIP2_MULT_PORTA_SRC6	INT_STAT_VIP2_MULT_PORTA_SRC5	INT_STAT_VIP2_MULT_PORTA_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_MULT_PORTA_SRC3	INT_STAT_VIP2_MULT_PORTA_SRC2	INT_STAT_VIP2_MULT_PORTA_SRC1	INT_STAT_VIP2_MULT_PORTA_SRC0	INT_STAT_VIP1_PORTB_RGB	INT_STAT_VIP1_PORTA_RGB	INT_STAT_VIP1_PORTB_CHROMA	INT_STAT_VIP1_PORTB_LUMA
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_PORTA_CHROMA	INT_STAT_VIP1_PORTA_LUMA	INT_STAT_VIP1_MULT_ANCB_SRC15	INT_STAT_VIP1_MULT_ANCB_SRC14	INT_STAT_VIP1_MULT_ANCB_SRC13	INT_STAT_VIP1_MULT_ANCB_SRC12	INT_STAT_VIP1_MULT_ANCB_SRC11	INT_STAT_VIP1_MULT_ANCB_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-251. VPDMA_int1_channel3_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP2_MULT_PORTB_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP2_MULT_PORTB_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP2_MULT_PORTB_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_MULT_PORTB_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP2_MULT_PORTA_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP2_MULT_PORTA_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-251. VPDMA_int1_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP2_MULT_PORTA_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP2_MULT_PORTA_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP2_MULT_PORTA_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP2_MULT_PORTA_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP2_MULT_PORTA_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP2_MULT_PORTA_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP2_MULT_PORTA_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP2_MULT_PORTA_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_MULT_PORTA_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP2_MULT_PORTA_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-251. VPDMA_int1_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP2_MULT_PORTA_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_MULT_PORTA_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_MULT_PORTA_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_MULT_PORTA_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_PORTB_RGB	W	0h	The last write DMA transaction has completed for channel vip1_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_PORTA_RGB	W	0h	The last write DMA transaction has completed for channel vip1_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_PORTB_CHROMA	W	0h	The last write DMA transaction has completed for channel vip1_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_PORTB_LUMA	W	0h	The last write DMA transaction has completed for channel vip1_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_PORTA_CHROMA	W	0h	The last write DMA transaction has completed for channel vip1_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_PORTA_LUMA	W	0h	The last write DMA transaction has completed for channel vip1_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-251. VPDMA_int1_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_MULT_ANCB_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_MULT_ANCB_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_MULT_ANCB_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_MULT_ANCB_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP1_MULT_ANCB_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP1_MULT_ANCB_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.40 VPDMA_int1_channel3_int_mask Register (offset = ACh) [reset = 0h]

VPDMA_int1_channel3_int_mask is shown in Figure 1-340 and described in Table 1-252.

Figure 1-340. VPDMA_int1_channel3_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP2_MULT_PORTB_SRC3	INT_MASK_VIP2_MULT_PORTB_SRC2	INT_MASK_VIP2_MULT_PORTB_SRC1	INT_MASK_VIP2_MULT_PORTB_SRC0	INT_MASK_VIP2_MULT_PORTA_SRC15	INT_MASK_VIP2_MULT_PORTA_SRC14	INT_MASK_VIP2_MULT_PORTA_SRC13	INT_MASK_VIP2_MULT_PORTA_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP2_MULT_PORTA_SRC11	INT_MASK_VIP2_MULT_PORTA_SRC10	INT_MASK_VIP2_MULT_PORTA_SRC9	INT_MASK_VIP2_MULT_PORTA_SRC8	INT_MASK_VIP2_MULT_PORTA_SRC7	INT_MASK_VIP2_MULT_PORTA_SRC6	INT_MASK_VIP2_MULT_PORTA_SRC5	INT_MASK_VIP2_MULT_PORTA_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_MULT_PORTA_SRC3	INT_MASK_VIP2_MULT_PORTA_SRC2	INT_MASK_VIP2_MULT_PORTA_SRC1	INT_MASK_VIP2_MULT_PORTA_SRC0	INT_MASK_VIP1_PORTB_RGB	INT_MASK_VIP1_PORTA_RGB	INT_MASK_VIP1_PORTB_CHROMA	INT_MASK_VIP1_PORTB_LUMA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_PORTA_CHROMA	INT_MASK_VIP1_PORTA_LUMA	INT_MASK_VIP1_MULT_ANCB_SRC15	INT_MASK_VIP1_MULT_ANCB_SRC14	INT_MASK_VIP1_MULT_ANCB_SRC13	INT_MASK_VIP1_MULT_ANCB_SRC12	INT_MASK_VIP1_MULT_ANCB_SRC11	INT_MASK_VIP1_MULT_ANCB_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-252. VPDMA_int1_channel3_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP2_MULT_PORTB_SRC3	R/W	0h	The interrupt for Video Input 2 Port B Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP2_MULT_PORTB_SRC2	R/W	0h	The interrupt for Video Input 2 Port B Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP2_MULT_PORTB_SRC1	R/W	0h	The interrupt for Video Input 2 Port B Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_MULT_PORTB_SRC0	R/W	0h	The interrupt for Video Input 2 Port B Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP2_MULT_PORTA_SRC15	R/W	0h	The interrupt for Video Input 2 Port A Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP2_MULT_PORTA_SRC14	R/W	0h	The interrupt for Video Input 2 Port A Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP2_MULT_PORTA_SRC13	R/W	0h	The interrupt for Video Input 2 Port A Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP2_MULT_PORTA_SRC12	R/W	0h	The interrupt for Video Input 2 Port A Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP2_MULT_PORTA_SRC11	R/W	0h	The interrupt for Video Input 2 Port A Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP2_MULT_PORTA_SRC10	R/W	0h	The interrupt for Video Input 2 Port A Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP2_MULT_PORTA_SRC9	R/W	0h	The interrupt for Video Input 2 Port A Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-252. VPDMA_int1_channel3_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP2_MULT_PORTA_SRC8	R/W	0h	The interrupt for Video Input 2 Port A Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP2_MULT_PORTA_SRC7	R/W	0h	The interrupt for Video Input 2 Port A Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP2_MULT_PORTA_SRC6	R/W	0h	The interrupt for Video Input 2 Port A Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_MULT_PORTA_SRC5	R/W	0h	The interrupt for Video Input 2 Port A Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_MULT_PORTA_SRC4	R/W	0h	The interrupt for Video Input 2 Port A Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_MULT_PORTA_SRC3	R/W	0h	The interrupt for Video Input 2 Port A Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_MULT_PORTA_SRC2	R/W	0h	The interrupt for Video Input 2 Port A Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_MULT_PORTA_SRC1	R/W	0h	The interrupt for Video Input 2 Port A Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_MULT_PORTA_SRC0	R/W	0h	The interrupt for Video Input 2 Port A Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_PORTB_RGB	R/W	0h	The interrupt for Video Input 1 Port B RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_PORTA_RGB	R/W	0h	The interrupt for Video Input 1 Port A RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_PORTB_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_PORTB_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_PORTA_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_PORTA_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_MULT_ANCB_SRC15	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_MULT_ANCB_SRC14	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_MULT_ANCB_SRC13	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-252. VPDMA_int1_channel3_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP1_MULT_ANCB_SRC12	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP1_MULT_ANCB_SRC11	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP1_MULT_ANCB_SRC10	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.41 VPDMA_int1_channel4_int_stat Register (offset = B0h) [reset = 0h]

VPDMA_int1_channel4_int_stat is shown in Figure 1-341 and described in Table 1-253.

Figure 1-341. VPDMA_int1_channel4_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP2_MULT_ANCB_SRC3	INT_STAT_VIP2_MULT_ANCB_SRC2	INT_STAT_VIP2_MULT_ANCB_SRC1	INT_STAT_VIP2_MULT_ANCB_SRC0	INT_STAT_VIP2_MULT_ANCA_SRC15	INT_STAT_VIP2_MULT_ANCA_SRC14	INT_STAT_VIP2_MULT_ANCA_SRC13	INT_STAT_VIP2_MULT_ANCA_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP2_MULT_ANCA_SRC11	INT_STAT_VIP2_MULT_ANCA_SRC10	INT_STAT_VIP2_MULT_ANCA_SRC9	INT_STAT_VIP2_MULT_ANCA_SRC8	INT_STAT_VIP2_MULT_ANCA_SRC7	INT_STAT_VIP2_MULT_ANCA_SRC6	INT_STAT_VIP2_MULT_ANCA_SRC5	INT_STAT_VIP2_MULT_ANCA_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_MULT_ANCA_SRC3	INT_STAT_VIP2_MULT_ANCA_SRC2	INT_STAT_VIP2_MULT_ANCA_SRC1	INT_STAT_VIP2_MULT_ANCA_SRC0	INT_STAT_VIP2_MULT_PORTB_SRC15	INT_STAT_VIP2_MULT_PORTB_SRC14	INT_STAT_VIP2_MULT_PORTB_SRC13	INT_STAT_VIP2_MULT_PORTB_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_PORTB_SRC11	INT_STAT_VIP2_MULT_PORTB_SRC10	INT_STAT_VIP2_MULT_PORTB_SRC9	INT_STAT_VIP2_MULT_PORTB_SRC8	INT_STAT_VIP2_MULT_PORTB_SRC7	INT_STAT_VIP2_MULT_PORTB_SRC6	INT_STAT_VIP2_MULT_PORTB_SRC5	INT_STAT_VIP2_MULT_PORTB_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-253. VPDMA_int1_channel4_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP2_MULT_ANCB_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP2_MULT_ANCB_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP2_MULT_ANCB_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_MULT_ANCB_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP2_MULT_ANCA_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP2_MULT_ANCA_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-253. VPDMA_int1_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP2_MULT_ANCA_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP2_MULT_ANCA_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP2_MULT_ANCA_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP2_MULT_ANCA_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP2_MULT_ANCA_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP2_MULT_ANCA_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP2_MULT_ANCA_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP2_MULT_ANCA_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_MULT_ANCA_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP2_MULT_ANCA_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-253. VPDMA_int1_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP2_MULT_ANCA_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_MULT_ANCA_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_MULT_ANCA_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_MULT_ANCA_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP2_MULT_PORTB_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP2_MULT_PORTB_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_MULT_PORTB_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_MULT_PORTB_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_MULT_PORTB_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP2_MULT_PORTB_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-253. VPDMA_int1_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP2_MULT_PORTB_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP2_MULT_PORTB_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP2_MULT_PORTB_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP2_MULT_PORTB_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP2_MULT_PORTB_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP2_MULT_PORTB_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.42 VPDMA_int1_channel4_int_mask Register (offset = B4h) [reset = 0h]

VPDMA_int1_channel4_int_mask is shown in Figure 1-342 and described in Table 1-254.

Figure 1-342. VPDMA_int1_channel4_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP2_MULT_ANCB_SRC3	INT_MASK_VIP2_MULT_ANCB_SRC2	INT_MASK_VIP2_MULT_ANCB_SRC1	INT_MASK_VIP2_MULT_ANCB_SRC0	INT_MASK_VIP2_MULT_ANCA_SRC15	INT_MASK_VIP2_MULT_ANCA_SRC14	INT_MASK_VIP2_MULT_ANCA_SRC13	INT_MASK_VIP2_MULT_ANCA_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP2_MULT_ANCA_SRC11	INT_MASK_VIP2_MULT_ANCA_SRC10	INT_MASK_VIP2_MULT_ANCA_SRC9	INT_MASK_VIP2_MULT_ANCA_SRC8	INT_MASK_VIP2_MULT_ANCA_SRC7	INT_MASK_VIP2_MULT_ANCA_SRC6	INT_MASK_VIP2_MULT_ANCA_SRC5	INT_MASK_VIP2_MULT_ANCA_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_MULT_ANCA_SRC3	INT_MASK_VIP2_MULT_ANCA_SRC2	INT_MASK_VIP2_MULT_ANCA_SRC1	INT_MASK_VIP2_MULT_ANCA_SRC0	INT_MASK_VIP2_MULT_PORTB_SRC15	INT_MASK_VIP2_MULT_PORTB_SRC14	INT_MASK_VIP2_MULT_PORTB_SRC13	INT_MASK_VIP2_MULT_PORTB_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_PORTB_SRC11	INT_MASK_VIP2_MULT_PORTB_SRC10	INT_MASK_VIP2_MULT_PORTB_SRC9	INT_MASK_VIP2_MULT_PORTB_SRC8	INT_MASK_VIP2_MULT_PORTB_SRC7	INT_MASK_VIP2_MULT_PORTB_SRC6	INT_MASK_VIP2_MULT_PORTB_SRC5	INT_MASK_VIP2_MULT_PORTB_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-254. VPDMA_int1_channel4_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP2_MULT_ANCB_SRC3	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP2_MULT_ANCB_SRC2	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP2_MULT_ANCB_SRC1	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_MULT_ANCB_SRC0	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP2_MULT_ANCA_SRC15	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP2_MULT_ANCA_SRC14	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP2_MULT_ANCA_SRC13	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP2_MULT_ANCA_SRC12	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP2_MULT_ANCA_SRC11	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP2_MULT_ANCA_SRC10	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP2_MULT_ANCA_SRC9	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-254. VPDMA_int1_channel4_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP2_MULT_ANCA_SRC8	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP2_MULT_ANCA_SRC7	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP2_MULT_ANCA_SRC6	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_MULT_ANCA_SRC5	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_MULT_ANCA_SRC4	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_MULT_ANCA_SRC3	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_MULT_ANCA_SRC2	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_MULT_ANCA_SRC1	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_MULT_ANCA_SRC0	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP2_MULT_PORTB_SRC15	R/W	0h	The interrupt for Video Input 2 Port B Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP2_MULT_PORTB_SRC14	R/W	0h	The interrupt for Video Input 2 Port B Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_MULT_PORTB_SRC13	R/W	0h	The interrupt for Video Input 2 Port B Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_MULT_PORTB_SRC12	R/W	0h	The interrupt for Video Input 2 Port B Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_MULT_PORTB_SRC11	R/W	0h	The interrupt for Video Input 2 Port B Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_MULT_PORTB_SRC10	R/W	0h	The interrupt for Video Input 2 Port B Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP2_MULT_PORTB_SRC9	R/W	0h	The interrupt for Video Input 2 Port B Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP2_MULT_PORTB_SRC8	R/W	0h	The interrupt for Video Input 2 Port B Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP2_MULT_PORTB_SRC7	R/W	0h	The interrupt for Video Input 2 Port B Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-254. VPDMA_int1_channel4_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP2_MULT_PORTB_SRC6	R/W	0h	The interrupt for Video Input 2 Port B Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP2_MULT_PORTB_SRC5	R/W	0h	The interrupt for Video Input 2 Port B Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP2_MULT_PORTB_SRC4	R/W	0h	The interrupt for Video Input 2 Port B Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.43 VPDMA_int1_channel5_int_stat Register (offset = B8h) [reset = 0h]

VPDMA_int1_channel5_int_stat is shown in Figure 1-343 and described in Table 1-255.

Figure 1-343. VPDMA_int1_channel5_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_TRANSCODE2_CHROMA	INT_STAT_TRANSCODE2_LUMA	INT_STAT_TRANSCODE1_CHROMA	INT_STAT_TRANSCODE1_LUMA	INT_STAT_AUX_IN	INT_STAT_PIP_FRAME	INT_STAT_POST_COMP_WR	INT_STAT_VBI_SD_VENC
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
Reserved	INT_STAT_NF_LAST_CHROMA	INT_STAT_NF_LAST_LUMA	INT_STAT_NF_WRITE_CHROMA	INT_STAT_NF_WRITE_LUMA	INT_STAT_NF_READ	INT_STAT_VIP2_PORTB_RGB	INT_STAT_VIP2_PORTA_RGB
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_PORTB_CHROMA	INT_STAT_VIP2_PORTB_LUMA	INT_STAT_VIP2_PORTA_CHROMA	INT_STAT_VIP2_PORTA_LUMA	INT_STAT_VIP2_MULT_ANCB_SRC15	INT_STAT_VIP2_MULT_ANCB_SRC14	INT_STAT_VIP2_MULT_ANCB_SRC13	INT_STAT_VIP2_MULT_ANCB_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_ANCB_SRC11	INT_STAT_VIP2_MULT_ANCB_SRC10	INT_STAT_VIP2_MULT_ANCB_SRC9	INT_STAT_VIP2_MULT_ANCB_SRC8	INT_STAT_VIP2_MULT_ANCB_SRC7	INT_STAT_VIP2_MULT_ANCB_SRC6	INT_STAT_VIP2_MULT_ANCB_SRC5	INT_STAT_VIP2_MULT_ANCB_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-255. VPDMA_int1_channel5_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_TRANSCODE2_CHROMA	W	0h	The last read DMA transaction has occurred for channel transcode2_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans2_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_TRANSCODE2_LUMA	W	0h	The last read DMA transaction has occurred for channel transcode2_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans2_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_TRANSCODE1_CHROMA	W	0h	The last read DMA transaction has occurred for channel transcode1_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans1_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_TRANSCODE1_LUMA	W	0h	The last read DMA transaction has occurred for channel transcode1_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans1_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_AUX_IN	W	0h	The last read DMA transaction has occurred for channel aux_in and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client comp_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-255. VPDMA_int1_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	INT_STAT_PIP_FRAME	W	0h	The last read DMA transaction has occurred for channel pip_frame and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client pip_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_POST_COMP_WR	W	0h	The last write DMA transaction has completed for channel post_comp_wr. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client hdmi_wrbk_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VBI_SD_VENC	W	0h	The last read DMA transaction has occurred for channel vbi_sd_venc and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client vbi_sdvenc will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	Reserved	R	0h	
22	INT_STAT_NF_LAST_CHROMA	W	0h	The last read DMA transaction has occurred for channel nf_last_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_420_uv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_NF_LAST_LUMA	W	0h	The last read DMA transaction has occurred for channel nf_last_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_420_y_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_NF_WRITE_CHROMA	W	0h	The last write DMA transaction has completed for channel nf_write_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_NF_WRITE_LUMA	W	0h	The last write DMA transaction has completed for channel nf_write_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_NF_READ	W	0h	The last read DMA transaction has occurred for channel nf_read and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_422_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_PORTB_RGB	W	0h	The last write DMA transaction has completed for channel vip2_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-255. VPDMA_int1_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	INT_STAT_VIP2_PORTA_RGB	W	0h	The last write DMA transaction has completed for channel vip2_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_VIP2_PORTB_CHROMA	W	0h	The last write DMA transaction has completed for channel vip2_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_PORTB_LUMA	W	0h	The last write DMA transaction has completed for channel vip2_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_PORTA_CHROMA	W	0h	The last write DMA transaction has completed for channel vip2_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_PORTA_LUMA	W	0h	The last write DMA transaction has completed for channel vip2_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP2_MULT_ANCB_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP2_MULT_ANCB_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_MULT_ANCB_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_MULT_ANCB_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_MULT_ANCB_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-255. VPDMA_int1_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT_STAT_VIP2_MULT_ANCB_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
5	INT_STAT_VIP2_MULT_ANCB_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP2_MULT_ANCB_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP2_MULT_ANCB_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP2_MULT_ANCB_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP2_MULT_ANCB_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP2_MULT_ANCB_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.44 VPDMA_int1_channel5_int_mask Register (offset = BCh) [reset = 0h]

VPDMA_int1_channel5_int_mask is shown in Figure 1-344 and described in Table 1-256.

Figure 1-344. VPDMA_int1_channel5_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_TRANSCODE2_CHROMA	INT_MASK_TRANSCODE2_LUMA	INT_MASK_TRANSCODE1_CHROMA	INT_MASK_TRANSCODE1_LUMA	INT_MASK_AUX_IN	INT_MASK_PIP_FRAME	INT_MASK_POST_COMP_WR	INT_MASK_VBI_SD_VENC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
Reserved	INT_MASK_NF_LAST_CHROMA	INT_MASK_NF_LAST_LUMA	INT_MASK_NF_WRITE_CHROMA	INT_MASK_NF_WRITE_LUMA	INT_MASK_NF_READ	INT_MASK_VIP2_PORTB_RGB	INT_MASK_VIP2_PORTA_RGB
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_PORTB_CHROMA	INT_MASK_VIP2_PORTB_LUMA	INT_MASK_VIP2_PORTA_CHROMA	INT_MASK_VIP2_PORTA_LUMA	INT_MASK_VIP2_MULT_ANCB_SRC15	INT_MASK_VIP2_MULT_ANCB_SRC14	INT_MASK_VIP2_MULT_ANCB_SRC13	INT_MASK_VIP2_MULT_ANCB_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_ANCB_SRC11	INT_MASK_VIP2_MULT_ANCB_SRC10	INT_MASK_VIP2_MULT_ANCB_SRC9	INT_MASK_VIP2_MULT_ANCB_SRC8	INT_MASK_VIP2_MULT_ANCB_SRC7	INT_MASK_VIP2_MULT_ANCB_SRC6	INT_MASK_VIP2_MULT_ANCB_SRC5	INT_MASK_VIP2_MULT_ANCB_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-256. VPDMA_int1_channel5_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_TRANSCODE2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_TRANSCODE2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_TRANSCODE1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_TRANSCODE1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_AUX_IN	R/W	0h	The interrupt for Auxilary Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_PIP_FRAME	R/W	0h	The interrupt for PIP Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_POST_COMP_WR	R/W	0h	The interrupt for Post Compositer Writeback to Memory should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VBI_SD_VENC	R/W	0h	The interrupt for SD Video Encoder VBI Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
23	Reserved	R	0h	
22	INT_MASK_NF_LAST_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_NF_LAST_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-256. VPDMA_int1_channel5_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_NF_WRITE_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_NF_WRITE_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_NF_READ	R/W	0h	The interrupt for Noise Filter Input Data 422 Interleaved should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_PORTB_RGB	R/W	0h	The interrupt for Video Input 2 Port B RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_PORTA_RGB	R/W	0h	The interrupt for Video Input 2 Port A RGB Data should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_PORTB_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_PORTB_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_PORTA_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_PORTA_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP2_MULT_ANCB_SRC15	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP2_MULT_ANCB_SRC14	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_MULT_ANCB_SRC13	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_MULT_ANCB_SRC12	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_MULT_ANCB_SRC11	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_MULT_ANCB_SRC10	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP2_MULT_ANCB_SRC9	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP2_MULT_ANCB_SRC8	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP2_MULT_ANCB_SRC7	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-256. VPDMA_int1_channel5_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP2_MULT_ANCB_SRC6	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP2_MULT_ANCB_SRC5	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP2_MULT_ANCB_SRC4	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.45 VPDMA_int1_channel6_int_stat Register (offset = C0h) [reset = 0h]

VPDMA_int1_channel6_int_stat is shown in Figure 1-345 and described in Table 1-257.

Figure 1-345. VPDMA_int1_channel6_int_stat Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved							INT_STAT_OTHER
R-0h							W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

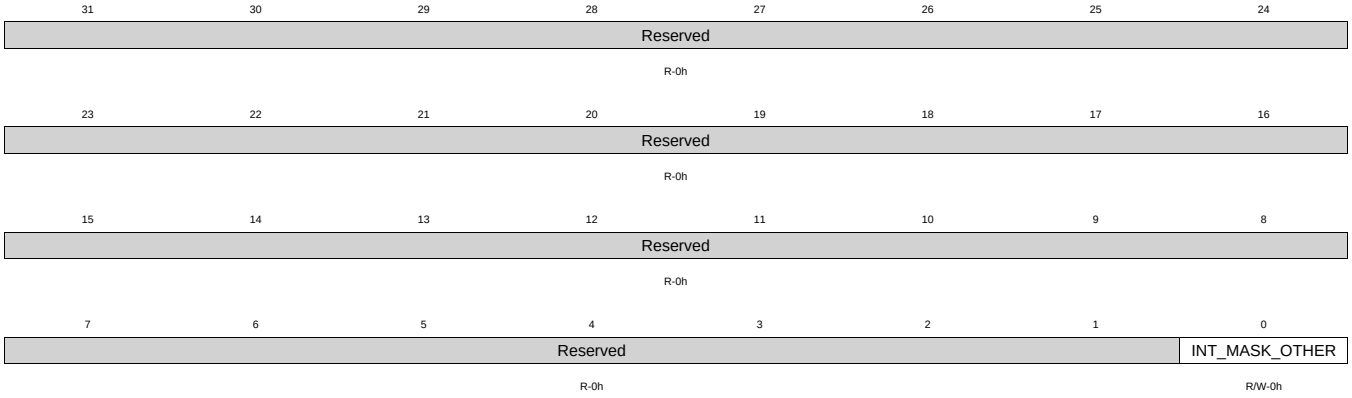
Table 1-257. VPDMA_int1_channel6_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	Reserved	R	0h	
0	INT_STAT_OTHER	W	0h	This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.46 VPDMA_int1_channel6_int_mask Register (offset = C4h) [reset = 0h]

VPDMA_int1_channel6_int_mask is shown in Figure 1-346 and described in Table 1-258.

Figure 1-346. VPDMA_int1_channel6_int_mask Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-258. VPDMA_int1_channel6_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	Reserved	R	0h	
0	INT_MASK_OTHER	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.47 VPDMA_int1_client0_int_stat Register (offset = C8h) [reset = 0h]

VPDMA_int1_client0_int_stat is shown in Figure 1-347 and described in Table 1-259.

Figure 1-347. VPDMA_int1_client0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_GRPX1_DATA	INT_STAT_COMP_WRBK	INT_STAT_SC_OUT	Reserved				
W-0h	W-0h	W-0h	R-0h				
23	22	21	20	19	18	17	16
Reserved			INT_STAT_SC_IN_LUMA	INT_STAT_SC_IN_CHROMA	INT_STAT_PIP_WRBK	INT_STAT_DEI_SC_OUT	Reserved
R-0h			W-0h	W-0h	W-0h	W-0h	R-0h
15	14	13	12	11	10	9	8
INT_STAT_DEI_HQ_MV_OUT	Reserved		INT_STAT_DEI_HQ_MV_IN	Reserved			
W-0h	R-0h		W-0h	R-0h			
7	6	5	4	3	2	1	0
Reserved		INT_STAT_DEI_HQ_3_CHROMA	INT_STAT_DEI_HQ_3_LUMA	INT_STAT_DEI_HQ_2_CHROMA	INT_STAT_DEI_HQ_2_LUMA	INT_STAT_DEI_HQ_1_LUMA	INT_STAT_DEI_HQ_1_CHROMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-259. VPDMA_int1_client0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_GRPX1_DATA	W	0h	The client interface grpx1_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_COMP_WRBK	W	0h	The client interface comp_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_SC_OUT	W	0h	The client interface sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28-21	Reserved	R	0h	
20	INT_STAT_SC_IN_LUMA	W	0h	The client interface sc_in_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_SC_IN_CHROMA	W	0h	The client interface sc_in_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-259. VPDMA_int1_client0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	INT_STAT_PIP_WRBK	W	0h	The client interface pip_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_DEI_SC_OUT	W	0h	The client interface dei_sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	Reserved	R	0h	
15	INT_STAT_DEI_HQ_MV_OUT	W	0h	The client interface dei_hq_mv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14-13	Reserved	R	0h	
12	INT_STAT_DEI_HQ_MV_IN	W	0h	The client interface dei_hq_mv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11-6	Reserved	R	0h	
5	INT_STAT_DEI_HQ_3_CHROMA	W	0h	The client interface dei_hq_3_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_DEI_HQ_3_LUMA	W	0h	The client interface dei_hq_3_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_DEI_HQ_2_CHROMA	W	0h	The client interface dei_hq_2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_DEI_HQ_2_LUMA	W	0h	The client interface dei_hq_2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-259. VPDMA_int1_client0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_STAT_DEI_HQ_1_LUMA	W	0h	The client interface dei_hq_1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_DEI_HQ_1_CHROMA	W	0h	The client interface dei_hq_1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.48 VPDMA_int1_client0_int_mask Register (offset = CCh) [reset = 0h]

VPDMA_int1_client0_int_mask is shown in Figure 1-348 and described in Table 1-260.

Figure 1-348. VPDMA_int1_client0_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_GRPX1_DATA	INT_MASK_COMP_WRBK	INT_MASK_SC_OUT	Reserved				
R/W-0h	R/W-0h	R/W-0h	R-0h				
23	22	21	20	19	18	17	16
Reserved			INT_MASK_SC_IN_LUMA	INT_MASK_SC_IN_CHROMA	INT_MASK_PIP_WRBK	INT_MASK_DEI_SC_OUT	Reserved
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
INT_MASK_DEI_HQ_MV_OUT	Reserved		INT_MASK_DEI_HQ_MV_IN	Reserved			
R/W-0h	R-0h		R/W-0h	R-0h			
7	6	5	4	3	2	1	0
Reserved		INT_MASK_DEI_HQ_3_CHROMA	INT_MASK_DEI_HQ_3_LUMA	INT_MASK_DEI_HQ_2_CHROMA	INT_MASK_DEI_HQ_2_LUMA	INT_MASK_DEI_HQ_1_LUMA	INT_MASK_DEI_HQ_1_CHROMA
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-260. VPDMA_int1_client0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_GRPX1_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_COMP_WRBK	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_SC_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28-21	Reserved	R	0h	
20	INT_MASK_SC_IN_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_SC_IN_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_PIP_WRBK	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_DEI_SC_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	Reserved	R	0h	
15	INT_MASK_DEI_HQ_MV_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14-13	Reserved	R	0h	
12	INT_MASK_DEI_HQ_MV_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11-6	Reserved	R	0h	

Table 1-260. VPDMA_int1_client0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_MASK_DEI_HQ_3_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_DEI_HQ_3_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_DEI_HQ_2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_DEI_HQ_2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_DEI_HQ_1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_DEI_HQ_1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.49 VPDMA_int1_client1_int_stat Register (offset = D0h) [reset = 0h]

VPDMA_int1_client1_int_stat is shown in Figure 1-349 and described in Table 1-261.

Figure 1-349. VPDMA_int1_client1_int_stat Register

31	30	29	28	27	26	25	24
Reserved		INT_STAT_VIP2_ANC_B	INT_STAT_VIP2_ANC_A	INT_STAT_VIP1_ANC_B	INT_STAT_VIP1_ANC_A	INT_STAT_TRANS2_LUMA	INT_STAT_TRANS2_CHROMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_TRANS1_LUMA	INT_STAT_TRANS1_CHROMA	INT_STAT_HDMI_WRBK_OUT	INT_STAT_VPI_CTL	INT_STAT_VBI_SDVENC	Reserved	INT_STAT_NF_420_UV_OUT	INT_STAT_NF_420_Y_OUT
W-0h	W-0h	W-0h	W-0h	W-0h	R-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_NF_420_UV_IN	INT_STAT_NF_420_Y_IN	INT_STAT_NF_422_IN	INT_STAT_GRPX3_ST	INT_STAT_GRPX2_ST	INT_STAT_GRPX1_ST	INT_STAT_VIP2_UP_UV	INT_STAT_VIP2_UP_Y
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_LO_UV	INT_STAT_VIP2_LO_Y	INT_STAT_VIP1_UP_UV	INT_STAT_VIP1_UP_Y	INT_STAT_VIP1_LO_UV	INT_STAT_VIP1_LO_Y	INT_STAT_GRPX3_DATA	INT_STAT_GRPX2_DATA
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-261. VPDMA_int1_client1_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	INT_STAT_VIP2_ANC_B	W	0h	The client interface vip2_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_ANC_A	W	0h	The client interface vip2_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_ANC_B	W	0h	The client interface vip1_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_ANC_A	W	0h	The client interface vip1_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_TRANS2_LUMA	W	0h	The client interface trans2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-261. VPDMA_int1_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	INT_STAT_TRANS2_CHROMA	W	0h	The client interface trans2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_TRANS1_LUMA	W	0h	The client interface trans1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_TRANS1_CHROMA	W	0h	The client interface trans1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_HDMI_WRBK_OUT	W	0h	The client interface hdmi_wrbk_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VPI_CTL	W	0h	The client interface vpi_ctl has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VBI_SDVENC	W	0h	The client interface vbi_sdvenc has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	Reserved	R	0h	
17	INT_STAT_NF_420_UV_OUT	W	0h	The client interface nf_420_uv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_NF_420_Y_OUT	W	0h	The client interface nf_420_y_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_NF_420_UV_IN	W	0h	The client interface nf_420_uv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-261. VPDMA_int1_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	INT_STAT_NF_420_Y_IN	W	0h	The client interface nf_420_y_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_NF_422_IN	W	0h	The client interface nf_422_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_GRPX3_ST	W	0h	The client interface grpx3_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_GRPX2_ST	W	0h	The client interface grpx2_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_GRPX1_ST	W	0h	The client interface grpx1_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_UP_UV	W	0h	The client interface vip2_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_UP_Y	W	0h	The client interface vip2_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_LO_UV	W	0h	The client interface vip2_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP2_LO_Y	W	0h	The client interface vip2_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-261. VPDMA_int1_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_UP_UV	W	0h	The client interface vip1_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_UP_Y	W	0h	The client interface vip1_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_LO_UV	W	0h	The client interface vip1_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_LO_Y	W	0h	The client interface vip1_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_GRPX3_DATA	W	0h	The client interface grpx3_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_GRPX2_DATA	W	0h	The client interface grpx2_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.50 VPDMA_int1_client1_int_mask Register (offset = D4h) [reset = 0h]

VPDMA_int1_client1_int_mask is shown in Figure 1-350 and described in Table 1-262.

Figure 1-350. VPDMA_int1_client1_int_mask Register

31	30	29	28	27	26	25	24
Reserved		INT_MASK_VIP2_ANC_B	INT_MASK_VIP2_ANC_A	INT_MASK_VIP1_ANC_B	INT_MASK_VIP1_ANC_A	INT_MASK_TRANS2_LUMA	INT_MASK_TRANS2_CHROMA
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_TRANS1_LUMA	INT_MASK_TRANS1_CHROMA	INT_MASK_HDMI_WRBK_OUT	INT_MASK_VPI_CTL	INT_MASK_VBI_SDVENC	Reserved	INT_MASK_NF_420_UV_OUT	INT_MASK_NF_420_Y_OUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_NF_420_UV_IN	INT_MASK_NF_420_Y_IN	INT_MASK_NF_422_IN	INT_MASK_GRPX3_ST	INT_MASK_GRPX2_ST	INT_MASK_GRPX1_ST	INT_MASK_VIP2_UP_UV	INT_MASK_VIP2_UP_Y
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_LO_UV	INT_MASK_VIP2_LO_Y	INT_MASK_VIP1_UP_UV	INT_MASK_VIP1_UP_Y	INT_MASK_VIP1_LO_UV	INT_MASK_VIP1_LO_Y	INT_MASK_GRPX3_DATA	INT_MASK_GRPX2_DATA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-262. VPDMA_int1_client1_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	INT_MASK_VIP2_ANC_B	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_ANC_A	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_ANC_B	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_ANC_A	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_TRANS2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_TRANS2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_TRANS1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_TRANS1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_HDMI_WRBK_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
20	INT_MASK_VPI_CTL	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-262. VPDMA_int1_client1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	INT_MASK_VBI_SDVENC	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	Reserved	R	0h	
17	INT_MASK_NF_420_UV_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_NF_420_Y_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_NF_420_UV_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_NF_420_Y_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_NF_422_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_GRPX3_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_GRPX2_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_GRPX1_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_UP_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_UP_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_LO_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_LO_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_UP_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_UP_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_LO_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_VIP1_LO_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_GRPX3_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-262. VPDMA_int1_client1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT_MASK_GRPX2_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.51 VPDMA_int1_list0_int_stat Register (offset = D8h) [reset = 0h]

VPDMA_int1_list0_int_stat is shown in Figure 1-351 and described in Table 1-263.

Figure 1-351. VPDMA_int1_list0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_CONTROL_DESCRIPTOR_INT15	INT_STAT_CONTROL_DESCRIPTOR_INT14	INT_STAT_CONTROL_DESCRIPTOR_INT13	INT_STAT_CONTROL_DESCRIPTOR_INT12	INT_STAT_CONTROL_DESCRIPTOR_INT11	INT_STAT_CONTROL_DESCRIPTOR_INT10	INT_STAT_CONTROL_DESCRIPTOR_INT9	INT_STAT_CONTROL_DESCRIPTOR_INT8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_CONTROL_DESCRIPTOR_INT7	INT_STAT_CONTROL_DESCRIPTOR_INT6	INT_STAT_CONTROL_DESCRIPTOR_INT5	INT_STAT_CONTROL_DESCRIPTOR_INT4	INT_STAT_CONTROL_DESCRIPTOR_INT3	INT_STAT_CONTROL_DESCRIPTOR_INT2	INT_STAT_CONTROL_DESCRIPTOR_INT1	INT_STAT_CONTROL_DESCRIPTOR_INT0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_LIST7_NOTIFY	INT_STAT_LIST7_COMPLETE	INT_STAT_LIST6_NOTIFY	INT_STAT_LIST6_COMPLETE	INT_STAT_LIST5_NOTIFY	INT_STAT_LIST5_COMPLETE	INT_STAT_LIST4_NOTIFY	INT_STAT_LIST4_COMPLETE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_LIST3_NOTIFY	INT_STAT_LIST3_COMPLETE	INT_STAT_LIST2_NOTIFY	INT_STAT_LIST2_COMPLETE	INT_STAT_LIST1_NOTIFY	INT_STAT_LIST1_COMPLETE	INT_STAT_LIST0_NOTIFY	INT_STAT_LIST0_COMPLETE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-263. VPDMA_int1_list0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_CONTROL_DESCRIPTOR_INT15	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 15. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_CONTROL_DESCRIPTOR_INT14	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 14. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_CONTROL_DESCRIPTOR_INT13	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 13. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_CONTROL_DESCRIPTOR_INT12	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 12. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_CONTROL_DESCRIPTOR_INT11	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 11. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_CONTROL_DESCRIPTOR_INT10	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 10. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_CONTROL_DESCRIPTOR_INT9	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 9. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_CONTROL_DESCRIPTOR_INT8	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 8. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-263. VPDMA_int1_list0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	INT_STAT_CONTROL_DESCRIPTOR_INT7	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 7. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_CONTROL_DESCRIPTOR_INT6	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 6. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_CONTROL_DESCRIPTOR_INT5	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 5. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_CONTROL_DESCRIPTOR_INT4	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 4. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_CONTROL_DESCRIPTOR_INT3	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 3. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_CONTROL_DESCRIPTOR_INT2	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 2. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_CONTROL_DESCRIPTOR_INT1	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 1. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_CONTROL_DESCRIPTOR_INT0	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 0. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_LIST7_NOTIFY	W	0h	A channel set by List 7 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_LIST7_COMPLETE	W	0h	List 7 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_LIST6_NOTIFY	W	0h	A channel set by List 6 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_LIST6_COMPLETE	W	0h	List 6 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_LIST5_NOTIFY	W	0h	A channel set by List 5 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_LIST5_COMPLETE	W	0h	List 5 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_LIST4_NOTIFY	W	0h	A channel set by List 4 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-263. VPDMA_int1_list0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT_STAT_LIST4_COMPLETE	W	0h	List 4 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_LIST3_NOTIFY	W	0h	A channel set by List 3 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_LIST3_COMPLETE	W	0h	List 3 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
5	INT_STAT_LIST2_NOTIFY	W	0h	A channel set by List 2 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_LIST2_COMPLETE	W	0h	List 2 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_LIST1_NOTIFY	W	0h	A channel set by List 1 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_LIST1_COMPLETE	W	0h	List 1 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_LIST0_NOTIFY	W	0h	A channel set by List 0 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_LIST0_COMPLETE	W	0h	List 0 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.52 VPDMA_int1_list0_int_mask Register (offset = DCh) [reset = 0h]

VPDMA_int1_list0_int_mask is shown in Figure 1-352 and described in Table 1-264.

Figure 1-352. VPDMA_int1_list0_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_CONTROL_DESCRIPTOR_INT15	INT_MASK_CONTROL_DESCRIPTOR_INT14	INT_MASK_CONTROL_DESCRIPTOR_INT13	INT_MASK_CONTROL_DESCRIPTOR_INT12	INT_MASK_CONTROL_DESCRIPTOR_INT11	INT_MASK_CONTROL_DESCRIPTOR_INT10	INT_MASK_CONTROL_DESCRIPTOR_INT9	INT_MASK_CONTROL_DESCRIPTOR_INT8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_CONTROL_DESCRIPTOR_INT7	INT_MASK_CONTROL_DESCRIPTOR_INT6	INT_MASK_CONTROL_DESCRIPTOR_INT5	INT_MASK_CONTROL_DESCRIPTOR_INT4	INT_MASK_CONTROL_DESCRIPTOR_INT3	INT_MASK_CONTROL_DESCRIPTOR_INT2	INT_MASK_CONTROL_DESCRIPTOR_INT1	INT_MASK_CONTROL_DESCRIPTOR_INT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_LIST7_NOTIFY	INT_MASK_LIST7_COMPLETE	INT_MASK_LIST6_NOTIFY	INT_MASK_LIST6_COMPLETE	INT_MASK_LIST5_NOTIFY	INT_MASK_LIST5_COMPLETE	INT_MASK_LIST4_NOTIFY	INT_MASK_LIST4_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_LIST3_NOTIFY	INT_MASK_LIST3_COMPLETE	INT_MASK_LIST2_NOTIFY	INT_MASK_LIST2_COMPLETE	INT_MASK_LIST1_NOTIFY	INT_MASK_LIST1_COMPLETE	INT_MASK_LIST0_NOTIFY	INT_MASK_LIST0_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-264. VPDMA_int1_list0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_CONTROL_DESCRIPTOR_INT15	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_CONTROL_DESCRIPTOR_INT14	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_CONTROL_DESCRIPTOR_INT13	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_CONTROL_DESCRIPTOR_INT12	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_CONTROL_DESCRIPTOR_INT11	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_CONTROL_DESCRIPTOR_INT10	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_CONTROL_DESCRIPTOR_INT9	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_CONTROL_DESCRIPTOR_INT8	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_CONTROL_DESCRIPTOR_INT7	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_CONTROL_DESCRIPTOR_INT6	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-264. VPDMA_int1_list0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	INT_MASK_CONTROL_DESCRIPTOR_INT5	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
20	INT_MASK_CONTROL_DESCRIPTOR_INT4	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_CONTROL_DESCRIPTOR_INT3	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_CONTROL_DESCRIPTOR_INT2	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_CONTROL_DESCRIPTOR_INT1	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_CONTROL_DESCRIPTOR_INT0	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_LIST7_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_LIST7_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_LIST6_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_LIST6_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_LIST5_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_LIST5_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_LIST4_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_LIST4_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_LIST3_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_LIST3_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_LIST2_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_LIST2_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

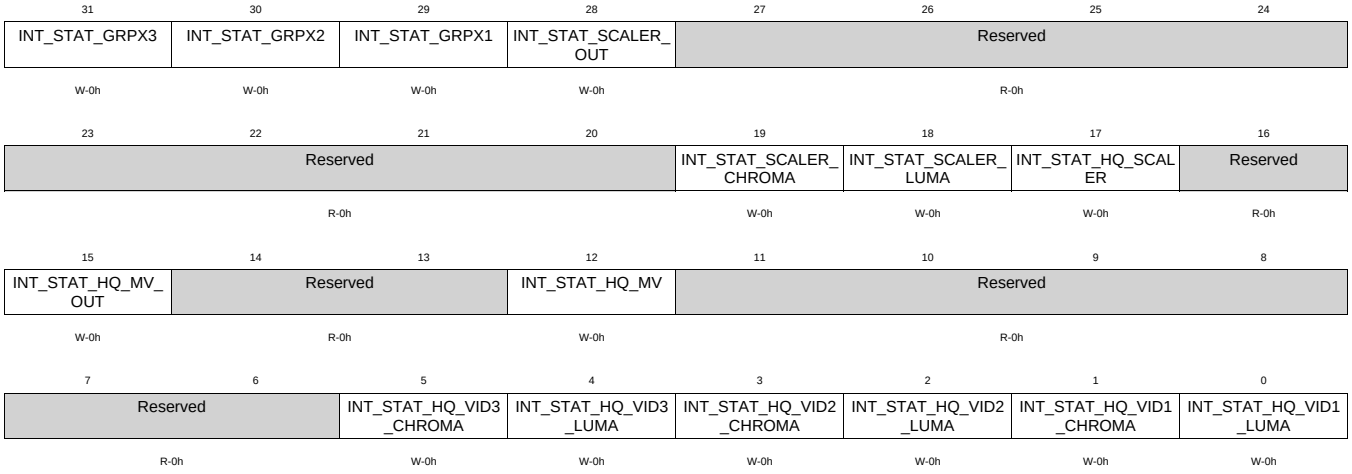
Table 1-264. VPDMA_int1_list0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT_MASK_LIST1_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_LIST1_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_LIST0_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_LIST0_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int1. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.53 VPDMA_int2_channel0_int_stat Register (offset = E0h) [reset = 0h]

VPDMA_int2_channel0_int_stat is shown in Figure 1-353 and described in Table 1-265.

Figure 1-353. VPDMA_int2_channel0_int_stat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-265. VPDMA_int2_channel0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_GRPX3	W	0h	The last read DMA transaction has occurred for channel grpx3 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_GRPX2	W	0h	The last read DMA transaction has occurred for channel grpx2 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_GRPX1	W	0h	The last read DMA transaction has occurred for channel grpx1 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_SCALER_OUT	W	0h	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27-20	Reserved	R	0h	
19	INT_STAT_SCALER_CHROMA	W	0h	The last write DMA transaction has completed for channel scaler_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-265. VPDMA_int2_channel0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	INT_STAT_SCALER_LUMA	W	0h	The last write DMA transaction has completed for channel scaler_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_HQ_SCALER	W	0h	The last write DMA transaction has completed for channel hq_scaler. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	Reserved	R	0h	
15	INT_STAT_HQ_MV_OUT	W	0h	The last write DMA transaction has completed for channel hq_mv_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_hq_mv_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14-13	Reserved	R	0h	
12	INT_STAT_HQ_MV	W	0h	The last read DMA transaction has occurred for channel hq_mv and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_hq_mv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11-6	Reserved	R	0h	
5	INT_STAT_HQ_VID3_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid3_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_3_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_HQ_VID3_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid3_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_3_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_HQ_VID2_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid2_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_2_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_HQ_VID2_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid2_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_2_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

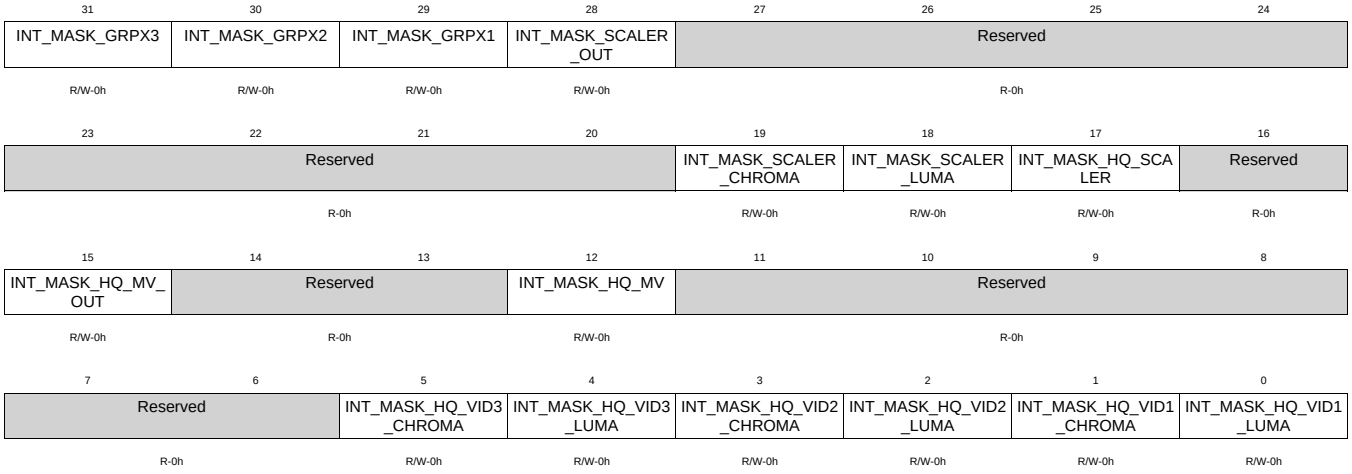
Table 1-265. VPDMA_int2_channel0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_STAT_HQ_VID1_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid1_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_1_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_HQ_VID1_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid1_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_1_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.54 VPDMA_int2_channel0_int_mask Register (offset = E4h) [reset = 0h]

VPDMA_int2_channel0_int_mask is shown in Figure 1-354 and described in Table 1-266.

Figure 1-354. VPDMA_int2_channel0_int_mask Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-266. VPDMA_int2_channel0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_GRPX3	R/W	0h	The interrupt for Graphcis 2 Data should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_GRPX2	R/W	0h	The interrupt for Graphics 1 Data should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_GRPX1	R/W	0h	The interrupt for Graphics 0 Data should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_SCALER_OUT	R/W	0h	The interrupt for Low Cost DEI Scalar Write to Memory should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
27-20	Reserved	R	0h	
19	INT_MASK_SCALER_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_SCALER_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_HQ_SCALER	R/W	0h	The interrupt for High Quality DEI Scaler Write to Memory should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	Reserved	R	0h	
15	INT_MASK_HQ_MV_OUT	R/W	0h	The interrupt for Low Cost DEI Motion Vector Write should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14-13	Reserved	R	0h	
12	INT_MASK_HQ_MV	R/W	0h	The interrupt for Low Cost DEI Motion Vector should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11-6	Reserved	R	0h	

Table 1-266. VPDMA_int2_channel0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_MASK_HQ_VID3_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_HQ_VID3_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_HQ_VID2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_HQ_VID2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_HQ_VID1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_HQ_VID1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.55 VPDMA_int2_channel1_int_stat Register (offset = E8h) [reset = 0h]

VPDMA_int2_channel1_int_stat is shown in Figure 1-355 and described in Table 1-267.

Figure 1-355. VPDMA_int2_channel1_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP1_MULT_PORTB_SRC9	INT_STAT_VIP1_MULT_PORTB_SRC8	INT_STAT_VIP1_MULT_PORTB_SRC7	INT_STAT_VIP1_MULT_PORTB_SRC6	INT_STAT_VIP1_MULT_PORTB_SRC5	INT_STAT_VIP1_MULT_PORTB_SRC4	INT_STAT_VIP1_MULT_PORTB_SRC3	INT_STAT_VIP1_MULT_PORTB_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP1_MULT_PORTB_SRC1	INT_STAT_VIP1_MULT_PORTB_SRC0	INT_STAT_VIP1_MULT_PORTA_SRC15	INT_STAT_VIP1_MULT_PORTA_SRC14	INT_STAT_VIP1_MULT_PORTA_SRC13	INT_STAT_VIP1_MULT_PORTA_SRC12	INT_STAT_VIP1_MULT_PORTA_SRC11	INT_STAT_VIP1_MULT_PORTA_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP1_MULT_PORTA_SRC9	INT_STAT_VIP1_MULT_PORTA_SRC8	INT_STAT_VIP1_MULT_PORTA_SRC7	INT_STAT_VIP1_MULT_PORTA_SRC6	INT_STAT_VIP1_MULT_PORTA_SRC5	INT_STAT_VIP1_MULT_PORTA_SRC4	INT_STAT_VIP1_MULT_PORTA_SRC3	INT_STAT_VIP1_MULT_PORTA_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_PORTA_SRC1	INT_STAT_VIP1_MULT_PORTA_SRC0	INT_STAT_GRPX3_CLUT	INT_STAT_GRPX2_CLUT	INT_STAT_GRPX1_CLUT	INT_STAT_GRPX3_STENCIL	INT_STAT_GRPX2_STENCIL	INT_STAT_GRPX1_STENCIL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-267. VPDMA_int2_channel1_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP1_MULT_PORTB_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP1_MULT_PORTB_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP1_MULT_PORTB_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP1_MULT_PORTB_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_MULT_PORTB_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_MULT_PORTB_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-267. VPDMA_int2_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP1_MULT_PORTB_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP1_MULT_PORTB_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP1_MULT_PORTB_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP1_MULT_PORTB_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP1_MULT_PORTA_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP1_MULT_PORTA_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP1_MULT_PORTA_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP1_MULT_PORTA_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP1_MULT_PORTA_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP1_MULT_PORTA_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-267. VPDMA_int2_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP1_MULT_PORTA_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP1_MULT_PORTA_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP1_MULT_PORTA_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP1_MULT_PORTA_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_MULT_PORTA_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_MULT_PORTA_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_MULT_PORTA_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_MULT_PORTA_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_MULT_PORTA_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_MULT_PORTA_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-267. VPDMA_int2_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_GRPX3_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx3_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_GRPX2_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx2_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_GRPX1_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx1_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_GRPX3_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx3_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_GRPX2_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx2_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_GRPX1_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx1_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.56 VPDMA_int2_channel1_int_mask Register (offset = ECh) [reset = 0h]

VPDMA_int2_channel1_int_mask is shown in Figure 1-356 and described in Table 1-268.

Figure 1-356. VPDMA_int2_channel1_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP1_MULT_PORTB_SRC9	INT_MASK_VIP1_MULT_PORTB_SRC8	INT_MASK_VIP1_MULT_PORTB_SRC7	INT_MASK_VIP1_MULT_PORTB_SRC6	INT_MASK_VIP1_MULT_PORTB_SRC5	INT_MASK_VIP1_MULT_PORTB_SRC4	INT_MASK_VIP1_MULT_PORTB_SRC3	INT_MASK_VIP1_MULT_PORTB_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP1_MULT_PORTB_SRC1	INT_MASK_VIP1_MULT_PORTB_SRC0	INT_MASK_VIP1_MULT_PORTA_SRC15	INT_MASK_VIP1_MULT_PORTA_SRC14	INT_MASK_VIP1_MULT_PORTA_SRC13	INT_MASK_VIP1_MULT_PORTA_SRC12	INT_MASK_VIP1_MULT_PORTA_SRC11	INT_MASK_VIP1_MULT_PORTA_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP1_MULT_PORTA_SRC9	INT_MASK_VIP1_MULT_PORTA_SRC8	INT_MASK_VIP1_MULT_PORTA_SRC7	INT_MASK_VIP1_MULT_PORTA_SRC6	INT_MASK_VIP1_MULT_PORTA_SRC5	INT_MASK_VIP1_MULT_PORTA_SRC4	INT_MASK_VIP1_MULT_PORTA_SRC3	INT_MASK_VIP1_MULT_PORTA_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_PORTA_SRC1	INT_MASK_VIP1_MULT_PORTA_SRC0	INT_MASK_GRPX3_CLUT	INT_MASK_GRPX2_CLUT	INT_MASK_GRPX1_CLUT	INT_MASK_GRPX3_STENCIL	INT_MASK_GRPX2_STENCIL	INT_MASK_GRPX1_STENCIL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-268. VPDMA_int2_channel1_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP1_MULT_PORTB_SRC9	R/W	0h	The interrupt for Video Input 1 Port B Channel 9 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP1_MULT_PORTB_SRC8	R/W	0h	The interrupt for Video Input 1 Port B Channel 8 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP1_MULT_PORTB_SRC7	R/W	0h	The interrupt for Video Input 1 Port B Channel 7 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP1_MULT_PORTB_SRC6	R/W	0h	The interrupt for Video Input 1 Port B Channel 6 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_MULT_PORTB_SRC5	R/W	0h	The interrupt for Video Input 1 Port B Channel 5 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_MULT_PORTB_SRC4	R/W	0h	The interrupt for Video Input 1 Port B Channel 4 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP1_MULT_PORTB_SRC3	R/W	0h	The interrupt for Video Input 1 Port B Channel 3 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP1_MULT_PORTB_SRC2	R/W	0h	The interrupt for Video Input 1 Port B Channel 2 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP1_MULT_PORTB_SRC1	R/W	0h	The interrupt for Video Input 1 Port B Channel 1 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP1_MULT_PORTB_SRC0	R/W	0h	The interrupt for Video Input 1 Port B Channel 0 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP1_MULT_PORTA_SRC15	R/W	0h	The interrupt for Video Input 1 Port A Channel 15 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-268. VPDMA_int2_channel1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP1_MULT_PORTA_SRC14	R/W	0h	The interrupt for Video Input 1 Port A Channel 14 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP1_MULT_PORTA_SRC13	R/W	0h	The interrupt for Video Input 1 Port A Channel 13 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP1_MULT_PORTA_SRC12	R/W	0h	The interrupt for Video Input 1 Port A Channel 12 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP1_MULT_PORTA_SRC11	R/W	0h	The interrupt for Video Input 1 Port A Channel 11 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP1_MULT_PORTA_SRC10	R/W	0h	The interrupt for Video Input 1 Port A Channel 10 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP1_MULT_PORTA_SRC9	R/W	0h	The interrupt for Video Input 1 Port A Channel 9 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP1_MULT_PORTA_SRC8	R/W	0h	The interrupt for Video Input 1 Port A Channel 8 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP1_MULT_PORTA_SRC7	R/W	0h	The interrupt for Video Input 1 Port A Channel 7 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP1_MULT_PORTA_SRC6	R/W	0h	The interrupt for Video Input 1 Port A Channel 6 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_MULT_PORTA_SRC5	R/W	0h	The interrupt for Video Input 1 Port A Channel 5 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_MULT_PORTA_SRC4	R/W	0h	The interrupt for Video Input 1 Port A Channel 4 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_MULT_PORTA_SRC3	R/W	0h	The interrupt for Video Input 1 Port A Channel 3 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_MULT_PORTA_SRC2	R/W	0h	The interrupt for Video Input 1 Port A Channel 2 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_MULT_PORTA_SRC1	R/W	0h	The interrupt for Video Input 1 Port A Channel 1 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_MULT_PORTA_SRC0	R/W	0h	The interrupt for Video Input 1 Port A Channel 0 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_GRPX3_CLUT	R/W	0h	The interrupt for Graphics 2 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_GRPX2_CLUT	R/W	0h	The interrupt for Graphics 1 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_GRPX1_CLUT	R/W	0h	The interrupt for Graphics 0 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-268. VPDMA_int2_channel1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_GRPX3_STENCIL	R/W	0h	The interrupt for Graphics 2 Stencil should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_GRPX2_STENCIL	R/W	0h	The interrupt for Graphics 1 Stencil should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_GRPX1_STENCIL	R/W	0h	The interrupt for Graphics 0 Stencil should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.57 VPDMA_int2_channel2_int_stat Register (offset = F0h) [reset = 0h]

VPDMA_int2_channel2_int_stat is shown in Figure 1-357 and described in Table 1-269.

Figure 1-357. VPDMA_int2_channel2_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP1_MULT_ANCB_SRC9	INT_STAT_VIP1_MULT_ANCB_SRC8	INT_STAT_VIP1_MULT_ANCB_SRC7	INT_STAT_VIP1_MULT_ANCB_SRC6	INT_STAT_VIP1_MULT_ANCB_SRC5	INT_STAT_VIP1_MULT_ANCB_SRC4	INT_STAT_VIP1_MULT_ANCB_SRC3	INT_STAT_VIP1_MULT_ANCB_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP1_MULT_ANCB_SRC1	INT_STAT_VIP1_MULT_ANCB_SRC0	INT_STAT_VIP1_MULT_ANCA_SRC15	INT_STAT_VIP1_MULT_ANCA_SRC14	INT_STAT_VIP1_MULT_ANCA_SRC13	INT_STAT_VIP1_MULT_ANCA_SRC12	INT_STAT_VIP1_MULT_ANCA_SRC11	INT_STAT_VIP1_MULT_ANCA_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP1_MULT_ANCA_SRC9	INT_STAT_VIP1_MULT_ANCA_SRC8	INT_STAT_VIP1_MULT_ANCA_SRC7	INT_STAT_VIP1_MULT_ANCA_SRC6	INT_STAT_VIP1_MULT_ANCA_SRC5	INT_STAT_VIP1_MULT_ANCA_SRC4	INT_STAT_VIP1_MULT_ANCA_SRC3	INT_STAT_VIP1_MULT_ANCA_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_ANCA_SRC1	INT_STAT_VIP1_MULT_ANCA_SRC0	INT_STAT_VIP1_MULT_PORTB_SRC15	INT_STAT_VIP1_MULT_PORTB_SRC14	INT_STAT_VIP1_MULT_PORTB_SRC13	INT_STAT_VIP1_MULT_PORTB_SRC12	INT_STAT_VIP1_MULT_PORTB_SRC11	INT_STAT_VIP1_MULT_PORTB_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-269. VPDMA_int2_channel2_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP1_MULT_ANCB_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP1_MULT_ANCB_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP1_MULT_ANCB_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP1_MULT_ANCB_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_MULT_ANCB_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_MULT_ANCB_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-269. VPDMA_int2_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP1_MULT_ANCB_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP1_MULT_ANCB_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP1_MULT_ANCB_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP1_MULT_ANCB_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP1_MULT_ANCA_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP1_MULT_ANCA_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP1_MULT_ANCA_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP1_MULT_ANCA_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP1_MULT_ANCA_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP1_MULT_ANCA_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-269. VPDMA_int2_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP1_MULT_ANCA_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP1_MULT_ANCA_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP1_MULT_ANCA_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP1_MULT_ANCA_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_MULT_ANCA_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_MULT_ANCA_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_MULT_ANCA_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_MULT_ANCA_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_MULT_ANCA_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_MULT_ANCA_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-269. VPDMA_int2_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_MULT_PORTB_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_MULT_PORTB_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_MULT_PORTB_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_MULT_PORTB_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP1_MULT_PORTB_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP1_MULT_PORTB_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.58 VPDMA_int2_channel2_int_mask Register (offset = F4h) [reset = 0h]

VPDMA_int2_channel2_int_mask is shown in Figure 1-358 and described in Table 1-270.

Figure 1-358. VPDMA_int2_channel2_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP1_MULT_ANCB_SRC9	INT_MASK_VIP1_MULT_ANCB_SRC8	INT_MASK_VIP1_MULT_ANCB_SRC7	INT_MASK_VIP1_MULT_ANCB_SRC6	INT_MASK_VIP1_MULT_ANCB_SRC5	INT_MASK_VIP1_MULT_ANCB_SRC4	INT_MASK_VIP1_MULT_ANCB_SRC3	INT_MASK_VIP1_MULT_ANCB_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP1_MULT_ANCB_SRC1	INT_MASK_VIP1_MULT_ANCB_SRC0	INT_MASK_VIP1_MULT_ANCA_SRC15	INT_MASK_VIP1_MULT_ANCA_SRC14	INT_MASK_VIP1_MULT_ANCA_SRC13	INT_MASK_VIP1_MULT_ANCA_SRC12	INT_MASK_VIP1_MULT_ANCA_SRC11	INT_MASK_VIP1_MULT_ANCA_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP1_MULT_ANCA_SRC9	INT_MASK_VIP1_MULT_ANCA_SRC8	INT_MASK_VIP1_MULT_ANCA_SRC7	INT_MASK_VIP1_MULT_ANCA_SRC6	INT_MASK_VIP1_MULT_ANCA_SRC5	INT_MASK_VIP1_MULT_ANCA_SRC4	INT_MASK_VIP1_MULT_ANCA_SRC3	INT_MASK_VIP1_MULT_ANCA_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_ANCA_SRC1	INT_MASK_VIP1_MULT_ANCA_SRC0	INT_MASK_VIP1_MULT_PORTB_SRC15	INT_MASK_VIP1_MULT_PORTB_SRC14	INT_MASK_VIP1_MULT_PORTB_SRC13	INT_MASK_VIP1_MULT_PORTB_SRC12	INT_MASK_VIP1_MULT_PORTB_SRC11	INT_MASK_VIP1_MULT_PORTB_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-270. VPDMA_int2_channel2_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP1_MULT_ANCB_SRC9	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP1_MULT_ANCB_SRC8	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP1_MULT_ANCB_SRC7	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP1_MULT_ANCB_SRC6	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_MULT_ANCB_SRC5	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_MULT_ANCB_SRC4	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP1_MULT_ANCB_SRC3	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP1_MULT_ANCB_SRC2	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP1_MULT_ANCB_SRC1	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP1_MULT_ANCB_SRC0	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP1_MULT_ANCA_SRC15	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-270. VPDMA_int2_channel2_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP1_MULT_ANCA_SRC14	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP1_MULT_ANCA_SRC13	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP1_MULT_ANCA_SRC12	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP1_MULT_ANCA_SRC11	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP1_MULT_ANCA_SRC10	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP1_MULT_ANCA_SRC9	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP1_MULT_ANCA_SRC8	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP1_MULT_ANCA_SRC7	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP1_MULT_ANCA_SRC6	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_MULT_ANCA_SRC5	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_MULT_ANCA_SRC4	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_MULT_ANCA_SRC3	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_MULT_ANCA_SRC2	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_MULT_ANCA_SRC1	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_MULT_ANCA_SRC0	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_MULT_PORTB_SRC15	R/W	0h	The interrupt for Video Input 1 Port B Channel 15 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_MULT_PORTB_SRC14	R/W	0h	The interrupt for Video Input 1 Port B Channel 14 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_MULT_PORTB_SRC13	R/W	0h	The interrupt for Video Input 1 Port B Channel 13 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-270. VPDMA_int2_channel2_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP1_MULT_PORTB_SRC12	R/W	0h	The interrupt for Video Input 1 Port B Channel 12 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP1_MULT_PORTB_SRC11	R/W	0h	The interrupt for Video Input 1 Port B Channel 11 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP1_MULT_PORTB_SRC10	R/W	0h	The interrupt for Video Input 1 Port B Channel 10 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.59 VPDMA_int2_channel3_int_stat Register (offset = F8h) [reset = 0h]

VPDMA_int2_channel3_int_stat is shown in Figure 1-359 and described in Table 1-271.

Figure 1-359. VPDMA_int2_channel3_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP2_MULT_PORTB_SRC3	INT_STAT_VIP2_MULT_PORTB_SRC2	INT_STAT_VIP2_MULT_PORTB_SRC1	INT_STAT_VIP2_MULT_PORTB_SRC0	INT_STAT_VIP2_MULT_PORTA_SRC15	INT_STAT_VIP2_MULT_PORTA_SRC14	INT_STAT_VIP2_MULT_PORTA_SRC13	INT_STAT_VIP2_MULT_PORTA_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP2_MULT_PORTA_SRC11	INT_STAT_VIP2_MULT_PORTA_SRC10	INT_STAT_VIP2_MULT_PORTA_SRC9	INT_STAT_VIP2_MULT_PORTA_SRC8	INT_STAT_VIP2_MULT_PORTA_SRC7	INT_STAT_VIP2_MULT_PORTA_SRC6	INT_STAT_VIP2_MULT_PORTA_SRC5	INT_STAT_VIP2_MULT_PORTA_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_MULT_PORTA_SRC3	INT_STAT_VIP2_MULT_PORTA_SRC2	INT_STAT_VIP2_MULT_PORTA_SRC1	INT_STAT_VIP2_MULT_PORTA_SRC0	INT_STAT_VIP1_PORTB_RGB	INT_STAT_VIP1_PORTA_RGB	INT_STAT_VIP1_PORTB_CHROMA	INT_STAT_VIP1_PORTB_LUMA
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_PORTA_CHROMA	INT_STAT_VIP1_PORTA_LUMA	INT_STAT_VIP1_MULT_ANCB_SRC15	INT_STAT_VIP1_MULT_ANCB_SRC14	INT_STAT_VIP1_MULT_ANCB_SRC13	INT_STAT_VIP1_MULT_ANCB_SRC12	INT_STAT_VIP1_MULT_ANCB_SRC11	INT_STAT_VIP1_MULT_ANCB_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-271. VPDMA_int2_channel3_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP2_MULT_PORTB_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP2_MULT_PORTB_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP2_MULT_PORTB_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_MULT_PORTB_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP2_MULT_PORTA_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP2_MULT_PORTA_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-271. VPDMA_int2_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP2_MULT_PORTA_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP2_MULT_PORTA_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP2_MULT_PORTA_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP2_MULT_PORTA_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP2_MULT_PORTA_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP2_MULT_PORTA_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP2_MULT_PORTA_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP2_MULT_PORTA_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_MULT_PORTA_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP2_MULT_PORTA_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-271. VPDMA_int2_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP2_MULT_PORTA_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_MULT_PORTA_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_MULT_PORTA_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_MULT_PORTA_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_PORTB_RGB	W	0h	The last write DMA transaction has completed for channel vip1_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_PORTA_RGB	W	0h	The last write DMA transaction has completed for channel vip1_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_PORTB_CHROMA	W	0h	The last write DMA transaction has completed for channel vip1_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_PORTB_LUMA	W	0h	The last write DMA transaction has completed for channel vip1_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_PORTA_CHROMA	W	0h	The last write DMA transaction has completed for channel vip1_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_PORTA_LUMA	W	0h	The last write DMA transaction has completed for channel vip1_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-271. VPDMA_int2_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_MULT_ANCB_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_MULT_ANCB_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_MULT_ANCB_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_MULT_ANCB_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP1_MULT_ANCB_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP1_MULT_ANCB_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.60 VPDMA_int2_channel3_int_mask Register (offset = FCh) [reset = 0h]

VPDMA_int2_channel3_int_mask is shown in Figure 1-360 and described in Table 1-272.

Figure 1-360. VPDMA_int2_channel3_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP2_MULT_PORTB_SRC3	INT_MASK_VIP2_MULT_PORTB_SRC2	INT_MASK_VIP2_MULT_PORTB_SRC1	INT_MASK_VIP2_MULT_PORTB_SRC0	INT_MASK_VIP2_MULT_PORTA_SRC15	INT_MASK_VIP2_MULT_PORTA_SRC14	INT_MASK_VIP2_MULT_PORTA_SRC13	INT_MASK_VIP2_MULT_PORTA_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP2_MULT_PORTA_SRC11	INT_MASK_VIP2_MULT_PORTA_SRC10	INT_MASK_VIP2_MULT_PORTA_SRC9	INT_MASK_VIP2_MULT_PORTA_SRC8	INT_MASK_VIP2_MULT_PORTA_SRC7	INT_MASK_VIP2_MULT_PORTA_SRC6	INT_MASK_VIP2_MULT_PORTA_SRC5	INT_MASK_VIP2_MULT_PORTA_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_MULT_PORTA_SRC3	INT_MASK_VIP2_MULT_PORTA_SRC2	INT_MASK_VIP2_MULT_PORTA_SRC1	INT_MASK_VIP2_MULT_PORTA_SRC0	INT_MASK_VIP1_PORTB_RGB	INT_MASK_VIP1_PORTA_RGB	INT_MASK_VIP1_PORTB_CHROMA	INT_MASK_VIP1_PORTB_LUMA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_PORTA_CHROMA	INT_MASK_VIP1_PORTA_LUMA	INT_MASK_VIP1_MULT_ANCB_SRC15	INT_MASK_VIP1_MULT_ANCB_SRC14	INT_MASK_VIP1_MULT_ANCB_SRC13	INT_MASK_VIP1_MULT_ANCB_SRC12	INT_MASK_VIP1_MULT_ANCB_SRC11	INT_MASK_VIP1_MULT_ANCB_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-272. VPDMA_int2_channel3_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP2_MULT_PORTB_SRC3	R/W	0h	The interrupt for Video Input 2 Port B Channel 3 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP2_MULT_PORTB_SRC2	R/W	0h	The interrupt for Video Input 2 Port B Channel 2 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP2_MULT_PORTB_SRC1	R/W	0h	The interrupt for Video Input 2 Port B Channel 1 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_MULT_PORTB_SRC0	R/W	0h	The interrupt for Video Input 2 Port B Channel 0 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP2_MULT_PORTA_SRC15	R/W	0h	The interrupt for Video Input 2 Port A Channel 15 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP2_MULT_PORTA_SRC14	R/W	0h	The interrupt for Video Input 2 Port A Channel 14 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP2_MULT_PORTA_SRC13	R/W	0h	The interrupt for Video Input 2 Port A Channel 13 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP2_MULT_PORTA_SRC12	R/W	0h	The interrupt for Video Input 2 Port A Channel 12 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP2_MULT_PORTA_SRC11	R/W	0h	The interrupt for Video Input 2 Port A Channel 11 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP2_MULT_PORTA_SRC10	R/W	0h	The interrupt for Video Input 2 Port A Channel 10 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP2_MULT_PORTA_SRC9	R/W	0h	The interrupt for Video Input 2 Port A Channel 9 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-272. VPDMA_int2_channel3_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP2_MULT_PORTA_SRC8	R/W	0h	The interrupt for Video Input 2 Port A Channel 8 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP2_MULT_PORTA_SRC7	R/W	0h	The interrupt for Video Input 2 Port A Channel 7 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP2_MULT_PORTA_SRC6	R/W	0h	The interrupt for Video Input 2 Port A Channel 6 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_MULT_PORTA_SRC5	R/W	0h	The interrupt for Video Input 2 Port A Channel 5 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_MULT_PORTA_SRC4	R/W	0h	The interrupt for Video Input 2 Port A Channel 4 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_MULT_PORTA_SRC3	R/W	0h	The interrupt for Video Input 2 Port A Channel 3 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_MULT_PORTA_SRC2	R/W	0h	The interrupt for Video Input 2 Port A Channel 2 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_MULT_PORTA_SRC1	R/W	0h	The interrupt for Video Input 2 Port A Channel 1 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_MULT_PORTA_SRC0	R/W	0h	The interrupt for Video Input 2 Port A Channel 0 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_PORTB_RGB	R/W	0h	The interrupt for Video Input 1 Port B RGB Data should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_PORTA_RGB	R/W	0h	The interrupt for Video Input 1 Port A RGB Data should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_PORTB_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_PORTB_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_PORTA_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_PORTA_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_MULT_ANCB_SRC15	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_MULT_ANCB_SRC14	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_MULT_ANCB_SRC13	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-272. VPDMA_int2_channel3_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP1_MULT_ANCB_SRC12	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP1_MULT_ANCB_SRC11	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP1_MULT_ANCB_SRC10	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.61 VPDMA_int2_channel4_int_stat Register (offset = 100h) [reset = 0h]

VPDMA_int2_channel4_int_stat is shown in Figure 1-361 and described in Table 1-273.

Figure 1-361. VPDMA_int2_channel4_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP2_MULT_ANCB_SRC3	INT_STAT_VIP2_MULT_ANCB_SRC2	INT_STAT_VIP2_MULT_ANCB_SRC1	INT_STAT_VIP2_MULT_ANCB_SRC0	INT_STAT_VIP2_MULT_ANCA_SRC15	INT_STAT_VIP2_MULT_ANCA_SRC14	INT_STAT_VIP2_MULT_ANCA_SRC13	INT_STAT_VIP2_MULT_ANCA_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP2_MULT_ANCA_SRC11	INT_STAT_VIP2_MULT_ANCA_SRC10	INT_STAT_VIP2_MULT_ANCA_SRC9	INT_STAT_VIP2_MULT_ANCA_SRC8	INT_STAT_VIP2_MULT_ANCA_SRC7	INT_STAT_VIP2_MULT_ANCA_SRC6	INT_STAT_VIP2_MULT_ANCA_SRC5	INT_STAT_VIP2_MULT_ANCA_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_MULT_ANCA_SRC3	INT_STAT_VIP2_MULT_ANCA_SRC2	INT_STAT_VIP2_MULT_ANCA_SRC1	INT_STAT_VIP2_MULT_ANCA_SRC0	INT_STAT_VIP2_MULT_PORTB_SRC15	INT_STAT_VIP2_MULT_PORTB_SRC14	INT_STAT_VIP2_MULT_PORTB_SRC13	INT_STAT_VIP2_MULT_PORTB_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_PORTB_SRC11	INT_STAT_VIP2_MULT_PORTB_SRC10	INT_STAT_VIP2_MULT_PORTB_SRC9	INT_STAT_VIP2_MULT_PORTB_SRC8	INT_STAT_VIP2_MULT_PORTB_SRC7	INT_STAT_VIP2_MULT_PORTB_SRC6	INT_STAT_VIP2_MULT_PORTB_SRC5	INT_STAT_VIP2_MULT_PORTB_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-273. VPDMA_int2_channel4_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP2_MULT_ANCB_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP2_MULT_ANCB_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP2_MULT_ANCB_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_MULT_ANCB_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP2_MULT_ANCA_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP2_MULT_ANCA_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-273. VPDMA_int2_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP2_MULT_ANCA_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP2_MULT_ANCA_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP2_MULT_ANCA_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP2_MULT_ANCA_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP2_MULT_ANCA_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP2_MULT_ANCA_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP2_MULT_ANCA_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP2_MULT_ANCA_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_MULT_ANCA_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP2_MULT_ANCA_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-273. VPDMA_int2_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP2_MULT_ANCA_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_MULT_ANCA_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_MULT_ANCA_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_MULT_ANCA_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP2_MULT_PORTB_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP2_MULT_PORTB_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_MULT_PORTB_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_MULT_PORTB_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_MULT_PORTB_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP2_MULT_PORTB_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-273. VPDMA_int2_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP2_MULT_PORTB_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP2_MULT_PORTB_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP2_MULT_PORTB_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP2_MULT_PORTB_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP2_MULT_PORTB_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP2_MULT_PORTB_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.62 VPDMA_int2_channel4_int_mask Register (offset = 104h) [reset = 0h]

VPDMA_int2_channel4_int_mask is shown in Figure 1-362 and described in Table 1-274.

Figure 1-362. VPDMA_int2_channel4_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP2_MULT_ANCB_SRC3	INT_MASK_VIP2_MULT_ANCB_SRC2	INT_MASK_VIP2_MULT_ANCB_SRC1	INT_MASK_VIP2_MULT_ANCB_SRC0	INT_MASK_VIP2_MULT_ANCA_SRC15	INT_MASK_VIP2_MULT_ANCA_SRC14	INT_MASK_VIP2_MULT_ANCA_SRC13	INT_MASK_VIP2_MULT_ANCA_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP2_MULT_ANCA_SRC11	INT_MASK_VIP2_MULT_ANCA_SRC10	INT_MASK_VIP2_MULT_ANCA_SRC9	INT_MASK_VIP2_MULT_ANCA_SRC8	INT_MASK_VIP2_MULT_ANCA_SRC7	INT_MASK_VIP2_MULT_ANCA_SRC6	INT_MASK_VIP2_MULT_ANCA_SRC5	INT_MASK_VIP2_MULT_ANCA_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_MULT_ANCA_SRC3	INT_MASK_VIP2_MULT_ANCA_SRC2	INT_MASK_VIP2_MULT_ANCA_SRC1	INT_MASK_VIP2_MULT_ANCA_SRC0	INT_MASK_VIP2_MULT_PORTB_SRC15	INT_MASK_VIP2_MULT_PORTB_SRC14	INT_MASK_VIP2_MULT_PORTB_SRC13	INT_MASK_VIP2_MULT_PORTB_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_PORTB_SRC11	INT_MASK_VIP2_MULT_PORTB_SRC10	INT_MASK_VIP2_MULT_PORTB_SRC9	INT_MASK_VIP2_MULT_PORTB_SRC8	INT_MASK_VIP2_MULT_PORTB_SRC7	INT_MASK_VIP2_MULT_PORTB_SRC6	INT_MASK_VIP2_MULT_PORTB_SRC5	INT_MASK_VIP2_MULT_PORTB_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-274. VPDMA_int2_channel4_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP2_MULT_ANCB_SRC3	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP2_MULT_ANCB_SRC2	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP2_MULT_ANCB_SRC1	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_MULT_ANCB_SRC0	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP2_MULT_ANCA_SRC15	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP2_MULT_ANCA_SRC14	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP2_MULT_ANCA_SRC13	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP2_MULT_ANCA_SRC12	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP2_MULT_ANCA_SRC11	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP2_MULT_ANCA_SRC10	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP2_MULT_ANCA_SRC9	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-274. VPDMA_int2_channel4_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP2_MULT_ANCA_SRC8	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP2_MULT_ANCA_SRC7	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP2_MULT_ANCA_SRC6	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_MULT_ANCA_SRC5	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_MULT_ANCA_SRC4	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_MULT_ANCA_SRC3	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_MULT_ANCA_SRC2	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_MULT_ANCA_SRC1	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_MULT_ANCA_SRC0	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP2_MULT_PORTB_SRC15	R/W	0h	The interrupt for Video Input 2 Port B Channel 15 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP2_MULT_PORTB_SRC14	R/W	0h	The interrupt for Video Input 2 Port B Channel 14 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_MULT_PORTB_SRC13	R/W	0h	The interrupt for Video Input 2 Port B Channel 13 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_MULT_PORTB_SRC12	R/W	0h	The interrupt for Video Input 2 Port B Channel 12 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_MULT_PORTB_SRC11	R/W	0h	The interrupt for Video Input 2 Port B Channel 11 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_MULT_PORTB_SRC10	R/W	0h	The interrupt for Video Input 2 Port B Channel 10 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP2_MULT_PORTB_SRC9	R/W	0h	The interrupt for Video Input 2 Port B Channel 9 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP2_MULT_PORTB_SRC8	R/W	0h	The interrupt for Video Input 2 Port B Channel 8 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP2_MULT_PORTB_SRC7	R/W	0h	The interrupt for Video Input 2 Port B Channel 7 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-274. VPDMA_int2_channel4_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP2_MULT_PORTB_SRC6	R/W	0h	The interrupt for Video Input 2 Port B Channel 6 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP2_MULT_PORTB_SRC5	R/W	0h	The interrupt for Video Input 2 Port B Channel 5 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP2_MULT_PORTB_SRC4	R/W	0h	The interrupt for Video Input 2 Port B Channel 4 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.63 VPDMA_int2_channel5_int_stat Register (offset = 108h) [reset = 0h]

VPDMA_int2_channel5_int_stat is shown in Figure 1-363 and described in Table 1-275.

Figure 1-363. VPDMA_int2_channel5_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_TRANSCODE2_CHROMA	INT_STAT_TRANSCODE2_LUMA	INT_STAT_TRANSCODE1_CHROMA	INT_STAT_TRANSCODE1_LUMA	INT_STAT_AUX_IN	INT_STAT_PIP_FRAME	INT_STAT_POST_COMP_WR	INT_STAT_VBI_SD_VENC
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
Reserved	INT_STAT_NF_LAST_CHROMA	INT_STAT_NF_LAST_LUMA	INT_STAT_NF_WRITE_CHROMA	INT_STAT_NF_WRITE_LUMA	INT_STAT_NF_READ	INT_STAT_VIP2_PORTB_RGB	INT_STAT_VIP2_PORTA_RGB
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_PORTB_CHROMA	INT_STAT_VIP2_PORTB_LUMA	INT_STAT_VIP2_PORTA_CHROMA	INT_STAT_VIP2_PORTA_LUMA	INT_STAT_VIP2_MULT_ANCB_SRC15	INT_STAT_VIP2_MULT_ANCB_SRC14	INT_STAT_VIP2_MULT_ANCB_SRC13	INT_STAT_VIP2_MULT_ANCB_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_ANCB_SRC11	INT_STAT_VIP2_MULT_ANCB_SRC10	INT_STAT_VIP2_MULT_ANCB_SRC9	INT_STAT_VIP2_MULT_ANCB_SRC8	INT_STAT_VIP2_MULT_ANCB_SRC7	INT_STAT_VIP2_MULT_ANCB_SRC6	INT_STAT_VIP2_MULT_ANCB_SRC5	INT_STAT_VIP2_MULT_ANCB_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-275. VPDMA_int2_channel5_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_TRANSCODE2_CHROMA	W	0h	The last read DMA transaction has occurred for channel transcode2_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans2_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_TRANSCODE2_LUMA	W	0h	The last read DMA transaction has occurred for channel transcode2_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans2_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_TRANSCODE1_CHROMA	W	0h	The last read DMA transaction has occurred for channel transcode1_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans1_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_TRANSCODE1_LUMA	W	0h	The last read DMA transaction has occurred for channel transcode1_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans1_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_AUX_IN	W	0h	The last read DMA transaction has occurred for channel aux_in and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client comp_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-275. VPDMA_int2_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	INT_STAT_PIP_FRAME	W	0h	The last read DMA transaction has occurred for channel pip_frame and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client pip_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_POST_COMP_WR	W	0h	The last write DMA transaction has completed for channel post_comp_wr. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client hdmi_wrbk_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VBI_SD_VENC	W	0h	The last read DMA transaction has occurred for channel vbi_sd_venc and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client vbi_sdvenc will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	Reserved	R	0h	
22	INT_STAT_NF_LAST_CHROMA	W	0h	The last read DMA transaction has occurred for channel nf_last_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_420_uv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_NF_LAST_LUMA	W	0h	The last read DMA transaction has occurred for channel nf_last_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_420_y_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_NF_WRITE_CHROMA	W	0h	The last write DMA transaction has completed for channel nf_write_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_NF_WRITE_LUMA	W	0h	The last write DMA transaction has completed for channel nf_write_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_NF_READ	W	0h	The last read DMA transaction has occurred for channel nf_read and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_422_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_PORTB_RGB	W	0h	The last write DMA transaction has completed for channel vip2_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-275. VPDMA_int2_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	INT_STAT_VIP2_PORTA_RGB	W	0h	The last write DMA transaction has completed for channel vip2_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_VIP2_PORTB_CHROMA	W	0h	The last write DMA transaction has completed for channel vip2_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_PORTB_LUMA	W	0h	The last write DMA transaction has completed for channel vip2_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_PORTA_CHROMA	W	0h	The last write DMA transaction has completed for channel vip2_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_PORTA_LUMA	W	0h	The last write DMA transaction has completed for channel vip2_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP2_MULT_ANCB_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP2_MULT_ANCB_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_MULT_ANCB_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_MULT_ANCB_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_MULT_ANCB_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-275. VPDMA_int2_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT_STAT_VIP2_MULT_ANCB_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
5	INT_STAT_VIP2_MULT_ANCB_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP2_MULT_ANCB_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP2_MULT_ANCB_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP2_MULT_ANCB_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP2_MULT_ANCB_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP2_MULT_ANCB_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.64 VPDMA_int2_channel5_int_mask Register (offset = 10Ch) [reset = 0h]

VPDMA_int2_channel5_int_mask is shown in Figure 1-364 and described in Table 1-276.

Figure 1-364. VPDMA_int2_channel5_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_TRANSCODE2_CHROMA	INT_MASK_TRANSCODE2_LUMA	INT_MASK_TRANSCODE1_CHROMA	INT_MASK_TRANSCODE1_LUMA	INT_MASK_AUX_IN	INT_MASK_PIP_FRAME	INT_MASK_POST_COMP_WR	INT_MASK_VBI_SD_VENC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
Reserved	INT_MASK_NF_LAST_CHROMA	INT_MASK_NF_LAST_LUMA	INT_MASK_NF_WRITE_CHROMA	INT_MASK_NF_WRITE_LUMA	INT_MASK_NF_READ	INT_MASK_VIP2_PORTB_RGB	INT_MASK_VIP2_PORTA_RGB
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_PORTB_CHROMA	INT_MASK_VIP2_PORTB_LUMA	INT_MASK_VIP2_PORTA_CHROMA	INT_MASK_VIP2_PORTA_LUMA	INT_MASK_VIP2_MULT_ANCB_SRC15	INT_MASK_VIP2_MULT_ANCB_SRC14	INT_MASK_VIP2_MULT_ANCB_SRC13	INT_MASK_VIP2_MULT_ANCB_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_ANCB_SRC11	INT_MASK_VIP2_MULT_ANCB_SRC10	INT_MASK_VIP2_MULT_ANCB_SRC9	INT_MASK_VIP2_MULT_ANCB_SRC8	INT_MASK_VIP2_MULT_ANCB_SRC7	INT_MASK_VIP2_MULT_ANCB_SRC6	INT_MASK_VIP2_MULT_ANCB_SRC5	INT_MASK_VIP2_MULT_ANCB_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-276. VPDMA_int2_channel5_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_TRANSCODE2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_TRANSCODE2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_TRANSCODE1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_TRANSCODE1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_AUX_IN	R/W	0h	The interrupt for Auxilary Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_PIP_FRAME	R/W	0h	The interrupt for PIP Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_POST_COMP_WR	R/W	0h	The interrupt for Post Compositer Writeback to Memory should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VBI_SD_VENC	R/W	0h	The interrupt for SD Video Encoder VBI Data should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
23	Reserved	R	0h	
22	INT_MASK_NF_LAST_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_NF_LAST_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-276. VPDMA_int2_channel5_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_NF_WRITE_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_NF_WRITE_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_NF_READ	R/W	0h	The interrupt for Noise Filter Input Data 422 Interleaved should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_PORTB_RGB	R/W	0h	The interrupt for Video Input 2 Port B RGB Data should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_PORTA_RGB	R/W	0h	The interrupt for Video Input 2 Port A RGB Data should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_PORTB_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_PORTB_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_PORTA_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_PORTA_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP2_MULT_ANCB_SRC15	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP2_MULT_ANCB_SRC14	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_MULT_ANCB_SRC13	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_MULT_ANCB_SRC12	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_MULT_ANCB_SRC11	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_MULT_ANCB_SRC10	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP2_MULT_ANCB_SRC9	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP2_MULT_ANCB_SRC8	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP2_MULT_ANCB_SRC7	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

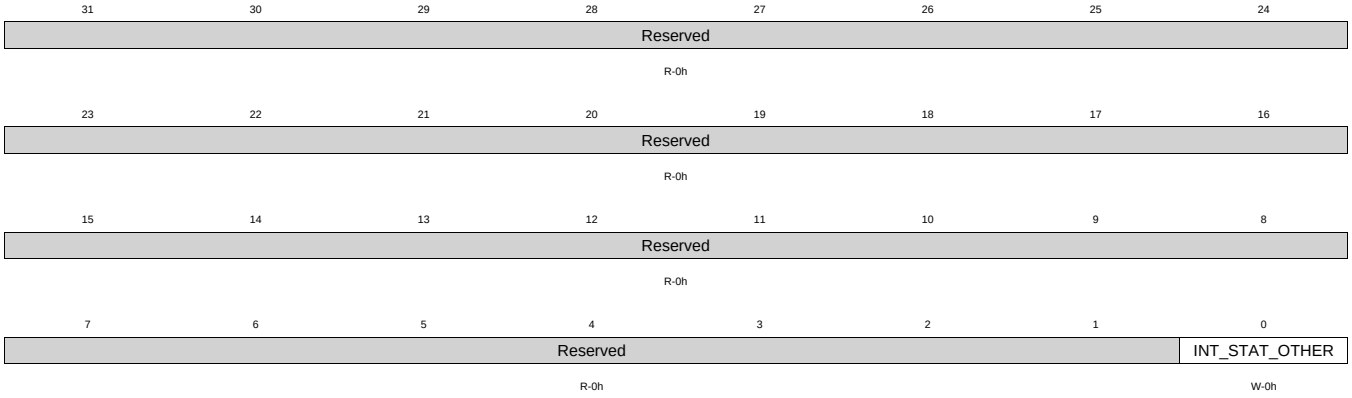
Table 1-276. VPDMA_int2_channel5_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP2_MULT_ANCB_SRC6	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP2_MULT_ANCB_SRC5	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP2_MULT_ANCB_SRC4	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.65 VPDMA_int2_channel6_int_stat Register (offset = 110h) [reset = 0h]

VPDMA_int2_channel6_int_stat is shown in Figure 1-365 and described in Table 1-277.

Figure 1-365. VPDMA_int2_channel6_int_stat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

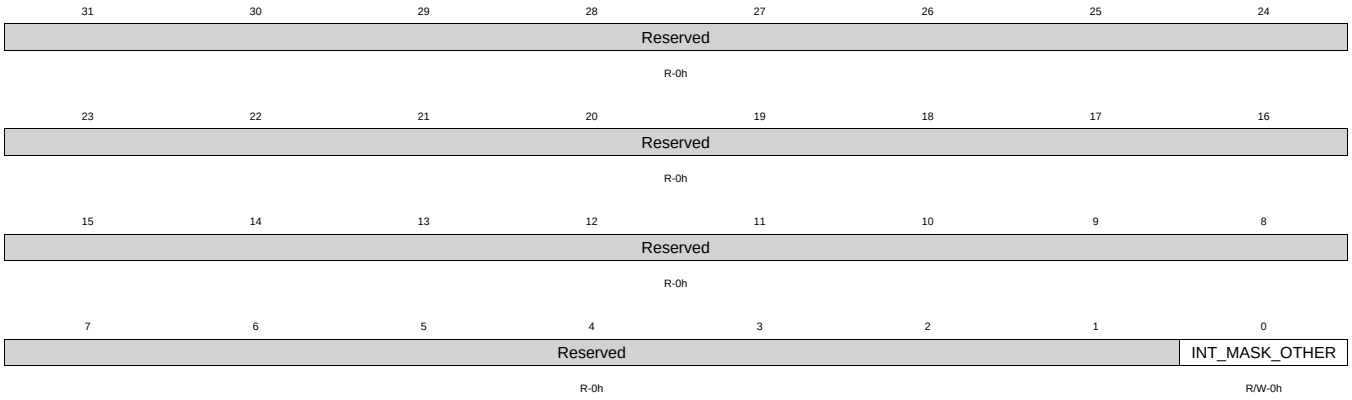
Table 1-277. VPDMA_int2_channel6_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	Reserved	R	0h	
0	INT_STAT_OTHER	W	0h	This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.66 VPDMA_int2_channel6_int_mask Register (offset = 114h) [reset = 0h]

VPDMA_int2_channel6_int_mask is shown in Figure 1-366 and described in Table 1-278.

Figure 1-366. VPDMA_int2_channel6_int_mask Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-278. VPDMA_int2_channel6_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	Reserved	R	0h	
0	INT_MASK_OTHER	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.67 VPDMA_int2_client0_int_stat Register (offset = 118h) [reset = 0h]

VPDMA_int2_client0_int_stat is shown in Figure 1-367 and described in Table 1-279.

Figure 1-367. VPDMA_int2_client0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_GRPX1_DATA	INT_STAT_COMP_WRBK	INT_STAT_SC_OUT	Reserved				
W-0h	W-0h	W-0h	R-0h				
23	22	21	20	19	18	17	16
Reserved			INT_STAT_SC_IN_LUMA	INT_STAT_SC_IN_CHROMA	INT_STAT_PIP_WRBK	INT_STAT_DEI_SC_OUT	Reserved
R-0h			W-0h	W-0h	W-0h	W-0h	R-0h
15	14	13	12	11	10	9	8
INT_STAT_DEI_HQ_MV_OUT	Reserved		INT_STAT_DEI_HQ_MV_IN	Reserved			
W-0h	R-0h		W-0h	R-0h			
7	6	5	4	3	2	1	0
Reserved		INT_STAT_DEI_HQ_3_CHROMA	INT_STAT_DEI_HQ_3_LUMA	INT_STAT_DEI_HQ_2_CHROMA	INT_STAT_DEI_HQ_2_LUMA	INT_STAT_DEI_HQ_1_LUMA	INT_STAT_DEI_HQ_1_CHROMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-279. VPDMA_int2_client0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_GRPX1_DATA	W	0h	The client interface grpx1_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_COMP_WRBK	W	0h	The client interface comp_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_SC_OUT	W	0h	The client interface sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28-21	Reserved	R	0h	
20	INT_STAT_SC_IN_LUMA	W	0h	The client interface sc_in_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_SC_IN_CHROMA	W	0h	The client interface sc_in_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-279. VPDMA_int2_client0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	INT_STAT_PIP_WRBK	W	0h	The client interface pip_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_DEI_SC_OUT	W	0h	The client interface dei_sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	Reserved	R	0h	
15	INT_STAT_DEI_HQ_MV_OUT	W	0h	The client interface dei_hq_mv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14-13	Reserved	R	0h	
12	INT_STAT_DEI_HQ_MV_IN	W	0h	The client interface dei_hq_mv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11-6	Reserved	R	0h	
5	INT_STAT_DEI_HQ_3_CHROMA	W	0h	The client interface dei_hq_3_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_DEI_HQ_3_LUMA	W	0h	The client interface dei_hq_3_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_DEI_HQ_2_CHROMA	W	0h	The client interface dei_hq_2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_DEI_HQ_2_LUMA	W	0h	The client interface dei_hq_2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

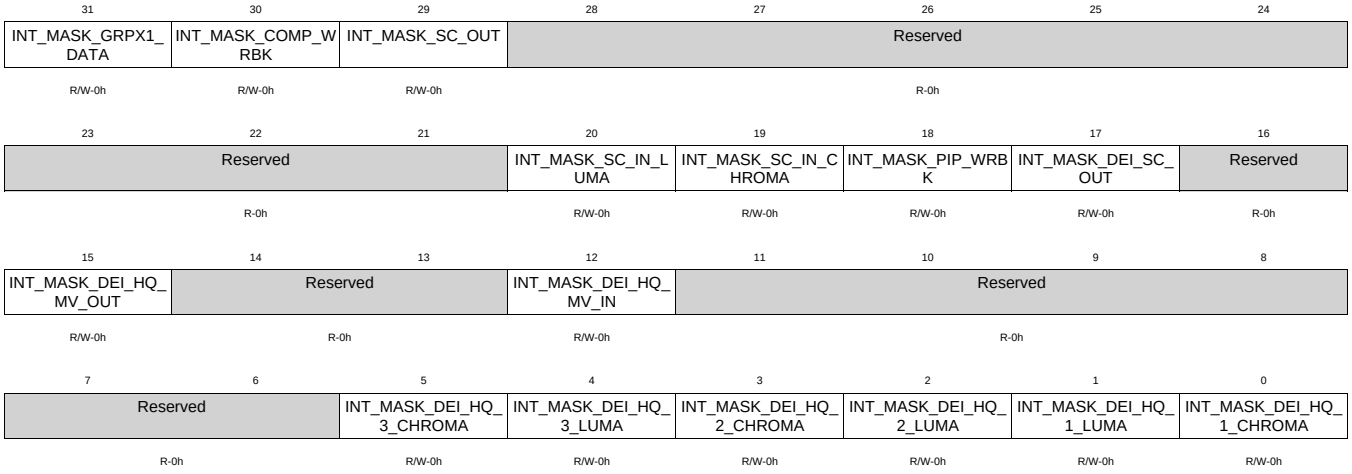
Table 1-279. VPDMA_int2_client0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_STAT_DEI_HQ_1_LUMA	W	0h	The client interface dei_hq_1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_DEI_HQ_1_CHROMA	W	0h	The client interface dei_hq_1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.68 VPDMA_int2_client0_int_mask Register (offset = 11Ch) [reset = 0h]

VPDMA_int2_client0_int_mask is shown in Figure 1-368 and described in Table 1-280.

Figure 1-368. VPDMA_int2_client0_int_mask Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-280. VPDMA_int2_client0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_GRPX1_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_COMP_WRBK	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_SC_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28-21	Reserved	R	0h	
20	INT_MASK_SC_IN_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_SC_IN_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_PIP_WRBK	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_DEI_SC_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	Reserved	R	0h	
15	INT_MASK_DEI_HQ_MV_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14-13	Reserved	R	0h	
12	INT_MASK_DEI_HQ_MV_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11-6	Reserved	R	0h	

Table 1-280. VPDMA_int2_client0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_MASK_DEI_HQ_3_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_DEI_HQ_3_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_DEI_HQ_2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_DEI_HQ_2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_DEI_HQ_1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_DEI_HQ_1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.69 VPDMA_int2_client1_int_stat Register (offset = 120h) [reset = 0h]

VPDMA_int2_client1_int_stat is shown in Figure 1-369 and described in Table 1-281.

Figure 1-369. VPDMA_int2_client1_int_stat Register

31	30	29	28	27	26	25	24
Reserved		INT_STAT_VIP2_ANC_B	INT_STAT_VIP2_ANC_A	INT_STAT_VIP1_ANC_B	INT_STAT_VIP1_ANC_A	INT_STAT_TRANS2_LUMA	INT_STAT_TRANS2_CHROMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_TRANS1_LUMA	INT_STAT_TRANS1_CHROMA	INT_STAT_HDMI_WRBK_OUT	INT_STAT_VPI_CTL	INT_STAT_VBI_SDVENC	Reserved	INT_STAT_NF_420_UV_OUT	INT_STAT_NF_420_Y_OUT
W-0h	W-0h	W-0h	W-0h	W-0h	R-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_NF_420_UV_IN	INT_STAT_NF_420_Y_IN	INT_STAT_NF_422_IN	INT_STAT_GRPX3_ST	INT_STAT_GRPX2_ST	INT_STAT_GRPX1_ST	INT_STAT_VIP2_UP_UV	INT_STAT_VIP2_UP_Y
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_LO_UV	INT_STAT_VIP2_LO_Y	INT_STAT_VIP1_UP_UV	INT_STAT_VIP1_UP_Y	INT_STAT_VIP1_LO_UV	INT_STAT_VIP1_LO_Y	INT_STAT_GRPX3_DATA	INT_STAT_GRPX2_DATA
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-281. VPDMA_int2_client1_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	INT_STAT_VIP2_ANC_B	W	0h	The client interface vip2_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_ANC_A	W	0h	The client interface vip2_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_ANC_B	W	0h	The client interface vip1_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_ANC_A	W	0h	The client interface vip1_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_TRANS2_LUMA	W	0h	The client interface trans2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-281. VPDMA_int2_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	INT_STAT_TRANS2_CHROMA	W	0h	The client interface trans2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_TRANS1_LUMA	W	0h	The client interface trans1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_TRANS1_CHROMA	W	0h	The client interface trans1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_HDMI_WRBK_OUT	W	0h	The client interface hdmi_wrbk_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VPI_CTL	W	0h	The client interface vpi_ctl has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VBI_SDVENC	W	0h	The client interface vbi_sdvenc has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	Reserved	R	0h	
17	INT_STAT_NF_420_UV_OUT	W	0h	The client interface nf_420_uv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_NF_420_Y_OUT	W	0h	The client interface nf_420_y_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_NF_420_UV_IN	W	0h	The client interface nf_420_uv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-281. VPDMA_int2_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	INT_STAT_NF_420_Y_IN	W	0h	The client interface nf_420_y_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_NF_422_IN	W	0h	The client interface nf_422_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_GRPX3_ST	W	0h	The client interface grpx3_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_GRPX2_ST	W	0h	The client interface grpx2_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_GRPX1_ST	W	0h	The client interface grpx1_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_UP_UV	W	0h	The client interface vip2_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_UP_Y	W	0h	The client interface vip2_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_LO_UV	W	0h	The client interface vip2_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP2_LO_Y	W	0h	The client interface vip2_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-281. VPDMA_int2_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_UP_UV	W	0h	The client interface vip1_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_UP_Y	W	0h	The client interface vip1_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_LO_UV	W	0h	The client interface vip1_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_LO_Y	W	0h	The client interface vip1_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_GRPX3_DATA	W	0h	The client interface grpx3_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_GRPX2_DATA	W	0h	The client interface grpx2_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.70 VPDMA_int2_client1_int_mask Register (offset = 124h) [reset = 0h]

VPDMA_int2_client1_int_mask is shown in Figure 1-370 and described in Table 1-282.

Figure 1-370. VPDMA_int2_client1_int_mask Register

31	30	29	28	27	26	25	24
Reserved		INT_MASK_VIP2_ANC_B	INT_MASK_VIP2_ANC_A	INT_MASK_VIP1_ANC_B	INT_MASK_VIP1_ANC_A	INT_MASK_TRANS2_LUMA	INT_MASK_TRANS2_CHROMA
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_TRANS1_LUMA	INT_MASK_TRANS1_CHROMA	INT_MASK_HDMI_WRBK_OUT	INT_MASK_VPI_CTL	INT_MASK_VBI_SDVENC	Reserved	INT_MASK_NF_420_UV_OUT	INT_MASK_NF_420_Y_OUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_NF_420_UV_IN	INT_MASK_NF_420_Y_IN	INT_MASK_NF_422_IN	INT_MASK_GRPX3_ST	INT_MASK_GRPX2_ST	INT_MASK_GRPX1_ST	INT_MASK_VIP2_UP_UV	INT_MASK_VIP2_UP_Y
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_LO_UV	INT_MASK_VIP2_LO_Y	INT_MASK_VIP1_UP_UV	INT_MASK_VIP1_UP_Y	INT_MASK_VIP1_LO_UV	INT_MASK_VIP1_LO_Y	INT_MASK_GRPX3_DATA	INT_MASK_GRPX2_DATA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-282. VPDMA_int2_client1_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	INT_MASK_VIP2_ANC_B	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_ANC_A	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_ANC_B	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_ANC_A	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_TRANS2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_TRANS2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_TRANS1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_TRANS1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_HDMI_WRBK_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
20	INT_MASK_VPI_CTL	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-282. VPDMA_int2_client1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	INT_MASK_VBI_SDVENC	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	Reserved	R	0h	
17	INT_MASK_NF_420_UV_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_NF_420_Y_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_NF_420_UV_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_NF_420_Y_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_NF_422_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_GRPX3_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_GRPX2_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_GRPX1_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_UP_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_UP_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_LO_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_LO_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_UP_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_UP_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_LO_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_VIP1_LO_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_GRPX3_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-282. VPDMA_int2_client1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT_MASK_GRPX2_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.71 VPDMA_int2_list0_int_stat Register (offset = 128h) [reset = 0h]

VPDMA_int2_list0_int_stat is shown in Figure 1-371 and described in Table 1-283.

Figure 1-371. VPDMA_int2_list0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_CONTROL_DESCRIPTOR_INT15	INT_STAT_CONTROL_DESCRIPTOR_INT14	INT_STAT_CONTROL_DESCRIPTOR_INT13	INT_STAT_CONTROL_DESCRIPTOR_INT12	INT_STAT_CONTROL_DESCRIPTOR_INT11	INT_STAT_CONTROL_DESCRIPTOR_INT10	INT_STAT_CONTROL_DESCRIPTOR_INT9	INT_STAT_CONTROL_DESCRIPTOR_INT8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_CONTROL_DESCRIPTOR_INT7	INT_STAT_CONTROL_DESCRIPTOR_INT6	INT_STAT_CONTROL_DESCRIPTOR_INT5	INT_STAT_CONTROL_DESCRIPTOR_INT4	INT_STAT_CONTROL_DESCRIPTOR_INT3	INT_STAT_CONTROL_DESCRIPTOR_INT2	INT_STAT_CONTROL_DESCRIPTOR_INT1	INT_STAT_CONTROL_DESCRIPTOR_INT0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_LIST7_NOTIFY	INT_STAT_LIST7_COMPLETE	INT_STAT_LIST6_NOTIFY	INT_STAT_LIST6_COMPLETE	INT_STAT_LIST5_NOTIFY	INT_STAT_LIST5_COMPLETE	INT_STAT_LIST4_NOTIFY	INT_STAT_LIST4_COMPLETE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_LIST3_NOTIFY	INT_STAT_LIST3_COMPLETE	INT_STAT_LIST2_NOTIFY	INT_STAT_LIST2_COMPLETE	INT_STAT_LIST1_NOTIFY	INT_STAT_LIST1_COMPLETE	INT_STAT_LIST0_NOTIFY	INT_STAT_LIST0_COMPLETE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-283. VPDMA_int2_list0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_CONTROL_DESCRIPTOR_INT15	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 15. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_CONTROL_DESCRIPTOR_INT14	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 14. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_CONTROL_DESCRIPTOR_INT13	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 13. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_CONTROL_DESCRIPTOR_INT12	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 12. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_CONTROL_DESCRIPTOR_INT11	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 11. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_CONTROL_DESCRIPTOR_INT10	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 10. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_CONTROL_DESCRIPTOR_INT9	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 9. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_CONTROL_DESCRIPTOR_INT8	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 8. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-283. VPDMA_int2_list0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	INT_STAT_CONTROL_DESCRIPTOR_INT7	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 7. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_CONTROL_DESCRIPTOR_INT6	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 6. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_CONTROL_DESCRIPTOR_INT5	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 5. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_CONTROL_DESCRIPTOR_INT4	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 4. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_CONTROL_DESCRIPTOR_INT3	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 3. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_CONTROL_DESCRIPTOR_INT2	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 2. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_CONTROL_DESCRIPTOR_INT1	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 1. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_CONTROL_DESCRIPTOR_INT0	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 0. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_LIST7_NOTIFY	W	0h	A channel set by List 7 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_LIST7_COMPLETE	W	0h	List 7 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_LIST6_NOTIFY	W	0h	A channel set by List 6 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_LIST6_COMPLETE	W	0h	List 6 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_LIST5_NOTIFY	W	0h	A channel set by List 5 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_LIST5_COMPLETE	W	0h	List 5 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_LIST4_NOTIFY	W	0h	A channel set by List 4 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-283. VPDMA_int2_list0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT_STAT_LIST4_COMPLETE	W	0h	List 4 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_LIST3_NOTIFY	W	0h	A channel set by List 3 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_LIST3_COMPLETE	W	0h	List 3 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
5	INT_STAT_LIST2_NOTIFY	W	0h	A channel set by List 2 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_LIST2_COMPLETE	W	0h	List 2 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_LIST1_NOTIFY	W	0h	A channel set by List 1 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_LIST1_COMPLETE	W	0h	List 1 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_LIST0_NOTIFY	W	0h	A channel set by List 0 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_LIST0_COMPLETE	W	0h	List 0 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.72 VPDMA_int2_list0_int_mask Register (offset = 12Ch) [reset = 0h]

VPDMA_int2_list0_int_mask is shown in Figure 1-372 and described in Table 1-284.

Figure 1-372. VPDMA_int2_list0_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_CONTROL_DESCRIPTOR_INT15	INT_MASK_CONTROL_DESCRIPTOR_INT14	INT_MASK_CONTROL_DESCRIPTOR_INT13	INT_MASK_CONTROL_DESCRIPTOR_INT12	INT_MASK_CONTROL_DESCRIPTOR_INT11	INT_MASK_CONTROL_DESCRIPTOR_INT10	INT_MASK_CONTROL_DESCRIPTOR_INT9	INT_MASK_CONTROL_DESCRIPTOR_INT8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_CONTROL_DESCRIPTOR_INT7	INT_MASK_CONTROL_DESCRIPTOR_INT6	INT_MASK_CONTROL_DESCRIPTOR_INT5	INT_MASK_CONTROL_DESCRIPTOR_INT4	INT_MASK_CONTROL_DESCRIPTOR_INT3	INT_MASK_CONTROL_DESCRIPTOR_INT2	INT_MASK_CONTROL_DESCRIPTOR_INT1	INT_MASK_CONTROL_DESCRIPTOR_INT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_LIST7_NOTIFY	INT_MASK_LIST7_COMPLETE	INT_MASK_LIST6_NOTIFY	INT_MASK_LIST6_COMPLETE	INT_MASK_LIST5_NOTIFY	INT_MASK_LIST5_COMPLETE	INT_MASK_LIST4_NOTIFY	INT_MASK_LIST4_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_LIST3_NOTIFY	INT_MASK_LIST3_COMPLETE	INT_MASK_LIST2_NOTIFY	INT_MASK_LIST2_COMPLETE	INT_MASK_LIST1_NOTIFY	INT_MASK_LIST1_COMPLETE	INT_MASK_LIST0_NOTIFY	INT_MASK_LIST0_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-284. VPDMA_int2_list0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_CONTROL_DESCRIPTOR_INT15	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_CONTROL_DESCRIPTOR_INT14	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_CONTROL_DESCRIPTOR_INT13	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_CONTROL_DESCRIPTOR_INT12	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_CONTROL_DESCRIPTOR_INT11	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_CONTROL_DESCRIPTOR_INT10	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_CONTROL_DESCRIPTOR_INT9	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_CONTROL_DESCRIPTOR_INT8	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_CONTROL_DESCRIPTOR_INT7	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_CONTROL_DESCRIPTOR_INT6	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-284. VPDMA_int2_list0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	INT_MASK_CONTROL_DESCRIPTOR_INT5	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
20	INT_MASK_CONTROL_DESCRIPTOR_INT4	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_CONTROL_DESCRIPTOR_INT3	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_CONTROL_DESCRIPTOR_INT2	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_CONTROL_DESCRIPTOR_INT1	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_CONTROL_DESCRIPTOR_INT0	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_LIST7_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_LIST7_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_LIST6_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_LIST6_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_LIST5_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_LIST5_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_LIST4_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_LIST4_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_LIST3_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_LIST3_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_LIST2_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_LIST2_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-284. VPDMA_int2_list0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT_MASK_LIST1_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_LIST1_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_LIST0_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_LIST0_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int2. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.73 VPDMA_int3_channel0_int_stat Register (offset = 130h) [reset = 0h]

VPDMA_int3_channel0_int_stat is shown in Figure 1-373 and described in Table 1-285.

Figure 1-373. VPDMA_int3_channel0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_GRPX3	INT_STAT_GRPX2	INT_STAT_GRPX1	INT_STAT_SCALER_OUT	Reserved			
W-0h	W-0h	W-0h	W-0h	R-0h			
23	22	21	20	19	18	17	16
Reserved				INT_STAT_SCALER_CHROMA	INT_STAT_SCALER_LUMA	INT_STAT_HQ_SCALER	Reserved
R-0h				W-0h	W-0h	W-0h	R-0h
15	14	13	12	11	10	9	8
INT_STAT_HQ_MV_OUT	Reserved		INT_STAT_HQ_MV	Reserved			
W-0h	R-0h		W-0h	R-0h			
7	6	5	4	3	2	1	0
Reserved		INT_STAT_HQ_VID3_CHROMA	INT_STAT_HQ_VID3_LUMA	INT_STAT_HQ_VID2_CHROMA	INT_STAT_HQ_VID2_LUMA	INT_STAT_HQ_VID1_CHROMA	INT_STAT_HQ_VID1_LUMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-285. VPDMA_int3_channel0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_GRPX3	W	0h	The last read DMA transaction has occurred for channel grpx3 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_GRPX2	W	0h	The last read DMA transaction has occurred for channel grpx2 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_GRPX1	W	0h	The last read DMA transaction has occurred for channel grpx1 and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_data will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_SCALER_OUT	W	0h	The last write DMA transaction has completed for channel scaler_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27-20	Reserved	R	0h	
19	INT_STAT_SCALER_CHROMA	W	0h	The last write DMA transaction has completed for channel scaler_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-285. VPDMA_int3_channel0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	INT_STAT_SCALER_LUMA	W	0h	The last write DMA transaction has completed for channel scaler_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_HQ_SCALER	W	0h	The last write DMA transaction has completed for channel hq_scaler. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_sc_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	Reserved	R	0h	
15	INT_STAT_HQ_MV_OUT	W	0h	The last write DMA transaction has completed for channel hq_mv_out. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client dei_hq_mv_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14-13	Reserved	R	0h	
12	INT_STAT_HQ_MV	W	0h	The last read DMA transaction has occurred for channel hq_mv and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_hq_mv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11-6	Reserved	R	0h	
5	INT_STAT_HQ_VID3_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid3_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_3_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_HQ_VID3_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid3_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_3_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_HQ_VID2_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid2_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_2_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_HQ_VID2_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid2_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_2_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

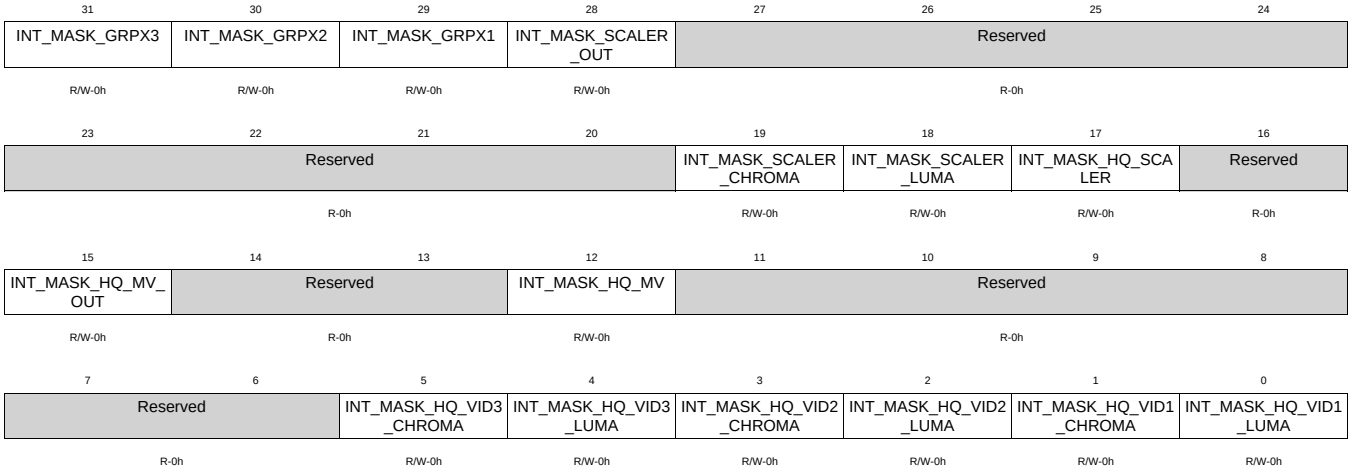
Table 1-285. VPDMA_int3_channel0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_STAT_HQ_VID1_CHROMA	W	0h	The last read DMA transaction has occurred for channel hq_vid1_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_1_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_HQ_VID1_LUMA	W	0h	The last read DMA transaction has occurred for channel hq_vid1_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client dei_1_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.74 VPDMA_int3_channel0_int_mask Register (offset = 134h) [reset = 0h]

VPDMA_int3_channel0_int_mask is shown in Figure 1-374 and described in Table 1-286.

Figure 1-374. VPDMA_int3_channel0_int_mask Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-286. VPDMA_int3_channel0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_GRPX3	R/W	0h	The interrupt for Graphcis 2 Data should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_GRPX2	R/W	0h	The interrupt for Graphics 1 Data should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_GRPX1	R/W	0h	The interrupt for Graphics 0 Data should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_SCALER_OUT	R/W	0h	The interrupt for Low Cost DEI Scalar Write to Memory should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
27-20	Reserved	R	0h	
19	INT_MASK_SCALER_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_SCALER_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_HQ_SCALER	R/W	0h	The interrupt for High Quality DEI Scaler Write to Memory should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	Reserved	R	0h	
15	INT_MASK_HQ_MV_OUT	R/W	0h	The interrupt for Low Cost DEI Motion Vector Write should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14-13	Reserved	R	0h	
12	INT_MASK_HQ_MV	R/W	0h	The interrupt for Low Cost DEI Motion Vector should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11-6	Reserved	R	0h	

Table 1-286. VPDMA_int3_channel0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_MASK_HQ_VID3_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_HQ_VID3_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_HQ_VID2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_HQ_VID2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_HQ_VID1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_HQ_VID1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.75 VPDMA_int3_channel1_int_stat Register (offset = 138h) [reset = 0h]

VPDMA_int3_channel1_int_stat is shown in Figure 1-375 and described in Table 1-287.

Figure 1-375. VPDMA_int3_channel1_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP1_MULT_PORTB_SRC9	INT_STAT_VIP1_MULT_PORTB_SRC8	INT_STAT_VIP1_MULT_PORTB_SRC7	INT_STAT_VIP1_MULT_PORTB_SRC6	INT_STAT_VIP1_MULT_PORTB_SRC5	INT_STAT_VIP1_MULT_PORTB_SRC4	INT_STAT_VIP1_MULT_PORTB_SRC3	INT_STAT_VIP1_MULT_PORTB_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP1_MULT_PORTB_SRC1	INT_STAT_VIP1_MULT_PORTB_SRC0	INT_STAT_VIP1_MULT_PORTA_SRC15	INT_STAT_VIP1_MULT_PORTA_SRC14	INT_STAT_VIP1_MULT_PORTA_SRC13	INT_STAT_VIP1_MULT_PORTA_SRC12	INT_STAT_VIP1_MULT_PORTA_SRC11	INT_STAT_VIP1_MULT_PORTA_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP1_MULT_PORTA_SRC9	INT_STAT_VIP1_MULT_PORTA_SRC8	INT_STAT_VIP1_MULT_PORTA_SRC7	INT_STAT_VIP1_MULT_PORTA_SRC6	INT_STAT_VIP1_MULT_PORTA_SRC5	INT_STAT_VIP1_MULT_PORTA_SRC4	INT_STAT_VIP1_MULT_PORTA_SRC3	INT_STAT_VIP1_MULT_PORTA_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_PORTA_SRC1	INT_STAT_VIP1_MULT_PORTA_SRC0	INT_STAT_GRPX3_CLUT	INT_STAT_GRPX2_CLUT	INT_STAT_GRPX1_CLUT	INT_STAT_GRPX3_STENCIL	INT_STAT_GRPX2_STENCIL	INT_STAT_GRPX1_STENCIL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-287. VPDMA_int3_channel1_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP1_MULT_PORTB_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP1_MULT_PORTB_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP1_MULT_PORTB_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP1_MULT_PORTB_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_MULT_PORTB_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_MULT_PORTB_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-287. VPDMA_int3_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP1_MULT_PORTB_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP1_MULT_PORTB_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP1_MULT_PORTB_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP1_MULT_PORTB_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP1_MULT_PORTA_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP1_MULT_PORTA_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP1_MULT_PORTA_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP1_MULT_PORTA_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP1_MULT_PORTA_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP1_MULT_PORTA_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-287. VPDMA_int3_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP1_MULT_PORTA_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP1_MULT_PORTA_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP1_MULT_PORTA_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP1_MULT_PORTA_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_MULT_PORTA_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_MULT_PORTA_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_MULT_PORTA_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_MULT_PORTA_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_MULT_PORTA_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_MULT_PORTA_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-287. VPDMA_int3_channel1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_GRPX3_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx3_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_GRPX2_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx2_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_GRPX1_CLUT	W	0h	The last read DMA transaction has occurred for channel grpx1_clut and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_clut_clt will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_GRPX3_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx3_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx3_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_GRPX2_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx2_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx2_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_GRPX1_STENCIL	W	0h	The last read DMA transaction has occurred for channel grpx1_stencil and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client grpx1_st will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.76 VPDMA_int3_channel1_int_mask Register (offset = 13Ch) [reset = 0h]

VPDMA_int3_channel1_int_mask is shown in Figure 1-376 and described in Table 1-288.

Figure 1-376. VPDMA_int3_channel1_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP1_MULT_PORTB_SRC9	INT_MASK_VIP1_MULT_PORTB_SRC8	INT_MASK_VIP1_MULT_PORTB_SRC7	INT_MASK_VIP1_MULT_PORTB_SRC6	INT_MASK_VIP1_MULT_PORTB_SRC5	INT_MASK_VIP1_MULT_PORTB_SRC4	INT_MASK_VIP1_MULT_PORTB_SRC3	INT_MASK_VIP1_MULT_PORTB_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP1_MULT_PORTB_SRC1	INT_MASK_VIP1_MULT_PORTB_SRC0	INT_MASK_VIP1_MULT_PORTA_SRC15	INT_MASK_VIP1_MULT_PORTA_SRC14	INT_MASK_VIP1_MULT_PORTA_SRC13	INT_MASK_VIP1_MULT_PORTA_SRC12	INT_MASK_VIP1_MULT_PORTA_SRC11	INT_MASK_VIP1_MULT_PORTA_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP1_MULT_PORTA_SRC9	INT_MASK_VIP1_MULT_PORTA_SRC8	INT_MASK_VIP1_MULT_PORTA_SRC7	INT_MASK_VIP1_MULT_PORTA_SRC6	INT_MASK_VIP1_MULT_PORTA_SRC5	INT_MASK_VIP1_MULT_PORTA_SRC4	INT_MASK_VIP1_MULT_PORTA_SRC3	INT_MASK_VIP1_MULT_PORTA_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_PORTA_SRC1	INT_MASK_VIP1_MULT_PORTA_SRC0	INT_MASK_GRPX3_CLUT	INT_MASK_GRPX2_CLUT	INT_MASK_GRPX1_CLUT	INT_MASK_GRPX3_STENCIL	INT_MASK_GRPX2_STENCIL	INT_MASK_GRPX1_STENCIL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-288. VPDMA_int3_channel1_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP1_MULT_PORTB_SRC9	R/W	0h	The interrupt for Video Input 1 Port B Channel 9 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP1_MULT_PORTB_SRC8	R/W	0h	The interrupt for Video Input 1 Port B Channel 8 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP1_MULT_PORTB_SRC7	R/W	0h	The interrupt for Video Input 1 Port B Channel 7 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP1_MULT_PORTB_SRC6	R/W	0h	The interrupt for Video Input 1 Port B Channel 6 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_MULT_PORTB_SRC5	R/W	0h	The interrupt for Video Input 1 Port B Channel 5 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_MULT_PORTB_SRC4	R/W	0h	The interrupt for Video Input 1 Port B Channel 4 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP1_MULT_PORTB_SRC3	R/W	0h	The interrupt for Video Input 1 Port B Channel 3 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP1_MULT_PORTB_SRC2	R/W	0h	The interrupt for Video Input 1 Port B Channel 2 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP1_MULT_PORTB_SRC1	R/W	0h	The interrupt for Video Input 1 Port B Channel 1 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP1_MULT_PORTB_SRC0	R/W	0h	The interrupt for Video Input 1 Port B Channel 0 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP1_MULT_PORTA_SRC15	R/W	0h	The interrupt for Video Input 1 Port A Channel 15 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-288. VPDMA_int3_channel1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP1_MULT_PORTA_SRC14	R/W	0h	The interrupt for Video Input 1 Port A Channel 14 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP1_MULT_PORTA_SRC13	R/W	0h	The interrupt for Video Input 1 Port A Channel 13 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP1_MULT_PORTA_SRC12	R/W	0h	The interrupt for Video Input 1 Port A Channel 12 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP1_MULT_PORTA_SRC11	R/W	0h	The interrupt for Video Input 1 Port A Channel 11 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP1_MULT_PORTA_SRC10	R/W	0h	The interrupt for Video Input 1 Port A Channel 10 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP1_MULT_PORTA_SRC9	R/W	0h	The interrupt for Video Input 1 Port A Channel 9 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP1_MULT_PORTA_SRC8	R/W	0h	The interrupt for Video Input 1 Port A Channel 8 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP1_MULT_PORTA_SRC7	R/W	0h	The interrupt for Video Input 1 Port A Channel 7 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP1_MULT_PORTA_SRC6	R/W	0h	The interrupt for Video Input 1 Port A Channel 6 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_MULT_PORTA_SRC5	R/W	0h	The interrupt for Video Input 1 Port A Channel 5 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_MULT_PORTA_SRC4	R/W	0h	The interrupt for Video Input 1 Port A Channel 4 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_MULT_PORTA_SRC3	R/W	0h	The interrupt for Video Input 1 Port A Channel 3 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_MULT_PORTA_SRC2	R/W	0h	The interrupt for Video Input 1 Port A Channel 2 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_MULT_PORTA_SRC1	R/W	0h	The interrupt for Video Input 1 Port A Channel 1 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_MULT_PORTA_SRC0	R/W	0h	The interrupt for Video Input 1 Port A Channel 0 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_GRPX3_CLUT	R/W	0h	The interrupt for Graphics 2 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_GRPX2_CLUT	R/W	0h	The interrupt for Graphics 1 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_GRPX1_CLUT	R/W	0h	The interrupt for Graphics 0 Color Lookup Table Load from Memory should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-288. VPDMA_int3_channel1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_GRPX3_STENCIL	R/W	0h	The interrupt for Graphics 2 Stencil should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_GRPX2_STENCIL	R/W	0h	The interrupt for Graphics 1 Stencil should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_GRPX1_STENCIL	R/W	0h	The interrupt for Graphics 0 Stencil should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.77 VPDMA_int3_channel2_int_stat Register (offset = 140h) [reset = 0h]

VPDMA_int3_channel2_int_stat is shown in Figure 1-377 and described in Table 1-289.

Figure 1-377. VPDMA_int3_channel2_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP1_MULT_ANCB_SRC9	INT_STAT_VIP1_MULT_ANCB_SRC8	INT_STAT_VIP1_MULT_ANCB_SRC7	INT_STAT_VIP1_MULT_ANCB_SRC6	INT_STAT_VIP1_MULT_ANCB_SRC5	INT_STAT_VIP1_MULT_ANCB_SRC4	INT_STAT_VIP1_MULT_ANCB_SRC3	INT_STAT_VIP1_MULT_ANCB_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP1_MULT_ANCB_SRC1	INT_STAT_VIP1_MULT_ANCB_SRC0	INT_STAT_VIP1_MULT_ANCA_SRC15	INT_STAT_VIP1_MULT_ANCA_SRC14	INT_STAT_VIP1_MULT_ANCA_SRC13	INT_STAT_VIP1_MULT_ANCA_SRC12	INT_STAT_VIP1_MULT_ANCA_SRC11	INT_STAT_VIP1_MULT_ANCA_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP1_MULT_ANCA_SRC9	INT_STAT_VIP1_MULT_ANCA_SRC8	INT_STAT_VIP1_MULT_ANCA_SRC7	INT_STAT_VIP1_MULT_ANCA_SRC6	INT_STAT_VIP1_MULT_ANCA_SRC5	INT_STAT_VIP1_MULT_ANCA_SRC4	INT_STAT_VIP1_MULT_ANCA_SRC3	INT_STAT_VIP1_MULT_ANCA_SRC2
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_MULT_ANCA_SRC1	INT_STAT_VIP1_MULT_ANCA_SRC0	INT_STAT_VIP1_MULT_PORTB_SRC15	INT_STAT_VIP1_MULT_PORTB_SRC14	INT_STAT_VIP1_MULT_PORTB_SRC13	INT_STAT_VIP1_MULT_PORTB_SRC12	INT_STAT_VIP1_MULT_PORTB_SRC11	INT_STAT_VIP1_MULT_PORTB_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-289. VPDMA_int3_channel2_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP1_MULT_ANCB_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP1_MULT_ANCB_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP1_MULT_ANCB_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP1_MULT_ANCB_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_MULT_ANCB_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_MULT_ANCB_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-289. VPDMA_int3_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP1_MULT_ANCB_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP1_MULT_ANCB_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP1_MULT_ANCB_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP1_MULT_ANCB_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP1_MULT_ANCA_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP1_MULT_ANCA_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP1_MULT_ANCA_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP1_MULT_ANCA_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP1_MULT_ANCA_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP1_MULT_ANCA_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-289. VPDMA_int3_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP1_MULT_ANCA_SRC9	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP1_MULT_ANCA_SRC8	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP1_MULT_ANCA_SRC7	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP1_MULT_ANCA_SRC6	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_MULT_ANCA_SRC5	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_MULT_ANCA_SRC4	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_MULT_ANCA_SRC3	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_MULT_ANCA_SRC2	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_MULT_ANCA_SRC1	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_MULT_ANCA_SRC0	W	0h	The last write DMA transaction has completed for channel vip1_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-289. VPDMA_int3_channel2_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_MULT_PORTB_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_MULT_PORTB_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_MULT_PORTB_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_MULT_PORTB_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP1_MULT_PORTB_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP1_MULT_PORTB_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.78 VPDMA_int3_channel2_int_mask Register (offset = 144h) [reset = 0h]

VPDMA_int3_channel2_int_mask is shown in Figure 1-378 and described in Table 1-290.

Figure 1-378. VPDMA_int3_channel2_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP1_MULT_ANCB_SRC9	INT_MASK_VIP1_MULT_ANCB_SRC8	INT_MASK_VIP1_MULT_ANCB_SRC7	INT_MASK_VIP1_MULT_ANCB_SRC6	INT_MASK_VIP1_MULT_ANCB_SRC5	INT_MASK_VIP1_MULT_ANCB_SRC4	INT_MASK_VIP1_MULT_ANCB_SRC3	INT_MASK_VIP1_MULT_ANCB_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP1_MULT_ANCB_SRC1	INT_MASK_VIP1_MULT_ANCB_SRC0	INT_MASK_VIP1_MULT_ANCA_SRC15	INT_MASK_VIP1_MULT_ANCA_SRC14	INT_MASK_VIP1_MULT_ANCA_SRC13	INT_MASK_VIP1_MULT_ANCA_SRC12	INT_MASK_VIP1_MULT_ANCA_SRC11	INT_MASK_VIP1_MULT_ANCA_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP1_MULT_ANCA_SRC9	INT_MASK_VIP1_MULT_ANCA_SRC8	INT_MASK_VIP1_MULT_ANCA_SRC7	INT_MASK_VIP1_MULT_ANCA_SRC6	INT_MASK_VIP1_MULT_ANCA_SRC5	INT_MASK_VIP1_MULT_ANCA_SRC4	INT_MASK_VIP1_MULT_ANCA_SRC3	INT_MASK_VIP1_MULT_ANCA_SRC2
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_MULT_ANCA_SRC1	INT_MASK_VIP1_MULT_ANCA_SRC0	INT_MASK_VIP1_MULT_PORTB_SRC15	INT_MASK_VIP1_MULT_PORTB_SRC14	INT_MASK_VIP1_MULT_PORTB_SRC13	INT_MASK_VIP1_MULT_PORTB_SRC12	INT_MASK_VIP1_MULT_PORTB_SRC11	INT_MASK_VIP1_MULT_PORTB_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-290. VPDMA_int3_channel2_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP1_MULT_ANCB_SRC9	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP1_MULT_ANCB_SRC8	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP1_MULT_ANCB_SRC7	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP1_MULT_ANCB_SRC6	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_MULT_ANCB_SRC5	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_MULT_ANCB_SRC4	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP1_MULT_ANCB_SRC3	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP1_MULT_ANCB_SRC2	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP1_MULT_ANCB_SRC1	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP1_MULT_ANCB_SRC0	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP1_MULT_ANCA_SRC15	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-290. VPDMA_int3_channel2_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP1_MULT_ANCA_SRC14	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP1_MULT_ANCA_SRC13	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP1_MULT_ANCA_SRC12	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP1_MULT_ANCA_SRC11	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP1_MULT_ANCA_SRC10	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP1_MULT_ANCA_SRC9	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP1_MULT_ANCA_SRC8	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP1_MULT_ANCA_SRC7	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP1_MULT_ANCA_SRC6	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_MULT_ANCA_SRC5	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_MULT_ANCA_SRC4	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_MULT_ANCA_SRC3	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_MULT_ANCA_SRC2	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_MULT_ANCA_SRC1	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_MULT_ANCA_SRC0	R/W	0h	The interrupt for Video Input 1 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_MULT_PORTB_SRC15	R/W	0h	The interrupt for Video Input 1 Port B Channel 15 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_MULT_PORTB_SRC14	R/W	0h	The interrupt for Video Input 1 Port B Channel 14 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_MULT_PORTB_SRC13	R/W	0h	The interrupt for Video Input 1 Port B Channel 13 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-290. VPDMA_int3_channel2_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP1_MULT_PORTB_SRC12	R/W	0h	The interrupt for Video Input 1 Port B Channel 12 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP1_MULT_PORTB_SRC11	R/W	0h	The interrupt for Video Input 1 Port B Channel 11 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP1_MULT_PORTB_SRC10	R/W	0h	The interrupt for Video Input 1 Port B Channel 10 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.79 VPDMA_int3_channel3_int_stat Register (offset = 148h) [reset = 0h]

VPDMA_int3_channel3_int_stat is shown in Figure 1-379 and described in Table 1-291.

Figure 1-379. VPDMA_int3_channel3_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP2_MULT_PORTB_SRC3	INT_STAT_VIP2_MULT_PORTB_SRC2	INT_STAT_VIP2_MULT_PORTB_SRC1	INT_STAT_VIP2_MULT_PORTB_SRC0	INT_STAT_VIP2_MULT_PORTA_SRC15	INT_STAT_VIP2_MULT_PORTA_SRC14	INT_STAT_VIP2_MULT_PORTA_SRC13	INT_STAT_VIP2_MULT_PORTA_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP2_MULT_PORTA_SRC11	INT_STAT_VIP2_MULT_PORTA_SRC10	INT_STAT_VIP2_MULT_PORTA_SRC9	INT_STAT_VIP2_MULT_PORTA_SRC8	INT_STAT_VIP2_MULT_PORTA_SRC7	INT_STAT_VIP2_MULT_PORTA_SRC6	INT_STAT_VIP2_MULT_PORTA_SRC5	INT_STAT_VIP2_MULT_PORTA_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_MULT_PORTA_SRC3	INT_STAT_VIP2_MULT_PORTA_SRC2	INT_STAT_VIP2_MULT_PORTA_SRC1	INT_STAT_VIP2_MULT_PORTA_SRC0	INT_STAT_VIP1_PORTB_RGB	INT_STAT_VIP1_PORTA_RGB	INT_STAT_VIP1_PORTB_CHROMA	INT_STAT_VIP1_PORTB_LUMA
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP1_PORTA_CHROMA	INT_STAT_VIP1_PORTA_LUMA	INT_STAT_VIP1_MULT_ANCB_SRC15	INT_STAT_VIP1_MULT_ANCB_SRC14	INT_STAT_VIP1_MULT_ANCB_SRC13	INT_STAT_VIP1_MULT_ANCB_SRC12	INT_STAT_VIP1_MULT_ANCB_SRC11	INT_STAT_VIP1_MULT_ANCB_SRC10
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-291. VPDMA_int3_channel3_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP2_MULT_PORTB_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP2_MULT_PORTB_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP2_MULT_PORTB_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_MULT_PORTB_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP2_MULT_PORTA_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP2_MULT_PORTA_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-291. VPDMA_int3_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP2_MULT_PORTA_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP2_MULT_PORTA_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP2_MULT_PORTA_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP2_MULT_PORTA_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP2_MULT_PORTA_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP2_MULT_PORTA_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP2_MULT_PORTA_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP2_MULT_PORTA_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_MULT_PORTA_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP2_MULT_PORTA_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-291. VPDMA_int3_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP2_MULT_PORTA_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_MULT_PORTA_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_MULT_PORTA_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_MULT_PORTA_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_porta_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP1_PORTB_RGB	W	0h	The last write DMA transaction has completed for channel vip1_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP1_PORTA_RGB	W	0h	The last write DMA transaction has completed for channel vip1_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP1_PORTB_CHROMA	W	0h	The last write DMA transaction has completed for channel vip1_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP1_PORTB_LUMA	W	0h	The last write DMA transaction has completed for channel vip1_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP1_PORTA_CHROMA	W	0h	The last write DMA transaction has completed for channel vip1_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP1_PORTA_LUMA	W	0h	The last write DMA transaction has completed for channel vip1_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-291. VPDMA_int3_channel3_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_MULT_ANCB_SRC15	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_MULT_ANCB_SRC14	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_MULT_ANCB_SRC13	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_MULT_ANCB_SRC12	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP1_MULT_ANCB_SRC11	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP1_MULT_ANCB_SRC10	W	0h	The last write DMA transaction has completed for channel vip1_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip1_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.80 VPDMA_int3_channel3_int_mask Register (offset = 14Ch) [reset = 0h]

VPDMA_int3_channel3_int_mask is shown in Figure 1-380 and described in Table 1-292.

Figure 1-380. VPDMA_int3_channel3_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP2_MULT_PORTB_SRC3	INT_MASK_VIP2_MULT_PORTB_SRC2	INT_MASK_VIP2_MULT_PORTB_SRC1	INT_MASK_VIP2_MULT_PORTB_SRC0	INT_MASK_VIP2_MULT_PORTA_SRC15	INT_MASK_VIP2_MULT_PORTA_SRC14	INT_MASK_VIP2_MULT_PORTA_SRC13	INT_MASK_VIP2_MULT_PORTA_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP2_MULT_PORTA_SRC11	INT_MASK_VIP2_MULT_PORTA_SRC10	INT_MASK_VIP2_MULT_PORTA_SRC9	INT_MASK_VIP2_MULT_PORTA_SRC8	INT_MASK_VIP2_MULT_PORTA_SRC7	INT_MASK_VIP2_MULT_PORTA_SRC6	INT_MASK_VIP2_MULT_PORTA_SRC5	INT_MASK_VIP2_MULT_PORTA_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_MULT_PORTA_SRC3	INT_MASK_VIP2_MULT_PORTA_SRC2	INT_MASK_VIP2_MULT_PORTA_SRC1	INT_MASK_VIP2_MULT_PORTA_SRC0	INT_MASK_VIP1_PORTB_RGB	INT_MASK_VIP1_PORTA_RGB	INT_MASK_VIP1_PORTB_CHROMA	INT_MASK_VIP1_PORTB_LUMA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP1_PORTA_CHROMA	INT_MASK_VIP1_PORTA_LUMA	INT_MASK_VIP1_MULT_ANCB_SRC15	INT_MASK_VIP1_MULT_ANCB_SRC14	INT_MASK_VIP1_MULT_ANCB_SRC13	INT_MASK_VIP1_MULT_ANCB_SRC12	INT_MASK_VIP1_MULT_ANCB_SRC11	INT_MASK_VIP1_MULT_ANCB_SRC10
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-292. VPDMA_int3_channel3_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP2_MULT_PORTB_SRC3	R/W	0h	The interrupt for Video Input 2 Port B Channel 3 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP2_MULT_PORTB_SRC2	R/W	0h	The interrupt for Video Input 2 Port B Channel 2 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP2_MULT_PORTB_SRC1	R/W	0h	The interrupt for Video Input 2 Port B Channel 1 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_MULT_PORTB_SRC0	R/W	0h	The interrupt for Video Input 2 Port B Channel 0 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP2_MULT_PORTA_SRC15	R/W	0h	The interrupt for Video Input 2 Port A Channel 15 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP2_MULT_PORTA_SRC14	R/W	0h	The interrupt for Video Input 2 Port A Channel 14 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP2_MULT_PORTA_SRC13	R/W	0h	The interrupt for Video Input 2 Port A Channel 13 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP2_MULT_PORTA_SRC12	R/W	0h	The interrupt for Video Input 2 Port A Channel 12 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP2_MULT_PORTA_SRC11	R/W	0h	The interrupt for Video Input 2 Port A Channel 11 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP2_MULT_PORTA_SRC10	R/W	0h	The interrupt for Video Input 2 Port A Channel 10 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP2_MULT_PORTA_SRC9	R/W	0h	The interrupt for Video Input 2 Port A Channel 9 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-292. VPDMA_int3_channel3_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP2_MULT_PORTA_SRC8	R/W	0h	The interrupt for Video Input 2 Port A Channel 8 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP2_MULT_PORTA_SRC7	R/W	0h	The interrupt for Video Input 2 Port A Channel 7 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP2_MULT_PORTA_SRC6	R/W	0h	The interrupt for Video Input 2 Port A Channel 6 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_MULT_PORTA_SRC5	R/W	0h	The interrupt for Video Input 2 Port A Channel 5 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_MULT_PORTA_SRC4	R/W	0h	The interrupt for Video Input 2 Port A Channel 4 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_MULT_PORTA_SRC3	R/W	0h	The interrupt for Video Input 2 Port A Channel 3 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_MULT_PORTA_SRC2	R/W	0h	The interrupt for Video Input 2 Port A Channel 2 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_MULT_PORTA_SRC1	R/W	0h	The interrupt for Video Input 2 Port A Channel 1 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_MULT_PORTA_SRC0	R/W	0h	The interrupt for Video Input 2 Port A Channel 0 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP1_PORTB_RGB	R/W	0h	The interrupt for Video Input 1 Port B RGB Data should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP1_PORTA_RGB	R/W	0h	The interrupt for Video Input 1 Port A RGB Data should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP1_PORTB_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP1_PORTB_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP1_PORTA_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP1_PORTA_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_MULT_ANCB_SRC15	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_MULT_ANCB_SRC14	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_MULT_ANCB_SRC13	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-292. VPDMA_int3_channel3_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP1_MULT_ANCB_SRC12	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP1_MULT_ANCB_SRC11	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP1_MULT_ANCB_SRC10	R/W	0h	The interrupt for Video Input 1 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.81 VPDMA_int3_channel4_int_stat Register (offset = 150h) [reset = 0h]

VPDMA_int3_channel4_int_stat is shown in Figure 1-381 and described in Table 1-293.

Figure 1-381. VPDMA_int3_channel4_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_VIP2_MULT_ANCB_SRC3	INT_STAT_VIP2_MULT_ANCB_SRC2	INT_STAT_VIP2_MULT_ANCB_SRC1	INT_STAT_VIP2_MULT_ANCB_SRC0	INT_STAT_VIP2_MULT_ANCA_SRC15	INT_STAT_VIP2_MULT_ANCA_SRC14	INT_STAT_VIP2_MULT_ANCA_SRC13	INT_STAT_VIP2_MULT_ANCA_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_VIP2_MULT_ANCA_SRC11	INT_STAT_VIP2_MULT_ANCA_SRC10	INT_STAT_VIP2_MULT_ANCA_SRC9	INT_STAT_VIP2_MULT_ANCA_SRC8	INT_STAT_VIP2_MULT_ANCA_SRC7	INT_STAT_VIP2_MULT_ANCA_SRC6	INT_STAT_VIP2_MULT_ANCA_SRC5	INT_STAT_VIP2_MULT_ANCA_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_MULT_ANCA_SRC3	INT_STAT_VIP2_MULT_ANCA_SRC2	INT_STAT_VIP2_MULT_ANCA_SRC1	INT_STAT_VIP2_MULT_ANCA_SRC0	INT_STAT_VIP2_MULT_PORTB_SRC15	INT_STAT_VIP2_MULT_PORTB_SRC14	INT_STAT_VIP2_MULT_PORTB_SRC13	INT_STAT_VIP2_MULT_PORTB_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_PORTB_SRC11	INT_STAT_VIP2_MULT_PORTB_SRC10	INT_STAT_VIP2_MULT_PORTB_SRC9	INT_STAT_VIP2_MULT_PORTB_SRC8	INT_STAT_VIP2_MULT_PORTB_SRC7	INT_STAT_VIP2_MULT_PORTB_SRC6	INT_STAT_VIP2_MULT_PORTB_SRC5	INT_STAT_VIP2_MULT_PORTB_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-293. VPDMA_int3_channel4_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_VIP2_MULT_ANCB_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_VIP2_MULT_ANCB_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_VIP2_MULT_ANCB_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_MULT_ANCB_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP2_MULT_ANCA_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP2_MULT_ANCA_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-293. VPDMA_int3_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INT_STAT_VIP2_MULT_ANCA_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VIP2_MULT_ANCA_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_VIP2_MULT_ANCA_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_VIP2_MULT_ANCA_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_VIP2_MULT_ANCA_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VIP2_MULT_ANCA_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VIP2_MULT_ANCA_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_VIP2_MULT_ANCA_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_MULT_ANCA_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_VIP2_MULT_ANCA_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-293. VPDMA_int3_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	INT_STAT_VIP2_MULT_ANCA_SRC3	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src3. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_MULT_ANCA_SRC2	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src2. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_MULT_ANCA_SRC1	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src1. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_MULT_ANCA_SRC0	W	0h	The last write DMA transaction has completed for channel vip2_mult_anca_src0. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_a then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP2_MULT_PORTB_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP2_MULT_PORTB_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_MULT_PORTB_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_MULT_PORTB_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_MULT_PORTB_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP2_MULT_PORTB_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-293. VPDMA_int3_channel4_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP2_MULT_PORTB_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP2_MULT_PORTB_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP2_MULT_PORTB_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP2_MULT_PORTB_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP2_MULT_PORTB_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP2_MULT_PORTB_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_portb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_uv then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.82 VPDMA_int3_channel4_int_mask Register (offset = 154h) [reset = 0h]

VPDMA_int3_channel4_int_mask is shown in Figure 1-382 and described in Table 1-294.

Figure 1-382. VPDMA_int3_channel4_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_VIP2_MULT_ANCB_SRC3	INT_MASK_VIP2_MULT_ANCB_SRC2	INT_MASK_VIP2_MULT_ANCB_SRC1	INT_MASK_VIP2_MULT_ANCB_SRC0	INT_MASK_VIP2_MULT_ANCA_SRC15	INT_MASK_VIP2_MULT_ANCA_SRC14	INT_MASK_VIP2_MULT_ANCA_SRC13	INT_MASK_VIP2_MULT_ANCA_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_VIP2_MULT_ANCA_SRC11	INT_MASK_VIP2_MULT_ANCA_SRC10	INT_MASK_VIP2_MULT_ANCA_SRC9	INT_MASK_VIP2_MULT_ANCA_SRC8	INT_MASK_VIP2_MULT_ANCA_SRC7	INT_MASK_VIP2_MULT_ANCA_SRC6	INT_MASK_VIP2_MULT_ANCA_SRC5	INT_MASK_VIP2_MULT_ANCA_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_MULT_ANCA_SRC3	INT_MASK_VIP2_MULT_ANCA_SRC2	INT_MASK_VIP2_MULT_ANCA_SRC1	INT_MASK_VIP2_MULT_ANCA_SRC0	INT_MASK_VIP2_MULT_PORTB_SRC15	INT_MASK_VIP2_MULT_PORTB_SRC14	INT_MASK_VIP2_MULT_PORTB_SRC13	INT_MASK_VIP2_MULT_PORTB_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_PORTB_SRC11	INT_MASK_VIP2_MULT_PORTB_SRC10	INT_MASK_VIP2_MULT_PORTB_SRC9	INT_MASK_VIP2_MULT_PORTB_SRC8	INT_MASK_VIP2_MULT_PORTB_SRC7	INT_MASK_VIP2_MULT_PORTB_SRC6	INT_MASK_VIP2_MULT_PORTB_SRC5	INT_MASK_VIP2_MULT_PORTB_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-294. VPDMA_int3_channel4_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_VIP2_MULT_ANCB_SRC3	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_VIP2_MULT_ANCB_SRC2	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_VIP2_MULT_ANCB_SRC1	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_MULT_ANCB_SRC0	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP2_MULT_ANCA_SRC15	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP2_MULT_ANCA_SRC14	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_VIP2_MULT_ANCA_SRC13	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VIP2_MULT_ANCA_SRC12	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_VIP2_MULT_ANCA_SRC11	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_VIP2_MULT_ANCA_SRC10	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_VIP2_MULT_ANCA_SRC9	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-294. VPDMA_int3_channel4_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_VIP2_MULT_ANCA_SRC8	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_VIP2_MULT_ANCA_SRC7	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_VIP2_MULT_ANCA_SRC6	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_MULT_ANCA_SRC5	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_MULT_ANCA_SRC4	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_MULT_ANCA_SRC3	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 3 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_MULT_ANCA_SRC2	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 2 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_MULT_ANCA_SRC1	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 1 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_MULT_ANCA_SRC0	R/W	0h	The interrupt for Video Input 2 Port A Ancillary Data Channel 0 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP2_MULT_PORTB_SRC15	R/W	0h	The interrupt for Video Input 2 Port B Channel 15 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP2_MULT_PORTB_SRC14	R/W	0h	The interrupt for Video Input 2 Port B Channel 14 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_MULT_PORTB_SRC13	R/W	0h	The interrupt for Video Input 2 Port B Channel 13 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_MULT_PORTB_SRC12	R/W	0h	The interrupt for Video Input 2 Port B Channel 12 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_MULT_PORTB_SRC11	R/W	0h	The interrupt for Video Input 2 Port B Channel 11 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_MULT_PORTB_SRC10	R/W	0h	The interrupt for Video Input 2 Port B Channel 10 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP2_MULT_PORTB_SRC9	R/W	0h	The interrupt for Video Input 2 Port B Channel 9 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP2_MULT_PORTB_SRC8	R/W	0h	The interrupt for Video Input 2 Port B Channel 8 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP2_MULT_PORTB_SRC7	R/W	0h	The interrupt for Video Input 2 Port B Channel 7 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-294. VPDMA_int3_channel4_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP2_MULT_PORTB_SRC6	R/W	0h	The interrupt for Video Input 2 Port B Channel 6 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP2_MULT_PORTB_SRC5	R/W	0h	The interrupt for Video Input 2 Port B Channel 5 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP2_MULT_PORTB_SRC4	R/W	0h	The interrupt for Video Input 2 Port B Channel 4 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.83 VPDMA_int3_channel5_int_stat Register (offset = 158h) [reset = 0h]

VPDMA_int3_channel5_int_stat is shown in Figure 1-383 and described in Table 1-295.

Figure 1-383. VPDMA_int3_channel5_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_TRANSCODE2_CHROMA	INT_STAT_TRANSCODE2_LUMA	INT_STAT_TRANSCODE1_CHROMA	INT_STAT_TRANSCODE1_LUMA	INT_STAT_AUX_IN	INT_STAT_PIP_FRAME	INT_STAT_POST_COMP_WR	INT_STAT_VBI_SD_VENC
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
Reserved	INT_STAT_NF_LAST_CHROMA	INT_STAT_NF_LAST_LUMA	INT_STAT_NF_WRITE_CHROMA	INT_STAT_NF_WRITE_LUMA	INT_STAT_NF_READ	INT_STAT_VIP2_PORTB_RGB	INT_STAT_VIP2_PORTA_RGB
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_VIP2_PORTB_CHROMA	INT_STAT_VIP2_PORTB_LUMA	INT_STAT_VIP2_PORTA_CHROMA	INT_STAT_VIP2_PORTA_LUMA	INT_STAT_VIP2_MULT_ANCB_SRC15	INT_STAT_VIP2_MULT_ANCB_SRC14	INT_STAT_VIP2_MULT_ANCB_SRC13	INT_STAT_VIP2_MULT_ANCB_SRC12
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_MULT_ANCB_SRC11	INT_STAT_VIP2_MULT_ANCB_SRC10	INT_STAT_VIP2_MULT_ANCB_SRC9	INT_STAT_VIP2_MULT_ANCB_SRC8	INT_STAT_VIP2_MULT_ANCB_SRC7	INT_STAT_VIP2_MULT_ANCB_SRC6	INT_STAT_VIP2_MULT_ANCB_SRC5	INT_STAT_VIP2_MULT_ANCB_SRC4
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-295. VPDMA_int3_channel5_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_TRANSCODE2_CHROMA	W	0h	The last read DMA transaction has occurred for channel transcode2_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans2_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_TRANSCODE2_LUMA	W	0h	The last read DMA transaction has occurred for channel transcode2_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans2_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_TRANSCODE1_CHROMA	W	0h	The last read DMA transaction has occurred for channel transcode1_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans1_chroma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_TRANSCODE1_LUMA	W	0h	The last read DMA transaction has occurred for channel transcode1_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client trans1_luma will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_AUX_IN	W	0h	The last read DMA transaction has occurred for channel aux_in and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client comp_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-295. VPDMA_int3_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	INT_STAT_PIP_FRAME	W	0h	The last read DMA transaction has occurred for channel pip_frame and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client pip_wrbk will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_POST_COMP_WR	W	0h	The last write DMA transaction has completed for channel post_comp_wr. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client hdmi_wrbk_out then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_VBI_SD_VENC	W	0h	The last read DMA transaction has occurred for channel vbi_sd_venc and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client vbi_sdvenc will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	Reserved	R	0h	
22	INT_STAT_NF_LAST_CHROMA	W	0h	The last read DMA transaction has occurred for channel nf_last_chroma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_420_uv_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_NF_LAST_LUMA	W	0h	The last read DMA transaction has occurred for channel nf_last_luma and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_420_y_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_NF_WRITE_CHROMA	W	0h	The last write DMA transaction has completed for channel nf_write_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_NF_WRITE_LUMA	W	0h	The last write DMA transaction has completed for channel nf_write_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_NF_READ	W	0h	The last read DMA transaction has occurred for channel nf_read and the channel is free to be updated for the next transfer. This will fire before the destination has received the data as it will have just been stored in the internal buffer. The client nf_422_in will now accept a new descriptor from the List Manager. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_VIP2_PORTB_RGB	W	0h	The last write DMA transaction has completed for channel vip2_portb_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_lo_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-295. VPDMA_int3_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	INT_STAT_VIP2_PORTA_RGB	W	0h	The last write DMA transaction has completed for channel vip2_porta_rgb. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_up_y then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_VIP2_PORTB_CHROMA	W	0h	The last write DMA transaction has completed for channel vip2_portb_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_VIP2_PORTB_LUMA	W	0h	The last write DMA transaction has completed for channel vip2_portb_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_VIP2_PORTA_CHROMA	W	0h	The last write DMA transaction has completed for channel vip2_porta_chroma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_VIP2_PORTA_LUMA	W	0h	The last write DMA transaction has completed for channel vip2_porta_luma. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_VIP2_MULT_ANCB_SRC15	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src15. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_VIP2_MULT_ANCB_SRC14	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src14. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_MULT_ANCB_SRC13	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src13. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_MULT_ANCB_SRC12	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src12. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_MULT_ANCB_SRC11	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src11. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-295. VPDMA_int3_channel5_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT_STAT_VIP2_MULT_ANCB_SRC10	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src10. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
5	INT_STAT_VIP2_MULT_ANCB_SRC9	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src9. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP2_MULT_ANCB_SRC8	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src8. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP2_MULT_ANCB_SRC7	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src7. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP2_MULT_ANCB_SRC6	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src6. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_VIP2_MULT_ANCB_SRC5	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src5. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_VIP2_MULT_ANCB_SRC4	W	0h	The last write DMA transaction has completed for channel vip2_mult_ancb_src4. All data from the channel has been sent and received by the external memory. If a new channel has not been setup for the client vip2_anc_b then the client will be fully empty at this point. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.84 VPDMA_int3_channel5_int_mask Register (offset = 15Ch) [reset = 0h]

VPDMA_int3_channel5_int_mask is shown in Figure 1-384 and described in Table 1-296.

Figure 1-384. VPDMA_int3_channel5_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_TRANSCODE2_CHROMA	INT_MASK_TRANSCODE2_LUMA	INT_MASK_TRANSCODE1_CHROMA	INT_MASK_TRANSCODE1_LUMA	INT_MASK_AUX_IN	INT_MASK_PIP_FRAME	INT_MASK_POST_COMP_WR	INT_MASK_VBI_SD_VENC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
Reserved	INT_MASK_NF_LAST_CHROMA	INT_MASK_NF_LAST_LUMA	INT_MASK_NF_WRITE_CHROMA	INT_MASK_NF_WRITE_LUMA	INT_MASK_NF_READ	INT_MASK_VIP2_PORTB_RGB	INT_MASK_VIP2_PORTA_RGB
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_VIP2_PORTB_CHROMA	INT_MASK_VIP2_PORTB_LUMA	INT_MASK_VIP2_PORTA_CHROMA	INT_MASK_VIP2_PORTA_LUMA	INT_MASK_VIP2_MULT_ANCB_SRC15	INT_MASK_VIP2_MULT_ANCB_SRC14	INT_MASK_VIP2_MULT_ANCB_SRC13	INT_MASK_VIP2_MULT_ANCB_SRC12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_MULT_ANCB_SRC11	INT_MASK_VIP2_MULT_ANCB_SRC10	INT_MASK_VIP2_MULT_ANCB_SRC9	INT_MASK_VIP2_MULT_ANCB_SRC8	INT_MASK_VIP2_MULT_ANCB_SRC7	INT_MASK_VIP2_MULT_ANCB_SRC6	INT_MASK_VIP2_MULT_ANCB_SRC5	INT_MASK_VIP2_MULT_ANCB_SRC4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-296. VPDMA_int3_channel5_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_TRANSCODE2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_TRANSCODE2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_TRANSCODE1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_TRANSCODE1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_AUX_IN	R/W	0h	The interrupt for Auxilary Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_PIP_FRAME	R/W	0h	The interrupt for PIP Data for the Compositor Frame From Memory should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_POST_COMP_WR	R/W	0h	The interrupt for Post Compositer Writeback to Memory should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_VBI_SD_VENC	R/W	0h	The interrupt for SD Video Encoder VBI Data should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
23	Reserved	R	0h	
22	INT_MASK_NF_LAST_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_NF_LAST_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-296. VPDMA_int3_channel5_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INT_MASK_NF_WRITE_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_NF_WRITE_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_NF_READ	R/W	0h	The interrupt for Noise Filter Input Data 422 Interleaved should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_VIP2_PORTB_RGB	R/W	0h	The interrupt for Video Input 2 Port B RGB Data should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_VIP2_PORTA_RGB	R/W	0h	The interrupt for Video Input 2 Port A RGB Data should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_VIP2_PORTB_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_VIP2_PORTB_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_VIP2_PORTA_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_VIP2_PORTA_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_VIP2_MULT_ANCB_SRC15	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 15 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_VIP2_MULT_ANCB_SRC14	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 14 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_MULT_ANCB_SRC13	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 13 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_MULT_ANCB_SRC12	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 12 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_MULT_ANCB_SRC11	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 11 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_MULT_ANCB_SRC10	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 10 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP2_MULT_ANCB_SRC9	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 9 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP2_MULT_ANCB_SRC8	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 8 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP2_MULT_ANCB_SRC7	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 7 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-296. VPDMA_int3_channel5_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_MASK_VIP2_MULT_ANCB_SRC6	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 6 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_VIP2_MULT_ANCB_SRC5	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 5 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_VIP2_MULT_ANCB_SRC4	R/W	0h	The interrupt for Video Input 2 Port B Ancillary Data Channel 4 should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.85 VPDMA_int3_channel6_int_stat Register (offset = 160h) [reset = 0h]

VPDMA_int3_channel6_int_stat is shown in Figure 1-385 and described in Table 1-297.

Figure 1-385. VPDMA_int3_channel6_int_stat Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved							INT_STAT_OTHER
R-0h							W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

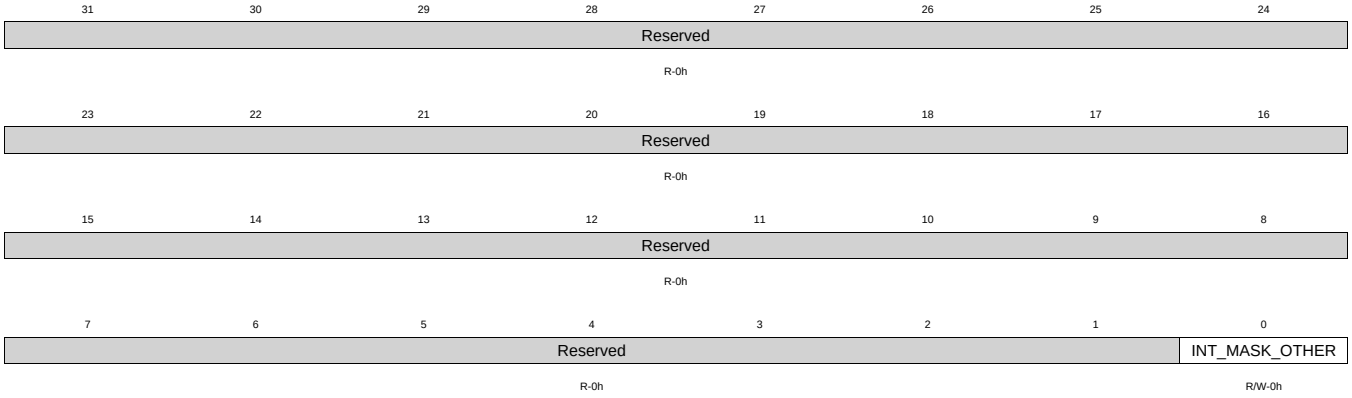
Table 1-297. VPDMA_int3_channel6_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	Reserved	R	0h	
0	INT_STAT_OTHER	W	0h	This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.86 VPDMA_int3_channel6_int_mask Register (offset = 164h) [reset = 0h]

VPDMA_int3_channel6_int_mask is shown in Figure 1-386 and described in Table 1-298.

Figure 1-386. VPDMA_int3_channel6_int_mask Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-298. VPDMA_int3_channel6_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	Reserved	R	0h	
0	INT_MASK_OTHER	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.87 VPDMA_int3_client0_int_stat Register (offset = 168h) [reset = 0h]

VPDMA_int3_client0_int_stat is shown in Figure 1-387 and described in Table 1-299.

Figure 1-387. VPDMA_int3_client0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_GRPX1_DATA	INT_STAT_COMP_WRBK	INT_STAT_SC_OUT	Reserved				
W-0h	W-0h	W-0h	R-0h				
23	22	21	20	19	18	17	16
Reserved			INT_STAT_SC_IN_LUMA	INT_STAT_SC_IN_CHROMA	INT_STAT_PIP_WRBK	INT_STAT_DEI_SC_OUT	Reserved
R-0h			W-0h	W-0h	W-0h	W-0h	R-0h
15	14	13	12	11	10	9	8
INT_STAT_DEI_HQ_MV_OUT	Reserved		INT_STAT_DEI_HQ_MV_IN	Reserved			
W-0h	R-0h		W-0h	R-0h			
7	6	5	4	3	2	1	0
Reserved		INT_STAT_DEI_HQ_3_CHROMA	INT_STAT_DEI_HQ_3_LUMA	INT_STAT_DEI_HQ_2_CHROMA	INT_STAT_DEI_HQ_2_LUMA	INT_STAT_DEI_HQ_1_LUMA	INT_STAT_DEI_HQ_1_CHROMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-299. VPDMA_int3_client0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_GRPX1_DATA	W	0h	The client interface grpx1_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_COMP_WRBK	W	0h	The client interface comp_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_SC_OUT	W	0h	The client interface sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28-21	Reserved	R	0h	
20	INT_STAT_SC_IN_LUMA	W	0h	The client interface sc_in_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_SC_IN_CHROMA	W	0h	The client interface sc_in_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-299. VPDMA_int3_client0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	INT_STAT_PIP_WRBK	W	0h	The client interface pip_wrbk has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_DEI_SC_OUT	W	0h	The client interface dei_sc_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	Reserved	R	0h	
15	INT_STAT_DEI_HQ_MV_OUT	W	0h	The client interface dei_hq_mv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14-13	Reserved	R	0h	
12	INT_STAT_DEI_HQ_MV_IN	W	0h	The client interface dei_hq_mv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11-6	Reserved	R	0h	
5	INT_STAT_DEI_HQ_3_CHROMA	W	0h	The client interface dei_hq_3_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_DEI_HQ_3_LUMA	W	0h	The client interface dei_hq_3_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_DEI_HQ_2_CHROMA	W	0h	The client interface dei_hq_2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_DEI_HQ_2_LUMA	W	0h	The client interface dei_hq_2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-299. VPDMA_int3_client0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_STAT_DEI_HQ_1_LUMA	W	0h	The client interface dei_hq_1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_DEI_HQ_1_CHROMA	W	0h	The client interface dei_hq_1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.88 VPDMA_int3_client0_int_mask Register (offset = 16Ch) [reset = 0h]

VPDMA_int3_client0_int_mask is shown in Figure 1-388 and described in Table 1-300.

Figure 1-388. VPDMA_int3_client0_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_GRPX1_DATA	INT_MASK_COMP_WRBK	INT_MASK_SC_OUT	Reserved				
R/W-0h	R/W-0h	R/W-0h	R-0h				

23	22	21	20	19	18	17	16
Reserved			INT_MASK_SC_IN_LUMA	INT_MASK_SC_IN_CHROMA	INT_MASK_PIP_WRBK	INT_MASK_DEI_SC_OUT	Reserved
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

15	14	13	12	11	10	9	8
INT_MASK_DEI_HQ_MV_OUT	Reserved		INT_MASK_DEI_HQ_MV_IN	Reserved			
R/W-0h	R-0h		R/W-0h	R-0h			

7	6	5	4	3	2	1	0
Reserved		INT_MASK_DEI_HQ_3_CHROMA	INT_MASK_DEI_HQ_3_LUMA	INT_MASK_DEI_HQ_2_CHROMA	INT_MASK_DEI_HQ_2_LUMA	INT_MASK_DEI_HQ_1_LUMA	INT_MASK_DEI_HQ_1_CHROMA
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-300. VPDMA_int3_client0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_GRPX1_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_COMP_WRBK	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_SC_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28-21	Reserved	R	0h	
20	INT_MASK_SC_IN_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_SC_IN_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_PIP_WRBK	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_DEI_SC_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	Reserved	R	0h	
15	INT_MASK_DEI_HQ_MV_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14-13	Reserved	R	0h	
12	INT_MASK_DEI_HQ_MV_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11-6	Reserved	R	0h	

Table 1-300. VPDMA_int3_client0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_MASK_DEI_HQ_3_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_DEI_HQ_3_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_DEI_HQ_2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_DEI_HQ_2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_DEI_HQ_1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_DEI_HQ_1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.89 VPDMA_int3_client1_int_stat Register (offset = 170h) [reset = 0h]

VPDMA_int3_client1_int_stat is shown in Figure 1-389 and described in Table 1-301.

Figure 1-389. VPDMA_int3_client1_int_stat Register

31	30	29	28	27	26	25	24
Reserved		INT_STAT_VIP2_ANC_B	INT_STAT_VIP2_ANC_A	INT_STAT_VIP1_ANC_B	INT_STAT_VIP1_ANC_A	INT_STAT_TRANS2_LUMA	INT_STAT_TRANS2_CHROMA
R-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_TRANS1_LUMA	INT_STAT_TRANS1_CHROMA	INT_STAT_HDMI_WRBK_OUT	INT_STAT_VPI_CTL	INT_STAT_VBI_SDVENC	Reserved	INT_STAT_NF_420_UV_OUT	INT_STAT_NF_420_Y_OUT
W-0h	W-0h	W-0h	W-0h	W-0h	R-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_NF_420_UV_IN	INT_STAT_NF_420_Y_IN	INT_STAT_NF_422_IN	INT_STAT_GRPX3_ST	INT_STAT_GRPX2_ST	INT_STAT_GRPX1_ST	INT_STAT_VIP2_UP_UV	INT_STAT_VIP2_UP_Y
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_VIP2_LO_UV	INT_STAT_VIP2_LO_Y	INT_STAT_VIP1_UP_UV	INT_STAT_VIP1_UP_Y	INT_STAT_VIP1_LO_UV	INT_STAT_VIP1_LO_Y	INT_STAT_GRPX3_DATA	INT_STAT_GRPX2_DATA
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-301. VPDMA_int3_client1_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	INT_STAT_VIP2_ANC_B	W	0h	The client interface vip2_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_VIP2_ANC_A	W	0h	The client interface vip2_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_VIP1_ANC_B	W	0h	The client interface vip1_anc_b has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_VIP1_ANC_A	W	0h	The client interface vip1_anc_a has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_TRANS2_LUMA	W	0h	The client interface trans2_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-301. VPDMA_int3_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	INT_STAT_TRANS2_CHROMA	W	0h	The client interface trans2_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
23	INT_STAT_TRANS1_LUMA	W	0h	The client interface trans1_luma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_TRANS1_CHROMA	W	0h	The client interface trans1_chroma has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_HDMI_WRBK_OUT	W	0h	The client interface hdmi_wrbk_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_VPI_CTL	W	0h	The client interface vpi_ctl has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_VBI_SDVENC	W	0h	The client interface vbi_sdvenc has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	Reserved	R	0h	
17	INT_STAT_NF_420_UV_OUT	W	0h	The client interface nf_420_uv_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_NF_420_Y_OUT	W	0h	The client interface nf_420_y_out has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_NF_420_UV_IN	W	0h	The client interface nf_420_uv_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-301. VPDMA_int3_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	INT_STAT_NF_420_Y_IN	W	0h	The client interface nf_420_y_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_NF_422_IN	W	0h	The client interface nf_422_in has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_GRPX3_ST	W	0h	The client interface grpx3_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_GRPX2_ST	W	0h	The client interface grpx2_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_GRPX1_ST	W	0h	The client interface grpx1_st has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_VIP2_UP_UV	W	0h	The client interface vip2_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
8	INT_STAT_VIP2_UP_Y	W	0h	The client interface vip2_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_VIP2_LO_UV	W	0h	The client interface vip2_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_VIP2_LO_Y	W	0h	The client interface vip2_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-301. VPDMA_int3_client1_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT_STAT_VIP1_UP_UV	W	0h	The client interface vip1_up_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_VIP1_UP_Y	W	0h	The client interface vip1_up_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_VIP1_LO_UV	W	0h	The client interface vip1_lo_uv has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_VIP1_LO_Y	W	0h	The client interface vip1_lo_y has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having received the End of Frame signal from the transmitting module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_GRPX3_DATA	W	0h	The client interface grpx3_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_GRPX2_DATA	W	0h	The client interface grpx2_data has reached its current configured interrupt event as specified by the last received control descriptor for this client. If no control descriptor has been configured this will default to having sent the End of Frame signal to the receiving module. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.90 VPDMA_int3_client1_int_mask Register (offset = 174h) [reset = 0h]

VPDMA_int3_client1_int_mask is shown in Figure 1-390 and described in Table 1-302.

Figure 1-390. VPDMA_int3_client1_int_mask Register

31	30	29	28	27	26	25	24
Reserved		INT_MASK_VIP2_ANC_B	INT_MASK_VIP2_ANC_A	INT_MASK_VIP1_ANC_B	INT_MASK_VIP1_ANC_A	INT_MASK_TRANS2_LUMA	INT_MASK_TRANS2_CHROMA
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_TRANS1_LUMA	INT_MASK_TRANS1_CHROMA	INT_MASK_HDMI_WRBK_OUT	INT_MASK_VPI_CTL	INT_MASK_VBI_SDVENC	Reserved	INT_MASK_NF_420_UV_OUT	INT_MASK_NF_420_Y_OUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_NF_420_UV_IN	INT_MASK_NF_420_Y_IN	INT_MASK_NF_422_IN	INT_MASK_GRPX3_ST	INT_MASK_GRPX2_ST	INT_MASK_GRPX1_ST	INT_MASK_VIP2_UP_UV	INT_MASK_VIP2_UP_Y
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_VIP2_LO_UV	INT_MASK_VIP2_LO_Y	INT_MASK_VIP1_UP_UV	INT_MASK_VIP1_UP_Y	INT_MASK_VIP1_LO_UV	INT_MASK_VIP1_LO_Y	INT_MASK_GRPX3_DATA	INT_MASK_GRPX2_DATA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-302. VPDMA_int3_client1_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	INT_MASK_VIP2_ANC_B	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_VIP2_ANC_A	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_VIP1_ANC_B	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_VIP1_ANC_A	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_TRANS2_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_TRANS2_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_TRANS1_LUMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_TRANS1_CHROMA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
21	INT_MASK_HDMI_WRBK_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
20	INT_MASK_VPI_CTL	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-302. VPDMA_int3_client1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	INT_MASK_VBI_SDVENC	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	Reserved	R	0h	
17	INT_MASK_NF_420_UV_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_NF_420_Y_OUT	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_NF_420_UV_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_NF_420_Y_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_NF_422_IN	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_GRPX3_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_GRPX2_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_GRPX1_ST	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_VIP2_UP_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_VIP2_UP_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_VIP2_LO_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_VIP2_LO_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_VIP1_UP_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_VIP1_UP_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
3	INT_MASK_VIP1_LO_UV	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_VIP1_LO_Y	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_GRPX3_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-302. VPDMA_int3_client1_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT_MASK_GRPX2_DATA	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.91 VPDMA_int3_list0_int_stat Register (offset = 178h) [reset = 0h]

VPDMA_int3_list0_int_stat is shown in Figure 1-391 and described in Table 1-303.

Figure 1-391. VPDMA_int3_list0_int_stat Register

31	30	29	28	27	26	25	24
INT_STAT_CONTROL_DESCRIPTOR_INT15	INT_STAT_CONTROL_DESCRIPTOR_INT14	INT_STAT_CONTROL_DESCRIPTOR_INT13	INT_STAT_CONTROL_DESCRIPTOR_INT12	INT_STAT_CONTROL_DESCRIPTOR_INT11	INT_STAT_CONTROL_DESCRIPTOR_INT10	INT_STAT_CONTROL_DESCRIPTOR_INT9	INT_STAT_CONTROL_DESCRIPTOR_INT8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
INT_STAT_CONTROL_DESCRIPTOR_INT7	INT_STAT_CONTROL_DESCRIPTOR_INT6	INT_STAT_CONTROL_DESCRIPTOR_INT5	INT_STAT_CONTROL_DESCRIPTOR_INT4	INT_STAT_CONTROL_DESCRIPTOR_INT3	INT_STAT_CONTROL_DESCRIPTOR_INT2	INT_STAT_CONTROL_DESCRIPTOR_INT1	INT_STAT_CONTROL_DESCRIPTOR_INT0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
INT_STAT_LIST7_NOTIFY	INT_STAT_LIST7_COMPLETE	INT_STAT_LIST6_NOTIFY	INT_STAT_LIST6_COMPLETE	INT_STAT_LIST5_NOTIFY	INT_STAT_LIST5_COMPLETE	INT_STAT_LIST4_NOTIFY	INT_STAT_LIST4_COMPLETE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
INT_STAT_LIST3_NOTIFY	INT_STAT_LIST3_COMPLETE	INT_STAT_LIST2_NOTIFY	INT_STAT_LIST2_COMPLETE	INT_STAT_LIST1_NOTIFY	INT_STAT_LIST1_COMPLETE	INT_STAT_LIST0_NOTIFY	INT_STAT_LIST0_COMPLETE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-303. VPDMA_int3_list0_int_stat Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_STAT_CONTROL_DESCRIPTOR_INT15	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 15. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
30	INT_STAT_CONTROL_DESCRIPTOR_INT14	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 14. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
29	INT_STAT_CONTROL_DESCRIPTOR_INT13	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 13. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
28	INT_STAT_CONTROL_DESCRIPTOR_INT12	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 12. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
27	INT_STAT_CONTROL_DESCRIPTOR_INT11	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 11. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
26	INT_STAT_CONTROL_DESCRIPTOR_INT10	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 10. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
25	INT_STAT_CONTROL_DESCRIPTOR_INT9	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 9. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
24	INT_STAT_CONTROL_DESCRIPTOR_INT8	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 8. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-303. VPDMA_int3_list0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	INT_STAT_CONTROL_DESCRIPTOR_INT7	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 7. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
22	INT_STAT_CONTROL_DESCRIPTOR_INT6	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 6. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
21	INT_STAT_CONTROL_DESCRIPTOR_INT5	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 5. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
20	INT_STAT_CONTROL_DESCRIPTOR_INT4	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 4. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
19	INT_STAT_CONTROL_DESCRIPTOR_INT3	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 3. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
18	INT_STAT_CONTROL_DESCRIPTOR_INT2	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 2. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
17	INT_STAT_CONTROL_DESCRIPTOR_INT1	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 1. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
16	INT_STAT_CONTROL_DESCRIPTOR_INT0	W	0h	A Send Interrupt Control Descriptor has been received by the list manager with a source value of 0. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
15	INT_STAT_LIST7_NOTIFY	W	0h	A channel set by List 7 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
14	INT_STAT_LIST7_COMPLETE	W	0h	List 7 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
13	INT_STAT_LIST6_NOTIFY	W	0h	A channel set by List 6 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
12	INT_STAT_LIST6_COMPLETE	W	0h	List 6 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
11	INT_STAT_LIST5_NOTIFY	W	0h	A channel set by List 5 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
10	INT_STAT_LIST5_COMPLETE	W	0h	List 5 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
9	INT_STAT_LIST4_NOTIFY	W	0h	A channel set by List 4 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

Table 1-303. VPDMA_int3_list0_int_stat Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT_STAT_LIST4_COMPLETE	W	0h	List 4 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
7	INT_STAT_LIST3_NOTIFY	W	0h	A channel set by List 3 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
6	INT_STAT_LIST3_COMPLETE	W	0h	List 3 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
5	INT_STAT_LIST2_NOTIFY	W	0h	A channel set by List 2 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
4	INT_STAT_LIST2_COMPLETE	W	0h	List 2 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
3	INT_STAT_LIST1_NOTIFY	W	0h	A channel set by List 1 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
2	INT_STAT_LIST1_COMPLETE	W	0h	List 1 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
1	INT_STAT_LIST0_NOTIFY	W	0h	A channel set by List 0 has completed and the Notify bit had been set in the descriptor for that channel. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.
0	INT_STAT_LIST0_COMPLETE	W	0h	List 0 has completed and a new list can be loaded. This event will cause a one to be set in this register until cleared by software. Write a 1 to this field to clear the value.

1.3.8.92 VPDMA_int3_list0_int_mask Register (offset = 17Ch) [reset = 0h]

VPDMA_int3_list0_int_mask is shown in Figure 1-392 and described in Table 1-304.

Figure 1-392. VPDMA_int3_list0_int_mask Register

31	30	29	28	27	26	25	24
INT_MASK_CONTROL_DESCRIPTOR_INT15	INT_MASK_CONTROL_DESCRIPTOR_INT14	INT_MASK_CONTROL_DESCRIPTOR_INT13	INT_MASK_CONTROL_DESCRIPTOR_INT12	INT_MASK_CONTROL_DESCRIPTOR_INT11	INT_MASK_CONTROL_DESCRIPTOR_INT10	INT_MASK_CONTROL_DESCRIPTOR_INT9	INT_MASK_CONTROL_DESCRIPTOR_INT8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INT_MASK_CONTROL_DESCRIPTOR_INT7	INT_MASK_CONTROL_DESCRIPTOR_INT6	INT_MASK_CONTROL_DESCRIPTOR_INT5	INT_MASK_CONTROL_DESCRIPTOR_INT4	INT_MASK_CONTROL_DESCRIPTOR_INT3	INT_MASK_CONTROL_DESCRIPTOR_INT2	INT_MASK_CONTROL_DESCRIPTOR_INT1	INT_MASK_CONTROL_DESCRIPTOR_INT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INT_MASK_LIST7_NOTIFY	INT_MASK_LIST7_COMPLETE	INT_MASK_LIST6_NOTIFY	INT_MASK_LIST6_COMPLETE	INT_MASK_LIST5_NOTIFY	INT_MASK_LIST5_COMPLETE	INT_MASK_LIST4_NOTIFY	INT_MASK_LIST4_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT_MASK_LIST3_NOTIFY	INT_MASK_LIST3_COMPLETE	INT_MASK_LIST2_NOTIFY	INT_MASK_LIST2_COMPLETE	INT_MASK_LIST1_NOTIFY	INT_MASK_LIST1_COMPLETE	INT_MASK_LIST0_NOTIFY	INT_MASK_LIST0_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-304. VPDMA_int3_list0_int_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_MASK_CONTROL_DESCRIPTOR_INT15	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
30	INT_MASK_CONTROL_DESCRIPTOR_INT14	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
29	INT_MASK_CONTROL_DESCRIPTOR_INT13	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
28	INT_MASK_CONTROL_DESCRIPTOR_INT12	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
27	INT_MASK_CONTROL_DESCRIPTOR_INT11	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
26	INT_MASK_CONTROL_DESCRIPTOR_INT10	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
25	INT_MASK_CONTROL_DESCRIPTOR_INT9	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
24	INT_MASK_CONTROL_DESCRIPTOR_INT8	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
23	INT_MASK_CONTROL_DESCRIPTOR_INT7	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
22	INT_MASK_CONTROL_DESCRIPTOR_INT6	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-304. VPDMA_int3_list0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	INT_MASK_CONTROL_DESCRIPTOR_INT5	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
20	INT_MASK_CONTROL_DESCRIPTOR_INT4	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
19	INT_MASK_CONTROL_DESCRIPTOR_INT3	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
18	INT_MASK_CONTROL_DESCRIPTOR_INT2	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
17	INT_MASK_CONTROL_DESCRIPTOR_INT1	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
16	INT_MASK_CONTROL_DESCRIPTOR_INT0	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
15	INT_MASK_LIST7_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
14	INT_MASK_LIST7_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
13	INT_MASK_LIST6_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
12	INT_MASK_LIST6_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
11	INT_MASK_LIST5_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
10	INT_MASK_LIST5_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
9	INT_MASK_LIST4_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
8	INT_MASK_LIST4_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
7	INT_MASK_LIST3_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
6	INT_MASK_LIST3_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
5	INT_MASK_LIST2_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
4	INT_MASK_LIST2_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

Table 1-304. VPDMA_int3_list0_int_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INT_MASK_LIST1_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
2	INT_MASK_LIST1_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
1	INT_MASK_LIST0_NOTIFY	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.
0	INT_MASK_LIST0_COMPLETE	R/W	0h	The interrupt for should generate an interrupt on interrupt vpdma_int3. Write a 1 for the interrupt event to trigger the interrupt signal.

1.3.8.93 VPDMA_dei_hq_1_chroma_cstat Register (offset = 300h) [reset = 0h]

VPDMA_dei_hq_1_chroma_cstat is shown in Figure 1-393 and described in Table 1-305.

Figure 1-393. VPDMA_dei_hq_1_chroma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				LINE_MODE	
R-0h	R-0h	R/W-0h				R/W-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-305. VPDMA_dei_hq_1_chroma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-8	LINE_MODE	R/W	0h	Selects the output mode of the line buffer. 0: repeat lines twice each output data line gets 2 times the number of frame lines. 1: each line once with Line Buffer Disabled.. so no mirroring. Each line gets frame lines with identical data. 2: Each line seen once Mirroring is enabled so the top lines get the top lines repeated at the top of the frame and the bottom lines have the bottom lines repeated. Each line of data gets frame lines + number of buffered lines. 3: each line once only on one line. Each data line gets number of frame lines divided by number of buffered lines.
7-0	Reserved	R	0h	

1.3.8.94 VPDMA_dei_hq_1_luma_cstat Register (offset = 304h) [reset = 0h]

VPDMA_dei_hq_1_luma_cstat is shown in Figure 1-394 and described in Table 1-306.

Figure 1-394. VPDMA_dei_hq_1_luma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-306. VPDMA_dei_hq_1_luma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.95 VPDMA_dei_hq_2_luma_cstat Register (offset = 308h) [reset = 0h]

VPDMA_dei_hq_2_luma_cstat is shown in Figure 1-395 and described in Table 1-307.

Figure 1-395. VPDMA_dei_hq_2_luma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-307. VPDMA_dei_hq_2_luma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.96 VPDMA_dei_hq_2_chroma_cstat Register (offset = 30Ch) [reset = 0h]

VPDMA_dei_hq_2_chroma_cstat is shown in Figure 1-396 and described in Table 1-308.

Figure 1-396. VPDMA_dei_hq_2_chroma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				LINE_MODE	
R-0h	R-0h	R/W-0h				R/W-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-308. VPDMA_dei_hq_2_chroma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-8	LINE_MODE	R/W	0h	Selects the output mode of the line buffer. 0: repeat lines twice each output data line gets 2 times the number of frame lines. 1: each line once with Line Buffer Disabled.. so no mirroring. Each line gets frame lines with identical data. 2: Each line seen once Mirroring is enabled so the top lines get the top lines repeated at the top of the frame and the bottom lines have the bottom lines repeated. Each line of data gets frame lines + number of buffered lines. 3: each line once only on one line. Each data line gets number of frame lines divided by number of buffered lines.
7-0	Reserved	R	0h	

1.3.8.97 VPDMA_dei_hq_3_luma_cstat Register (offset = 310h) [reset = 0h]

VPDMA_dei_hq_3_luma_cstat is shown in Figure 1-397 and described in Table 1-309.

Figure 1-397. VPDMA_dei_hq_3_luma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-309. VPDMA_dei_hq_3_luma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.98 VPDMA_dei_hq_3_chroma_cstat Register (offset = 314h) [reset = 0h]

VPDMA_dei_hq_3_chroma_cstat is shown in Figure 1-398 and described in Table 1-310.

Figure 1-398. VPDMA_dei_hq_3_chroma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				LINE_MODE	
R-0h	R-0h	R/W-0h				R/W-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-310. VPDMA_dei_hq_3_chroma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-8	LINE_MODE	R/W	0h	Selects the output mode of the line buffer. 0: repeat lines twice each output data line gets 2 times the number of frame lines. 1: each line once with Line Buffer Disabled.. so no mirroring. Each line gets frame lines with identical data. 2: Each line seen once Mirroring is enabled so the top lines get the top lines repeated at the top of the frame and the bottom lines have the bottom lines repeated. Each line of data gets frame lines + number of buffered lines. 3: each line once only on one line. Each data line gets number of frame lines divided by number of buffered lines.
7-0	Reserved	R	0h	

1.3.8.99 VPDMA_dei_hq_mv_in_cstat Register (offset = 330h) [reset = 0h]

VPDMA_dei_hq_mv_in_cstat is shown in Figure 1-399 and described in Table 1-311.

Figure 1-399. VPDMA_dei_hq_mv_in_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-311. VPDMA_dei_hq_mv_in_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.100 VPDMA_dei_hq_mv_out_cstat Register (offset = 33Ch) [reset = 0h]

VPDMA_dei_hq_mv_out_cstat is shown in Figure 1-400 and described in Table 1-312.

Figure 1-400. VPDMA_dei_hq_mv_out_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-312. VPDMA_dei_hq_mv_out_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.101 VPDMA_dei_sc_out_cstat Register (offset = 344h) [reset = 0h]

VPDMA_dei_sc_out_cstat is shown in Figure 1-401 and described in Table 1-313.

Figure 1-401. VPDMA_dei_sc_out_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

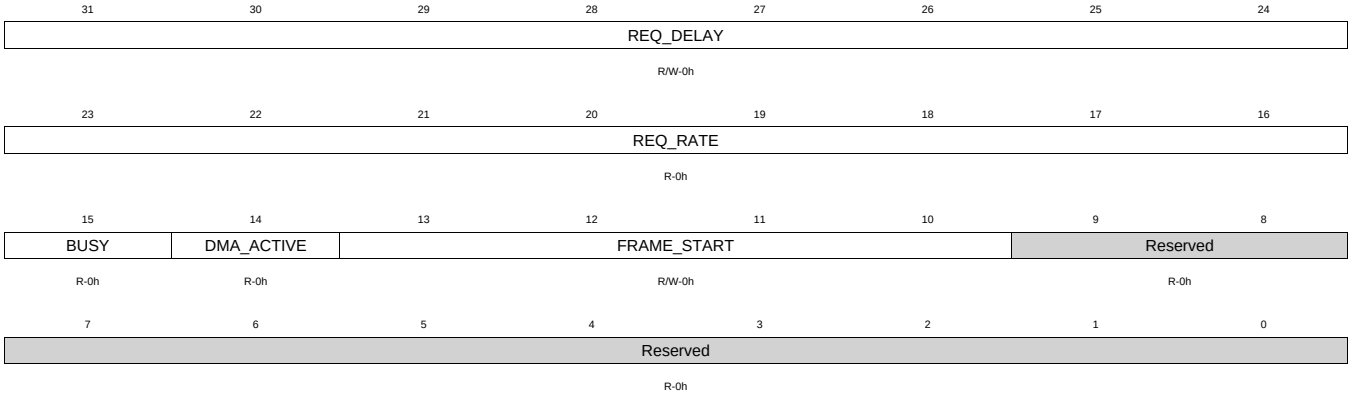
Table 1-313. VPDMA_dei_sc_out_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.102 VPDMA_pip_wrbk_cstat Register (offset = 348h) [reset = 0h]

VPDMA_pip_wrbk_cstat is shown in Figure 1-402 and described in Table 1-314.

Figure 1-402. VPDMA_pip_wrbk_cstat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-314. VPDMA_pip_wrbk_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.103 VPDMA_sc_in_chroma_cstat Register (offset = 34Ch) [reset = 0h]

VPDMA_sc_in_chroma_cstat is shown in Figure 1-403 and described in Table 1-315.

Figure 1-403. VPDMA_sc_in_chroma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				LINE_MODE	
R-0h	R-0h	R/W-0h				R/W-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

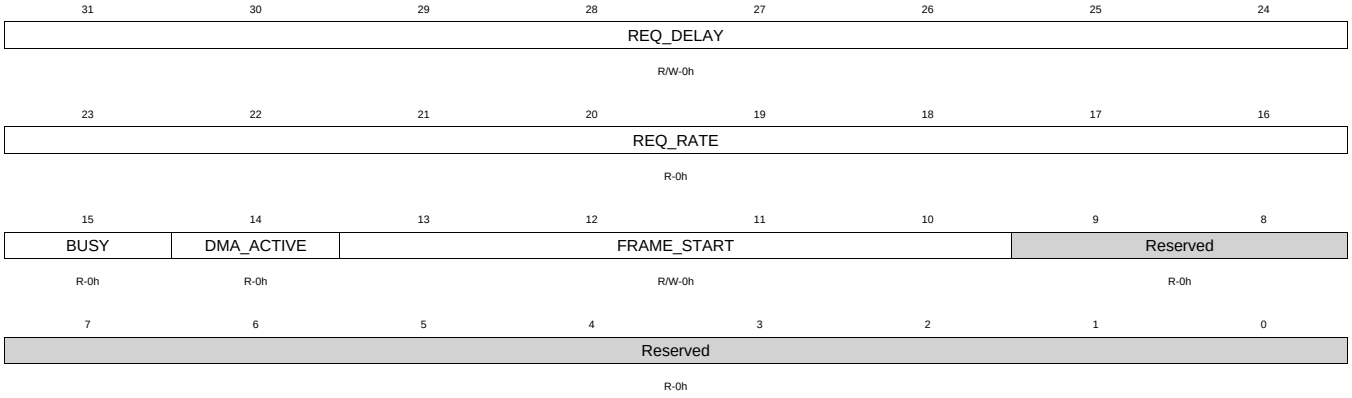
Table 1-315. VPDMA_sc_in_chroma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-8	LINE_MODE	R/W	0h	Selects the output mode of the line buffer. 0 = repeat lines twice each output data line gets 2 times the number of frame lines. 1 = each line once with Line Buffer Disabled, so no mirroring. Each line gets frame lines with identical data. 2 = Each line seen once Mirroring is enabled so the top lines get the top lines repeated at the top of the frame and the bottom lines have the bottom lines repeated. Each line of data gets frame lines + number of buffered lines. 3 = each line once only on one line. Each data line gets number of frame lines divided by number of buffered lines.
7-0	Reserved	R	0h	

1.3.8.104 VPDMA_sc_in_luma_cstat Register (offset = 350h) [reset = 0h]

VPDMA_sc_in_luma_cstat is shown in Figure 1-404 and described in Table 1-316.

Figure 1-404. VPDMA_sc_in_luma_cstat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-316. VPDMA_sc_in_luma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.105 VPDMA_sc_out_cstat Register (offset = 374h) [reset = 0h]

VPDMA_sc_out_cstat is shown in Figure 1-405 and described in Table 1-317.

Figure 1-405. VPDMA_sc_out_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-317. VPDMA_sc_out_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.106 VPDMA_comp_wrbk_cstat Register (offset = 378h) [reset = 0h]

VPDMA_comp_wrbk_cstat is shown in Figure 1-406 and described in Table 1-318.

Figure 1-406. VPDMA_comp_wrbk_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-318. VPDMA_comp_wrbk_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.107 VPDMA_grpx1_data_cstat Register (offset = 37Ch) [reset = 0h]

VPDMA_grpx1_data_cstat is shown in Figure 1-407 and described in Table 1-319.

Figure 1-407. VPDMA_grpx1_data_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-319. VPDMA_grpx1_data_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.108 VPDMA_grpx2_data_cstat Register (offset = 380h) [reset = 0h]

VPDMA_grpx2_data_cstat is shown in Figure 1-408 and described in Table 1-320.

Figure 1-408. VPDMA_grpx2_data_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-320. VPDMA_grpx2_data_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.109 VPDMA_grpx3_data_cstat Register (offset = 384h) [reset = 0h]

VPDMA_grpx3_data_cstat is shown in Figure 1-409 and described in Table 1-321.

Figure 1-409. VPDMA_grpx3_data_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

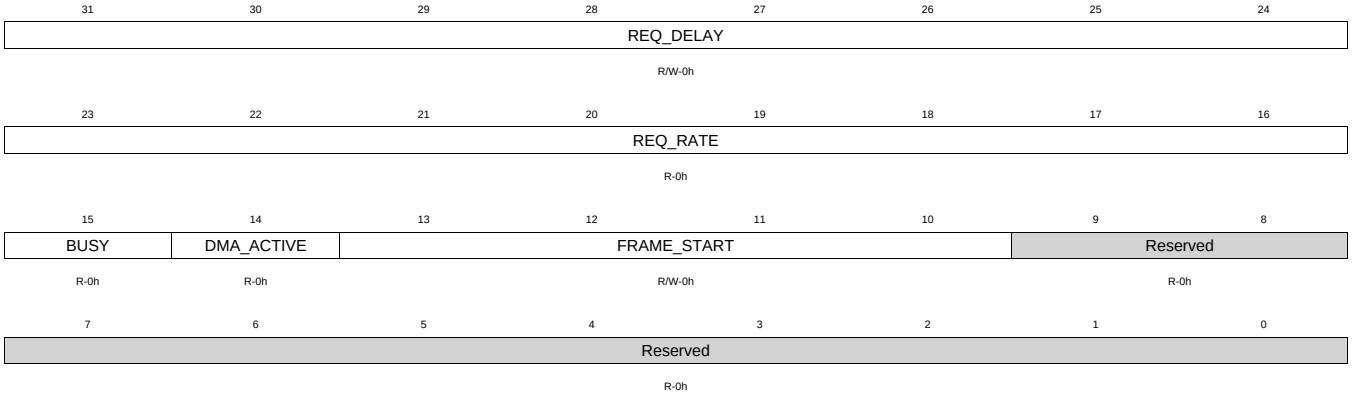
Table 1-321. VPDMA_grpx3_data_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.110 VPDMA_vip1_lo_y_cstat Register (offset = 388h) [reset = 0h]

VPDMA_vip1_lo_y_cstat is shown in Figure 1-410 and described in Table 1-322.

Figure 1-410. VPDMA_vip1_lo_y_cstat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-322. VPDMA_vip1_lo_y_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.111 VPDMA_vip1_lo_uv_cstat Register (offset = 38Ch) [reset = 0h]

VPDMA_vip1_lo_uv_cstat is shown in Figure 1-411 and described in Table 1-323.

Figure 1-411. VPDMA_vip1_lo_uv_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

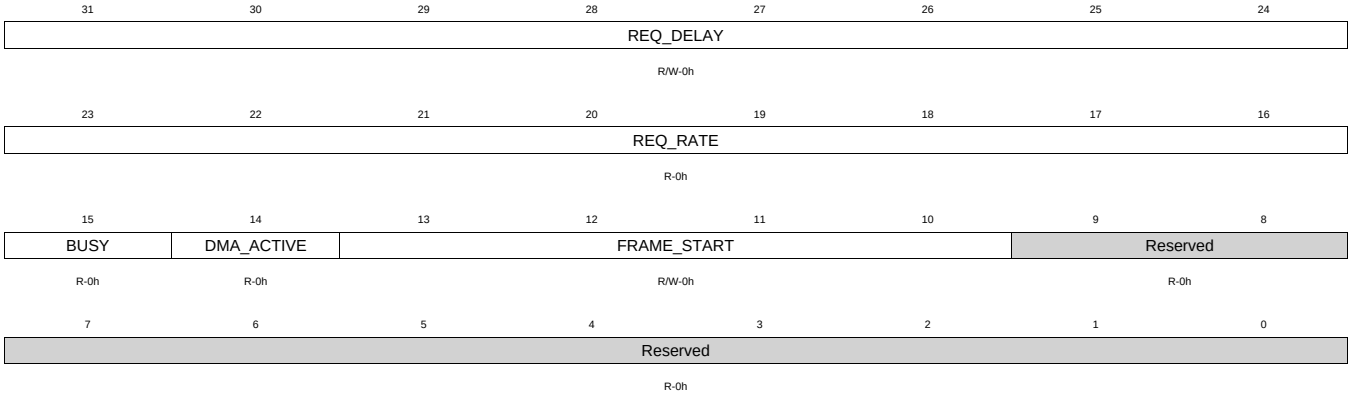
Table 1-323. VPDMA_vip1_lo_uv_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.112 VPDMA_vip1_up_y_cstat Register (offset = 390h) [reset = 0h]

VPDMA_vip1_up_y_cstat is shown in Figure 1-412 and described in Table 1-324.

Figure 1-412. VPDMA_vip1_up_y_cstat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

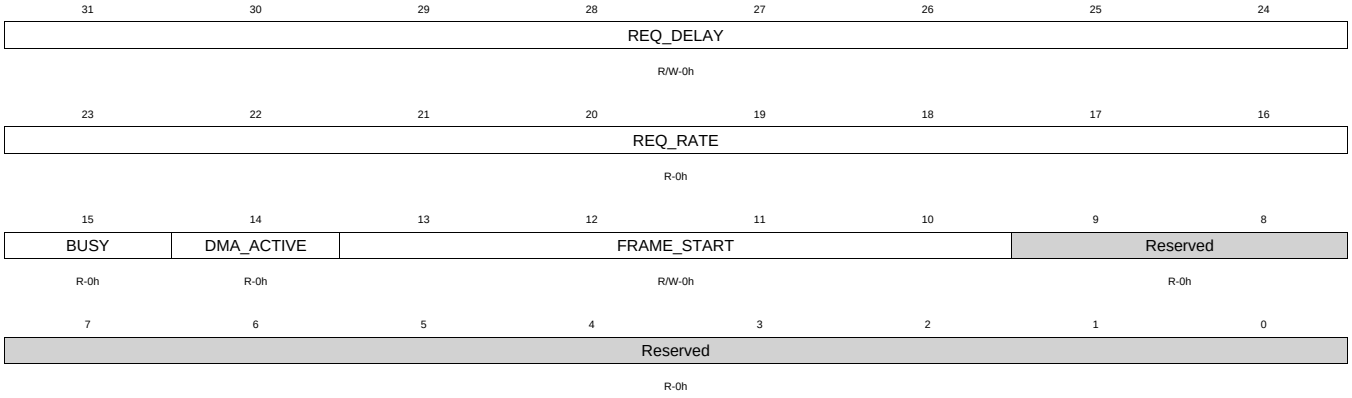
Table 1-324. VPDMA_vip1_up_y_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.113 VPDMA_vip1_up_uv_cstat Register (offset = 394h) [reset = 0h]

VPDMA_vip1_up_uv_cstat is shown in Figure 1-413 and described in Table 1-325.

Figure 1-413. VPDMA_vip1_up_uv_cstat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

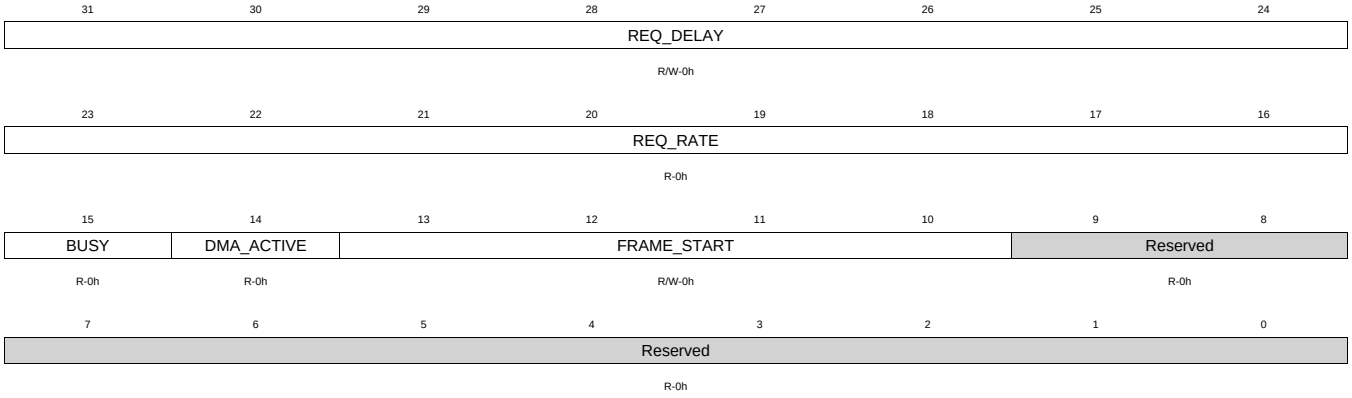
Table 1-325. VPDMA_vip1_up_uv_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.114 VPDMA_vip2_lo_y_cstat Register (offset = 398h) [reset = 0h]

VPDMA_vip2_lo_y_cstat is shown in Figure 1-414 and described in Table 1-326.

Figure 1-414. VPDMA_vip2_lo_y_cstat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-326. VPDMA_vip2_lo_y_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.115 VPDMA_vip2_lo_uv_cstat Register (offset = 39Ch) [reset = 0h]

VPDMA_vip2_lo_uv_cstat is shown in Figure 1-415 and described in Table 1-327.

Figure 1-415. VPDMA_vip2_lo_uv_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-327. VPDMA_vip2_lo_uv_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.116 VPDMA_vip2_up_y_cstat Register (offset = 3A0h) [reset = 0h]

VPDMA_vip2_up_y_cstat is shown in Figure 1-416 and described in Table 1-328.

Figure 1-416. VPDMA_vip2_up_y_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-328. VPDMA_vip2_up_y_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.117 VPDMA_vip2_up_uv_cstat Register (offset = 3A4h) [reset = 0h]

VPDMA_vip2_up_uv_cstat is shown in Figure 1-417 and described in Table 1-329.

Figure 1-417. VPDMA_vip2_up_uv_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-329. VPDMA_vip2_up_uv_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.118 VPDMA_grpx1_st_cstat Register (offset = 3A8h) [reset = 0h]

VPDMA_grpx1_st_cstat is shown in Figure 1-418 and described in Table 1-330.

Figure 1-418. VPDMA_grpx1_st_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-330. VPDMA_grpx1_st_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.119 VPDMA_grpx2_st_cstat Register (offset = 3ACh) [reset = 0h]

VPDMA_grpx2_st_cstat is shown in Figure 1-419 and described in Table 1-331.

Figure 1-419. VPDMA_grpx2_st_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-331. VPDMA_grpx2_st_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.120 VPDMA_grpx3_st_cstat Register (offset = 3B0h) [reset = 0h]

VPDMA_grpx3_st_cstat is shown in Figure 1-420 and described in Table 1-332.

Figure 1-420. VPDMA_grpx3_st_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

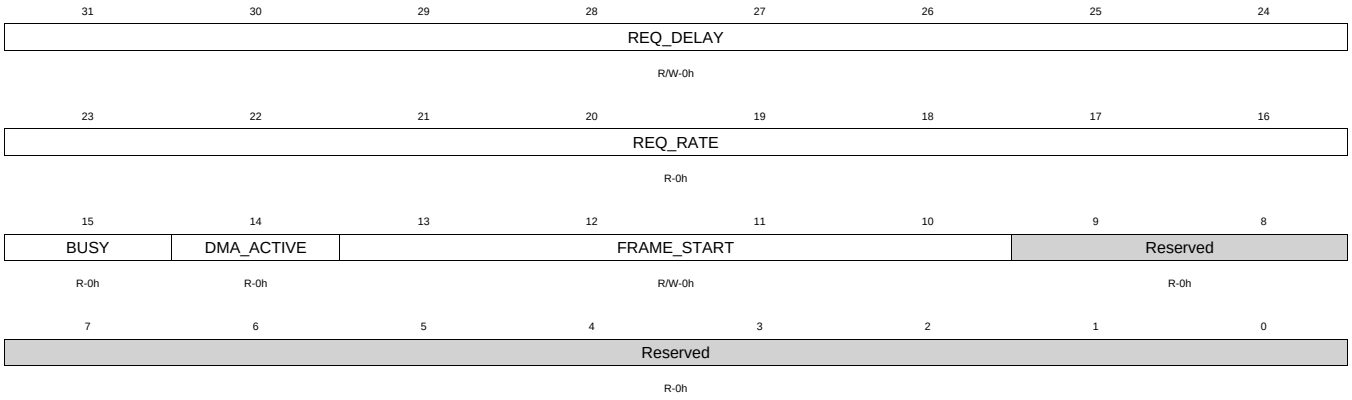
Table 1-332. VPDMA_grpx3_st_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.121 VPDMA_nf_422_in_cstat Register (offset = 3B4h) [reset = 0h]

VPDMA_nf_422_in_cstat is shown in Figure 1-421 and described in Table 1-333.

Figure 1-421. VPDMA_nf_422_in_cstat Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-333. VPDMA_nf_422_in_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.122 VPDMA_nf_420_y_in_cstat Register (offset = 3B8h) [reset = 0h]

VPDMA_nf_420_y_in_cstat is shown in Figure 1-422 and described in Table 1-334.

Figure 1-422. VPDMA_nf_420_y_in_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-334. VPDMA_nf_420_y_in_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.123 VPDMA_nf_420_uv_in_cstat Register (offset = 3BCh) [reset = 0h]

VPDMA_nf_420_uv_in_cstat is shown in Figure 1-423 and described in Table 1-335.

Figure 1-423. VPDMA_nf_420_uv_in_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-335. VPDMA_nf_420_uv_in_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.124 VPDMA_nf_420_y_out_cstat Register (offset = 3C0h) [reset = 0h]

VPDMA_nf_420_y_out_cstat is shown in Figure 1-424 and described in Table 1-336.

Figure 1-424. VPDMA_nf_420_y_out_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-336. VPDMA_nf_420_y_out_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.125 VPDMA_nf_420_uv_out_cstat Register (offset = 3C4h) [reset = 0h]

VPDMA_nf_420_uv_out_cstat is shown in Figure 1-425 and described in Table 1-337.

Figure 1-425. VPDMA_nf_420_uv_out_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-337. VPDMA_nf_420_uv_out_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.126 VPDMA_vbi_sdvenc_cstat Register (offset = 3CCh) [reset = 0h]

VPDMA_vbi_sdvenc_cstat is shown in Figure 1-426 and described in Table 1-338.

Figure 1-426. VPDMA_vbi_sdvenc_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-338. VPDMA_vbi_sdvenc_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.127 VPDMA_vpi_ctl_cstat Register (offset = 3D0h) [reset = 0h]

VPDMA_vpi_ctl_cstat is shown in Figure 1-427 and described in Table 1-339.

Figure 1-427. VPDMA_vpi_ctl_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-339. VPDMA_vpi_ctl_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.128 VPDMA_hdmi_wrbk_out_cstat Register (offset = 3D4h) [reset = 0h]

VPDMA_hdmi_wrbk_out_cstat is shown in Figure 1-428 and described in Table 1-340.

Figure 1-428. VPDMA_hdmi_wrbk_out_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-340. VPDMA_hdmi_wrbk_out_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.129 VPDMA_trans1_chroma_cstat Register (offset = 3D8h) [reset = 0h]

VPDMA_trans1_chroma_cstat is shown in Figure 1-429 and described in Table 1-341.

Figure 1-429. VPDMA_trans1_chroma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							

23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							

15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				LINE_MODE	
R-0h	R-0h	R/W-0h				R/W-0h	

7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-341. VPDMA_trans1_chroma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-8	LINE_MODE	R/W	0h	Selects the output mode of the line buffer. 0: repeat lines twice each output data line gets 2 times the number of frame lines. 1: each line once with Line Buffer Disabled.. so no mirroring. Each line gets frame lines with identical data. 2: Each line seen once Mirroring is enabled so the top lines get the top lines repeated at the top of the frame and the bottom lines have the bottom lines repeated. Each line of data gets frame lines + number of buffered lines. 3: each line once only on one line. Each data line gets number of frame lines divided by number of buffered lines.
7-0	Reserved	R	0h	

1.3.8.130 VPDMA_trans1_luma_cstat Register (offset = 3DCh) [reset = 0h]

VPDMA_trans1_luma_cstat is shown in Figure 1-430 and described in Table 1-342.

Figure 1-430. VPDMA_trans1_luma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-342. VPDMA_trans1_luma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.131 VPDMA_trans2_chroma_cstat Register (offset = 3E0h) [reset = 0h]

VPDMA_trans2_chroma_cstat is shown in Figure 1-431 and described in Table 1-343.

Figure 1-431. VPDMA_trans2_chroma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				LINE_MODE	
R-0h	R-0h	R/W-0h				R/W-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-343. VPDMA_trans2_chroma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-8	LINE_MODE	R/W	0h	Selects the output mode of the line buffer. 0: repeat lines twice each output data line gets 2 times the number of frame lines. 1: each line once with Line Buffer Disabled.. so no mirroring. Each line gets frame lines with identical data. 2: Each line seen once Mirroring is enabled so the top lines get the top lines repeated at the top of the frame and the bottom lines have the bottom lines repeated. Each line of data gets frame lines + number of buffered lines. 3: each line once only on one line. Each data line gets number of frame lines divided by number of buffered lines.
7-0	Reserved	R	0h	

1.3.8.132 VPDMA_trans2_luma_cstat Register (offset = 3E4h) [reset = 0h]

VPDMA_trans2_luma_cstat is shown in Figure 1-432 and described in Table 1-344.

Figure 1-432. VPDMA_trans2_luma_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-344. VPDMA_trans2_luma_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.133 VPDMA_vip1_anc_a_cstat Register (offset = 3E8h) [reset = 0h]

VPDMA_vip1_anc_a_cstat is shown in Figure 1-433 and described in Table 1-345.

Figure 1-433. VPDMA_vip1_anc_a_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-345. VPDMA_vip1_anc_a_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.134 VPDMA_vip1_anc_b_cstat Register (offset = 3ECh) [reset = 0h]

VPDMA_vip1_anc_b_cstat is shown in Figure 1-434 and described in Table 1-346.

Figure 1-434. VPDMA_vip1_anc_b_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-346. VPDMA_vip1_anc_b_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.135 VPDMA_vip2_anc_a_cstat Register (offset = 3F0h) [reset = 0h]

VPDMA_vip2_anc_a_cstat is shown in Figure 1-435 and described in Table 1-347.

Figure 1-435. VPDMA_vip2_anc_a_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-347. VPDMA_vip2_anc_a_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.8.136 VPDMA_vip2_anc_b_cstat Register (offset = 3F4h) [reset = 0h]

VPDMA_vip2_anc_b_cstat is shown in Figure 1-436 and described in Table 1-348.

Figure 1-436. VPDMA_vip2_anc_b_cstat Register

31	30	29	28	27	26	25	24
REQ_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
REQ_RATE							
R-0h							
15	14	13	12	11	10	9	8
BUSY	DMA_ACTIVE	FRAME_START				Reserved	
R-0h	R-0h	R/W-0h				R-0h	
7	6	5	4	3	2	1	0
Reserved							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-348. VPDMA_vip2_anc_b_cstat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	REQ_DELAY	R/W	0h	The minimum number of clock cycles between requests being issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins and the first request of a frame will go as soon as possible.
23-16	REQ_RATE	R	0h	The number of clock cycles between the last two requests issued. This value is multiplied by 32 to get the actual number of cycles.This value is only accurate for the current frame. The internal counters used to calculate the rate are reset when a new frame begins.
15	BUSY	R	0h	Signals if the client is currently active. This bit is set as soon as we the channel is received by the client from the list manager and is cleared when the channel is cleared from the shared memory.
14	DMA_ACTIVE	R	0h	Signals if the client is currently actively sending DMA requests
13-10	FRAME_START	R/W	0h	The source of the start frame event for the client. 0 = Change in hdmi_field_id 1 = Change in dvo2_field_id 2 = RESERVED 3 = Change in value of sd_field_id 4 = Change in value of List Manager Internal Field - 0 5 = Change in value of List Manager Internal Field - 1 6 = Change in value of List Manager Internal Field - 2 7 = Start whenever channel is free
9-0	Reserved	R	0h	

1.3.9 HD_VENC_D Registers

Table 1-349 lists the memory-mapped registers for the HD_VENC_D. All register offset addresses not listed in Table 1-349 should be considered as reserved locations and the register contents should not be modified.

Table 1-349. HD_VENC_D REGISTERS

Offset	Acronym	Register Name	Section
0h	HD_VENC_D_cfg0	VENC Mode Register	Section 1.3.9.1
4h	HD_VENC_D_cfg1	Color Space Converter Coefficient Register	Section 1.3.9.2
8h	HD_VENC_D_cfg2	Color Space Converter Coefficient Register	Section 1.3.9.3
Ch	HD_VENC_D_cfg3	Color Space Converter Coefficient Register	Section 1.3.9.4
10h	HD_VENC_D_cfg4	Color Space Converter Coefficient Register	Section 1.3.9.5
14h	HD_VENC_D_cfg5	Color Space Converter Coefficient Register	Section 1.3.9.6
18h	HD_VENC_D_cfg6	Color Space Converter Coefficient Register	Section 1.3.9.7
1Ch	HD_VENC_D_cfg7	Reserved Register	Section 1.3.9.8
20h	HD_VENC_D_cfg8	Reserved Register	Section 1.3.9.9
24h	HD_VENC_D_cfg9	Reserved Register	Section 1.3.9.10
28h	HD_VENC_D_cfg10	Frame Size Register	Section 1.3.9.11
2Ch	HD_VENC_D_cfg11	Reserved Register	Section 1.3.9.12
30h	HD_VENC_D_cfg12	Active Pixels per Line Register	Section 1.3.9.13
34h	HD_VENC_D_cfg13	VENC Control Register	Section 1.3.9.14
38h	HD_VENC_D_cfg14	Reserved Register	Section 1.3.9.15
3Ch	HD_VENC_D_cfg15	DVO Control Register	Section 1.3.9.16
40h	HD_VENC_D_cfg16	DVO Control Register	Section 1.3.9.17
44h	HD_VENC_D_cfg17	DVO Control Register	Section 1.3.9.18
48h	HD_VENC_D_cfg18	DVO Control Register	Section 1.3.9.19
4Ch	HD_VENC_D_cfg19	DVO Control Register	Section 1.3.9.20
50h	HD_VENC_D_cfg20	DVO/Compositor IF Control Register	Section 1.3.9.21
54h	HD_VENC_D_cfg21	Compositor IF Control Register	Section 1.3.9.22
58h	HD_VENC_D_cfg22	Compositor IF Control Register	Section 1.3.9.23
5Ch	HD_VENC_D_cfg23	Compositor IF Control Register	Section 1.3.9.24
60h	HD_VENC_D_cfg24	Compositor IF Control Register	Section 1.3.9.25
64h	HD_VENC_D_cfg25	Compositor IF Control Register	Section 1.3.9.26
1000h-1FFFh	HD_VENC_D_GAMMA_LUT	Gamma Lookup Table	Section 1.3.9.27

1.3.9.1 HD_VENC_D_cfg0 Register (offset = 0h) [reset = 0h]

HD_VENC_D_cfg0 is shown in Figure 1-437 and described in Table 1-350.

VENC Mode Register

Figure 1-437. HD_VENC_D_cfg0 Register

31	30	29	28	27	26	25	24
Reserved	START	JED	Reserved	DVO_OFF	S_422	I_DVO_A	I_DVO_H
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
I_DVO_V	I_DVO_F	IVT_FID	Reserved		DVO_FMT		
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h		
15	14	13	12	11	10	9	8
STEST	Reserved	BYPS_GC	Reserved				
R/W-0h	R-0h	R/W-0h	R-0h				
7	6	5	4	3	2	1	0
Reserved		BYPS_CS	Reserved	I_PN	Reserved		
R-0h		R/W-0h	R-0h	R/W-0h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-350. HD_VENC_D_cfg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Reserved	R	0h	Reserved
30	START	R/W	0h	This bit will start the operation of encoder. 0: encoder is in standby mode.. no data and signals will be outputted 1: encoder is in the normal operation mode. During the normal operation, this bit should be kept at 1. Normally software will set the bit whenever the operation needs to be started.
29	JED	R/W	0h	This bit can enable the JEIDA output format 0: DVO will output data in normal format 1: DVO will output data in JEIDA format The JEIDA format is used to interface certain LCD panels. It is used in RGB discrete sync mode only.
28	Reserved	R	0h	Reserved
27	DVO_OFF	R/W	0h	This bit forces the DVO to 0s. 0: for normal operation 1: to force the DVO to 0s
26	S_422	R/W	0h	When the DVO output is in 4:2:2 YCbCr format, this bit controls the CbCr format. 0: The CBCR data is generated by a 444-to422- decimation filter. 1: The CBCR data are captured by every-other pixel. (skip one pixel at a time)
25	I_DVO_A	R/W	0h	This bit controls the polarity of DVO_ACTVID signal. 0: Active High 1: Active Low
24	I_DVO_H	R/W	0h	This bit controls the polarity of DVO_HS signal. 0: Active High 1: Active Low
23	I_DVO_V	R/W	0h	This bit controls the polarity of DVO_VS signal. 0: Active High 1: Active Low

Table 1-350. HD_VENC_D_cfg0 Register Field Descriptions (continued)

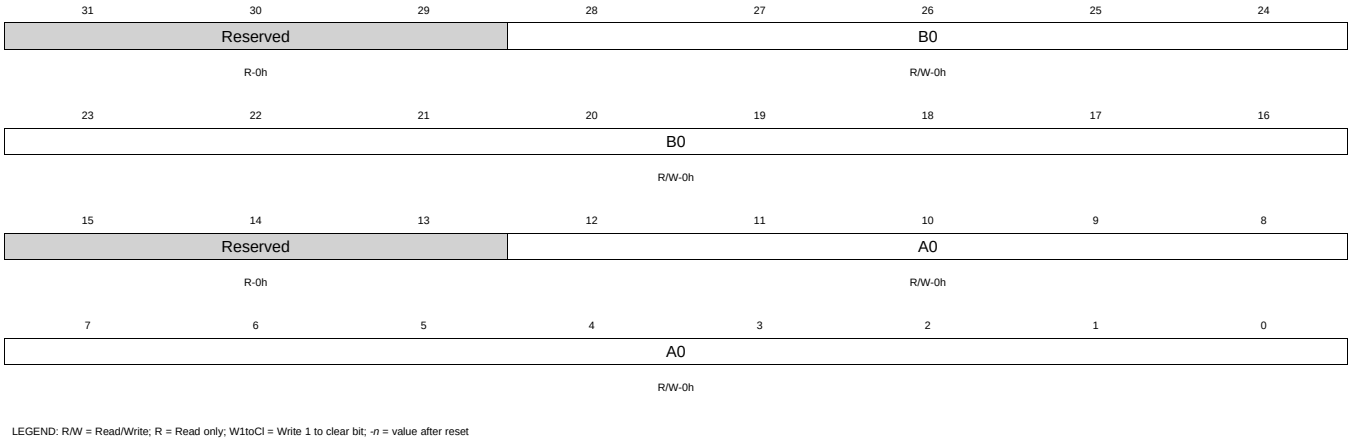
Bit	Field	Type	Reset	Description
22	I_DVO_F	R/W	0h	This bit controls the polarity of DVO_FID signal. 0: Not invert 1: The DVO_FID signal will be inverted
21	IVT_FID	R/W	0h	This bit controls the polarity of DTV_FID signal. 0: Not invert 1: The DTV_FID signal will be inverted
20-19	Reserved	R	0h	Reserved
18-16	DVO_FMT	R/W	0h	These three bits define the format of digital video output port. 000: Single channel 10-bit CCIR656 video stream for SD outputs. The clock rate of the strem is 2X pixel rate. For 480i format, clk2x = 27 MHz. For 480p format, clk2x = 54 MHz. 001: Two channel 10-bit CCIR656 video streams. The video data is in YCbCr 422 format. The data rate equals to the pixel rate. 010: Three channel 10-bit video streams with embedded sync SAV/EAV. The video format can by YCbCr 444 or RGB. And the data rate equals to the pixel rate. 011: Three channel 10-bit video streams with dedicated HS/VS/FID/ACTVID sync signals. The three channel component digital video can be RGB or YCbCr444 format. It can be used for all display formats. And the data rate equals to the pixel rate. 100: Two channel 10-bit video streams with dedicated HS/VS/FID/ACTVID sync signals. The video data format is YCbCr422. The first channel is Y. and CbCr are multiplexed on the second channel. It can be used for all display formats. And the data rate equals to the pixel rate.
15	STEST	R/W	0h	Self test mode: 0: The HD encoder will be in normal operation mode 1: The HD encoder will enter self-test mode. The encoder will generate a 100% color bar internally. The video data from OSD will be ignored.
14	Reserved	R	0h	Reserved
13	BYPS_GC	R/W	0h	Bypass Gamma Correction block: 0 : Apply Gamma-correction to video data 1 : Bypassed Gamma-correction
12-6	Reserved	R	0h	Reserved
5	BYPS_CS	R/W	0h	Bypass color space converter. This means that no color space conversion is needed. If it is not bypassed, the proper coefficient should be set in the corresponding registers. 0 : Color space conversion is engaged 1 : Bypass
4	Reserved	R	0h	Reserved
3	I_PN	R/W	0h	Scan format: 0 : Progressive 1 : Interlace
2-0	Reserved	R	0h	Reserved

1.3.9.2 HD_VENC_D_cfg1 Register (offset = 4h) [reset = 0h]

HD_VENC_D_cfg1 is shown in Figure 1-438 and described in Table 1-351.

Color Space Converter Coefficient Register

Figure 1-438. HD_VENC_D_cfg1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-351. HD_VENC_D_cfg1 Register Field Descriptions

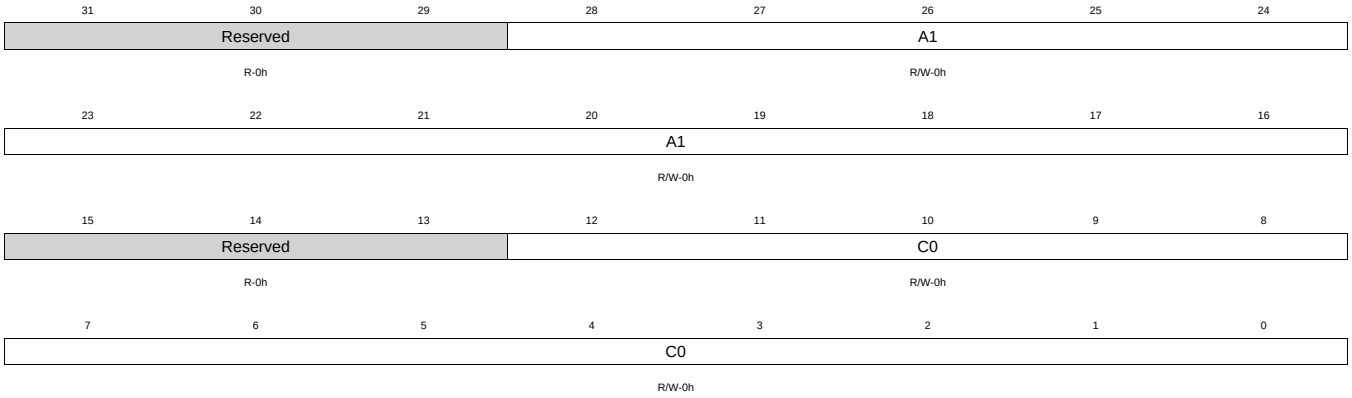
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-16	B0	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in HD_VENC_D_cfg1)
15-13	Reserved	R	0h	Reserved
12-0	A0	R/W	0h	Its is represented as Q3.10 number. So the value ranges from -4 to +4. To convert a decimal number, multiply the number by 1024 and write it in the register in hex format. For example, to program 0.673, 0x2B1 should be written in the register. (round)(0.673 X 1024) = (round)689.152 = 689 = 0x2B1. If the real number is negative, then multiply it by 1024, and convert it to 2's compliment format in 12-bit. For example, if a coefficient is -1.893, 0x186E needs to be written in the register. (round)(-1.893*1024)= -1938 = 0x186E (2'S compliment format of -1938 in 13-bit width)

1.3.9.3 HD_VENC_D_cfg2 Register (offset = 8h) [reset = 0h]

HD_VENC_D_cfg2 is shown in Figure 1-439 and described in Table 1-352.

Color Space Converter Coefficient Register

Figure 1-439. HD_VENC_D_cfg2 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-352. HD_VENC_D_cfg2 Register Field Descriptions

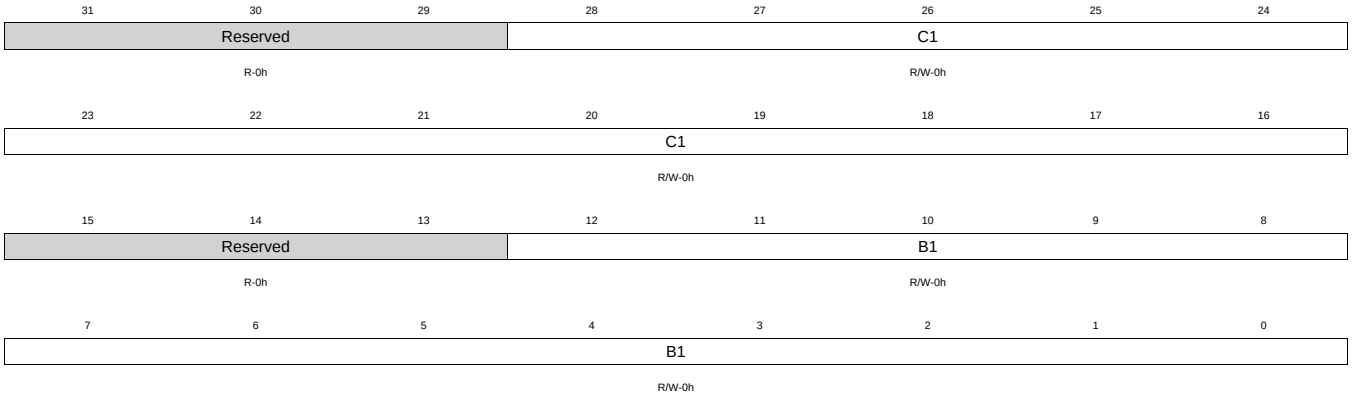
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-16	A1	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in HD_VENC_D_cfg1)
15-13	Reserved	R	0h	Reserved
12-0	C0	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in HD_VENC_D_cfg1)

1.3.9.4 HD_VENC_D_cfg3 Register (offset = Ch) [reset = 0h]

HD_VENC_D_cfg3 is shown in Figure 1-440 and described in Table 1-353.

Color Space Converter Coefficient Register

Figure 1-440. HD_VENC_D_cfg3 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-353. HD_VENC_D_cfg3 Register Field Descriptions

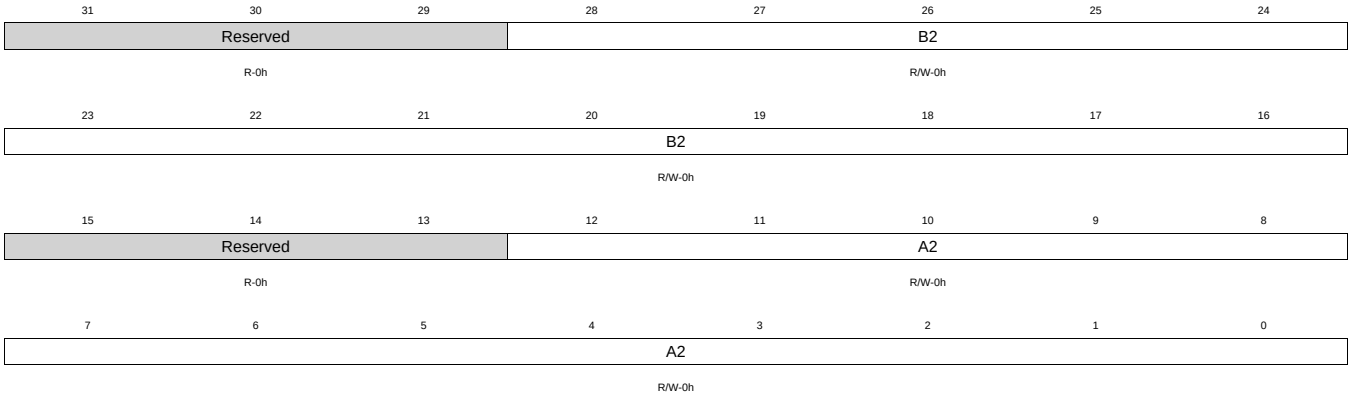
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-16	C1	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in HD_VENC_D_cfg1)
15-13	Reserved	R	0h	Reserved
12-0	B1	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in HD_VENC_D_cfg1)

1.3.9.5 HD_VENC_D_cfg4 Register (offset = 10h) [reset = 0h]

HD_VENC_D_cfg4 is shown in Figure 1-441 and described in Table 1-354.

Color Space Converter Coefficient Register

Figure 1-441. HD_VENC_D_cfg4 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-354. HD_VENC_D_cfg4 Register Field Descriptions

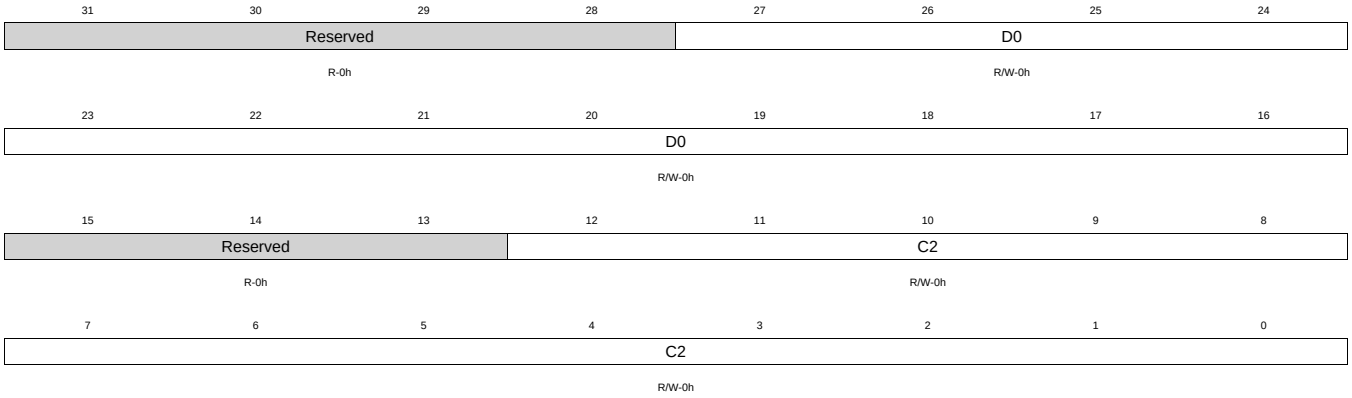
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	Reserved
28-16	B2	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in HD_VENC_D_cfg1)
15-13	Reserved	R	0h	Reserved
12-0	A2	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in HD_VENC_D_cfg1)

1.3.9.6 HD_VENC_D_cfg5 Register (offset = 14h) [reset = 0h]

HD_VENC_D_cfg5 is shown in Figure 1-442 and described in Table 1-355.

Color Space Converter Coefficient Register

Figure 1-442. HD_VENC_D_cfg5 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-355. HD_VENC_D_cfg5 Register Field Descriptions

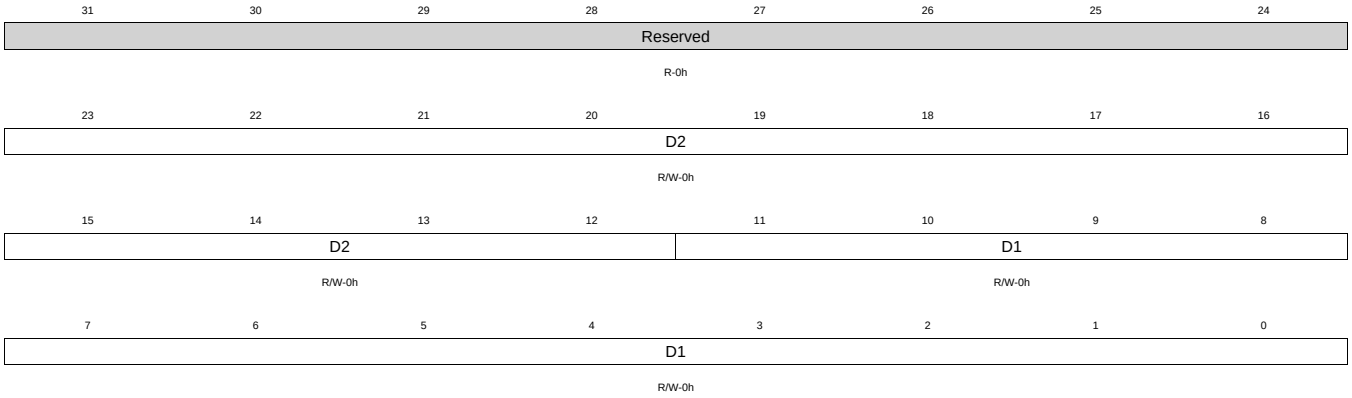
Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	Reserved
27-16	D0	R/W	0h	Coefficients of color space converter. This coefficient is an integer number in the range of -2048 to 2047. It is in 12-bit wide 2's compliment format. The MSB is sign bit. For example, if this coefficient is 749, then 0x2ED (hex format) should be assigned to this register. Another example, if this coefficient is -1021, then 0xC03 should be assigned to this register.
15-13	Reserved	R	0h	Reserved
12-0	C2	R/W	0h	Coefficients of color space converter. This coefficient is a real number in the range of -4 to +4 represent in Q3.10 format. The MSB is sign bit. (Same format conversion as A0 in HD_VENC_D_cfg1)

1.3.9.7 HD_VENC_D_cfg6 Register (offset = 18h) [reset = 0h]

HD_VENC_D_cfg6 is shown in Figure 1-443 and described in Table 1-356.

Color Space Converter Coefficient Register

Figure 1-443. HD_VENC_D_cfg6 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-356. HD_VENC_D_cfg6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	D2	R/W	0h	Coefficients of color space converter. This coefficient is an integer number in the range of -2048 to 2047. It is in 12-bit wide 2's compliment format. The MSB is sign bit. (Same format conversion as D0 in HD_VENC_D_cfg5)
11-0	D1	R/W	0h	Coefficients of color space converter. This coefficient is an integer number in the range of -2048 to 2047. It is in 12-bit wide 2's compliment format. The MSB is sign bit. (Same format conversion as D0 in HD_VENC_D_cfg5)

1.3.9.8 HD_VENC_D_cfg7 Register (offset = 1Ch) [reset = 0h]

HD_VENC_D_cfg7 is shown in Figure 1-444 and described in Table 1-357.

Reserved Register

Figure 1-444. HD_VENC_D_cfg7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-357. HD_VENC_D_cfg7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.9.9 HD_VENC_D_cfg8 Register (offset = 20h) [reset = 0h]

HD_VENC_D_cfg8 is shown in Figure 1-445 and described in Table 1-358.

Reserved Register

Figure 1-445. HD_VENC_D_cfg8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-358. HD_VENC_D_cfg8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.9.10 HD_VENC_D_cfg9 Register (offset = 24h) [reset = 0h]

HD_VENC_D_cfg9 is shown in Figure 1-446 and described in Table 1-359.

Reserved Register

Figure 1-446. HD_VENC_D_cfg9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-359. HD_VENC_D_cfg9 Register Field Descriptions

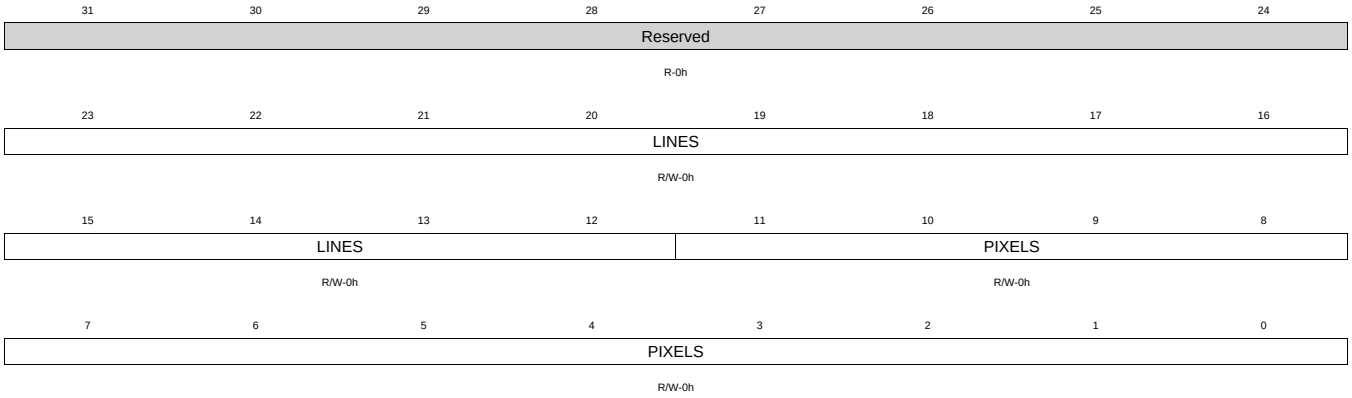
Bit	Field	Type	Reset	Description
31-20	Reserved	R	0h	Reserved

1.3.9.11 HD_VENC_D_cfg10 Register (offset = 28h) [reset = 0h]

HD_VENC_D_cfg10 is shown in Figure 1-447 and described in Table 1-360.

Frame Size Register

Figure 1-447. HD_VENC_D_cfg10 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-360. HD_VENC_D_cfg10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	LINES	R/W	0h	Defines the total number of lines per frame.
11-0	PIXELS	R/W	0h	Defines the total number of pixels per line.

1.3.9.12 HD_VENC_D_cfg11 Register (offset = 2Ch) [reset = 0h]

HD_VENC_D_cfg11 is shown in Figure 1-448 and described in Table 1-361.

Reserved Register

Figure 1-448. HD_VENC_D_cfg11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-361. HD_VENC_D_cfg11 Register Field Descriptions

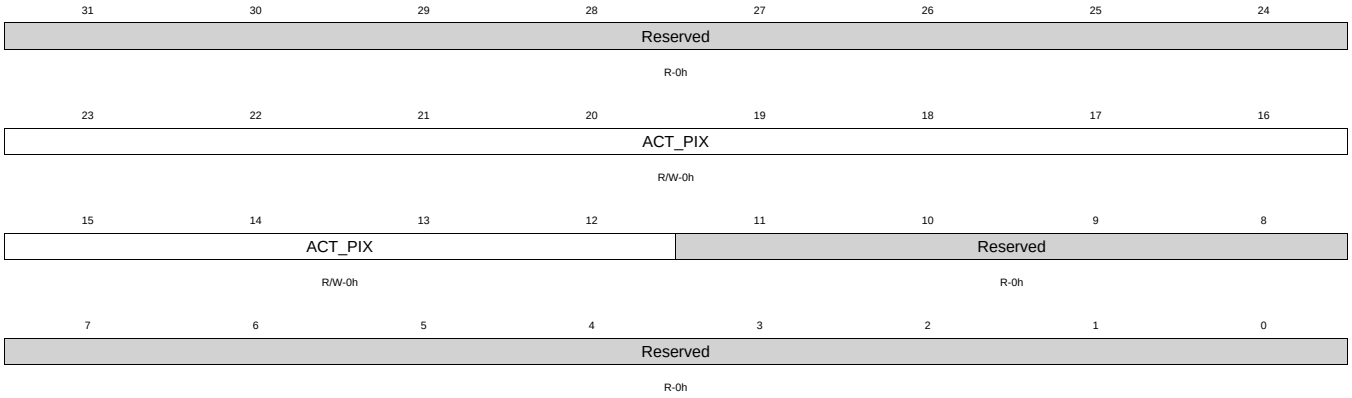
Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved

1.3.9.13 HD_VENC_D_cfg12 Register (offset = 30h) [reset = 0h]

HD_VENC_D_cfg12 is shown in Figure 1-449 and described in Table 1-362.

Active Pixels per Line Register

Figure 1-449. HD_VENC_D_cfg12 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-362. HD_VENC_D_cfg12 Register Field Descriptions

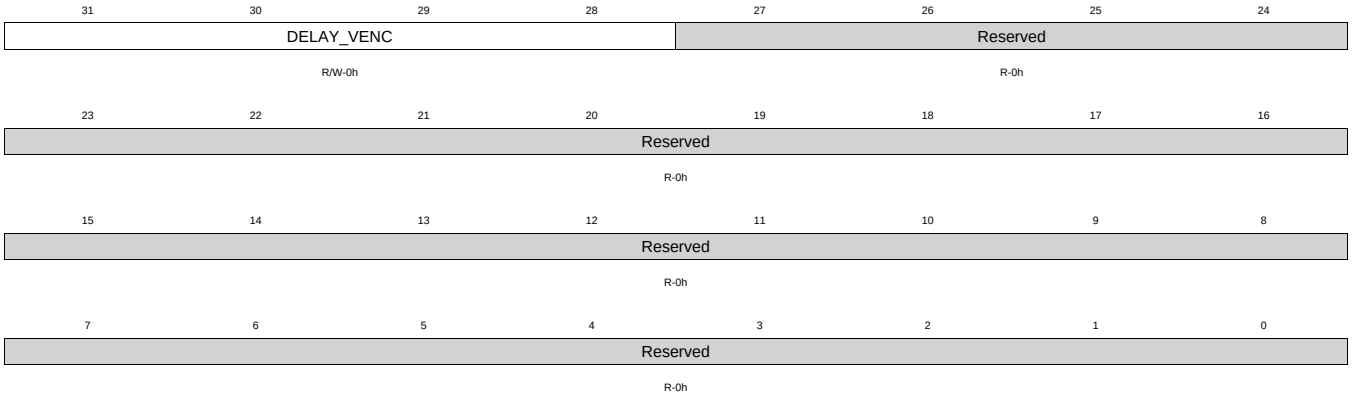
Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	ACT_PIX	R/W	0h	Defines the number of active pixels in one video line.
11-0	Reserved	R	0h	Reserved

1.3.9.14 HD_VENC_D_cfg13 Register (offset = 34h) [reset = 0h]

HD_VENC_D_cfg13 is shown in Figure 1-450 and described in Table 1-363.

VENC Control Register

Figure 1-450. HD_VENC_D_cfg13 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-363. HD_VENC_D_cfg13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	DELAY_VENC	R/W	0h	The high-4-bits of the delay counter of VENC_EN signal.. the low 8-bit of this counter is specified in CFG20
27-0	Reserved	R	0h	Reserved

1.3.9.15 HD_VENC_D_cfg14 Register (offset = 38h) [reset = 0h]

HD_VENC_D_cfg14 is shown in Figure 1-451 and described in Table 1-364.

Reserved Register

Figure 1-451. HD_VENC_D_cfg14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-364. HD_VENC_D_cfg14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved

1.3.9.16 HD_VENC_D_cfg15 Register (offset = 3Ch) [reset = 0h]

HD_VENC_D_cfg15 is shown in Figure 1-452 and described in Table 1-365.

DVO Control Register

Figure 1-452. HD_VENC_D_cfg15 Register

31	30	29	28	27	26	25	24
DVO_HS_WD							
R/W-0h							

23	22	21	20	19	18	17	16
DVO_AVD_HW							
R/W-0h							

15	14	13	12	11	10	9	8
DVO_AVD_HW				DVO_AVST_H			
R/W-0h				R/W-0h			

7	6	5	4	3	2	1	0
DVO_AVST_H							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-365. HD_VENC_D_cfg15 Register Field Descriptions

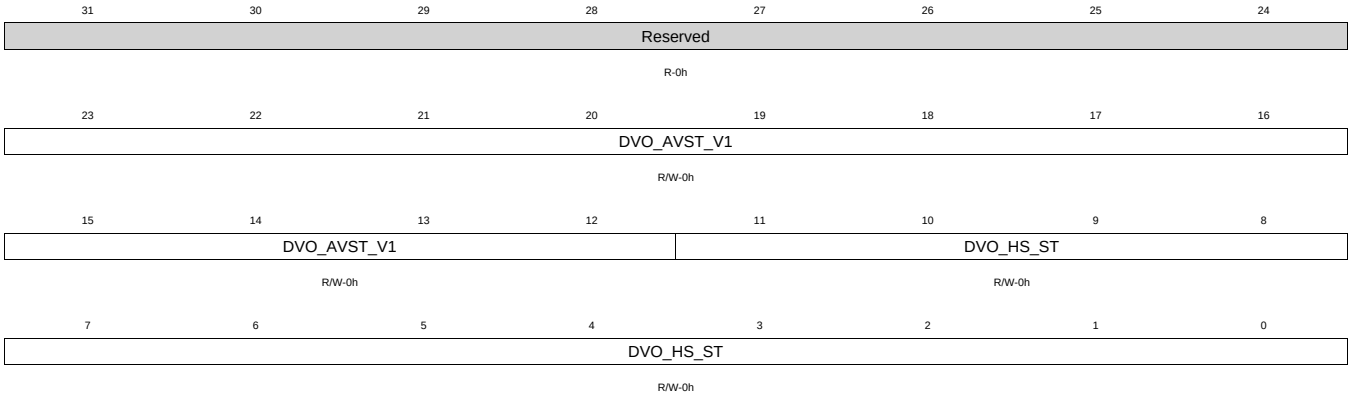
Bit	Field	Type	Reset	Description
31-24	DVO_HS_WD	R/W	0h	Defines the width of DVO_HS pulse (in number of pixels).
23-12	DVO_AVD_HW	R/W	0h	Defines the width of each active video line (in number of pixels).
11-0	DVO_AVST_H	R/W	0h	Active Video Start Time DVO_AVST_H = CFG10.PIXELS – CFG12.ACT_PIX This parameter defines the SAV location in embedded sync mode and the location of the first active pixel on the DVO output in discrete sync mode.

1.3.9.17 HD_VENC_D_cfg16 Register (offset = 40h) [reset = 0h]

HD_VENC_D_cfg16 is shown in Figure 1-453 and described in Table 1-366.

DVO Control Register

Figure 1-453. HD_VENC_D_cfg16 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-366. HD_VENC_D_cfg16 Register Field Descriptions

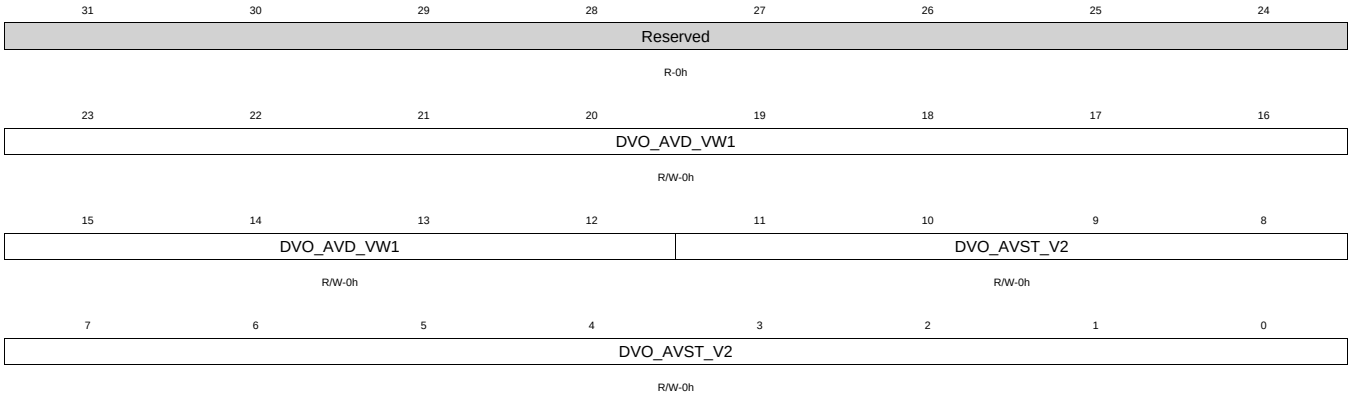
Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	DVO_AVST_V1	R/W	0h	In progressive mode, it defines the first active line in a frame. In interlace mode, it defines the first active line of the first field in a frame.
11-0	DVO_HS_ST	R/W	0h	Defines the starting location of the DVO_HS pulse on each line.

1.3.9.18 HD_VENC_D_cfg17 Register (offset = 44h) [reset = 0h]

HD_VENC_D_cfg17 is shown in Figure 1-454 and described in Table 1-367.

DVO Control Register

Figure 1-454. HD_VENC_D_cfg17 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-367. HD_VENC_D_cfg17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	DVO_AVD_VW1	R/W	0h	In progressive mode, it defines the number of active video lines in a frame. In interlace mode, it defines the number of active lines in the first field.
11-0	DVO_AVST_V2	R/W	0h	Defines the first active line of second field in a frame. This parameter is only used in interlace mode.

1.3.9.19 HD_VENC_D_cfg18 Register (offset = 48h) [reset = 0h]

HD_VENC_D_cfg18 is shown in Figure 1-455 and described in Table 1-368.

DVO Control Register

Figure 1-455. HD_VENC_D_cfg18 Register

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-368. HD_VENC_D_cfg18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DVO_VS_WD1	R/W	0h	In progressive mode. it defines the width of the DVO_VS pulse In interlace mode. it defines the width of the DVO_VS pulse of the first field.
23-12	DVO_VS_ST1	R/W	0h	In progressive mode, it defines the starting location of the DVO_VS pulse in a frame. In interlace mode, it defines the starting location of DVO_VS pulse of the first field.
11-0	DVO_AVD_VW2	R/W	0h	Defines the number of active lines in the second field. This parameter is only used in interlace mode.

1.3.9.20 HD_VENC_D_cfg19 Register (offset = 4Ch) [reset = 0h]

HD_VENC_D_cfg19 is shown in Figure 1-456 and described in Table 1-369.

DVO Control Register

Figure 1-456. HD_VENC_D_cfg19 Register

31	30	29	28	27	26	25	24
DVO_VS_WD2							
R/W-0h							

23	22	21	20	19	18	17	16
DVO_FID_ST1							
R/W-0h							

15	14	13	12	11	10	9	8
DVO_FID_ST1				DVO_VS_ST2			
R/W-0h				R/W-0h			

7	6	5	4	3	2	1	0
DVO_VS_ST2							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-369. HD_VENC_D_cfg19 Register Field Descriptions

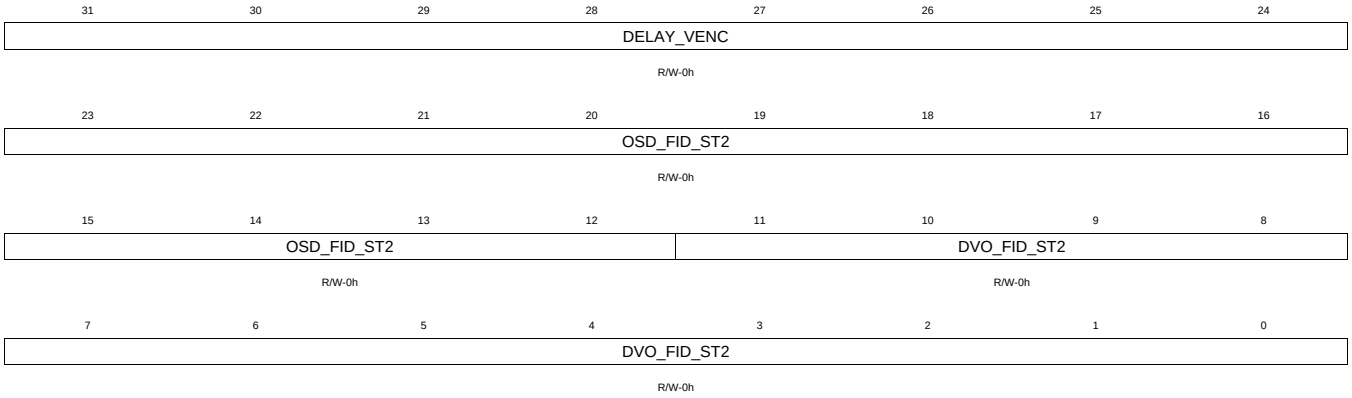
Bit	Field	Type	Reset	Description
31-24	DVO_VS_WD2	R/W	0h	Defines the width of the DVO_VS pulse of the second field (in number of lines)
23-12	DVO_FID_ST1	R/W	0h	This parameter defines the top field line number at which the DVO_FID will switch (only applicable in the interlaced mode).
11-0	DVO_VS_ST2	R/W	0h	Defines the starting location of the DVO_VS of the second field. This parameter is only used in interlace mode.

1.3.9.21 HD_VENC_D_cfg20 Register (offset = 50h) [reset = 0h]

HD_VENC_D_cfg20 is shown in Figure 1-457 and described in Table 1-370.

DVO/Compositor IF Control Register

Figure 1-457. HD_VENC_D_cfg20 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-370. HD_VENC_D_cfg20 Register Field Descriptions

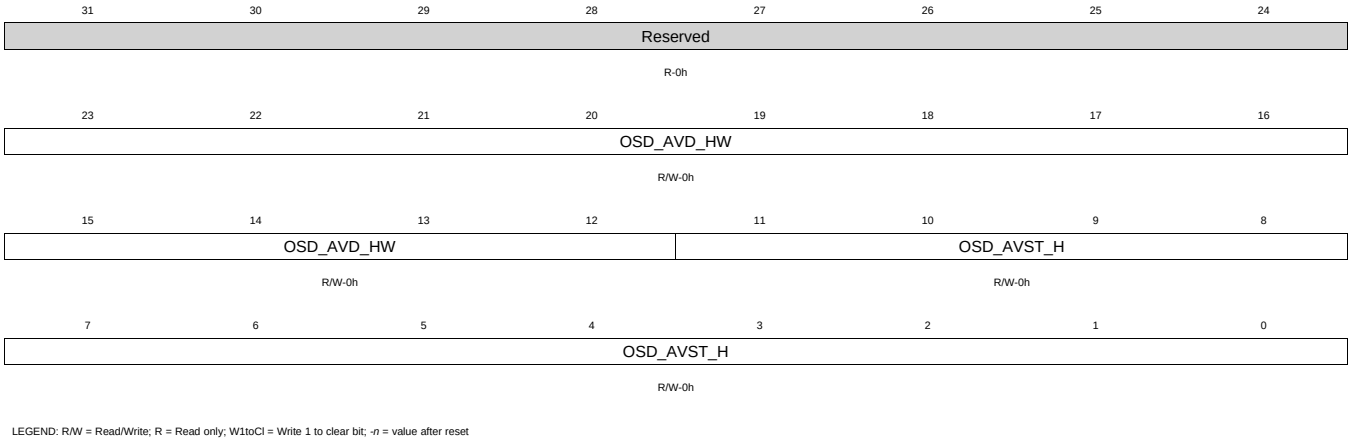
Bit	Field	Type	Reset	Description
31-24	DELAY_VENC	R/W	0h	These are the low 8-bits of the delay counter of VENC_EN signal from top. The high 4-bit is in CFG13. The maximum delay from the VENC_EN's activation is 4096 pixel clock periods.
23-12	OSD_FID_ST2	R/W	0h	This parameter defines the bottom field line number at which the DTV_FID will switch. This parameter is only used in interlace mode. OSD_FID_ST2 = int (cfg010.lines/2 + OSD_FID_ST1)
11-0	DVO_FID_ST2	R/W	0h	Defines the starting location of the second field in interlace mode. This parameter is only used in interlace mode.

1.3.9.22 HD_VENC_D_cfg21 Register (offset = 54h) [reset = 0h]

HD_VENC_D_cfg21 is shown in Figure 1-458 and described in Table 1-371.

Compositor IF Control Register

Figure 1-458. HD_VENC_D_cfg21 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-371. HD_VENC_D_cfg21 Register Field Descriptions

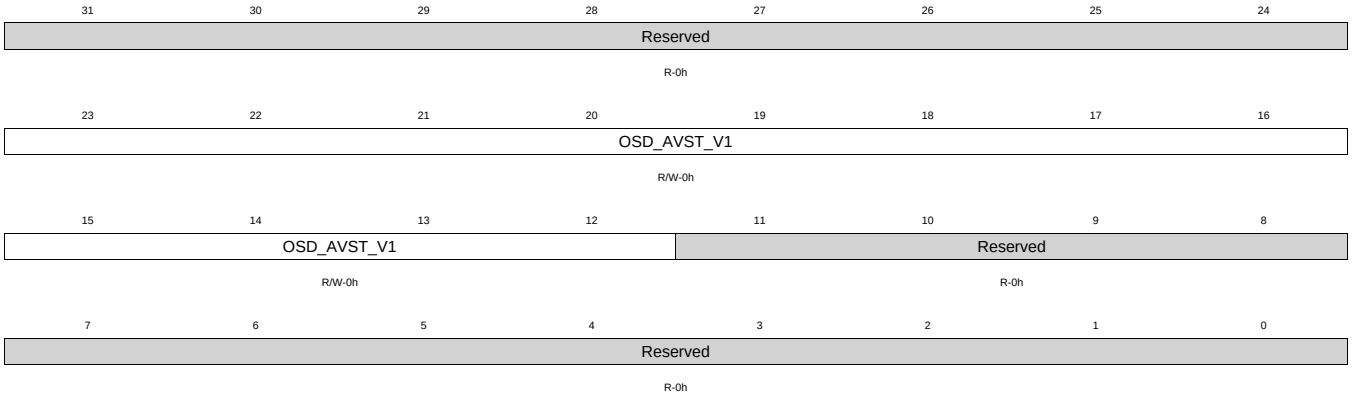
Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	OSD_AVD_HW	R/W	0h	Defines the width of each active video line (in number of pixels).
11-0	OSD_AVST_H	R/W	0h	This parameters defines when the first pixel on each line must appear at the input of the HD_VENC (a fixed offset from DVO_AVST_H). OSD_AVST_H = DVO_AVST_H – 8.

1.3.9.23 HD_VENC_D_cfg22 Register (offset = 58h) [reset = 0h]

HD_VENC_D_cfg22 is shown in Figure 1-459 and described in Table 1-372.

Compositor IF Control Register

Figure 1-459. HD_VENC_D_cfg22 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-372. HD_VENC_D_cfg22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	OSD_AVST_V1	R/W	0h	In progressive mode. it defines the first active line in a frame. In interlace mode. it defines the first active line of first field in a frame (The line number starts at 0)
11-0	Reserved	R	0h	Reserved

1.3.9.24 HD_VENC_D_cfg23 Register (offset = 5Ch) [reset = 0h]

HD_VENC_D_cfg23 is shown in Figure 1-460 and described in Table 1-373.

Compositor IF Control Register

Figure 1-460. HD_VENC_D_cfg23 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
OSD_AVD_VW1							
R/W-0h							

15	14	13	12	11	10	9	8
OSD_AVD_VW1				OSD_AVST_V2			
R/W-0h				R/W-0h			

7	6	5	4	3	2	1	0
OSD_AVST_V2							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-373. HD_VENC_D_cfg23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	OSD_AVD_VW1	R/W	0h	Defines the number of active lines for the input frame (or first field) of the HD_VENC_D. Normally, this should be same as DVO_AVD_VW1.
11-0	OSD_AVST_V2	R/W	0h	Defines the first active line of second field in a frame. This parameter is only used in interlace mode.

1.3.9.25 HD_VENC_D_cfg24 Register (offset = 60h) [reset = 0h]

HD_VENC_D_cfg24 is shown in Figure 1-461 and described in Table 1-374.

Compositor IF Control Register

Figure 1-461. HD_VENC_D_cfg24 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved				OSD_AVD_VW2			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
OSD_AVD_VW2							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-374. HD_VENC_D_cfg24 Register Field Descriptions

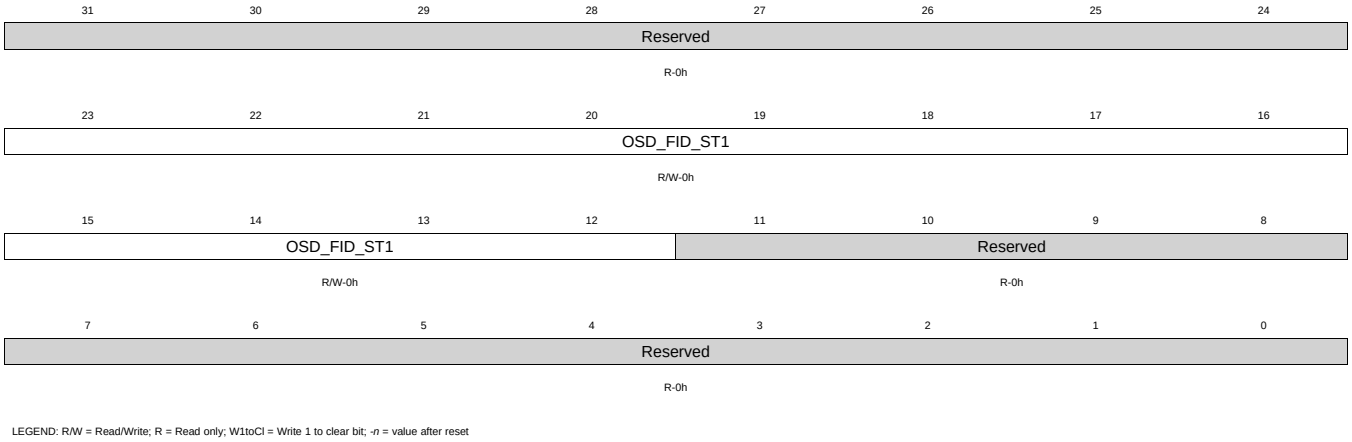
Bit	Field	Type	Reset	Description
31-12	Reserved	R	0h	Reserved
11-0	OSD_AVD_VW2	R/W	0h	Defines the number of active lines in the second field. This parameter is only used in interface mode.

1.3.9.26 HD_VENC_D_cfg25 Register (offset = 64h) [reset = 0h]

HD_VENC_D_cfg25 is shown in Figure 1-462 and described in Table 1-375.

Compositor IF Control Register

Figure 1-462. HD_VENC_D_cfg25 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-375. HD_VENC_D_cfg25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	Reserved
23-12	OSD_FID_ST1	R/W	0h	This parameter defines the frame line (for progressive mode) or top field line (for interlaced mode) number at which the DTV_FID will switch. Progressive mode: OSD_FID_ST1 = int ((cfg010.lines – cfg023.osd_avd_vw1)/3) Interlace mode: OSD_FID_ST1 = int ((cfg010.lines/2 – cfg023.osd_avd_vw1)/3)
11-0	Reserved	R	0h	Reserved

Note: DTV_FID switches to both progressive and interlaced mode to indicate to internal processing modules that a new frame/field is starting. The above OSD_FID_ST1 parameter setup configures the DTV_FID to switch about 1/3 into the VBI period, giving sufficient timing margin for DMA set-up and video pipeline fill-up prior to the next active video period.

1.3.9.27 HD_VEND_D_GAMMA_LUT Register (offset = 1000h-1FFFh) [reset = 0h]

HD_VEND_D_GAMMA_LUT is shown in Figure 1-463 and described in Table 1-376.

Figure 1-463. HD_VEND_D_GAMMA_LUT Register

31	30	29	28	27	26	25	24
Reserved		lut2[a]					
R-0		R/W-0h					
23	22	21	20	19	18	17	16
lut2[a]				lut1[a]			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
lut1[a]						lut0[a]	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
lut0[a]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-376. HD_VEND_D_GAMMA_LUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	Reserved
29-20	lut2[a]	R/W	-	Value for lut2[a], where a corresponds to bits [11:2] of the source address
19-10	lut1[a]	R/W	-	Value for lu12[a], where a corresponds to bits [11:2] of the source address
9-0	lut0[a]	R/W	-	Value for lut0[a], where a corresponds to bits [11:2] of the source address

Note: The reset value of the HD_VENC_D_GAMMA_LUT registers are undefined. If Gamma Correction functionality is to be used (controlled by HD_VENC_D_cfg0.BYPS_GC), this MMR area must be loaded by software before enabling HD_VENC_D.

1.3.10 NOISE_FILTER Registers

Table 1-377 lists the memory-mapped registers for the NOISE_FILTER. All register offset addresses not listed in Table 1-377 should be considered as reserved locations and the register contents should not be modified.

Table 1-377. NOISE_FILTER REGISTERS

Offset	Acronym	Register Name	Section
0h	nf_reg0	NF Mode Reg	Section 1.3.10.1
4h	nf_reg1	NF Video Size Config Reg	Section 1.3.10.2
8h	nf_reg2	NF Spatial Strength Y Reg	Section 1.3.10.3
Ch	nf_reg3	NF Spatial Strength UV Reg	Section 1.3.10.4
10h	nf_reg4	NF Temporal Filter Config Reg	Section 1.3.10.5
14h	nf_reg5	NF Noise Config Reg	Section 1.3.10.6
18h	nf_reg6	NF BW Threshold Config Reg	Section 1.3.10.7
1Ch	nf_reg7	NF Saved Noise Frame Index Reg	Section 1.3.10.8
20h	nf_reg8	NF Saved Noise Frame Y Data Reg	Section 1.3.10.9
24h	nf_reg9	NF Saved Noise Frame UV Data Reg	Section 1.3.10.10

1.3.10.1 nf_reg0 Register (offset = 0h) [reset = 0h]

nf_reg0 is shown in Figure 1-464 and described in Table 1-378.

Figure 1-464. nf_reg0 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved			NF_UPDATE_FRAME_NOISE	NF_LOAD_FRAME_NOISE	NF_BYPASS_CFG		NF_VIDEO_INDEX
R-0h			R/W-0h	R/W-0h	R/W-0h		R/W-0h

7	6	5	4	3	2	1	0
NF_VIDEO_INDEX				Reserved	NF_REF_CFG		NF_EN
R/W-0h				R-0h	R/W-0h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-378. nf_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	Reserved	R	0h	Reserved (Write 0x0 only)
12	NF_UPDATE_FRAME_NOISE	R/W	0h	NF Frame Noise Update Enable 0: Do not Update 1: Update When set to 1, frameNoise_previous registers get updated at the end of current frame processing. When set to 0.. updates are not done allowing next frame to use the same initial frame noise value used by the previous frame.
11	NF_LOAD_FRAME_NOISE	R/W	0h	NF Frame Noise Load Enable When a new video is assigned to nf_video_index.. this bit needs to be set to initialize (clear or reload) internally stored frameNoise_previous registers. 0: Do not overwrite 1: Inititalize (overwrite) When set to 1, values last written into NF_REG8 and NF_REG9 are used as new initial values.
10-9	NF_BYPASS_CFG	R/W	0h	NF Bypass Configuration - Reserved for DEBUG purpose only (Important : Write only 0) To perform configure DSS_NF in a bypass mode (spatial input bypass), configure the DSS_NF normally and set the spatial and temporal strength registers to 0x0.
8-4	NF_VIDEO_INDEX	R/W	0h	NF Video Index: Index to select stored noise level (0 - 31)
3	Reserved	R	0h	
2-1	NF_REF_CFG	R/W	0h	NF Reference Frame Configuration 00: DMA enabled.. Data Passed 01: DMA enabled.. Output Forced to Black 1x: DMA disabled.. Output Forced to Black (for first pass through the NF processing with no valid REF frame in the memory)
0	NF_EN	R/W	0h	NF Enable: 0: Disabled 1: Enabled

1.3.10.2 nf_reg1 Register (offset = 4h) [reset = 0h]

nf_reg1 is shown in Figure 1-465 and described in Table 1-379.

Figure 1-465. nf_reg1 Register

31	30	29	28	27	26	25	24
Reserved					HEIGHT		
R-0h					R/W-0h		

23	22	21	20	19	18	17	16
HEIGHT							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved					WIDTH		
R-0h					R/W-0h		

7	6	5	4	3	2	1	0
WIDTH							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-379. nf_reg1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	HEIGHT	R/W	0h	Number of lines per frame
15-11	Reserved	R	0h	
10-0	WIDTH	R/W	0h	Number of pixels per line

1.3.10.3 nf_reg2 Register (offset = 8h) [reset = 00000808h]

nf_reg2 is shown in Figure 1-466 and described in Table 1-380.

Figure 1-466. nf_reg2 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
SPATIAL_STRENGTH_Y_HIGH							
R/W-8h							

7	6	5	4	3	2	1	0
SPATIAL_STRENGTH_Y_LOW							
R/W-8h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-380. nf_reg2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	
15-8	SPATIAL_STRENGTH_Y_HIGH	R/W	8h	Spatial high-frequency filter strength of Y channel. 0 means disabled.
7-0	SPATIAL_STRENGTH_Y_LOW	R/W	8h	Spatial low-frequency filter strength of Y channel. 0 means disabled.

1.3.10.4 nf_reg3 Register (offset = Ch) [reset = 10101010h]

nf_reg3 is shown in Figure 1-467 and described in Table 1-381.

Figure 1-467. nf_reg3 Register

31	30	29	28	27	26	25	24
SPATIAL_STRENGTH_V_HIGH							
R/W-10h							
23	22	21	20	19	18	17	16
SPATIAL_STRENGTH_V_LOW							
R/W-10h							
15	14	13	12	11	10	9	8
SPATIAL_STRENGTH_U_HIGH							
R/W-10h							
7	6	5	4	3	2	1	0
SPATIAL_STRENGTH_U_LOW							
R/W-10h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

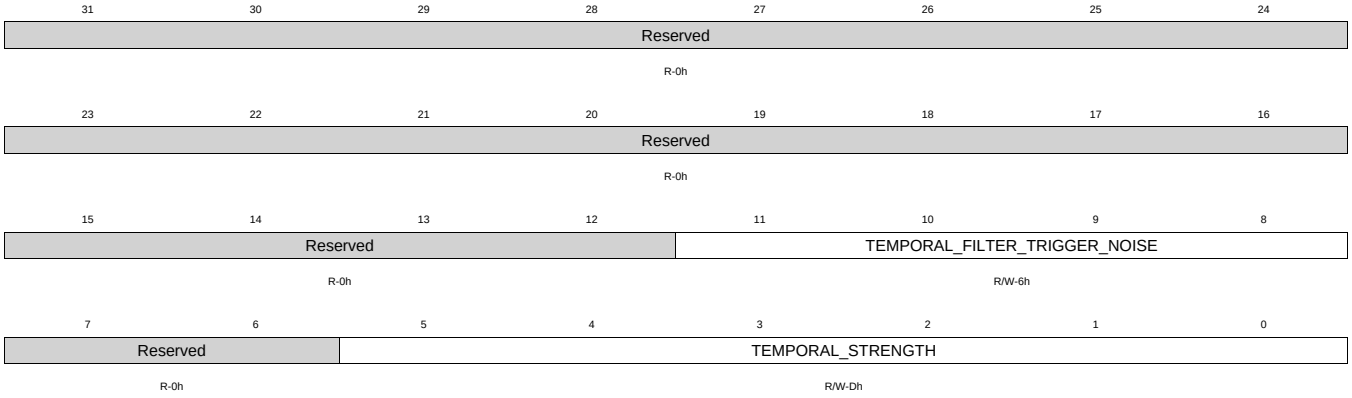
Table 1-381. nf_reg3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SPATIAL_STRENGTH_V_HIGH	R/W	10h	Spatial high-frequency filter strength of V channel. 0 means disabled.
23-16	SPATIAL_STRENGTH_V_LOW	R/W	10h	Spatial low-frequency filter strength of V channel. 0 means disabled.
15-8	SPATIAL_STRENGTH_U_HIGH	R/W	10h	Spatial high-frequency filter strength of U channel. 0 means disabled.
7-0	SPATIAL_STRENGTH_U_LOW	R/W	10h	Spatial low-frequency filter strength of U channel. 0 means disabled.

1.3.10.5 nf_reg4 Register (offset = 10h) [reset = 0000060Dh]

nf_reg4 is shown in Figure 1-468 and described in Table 1-382.

Figure 1-468. nf_reg4 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-382. nf_reg4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	Reserved	R	0h	
11-8	TEMPORAL_FILTER_TRIGGER_NOISE	R/W	6h	The smallest noise level to fully trigger temporal filter.
7-6	Reserved	R	0h	
5-0	TEMPORAL_STRENGTH	R/W	Dh	Temporal filter strength. 0 means disabled.

1.3.10.6 nf_reg5 Register (offset = 14h) [reset = 000000ADh]

nf_reg5 is shown in Figure 1-469 and described in Table 1-383.

Figure 1-469. nf_reg5 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							MAX_NOISE
R-0h							R/W-Ah

7	6	5	4	3	2	1	0
MAX_NOISE				NOISE_IIR_COEFFICIENT			
R/W-Ah				R/W-Dh			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-383. nf_reg5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	Reserved	R	0h	
8-4	MAX_NOISE	R/W	Ah	Max of the possible noise level.
3-0	NOISE_IIR_COEFFICIENT	R/W	Dh	Noise level IIR filter coefficient.

1.3.10.7 nf_reg6 Register (offset = 18h) [reset = 00000F0Fh]

nf_reg6 is shown in Figure 1-470 and described in Table 1-384.

Figure 1-470. nf_reg6 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved		PURE_WHITE_THRESHOLD					
R-0h		R/W-Fh					
7	6	5	4	3	2	1	0
Reserved		PURE_BLACK_THRESHOLD					
R-0h		R/W-Fh					

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-384. nf_reg6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	Reserved	R	0h	
13-8	PURE_WHITE_THRESHOLD	R/W	Fh	A tile is considered pure white if all pixel values are above pure_white_threshold.
7-6	Reserved	R	0h	
5-0	PURE_BLACK_THRESHOLD	R/W	Fh	A tile is considered pure black if all pixel values are below pure_black_threshold.

1.3.10.8 nf_reg7 Register (offset = 1Ch) [reset = 0h]

nf_reg7 is shown in Figure 1-471 and described in Table 1-385.

Figure 1-471. nf_reg7 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
Reserved			FRAME_NOISE_READ_INDEX				
R-0h			R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-385. nf_reg7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	Reserved	R	0h	
4-0	FRAME_NOISE_READ_INDEX	R/W	0h	Saved Frame Noise Register bank index (used to select one of 32 registers when accessing NF_REG8 or NF_REG9)

1.3.10.9 nf_reg8 Register (offset = 20h) [reset = 0h]

nf_reg8 is shown in Figure 1-472 and described in Table 1-386.

Figure 1-472. nf_reg8 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved			FRAME_NOISE_Y				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
FRAME_NOISE_Y							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-386. nf_reg8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	Reserved	R	0h	
12-0	FRAME_NOISE_Y	R/W	0h	Saved Frame Noise Luma (y) (Read) Save Frame_noise_y selected by Frame_noise_read_index register (Write) Value to be written to the Frame_noise_y selected by NF_REG0(nf_video_index) at the beginning of a new frame

1.3.10.10 nf_reg9 Register (offset = 24h) [reset = 0h]

nf_reg9 is shown in Figure 1-473 and described in Table 1-387.

Figure 1-473. nf_reg9 Register

31	30	29	28	27	26	25	24
Reserved			FRAME_NOISE_U				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
FRAME_NOISE_U							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			FRAME_NOISE_V				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
FRAME_NOISE_V							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-387. nf_reg9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	FRAME_NOISE_U	R/W	0h	Saved Frame Noise Chroma(cb/u) (Read) Save Frame_noise_v selected by Frame_noise_read_index register (Write) Value to be written to the Frame_noise_u selected by NF_REG0(nf_video_index) at the beginning of a new frame
15-13	Reserved	R	0h	
12-0	FRAME_NOISE_V	R/W	0h	Saved Frame Noise Chroma(cr/v) (Read) Save Frame_noise_v selected by Frame_noise_read_index register (Write) Value to be written to the Frame_noise_v selected by NF_REG0(nf_video_index) at the beginning of a new frame

1.3.11 SC_M Registers

Table 1-388 lists the memory-mapped registers for the SC_M. All register offset addresses not listed in Table 1-388 should be considered as reserved locations and the register contents should not be modified.

Table 1-388. SC_M REGISTERS

Offset	Acronym	Register Name	Section
0h	SC_M_cfg_sc0	SC Mode Configuration Reg	Section 1.3.11.1
4h	SC_M_cfg_sc1	SC Vertical Scaler Config Reg 0	Section 1.3.11.2
8h	SC_M_cfg_sc2	SC Vertical Scaler Config Reg 1	Section 1.3.11.3
Ch	SC_M_cfg_sc3	SC Vertical Scaler Config Reg 2	Section 1.3.11.4
10h	SC_M_cfg_sc4	SC Target Size Reg	Section 1.3.11.5
14h	SC_M_cfg_sc5	SC Source Size Reg	Section 1.3.11.6
18h	SC_M_cfg_sc6	SC Vertical Scaler Config Reg 3	Section 1.3.11.7
20h	SC_M_cfg_sc8	SC Horizontal Scaler Config Reg 0	Section 1.3.11.8
24h	SC_M_cfg_sc9	SC Horizontal Scaler Config Reg 1	Section 1.3.11.9
28h	SC_M_cfg_sc10	SC Horizontal Scaler Config Reg 2	Section 1.3.11.10
2Ch	SC_M_cfg_sc11	SC Horizontal Scaler Config Reg 3	Section 1.3.11.11
30h	SC_M_cfg_sc12	SC Horizontal Scaler Config Reg 4	Section 1.3.11.12
34h	SC_M_cfg_sc13	SC Vertical Scaler Config Reg 4	Section 1.3.11.13
44h	SC_M_cfg_sc17	SC Vertical Scaler Config Reg 5	Section 1.3.11.14
48h	SC_M_cfg_sc18	SC Vertical Scaler Config Reg 6	Section 1.3.11.15
4Ch	SC_M_cfg_sc19	SC Peaking Filter Config Reg 0	Section 1.3.11.16
50h	SC_M_cfg_sc20	SC Peaking Filter Config Reg 1	Section 1.3.11.17
54h	SC_M_cfg_sc21	SC Peaking Filter Config Reg 2	Section 1.3.11.18
58h	SC_M_cfg_sc22	SC Peaking Filter Config Reg 3	Section 1.3.11.19
5Ch	SC_M_cfg_sc23	SC Edeg Detection Config Reg 3	Section 1.3.11.20
60h	SC_M_cfg_sc24	SC Trimmer Config Reg 0	Section 1.3.11.21
64h	SC_M_cfg_sc25	SC Trimmer Config Reg 1	Section 1.3.11.22

1.3.11.1 SC_M_cfg_sc0 Register (offset = 0h) [reset = 0h]

SC_M_cfg_sc0 is shown in Figure 1-474 and described in Table 1-389.

Figure 1-474. SC_M_cfg_sc0 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							CFG_FID_SELFGEN
R-0h							R/W-0h
15	14	13	12	11	10	9	8
CFG_TRIM	CFG_Y_PK_EN	Reserved			CFG_INTERLACE_I	CFG_HP_BYPASS	CFG_DCM_4X
R/W-0h	R/W-0h	R-0h			R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CFG_DCM_2X	CFG_AUTO_HS	Reserved	CFG_USE_RAV	CFG_INVT_FID	CFG_SC_BYPASS	CFG_LINEAR	CFG_INTERLACE_O
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-389. SC_M_cfg_sc0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	Reserved	R	0h	
16	CFG_FID_SELFGEN	R/W	0h	FID self generate enable. When input is progressive and this bit is set, the SC generates self-toggling (top/bottom) output FID when performing interlacing.
15	CFG_TRIM	R/W	0h	Trimming enable. When 1, the input image whose size is specified by orgW and orgH registers is trimmed to the size with srcW and srcH from the offset specified by offW and offH. 0: disable trimming 1: enable trimming
14	CFG_Y_PK_EN	R/W	0h	This parameter is used by peaking block. 0: disable luma peaking 1: enable luma peaking
13-11	Reserved	R	0h	
10	CFG_INTERLACE_I	R/W	0h	This parameter is used by both horizontal and vertical scaling 0: the input video format is progressive 1: the input video format is interlace
9	CFG_HP_BYPASS	R/W	0h	This parameter is used by horizontal scaling. If cfg_auto_hs is 0, horizontal polyphase filter is always enabled. In this case, this register is DON'T CARE. If cfg_auto_hs is 1, 0 : The polyphase scaler is always used regardless of the scaling ratio. 1 : The polyphase scaler is bypassed only when (tar_w == src_w) or (tar_w == src_w/2) or (tar_w == src_w/4)
8	CFG_DCM_4X	R/W	0h	This parameter is used by horizontal scaling. 0: the 4X decimation filter is disabled 1: the 4X decimation filter is enabled Note: (1) Either 2X or 4X can be enabled, but they cannot be enabled simultaneously. (2) This register is only set to 1 when it makes sense to do so. Typically, it is used when (horizontal scale ratio < 0.25). (3) This register is DON'T CARE when cfg_auto_hs = 1.

Table 1-389. SC_M_cfg_sc0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CFG_DCM_2X	R/W	0h	This parameter is used by horizontal scaling. 0: the 2X decimation filter is disabled 1: the 2X decimation filter is enabled Note: (1) Either 2X or 4X can be enabled, but they cannot be enabled simultaneously. (2) This register is only set to 1 when it makes sense to do so. Typically, it is used when (0.25 < horizontal scale ratio < 0.5). (3) This register is DON'T CARE when cfg_auto_hs = 1.
6	CFG_AUTO_HS	R/W	0h	This parameter is used by horizontal scaling. 0: the cfg_dcm_2x and cfg_dcm_4x bits will enable appropriate decimation filters 1: HW will decide whether up-scaling or down-scaling is required based on horizontal scaling ratio (SR). SR > 0.5 : horizontal polyphase filter is enabled, all decimation filters are disabled SR = 0.5 : dcm_2x is enabled, horizontal polyphase filter is enabled or disabled based on cfg_hp_bypass 0.5 > SR > 0.25 : dcm_2x and horizontal polyphase filter both are enabled SR = 0.25 : dcm_4x is enabled, horizontal polyphase filter is enabled or disabled based on cfg_hp_bypass 0.25 > SR > 0.125 : dcm_4x and horizontal polyphase filter are both enabled SR <= 0.125 : Functionally supported, but not recommended in auto mode for image quality concerns
5	Reserved	R	0h	
4	CFG_USE_RAV	R/W	0h	This parameter is used by vertical scaling. 0: Poly-phase filter will be used for the vertical scaling 1: Running average filter will be used for the vertical scaling (down scaling only)
3	CFG_INVT_FID	R/W	0h	This parameter inverts the polarity of the incoming FID bit before applying to Scaler function. 0: treat incoming FID=0 to be bottom field and FID=1 to be top field data 1: treat incoming FID=1 to be bottom field and FID=0 to be top field data Incoming FID is the FID value programmed in the VPDMA descriptor. For this device, CFG_INVT_FID should be set to 0x1 always.
2	CFG_SC_BYPASS	R/W	0h	This parameter is a general purpose. 0: Scaling module will engaged 1: Scaling module will be bypassed
1	CFG_LINEAR	R/W	0h	This parameter is used by horizontal scaling. 0: Anamorphic scaling... 1: Linear scaling
0	CFG_INTERLACE_O	R/W	0h	This parameter is used by vertical scaling. 0: The output format of SC is progressive 1: The output format of SC is interlace

1.3.11.2 SC_M_cfg_sc1 Register (offset = 4h) [reset = 0h]

SC_M_cfg_sc1 is shown in Figure 1-475 and described in Table 1-390.

Figure 1-475. SC_M_cfg_sc1 Register

31	30	29	28	27	26	25	24
Reserved					CFG_ROW_ACC_INC		
R-0h					R/W-0h		

23	22	21	20	19	18	17	16
CFG_ROW_ACC_INC							
R/W-0h							

15	14	13	12	11	10	9	8
CFG_ROW_ACC_INC							
R/W-0h							

7	6	5	4	3	2	1	0
CFG_ROW_ACC_INC							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-390. SC_M_cfg_sc1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-0	CFG_ROW_ACC_INC	R/W	0h	This parameter is used by vertical scaling. It defines the increment of the row accumulator in vertical poly-phase filter. It can be calculated by following formula: row_acc_inc = round(2^16 *(src_h)/(tar_h)) In case of interlaced input, srcH is input field height In case of interlaced output, tarH is output field height.

1.3.11.3 SC_M_cfg_sc2 Register (offset = 8h) [reset = 0h]

SC_M_cfg_sc2 is shown in Figure 1-476 and described in Table 1-391.

Figure 1-476. SC_M_cfg_sc2 Register

31	30	29	28	27	26	25	24
Reserved				CFG_ROW_ACC_OFFSET			
R-0h				R/W-0h			

23	22	21	20	19	18	17	16
CFG_ROW_ACC_OFFSET							
R/W-0h							

15	14	13	12	11	10	9	8
CFG_ROW_ACC_OFFSET							
R/W-0h							

7	6	5	4	3	2	1	0
CFG_ROW_ACC_OFFSET							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-391. SC_M_cfg_sc2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	
27-0	CFG_ROW_ACC_OFFSET	R/W	0h	This parameter is used by vertical scaling. It defines the vertical offset during vertical scaling. In progressive mode: this offset will be applied to a frame. In interlace mode: this offset will be applied to the top field.

1.3.11.4 SC_M_cfg_sc3 Register (offset = Ch) [reset = 0h]

SC_M_cfg_sc3 is shown in Figure 1-477 and described in Table 1-392.

Figure 1-477. SC_M_cfg_sc3 Register

31	30	29	28	27	26	25	24
Reserved				CFG_ROW_ACC_OFFSET_B			
R-0h				R/W-0h			

23	22	21	20	19	18	17	16
CFG_ROW_ACC_OFFSET_B							
R/W-0h							

15	14	13	12	11	10	9	8
CFG_ROW_ACC_OFFSET_B							
R/W-0h							

7	6	5	4	3	2	1	0
CFG_ROW_ACC_OFFSET_B							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

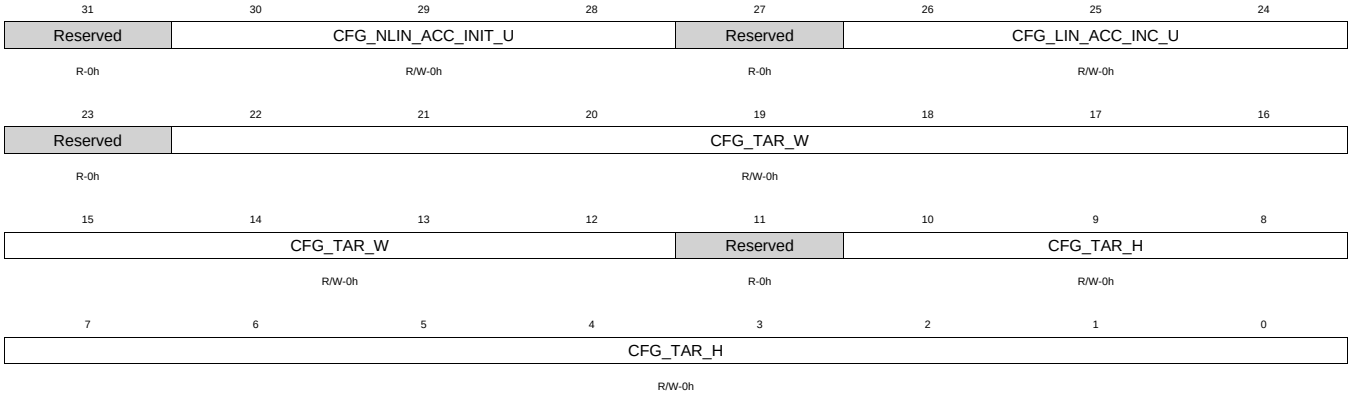
Table 1-392. SC_M_cfg_sc3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	
27-0	CFG_ROW_ACC_OFFSET_B	R/W	0h	This parameter is used by vertical scaling. It defines the vertical offset during vertical scaling. In progressive mode: this parameter will not be used. In interlace mode: this offset will be applied to the bottom field.

1.3.11.5 SC_M_cfg_sc4 Register (offset = 10h) [reset = 0h]

SC_M_cfg_sc4 is shown in Figure 1-478 and described in Table 1-393.

Figure 1-478. SC_M_cfg_sc4 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

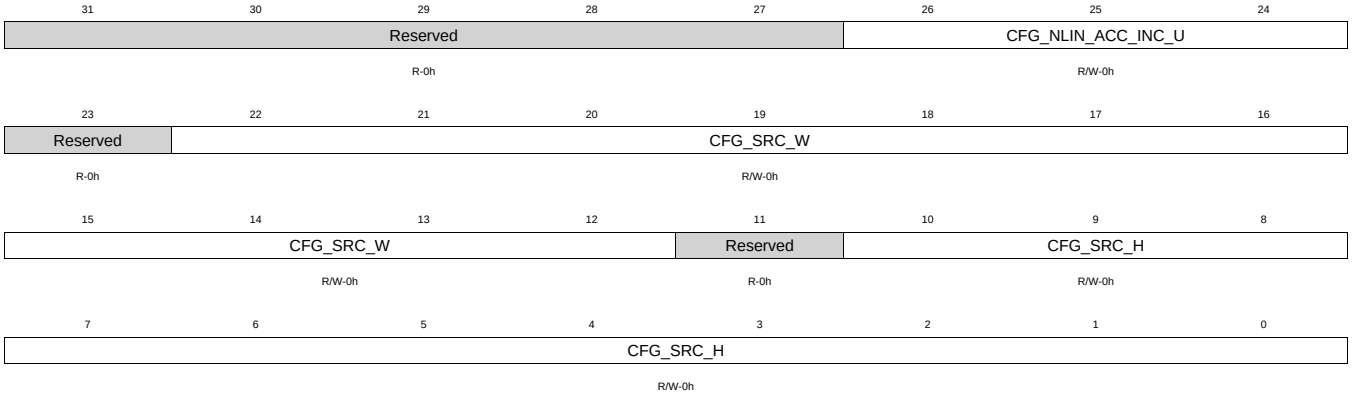
Table 1-393. SC_M_cfg_sc4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Reserved	R	0h	
30-28	CFG_NLIN_ACC_INIT_U	R/W	0h	This parameter is used by horizontal scaling. The 3 MSBbits of 'nlin_acc_init' that is defined in SC_CFG10
27	Reserved	R	0h	
26-24	CFG_LIN_ACC_INC_U	R/W	0h	This parameter is used by horizontal scaling. The 3 MSBbits of 'lin_acc_inc' that is defined in SC_CFG9
23	Reserved	R	0h	
22-12	CFG_TAR_W	R/W	0h	This parameter is a general purpose. Scaled target picture width.. unit is pixel... This parameter defines the final output picture size
11	Reserved	R	0h	
10-0	CFG_TAR_H	R/W	0h	This parameter is a general purpose. Scaled target picture height.. unit is line... This parameter defines the final output picture size. For the interlace output.. it should be the number of lines per field.

1.3.11.6 SC_M_cfg_sc5 Register (offset = 14h) [reset = 0h]

SC_M_cfg_sc5 is shown in Figure 1-479 and described in Table 1-394.

Figure 1-479. SC_M_cfg_sc5 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

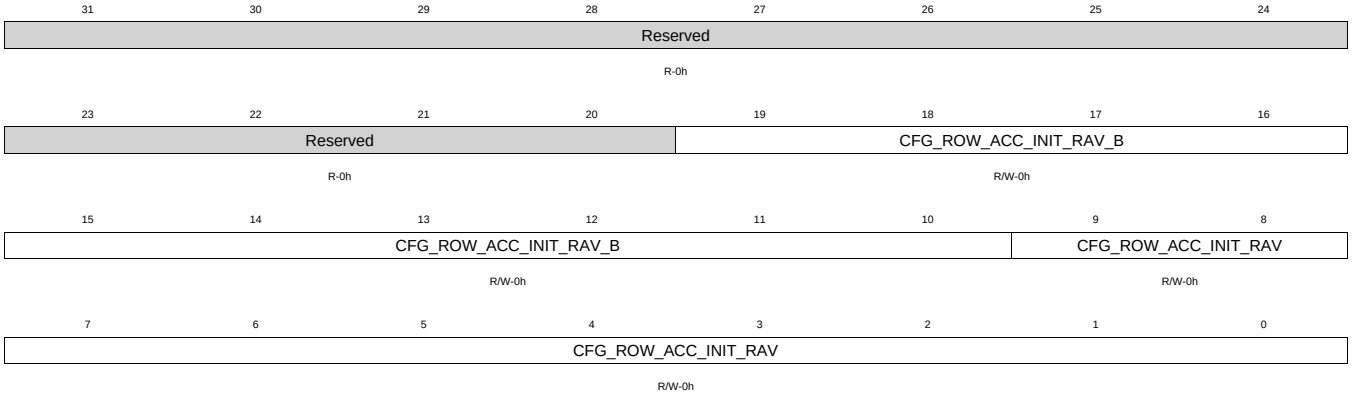
Table 1-394. SC_M_cfg_sc5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-24	CFG_NLIN_ACC_INC_U	R/W	0h	This parameter is used by horizontal scaling. The 3 MSBbits of 'nlin_acc_inc' that is defined in SC_CFG11
23	Reserved	R	0h	
22-12	CFG_SRC_W	R/W	0h	This parameter is a general purpose. This parameter defines the width of the source image
11	Reserved	R	0h	
10-0	CFG_SRC_H	R/W	0h	This parameter is a general purpose. This parameter defines the height of the source image. For the interlace input.. it should be the number of lines per field.

1.3.11.7 SC_M_cfg_sc6 Register (offset = 18h) [reset = 0h]

SC_M_cfg_sc6 is shown in Figure 1-480 and described in Table 1-395.

Figure 1-480. SC_M_cfg_sc6 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

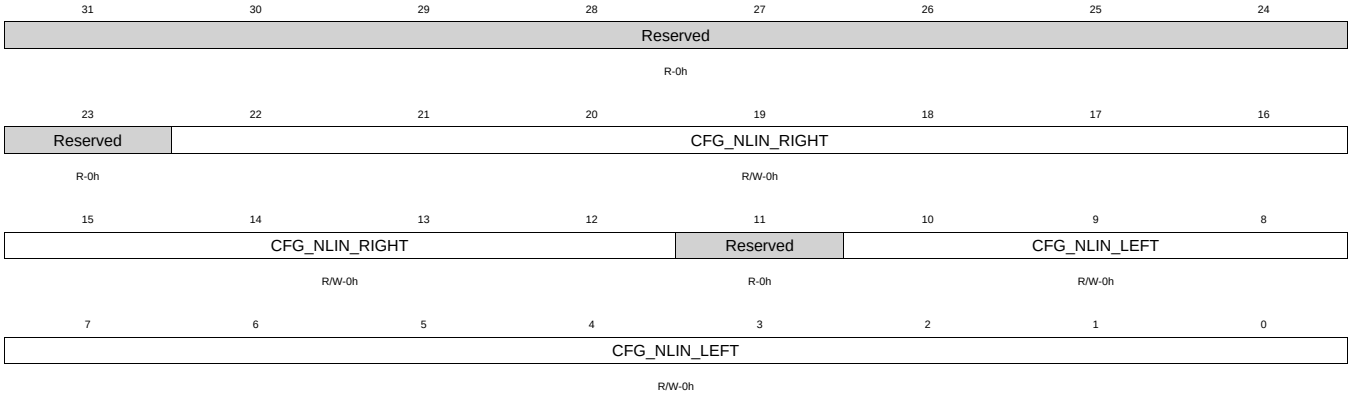
Table 1-395. SC_M_cfg_sc6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	Reserved	R	0h	
19-10	CFG_ROW_ACC_INIT_RAV_B	R/W	0h	This parameter is used by vertical scaling... it is used only when the input is interlace format. In vertical down scaling.. the running average filter is applied. This parameter sets the initialization value of the row accumulator in running average filter (for bottom field of interlace format)
9-0	CFG_ROW_ACC_INIT_RAV	R/W	0h	This parameter is used by vertical scaling. In vertical down scaling.. the running average filter is applied. This parameter sets the initialization value of the row accumulator in running average filter (for progressive format or top field of interlace format)

1.3.11.8 SC_M_cfg_sc8 Register (offset = 20h) [reset = 0h]

SC_M_cfg_sc8 is shown in Figure 1-481 and described in Table 1-396.

Figure 1-481. SC_M_cfg_sc8 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

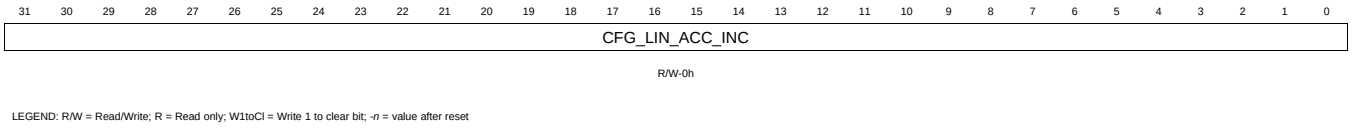
Table 1-396. SC_M_cfg_sc8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	Reserved	R	0h	
22-12	CFG_NLIN_RIGHT	R/W	0h	This parameter is used by horizontal scaling. In anamorphic mode.. this parameter defines the width of the strip on right-hand side. In other words.. it defines the location of the last pixel where the linear scaling is ended. The unit is the 'pixel location' in an active video line. This parameter will not be used in linear scaling
11	Reserved	R	0h	
10-0	CFG_NLIN_LEFT	R/W	0h	This parameter is used by horizontal scaling. In anamorphic mode.. this parameter defines the width of the strip on left-hand side. In other words.. it defines the location of the last pixel in the left-side-nonlinear strip. The unit is the 'pixel location' in an active video line. This parameter will not be used in linear scaling

1.3.11.9 SC_M_cfg_sc9 Register (offset = 24h) [reset = 0h]

SC_M_cfg_sc9 is shown in Figure 1-482 and described in Table 1-397.

Figure 1-482. SC_M_cfg_sc9 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-397. SC_M_cfg_sc9 Register Field Descriptions

Bit	Field	Type	Reset	Description

31-0	CFG_LIN_ACC_INC	R/W	0h	This parameter is used by horizontal scaling. It defines the increment of the linear accumulator.
				if ((cfg_dcm_2x==0) && (cfg_dcm_4x==0)) then lin_acc_inc = round(2^24*(srcWi) /(tarWi))
				if ((cfg_dcm_2x==1) && (cfg_dcm_4x==0)) then lin_acc_inc = round(2^24*(srcWi/2) /(tarWi))
				if ((cfg_dcm_2x==0) && (cfg_dcm_4x==1)) then lin_acc_inc = round(2^24*(srcWi/4) /(tarWi))
				where srcWi and tarWi are the inner source width and the inner target width respectively.

1.3.11.10 SC_M_cfg_sc10 Register (offset = 28h) [reset = 0h]

SC_M_cfg_sc10 is shown in Figure 1-483 and described in Table 1-398.

Figure 1-483. SC_M_cfg_sc10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG_NLIN_ACC_INIT																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-398. SC_M_cfg_sc10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CFG_NLIN_ACC_INIT	R/W	0h	This parameter is used by horizontal scaling. It is used by nonlinear scaling only. It defines the initialization value of the nonlinear accumulator. nlin_acc_init = K*(1-2*d) Here the definitions of K and d are the same as in SC_CFG11

1.3.11.11 SC_M_cfg_sc11 Register (offset = 2Ch) [reset = 0h]

SC_M_cfg_sc11 is shown in Figure 1-484 and described in Table 1-399.

Figure 1-484. SC_M_cfg_sc11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG_NLIN_ACC_INC																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-399. SC_M_cfg_sc11 Register Field Descriptions

Bit	Field	Type	Reset	Description

31-0	CFG_NLIN_ACC_INC	R/W	0h	This parameter is used by horizontal scaling. It is used by nonlinear scaling only. It defines the increment of the nonlinear accumulator.
				if upscaling then
				d = 0
				if Ltar !=0 then
				K =round[2^24*Lsrc/(Ltar*Ltar)]
				where Lsrc= (srcW-srcWi)/2
				else K = 0
				elseif downscaling
				d = (tarW-1)/2
				if Ltar!=0 then K = round[2^24 * Lsrc / (Ltar*(Ltar-2d))]
				where Lsrc= (srcW-srcWi)/(2n) and n=1..2 or 4
				else K = 0
				nlin_acc_inc = 2*K (negative for downscaling)

1.3.11.12 SC_M_cfg_sc12 Register (offset = 30h) [reset = 0h]

SC_M_cfg_sc12 is shown in Figure 1-485 and described in Table 1-400.

Figure 1-485. SC_M_cfg_sc12 Register

31	30	29	28	27	26	25	24
Reserved							CFG_COL_ACC_OFFSET
R-0h							R/W-0h

23	22	21	20	19	18	17	16
CFG_COL_ACC_OFFSET							
R/W-0h							

15	14	13	12	11	10	9	8
CFG_COL_ACC_OFFSET							
R/W-0h							

7	6	5	4	3	2	1	0
CFG_COL_ACC_OFFSET							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

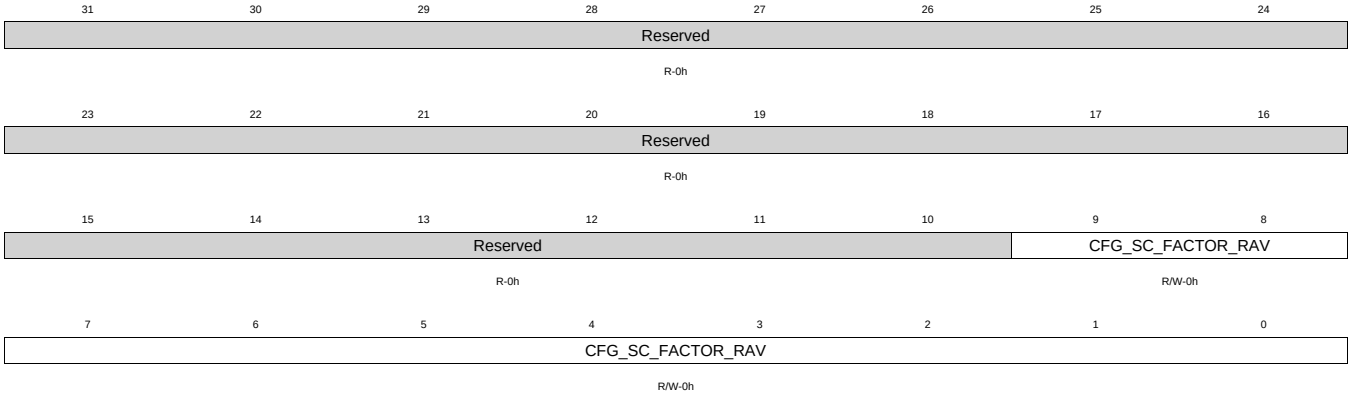
Table 1-400. SC_M_cfg_sc12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	Reserved	R	0h	
24-0	CFG_COL_ACC_OFFSET	R/W	0h	This parameter is used in horizontal scaling. It defines the luma accumulator's offset. Normally this parameter can be set as 0 if no horizontal offset is involved. In some applications.. such as Pan and Scan.. a corresponding offset value should be set. The format is 1.24.

1.3.11.13 SC_M_cfg_sc13 Register (offset = 34h) [reset = 0h]

SC_M_cfg_sc13 is shown in Figure 1-486 and described in Table 1-401.

Figure 1-486. SC_M_cfg_sc13 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-401. SC_M_cfg_sc13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	Reserved	R	0h	
9-0	CFG_SC_FACTOR_RAV	R/W	0h	This parameter is used by vertical scaling. Vertical scaling factor: It is defined as following: 1024*tarH/srcH. It is used for downscaling by the running average filter

1.3.11.14 SC_M_cfg_sc17 Register (offset = 44h) [reset = 0h]

SC_M_cfg_sc17 is shown in Figure 1-487 and described in Table 1-402.

Figure 1-487. SC_M_cfg_sc17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-402. SC_M_cfg_sc17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.11.15 SC_M_cfg_sc18 Register (offset = 48h) [reset = 0h]

SC_M_cfg_sc18 is shown in Figure 1-488 and described in Table 1-403.

Figure 1-488. SC_M_cfg_sc18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-403. SC_M_cfg_sc18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.11.16 SC_M_cfg_sc19 Register (offset = 4Ch) [reset = 0h]

SC_M_cfg_sc19 is shown in Figure 1-489 and described in Table 1-404.

Figure 1-489. SC_M_cfg_sc19 Register

31	30	29	28	27	26	25	24
CFG_HPF_COEF3							
R/W-0h							
23	22	21	20	19	18	17	16
CFG_HPF_COEF2							
R/W-0h							
15	14	13	12	11	10	9	8
CFG_HPF_COEF1							
R/W-0h							
7	6	5	4	3	2	1	0
CFG_HPF_COEF0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

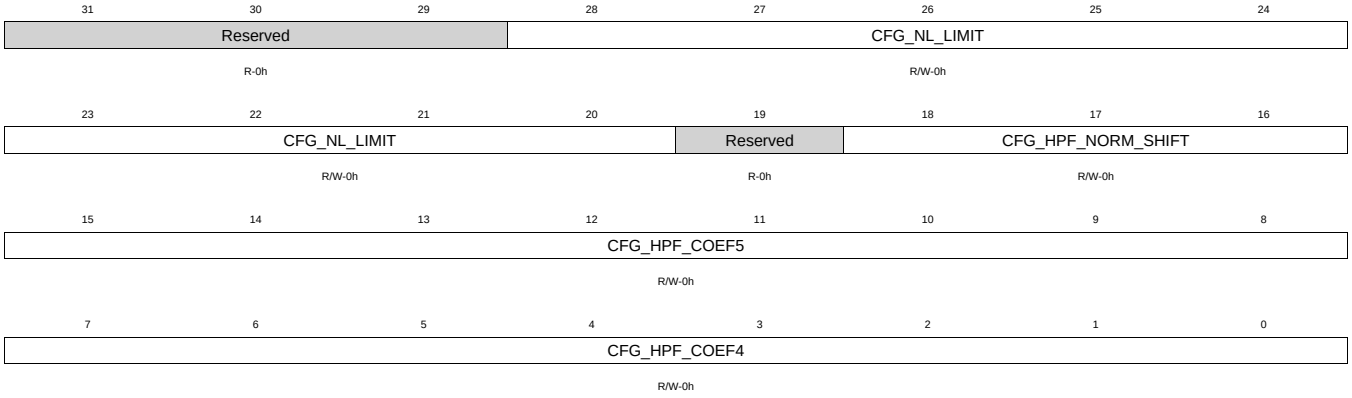
Table 1-404. SC_M_cfg_sc19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CFG_HPF_COEF3	R/W	0h	This parameter is used by the peaking block. Defines the coefficient 3 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.
23-16	CFG_HPF_COEF2	R/W	0h	This parameter is used by the peaking block. Defines the coefficient 2 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.
15-8	CFG_HPF_COEF1	R/W	0h	This parameter is used by the peaking block. Defines the coefficient 1 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.
7-0	CFG_HPF_COEF0	R/W	0h	This parameter is used by the peaking block. Defines the coefficient 0 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm_shift.

1.3.11.17 SC_M_cfg_sc20 Register (offset = 50h) [reset = 0h]

SC_M_cfg_sc20 is shown in Figure 1-490 and described in Table 1-405.

Figure 1-490. SC_M_cfg_sc20 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

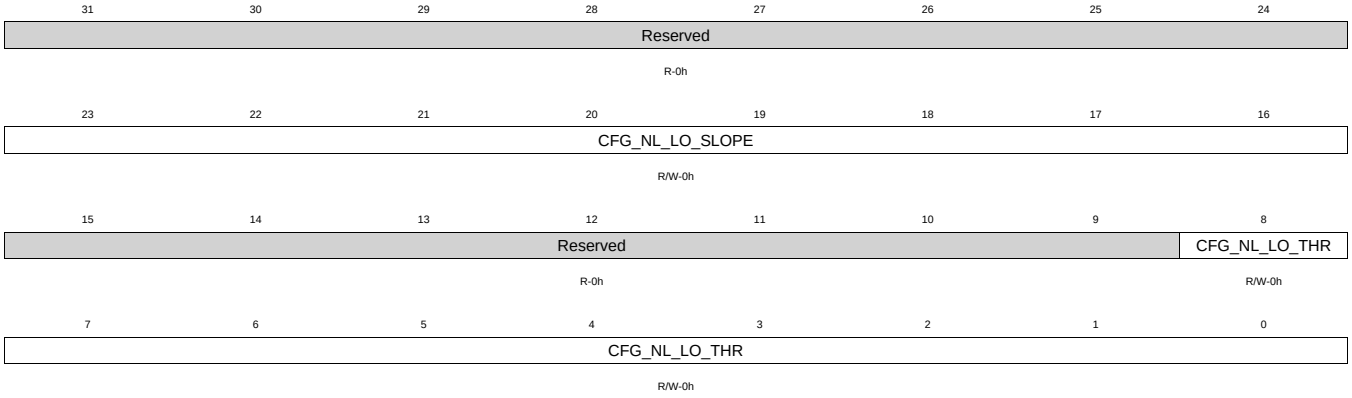
Table 1-405. SC_M_cfg_sc20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-20	CFG_NL_LIMIT	R/W	0h	This parameter is used by the peaking block. The maximum of clipping.
19	Reserved	R	0h	
18-16	CFG_HPF_NORM_SHIFT	R/W	0h	This parameter is used by the peaking block. Defines the decimal point of the hpf coefficient.
15-8	CFG_HPF_COEF5	R/W	0h	This parameter is used by the peaking block. Defines the coefficient 5 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm.
7-0	CFG_HPF_COEF4	R/W	0h	This parameter is used by the peaking block. Defines the coefficient 4 of the HPF used in the peaking filter. Signed. Decimal point is defined by hpf_norm.

1.3.11.18 SC_M_cfg_sc21 Register (offset = 54h) [reset = 0h]

SC_M_cfg_sc21 is shown in Figure 1-491 and described in Table 1-406.

Figure 1-491. SC_M_cfg_sc21 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

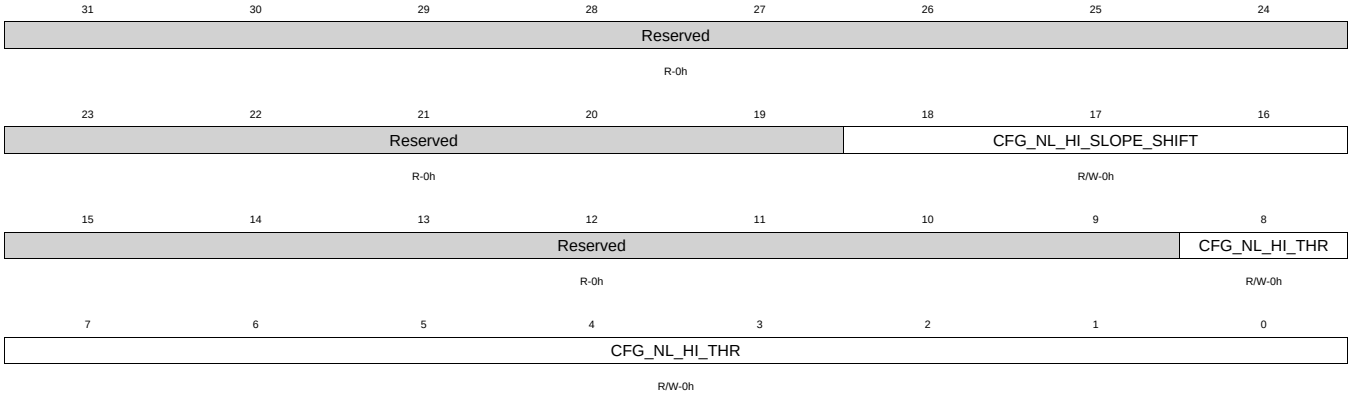
Table 1-406. SC_M_cfg_sc21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	
23-16	CFG_NL_LO_SLOPE	R/W	0h	This parameter is used by the peaking block. Slope of the nonlinear peaking function. The format is fixed point 4.4.
15-9	Reserved	R	0h	
8-0	CFG_NL_LO_THR	R/W	0h	This parameter is used by the peaking block. Threshold for the nonlinear peaking function. Must be 0

1.3.11.19 SC_M_cfg_sc22 Register (offset = 58h) [reset = 0h]

SC_M_cfg_sc22 is shown in Figure 1-492 and described in Table 1-407.

Figure 1-492. SC_M_cfg_sc22 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-407. SC_M_cfg_sc22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	Reserved	R	0h	
18-16	CFG_NL_HI_SLOPE_SHIFT	R/W	0h	This parameter is used by the peaking block. Slope of the nonlinear peaking function. The gain is 2^(nl_hi_slope_shift-3).
15-9	Reserved	R	0h	
8-0	CFG_NL_HI_THR	R/W	0h	This parameter is used by the peaking block. Threshold for the nonlinear peaking function. Must be nl_hi_thr.

1.3.11.20 SC_M_cfg_sc23 Register (offset = 5Ch) [reset = 0h]

SC_M_cfg_sc23 is shown in Figure 1-493 and described in Table 1-408.

Figure 1-493. SC_M_cfg_sc23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

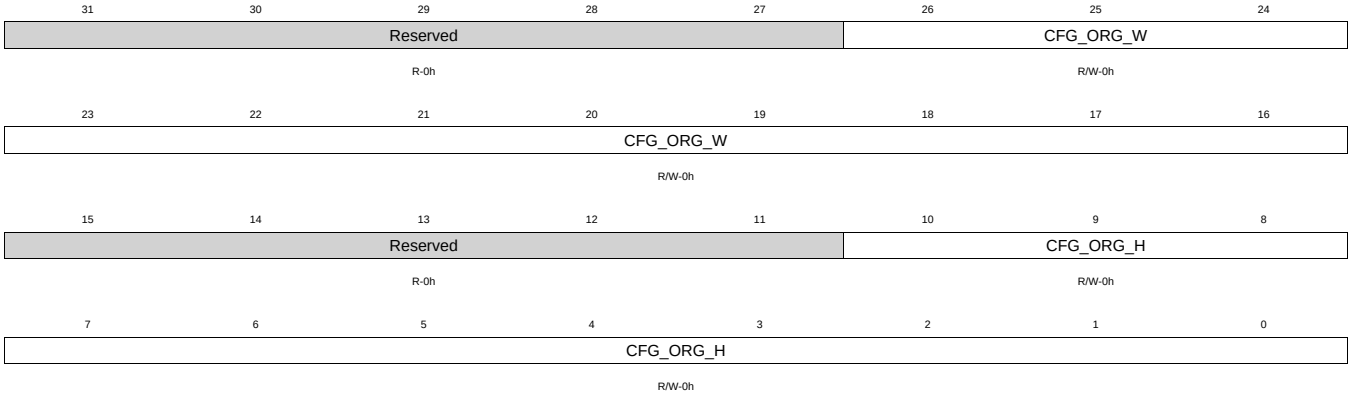
Table 1-408. SC_M_cfg_sc23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Reserved	R	0h	Reserved

1.3.11.21 SC_M_cfg_sc24 Register (offset = 60h) [reset = 0h]

SC_M_cfg_sc24 is shown in Figure 1-494 and described in Table 1-409.

Figure 1-494. SC_M_cfg_sc24 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

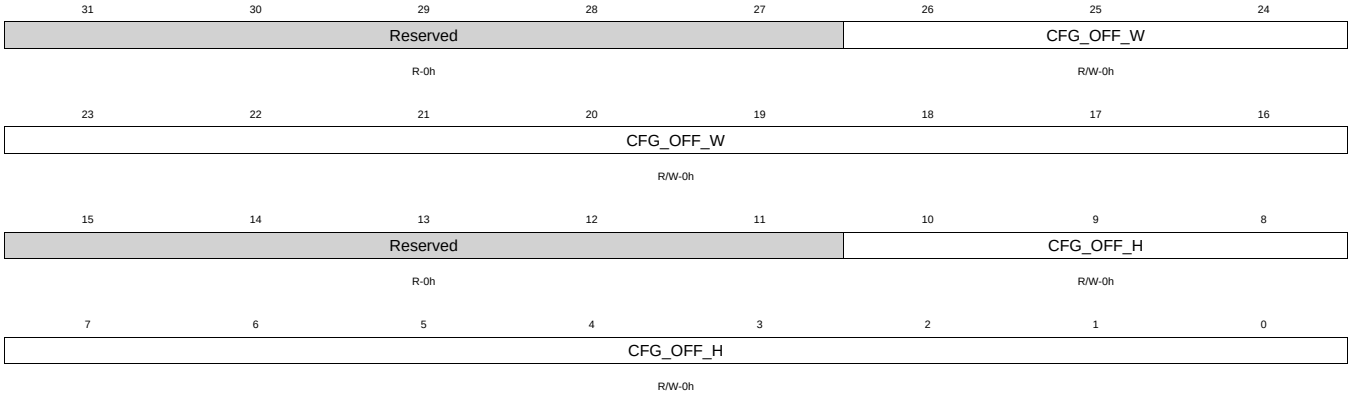
Table 1-409. SC_M_cfg_sc24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	CFG_ORG_W	R/W	0h	This parameter is used by the trimmer. Width of the original input image.
15-11	Reserved	R	0h	
10-0	CFG_ORG_H	R/W	0h	This parameter is used by the trimmer. Height of the original input image.

1.3.11.22 SC_M_cfg_sc25 Register (offset = 64h) [reset = 0h]

SC_M_cfg_sc25 is shown in Figure 1-495 and described in Table 1-410.

Figure 1-495. SC_M_cfg_sc25 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-410. SC_M_cfg_sc25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	CFG_OFF_W	R/W	0h	This parameter is used by the trimmer. Horizontal offset from the left of the original input image.
15-11	Reserved	R	0h	
10-0	CFG_OFF_H	R/W	0h	This parameter is used by the trimmer. Vertical offset from the top of the original input image.

1.3.12 SD_VENC Registers

Table 1-411 lists the memory-mapped registers for the SD_VENC. All register offset addresses not listed in Table 1-411 should be considered as reserved locations and the register contents should not be modified.

Table 1-411. SD_VENC REGISTERS

Offset	Acronym	Register Name	Section
0h	SD_VENC_pid	Revision Register	Section 1.3.12.1
4h	SD_VENC_vmod	VENC Mode	Section 1.3.12.2
8h	SD_VENC_slave	Slave Control	Section 1.3.12.3
Ch	SD_VENC_size	Picture Size	Section 1.3.12.4
10h	SD_VENC_pol	Polarity	Section 1.3.12.5
14h	SD_VENC_dtvs0	DTV Sync Timing 0	Section 1.3.12.6
18h	SD_VENC_dtvs1	DTV Sync Timing 1	Section 1.3.12.7
1Ch	SD_VENC_dtvs2	DTV Sync Timing 2	Section 1.3.12.8
20h	SD_VENC_dtvs3	DTV Sync Timing 3	Section 1.3.12.9
24h	SD_VENC_dtvs4	DTV Sync Timing 4	Section 1.3.12.10
28h	SD_VENC_dtvs5	DTV Sync Timing 5	Section 1.3.12.11
2Ch	SD_VENC_dtvs6	DTV Sync Timing 6	Section 1.3.12.12
30h	SD_VENC_dtvs7	DTV Sync Timing 7	Section 1.3.12.13
54h	SD_VENC_tvdetgp0	TVDETGP Timing 0	Section 1.3.12.14
58h	SD_VENC_tvdetgp1	TVDETGP Timing 1	Section 1.3.12.15
5Ch	SD_VENC_irq0	IRQ Timing	Section 1.3.12.16
80h	SD_VENC_estat	Encoder Status	Section 1.3.12.17
84h	SD_VENC_ectl	Encoder Control	Section 1.3.12.18
88h	SD_VENC_etmg0	Encoder Timing 0	Section 1.3.12.19
8Ch	SD_VENC_etmg1	Encoder Timing 1	Section 1.3.12.20
90h	SD_VENC_etmg2	Encoder Timing 2	Section 1.3.12.21
94h	SD_VENC_etmg3	Encoder Timing 3	Section 1.3.12.22
98h	SD_VENC_etmg4	Encoder Timing 4	Section 1.3.12.23
9Ch	SD_VENC_cvbs0	CVBS Control 0	Section 1.3.12.24
A0h	SD_VENC_cvbs1	CVBS Control 1	Section 1.3.12.25
ACh	SD_VENC_ccsc0	CVBS Color Space Conversion 0	Section 1.3.12.26
B0h	SD_VENC_ccsc1	CVBS Color Space Conversion 1	Section 1.3.12.27
B4h	SD_VENC_ccsc2	CVBS Color Space Conversion 2	Section 1.3.12.28
B8h	SD_VENC_ccsc3	CVBS Color Space Conversion 3	Section 1.3.12.29
BCh	SD_VENC_ccsc4	CVBS Color Space Conversion 4	Section 1.3.12.30
C0h	SD_VENC_ccsc5	CVBS Color Space Conversion 5	Section 1.3.12.31
C4h	SD_VENC_ccsc6	CVBS Color Space Conversion 6	Section 1.3.12.32
C8h	SD_VENC_ccsc7	CVBS Color Space Conversion 7	Section 1.3.12.33
CCh	SD_VENC_ccsc8	CVBS Color Space Conversion 8	Section 1.3.12.34
F4h	SD_VENC_cygclp	CVBS Y Clip	Section 1.3.12.35
F8h	SD_VENC_cubclp	CVBS U Clip	Section 1.3.12.36
FCh	SD_VENC_cvrclp	CVBS V Clip	Section 1.3.12.37
10Ch	SD_VENC_ylpf0	CVBS Luma LPF Coefficient 0	Section 1.3.12.38
110h	SD_VENC_ylpf1	CVBS Luma LPF Coefficient 1	Section 1.3.12.39
114h	SD_VENC_clpf0	CVBS Chroma LPF Coefficient 0	Section 1.3.12.40
118h	SD_VENC_clpf1	CVBS Chroma LPF Coefficient 1	Section 1.3.12.41
11Ch	SD_VENC_upf0	2x Upsampling Coefficient 0	Section 1.3.12.42
120h	SD_VENC_upf1	2x Upsampling Coefficient 1	Section 1.3.12.43

Table 1-411. SD_VENC REGISTERS (continued)

Offset	Acronym	Register Name	Section
124h	SD_VENC_l21ctl	Line 21 Control	Section 1.3.12.44
128h	SD_VENC_l21do	Line 21 Data Even Field	Section 1.3.12.45
12Ch	SD_VENC_l21de	Line 21 Data Odd Field	Section 1.3.12.46
130h	SD_VENC_wss	WSS Control	Section 1.3.12.47
148h	SD_VENC_scctl0	Sub-carrier Frequency Control 0	Section 1.3.12.48
14Ch	SD_VENC_scctl1	Sub-carrier Frequency Control 1	Section 1.3.12.49
150h	SD_VENC_dacsel	DAC Output Signal Select	Section 1.3.12.50
154h	SD_VENC_dupf0	DAC 2x Upsampling Coefficient 0	Section 1.3.12.51
158h	SD_VENC_dupf1	DAC 2x Upsampling Coefficient 1	Section 1.3.12.52
15Ch	SD_VENC_dactst	DAC Test Mode	Section 1.3.12.53
1FCh	SD_VENC_vtest	Internal Test Register	Section 1.3.12.54

1.3.12.1 SD_VENC_pid Register (offset = 0h) [reset = 4FFF0000h]

SD_VENC_pid is shown in Figure 1-496 and described in Table 1-412.

Revision Register

Figure 1-496. SD_VENC_pid Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID																															
R-4FFF0000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-412. SD_VENC_pid Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID	R	4FFF0000h	Revision ID.

1.3.12.2 SD_VENC_vmod Register (offset = 4h) [reset = 4h]

SD_VENC_vmod is shown in Figure 1-497 and described in Table 1-413.

VENC Mode

Figure 1-497. SD_VENC_vmod Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
Reserved		DIIV	CBAR	UEL	ITLC	Reserved	VIEN
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-1h	R-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-413. SD_VENC_vmod Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	Reserved	R	0h	Reserved
5	DIIV	R/W	0h	Input data inversion 0: No inversion 1: Input inverted
4	CBAR	R/W	0h	Color-bar mode 0: Normal output 1: Color-bar output
3	UEL	R/W	0h	Unequal line per field. When 1, the line per field alternately toggles between (VITV-1)/2 and (VITV+1)/2. When 0, the line per field is always VITV/2. Effective in interlace mode (ITLC=1). 0: Normal 1: Unequal lines per field.
2	ITLC	R/W	1h	Scan mode. 0: Progressive 1: Interlace
1	Reserved	R	0h	Reserved
0	VIEN	R/W	0h	Video encoder enable. Setting 1 brings this module into operation. Setting 0 resets internal circuits in this module. 0: Video encoder reset 1: Video encoder enable

1.3.12.3 SD_VENC_slave Register (offset = 8h) [reset = 0h]

SD_VENC_slave is shown in Figure 1-498 and described in Table 1-414.

Slave Control

Figure 1-498. SD_VENC_slave Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved		FMD		FIP	VIP	HIP	SLV
R-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-414. SD_VENC_slave Register Field Descriptions

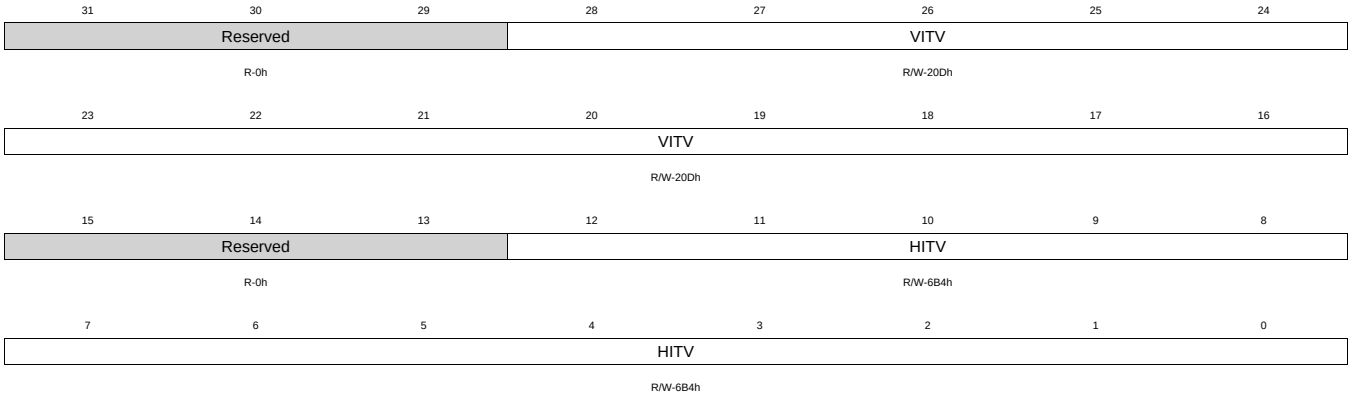
Bit	Field	Type	Reset	Description
31-6	Reserved	R	0h	
5-4	FMD	R/W	0h	Field detection mode. Effective in slave operation (SLAVE=1). 0: latch external field at external vsync rise edge. 1: use raw external field 2: use external vsync as field ID 3: detect external vsync phase
3	FIP	R/W	0h	FID input polarity. Effective in slave operation (SLAVE=1). External field signal is inverted at EXFEN=1. 0: Non-inverse 1: Inverse
2	VIP	R/W	0h	VSYNC input polarity. Effective in slave operation (SLAVE=1). 0: Active H 1: Active L
1	HIP	R/W	0h	HSYNC input polarity. Effective in slave operation (SLAVE=1). 0: Active H 1: Active L
0	SLV	R/W	0h	Master/slave select. Set 1 to operate this module in slave mode in synchronization with external sync signal. 0: Master mode 1: Slave mode

1.3.12.4 SD_VENC_size Register (offset = Ch) [reset = 020D06B4h]

SD_VENC_size is shown in Figure 1-499 and described in Table 1-415.

Picture Size

Figure 1-499. SD_VENC_size Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-415. SD_VENC_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	VITV	R/W	20Dh	Vertical interval. Specify the number of lines per frame.
15-13	Reserved	R	0h	
12-0	HITV	R/W	6B4h	Horizontal interval. Specify the number of clocks per line.

1.3.12.5 SD_VENC_pol Register (offset = 10h) [reset = 0h]

SD_VENC_pol is shown in Figure 1-500 and described in Table 1-416.

Polarity

Figure 1-500. SD_VENC_pol Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							TVDETGP_POL
R-0h							R/W-0h
7	6	5	4	3	2	1	0
Reserved				DTV_AVID_POL	DTV_FID_POL	DTV_VS_POL	DTV_HS_POL
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-416. SD_VENC_pol Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	Reserved	R	0h	
8	TVDETGP_POL	R/W	0h	TVDETGP output polarity. 0: Active H 1: Active L
7-4	Reserved	R	0h	
3	DTV_AVID_POL	R/W	0h	DTV AVID output polarity. 0: Active H 1: Active L
2	DTV_FID_POL	R/W	0h	DTV FID output polarity 0: Non-inverse 1: Inverse
1	DTV_VS_POL	R/W	0h	DTV VSYNC output polarity. 0: Active H 1: Active L
0	DTV_HS_POL	R/W	0h	DTV HSYNC output polarity 0: Active H 1: Active L

1.3.12.6 SD_VENC_dtvs0 Register (offset = 14h) [reset = 0h]

SD_VENC_dtvs0 is shown in Figure 1-501 and described in Table 1-417.

DTV Sync Timing 0

Figure 1-501. SD_VENC_dtvs0 Register

31	30	29	28	27	26	25	24
Reserved			DTV_HS_H_STP				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
DTV_HS_H_STP							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			DTV_HS_H_STA				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
DTV_HS_H_STA							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-417. SD_VENC_dtvs0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	DTV_HS_H_STP	R/W	0h	DTV HSYNC output stop pixel.
15-13	Reserved	R	0h	
12-0	DTV_HS_H_STA	R/W	0h	DTV HSYNC output start pixel.

1.3.12.7 SD_VENC_dtvs1 Register (offset = 18h) [reset = 0h]

SD_VENC_dtvs1 is shown in Figure 1-502 and described in Table 1-418.

DTV Sync Timing 1

Figure 1-502. SD_VENC_dtvs1 Register

31	30	29	28	27	26	25	24
Reserved			DTV_VS_H_STP				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
DTV_VS_H_STP							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			DTV_VS_H_STA				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
DTV_VS_H_STA							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-418. SD_VENC_dtvs1 Register Field Descriptions

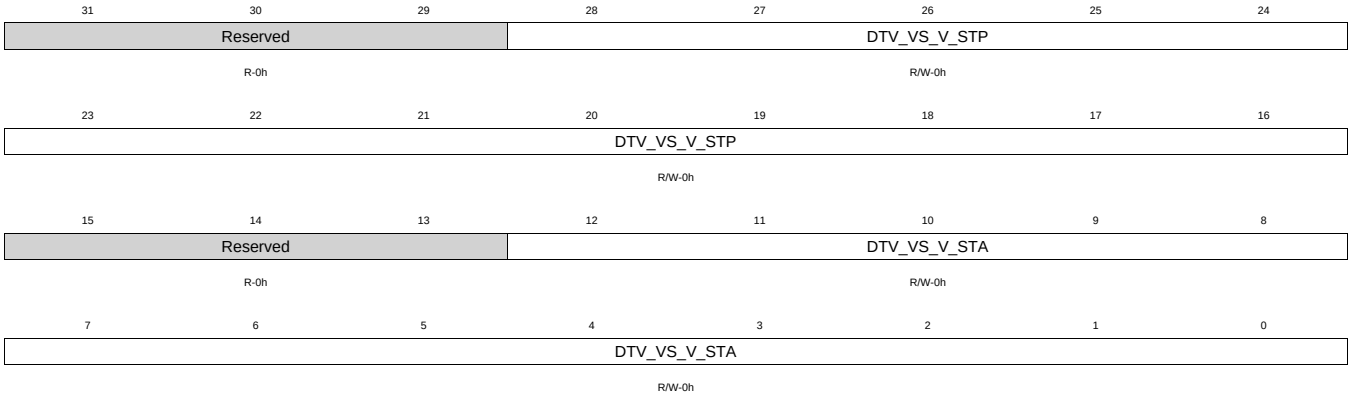
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	DTV_VS_H_STP	R/W	0h	DTV VSYNC output stop pixel.
15-13	Reserved	R	0h	
12-0	DTV_VS_H_STA	R/W	0h	DTV VSYNC output start pixel.

1.3.12.8 SD_VENC_dtvs2 Register (offset = 1Ch) [reset = 0h]

SD_VENC_dtvs2 is shown in Figure 1-503 and described in Table 1-419.

DTV Sync Timing 2

Figure 1-503. SD_VENC_dtvs2 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-419. SD_VENC_dtvs2 Register Field Descriptions

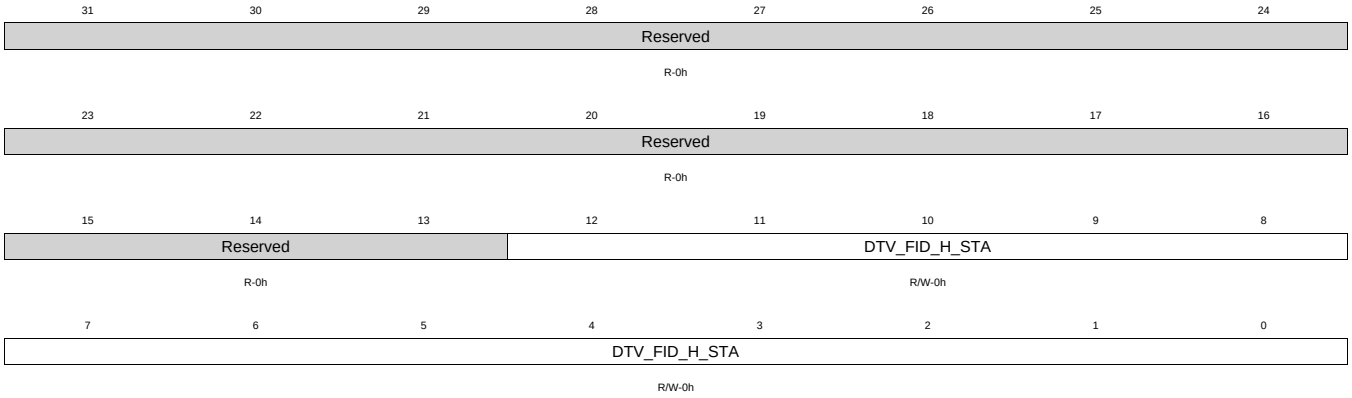
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	DTV_VS_V_STP	R/W	0h	DTV VSYNC output stop line.
15-13	Reserved	R	0h	
12-0	DTV_VS_V_STA	R/W	0h	DTV VSYNC output start line.

1.3.12.9 SD_VENC_dtvs3 Register (offset = 20h) [reset = 0h]

SD_VENC_dtvs3 is shown in Figure 1-504 and described in Table 1-420.

DTV Sync Timing 3

Figure 1-504. SD_VENC_dtvs3 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-420. SD_VENC_dtvs3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	Reserved	R	0h	
12-0	DTV_FID_H_STA	R/W	0h	DTV FID output toggle pixel position.

1.3.12.10 SD_VENC_dtvs4 Register (offset = 24h) [reset = 20000000h]

SD_VENC_dtvs4 is shown in Figure 1-505 and described in Table 1-421.

DTV Sync Timing 4

Figure 1-505. SD_VENC_dtvs4 Register

31	30	29	28	27	26	25	24
Reserved		DTV_FID_F_STA1	DTV_FID_V_STA1				
R-0h		R/W-1h	R/W-0h				
23	22	21	20	19	18	17	16
DTV_FID_V_STA1							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved		DTV_FID_F_STA0	DTV_FID_V_STA0				
R-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
DTV_FID_V_STA0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-421. SD_VENC_dtvs4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Reserved	R	0h	
29	DTV_FID_F_STA1	R/W	1h	DTV FID output start field for fid=1.
28-16	DTV_FID_V_STA1	R/W	0h	DTV FID output start line for fid=1.
15-14	Reserved	R	0h	
13	DTV_FID_F_STA0	R/W	0h	DTV FID output start field for fid=0. Optionally works as force FID toggle enable in progressive or non-interlace mode.
12-0	DTV_FID_V_STA0	R/W	0h	DTV FID output start line for fid=0.

1.3.12.11 SD_VENC_dtvs5 Register (offset = 28h) [reset = 0h]

SD_VENC_dtvs5 is shown in Figure 1-506 and described in Table 1-422.

DTV Sync Timing 5

Figure 1-506. SD_VENC_dtvs5 Register

31	30	29	28	27	26	25	24
Reserved			DTV_AVID_H_STP				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
DTV_AVID_H_STP							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			DTV_AVID_H_STA				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
DTV_AVID_H_STA							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-422. SD_VENC_dtvs5 Register Field Descriptions

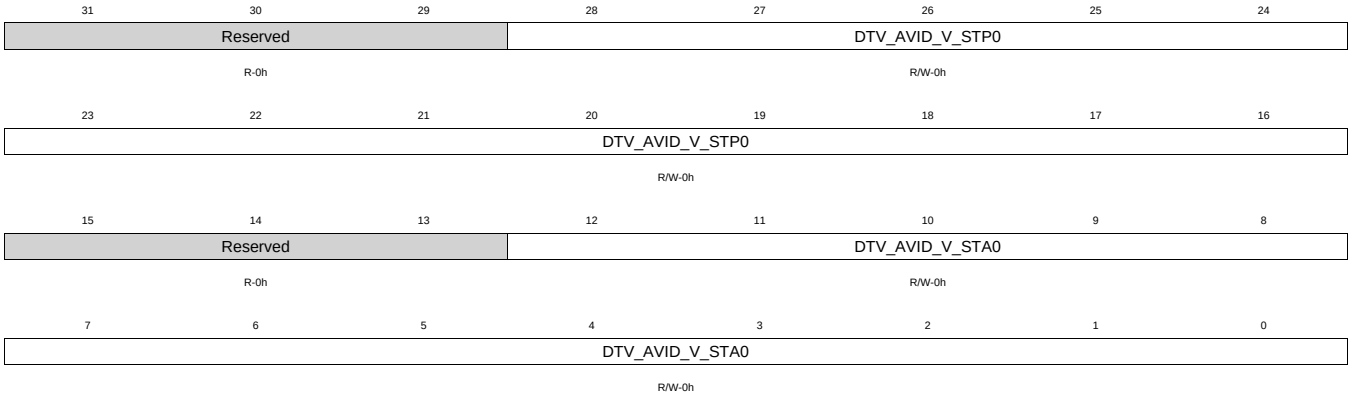
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	DTV_AVID_H_STP	R/W	0h	DTV AVID output stop pixel.
15-13	Reserved	R	0h	
12-0	DTV_AVID_H_STA	R/W	0h	DTV AVID output start pixel.

1.3.12.12 SD_VENC_dtvs6 Register (offset = 2Ch) [reset = 0h]

SD_VENC_dtvs6 is shown in Figure 1-507 and described in Table 1-423.

DTV Sync Timing 6

Figure 1-507. SD_VENC_dtvs6 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-423. SD_VENC_dtvs6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	DTV_AVID_V_STP0	R/W	0h	DTV AVID output stop line for fid=0.
15-13	Reserved	R	0h	
12-0	DTV_AVID_V_STA0	R/W	0h	DTV AVID output start line for fid=0.

1.3.12.13 SD_VENC_dtvs7 Register (offset = 30h) [reset = 0h]

SD_VENC_dtvs7 is shown in Figure 1-508 and described in Table 1-424.

DTV Sync Timing 7

Figure 1-508. SD_VENC_dtvs7 Register

31	30	29	28	27	26	25	24
Reserved			DTV_AVID_V_STP1				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
DTV_AVID_V_STP1							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			DTV_AVID_V_STA1				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
DTV_AVID_V_STA1							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-424. SD_VENC_dtvs7 Register Field Descriptions

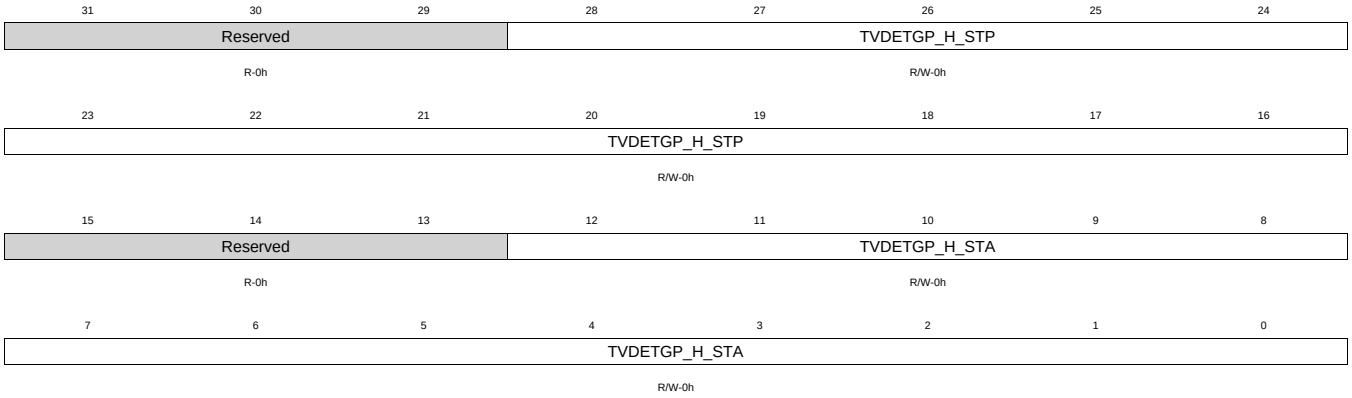
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	DTV_AVID_V_STP1	R/W	0h	DTV AVID output stop line for fid=1.
15-13	Reserved	R	0h	
12-0	DTV_AVID_V_STA1	R/W	0h	DTV AVID output start line for fid=1.

1.3.12.14 SD_VENC_tvdetgp0 Register (offset = 54h) [reset = 0h]

SD_VENC_tvdetgp0 is shown in Figure 1-509 and described in Table 1-425.

TVDETGP Timing 0

Figure 1-509. SD_VENC_tvdetgp0 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-425. SD_VENC_tvdetgp0 Register Field Descriptions

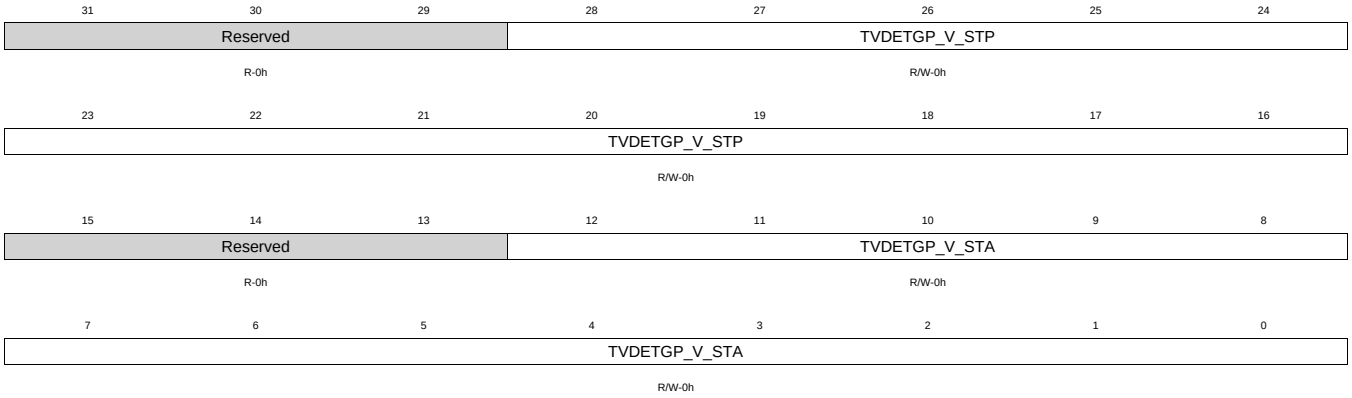
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	TVDETGP_H_STP	R/W	0h	TVDETGP output stop pixel.
15-13	Reserved	R	0h	
12-0	TVDETGP_H_STA	R/W	0h	TVDETGP output start pixel.

1.3.12.15 SD_VENC_tvdetgp1 Register (offset = 58h) [reset = 0h]

SD_VENC_tvdetgp1 is shown in Figure 1-510 and described in Table 1-426.

TVDETGP Timing 1

Figure 1-510. SD_VENC_tvdetgp1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-426. SD_VENC_tvdetgp1 Register Field Descriptions

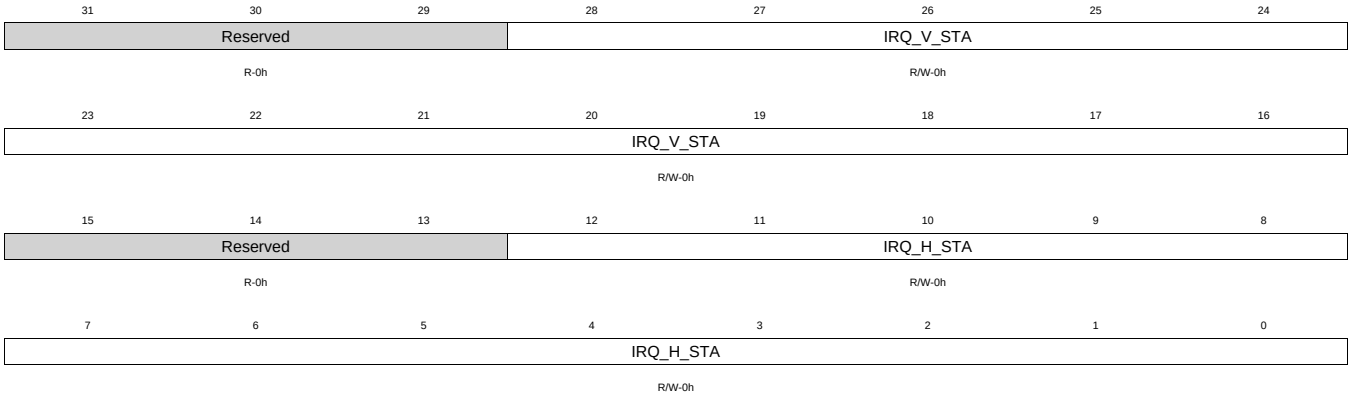
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	TVDETGP_V_STP	R/W	0h	TVDETGP output stop line.
15-13	Reserved	R	0h	
12-0	TVDETGP_V_STA	R/W	0h	TVDETGP output start line.

1.3.12.16 SD_VENC_irq0 Register (offset = 5Ch) [reset = 0h]

SD_VENC_irq0 is shown in Figure 1-511 and described in Table 1-427.

IRQ Timing

Figure 1-511. SD_VENC_irq0 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-427. SD_VENC_irq0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	IRQ_V_STA	R/W	0h	IRQ output start line
15-13	Reserved	R	0h	
12-0	IRQ_H_STA	R/W	0h	IRQ output start pixel.

1.3.12.17 SD_VENC_estat Register (offset = 80h) [reset = 0h]

SD_VENC_estat is shown in Figure 1-512 and described in Table 1-428.

Encoder Status

Figure 1-512. SD_VENC_estat Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved			FIDST	Reserved		CAEST	CAOST
R-0h			R-0h	R-0h		R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-428. SD_VENC_estat Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	Reserved	R	0h	
4	FIDST	R	0h	Field ID monitor.
3-2	Reserved	R	0h	
1	CAEST	R	0h	Closed caption status (even field). This bit shows 0 when caption data register (L21DE) is ready to be input.. and changes to 1 when data is written to L21DE. This bit is automatically cleared to 0 when a caption data transmission is completed on the line 284(NTSC) or 335(PAL) in even field.
0	CAOST	R	0h	Closed caption status (odd field). This bit shows 0 when caption data register (L21DO) is ready to be input.. and changes to 1 when data is written to L21DO. This bit is automatically cleared to 0 when a caption data transmission is completed on the line 21(NTSC) or 22(PAL) in odd field.

1.3.12.18 SD_VENC_ectl Register (offset = 84h) [reset = 0h]

SD_VENC_ectl is shown in Figure 1-513 and described in Table 1-429.

Encoder Control

Figure 1-513. SD_VENC_ectl Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved				FMT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
Reserved	PXLR	VBIEN	BLS	SVSW	DUPS	UPS	GAM
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-429. SD_VENC_ectl Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	Reserved	R	0h	
11-8	FMT	R/W	0h	TV scan format select. 0: 525i 1: 625i 2-15: Reserved
7	Reserved	R	0h	
6	PXLR	R/W	0h	Pixel rate. Set 0 when the pixel rate is half of the VENC clock. It is used to determine the internal pipeline delay alignment. 0: 1x 1: 2x
5	VBIEN	R/W	0h	VBI enable. 0: Off 1: On
4	BLS	R/W	0h	Blanking shape disable. When 1.. blanking shaping feature is disabled. 0: Enable 1: Disable
3	SVSW	R/W	0h	SD vertical sync width 0: 3H 1: 2.5H
2	DUPS	R/W	0h	DAC 2x oversampling enable. 0: Off 1: On
1	UPS	R/W	0h	2x up-sampling enable. 0: Off 1: On
0	GAM	R/W	0h	Gamma correction 0: Off 1: On

1.3.12.19 SD_VENC_etmg0 Register (offset = 88h) [reset = 069400F4h]

SD_VENC_etmg0 is shown in Figure 1-514 and described in Table 1-430.

Encoder Timing 0

Figure 1-514. SD_VENC_etmg0 Register

31	30	29	28	27	26	25	24
Reserved			AV_H_STP				
R-0h			R/W-694h				
23	22	21	20	19	18	17	16
AV_H_STP							
R/W-694h							
15	14	13	12	11	10	9	8
Reserved			AV_H_STA				
R-0h			R/W-F4h				
7	6	5	4	3	2	1	0
AV_H_STA							
R/W-F4h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-430. SD_VENC_etmg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	AV_H_STP	R/W	694h	Active video horizontal stop position.
15-13	Reserved	R	0h	
12-0	AV_H_STA	R/W	F4h	Active video horizontal start position.

1.3.12.20 SD_VENC_etmg1 Register (offset = 8Ch) [reset = 02070022h]

SD_VENC_etmg1 is shown in Figure 1-515 and described in Table 1-431.

Encoder Timing 1

Figure 1-515. SD_VENC_etmg1 Register

31	30	29	28	27	26	25	24
Reserved			AV_V_STP0				
R-0h			R/W-207h				
23	22	21	20	19	18	17	16
AV_V_STP0							
R/W-207h							
15	14	13	12	11	10	9	8
Reserved			AV_V_STA0				
R-0h			R/W-22h				
7	6	5	4	3	2	1	0
AV_V_STA0							
R/W-22h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-431. SD_VENC_etmg1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	AV_V_STP0	R/W	207h	Active video vertical stop position for fid=0.
15-13	Reserved	R	0h	
12-0	AV_V_STA0	R/W	22h	Active video vertical start position for fid=0.

1.3.12.21 SD_VENC_etmg2 Register (offset = 90h) [reset = 02070022h]

SD_VENC_etmg2 is shown in Figure 1-516 and described in Table 1-432.

Encoder Timing 2

Figure 1-516. SD_VENC_etmg2 Register

31	30	29	28	27	26	25	24
Reserved			AV_V_STP1				
R-0h			R/W-207h				
23	22	21	20	19	18	17	16
AV_V_STP1							
R/W-207h							
15	14	13	12	11	10	9	8
Reserved			AV_V_STA1				
R-0h			R/W-22h				
7	6	5	4	3	2	1	0
AV_V_STA1							
R/W-22h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-432. SD_VENC_etmg2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	AV_V_STP1	R/W	207h	Active video vertical stop position for fid=1.
15-13	Reserved	R	0h	
12-0	AV_V_STA1	R/W	22h	Active video vertical start position for fid=1.

1.3.12.22 SD_VENC_etmg3 Register (offset = 94h) [reset = 00D3008Fh]

SD_VENC_etmg3 is shown in Figure 1-517 and described in Table 1-433.

Encoder Timing 3

Figure 1-517. SD_VENC_etmg3 Register

31	30	29	28	27	26	25	24
Reserved							BST_H_STP
R-0h							R/W-D3h

23	22	21	20	19	18	17	16
BST_H_STP							
R/W-D3h							

15	14	13	12	11	10	9	8
Reserved							BST_H_STA
R-0h							R/W-8Fh

7	6	5	4	3	2	1	0
BST_H_STA							
R/W-8Fh							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-433. SD_VENC_etmg3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	Reserved	R	0h	
24-16	BST_H_STP	R/W	D3h	Color burst stop position.
15-9	Reserved	R	0h	
8-0	BST_H_STA	R/W	8Fh	Color burst start position.

1.3.12.23 SD_VENC_etmg4 Register (offset = 98h) [reset = 0h]

SD_VENC_etmg4 is shown in Figure 1-518 and described in Table 1-434.

Encoder Timing 4

Figure 1-518. SD_VENC_etmg4 Register

31	30	29	28	27	26	25	24
Reserved			VBI_H_STP				
R-0h			R/W-0h				

23	22	21	20	19	18	17	16
VBI_H_STP							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved			VBI_H_STA				
R-0h			R/W-0h				

7	6	5	4	3	2	1	0
VBI_H_STA							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-434. SD_VENC_etmg4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	VBI_H_STP	R/W	0h	VBI request stop position.
15-13	Reserved	R	0h	
12-0	VBI_H_STA	R/W	0h	VBI request start position.

1.3.12.24 SD_VENC_cvbs0 Register (offset = 9Ch) [reset = 034400BCh]

SD_VENC_cvbs0 is shown in Figure 1-519 and described in Table 1-435.

CVBS Control 0

Figure 1-519. SD_VENC_cvbs0 Register

31	30	29	28	27	26	25	24
Reserved				CSLVL			
R-0h				R/W-344h			

23	22	21	20	19	18	17	16
CSLVL							
R/W-344h							

15	14	13	12	11	10	9	8
Reserved				CTLVL			
R-0h				R/W-BCh			

7	6	5	4	3	2	1	0
CTLVL							
R/W-BCh							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-435. SD_VENC_cvbs0 Register Field Descriptions

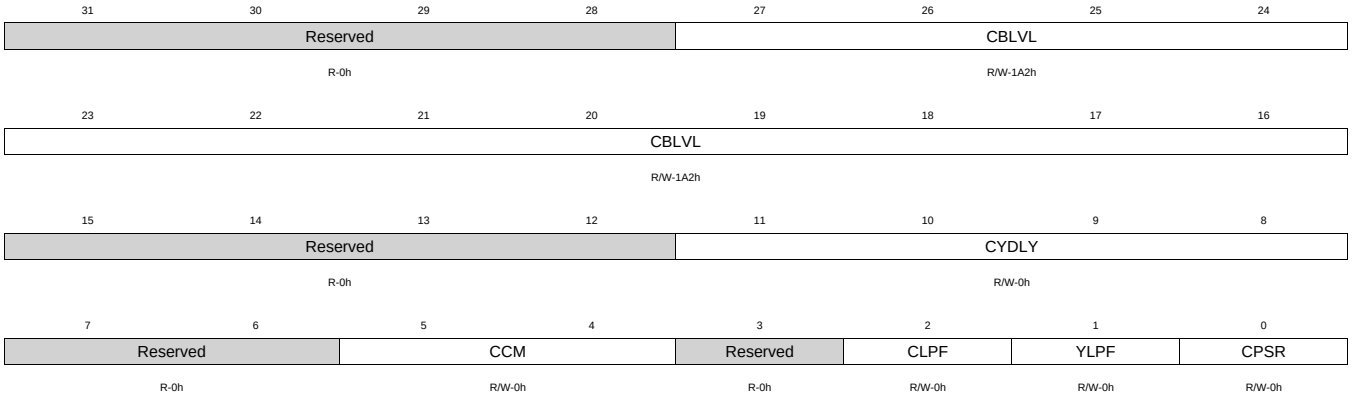
Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	
27-16	CSLVL	R/W	344h	CVBS sync amplitude.
15-12	Reserved	R	0h	
11-0	CTLVL	R/W	BCh	CVBS sync-tip amplitude.

1.3.12.25 SD_VENC_cvbs1 Register (offset = A0h) [reset = 01A20000h]

SD_VENC_cvbs1 is shown in Figure 1-520 and described in Table 1-436.

CVBS Control 1

Figure 1-520. SD_VENC_cvbs1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-436. SD_VENC_cvbs1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	
27-16	CBLVL	R/W	1A2h	CVBS burst amplitude.
15-12	Reserved	R	0h	
11-8	CYDLY	R/W	0h	CVBS Y delay adjustment. s3.0
7-6	Reserved	R	0h	
5-4	CCM	R/W	0h	CVBS color modulation mode 0: NTSC 1: PAL 2: SECAM 3: Reserved
3	Reserved	R	0h	
2	CLPF	R/W	0h	CVBS chroma LPF enable 0: Off 1: On
1	YLPF	R/W	0h	CVBS luma LPF enable 0: Off 1: On
0	CPSR	R/W	0h	CVBS picture sync ratio 0: 10:4 1: 7:3

1.3.12.26 SD_VENC_ccsc0 Register (offset = ACh) [reset = 0037011Dh]

SD_VENC_ccsc0 is shown in Figure 1-521 and described in Table 1-437.

CVBS Color Space Conversion 0

Figure 1-521. SD_VENC_ccsc0 Register

31	30	29	28	27	26	25	24
Reserved			CCSCB0				
R-0h			R/W-37h				
23	22	21	20	19	18	17	16
CCSCB0							
R/W-37h							
15	14	13	12	11	10	9	8
Reserved			CCSCA0				
R-0h			R/W-11Dh				
7	6	5	4	3	2	1	0
CCSCA0							
R/W-11Dh							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-437. SD_VENC_ccsc0 Register Field Descriptions

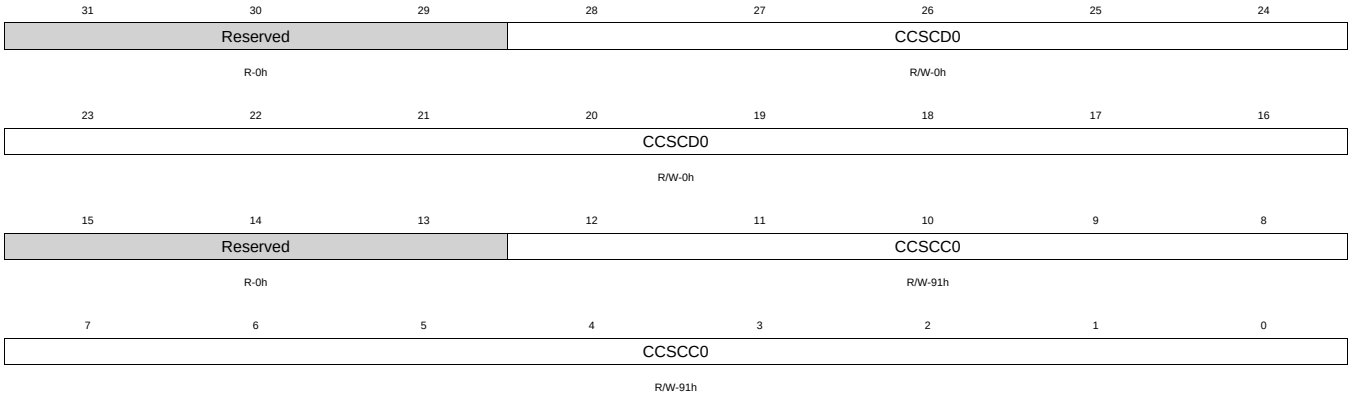
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CCSCB0	R/W	37h	Coefficients of color space converter for CVBS. s6.6
15-13	Reserved	R	0h	
12-0	CCSCA0	R/W	11Dh	Coefficients of color space converter for CVBS. s6.6

1.3.12.27 SD_VENC_ccsc1 Register (offset = B0h) [reset = 00000091h]

SD_VENC_ccsc1 is shown in Figure 1-522 and described in Table 1-438.

CVBS Color Space Conversion 1

Figure 1-522. SD_VENC_ccsc1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-438. SD_VENC_ccsc1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CCSCD0	R/W	0h	Coefficients of color space converter for CVBS. s8.4
15-13	Reserved	R	0h	
12-0	CCSCC0	R/W	91h	Coefficients of color space converter for CVBS. s6.6

1.3.12.28 SD_VENC_ccsc2 Register (offset = B4h) [reset = 0000009Dh]

SD_VENC_ccsc2 is shown in Figure 1-523 and described in Table 1-439.

CVBS Color Space Conversion 2

Figure 1-523. SD_VENC_ccsc2 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved			CCSCE0				
R-0h			R/W-9Dh				
7	6	5	4	3	2	1	0
CCSCE0							
R/W-9Dh							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-439. SD_VENC_ccsc2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	Reserved	R	0h	
12-0	CCSCE0	R/W	9Dh	Coefficients of color space converter for CVBS. s12.0

1.3.12.29 SD_VENC_ccsc3 Register (offset = B8h) [reset = 00D31F74h]

SD_VENC_ccsc3 is shown in Figure 1-524 and described in Table 1-440.

CVBS Color Space Conversion 3

Figure 1-524. SD_VENC_ccsc3 Register

31	30	29	28	27	26	25	24
Reserved			CCSCB1				
R-0h			R/W-D3h				
23	22	21	20	19	18	17	16
CCSCB1							
R/W-D3h							
15	14	13	12	11	10	9	8
Reserved			CCSCA1				
R-7h			R/W-1F74h				
7	6	5	4	3	2	1	0
CCSCA1							
R/W-1F74h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-440. SD_VENC_ccsc3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CCSCB1	R/W	D3h	Coefficients of color space converter for CVBS. s6.6
15-13	Reserved	R	7h	
12-0	CCSCA1	R/W	1F74h	Coefficients of color space converter for CVBS. s6.6

1.3.12.30 SD_VENC_ccsc4 Register (offset = BCh) [reset = 00001FB9h]

SD_VENC_ccsc4 is shown in Figure 1-525 and described in Table 1-441.

CVBS Color Space Conversion 4

Figure 1-525. SD_VENC_ccsc4 Register

31	30	29	28	27	26	25	24
Reserved			CCSCD1				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
CCSCD1							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			CCSCC1				
R-0h			R/W-1FB9h				
7	6	5	4	3	2	1	0
CCSCC1							
R/W-1FB9h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-441. SD_VENC_ccsc4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CCSCD1	R/W	0h	Coefficients of color space converter for CVBS. s8.4
15-13	Reserved	R	0h	
12-0	CCSCC1	R/W	1FB9h	Coefficients of color space converter for CVBS. s6.6

1.3.12.31 SD_VENC_ccsc5 Register (offset = C0h) [reset = 0h]

SD_VENC_ccsc5 is shown in Figure 1-526 and described in Table 1-442.

CVBS Color Space Conversion 5

Figure 1-526. SD_VENC_ccsc5 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved			CCSCE1				
R-0h			R/W-0h				

7	6	5	4	3	2	1	0
CCSCE1							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-442. SD_VENC_ccsc5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	Reserved	R	0h	
12-0	CCSCE1	R/W	0h	Coefficients of color space converter for CVBS. s12.0

1.3.12.32 SD_VENC_ccsc6 Register (offset = C4h) [reset = 1FD01F06h]

SD_VENC_ccsc6 is shown in Figure 1-527 and described in Table 1-443.

CVBS Color Space Conversion 6

Figure 1-527. SD_VENC_ccsc6 Register

31	30	29	28	27	26	25	24
Reserved			CCSCB2				
R-0h			R/W-1FD0h				
23	22	21	20	19	18	17	16
CCSCB2							
R/W-1FD0h							
15	14	13	12	11	10	9	8
Reserved			CCSCA2				
R-0h			R/W-1F06h				
7	6	5	4	3	2	1	0
CCSCA2							
R/W-1F06h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-443. SD_VENC_ccsc6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CCSCB2	R/W	1FD0h	Coefficients of color space converter for CVBS. s6.6
15-13	Reserved	R	0h	
12-0	CCSCA2	R/W	1F06h	Coefficients of color space converter for CVBS. s6.6

1.3.12.33 SD_VENC_ccsc7 Register (offset = C8h) [reset = 0000012Ah]

SD_VENC_ccsc7 is shown in Figure 1-528 and described in Table 1-444.

CVBS Color Space Conversion 7

Figure 1-528. SD_VENC_ccsc7 Register

31	30	29	28	27	26	25	24
Reserved			CCSCD2				
R-0h			R/W-0h				
23	22	21	20	19	18	17	16
CCSCD2							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved			CCSCC2				
R-0h			R/W-12Ah				
7	6	5	4	3	2	1	0
CCSCC2							
R/W-12Ah							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-444. SD_VENC_ccsc7 Register Field Descriptions

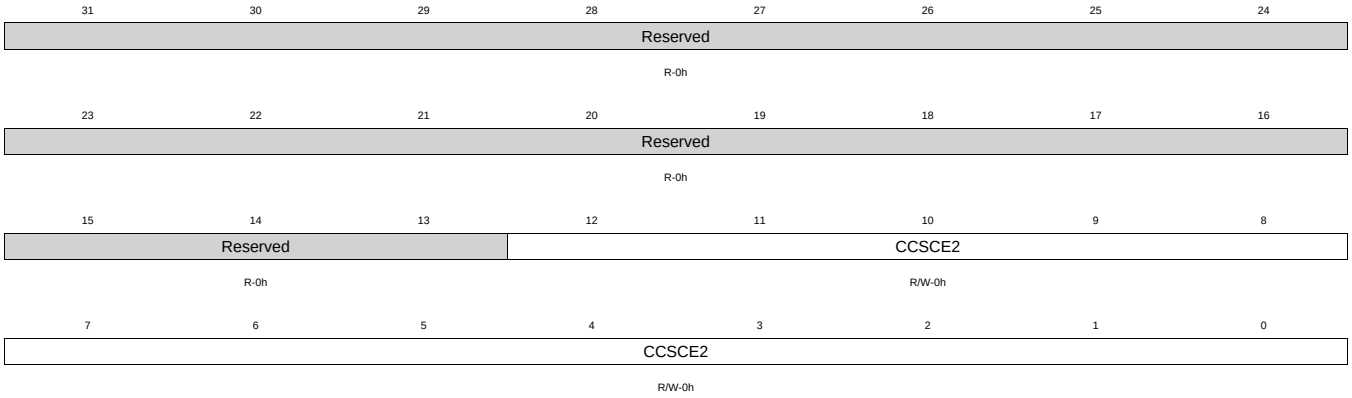
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CCSCD2	R/W	0h	Coefficients of color space converter for CVBS. s8.4
15-13	Reserved	R	0h	
12-0	CCSCC2	R/W	12Ah	Coefficients of color space converter for CVBS. s6.6

1.3.12.34 SD_VENC_ccsc8 Register (offset = CCh) [reset = 0h]

SD_VENC_ccsc8 is shown in Figure 1-529 and described in Table 1-445.

CVBS Color Space Conversion 8

Figure 1-529. SD_VENC_ccsc8 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-445. SD_VENC_ccsc8 Register Field Descriptions

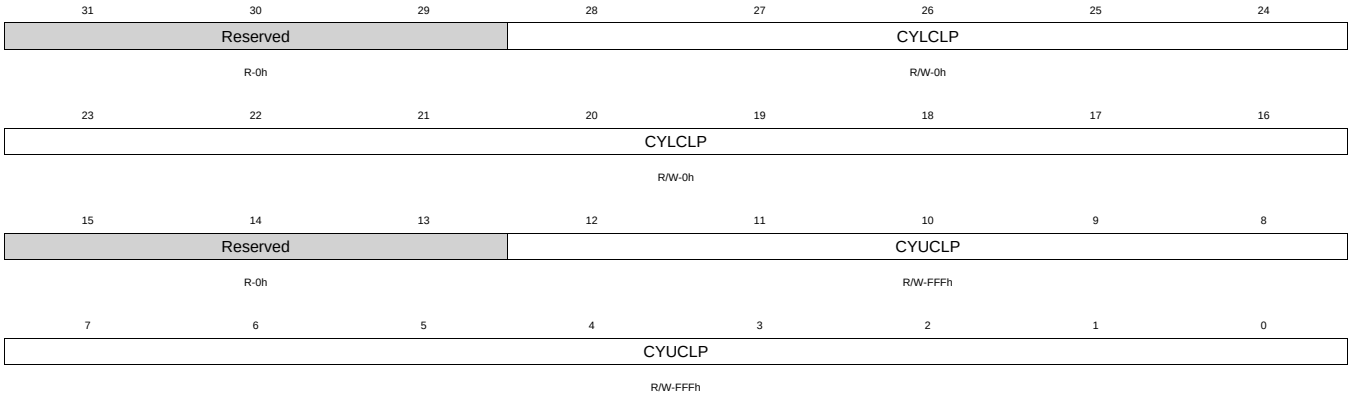
Bit	Field	Type	Reset	Description
31-13	Reserved	R	0h	
12-0	CCSCE2	R/W	0h	Coefficients of color space converter for CVBS. s12.0

1.3.12.35 SD_VENC_cygclp Register (offset = F4h) [reset = 00000FFFh]

SD_VENC_cygclp is shown in Figure 1-530 and described in Table 1-446.

CVBS Y Clip

Figure 1-530. SD_VENC_cygclp Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-446. SD_VENC_cygclp Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CYLCLP	R/W	0h	CVBS Y Lower Limit. s12.0
15-13	Reserved	R	0h	
12-0	CYUCLP	R/W	FFFh	CVBS Y Upper Limit. s12.0

1.3.12.36 SD_VENC_cubclp Register (offset = F8h) [reset = 180007FFh]

SD_VENC_cubclp is shown in Figure 1-531 and described in Table 1-447.

CVBS U Clip

Figure 1-531. SD_VENC_cubclp Register

31	30	29	28	27	26	25	24
Reserved			CULCLP				
R-0h			R/W-1800h				
23	22	21	20	19	18	17	16
CULCLP							
R/W-1800h							
15	14	13	12	11	10	9	8
Reserved			CUUCLP				
R-0h			R/W-7FFh				
7	6	5	4	3	2	1	0
CUUCLP							
R/W-7FFh							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-447. SD_VENC_cubclp Register Field Descriptions

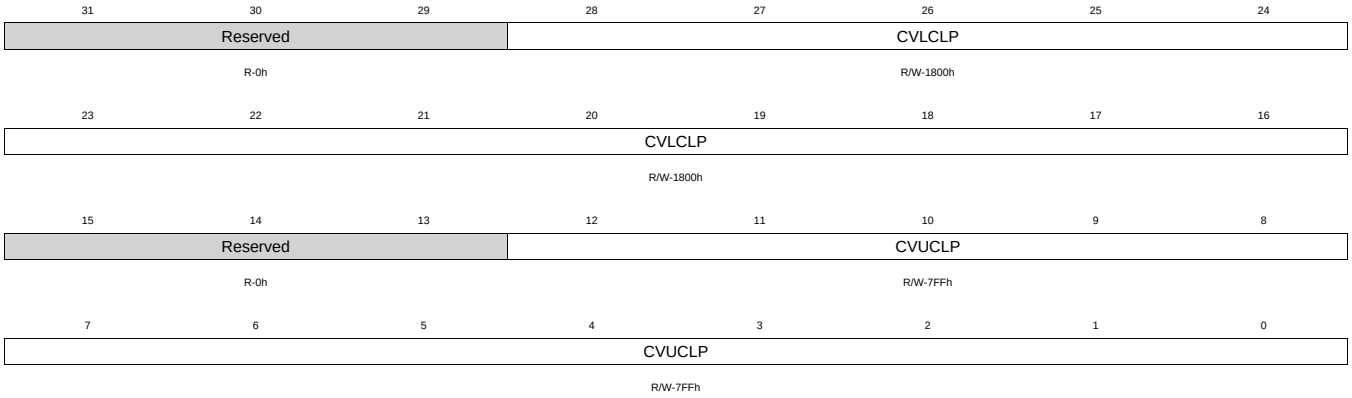
Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CULCLP	R/W	1800h	CVBS U Lower Limit. s12.0
15-13	Reserved	R	0h	
12-0	CUUCLP	R/W	7FFh	CVBS U Upper Limit. s12.0

1.3.12.37 SD_VENC_cvrclp Register (offset = FCh) [reset = 180007FFh]

SD_VENC_cvrclp is shown in Figure 1-532 and described in Table 1-448.

CVBS V Clip

Figure 1-532. SD_VENC_cvrclp Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-448. SD_VENC_cvrclp Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28-16	CVLCLP	R/W	1800h	CVBS V Lower Limit. s12.0
15-13	Reserved	R	0h	
12-0	CVUCLP	R/W	7FFh	CVBS V Vpper Limit. s12.0

1.3.12.38 SD_VENC_ylpf0 Register (offset = 10Ch) [reset = 0h]

SD_VENC_ylpf0 is shown in Figure 1-533 and described in Table 1-449.

CVBS Luma LPF Coefficient 0

Figure 1-533. SD_VENC_ylpf0 Register

31	30	29	28	27	26	25	24
YLPFC3							
R/W-0h							
23	22	21	20	19	18	17	16
YLPFC2							
R/W-0h							
15	14	13	12	11	10	9	8
YLPFC1							
R/W-0h							
7	6	5	4	3	2	1	0
YLPFC0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-449. SD_VENC_ylpf0 Register Field Descriptions

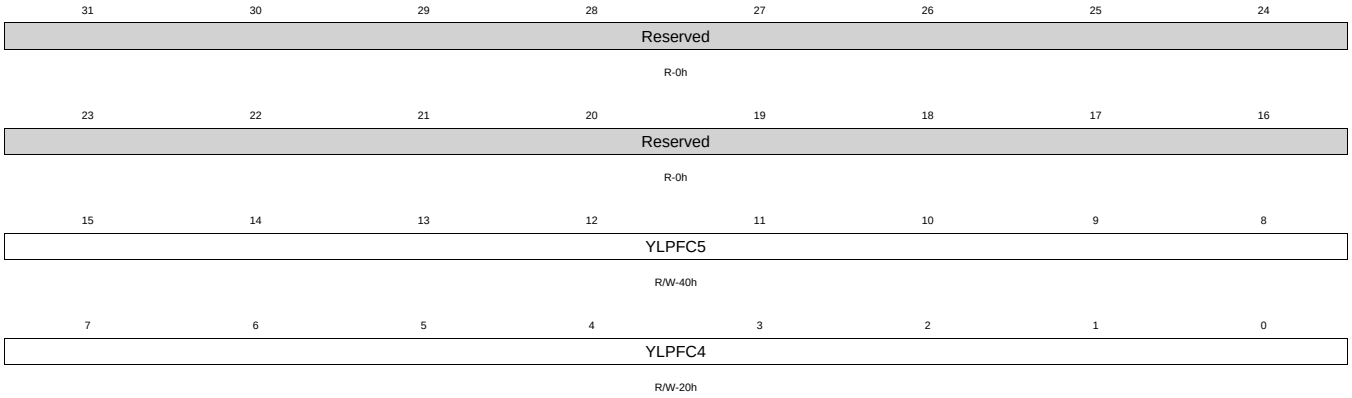
Bit	Field	Type	Reset	Description
31-24	YLPFC3	R/W	0h	Luma LPF coefficient 3. s0.7.
23-16	YLPFC2	R/W	0h	Luma LPF coefficient 2. s0.7.
15-8	YLPFC1	R/W	0h	Luma LPF coefficient 1. s0.7.
7-0	YLPFC0	R/W	0h	Luma LPF coefficient 0. s0.7.

1.3.12.39 SD_VENC_ylpf1 Register (offset = 110h) [reset = 00004020h]

SD_VENC_ylpf1 is shown in Figure 1-534 and described in Table 1-450.

CVBS Luma LPF Coefficient 1

Figure 1-534. SD_VENC_ylpf1 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-450. SD_VENC_ylpf1 Register Field Descriptions

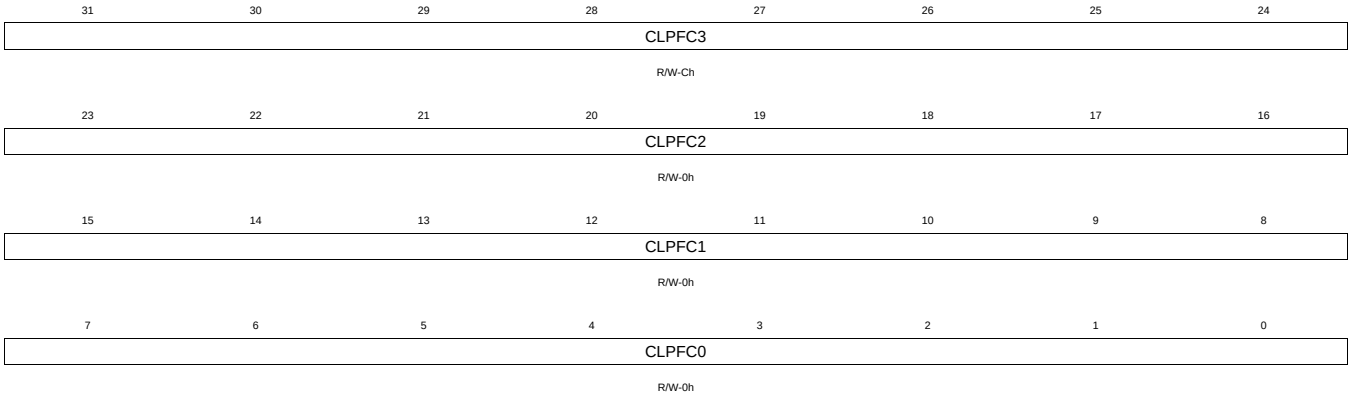
Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	
15-8	YLPFC5	R/W	40h	Luma LPF coefficient 5. s0.7.
7-0	YLPFC4	R/W	20h	Luma LPF coefficient 4. s0.7.

1.3.12.40 SD_VENC_clpf0 Register (offset = 114h) [reset = 0C000000h]

SD_VENC_clpf0 is shown in Figure 1-535 and described in Table 1-451.

CVBS Chroma LPF Coefficient 0

Figure 1-535. SD_VENC_clpf0 Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-451. SD_VENC_clpf0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CLPFC3	R/W	Ch	Chroma LPF coefficient 3. s0.7.
23-16	CLPFC2	R/W	0h	Chroma LPF coefficient 2. s0.7.
15-8	CLPFC1	R/W	0h	Chroma LPF coefficient 1. s0.7.
7-0	CLPFC0	R/W	0h	Chroma LPF coefficient 0. s0.7.

1.3.12.41 SD_VENC_clpf1 Register (offset = 118h) [reset = 00002820h]

SD_VENC_clpf1 is shown in Figure 1-536 and described in Table 1-452.

CVBS Chroma LPF Coefficient 1

Figure 1-536. SD_VENC_clpf1 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
CLPFC5							
R/W-28h							

7	6	5	4	3	2	1	0
CLPFC4							
R/W-20h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-452. SD_VENC_clpf1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	
15-8	CLPFC5	R/W	28h	Chroma LPF coefficient 5. s0.7.
7-0	CLPFC4	R/W	20h	Chroma LPF coefficient 4. s0.7.

1.3.12.42 SD_VENC_upf0 Register (offset = 11Ch) [reset = 0h]

SD_VENC_upf0 is shown in Figure 1-537 and described in Table 1-453.

2x Upsampling Coefficient 0

Figure 1-537. SD_VENC_upf0 Register

31	30	29	28	27	26	25	24
UPFC3							
R/W-0h							
23	22	21	20	19	18	17	16
UPFC2							
R/W-0h							
15	14	13	12	11	10	9	8
UPFC1							
R/W-0h							
7	6	5	4	3	2	1	0
UPFC0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-453. SD_VENC_upf0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	UPFC3	R/W	0h	2x up-sampling filter coefficient 3. s0.7.
23-16	UPFC2	R/W	0h	2x up-sampling filter coefficient 2. s0.7.
15-8	UPFC1	R/W	0h	2x up-sampling filter coefficient 1. s0.7.
7-0	UPFC0	R/W	0h	2x up-sampling filter coefficient 0. s0.7.

1.3.12.43 SD_VENC_upf1 Register (offset = 120h) [reset = 004EEC06h]

SD_VENC_upf1 is shown in Figure 1-538 and described in Table 1-454.

2x Upsampling Coefficient 1

Figure 1-538. SD_VENC_upf1 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
UPFC6							
R/W-4Eh							
15	14	13	12	11	10	9	8
UPFC5							
R/W-ECh							
7	6	5	4	3	2	1	0
UPFC4							
R/W-6h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-454. SD_VENC_upf1 Register Field Descriptions

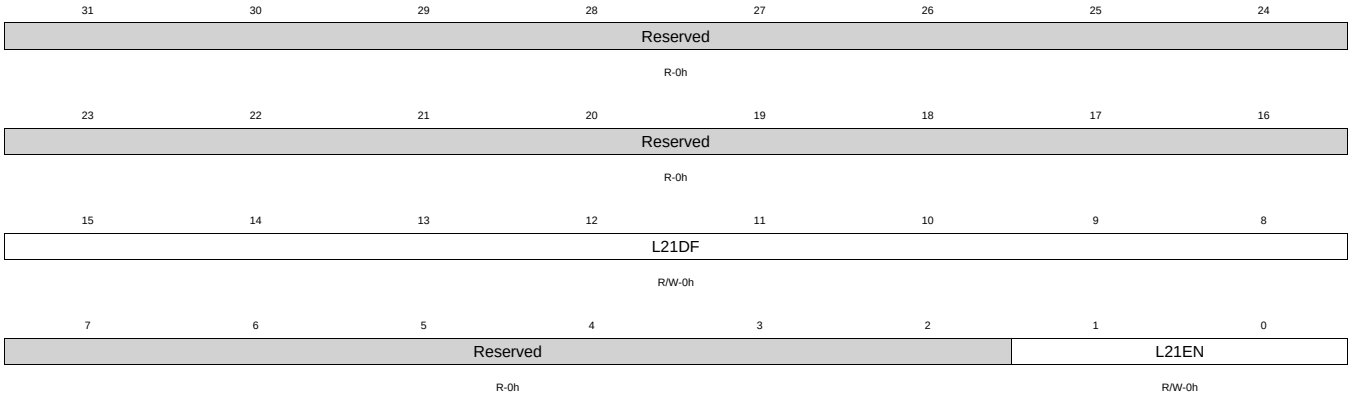
Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	
23-16	UPFC6	R/W	4Eh	2x up-sampling filter coefficient 6. s0.7.
15-8	UPFC5	R/W	ECh	2x up-sampling filter coefficient 5. s0.7.
7-0	UPFC4	R/W	6h	2x up-sampling filter coefficient 4. s0.7.

1.3.12.44 SD_VENC_l21ctl Register (offset = 124h) [reset = 0h]

SD_VENC_l21ctl is shown in Figure 1-539 and described in Table 1-455.

Line 21 Control

Figure 1-539. SD_VENC_l21ctl Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-455. SD_VENC_l21ctl Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	
15-8	L21DF	R/W	0h	Closed caption default data register. When the caption data register (L21DO or L21DE) is not updated before the caption data transmission timing for the corresponding field.. the ASCII code specified by this register is automatically transmitted for closed caption data.
7-2	Reserved	R	0h	
1-0	L21EN	R/W	0h	Closed caption field select. Specify the fields on which closed captioning is enabled. Closed caption data is transmitted on the line 21 for odd field and the line 284 for even field (line 22 and 335 for PAL). 0: No data output 1: Odd field 2: Even field 3: Both fields

1.3.12.45 SD_VENC_l21do Register (offset = 128h) [reset = 0h]

SD_VENC_l21do is shown in Figure 1-540 and described in Table 1-456.

Line 21 Data Even Field

Figure 1-540. SD_VENC_l21do Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
L21DO0							
R/W-0h							
7	6	5	4	3	2	1	0
L21DO1							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-456. SD_VENC_l21do Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	
15-8	L21DO0	R/W	0h	Closed caption data0 (odd field). Specify the ASCII code of the 1st byte to be transmitted in closed captioning for odd field.
7-0	L21DO1	R/W	0h	Closed caption data1 (odd field). Specify the ASCII code of the 2nd byte to be transmitted in closed captioning for odd field.

1.3.12.46 SD_VENC_l21de Register (offset = 12Ch) [reset = 0h]

SD_VENC_l21de is shown in Figure 1-541 and described in Table 1-457.

Line 21 Data Odd Field

Figure 1-541. SD_VENC_l21de Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
L21DE0							
R/W-0h							

7	6	5	4	3	2	1	0
L21DE1							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-457. SD_VENC_l21de Register Field Descriptions

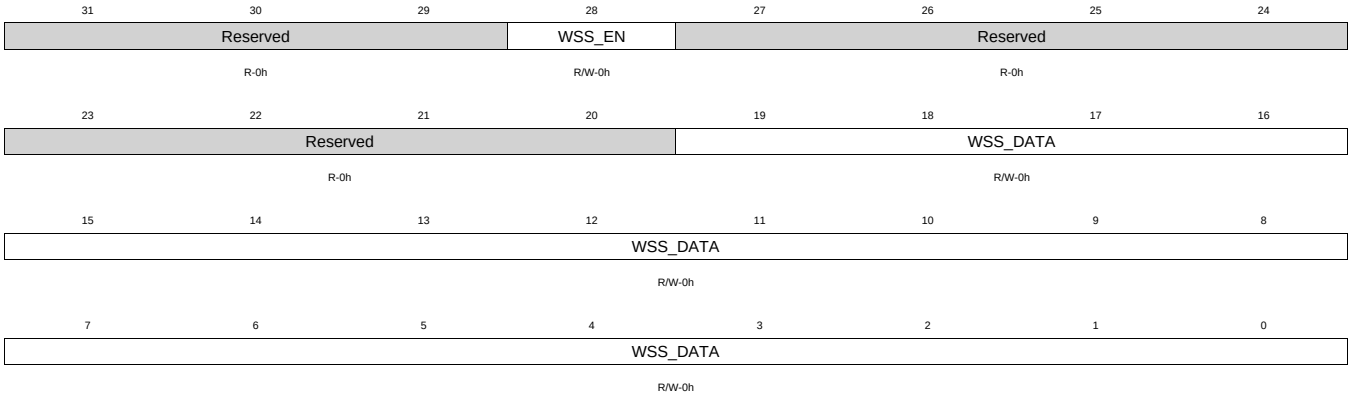
Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	
15-8	L21DE0	R/W	0h	Closed caption data0 (even field). Specify the ASCII code of the 1st byte to be transmitted in closed captioning for even field.
7-0	L21DE1	R/W	0h	Closed caption data1 (even field). Specify the ASCII code of the 2nd byte to be transmitted in closed captioning for even field.

1.3.12.47 SD_VENC_wss Register (offset = 130h) [reset = 0h]

SD_VENC_wss is shown in Figure 1-542 and described in Table 1-458.

WSS Control

Figure 1-542. SD_VENC_wss Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-458. SD_VENC_wss Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	Reserved	R	0h	
28	WSS_EN	R/W	0h	CGMS/WSS insertion enable 0: Disable 1: Enable
27-20	Reserved	R	0h	
19-0	WSS_DATA	R/W	0h	WSS data register (525i) bit1-0: WORD0 bit5-2: WORD1 bit13-6:WORD2 bit19-14: CRC (625i) bit3-0: GROUP1 bit7-4: GROUP2 bit10-8: GROUP3 bit13-11: GROUP4 bit19-14: unused

1.3.12.48 SD_VENC_scctl0 Register (offset = 148h) [reset = 00870000h]

SD_VENC_scctl0 is shown in Figure 1-543 and described in Table 1-459.

Sub-carrier Frequency Control 0

Figure 1-543. SD_VENC_scctl0 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
SCP0							
R/W-87h							

15	14	13	12	11	10	9	8
Reserved						SCSD	
R-0h						R/W-0h	

7	6	5	4	3	2	1	0
SCSD							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-459. SD_VENC_scctl0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	
23-16	SCP0	R/W	87h	Sub-carrier frequency parameter 0. Default is 135.
15-10	Reserved	R	0h	
9-0	SCSD	R/W	0h	Sub-carrier initial phase value. The degree can be specified by SCSD/1024*360.

1.3.12.49 SD_VENC_scctl1 Register (offset = 14Ch) [reset = 00210019h]

SD_VENC_scctl1 is shown in Figure 1-544 and described in Table 1-460.

Sub-carrier Frequency Control 1

Figure 1-544. SD_VENC_scctl1 Register

31	30	29	28	27	26	25	24
SCP2							
R/W-21h							

23	22	21	20	19	18	17	16
SCP2							
R/W-21h							

15	14	13	12	11	10	9	8
SCP1							
R/W-19h							

7	6	5	4	3	2	1	0
SCP1							
R/W-19h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-460. SD_VENC_scctl1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SCP2	R/W	21h	Sub-carrier frequency parameter 2. Default is 33. Fsc = (SCP0 + SCP1/SCP2) * Fin / 1024
15-0	SCP1	R/W	19h	Sub-carrier frequency parameter 1. Default is 25.

1.3.12.50 SD_VENC_dacsel Register (offset = 150h) [reset = 0h]

SD_VENC_dacsel is shown in Figure 1-545 and described in Table 1-461.

DAC Output Signal Select

Figure 1-545. SD_VENC_dacsel Register

31	30	29	28	27	26	25	24
Reserved						DA1E	DA0E
R-0h						R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
DA1S				DA0S			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-461. SD_VENC_dacsel Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	Reserved	R	0h	
25	DA1E	R/W	0h	DAC1 enable
24	DA0E	R/W	0h	DAC0 enable 0: DAC power down 1: DAC enable
23-8	Reserved	R	0h	
7-4	DA1S	R/W	0h	DAC1 output select. See DAC0S.
3-0	DA0S	R/W	0h	DAC0 output select. 0: CVBS 1: S-Video Y 2: S-Video; 3-15: Reserved

1.3.12.51 SD_VENC_dupf0 Register (offset = 154h) [reset = 0h]

SD_VENC_dupf0 is shown in Figure 1-546 and described in Table 1-462.

DAC 2x Upsampling Coefficient 0

Figure 1-546. SD_VENC_dupf0 Register

31	30	29	28	27	26	25	24
DUPFC3							
R/W-0h							
23	22	21	20	19	18	17	16
DUPFC2							
R/W-0h							
15	14	13	12	11	10	9	8
DUPFC1							
R/W-0h							
7	6	5	4	3	2	1	0
DUPFC0							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-462. SD_VENC_dupf0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DUPFC3	R/W	0h	DAC 2x oversampling filter coefficient 3. s0.7. (Default=0)
23-16	DUPFC2	R/W	0h	DAC 2x oversampling filter coefficient 2. s0.7. (Default=0)
15-8	DUPFC1	R/W	0h	DAC 2x oversampling filter coefficient 1. s0.7. (Default=0)
7-0	DUPFC0	R/W	0h	DAC 2x oversampling filter coefficient 0. s0.7. (Default=0)

1.3.12.52 SD_VENC_dupf1 Register (offset = 158h) [reset = 004EEC06h]

SD_VENC_dupf1 is shown in Figure 1-547 and described in Table 1-463.

DAC 2x Upsampling Coefficient 1

Figure 1-547. SD_VENC_dupf1 Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
DUPFC6							
R/W-4Eh							
15	14	13	12	11	10	9	8
DUPFC5							
R/W-ECh							
7	6	5	4	3	2	1	0
DUPFC4							
R/W-6h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-463. SD_VENC_dupf1 Register Field Descriptions

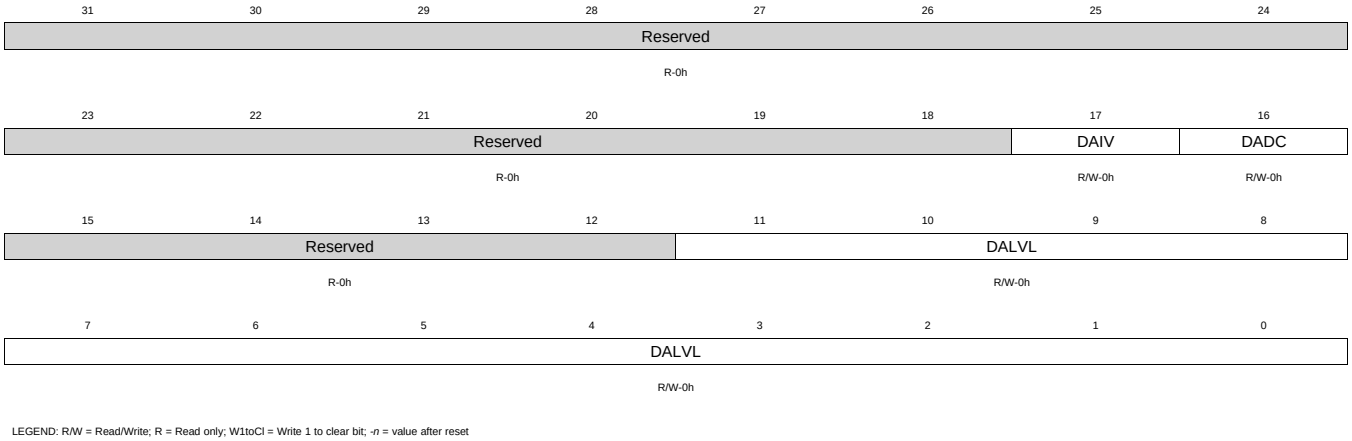
Bit	Field	Type	Reset	Description
31-24	Reserved	R	0h	
23-16	DUPFC6	R/W	4Eh	DAC 2x oversampling filter coefficient 6. s0.7. (Default=78)
15-8	DUPFC5	R/W	ECh	DAC 2x oversampling filter coefficient 5. s0.7. (Default=-20)
7-0	DUPFC4	R/W	6h	DAC 2x oversampling filter coefficient 4. s0.7. (Default=6)

1.3.12.53 SD_VENC_dactst Register (offset = 15Ch) [reset = 0h]

SD_VENC_dactst is shown in Figure 1-548 and described in Table 1-464.

DAC Test Mode

Figure 1-548. SD_VENC_dactst Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-464. SD_VENC_dactst Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	Reserved	R	0h	
17	DAIV	R/W	0h	DAC output invert mode. Setting 1 inverts the DAC output code. 0: Non-Inverse 1: Inverse
16	DADC	R/W	0h	DAC DC output mode. Setting 1 converts the value written in the DALVL register to DAC and directly outputs from DAOUT. 0: Normal 1: DC output mode
15-12	Reserved	R	0h	
11-0	DALVL	R/W	0h	DAC DC level control

1.3.12.54 SD_VENC_vtest Register (offset = 1FCh) [reset = 0h]

SD_VENC_vtest is shown in Figure 1-549 and described in Table 1-465.

Internal Test Register

Figure 1-549. SD_VENC_vtest Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTST																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-465. SD_VENC_vtest Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VTST	R/W	0h	Reserved for internal testing. Should be always zero for normal usage.

1.3.13 VCOMP Registers

Table 1-466 lists the memory-mapped registers for the VCOMP. All register offset addresses not listed in Table 1-466 should be considered as reserved locations and the register contents should not be modified.

Table 1-466. VCOMP REGISTERS

Offset	Acronym	Register Name	Section
0h	VCOMP_reg0	VCOMP Main Register 1	Section 1.3.13.1
4h	VCOMP_reg1	VCOMP Main Register 2	Section 1.3.13.2
8h	VCOMP_reg2	VCOMP Main Register 3	Section 1.3.13.3
Ch	VCOMP_reg3	VCOMP Aux Register 1	Section 1.3.13.4
10h	VCOMP_reg4	VCOMP Aux Register 2	Section 1.3.13.5
14h	VCOMP_reg5	VCOMP Aux Register 3	Section 1.3.13.6
18h	VCOMP_reg6	VCOMP Display Register 1	Section 1.3.13.7
1Ch	VCOMP_reg7	VCOMP Display Register 2	Section 1.3.13.8
20h	VCOMP_reg8	VCOMP Display Register 3	Section 1.3.13.9
24h	VCOMP_reg9	VCOMP Display Register 4	Section 1.3.13.10
28h	VCOMP_reg10	VCOMP Display Register 5	Section 1.3.13.11
2Ch	VCOMP_reg11	VCOMP Display Register 6	Section 1.3.13.12
30h	VCOMP_reg12	VCOMP Display Register 7	Section 1.3.13.13

1.3.13.1 VCOMP_reg0 Register (offset = 0h) [reset = 0h]

VCOMP_reg0 is shown in Figure 1-550 and described in Table 1-467.

Figure 1-550. VCOMP_reg0 Register

31	30	29	28	27	26	25	24
CFG_MAIN_ENABLE	CFG_MAIN_FIXED_DATA_SEND	Reserved		CFG_MAIN_NATIVE_NUMLINES			
R/W-0h	R/W-0h	R-0h		R/W-0h			

23	22	21	20	19	18	17	16
CFG_MAIN_NATIVE_NUMLINES							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved				CFG_MAIN_NATIVE_NUMPIX_PER_LINE			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
CFG_MAIN_NATIVE_NUMPIX_PER_LINE							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-467. VCOMP_reg0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFG_MAIN_ENABLE	R/W	0h	0 = Disable Main Plane 1 = Enable Main Plane
30	CFG_MAIN_FIXED_DATA_SEND	R/W	0h	0 = Send out the main source data 1 = When the main source is enabled.. send the alternate main Y/Cb/Cr values instead of the true source picture. This bit allows the datapath to flush through without outputing the actual picture. The main window would be seen as a constant color.
29-28	Reserved	R	0h	Reserved
27-16	CFG_MAIN_NATIVE_NUMLINES	R/W	0h	Number of lines in a field or frame from the incoming main source
15-12	Reserved	R	0h	Reserved
11-0	CFG_MAIN_NATIVE_NUMPIX_PER_LINE	R/W	0h	Number of pixels per line from the incoming main source

1.3.13.2 VCOMP_reg1 Register (offset = 4h) [reset = 0h]

VCOMP_reg1 is shown in Figure 1-551 and described in Table 1-468.

Figure 1-551. VCOMP_reg1 Register

31	30	29	28	27	26	25	24
Reserved	CFG_MAIN_STARTUP_HANDLING	Reserved		CFG_MAIN_SKIP_NUMPIX			
R-0h	R/W-0h	R-0h		R/W-0h			

23	22	21	20	19	18	17	16
CFG_MAIN_SKIP_NUMPIX							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved				CFG_MAIN_USE_NUMPIX			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
CFG_MAIN_USE_NUMPIX							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-468. VCOMP_reg1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Reserved	R	0h	Reserved
30	CFG_MAIN_STARTUP_HANDLING	R/W	0h	0 = Default condition for video in/video out operation 1 = Set for video in/no video out The Main source must be disabled when this bit is set. The NF and pixel data to the downstream module is not sent. This mode forces the VCOMP to request pictures from the upstream modules. Thus, these modules (like the DEI) can go ahead and load up with one or more input fields/frames before sending actual pictures to the output. Alternately, the config reg can be set to '0' and the fixed_data_send feature can send a color plane to downstream modules. cfg_main_enable should be '0' when this bit is set. If both the Main and the Aux are turned off, no nf or pixel data will propagate downstream of the dss_vcomp.
29-28	Reserved	R	0h	Reserved
27-16	CFG_MAIN_SKIP_NUMPIX	R/W	0h	Starting from the first pixel of each line. this field determines the number of incoming pixels to discard as part of the Compositor's picture clipping feature. SKIP_NUMPIX should be even - For odd values, U and V will get swapped in output. As a workaround to support odd values, swap format may be used in the VPDMA descriptor to counteract this problem.
15-12	Reserved	R	0h	Reserved
11-0	CFG_MAIN_USE_NUMPIX	R/W	0h	After main_skip_numpix number of pixels, this field determiines the number of pixels to use from each incoming line. This field allows the input picture to be clipped.

1.3.13.3 VCOMP_reg2 Register (offset = 8h) [reset = 0h]

VCOMP_reg2 is shown in Figure 1-552 and described in Table 1-469.

Figure 1-552. VCOMP_reg2 Register

31	30	29	28	27	26	25	24
Reserved				CFG_MAIN_SKIP_NUMLINES			
R-0h				R/W-0h			

23	22	21	20	19	18	17	16
CFG_MAIN_SKIP_NUMLINES							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved				CFG_MAIN_USE_NUMLINES			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
CFG_MAIN_USE_NUMLINES							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-469. VCOMP_reg2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	Reserved
27-16	CFG_MAIN_SKIP_NUMLINES	R/W	0h	Starting from the first line of each field or frame.. this field determines the number of incoming lines to discard as part of the Compositor's picture clipping feature.
15-12	Reserved	R	0h	Reserved
11-0	CFG_MAIN_USE_NUMLINES	R/W	0h	After main_skip_numlines number of lines.. this field determines the number of lines to use from each incoming field or frame. This field allows the input picture to be clipped.

1.3.13.4 VCOMP_reg3 Register (offset = Ch) [reset = 0h]

VCOMP_reg3 is shown in Figure 1-553 and described in Table 1-470.

Figure 1-553. VCOMP_reg3 Register

31	30	29	28	27	26	25	24
CFG_AUX_ENABLE	CFG_AUX_FIXED_DATA_SEND	Reserved		CFG_AUX_NATIVE_NUMLINES			
R/W-0h	R/W-0h	R-0h		R/W-0h			

23	22	21	20	19	18	17	16
CFG_AUX_NATIVE_NUMLINES							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved				CFG_AUX_NATIVE_NUMPIX_PER_LINE			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
CFG_AUX_NATIVE_NUMPIX_PER_LINE							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-470. VCOMP_reg3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFG_AUX_ENABLE	R/W	0h	0 = Disable Aux Plane 1 = Enable Aux Plane
30	CFG_AUX_FIXED_DATA_SEND	R/W	0h	0 = Send out the aux source data 1 = When the aux source is enabled.. send the alternate aux Y/Cb/Cr values instead of the true source picture. This bit allows the datapath to flush through without outputing the actual picture. The aux window would be seen as a constant color.
29-28	Reserved	R	0h	Reserved
27-16	CFG_AUX_NATIVE_NUMLINES	R/W	0h	Number of lines in a field or frame from the incoming aux source
15-12	Reserved	R	0h	Reserved
11-0	CFG_AUX_NATIVE_NUMPIX_PER_LINE	R/W	0h	Number of pixels per line from the incoming aux source

1.3.13.5 VCOMP_reg4 Register (offset = 10h) [reset = 0h]

VCOMP_reg4 is shown in Figure 1-554 and described in Table 1-471.

Figure 1-554. VCOMP_reg4 Register

31	30	29	28	27	26	25	24
Reserved	CFG_AUX_STARTUP_HANDLING	Reserved		CFG_AUX_SKIP_NUMPIX			
R-0h	R/W-0h	R-0h		R/W-0h			
23	22	21	20	19	18	17	16
CFG_AUX_SKIP_NUMPIX							
R/W-0h							
15	14	13	12	11	10	9	8
Reserved				CFG_AUX_USE_NUMPIX			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
CFG_AUX_USE_NUMPIX							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-471. VCOMP_reg4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Reserved	R	0h	Reserved
30	CFG_AUX_STARTUP_HANDLING	R/W	0h	0 = Default condition for video in/video out operation 1 = Set for video in/no video out The Aux source must be disabled when this bit is set. The NF and pixel data to the downstream module is not sent. This mode forces the VCOMP to request pictures from the upstream modules. Thus, these modules (like the DEI) can go ahead and load up with one or more input fields/frames before sending actual pictures to the output. Alternately, the config reg can be set to '0' and the fixed_data_send feature can send a color plane to downstream modules. cfg_aux_enable should be '0' when this bit is set. If both the Main and the Aux are turned off, no nf or pixel data will propagate downstream of the dss_vcomp.
29-28	Reserved	R	0h	Reserved
27-16	CFG_AUX_SKIP_NUMPIX	R/W	0h	Starting from the first pixel of each line.. this field determines the number of incoming pixels to discard as part of the Compositor's picture clipping feature. SKIP_NUMPIX should be even - For odd values, U and V will get swapped in output. As a workaround to support odd values, swap format may be used in the VPDMA descriptor to counteract this problem.
15-12	Reserved	R	0h	Reserved
11-0	CFG_AUX_USE_NUMPIX	R/W	0h	After aux_skip_numpix number of pixels, this field determiines the number of pixels to use from each incoming line. This field allows the input picture to be clipped.

1.3.13.6 VCOMP_reg5 Register (offset = 14h) [reset = 0h]

VCOMP_reg5 is shown in Figure 1-555 and described in Table 1-472.

Figure 1-555. VCOMP_reg5 Register

31	30	29	28	27	26	25	24
Reserved				CFG_AUX_SKIP_NUMLINES			
R-0h				R/W-0h			

23	22	21	20	19	18	17	16
CFG_AUX_SKIP_NUMLINES							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved				CFG_AUX_USE_NUMLINES			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
CFG_AUX_USE_NUMLINES							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-472. VCOMP_reg5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	Reserved
27-16	CFG_AUX_SKIP_NUMLINES	R/W	0h	Starting from the first line of each field or frame.. this field determines the number of incoming lines to discard as part of the Compositor's picture clipping feature.
15-12	Reserved	R	0h	Reserved
11-0	CFG_AUX_USE_NUMLINES	R/W	0h	After aux_skip_numlines number of lines.. this field determines the number of lines to use from each incoming field or frame. This field allows the input picture to be clipped.

1.3.13.7 VCOMP_reg6 Register (offset = 18h) [reset = 0h]

VCOMP_reg6 is shown in Figure 1-556 and described in Table 1-473.

Figure 1-556. VCOMP_reg6 Register

31	30	29	28	27	26	25	24
Reserved				CFG_DSPLY_NUMLINES			
R-0h				R/W-0h			

23	22	21	20	19	18	17	16
CFG_DSPLY_NUMLINES							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved				CFG_DSPLY_NUMPIX_PER_LINE			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
CFG_DSPLY_NUMPIX_PER_LINE							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-473. VCOMP_reg6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	Reserved
27-16	CFG_DSPLY_NUMLINES	R/W	0h	Number of lines in a field or frame for the output picture.
15-12	Reserved	R	0h	Reserved
11-0	CFG_DSPLY_NUMPIX_PER_LINE	R/W	0h	Number of pixels per line for the output picture.

1.3.13.8 VCOMP_reg7 Register (offset = 1Ch) [reset = 0h]

VCOMP_reg7 is shown in Figure 1-557 and described in Table 1-474.

Figure 1-557. VCOMP_reg7 Register

31	30	29	28	27	26	25	24
Reserved				CFG_DSPLY_MAIN_Y_ORIGIN			
R-0h				R/W-0h			

23	22	21	20	19	18	17	16
CFG_DSPLY_MAIN_Y_ORIGIN							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved				CFG_DSPLAY_MAIN_X_ORIGIN			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
CFG_DSPLAY_MAIN_X_ORIGIN							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-474. VCOMP_reg7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	Reserved	R	0h	Reserved
27-16	CFG_DSPLY_MAIN_Y_ORIGIN	R/W	0h	Row origin index for the Main source picture . This source picture is the result of any cropping by cfg_main_skip_numlines. (x..y) = (0..0) is the top left corner of the display.
15-12	Reserved	R	0h	Reserved
11-0	CFG_DSPLAY_MAIN_X_ORIGIN	R/W	0h	Column origin index for the Main source picture. This source picture is the result of any cropping by cfg_main_skip_numpix. (x..y) = (0..0) is the top left corner of the display.

1.3.13.9 VCOMP_reg8 Register (offset = 20h) [reset = 0h]

VCOMP_reg8 is shown in Figure 1-558 and described in Table 1-475.

Figure 1-558. VCOMP_reg8 Register

31	30	29	28	27	26	25	24
CFG_DWNSTRM_SRC_FID_CTRL		Reserved		CFG_DSPLY_AUX_Y_ORIGIN			
R/W-0h		R-0h		R/W-0h			

23	22	21	20	19	18	17	16
CFG_DSPLY_AUX_Y_ORIGIN							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved				CFG_DSPLAY_AUX_X_ORIGIN			
R-0h				R/W-0h			

7	6	5	4	3	2	1	0
CFG_DSPLAY_AUX_X_ORIGIN							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-475. VCOMP_reg8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	CFG_DWNSTRM_SRC_FID_CTRL	R/W	0h	00 = Source FID (bit 0) out of the VCOMP is the same as the respective bit from the Upstream Module 01 = Source FID (bit 0) out of the VCOMP is the inverse of the respective bit from the Upstream Module 10 = Source FID (bit 0) out of the VCOMP is '0'. 11 = Source FID (bit 0) out of the VCOMP is '1'. When both the Main and Aux sources are enabled.. NF and the Source/Encoder FID values are taken from the Main or Aux ports as defined in cfg_nf_handling. Otherwise.. NF and the Source/Encoder FID values are taken from the Active port. In no plane is active.. then no NF will be sent downstream. This register setting enables Bit 0.. representing the Source Picture FID.. to be the same as the Upstream Input.. the inverse of the Upstream Input.. programmably set to '0'.. or programmably set to '1'.
29-28	Reserved	R	0h	Reserved
27-16	CFG_DSPLY_AUX_Y_ORIGIN	R/W	0h	Row origin index for the Aux source picture. This source picture is the result of any cropping by cfg_aux_skip_numlines. (x..y) = (0..0) is the top left corner of the display.
15-12	Reserved	R	0h	Reserved
11-0	CFG_DSPLAY_AUX_X_ORIGIN	R/W	0h	Column origin index for the Aux source picture. This source picture is the result of any cropping by cfg_aux_skip_numpix. (x..y) = (0..0) is the top left corner of the display.

1.3.13.10 VCOMP_reg9 Register (offset = 24h) [reset = 0h]

VCOMP_reg9 is shown in Figure 1-559 and described in Table 1-476.

Figure 1-559. VCOMP_reg9 Register

31	30	29	28	27	26	25	24
CFG_MAIN_AUX_N_ONTOP	Reserved	CFG_DSPLY_BCKGRND_CR_VAL					
R/W-0h	R-0h	R/W-0h					
23	22	21	20	19	18	17	16
CFG_DSPLY_BCKGRND_CR_VAL				CFG_DSPLY_BCKGRND_CB_VAL			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
CFG_DSPLY_BCKGRND_CB_VAL						CFG_DSPLY_BCKGRND_Y_VAL	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
CFG_DSPLY_BCKGRND_Y_VAL							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-476. VCOMP_reg9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFG_MAIN_AUX_N_ONTOP	R/W	0h	When '1..' the Main window takes precedence over the Aux window in display areas where they overlap. When '0..' the Aux window takes precedence over the Main window in display areas where they overlap.
30	Reserved	R	0h	Reserved
29-20	CFG_DSPLY_BCKGRND_CR_VAL	R/W	0h	Background Cr/Chroma value for the display output.
19-10	CFG_DSPLY_BCKGRND_CB_VAL	R/W	0h	Background Cb/Chroma value for the display output.
9-0	CFG_DSPLY_BCKGRND_Y_VAL	R/W	0h	Background Y/Luma value for the display output.

1.3.13.11 VCOMP_reg10 Register (offset = 28h) [reset = 0h]

VCOMP_reg10 is shown in Figure 1-560 and described in Table 1-477.

Figure 1-560. VCOMP_reg10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG_DSPLY_TIMEOUT_COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-477. VCOMP_reg10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CFG_DSPLY_TIMEOUT_COUNT	R/W	0h	Timeout counter in DSS system clock cycles. An internal counter is reset to this value following a vpi_fp pulse to the VCOMP module. The VCOMP will start sending data to the downsteam module after the counter counts down to 0. The NF will be sent downstream based on the Main or Aux NF arrivals and the setting for cfg_nf_handling. The NF output will not be delayed. Likewise.. the Main and Aux request of data from the upstream modules are not delayed. Only the downstream output of pixel data is delayed. Generally.. this register should be set to 0x0.

1.3.13.12 VCOMP_reg11 Register (offset = 2Ch) [reset = 0h]

VCOMP_reg11 is shown in Figure 1-561 and described in Table 1-478.

Figure 1-561. VCOMP_reg11 Register

31	30	29	28	27	26	25	24
CFG_NF_HANDLING		CFG_DSPLY_ALT_MAIN_CR_VAL					
R/W-0h		R/W-0h					
23	22	21	20	19	18	17	16
CFG_DSPLY_ALT_MAIN_CR_VAL				CFG_DSPLY_ALT_MAIN_CB_VAL			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
CFG_DSPLY_ALT_MAIN_CB_VAL						CFG_DSPLY_ALT_MAIN_Y_VAL	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
CFG_DSPLY_ALT_MAIN_Y_VAL							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-478. VCOMP_reg11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	CFG_NF_HANDLING	R/W	0h	00' = When both Main and Aux sources are enabled.. the first NF to enter the VCOMP is used 01 = Undefined 10 = When both Main and Aux sources are enabled.. the Main source's NF is used 11 = When both Main and Aux sources are enabled.. the Aux source's NF is used
29-20	CFG_DSPLY_ALT_MAIN_CR_VAL	R/W	0h	Alternate Main Cr/Chroma value for the background display output. Used when main_fixed_data_send = 1.
19-10	CFG_DSPLY_ALT_MAIN_CB_VAL	R/W	0h	Alternate Main Cb/Chroma value for the background display output. Used when main_fixed_data_send = 1.
9-0	CFG_DSPLY_ALT_MAIN_Y_VAL	R/W	0h	Alternate Main Y/Luma value for the background display output. Used when main_fixed_data_send = 1.

1.3.13.13 VCOMP_reg12 Register (offset = 30h) [reset = 0h]

VCOMP_reg12 is shown in Figure 1-562 and described in Table 1-479.

Figure 1-562. VCOMP_reg12 Register

31	30	29	28	27	26	25	24
CFG_DWNSTRM_ENC_FID_CTRL		CFG_DSPLY_ALT_AUX_CR_VAL					
R/W-0h		R/W-0h					

23	22	21	20	19	18	17	16
CFG_DSPLY_ALT_AUX_CR_VAL				CFG_DSPLY_ALT_AUX_CB_VAL			
R/W-0h				R/W-0h			

15	14	13	12	11	10	9	8
CFG_DSPLY_ALT_AUX_CB_VAL						CFG_DSPLY_ALT_AUX_Y_VAL	
R/W-0h						R/W-0h	

7	6	5	4	3	2	1	0
CFG_DSPLY_ALT_AUX_Y_VAL							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-479. VCOMP_reg12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	CFG_DWNSTRM_ENC_FID_CTRL	R/W	0h	00 = Encoder FID (bit 1) out of the VCOMP is the same as the respective bit from the Upstream Module 01 = Encoder FID (bit 1) out of the VCOMP is the inverse of the respective bit from the Upstream Module 10 = Encoder FID (bit 1) out of the VCOMP is '0'. 11 = Encoder FID (bit 1) out of the VCOMP is '1'. When both the Main and Aux sources are enabled.. NF and the Source/Encoder FID values are taken from the Main or Aux ports as defined in cfg_nf_handling. Otherwise.. NF and the Source/Encoder FID values are taken from the Active port. In no plane is active.. then no NF will be sent downstream. This register setting enables Bit 1.. representing the Encoder FID.. to be the same as the Upstream Input.. the inverse of the Upstream Input.. programmably set to '0'.. or programmably set to '1'.
29-20	CFG_DSPLY_ALT_AUX_CR_VAL	R/W	0h	Alternate Aux Cr/Chroma value for the background display output. Used when aux_fixed_data_send = 1.
19-10	CFG_DSPLY_ALT_AUX_CB_VAL	R/W	0h	Alternate Aux Cb/Chroma value for the background display output. Used when aux_fixed_data_send = 1.
9-0	CFG_DSPLY_ALT_AUX_Y_VAL	R/W	0h	Alternate Aux Y/Luma value for the background display output. Used when aux_fixed_data_send = 1.

1.3.14 VIP_PARSER Registers

Table 1-480 lists the memory-mapped registers for the VIP_PARSER. All register offset addresses not listed in Table 1-480 should be considered as reserved locations and the register contents should not be modified.

Table 1-480. VIP_PARSER REGISTERS

Offset	Acronym	Register Name	Section
0h	VIP_PARSER_main	Main Configuration for VIP Parser	Section 1.3.14.1
4h	VIP_PARSER_port_a	Configuration for Input Port A	Section 1.3.14.2
8h	VIP_PARSER_xtra_port_a	More Configuration for Input Port A	Section 1.3.14.3
Ch	VIP_PARSER_port_b	Configuration for Input Port B	Section 1.3.14.4
10h	VIP_PARSER_xtra_port_b	More Configuration for Input Port B	Section 1.3.14.5
14h	VIP_PARSER_fiq_mask	Interrupt Mask Register	Section 1.3.14.6
18h	VIP_PARSER_fiq_clear	Interrupt Clear Register	Section 1.3.14.7
1Ch	VIP_PARSER_fiq_status	Interrupt Status Register	Section 1.3.14.8
20h	VIP_PARSER_output_port_a_src_fid	Current and Previous Output Port A Source FID values	Section 1.3.14.9
24h	VIP_PARSER_output_port_a_enc_fid	Current and Previous Output Port A Encoder FID values	Section 1.3.14.10
28h	VIP_PARSER_output_port_b_src_fid	Current and Previous Output Port B Source FID values	Section 1.3.14.11
2Ch	VIP_PARSER_output_port_b_enc_fid	Current and Previous Output Port B Encoder FID values	Section 1.3.14.12
30h	VIP_PARSER_output_port_a_src0_size	Width and Height for Source 0	Section 1.3.14.13
34h	VIP_PARSER_output_port_a_src1_size	Width and Height for Source 1	Section 1.3.14.14
38h	VIP_PARSER_output_port_a_src2_size	Width and Height for Source 2	Section 1.3.14.15
3Ch	VIP_PARSER_output_port_a_src3_size	Width and Height for Source 3	Section 1.3.14.16
40h	VIP_PARSER_output_port_a_src4_size	Width and Height for Source 4	Section 1.3.14.17
44h	VIP_PARSER_output_port_a_src5_size	Width and Height for Source 5	Section 1.3.14.18
48h	VIP_PARSER_output_port_a_src6_size	Width and Height for Source 6	Section 1.3.14.19
4Ch	VIP_PARSER_output_port_a_src7_size	Width and Height for Source 7	Section 1.3.14.20
50h	VIP_PARSER_output_port_a_src8_size	Width and Height for Source 8	Section 1.3.14.21
54h	VIP_PARSER_output_port_a_src9_size	Width and Height for Source 9	Section 1.3.14.22
58h	VIP_PARSER_output_port_a_src10_size	Width and Height for Source 10	Section 1.3.14.23
5Ch	VIP_PARSER_output_port_a_src11_size	Width and Height for Source 11	Section 1.3.14.24
60h	VIP_PARSER_output_port_a_src12_size	Width and Height for Source 12	Section 1.3.14.25
64h	VIP_PARSER_output_port_a_src13_size	Width and Height for Source 13	Section 1.3.14.26
68h	VIP_PARSER_output_port_a_src14_size	Width and Height for Source 14	Section 1.3.14.27
6Ch	VIP_PARSER_output_port_a_src15_size	Width and Height for Source 15	Section 1.3.14.28
70h	VIP_PARSER_output_port_b_src0_size	Width and Height for Source 0	Section 1.3.14.29

Table 1-480. VIP_PARSER REGISTERS (continued)

Offset	Acronym	Register Name	Section
74h	VIP_PARSER_output_port_b_src1_size	Width and Height for Source 1	Section 1.3.14.30
78h	VIP_PARSER_output_port_b_src2_size	Width and Height for Source 2	Section 1.3.14.31
7Ch	VIP_PARSER_output_port_b_src3_size	Width and Height for Source 3	Section 1.3.14.32
80h	VIP_PARSER_output_port_b_src4_size	Width and Height for Source 4	Section 1.3.14.33
84h	VIP_PARSER_output_port_b_src5_size	Width and Height for Source 5	Section 1.3.14.34
88h	VIP_PARSER_output_port_b_src6_size	Width and Height for Source 6	Section 1.3.14.35
8Ch	VIP_PARSER_output_port_b_src7_size	Width and Height for Source 7	Section 1.3.14.36
90h	VIP_PARSER_output_port_b_src8_size	Width and Height for Source 8	Section 1.3.14.37
94h	VIP_PARSER_output_port_b_src9_size	Width and Height for Source 9	Section 1.3.14.38
98h	VIP_PARSER_output_port_b_src10_size	Width and Height for Source 10	Section 1.3.14.39
9Ch	VIP_PARSER_output_port_b_src11_size	Width and Height for Source 11	Section 1.3.14.40
A0h	VIP_PARSER_output_port_b_src12_size	Width and Height for Source 12	Section 1.3.14.41
A4h	VIP_PARSER_output_port_b_src13_size	Width and Height for Source 13	Section 1.3.14.42
A8h	VIP_PARSER_output_port_b_src14_size	Width and Height for Source 14	Section 1.3.14.43
ACh	VIP_PARSER_output_port_b_src15_size	Width and Height for Source 15	Section 1.3.14.44
B0h	VIP_PARSER_port_a_vdet_vec	VDET bit settings for Line Mux Mode for Port A	Section 1.3.14.45
B4h	VIP_PARSER_port_b_vdet_vec	VDET bit setting sfor Line Mux Mode for Port B	Section 1.3.14.46
B8h	VIP_PARSER_xtra2_port_a	Ancillary Cropping Configuration for Input Port A	Section 1.3.14.47
BCh	VIP_PARSER_xtra3_port_a	Ancillary Cropping Configuration for Input Port A	Section 1.3.14.48
C0h	VIP_PARSER_xtra4_port_a	Active Video Cropping Configuration for Input Port A	Section 1.3.14.49
C4h	VIP_PARSER_xtra5_port_a	Active Video Cropping Configuration for Input Port A	Section 1.3.14.50
C8h	VIP_PARSER_xtra2_port_b	Ancillary Cropping Configuration for Input Port B	Section 1.3.14.51
CCh	VIP_PARSER_xtra3_port_b	Ancillary Cropping Configuration for Input Port B	Section 1.3.14.52
D0h	VIP_PARSER_xtra4_port_b	Active Video Cropping Configuration for Input Port B	Section 1.3.14.53
D4h	VIP_PARSER_xtra5_port_b	Active Video Cropping Configuration for Input Port B	Section 1.3.14.54
D8h	VIP_PARSER_xtra6_port_a	Cfg Disable Active Srcnum Vector Input for Port A	Section 1.3.14.55
DCh	VIP_PARSER_xtra7_port_b	Cfg Disable Active Srcnum Vector Input for Port B	Section 1.3.14.56

1.3.14.1 VIP_PARSER_main Register (offset = 0h) [reset = 0h]

VIP_PARSER_main is shown in Figure 1-563 and described in Table 1-481.

Main Configuration for VIP Parser

Figure 1-563. VIP_PARSER_main Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved		CLIP_ACTIVE	CLIP_BLNK	Reserved		DATA_INTERFACE_MODE	
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-481. VIP_PARSER_main Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	Reserved	R	0h	
5	CLIP_ACTIVE	R/W	0h	Discrete Sync Only '0' = Do not clip active pixels '1' = Clip Active Pixels as follows: 0xFF -andgt; 0xFE.. 0x00 -andgt; 0x01
4	CLIP_BLNK	R/W	0h	Discrete Sync Only '0' = Do not clip Blanking Data '1' = Clip Blanking Data as follows: 0xFF -andgt; 0xFE.. 0x00 -andgt; 0x01
3-2	Reserved	R	0h	
1-0	DATA_INTERFACE_MODE	R/W	0h	00 = 24b data interface. Uses Port A settings 01 = 16b data interface. Uses Port A settings. 10 = Dual independent 8b data interfaces. Uses independent Port A and Port B settings. 11 = Undefined

NOTE: Embedded sync input source is already clipped because the two 0x00 and 0xFF codes are illegal values in the active video data and they are reserved only for start codes.

If there is any need to down the line to pack this stream into an embedded sync format (input source contains the 0x00 and 0xFF codes), then the VIP Parser can be configured to clip the data on the way to being stored in memory. This prevents MPU or DSP to go through every byte to check if the data has to be clipped.

1.3.14.2 VIP_PARSER_port_a Register (offset = 4h) [reset = 0h]

VIP_PARSER_port_a is shown in Figure 1-564 and described in Table 1-482.

Configuration for Input Port A

Figure 1-564. VIP_PARSER_port_a Register

31	30	29	28	27	26	25	24
analyzer_fvh_err_correction_enable	ANALYZER_2X4X_SRCNUM_POS	FID_SKEW_POSTCOUNT					
R-0h	R/W-0h	R/W-0h					
23	22	21	20	19	18	17	16
SW_RESET	DISCRETE_BASIC_MODE	FID_SKEW_PRECOUNT					
R/W-0h	R/W-0h	R/W-0h					
15	14	13	12	11	10	9	8
USE_ACTVID_HSYNC_N	FID_DETECT_MODE	ACTVID_POLARITY	VSYNC_POLARITY	HSYNC_POLARITY	PIXCLK_EDGE_POLARITY	FID_POLARITY	ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CLR_ASYNC_FIFO_RD	CLR_ASYNC_FIFO_WR	CTRL_CHAN_SEL		SYNC_TYPE			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-482. VIP_PARSER_port_a Register Field Descriptions

Bit	Field	Type	Reset	Description
31	analyzer_fvh_err_correction_enable	R/W	0h	Embedded Sync Only 0 = Ignore the protection bits in the XV (fvh) codeword header. This setting is typically desired. 1 = Use the protection bits in an attempt to do error correction for the fvh control bits.
30	ANALYZER_2X4X_SRCNUM_POS	R/W	0h	Embedded Sync Only 0 = For 2x/4x mux mode.. srcnum is in the least significant nibble of the XV/fvh codeword (srcnum replaces the protection bits) 1 = For 2x/4x mux mode.. srcnum is in the least significant nibble of a horizontal blanking pixel value
29-24	FID_SKEW_POSTCOUNT	R/W	0h	Discrete Sync Only post count value when using vsync skew in FID determination
23	SW_RESET	R/W	0h	0 = Normal 1 = Reset Port A logic. Must be set to '0' again by the software for the module to function.

Table 1-482. VIP_PARSER_port_a Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	DISCRETE_BASIC_MODE	R/W	0h	This register is valid for Discrete Sync mode only. 0 = Normal Discrete Mode. Hsync Style Capture operates as follows: - Captures line starting from HSYNC inactive to active condition. - VSYNC determined by sync window. - FID can be determined by VSYNC skew or captured from pin at first pixel in first line. ACTVID style capture works as follows: - Captures line during contiguous ACTVID envelope. - VSYNC is captured at the first pixel in each line. - FID is captured on first pixel of ACTVID window. 1 = Basic Discrete Mode. When using hsync with Hsync Style Capture operates as follows: - The last line of active video ends on the pixel clock cycle where VSYNC transitions from inactive to active. - FID pin value is captured on this cycle and is used for the next field. - FID detection by VSYNC skew is not allowed. ACTVID style capture works as follows: - VSYNC is expected to transition from inactive to active between ACTVID window. - This VSYNC transition allows the next line in an ACTVID envelope to be sent to a new VPDMA buffer. - FID value is determined by the FID pin value on the cycle where VSYNC transitions from inactive to active. In basic discrete mode, there is no Vertical Ancillary Data. Therefore, VPDMA descriptors should not use Ancillary Data channels.
21-16	FID_SKEW_PRECOUNT	R/W	0h	Discrete Sync Only pre count value when using vsync skew in FID determination
15	USE_ACTVID_HSYNC_N	R/W	0h	Discrete Sync Only 0 = Use HSYNC style line capture 1 = Use ACTVID style line capture
14	FID_DETECT_MODE	R/W	0h	Discrete Sync Only 0 = Take FID from pin 1 = FID is determined by VSYNC skew
13	ACTVID_POLARITY	R/W	0h	Discrete Sync Only 0 = ACTVID is active low 1 = ACTVID is active high
12	VSYNC_POLARITY	R/W	0h	Discrete Sync Only 0 = VSYNC is active low 1 = VSYNC is active high
11	HSYNC_POLARITY	R/W	0h	Discrete Sync Only 0 = HSYNC is active low 1 = HSYNC is active high
10	PIXCLK_EDGE_POLARITY	R/W	0h	0 = Rising Edge is active PIXCLK edge 1 = Falling Edge is active PIXCLK edge
9	FID_POLARITY	R/W	0h	0 = Keep FID as found 1 = Invert Determined Value of FID Value on FID pin in discrete sync or value of "F-bit" in embedded sync indicates whether a field is EVEN or ODD (time-domain). However modules in HDVPSS follow convention (top/bottom) as specified in the table of HDVPSS Acronyms. As a result, fid_polarity needs to be set appropriately. Typically, this will result in different configuration for fid_polarity between PAL and NTSC modes.

Table 1-482. VIP_PARSER_port_a Register Field Descriptions (continued)

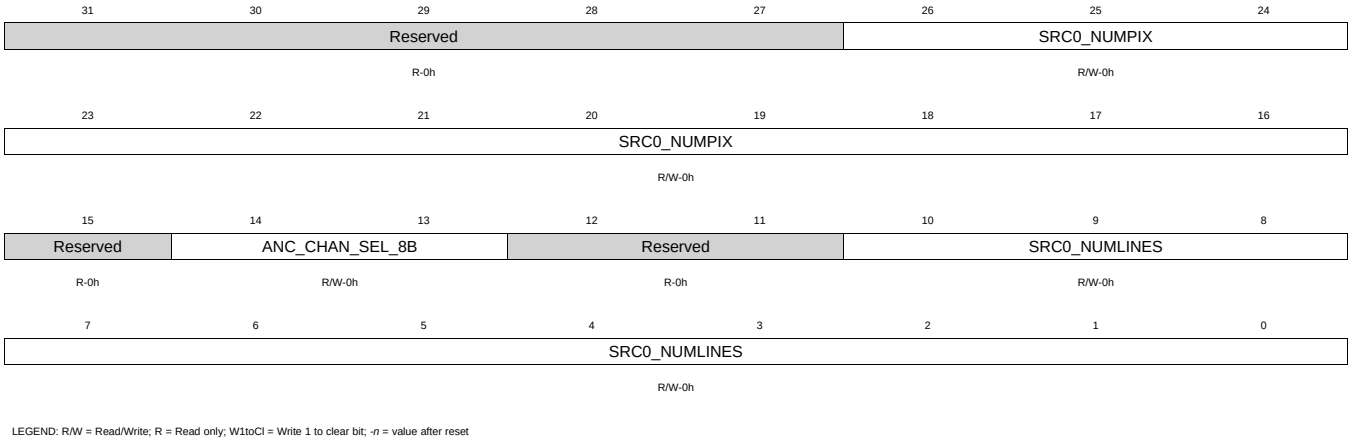
Bit	Field	Type	Reset	Description
8	ENABLE	R/W	0h	0 = Disable Port 1 = Enable Port
7	CLR_ASYNC_FIFO_RD	R/W	0h	0 = Normal 1 = Clear Async FIFO Read Logic
6	CLR_ASYNC_FIFO_WR	R/W	0h	0 = Normal 1 = Clear Async FIFO Write Logic
5-4	CTRL_CHAN_SEL	R/W	0h	Embedded Sync Only In 8b mode.. there is only one channel on data[7:0]. In 16b mode.. there are two channels. The Luma Channel is on data[15:8]. The Chroma Channel is on data[7:0]. In 24b mode.. there are three channels. The R channel is on data[23:16].. the G channel is on [15:8].. and the B channel is on data[7:0]. 00 = Use data[7:0] to extract control codes. 01 = Use data[15:8] to extract control codes. 10 = Use data[23:16] to extract control codes. 11 = Undefined In 16b and 24b modes.. this register is also used to select the channel from which Ancillary Data is extracted. The Ancillary Data channel must be the same as the control code channel. For 8b mode.. the anc_chan_sel_8b register is used to select the Luma or Chroma channel from which Ancillary Data is taken.
3-0	SYNC_TYPE	R/W	0h	0000 = embedded sync single 4:2:2 YUV stream 0001 = embedded sync 2x multiplexed 4:2:2 YUV stream 0010 = embedded sync 4x multiplexed 4:2:2 YUV stream 0011 = embedded sync line multiplexed 4:2:2 YUV stream 0100 = discrete sync single 4:2:2 YUV stream 0101 = embedded sync single RGB stream or single 444 YUV stream 0110 = reserved 0111 = reserved 1000 = reserved 1001 = reserved 1010 = discrete sync single 24b RGB stream

1.3.14.3 VIP_PARSER_xtra_port_a Register (offset = 8h) [reset = 0h]

VIP_PARSER_xtra_port_a is shown in Figure 1-565 and described in Table 1-483.

More Configuration for Input Port A

Figure 1-565. VIP_PARSER_xtra_port_a Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-483. VIP_PARSER_xtra_port_a Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	SRC0_NUMPIX	R/W	0h	Number of expected pixels on Source Number 0. The Port_a_src0_size interrupt will trigger if a line is encountered that differs from this pixelcount.
15	Reserved	R	0h	
14-13	ANC_CHAN_SEL_8B	R/W	0h	In 8b mode, Vertically Ancillary Data typically resides in the Luma sites. This bit allows vertical ancillary data to be extracted from the chroma sites instead. 00 = Extract 8b Mode Vertical Ancillary Data from Luma Sites 01 = Extract 8b Mode Vertical Ancillary Data from Chroma Sites 10, 11 = Extract every single sample of vertical ancillary data The output line is twice as wide as the other modes. For 16b and 24b inputs, ctrl_chan_sel is used to select which channel is used as a source for vertical ancillary data.
12-11	Reserved	R	0h	
10-0	SRC0_NUMLINES	R/W	0h	Number of expected lines on Source Number 0. The Port_a_src0_size interrupt will trigger if a field/frame is encountered that differs from this linecount.

1.3.14.4 VIP_PARSER_port_b Register (offset = Ch) [reset = 0h]

VIP_PARSER_port_b is shown in Figure 1-566 and described in Table 1-484.

Configuration for Input Port B

Figure 1-566. VIP_PARSER_port_b Register

31	30	29	28	27	26	25	24
analyzer_fvh_err_correction_enable	ANALYZER_2X4X_SRCNUM_POS	FID_SKEW_POSTCOUNT					
R-0h	R/W-0h	R/W-0h					
23	22	21	20	19	18	17	16
SW_RESET	DISCRETE_BASIC_MODE	FID_SKEW_PRECOUNT					
R/W-0h	R/W-0h	R/W-0h					
15	14	13	12	11	10	9	8
USE_ACTVID_HSYNC_N	FID_DETECT_MODE	ACTVID_POLARITY	VSYNC_POLARITY	HSYNC_POLARITY	PIXCLK_EDGE_POLARITY	FID_POLARITY	ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CLR_ASYNC_FIFO_RD	CLR_ASYNC_FIFO_WR	CTRL_CHAN_SEL		SYNC_TYPE			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-484. VIP_PARSER_port_b Register Field Descriptions

Bit	Field	Type	Reset	Description
31	analyzer_fvh_err_correction_enable	R/W	0h	Embedded Sync Only 0 = Ignore the protection bits in the XV (fvh) codeword header. This setting is typically desired. 1 = Use the protection bits in an attempt to do error correction for the fvh control bits.
30	ANALYZER_2X4X_SRCNUM_POS	R/W	0h	Embedded Sync Only 0 = For 2x/4x mux mode.. srcnum is in the least significant nibble of the XV/fvh codeword (srcnum replaces the protection bits) 1 = For 2x/4x mux mode.. srcnum is in the least significant nibble of a horizontal blanking pixel value
29-24	FID_SKEW_POSTCOUNT	R/W	0h	Discrete Sync Only post count value when using vsync skew in FID determination
23	SW_RESET	R/W	0h	0 = Normal 1 = Reset Port B logic. Must be set to '0' again by the software for the module to function.

Table 1-484. VIP_PARSER_port_b Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	DISCRETE_BASIC_MODE	R/W	0h	This register is valid for Discrete Sync mode only. 0 = Normal Discrete Mode. Hsync Style Capture operates as follows: - Captures line starting from HSYNC inactive to active condition. - VSYNC determined by sync window. - FID can be determined by VSYNC skew or captured from pin at first pixel in first line. ACTVID style capture works as follows: - Captures line during contiguous ACTVID envelope. - VSYNC is captured at the first pixel in each line. - FID is captured on first pixel of ACTVID window. 1 = Basic Discrete Mode. When using hsync with Hsync Style Capture operates as follows: - The last line of active video ends on the pixel clock cycle where VSYNC transitions from inactive to active. - FID pin value is captured on this cycle and is used for the next field. - FID detection by VSYNC skew is not allowed. ACTVID style capture works as follows: - VSYNC is expected to transition from inactive to active between ACTVID window. - This VSYNC transition allows the next line in an ACTVID envelope to be sent to a new VPDMA buffer. - FID value is determined by the FID pin value on the cycle where VSYNC transitions from inactive to active. In basic discrete mode, there is no Vertical Ancillary Data. Therefore, VPDMA descriptors should not use Ancillary Data channels.
21-16	FID_SKEW_PRECOUNT	R/W	0h	Discrete Sync Only pre count value when using vsync skew in FID determination
15	USE_ACTVID_HSYNC_N	R/W	0h	Discrete Sync Only 0 = Use HSYNC style line capture 1 = Use ACTVID style line capture
14	FID_DETECT_MODE	R/W	0h	Discrete Sync Only 0 = Take FID from pin 1 = FID is determined by VSYNC skew
13	ACTVID_POLARITY	R/W	0h	Discrete Sync Only 0 = ACTVID is active low 1 = ACTVID is active high
12	VSYNC_POLARITY	R/W	0h	Discrete Sync Only 0 = VSYNC is active low 1 = VSYNC is active high
11	HSYNC_POLARITY	R/W	0h	Discrete Sync Only 0 = HSYNC is active low 1 = HSYNC is active high
10	PIXCLK_EDGE_POLARITY	R/W	0h	0 = Rising Edge is active PIXCLK edge 1 = Falling Edge is active PIXCLK edge
9	FID_POLARITY	R/W	0h	0 = Keep FID as found 1 = Invert Determined Value of FID Value on FID pin in discrete sync or value of "F-bit" in embedded sync indicates whether a field is EVEN or ODD (time-domain). However modules in HDVPSS follow convention (top/bottom) as specified in the table of HDVPSS Acronyms. As a result, fid_polarity needs to be set appropriately. Typically, this will result in different configuration for fid_polarity between PAL and NTSC modes.

Table 1-484. VIP_PARSER_port_b Register Field Descriptions (continued)

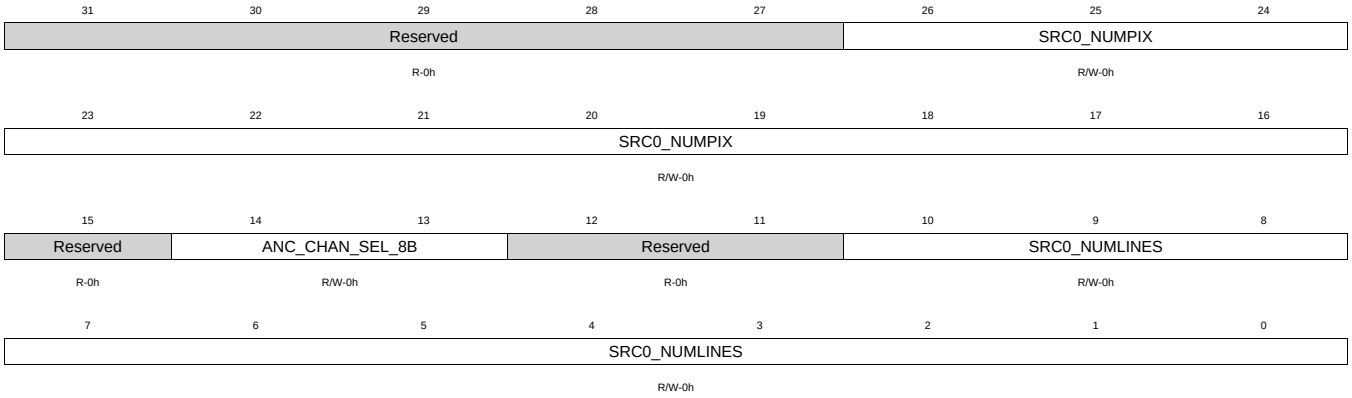
Bit	Field	Type	Reset	Description
8	ENABLE	R/W	0h	0 = Disable 1 = Enable
7	CLR_ASYNC_FIFO_RD	R/W	0h	0 = Normal 1 = Clear Async FIFO Read Logic
6	CLR_ASYNC_FIFO_WR	R/W	0h	0 = Normal 1 = Clear Async FIFO Write Logic
5-4	CTRL_CHAN_SEL	R/W	0h	PORT B supports on 8b mode. Always write 0 to this field. The anc_chan_sel_8b register is used to select the Luma or Chroma channel from which Ancillary Data is taken.
3-0	SYNC_TYPE	R/W	0h	0000 = embedded sync single YUV stream 0001 = embedded sync 2x multiplexed YUV stream 0010 = embedded sync 4x multiplexed YUV stream 0011 = embedded sync line multiplexed YUV stream 0100 = discrete sync single YUV stream 0101 = embedded sync single RGB stream 0110 = reserved 0111 = reserved 1000 = reserved 1001 = reserved 1010 = discrete sync single 24b RGB stream

1.3.14.5 VIP_PARSER_xtra_port_b Register (offset = 10h) [reset = 0h]

VIP_PARSER_xtra_port_b is shown in Figure 1-567 and described in Table 1-485.

More Configuration for Input Port B

Figure 1-567. VIP_PARSER_xtra_port_b Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-485. VIP_PARSER_xtra_port_b Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	SRC0_NUMPIX	R/W	0h	Number of expected pixels on Source Number 0. The Port_b_src0_size interrupt will trigger if a line is encountered that differs from this pixelcount.
15	Reserved	R	0h	
14-13	ANC_CHAN_SEL_8B	R/W	0h	In 8b mode, Vertically Ancillary Data typically resides in the Luma sites. This bit allows vertical ancillary data to be extracted from the chroma sites instead. 00 = Extract 8b Mode Vertical Ancillary Data from Luma Sites 01 = Extract 8b Mode Vertical Ancillary Data from Chroma Sites 10, 11 = Extract every single sample of vertical ancillary data. The output line is twice as wide as the other modes.
12-11	Reserved	R	0h	
10-0	SRC0_NUMLINES	R/W	0h	Number of expected lines on Source Number 0. The Port_b_src0_size interrupt will trigger if a field/frame is encountered that differs from this linecount.

1.3.14.6 VIP_PARSER_fiq_mask Register (offset = 14h) [reset = 0h]

VIP_PARSER_fiq_mask is shown in Figure 1-568 and described in Table 1-486.

Mask Bits for ARM FIQs. A 0 means the Host ARM will get an interrupt if the hardware sets one. A 1 in the mask bitfield means that the hardware interrupt is masked and the ARM will not be interrupted.

Figure 1-568. VIP_PARSER_fiq_mask Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved		PORT_B_CFG_DISABLE_COMPLETE_MASK	PORT_A_CFG_DISABLE_COMPLETE_MASK	PORT_B_ANC_PROTOCOL_VIOLATION_MASK	PORT_B_YUV_PROTOCOL_VIOLATION_MASK	PORT_A_ANC_PROTOCOL_VIOLATION_MASK	PORT_A_YUV_PROTOCOL_VIOLATION_MASK
R-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PORT_B_SRC0_SIZE	PORT_A_SRC0_SIZE	PORT_B_DISCONN	PORT_B_CONN	PORT_A_DISCONN	PORT_A_CONN	OUTPUT_FIFO_PRTB_ANC_OF	Reserved
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h
7	6	5	4	3	2	1	0
OUTPUT_FIFO_PRTB_YUV_OF	OUTPUT_FIFO_PRTA_ANC_OF	Reserved	OUTPUT_FIFO_PRTA_YUV_OF	ASYNC_FIFO_PRTB_OF	ASYNC_FIFO_PRTA_OF	PRTB_VDET_MASK	PRTA_VDET_MASK
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-486. VIP_PARSER_fiq_mask Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	Reserved	R	0h	
21	PORT_B_CFG_DISABLE_COMPLETE_MASK	R/W	0h	Port B Cfg Disable Complete Mask
20	PORT_A_CFG_DISABLE_COMPLETE_MASK	R/W	0h	Port A Cfg Disable Complete Mask
19	PORT_B_ANC_PROTOCOL_VIOLATION_MASK	R/W	0h	Port B ANC VPI Protocol Violation Mask
18	PORT_B_YUV_PROTOCOL_VIOLATION_MASK	R/W	0h	Port B YUV VPI Protocol Violation Mask
17	PORT_A_ANC_PROTOCOL_VIOLATION_MASK	R/W	0h	Port A ANC VPI Protocol Violation Mask
16	PORT_A_YUV_PROTOCOL_VIOLATION_MASK	R/W	0h	Port A YUV VPI Protocol Violation Mask
15	PORT_B_SRC0_SIZE	R/W	0h	Video size detected on Port B does not match size programmed in xtra_port_b register
14	PORT_A_SRC0_SIZE	R/W	0h	Video size detected on Port A does not match size programmed in xtra_port_a register
13	PORT_B_DISCONN	R/W	0h	Port B Link Disconnect Srcnum 0 Mask
12	PORT_B_CONN	R/W	0h	Port B Link Connect Srcnum 0 Mask
11	PORT_A_DISCONN	R/W	0h	Port A Link Disconnect Scrnum 0 Mask
10	PORT_A_CONN	R/W	0h	Port A Link Connect Srcnum 0 Mask
9	OUTPUT_FIFO_PRTB_ANC_OF	R/W	0h	Output FIFO Port B Ancillary Overflow Mask
8	Reserved	R	0h	
7	OUTPUT_FIFO_PRTB_YUV_OF	R/W	0h	Output FIFO Port B Luma Overflow Mask
6	OUTPUT_FIFO_PRTA_ANC_OF	R/W	0h	Output FIFO Port A Ancillary Overflow Mask

Table 1-486. VIP_PARSER_fiq_mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Reserved	R	0h	
4	OUTPUT_FIFO_PRTA_YUV_OF	R/W	0h	Output FIFO Port A Luma Overflow Mask
3	ASYNC_FIFO_PRTB_OF	R/W	0h	Port B Async FIFO Overflow FIQ Mask
2	ASYNC_FIFO_PRTA_OF	R/W	0h	Port A Async FIFO Overflow FIQ Mask
1	PRTB_VDET_MASK	R/W	0h	Port B Video Detect FIQ Mask
0	PRTA_VDET_MASK	R/W	0h	Port A Video Detect FIQ Mask

1.3.14.7 VIP_PARSER_fiq_clear Register (offset = 18h) [reset = 0h]

VIP_PARSER_fiq_clear is shown in Figure 1-569 and described in Table 1-487.

Clears bits in the FIQ Status

Figure 1-569. VIP_PARSER_fiq_clear Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved		PORT_B_CFG_DISABLE_COMPLETE_CLR	PORT_A_CFG_DISABLE_COMPLETE_CLR	PORT_B_ANC_PROTOCOL_VIOLATION_CLR	PORT_B_YUV_PROTOCOL_VIOLATION_CLR	PORT_A_ANC_PROTOCOL_VIOLATION_CLR	PORT_A_YUV_PROTOCOL_VIOLATION_CLR
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PORT_B_SRC0_SIZE_CLR	PORT_A_SRC0_SIZE_CLR	PORT_B_DISCONN_CLR	PORT_B_CONN_CLR	PORT_A_DISCONN_CLR	PORT_A_CONN_CLR	OUTPUT_FIFO_PRTB_ANC_CLR	Reserved
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h
7	6	5	4	3	2	1	0
OUTPUT_FIFO_PRTB_YUV_CLR	OUTPUT_FIFO_PRTA_ANC_CLR	Reserved	OUTPUT_FIFO_PRTA_YUV_CLR	ASYNC_FIFO_PRTB_CLR	ASYNC_FIFO_PRTA_CLR	PRTB_VDET_CLR	PRTA_VDET_CLR
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-487. VIP_PARSER_fiq_clear Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	Reserved	R	0h	
21	PORT_B_CFG_DISABLE_COMPLETE_CLR	R/W	0h	Write '1' followed by '0' to Clear Port B Cfg Disable Complete FIQ
20	PORT_A_CFG_DISABLE_COMPLETE_CLR	R/W	0h	Write '1' followed by '0' to Clear Port A Cfg Disable Complete FIQ
19	PORT_B_ANC_PROTOCOL_VIOLATION_CLR	R/W	0h	Write '1' followed by '0' to Clear Port B ANC VPI Protocol Violation FIQ
18	PORT_B_YUV_PROTOCOL_VIOLATION_CLR	R/W	0h	Write '1' followed by '0' to Clear Port B YUV VPI Protocol Violation FIQ
17	PORT_A_ANC_PROTOCOL_VIOLATION_CLR	R/W	0h	Write '1' followed by '0' to Clear Port A ANC VPI Protocol Violation FIQ
16	PORT_A_YUV_PROTOCOL_VIOLATION_CLR	R/W	0h	Write '1' followed by '0' to Clear Port A YUV VPI Protocol Violation FIQ
15	PORT_B_SRC0_SIZE_CLR	R/W	0h	Write '1' followed by '0' to Clear Port B Src0 Size FIQ
14	PORT_A_SRC0_SIZE_CLR	R/W	0h	Write '1' followed by '0' to Clear Port A Src0 Size FIQ
13	PORT_B_DISCONN_CLR	R/W	0h	Write '1' followed by '0' to Clear Port B Link Disconnect FIQ
12	PORT_B_CONN_CLR	R/W	0h	Write '1' followed by '0' to Clear Port B Link Connect FIQ
11	PORT_A_DISCONN_CLR	R/W	0h	Write '1' followed by '0' to Clear Port A Link Disconnect FIQ
10	PORT_A_CONN_CLR	R/W	0h	Write '1' followed by '0' to Clear Port A Link Connect FIQ
9	OUTPUT_FIFO_PRTB_ANC_CLR	R/W	0h	Write '1' followed by '0' to Clear Output FIFO Port B Ancillary Overflow FIQ
8	Reserved	R	0h	
7	OUTPUT_FIFO_PRTB_YUV_CLR	R/W	0h	Write '1' followed by '0' to Clear Output FIFO Port B Luma Overflow FIQ
6	OUTPUT_FIFO_PRTA_ANC_CLR	R/W	0h	Write '1' followed by '0' to Clear Output FIFO Port A Ancillary Overflow FIQ
5	Reserved	R	0h	

Table 1-487. VIP_PARSER_fiq_clear Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	OUTPUT_FIFO_PRTA_YUV_CLR	R/W	0h	Write '1' followed by '0' to Clear Output FIFO Port A Luma Overflow FIQ
3	ASYNC_FIFO_PRTB_CLR	R/W	0h	Write '1' followed by '0' to Clear Async FIFO Port B Overflow FIQ
2	ASYNC_FIFO_PRTA_CLR	R/W	0h	Write '1' followed by '0' to Clear Async FIFO Port A Overflow FIQ
1	PRTB_VDET_CLR	R/W	0h	Write '1' followed by '0' to Clear Video Detect FIQ for Port B
0	PRTA_VDET_CLR	R/W	0h	Write '1' followed by '0' to Clear Video Detect FIQ for Port A

1.3.14.8 VIP_PARSER_fiq_status Register (offset = 1Ch) [reset = 0h]

VIP_PARSER_fiq_status is shown in Figure 1-570 and described in Table 1-488.

FIQ Status values

Figure 1-570. VIP_PARSER_fiq_status Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved		PORT_B_CFG_DISABLE_COMPLETE_CLR	PORT_A_CFG_DISABLE_COMPLETE	PORT_B_ANC_PROTOCOL_VIOLATION	PORT_B_YUV_PROTOCOL_VIOLATION	PORT_A_ANC_PROTOCOL_VIOLATION	PORT_A_YUV_PROTOCOL_VIOLATION
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

15	14	13	12	11	10	9	8
PORT_B_SRC0_SIZE_STATUS	PORT_A_SRC0_SIZE_STATUS	PORT_B_DISCONN_STATUS	PORT_B_CONN_STATUS	PORT_A_DISCONN_STATUS	PORT_A_CONN_STATUS	OUTPUT_FIFO_PRTB_ANC_STATUS	OUTPUT_FIFO_PRTB_CHROMA_STATUS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

7	6	5	4	3	2	1	0
OUTPUT_FIFO_PRTB_LUMA_STATUS	OUTPUT_FIFO_PRTA_ANC_STATUS	OUTPUT_FIFO_PRTA_CHROMA_STATUS	OUTPUT_FIFO_PRTA_LUMA_STATUS	ASYNC_FIFO_PRTB_STATUS	ASYNC_FIFO_PRTA_STATUS	PRTB_VDET_STATUS	PRTA_VDET_STATUS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-488. VIP_PARSER_fiq_status Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	Reserved	R	0h	
21	PORT_B_CFG_DISABLE_COMPLETE_CLR	R	0h	Port B Cfg Disable Complete FIQ
20	PORT_A_CFG_DISABLE_COMPLETE	R	0h	Port A Cfg Disable Complete FIQ
19	PORT_B_ANC_PROTOCOL_VIOLATION	R	0h	Port B ANC VPI Protocol Violation FIQ
18	PORT_B_YUV_PROTOCOL_VIOLATION	R	0h	Port B YUV VPI Protocol Violation FIQ
17	PORT_A_ANC_PROTOCOL_VIOLATION	R	0h	Port A ANC VPI Protocol Violation FIQ
16	PORT_A_YUV_PROTOCOL_VIOLATION	R	0h	Port A YUV VPI Protocol Violation FIQ
15	PORT_B_SRC0_SIZE_STATUS	R	0h	Port B Source 0 Size FIQ
14	PORT_A_SRC0_SIZE_STATUS	R	0h	Port A Source 0 Size FIQ
13	PORT_B_DISCONN_STATUS	R	0h	Port B Disconnect FIQ
12	PORT_B_CONN_STATUS	R	0h	Port B Connect FIQ
11	PORT_A_DISCONN_STATUS	R	0h	Port A Disconnect FIQ
10	PORT_A_CONN_STATUS	R	0h	Port A Connect FIQ
9	OUTPUT_FIFO_PRTB_ANC_STATUS	R	0h	Output FIFO Port B Ancillary Overflow Status
8	OUTPUT_FIFO_PRTB_CHROMA_STATUS	R	0h	Output FIFO Port B Chroma Overflow Status

Table 1-488. VIP_PARSER_fiq_status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	OUTPUT_FIFO_PRTB_LUMA_STATUS	R	0h	Output FIFO Port B Luma Overflow Status
6	OUTPUT_FIFO_PRTA_ANC_STATUS	R	0h	Output FIFO Port A Ancillary Overflow Status
5	OUTPUT_FIFO_PRTA_CHROMA_STATUS	R	0h	Output FIFO Port A Chroma Overflow Status
4	OUTPUT_FIFO_PRTA_LUMA_STATUS	R	0h	Output FIFO Port A Luma Overflow Status
3	ASYNC_FIFO_PRTB_STATUS	R	0h	Async FIFO Port B Overflow Status
2	ASYNC_FIFO_PRTA_STATUS	R	0h	Async FIFO Port A Overflow Status
1	PRTB_VDET_STATUS	R	0h	VDET Status for Port B
0	PRTA_VDET_STATUS	R	0h	VDET Status for Port A

1.3.14.9 VIP_PARSER_output_port_a_src_fid Register (offset = 20h) [reset = FFFFFFFFh]

VIP_PARSER_output_port_a_src_fid is shown in Figure 1-571 and described in Table 1-489.

Current and Previous Output Port A Source FID values

Figure 1-571. VIP_PARSER_output_port_a_src_fid Register

31	30	29	28	27	26	25	24
PRTA_SRC15_CURR_SOURCE_FID	PRTA_SRC15_PREV_SOURCE_FID	PRTA_SRC14_CURR_SOURCE_FID	PRTA_SRC14_PREV_SOURCE_FID	PRTA_SRC13_CURR_SOURCE_FID	PRTA_SRC13_PREV_SOURCE_FID	PRTA_SRC12_CURR_SOURCE_FID	PRTA_SRC12_PREV_SOURCE_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
23	22	21	20	19	18	17	16
PRTA_SRC11_CURR_SOURCE_FID	PRTA_SRC11_PREV_SOURCE_FID	PRTA_SRC10_CURR_SOURCE_FID	PRTA_SRC10_PREV_SOURCE_FID	PRTA_SRC9_CURR_SOURCE_FID	PRTA_SRC9_PREV_SOURCE_FID	PRTA_SRC8_CURR_SOURCE_FID	PRTA_SRC8_PREV_SOURCE_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
15	14	13	12	11	10	9	8
PRTA_SRC7_CURR_SOURCE_FID	PRTA_SRC7_PREV_SOURCE_FID	PRTA_SRC6_CURR_SOURCE_FID	PRTA_SRC6_PREV_SOURCE_FID	PRTA_SRC5_CURR_SOURCE_FID	PRTA_SRC5_PREV_SOURCE_FID	PRTA_SRC4_CURR_SOURCE_FID	PRTA_SRC4_PREV_SOURCE_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
PRTA_SRC3_CURR_SOURCE_FID	PRTA_SRC3_PREV_SOURCE_FID	PRTA_SRC2_CURR_SOURCE_FID	PRTA_SRC2_PREV_SOURCE_FID	PRTA_SRC1_CURR_SOURCE_FID	PRTA_SRC1_PREV_SOURCE_FID	PRTA_SRC0_CURR_SOURCE_FID	PRTA_SRC0_PREV_SOURCE_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-489. VIP_PARSER_output_port_a_src_fid Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRTA_SRC15_CURR_SOURCE_FID	R	1h	For Source ID 15 from Port A.. Source Field ID for Current Field
30	PRTA_SRC15_PREV_SOURCE_FID	R	1h	For Source ID 15 from Port A.. Source Field ID for Previous Field
29	PRTA_SRC14_CURR_SOURCE_FID	R	1h	For Source ID 14 from Port A.. Source Field ID for Current Field
28	PRTA_SRC14_PREV_SOURCE_FID	R	1h	For Source ID 14 from Port A.. Source Field ID for Previous Field
27	PRTA_SRC13_CURR_SOURCE_FID	R	1h	For Source ID 13 from Port A.. Source Field ID for Current Field
26	PRTA_SRC13_PREV_SOURCE_FID	R	1h	For Source ID 13 from Port A.. Source Field ID for Previous Field
25	PRTA_SRC12_CURR_SOURCE_FID	R	1h	For Source ID 12 from Port A.. Source Field ID for Current Field
24	PRTA_SRC12_PREV_SOURCE_FID	R	1h	For Source ID 12 from Port A.. Source Field ID for Previous Field
23	PRTA_SRC11_CURR_SOURCE_FID	R	1h	For Source ID 11 from Port A.. Source Field ID for Current Field
22	PRTA_SRC11_PREV_SOURCE_FID	R	1h	For Source ID 11 from Port A.. Source Field ID for Previous Field
21	PRTA_SRC10_CURR_SOURCE_FID	R	1h	For Source ID 10 from Port A.. Source Field ID for Current Field
20	PRTA_SRC10_PREV_SOURCE_FID	R	1h	For Source ID 10 from Port A.. Source Field ID for Previous Field
19	PRTA_SRC9_CURR_SOURCE_FID	R	1h	For Source ID 9 from Port A.. Source Field ID for Current Field
18	PRTA_SRC9_PREV_SOURCE_FID	R	1h	For Source ID 9 from Port A.. Source Field ID for Previous Field
17	PRTA_SRC8_CURR_SOURCE_FID	R	1h	For Source ID 8 from Port A.. Source Field ID for Current Field

Table 1-489. VIP_PARSER_output_port_a_src_fid Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRTA_SRC8_PREV_SOURCE_FID	R	1h	For Source ID 8 from Port A.. Source Field ID for Previous Field
15	PRTA_SRC7_CURR_SOURCE_FID	R	1h	For Source ID 7 from Port A.. Source Field ID for Current Field
14	PRTA_SRC7_PREV_SOURCE_FID	R	1h	For Source ID 7 from Port A.. Source Field ID for Previous Field
13	PRTA_SRC6_CURR_SOURCE_FID	R	1h	For Source ID 6 from Port A.. Source Field ID for Current Field
12	PRTA_SRC6_PREV_SOURCE_FID	R	1h	For Source ID 6 from Port A.. Source Field ID for Previous Field
11	PRTA_SRC5_CURR_SOURCE_FID	R	1h	For Source ID 5 from Port A.. Source Field ID for Current Field
10	PRTA_SRC5_PREV_SOURCE_FID	R	1h	For Source ID 5 from Port A.. Source Field ID for Previous Field
9	PRTA_SRC4_CURR_SOURCE_FID	R	1h	For Source ID 4 from Port A.. Source Field ID for Current Field
8	PRTA_SRC4_PREV_SOURCE_FID	R	1h	For Source ID 4 from Port A.. Source Field ID for Previous Field
7	PRTA_SRC3_CURR_SOURCE_FID	R	1h	For Source ID 3 from Port A.. Source Field ID for Current Field
6	PRTA_SRC3_PREV_SOURCE_FID	R	1h	For Source ID 3 from Port A.. Source Field ID for Previous Field
5	PRTA_SRC2_CURR_SOURCE_FID	R	1h	For Source ID 2 from Port A.. Source Field ID for Current Field
4	PRTA_SRC2_PREV_SOURCE_FID	R	1h	For Source ID 2 from Port A.. Source Field ID for Previous Field
3	PRTA_SRC1_CURR_SOURCE_FID	R	1h	For Source ID 1 from Port A.. Source Field ID for Current Field
2	PRTA_SRC1_PREV_SOURCE_FID	R	1h	For Source ID 1 from Port A.. Source Field ID for Previous Field
1	PRTA_SRC0_CURR_SOURCE_FID	R	1h	For Source ID 0 from Port A.. Source Field ID for Current Field
0	PRTA_SRC0_PREV_SOURCE_FID	R	1h	For Source ID 0 from Port A.. Source Field ID for Previous Field

1.3.14.10 VIP_PARSER_output_port_a_enc_fid Register (offset = 24h) [reset = FFFFFFFFh]

VIP_PARSER_output_port_a_enc_fid is shown in Figure 1-572 and described in Table 1-490.

Current and Previous Output Port A Encoder FID values

Figure 1-572. VIP_PARSER_output_port_a_enc_fid Register

31	30	29	28	27	26	25	24
PRTA_SRC15_CURR_ENC_FID	PRTA_SRC15_PREV_ENC_FID	PRTA_SRC14_CURR_ENC_FID	PRTA_SRC14_PREV_ENC_FID	PRTA_SRC13_CURR_ENC_FID	PRTA_SRC13_PREV_ENC_FID	PRTA_SRC12_CURR_ENC_FID	PRTA_SRC12_PREV_ENC_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
23	22	21	20	19	18	17	16
PRTA_SRC11_CURR_ENC_FID	PRTA_SRC11_PREV_ENC_FID	PRTA_SRC10_CURR_ENC_FID	PRTA_SRC10_PREV_ENC_FID	PRTA_SRC9_CURR_ENC_FID	PRTA_SRC9_PREV_ENC_FID	PRTA_SRC8_CURR_ENC_FID	PRTA_SRC8_PREV_ENC_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
15	14	13	12	11	10	9	8
PRTA_SRC7_CURR_ENC_FID	PRTA_SRC7_PREV_ENC_FID	PRTA_SRC6_CURR_ENC_FID	PRTA_SRC6_PREV_ENC_FID	PRTA_SRC5_CURR_ENC_FID	PRTA_SRC5_PREV_ENC_FID	PRTA_SRC4_CURR_ENC_FID	PRTA_SRC4_PREV_ENC_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
PRTA_SRC3_CURR_ENC_FID	PRTA_SRC3_PREV_ENC_FID	PRTA_SRC2_CURR_ENC_FID	PRTA_SRC2_PREV_ENC_FID	PRTA_SRC1_CURR_ENC_FID	PRTA_SRC1_PREV_ENC_FID	PRTA_SRC0_CURR_ENC_FID	PRTA_SRC0_PREV_ENC_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-490. VIP_PARSER_output_port_a_enc_fid Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRTA_SRC15_CURR_ENC_FID	R	1h	For Source ID 15 from Port A.. Encoder Field ID for Current Field
30	PRTA_SRC15_PREV_ENC_FID	R	1h	For Source ID 15 from Port A.. Encoder Field ID for Previous Field
29	PRTA_SRC14_CURR_ENC_FID	R	1h	For Source ID 14 from Port A.. Encoder Field ID for Current Field
28	PRTA_SRC14_PREV_ENC_FID	R	1h	For Source ID 14 from Port A.. Encoder Field ID for Previous Field
27	PRTA_SRC13_CURR_ENC_FID	R	1h	For Source ID 13 from Port A.. Encoder Field ID for Current Field
26	PRTA_SRC13_PREV_ENC_FID	R	1h	For Source ID 13 from Port A.. Encoder Field ID for Previous Field
25	PRTA_SRC12_CURR_ENC_FID	R	1h	For Source ID 12 from Port A.. Encoder Field ID for Current Field
24	PRTA_SRC12_PREV_ENC_FID	R	1h	For Source ID 12 from Port A.. Encoder Field ID for Previous Field
23	PRTA_SRC11_CURR_ENC_FID	R	1h	For Source ID 11 from Port A.. Encoder Field ID for Current Field
22	PRTA_SRC11_PREV_ENC_FID	R	1h	For Source ID 11 from Port A.. Encoder Field ID for Previous Field
21	PRTA_SRC10_CURR_ENC_FID	R	1h	For Source ID 10 from Port A.. Encoder Field ID for Current Field
20	PRTA_SRC10_PREV_ENC_FID	R	1h	For Source ID 10 from Port A.. Encoder Field ID for Previous Field
19	PRTA_SRC9_CURR_ENC_FID	R	1h	For Source ID 9 from Port A.. Encoder Field ID for Current Field
18	PRTA_SRC9_PREV_ENC_FID	R	1h	For Source ID 9 from Port A.. Encoder Field ID for Previous Field
17	PRTA_SRC8_CURR_ENC_FID	R	1h	For Source ID 8 from Port A.. Encoder Field ID for Current Field

Table 1-490. VIP_PARSER_output_port_a_enc_fid Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRTA_SRC8_PREV_ENC_FID	R	1h	For Source ID 8 from Port A.. Encoder Field ID for Previous Field
15	PRTA_SRC7_CURR_ENC_FID	R	1h	For Source ID 7 from Port A.. Encoder Field ID for Current Field
14	PRTA_SRC7_PREV_ENC_FID	R	1h	For Source ID 7 from Port A.. Encoder Field ID for Previous Field
13	PRTA_SRC6_CURR_ENC_FID	R	1h	For Source ID 6 from Port A.. Encoder Field ID for Current Field
12	PRTA_SRC6_PREV_ENC_FID	R	1h	For Source ID 6 from Port A.. Encoder Field ID for Previous Field
11	PRTA_SRC5_CURR_ENC_FID	R	1h	For Source ID 5 from Port A.. Encoder Field ID for Current Field
10	PRTA_SRC5_PREV_ENC_FID	R	1h	For Source ID 5 from Port A.. Encoder Field ID for Previous Field
9	PRTA_SRC4_CURR_ENC_FID	R	1h	For Source ID 4 from Port A.. Encoder Field ID for Current Field
8	PRTA_SRC4_PREV_ENC_FID	R	1h	For Source ID 4 from Port A.. Encoder Field ID for Previous Field
7	PRTA_SRC3_CURR_ENC_FID	R	1h	For Source ID 3 from Port A.. Encoder Field ID for Current Field
6	PRTA_SRC3_PREV_ENC_FID	R	1h	For Source ID 3 from Port A.. Encoder Field ID for Previous Field
5	PRTA_SRC2_CURR_ENC_FID	R	1h	For Source ID 2 from Port A.. Encoder Field ID for Current Field
4	PRTA_SRC2_PREV_ENC_FID	R	1h	For Source ID 2 from Port A.. Encoder Field ID for Previous Field
3	PRTA_SRC1_CURR_ENC_FID	R	1h	For Source ID 1 from Port A.. Encoder Field ID for Current Field
2	PRTA_SRC1_PREV_ENC_FID	R	1h	For Source ID 1 from Port A.. Encoder Field ID for Previous Field
1	PRTA_SRC0_CURR_ENC_FID	R	1h	For Source ID 0 from Port A.. Encoder Field ID for Current Field
0	PRTA_SRC0_PREV_ENC_FID	R	1h	For Source ID 0 from Port A.. Encoder Field ID for Previous Field

1.3.14.11 VIP_PARSER_output_port_b_src_fid Register (offset = 28h) [reset = FFFFFFFFh]

VIP_PARSER_output_port_b_src_fid is shown in Figure 1-573 and described in Table 1-491.

Current and Previous Output Port B Source FID values

Figure 1-573. VIP_PARSER_output_port_b_src_fid Register

31	30	29	28	27	26	25	24
PRTB_SRC15_CURR_SOURCE_FID	PRTB_SRC15_PREV_SOURCE_FID	PRTB_SRC14_CURR_SOURCE_FID	PRTB_SRC14_PREV_SOURCE_FID	PRTB_SRC13_CURR_SOURCE_FID	PRTB_SRC13_PREV_SOURCE_FID	PRTB_SRC12_CURR_SOURCE_FID	PRTB_SRC12_PREV_SOURCE_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
23	22	21	20	19	18	17	16
PRTB_SRC11_CURR_SOURCE_FID	PRTB_SRC11_PREV_SOURCE_FID	PRTB_SRC10_CURR_SOURCE_FID	PRTB_SRC10_PREV_SOURCE_FID	PRTB_SRC9_CURR_SOURCE_FID	PRTB_SRC9_PREV_SOURCE_FID	PRTB_SRC8_CURR_SOURCE_FID	PRTB_SRC8_PREV_SOURCE_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
15	14	13	12	11	10	9	8
PRTB_SRC7_CURR_SOURCE_FID	PRTB_SRC7_PREV_SOURCE_FID	PRTB_SRC6_CURR_SOURCE_FID	PRTB_SRC6_PREV_SOURCE_FID	PRTB_SRC5_CURR_SOURCE_FID	PRTB_SRC5_PREV_SOURCE_FID	PRTB_SRC4_CURR_SOURCE_FID	PRTB_SRC4_PREV_SOURCE_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
PRTB_SRC3_CURR_SOURCE_FID	PRTB_SRC3_PREV_SOURCE_FID	PRTB_SRC2_CURR_SOURCE_FID	PRTB_SRC2_PREV_SOURCE_FID	PRTB_SRC1_CURR_SOURCE_FID	PRTB_SRC1_PREV_SOURCE_FID	PRTB_SRC0_CURR_SOURCE_FID	PRTB_SRC0_PREV_SOURCE_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-491. VIP_PARSER_output_port_b_src_fid Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRTB_SRC15_CURR_SOURCE_FID	R	1h	For Source ID 15 from Port B.. Source Field ID for Current Field
30	PRTB_SRC15_PREV_SOURCE_FID	R	1h	For Source ID 15 from Port B.. Source Field ID for Previous Field
29	PRTB_SRC14_CURR_SOURCE_FID	R	1h	For Source ID 14 from Port B.. Source Field ID for Current Field
28	PRTB_SRC14_PREV_SOURCE_FID	R	1h	For Source ID 14 from Port B.. Source Field ID for Previous Field
27	PRTB_SRC13_CURR_SOURCE_FID	R	1h	For Source ID 13 from Port B.. Source Field ID for Current Field
26	PRTB_SRC13_PREV_SOURCE_FID	R	1h	For Source ID 13 from Port B.. Source Field ID for Previous Field
25	PRTB_SRC12_CURR_SOURCE_FID	R	1h	For Source ID 12 from Port B.. Source Field ID for Current Field
24	PRTB_SRC12_PREV_SOURCE_FID	R	1h	For Source ID 12 from Port B.. Source Field ID for Previous Field
23	PRTB_SRC11_CURR_SOURCE_FID	R	1h	For Source ID 11 from Port B.. Source Field ID for Current Field
22	PRTB_SRC11_PREV_SOURCE_FID	R	1h	For Source ID 11.. from Port B Source Field ID for Previous Field
21	PRTB_SRC10_CURR_SOURCE_FID	R	1h	For Source ID 10 from Port B.. Source Field ID for Current Field
20	PRTB_SRC10_PREV_SOURCE_FID	R	1h	For Source ID 10 from Port B.. Source Field ID for Previous Field
19	PRTB_SRC9_CURR_SOURCE_FID	R	1h	For Source ID 9 from Port B.. Source Field ID for Current Field
18	PRTB_SRC9_PREV_SOURCE_FID	R	1h	For Source ID 9 from Port B.. Source Field ID for Previous Field
17	PRTB_SRC8_CURR_SOURCE_FID	R	1h	For Source ID 8 from Port B.. Source Field ID for Current Field

Table 1-491. VIP_PARSER_output_port_b_src_fid Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRTB_SRC8_PREV_SOURCE_FID	R	1h	For Source ID 8 from Port B.. Source Field ID for Previous Field
15	PRTB_SRC7_CURR_SOURCE_FID	R	1h	For Source ID 7 from Port B.. Source Field ID for Current Field
14	PRTB_SRC7_PREV_SOURCE_FID	R	1h	For Source ID 7 from Port B.. Source Field ID for Previous Field
13	PRTB_SRC6_CURR_SOURCE_FID	R	1h	For Source ID 6 from Port B.. Source Field ID for Current Field
12	PRTB_SRC6_PREV_SOURCE_FID	R	1h	For Source ID 6 from Port B.. Source Field ID for Previous Field
11	PRTB_SRC5_CURR_SOURCE_FID	R	1h	For Source ID 5 from Port B.. Source Field ID for Current Field
10	PRTB_SRC5_PREV_SOURCE_FID	R	1h	For Source ID 5 from Port B.. Source Field ID for Previous Field
9	PRTB_SRC4_CURR_SOURCE_FID	R	1h	For Source ID 4 from Port B.. Source Field ID for Current Field
8	PRTB_SRC4_PREV_SOURCE_FID	R	1h	For Source ID 4 from Port B.. Source Field ID for Previous Field
7	PRTB_SRC3_CURR_SOURCE_FID	R	1h	For Source ID 3 from Port B.. Source Field ID for Current Field
6	PRTB_SRC3_PREV_SOURCE_FID	R	1h	For Source ID 3 from Port B.. Source Field ID for Previous Field
5	PRTB_SRC2_CURR_SOURCE_FID	R	1h	For Source ID 2 from Port B.. Source Field ID for Current Field
4	PRTB_SRC2_PREV_SOURCE_FID	R	1h	For Source ID 2 from Port B.. Source Field ID for Previous Field
3	PRTB_SRC1_CURR_SOURCE_FID	R	1h	For Source ID 1 from Port B.. Source Field ID for Current Field
2	PRTB_SRC1_PREV_SOURCE_FID	R	1h	For Source ID 1 from Port B.. Source Field ID for Previous Field
1	PRTB_SRC0_CURR_SOURCE_FID	R	1h	For Source ID 0 from Port B.. Source Field ID for Current Field
0	PRTB_SRC0_PREV_SOURCE_FID	R	1h	For Source ID 0 from Port B.. Source Field ID for Previous Field

1.3.14.12 VIP_PARSER_output_port_b_enc_fid Register (offset = 2Ch) [reset = FFFFFFFFh]

VIP_PARSER_output_port_b_enc_fid is shown in Figure 1-574 and described in Table 1-492.

Current and Previous Output Port B Encoder FID values

Figure 1-574. VIP_PARSER_output_port_b_enc_fid Register

31	30	29	28	27	26	25	24
PRTB_SRC15_CURR_ENC_FID	PRTB_SRC15_PREV_ENC_FID	PRTB_SRC14_CURR_ENC_FID	PRTB_SRC14_PREV_ENC_FID	PRTB_SRC13_CURR_ENC_FID	PRTB_SRC13_PREV_ENC_FID	PRTB_SRC12_CURR_ENC_FID	PRTB_SRC12_PREV_ENC_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
23	22	21	20	19	18	17	16
PRTB_SRC11_CURR_ENC_FID	PRTB_SRC11_PREV_ENC_FID	PRTB_SRC10_CURR_ENC_FID	PRTB_SRC10_PREV_ENC_FID	PRTB_SRC9_CURR_ENC_FID	PRTB_SRC9_PREV_ENC_FID	PRTB_SRC8_CURR_ENC_FID	PRTB_SRC8_PREV_ENC_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
15	14	13	12	11	10	9	8
PRTB_SRC7_CURR_ENC_FID	PRTB_SRC7_PREV_ENC_FID	PRTB_SRC6_CURR_ENC_FID	PRTB_SRC6_PREV_ENC_FID	PRTB_SRC5_CURR_ENC_FID	PRTB_SRC5_PREV_ENC_FID	PRTB_SRC4_CURR_ENC_FID	PRTB_SRC4_PREV_ENC_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
PRTB_SRC3_CURR_ENC_FID	PRTB_SRC3_PREV_ENC_FID	PRTB_SRC2_CURR_ENC_FID	PRTB_SRC2_PREV_ENC_FID	PRTB_SRC1_CURR_ENC_FID	PRTB_SRC1_PREV_ENC_FID	PRTB_SRC0_CURR_ENC_FID	PRTB_SRC0_PREV_ENC_FID
R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-492. VIP_PARSER_output_port_b_enc_fid Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRTB_SRC15_CURR_ENC_FID	R	1h	For Source ID 15 from Port B.. Encoder Field ID for Current Field
30	PRTB_SRC15_PREV_ENC_FID	R	1h	For Source ID 15 from Port B.. Encoder Field ID for Previous Field
29	PRTB_SRC14_CURR_ENC_FID	R	1h	For Source ID 14 from Port B.. Encoder Field ID for Current Field
28	PRTB_SRC14_PREV_ENC_FID	R	1h	For Source ID 14 from Port B.. Encoder Field ID for Previous Field
27	PRTB_SRC13_CURR_ENC_FID	R	1h	For Source ID 13 from Port B.. Encoder Field ID for Current Field
26	PRTB_SRC13_PREV_ENC_FID	R	1h	For Source ID 13 from Port B.. Encoder Field ID for Previous Field
25	PRTB_SRC12_CURR_ENC_FID	R	1h	For Source ID 12 from Port B.. Encoder Field ID for Current Field
24	PRTB_SRC12_PREV_ENC_FID	R	1h	For Source ID 12 from Port B.. Encoder Field ID for Previous Field
23	PRTB_SRC11_CURR_ENC_FID	R	1h	For Source ID 11 from Port B.. Encoder Field ID for Current Field
22	PRTB_SRC11_PREV_ENC_FID	R	1h	For Source ID 11 from Port B.. Encoder Field ID for Previous Field
21	PRTB_SRC10_CURR_ENC_FID	R	1h	For Source ID 10 from Port B.. Encoder Field ID for Current Field
20	PRTB_SRC10_PREV_ENC_FID	R	1h	For Source ID 10 from Port B.. Encoder Field ID for Previous Field
19	PRTB_SRC9_CURR_ENC_FID	R	1h	For Source ID 9 from Port B.. Encoder Field ID for Current Field
18	PRTB_SRC9_PREV_ENC_FID	R	1h	For Source ID 9 from Port B.. Encoder Field ID for Previous Field
17	PRTB_SRC8_CURR_ENC_FID	R	1h	For Source ID 8 from Port B.. Encoder Field ID for Current Field

Table 1-492. VIP_PARSER_output_port_b_enc_fid Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRTB_SRC8_PREV_ENC_FID	R	1h	For Source ID 8 from Port B.. Encoder Field ID for Previous Field
15	PRTB_SRC7_CURR_ENC_FID	R	1h	For Source ID 7 from Port B.. Encoder Field ID for Current Field
14	PRTB_SRC7_PREV_ENC_FID	R	1h	For Source ID 7 from Port B.. Encoder Field ID for Previous Field
13	PRTB_SRC6_CURR_ENC_FID	R	1h	For Source ID 6 from Port B.. Encoder Field ID for Current Field
12	PRTB_SRC6_PREV_ENC_FID	R	1h	For Source ID 6 from Port B.. Encoder Field ID for Previous Field
11	PRTB_SRC5_CURR_ENC_FID	R	1h	For Source ID 5 from Port B.. Encoder Field ID for Current Field
10	PRTB_SRC5_PREV_ENC_FID	R	1h	For Source ID 5 from Port B.. Encoder Field ID for Previous Field
9	PRTB_SRC4_CURR_ENC_FID	R	1h	For Source ID 4 from Port B.. Encoder Field ID for Current Field
8	PRTB_SRC4_PREV_ENC_FID	R	1h	For Source ID 4 from Port B.. Encoder Field ID for Previous Field
7	PRTB_SRC3_CURR_ENC_FID	R	1h	For Source ID 3 from Port B.. Encoder Field ID for Current Field
6	PRTB_SRC3_PREV_ENC_FID	R	1h	For Source ID 3 from Port B.. Encoder Field ID for Previous Field
5	PRTB_SRC2_CURR_ENC_FID	R	1h	For Source ID 2 from Port B.. Encoder Field ID for Current Field
4	PRTB_SRC2_PREV_ENC_FID	R	1h	For Source ID 2 from Port B.. Encoder Field ID for Previous Field
3	PRTB_SRC1_CURR_ENC_FID	R	1h	For Source ID 1 from Port B.. Encoder Field ID for Current Field
2	PRTB_SRC1_PREV_ENC_FID	R	1h	For Source ID 1 from Port B.. Encoder Field ID for Previous Field
1	PRTB_SRC0_CURR_ENC_FID	R	1h	For Source ID 0 from Port B.. Encoder Field ID for Current Field
0	PRTB_SRC0_PREV_ENC_FID	R	1h	For Source ID 0 from Port B.. Encoder Field ID for Previous Field

1.3.14.13 VIP_PARSER_output_port_a_src0_size Register (offset = 30h) [reset = 0h]

VIP_PARSER_output_port_a_src0_size is shown in Figure 1-575 and described in Table 1-493.

Width and Height for Source 0

Figure 1-575. VIP_PARSER_output_port_a_src0_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC0_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC0_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC0_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC0_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-493. VIP_PARSER_output_port_a_src0_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC0_WIDTH	R	0h	On Port A.. Width of Source ID 0
15-11	Reserved	R	0h	
10-0	PRTA_SRC0_HEIGHT	R	0h	On Port A.. Height of Source ID 0

1.3.14.14 VIP_PARSER_output_port_a_src1_size Register (offset = 34h) [reset = 0h]

VIP_PARSER_output_port_a_src1_size is shown in Figure 1-576 and described in Table 1-494.

Width and Height for Source 1

Figure 1-576. VIP_PARSER_output_port_a_src1_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC1_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC1_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC1_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC1_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-494. VIP_PARSER_output_port_a_src1_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC1_WIDTH	R	0h	On Port A.. Width of Source ID 1
15-11	Reserved	R	0h	
10-0	PRTA_SRC1_HEIGHT	R	0h	On Port A.. Height of Source ID 1

1.3.14.15 VIP_PARSER_output_port_a_src2_size Register (offset = 38h) [reset = 0h]

VIP_PARSER_output_port_a_src2_size is shown in Figure 1-577 and described in Table 1-495.

Width and Height for Source 2

Figure 1-577. VIP_PARSER_output_port_a_src2_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC2_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC2_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC2_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC2_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-495. VIP_PARSER_output_port_a_src2_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC2_WIDTH	R	0h	On Port A.. Width of Source ID 2
15-11	Reserved	R	0h	
10-0	PRTA_SRC2_HEIGHT	R	0h	On Port A.. Height of Source ID 2

1.3.14.16 VIP_PARSER_output_port_a_src3_size Register (offset = 3Ch) [reset = 0h]

VIP_PARSER_output_port_a_src3_size is shown in Figure 1-578 and described in Table 1-496.

Width and Height for Source 3

Figure 1-578. VIP_PARSER_output_port_a_src3_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC3_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC3_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC3_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC3_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-496. VIP_PARSER_output_port_a_src3_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC3_WIDTH	R	0h	On Port A.. Width of Source ID 3
15-11	Reserved	R	0h	
10-0	PRTA_SRC3_HEIGHT	R	0h	On Port A.. Height of Source ID 3

1.3.14.17 VIP_PARSER_output_port_a_src4_size Register (offset = 40h) [reset = 0h]

VIP_PARSER_output_port_a_src4_size is shown in Figure 1-579 and described in Table 1-497.

Width and Height for Source 4

Figure 1-579. VIP_PARSER_output_port_a_src4_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC4_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC4_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC4_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC4_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-497. VIP_PARSER_output_port_a_src4_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC4_WIDTH	R	0h	On Port A.. Width of Source ID 4
15-11	Reserved	R	0h	
10-0	PRTA_SRC4_HEIGHT	R	0h	On Port A.. Height of Source ID 4

1.3.14.18 VIP_PARSER_output_port_a_src5_size Register (offset = 44h) [reset = 0h]

VIP_PARSER_output_port_a_src5_size is shown in Figure 1-580 and described in Table 1-498.

Width and Height for Source 5

Figure 1-580. VIP_PARSER_output_port_a_src5_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC5_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC5_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC5_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC5_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-498. VIP_PARSER_output_port_a_src5_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC5_WIDTH	R	0h	On Port A.. Width of Source ID 5
15-11	Reserved	R	0h	
10-0	PRTA_SRC5_HEIGHT	R	0h	On Port A.. Height of Source ID 5

1.3.14.19 VIP_PARSER_output_port_a_src6_size Register (offset = 48h) [reset = 0h]

VIP_PARSER_output_port_a_src6_size is shown in Figure 1-581 and described in Table 1-499.

Width and Height for Source 6

Figure 1-581. VIP_PARSER_output_port_a_src6_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC6_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC6_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC6_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC6_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-499. VIP_PARSER_output_port_a_src6_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC6_WIDTH	R	0h	On Port A.. Width of Source ID 6
15-11	Reserved	R	0h	
10-0	PRTA_SRC6_HEIGHT	R	0h	On Port A.. Height of Source ID 6

1.3.14.20 VIP_PARSER_output_port_a_src7_size Register (offset = 4Ch) [reset = 0h]

VIP_PARSER_output_port_a_src7_size is shown in Figure 1-582 and described in Table 1-500.

Width and Height for Source 7

Figure 1-582. VIP_PARSER_output_port_a_src7_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC7_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC7_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC7_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC7_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-500. VIP_PARSER_output_port_a_src7_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC7_WIDTH	R	0h	On Port A.. Width of Source ID 7
15-11	Reserved	R	0h	
10-0	PRTA_SRC7_HEIGHT	R	0h	On Port A.. Height of Source ID 7

1.3.14.21 VIP_PARSER_output_port_a_src8_size Register (offset = 50h) [reset = 0h]

VIP_PARSER_output_port_a_src8_size is shown in Figure 1-583 and described in Table 1-501.

Width and Height for Source 8

Figure 1-583. VIP_PARSER_output_port_a_src8_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC8_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC8_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC8_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC8_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-501. VIP_PARSER_output_port_a_src8_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC8_WIDTH	R	0h	On Port A.. Width of Source ID 8
15-11	Reserved	R	0h	
10-0	PRTA_SRC8_HEIGHT	R	0h	On Port A.. Height of Source ID 8

1.3.14.22 VIP_PARSER_output_port_a_src9_size Register (offset = 54h) [reset = 0h]

VIP_PARSER_output_port_a_src9_size is shown in Figure 1-584 and described in Table 1-502.

Width and Height for Source 9

Figure 1-584. VIP_PARSER_output_port_a_src9_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC9_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC9_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC9_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC9_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-502. VIP_PARSER_output_port_a_src9_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC9_WIDTH	R	0h	On Port A.. Width of Source ID 9
15-11	Reserved	R	0h	
10-0	PRTA_SRC9_HEIGHT	R	0h	On Port A.. Height of Source ID 9

1.3.14.23 VIP_PARSER_output_port_a_src10_size Register (offset = 58h) [reset = 0h]

VIP_PARSER_output_port_a_src10_size is shown in Figure 1-585 and described in Table 1-503.

Width and Height for Source 10

Figure 1-585. VIP_PARSER_output_port_a_src10_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC10_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC10_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC10_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC10_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-503. VIP_PARSER_output_port_a_src10_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC10_WIDTH	R	0h	On Port A.. Width of Source ID 10
15-11	Reserved	R	0h	
10-0	PRTA_SRC10_HEIGHT	R	0h	On Port A.. Height of Source ID 10

1.3.14.24 VIP_PARSER_output_port_a_src11_size Register (offset = 5Ch) [reset = 0h]

VIP_PARSER_output_port_a_src11_size is shown in Figure 1-586 and described in Table 1-504.

Width and Height for Source 11

Figure 1-586. VIP_PARSER_output_port_a_src11_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC11_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC11_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC11_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC11_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-504. VIP_PARSER_output_port_a_src11_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC11_WIDTH	R	0h	On Port A.. Width of Source ID 11
15-11	Reserved	R	0h	
10-0	PRTA_SRC11_HEIGHT	R	0h	On Port A.. Height of Source ID 11

1.3.14.25 VIP_PARSER_output_port_a_src12_size Register (offset = 60h) [reset = 0h]

VIP_PARSER_output_port_a_src12_size is shown in Figure 1-587 and described in Table 1-505.

Width and Height for Source 12

Figure 1-587. VIP_PARSER_output_port_a_src12_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC12_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC12_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC12_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC12_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-505. VIP_PARSER_output_port_a_src12_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC12_WIDTH	R	0h	On Port A.. Width of Source ID 12
15-11	Reserved	R	0h	
10-0	PRTA_SRC12_HEIGHT	R	0h	On Port A.. Height of Source ID 12

1.3.14.26 VIP_PARSER_output_port_a_src13_size Register (offset = 64h) [reset = 0h]

VIP_PARSER_output_port_a_src13_size is shown in Figure 1-588 and described in Table 1-506.

Width and Height for Source 13

Figure 1-588. VIP_PARSER_output_port_a_src13_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC13_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC13_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC13_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC13_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-506. VIP_PARSER_output_port_a_src13_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC13_WIDTH	R	0h	On Port A.. Width of Source ID 13
15-11	Reserved	R	0h	
10-0	PRTA_SRC13_HEIGHT	R	0h	On Port A.. Height of Source ID 13

1.3.14.27 VIP_PARSER_output_port_a_src14_size Register (offset = 68h) [reset = 0h]

VIP_PARSER_output_port_a_src14_size is shown in Figure 1-589 and described in Table 1-507.

Width and Height for Source 14

Figure 1-589. VIP_PARSER_output_port_a_src14_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC14_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC14_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC14_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC14_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-507. VIP_PARSER_output_port_a_src14_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC14_WIDTH	R	0h	On Port A.. Width of Source ID 14
15-11	Reserved	R	0h	
10-0	PRTA_SRC14_HEIGHT	R	0h	On Port A.. Height of Source ID 14

1.3.14.28 VIP_PARSER_output_port_a_src15_size Register (offset = 6Ch) [reset = 0h]

VIP_PARSER_output_port_a_src15_size is shown in Figure 1-590 and described in Table 1-508.

Width and Height for Source 15

Figure 1-590. VIP_PARSER_output_port_a_src15_size Register

31	30	29	28	27	26	25	24
Reserved					PRTA_SRC15_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTA_SRC15_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTA_SRC15_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTA_SRC15_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-508. VIP_PARSER_output_port_a_src15_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTA_SRC15_WIDTH	R	0h	On Port A.. Width of Source ID 15
15-11	Reserved	R	0h	
10-0	PRTA_SRC15_HEIGHT	R	0h	On Port A.. Height of Source ID 15

1.3.14.29 VIP_PARSER_output_port_b_src0_size Register (offset = 70h) [reset = 0h]

VIP_PARSER_output_port_b_src0_size is shown in Figure 1-591 and described in Table 1-509.

Width and Height for Source 0

Figure 1-591. VIP_PARSER_output_port_b_src0_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC0_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC0_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC0_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC0_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-509. VIP_PARSER_output_port_b_src0_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC0_WIDTH	R	0h	On Port B.. Width of Source ID 0
15-11	Reserved	R	0h	
10-0	PRTB_SRC0_HEIGHT	R	0h	On Port B.. Height of Source ID 0

1.3.14.30 VIP_PARSER_output_port_b_src1_size Register (offset = 74h) [reset = 0h]

VIP_PARSER_output_port_b_src1_size is shown in Figure 1-592 and described in Table 1-510.

Width and Height for Source 1

Figure 1-592. VIP_PARSER_output_port_b_src1_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC1_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC1_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC1_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC1_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-510. VIP_PARSER_output_port_b_src1_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC1_WIDTH	R	0h	On Port B.. Width of Source ID 1
15-11	Reserved	R	0h	
10-0	PRTB_SRC1_HEIGHT	R	0h	On Port B.. Height of Source ID 1

1.3.14.31 VIP_PARSER_output_port_b_src2_size Register (offset = 78h) [reset = 0h]

VIP_PARSER_output_port_b_src2_size is shown in Figure 1-593 and described in Table 1-511.

Width and Height for Source 2

Figure 1-593. VIP_PARSER_output_port_b_src2_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC2_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC2_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC2_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC2_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-511. VIP_PARSER_output_port_b_src2_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC2_WIDTH	R	0h	On Port B.. Width of Source ID 2
15-11	Reserved	R	0h	
10-0	PRTB_SRC2_HEIGHT	R	0h	On Port B.. Height of Source ID 2

1.3.14.32 VIP_PARSER_output_port_b_src3_size Register (offset = 7Ch) [reset = 0h]

VIP_PARSER_output_port_b_src3_size is shown in Figure 1-594 and described in Table 1-512.

Width and Height for Source 3

Figure 1-594. VIP_PARSER_output_port_b_src3_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC3_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC3_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC3_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC3_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-512. VIP_PARSER_output_port_b_src3_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC3_WIDTH	R	0h	On Port B.. Width of Source ID 3
15-11	Reserved	R	0h	
10-0	PRTB_SRC3_HEIGHT	R	0h	On Port B.. Height of Source ID 3

1.3.14.33 VIP_PARSER_output_port_b_src4_size Register (offset = 80h) [reset = 0h]

VIP_PARSER_output_port_b_src4_size is shown in Figure 1-595 and described in Table 1-513.

Width and Height for Source 4

Figure 1-595. VIP_PARSER_output_port_b_src4_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC4_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC4_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC4_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC4_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-513. VIP_PARSER_output_port_b_src4_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC4_WIDTH	R	0h	On Port B.. Width of Source ID 4
15-11	Reserved	R	0h	
10-0	PRTB_SRC4_HEIGHT	R	0h	On Port B.. Height of Source ID 4

1.3.14.34 VIP_PARSER_output_port_b_src5_size Register (offset = 84h) [reset = 0h]

VIP_PARSER_output_port_b_src5_size is shown in Figure 1-596 and described in Table 1-514.

Width and Height for Source 5

Figure 1-596. VIP_PARSER_output_port_b_src5_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC5_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC5_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC5_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC5_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-514. VIP_PARSER_output_port_b_src5_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC5_WIDTH	R	0h	On Port B.. Width of Source ID 5
15-11	Reserved	R	0h	
10-0	PRTB_SRC5_HEIGHT	R	0h	On Port B.. Height of Source ID 5

1.3.14.35 VIP_PARSER_output_port_b_src6_size Register (offset = 88h) [reset = 0h]

VIP_PARSER_output_port_b_src6_size is shown in Figure 1-597 and described in Table 1-515.

Width and Height for Source 6

Figure 1-597. VIP_PARSER_output_port_b_src6_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC6_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC6_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC6_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC6_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-515. VIP_PARSER_output_port_b_src6_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC6_WIDTH	R	0h	On Port B.. Width of Source ID 6
15-11	Reserved	R	0h	
10-0	PRTB_SRC6_HEIGHT	R	0h	On Port B.. Height of Source ID 6

1.3.14.36 VIP_PARSER_output_port_b_src7_size Register (offset = 8Ch) [reset = 0h]

VIP_PARSER_output_port_b_src7_size is shown in Figure 1-598 and described in Table 1-516.

Width and Height for Source 7

Figure 1-598. VIP_PARSER_output_port_b_src7_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC7_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC7_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC7_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC7_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-516. VIP_PARSER_output_port_b_src7_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC7_WIDTH	R	0h	On Port B.. Width of Source ID 7
15-11	Reserved	R	0h	
10-0	PRTB_SRC7_HEIGHT	R	0h	On Port B.. Height of Source ID 7

1.3.14.37 VIP_PARSER_output_port_b_src8_size Register (offset = 90h) [reset = 0h]

VIP_PARSER_output_port_b_src8_size is shown in Figure 1-599 and described in Table 1-517.

Width and Height for Source 8

Figure 1-599. VIP_PARSER_output_port_b_src8_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC8_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC8_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC8_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC8_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-517. VIP_PARSER_output_port_b_src8_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC8_WIDTH	R	0h	On Port B.. Width of Source ID 8
15-11	Reserved	R	0h	
10-0	PRTB_SRC8_HEIGHT	R	0h	On Port B.. Height of Source ID 8

1.3.14.38 VIP_PARSER_output_port_b_src9_size Register (offset = 94h) [reset = 0h]

VIP_PARSER_output_port_b_src9_size is shown in Figure 1-600 and described in Table 1-518.

Width and Height for Source 9

Figure 1-600. VIP_PARSER_output_port_b_src9_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC9_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC9_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC9_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC9_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-518. VIP_PARSER_output_port_b_src9_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC9_WIDTH	R	0h	On Port B.. Width of Source ID 9
15-11	Reserved	R	0h	
10-0	PRTB_SRC9_HEIGHT	R	0h	On Port B.. Height of Source ID 9

1.3.14.39 VIP_PARSER_output_port_b_src10_size Register (offset = 98h) [reset = 0h]

VIP_PARSER_output_port_b_src10_size is shown in Figure 1-601 and described in Table 1-519.

Width and Height for Source 10

Figure 1-601. VIP_PARSER_output_port_b_src10_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC10_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC10_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC10_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC10_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-519. VIP_PARSER_output_port_b_src10_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC10_WIDTH	R	0h	On Port B.. Width of Source ID 10
15-11	Reserved	R	0h	
10-0	PRTB_SRC10_HEIGHT	R	0h	On Port B.. Height of Source ID 10

1.3.14.40 VIP_PARSER_output_port_b_src11_size Register (offset = 9Ch) [reset = 0h]

VIP_PARSER_output_port_b_src11_size is shown in Figure 1-602 and described in Table 1-520.

Width and Height for Source 11

Figure 1-602. VIP_PARSER_output_port_b_src11_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC11_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC11_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC11_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC11_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-520. VIP_PARSER_output_port_b_src11_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC11_WIDTH	R	0h	On Port B.. Width of Source ID 11
15-11	Reserved	R	0h	
10-0	PRTB_SRC11_HEIGHT	R	0h	On Port B.. Height of Source ID 11

1.3.14.41 VIP_PARSER_output_port_b_src12_size Register (offset = A0h) [reset = 0h]

VIP_PARSER_output_port_b_src12_size is shown in Figure 1-603 and described in Table 1-521.

Width and Height for Source 12

Figure 1-603. VIP_PARSER_output_port_b_src12_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC12_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC12_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC12_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC12_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-521. VIP_PARSER_output_port_b_src12_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC12_WIDTH	R	0h	On Port B.. Width of Source ID 12
15-11	Reserved	R	0h	
10-0	PRTB_SRC12_HEIGHT	R	0h	On Port B.. Height of Source ID 12

1.3.14.42 VIP_PARSER_output_port_b_src13_size Register (offset = A4h) [reset = 0h]

VIP_PARSER_output_port_b_src13_size is shown in Figure 1-604 and described in Table 1-522.

Width and Height for Source 13

Figure 1-604. VIP_PARSER_output_port_b_src13_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC13_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC13_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC13_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC13_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-522. VIP_PARSER_output_port_b_src13_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC13_WIDTH	R	0h	On Port B.. Width of Source ID 13
15-11	Reserved	R	0h	
10-0	PRTB_SRC13_HEIGHT	R	0h	On Port B.. Height of Source ID 13

1.3.14.43 VIP_PARSER_output_port_b_src14_size Register (offset = A8h) [reset = 0h]

VIP_PARSER_output_port_b_src14_size is shown in Figure 1-605 and described in Table 1-523.

Width and Height for Source 14

Figure 1-605. VIP_PARSER_output_port_b_src14_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC14_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC14_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC14_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC14_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-523. VIP_PARSER_output_port_b_src14_size Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC14_WIDTH	R	0h	On Port B.. Width of Source ID 14
15-11	Reserved	R	0h	
10-0	PRTB_SRC14_HEIGHT	R	0h	On Port B.. Height of Source ID 14

1.3.14.44 VIP_PARSER_output_port_b_src15_size Register (offset = ACh) [reset = 0h]

VIP_PARSER_output_port_b_src15_size is shown in Figure 1-606 and described in Table 1-524.

Width and Height for Source 15

Figure 1-606. VIP_PARSER_output_port_b_src15_size Register

31	30	29	28	27	26	25	24
Reserved					PRTB_SRC15_WIDTH		
R-0h					R-0h		

23	22	21	20	19	18	17	16
PRTB_SRC15_WIDTH							
R-0h							

15	14	13	12	11	10	9	8
Reserved					PRTB_SRC15_HEIGHT		
R-0h					R-0h		

7	6	5	4	3	2	1	0
PRTB_SRC15_HEIGHT							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-524. VIP_PARSER_output_port_b_src15_size Register Field Descriptions

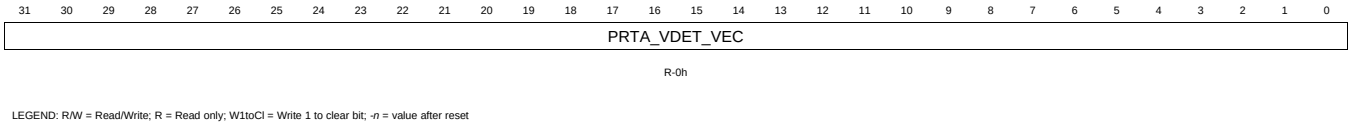
Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	PRTB_SRC15_WIDTH	R	0h	On Port B.. Width of Source ID 15
15-11	Reserved	R	0h	
10-0	PRTB_SRC15_HEIGHT	R	0h	On Port B.. Height of Source ID 15

1.3.14.45 VIP_PARSER_port_a_vdet_vec Register (offset = B0h) [reset = 0h]

VIP_PARSER_port_a_vdet_vec is shown in Figure 1-607 and described in Table 1-525.

Each bit represents the VDET bit setting for Line Mux Mode

Figure 1-607. VIP_PARSER_port_a_vdet_vec Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-525. VIP_PARSER_port_a_vdet_vec Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRTA_VDET_VEC	R	0h	For Embedded Sync Only In Line Mux Mode.. each bit represents the vdet value on Port A for the corresponding source id. This vector is meaningless for 1x/2x/4x mux modes.

1.3.14.46 VIP_PARSER_port_b_vdet_vec Register (offset = B4h) [reset = 0h]

VIP_PARSER_port_b_vdet_vec is shown in Figure 1-608 and described in Table 1-526.

Each bit represents the VDET bit setting for Line Mux Mode

Figure 1-608. VIP_PARSER_port_b_vdet_vec Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRTB_VDET_VEC																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-526. VIP_PARSER_port_b_vdet_vec Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRTB_VDET_VEC	R	0h	For Embedded Sync Only In Line Mux Mode.. each bit represents the vdet value on Port B for the corresponding source id. This vector is meaningless for 1x/2x/4x mux modes.

1.3.14.47 VIP_PARSER_xtra2_port_a Register (offset = B8h) [reset = 0h]

VIP_PARSER_xtra2_port_a is shown in Figure 1-609 and described in Table 1-527.

Ancillary Cropping Configuration for Input Port A

Figure 1-609. VIP_PARSER_xtra2_port_a Register

31	30	29	28	27	26	25	24
ANC_TARGET_SRCNUM				Reserved	ANC_USE_NUMPIX		
R/W-0h				R-0h	R/W-0h		
23	22	21	20	19	18	17	16
ANC_USE_NUMPIX							
R/W-0h							
15	14	13	12	11	10	9	8
ANC_BYPASS_N	Reserved				ANC_SKIP_NUMPIX		
R/W-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ANC_SKIP_NUMPIX							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-527. VIP_PARSER_xtra2_port_a Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ANC_TARGET_SRCNUM	R/W	0h	The cropping module can work on only one srcnum, specified in this field, for each dss_vip_parser output port (Ancillary data).
27	Reserved	R	0h	
26-16	ANC_USE_NUMPIX	R/W	0h	When cropping, the number of pixels to keep after the skip_numpix value. skip_numpix + use_numpix must be smaller than the original line width.
15	ANC_BYPASS_N	R/W	0h	0 : Bypass cropping module 1 : Cropping module enabled
14-11	Reserved	R	0h	
10-0	ANC_SKIP_NUMPIX	R/W	0h	The number of pixels to crop from the beginning of each line.

1.3.14.48 VIP_PARSER_xtra3_port_a Register (offset = BCh) [reset = 0h]

VIP_PARSER_xtra3_port_a is shown in Figure 1-610 and described in Table 1-528.

Ancillary Cropping Configuration for Input Port A

Figure 1-610. VIP_PARSER_xtra3_port_a Register

31	30	29	28	27	26	25	24
Reserved					ANC_USE_NUMLINES		
R-0h					R/W-0h		

23	22	21	20	19	18	17	16
ANC_USE_NUMLINES							
R/W-0h							

15	14	13	12	11	10	9	8
Reserved					ANC_SKIP_NUMLINES		
R-0h					R/W-0h		

7	6	5	4	3	2	1	0
ANC_SKIP_NUMLINES							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-528. VIP_PARSER_xtra3_port_a Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	ANC_USE_NUMLINES	R/W	0h	When cropping, the number of lines to keep after the skip_numlines value. Use_numlines + skip_numlines must be smaller than the total number of lines in the srcnum's ancillary data region.
15-11	Reserved	R	0h	
10-0	ANC_SKIP_NUMLINES	R/W	0h	The number of lines to crop from the top of the vertical ancillary data region.

1.3.14.49 VIP_PARSER_xtra4_port_a Register (offset = C0h) [reset = 0h]

VIP_PARSER_xtra4_port_a is shown in Figure 1-611 and described in Table 1-529.

Active Video Cropping Configuration for Input Port A

Figure 1-611. VIP_PARSER_xtra4_port_a Register

31	30	29	28	27	26	25	24
ACT_TARGET_SRCNUM				Reserved	ACT_USE_NUMPIX		
R/W-0h				R-0h	R/W-0h		
23	22	21	20	19	18	17	16
ACT_USE_NUMPIX							
R/W-0h							
15	14	13	12	11	10	9	8
ACT_BYPASS_N	Reserved				ACT_SKIP_NUMPIX		
R/W-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ACT_SKIP_NUMPIX							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-529. VIP_PARSER_xtra4_port_a Register Field Descriptions

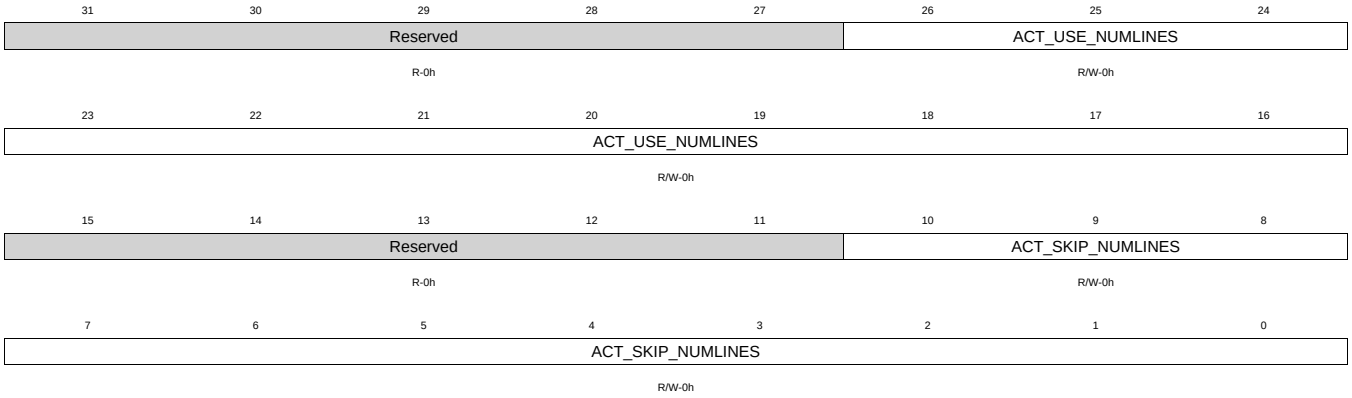
Bit	Field	Type	Reset	Description
31-28	ACT_TARGET_SRCNUM	R/W	0h	The cropping module can work on only one srcnum, specified in this field, for each dss_vip_parser output port (Active video).
27	Reserved	R	0h	
26-16	ACT_USE_NUMPIX	R/W	0h	When cropping, the number of pixels to keep after the skip_numpix value. skip_numpix + use_numpix must be smaller than the original line width.
15	ACT_BYPASS_N	R/W	0h	0 : Bypass cropping module 1 : Cropping module enabled
14-11	Reserved	R	0h	
10-0	ACT_SKIP_NUMPIX	R/W	0h	The number of pixels to crop from the beginning of each line.

1.3.14.50 VIP_PARSER_xtra5_port_a Register (offset = C4h) [reset = 0h]

VIP_PARSER_xtra5_port_a is shown in Figure 1-612 and described in Table 1-530.

Active Video Cropping Configuration for Input Port A

Figure 1-612. VIP_PARSER_xtra5_port_a Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-530. VIP_PARSER_xtra5_port_a Register Field Descriptions

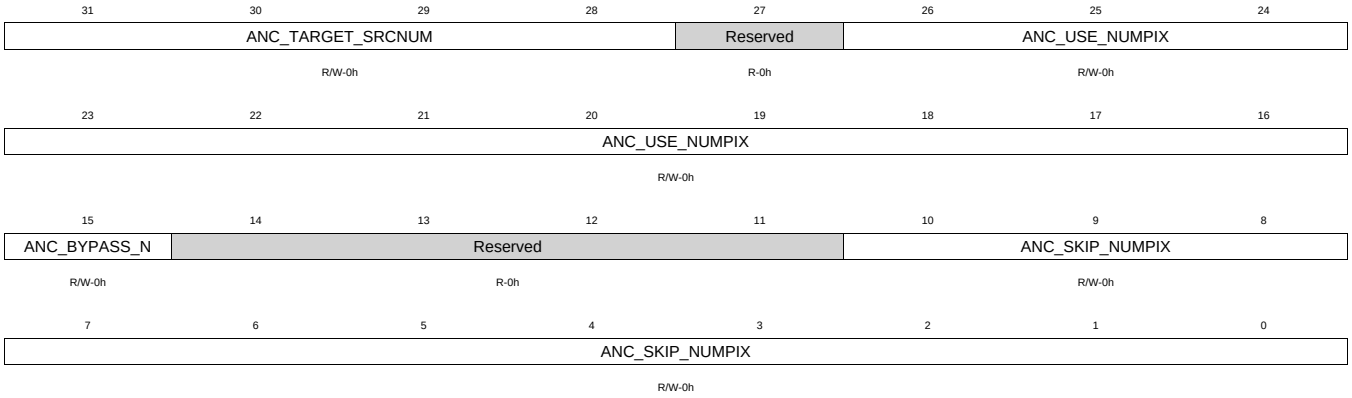
Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	ACT_USE_NUMLINES	R/W	0h	When cropping, the number of lines to keep after the skip_numlines value. Use_numlines + skip_numlines must be smaller than the total number of lines in the srcnum's active video region.
15-11	Reserved	R	0h	
10-0	ACT_SKIP_NUMLINES	R/W	0h	The number of lines to crop from the top of the vertical active video region.

1.3.14.51 VIP_PARSER_xtra2_port_b Register (offset = C8h) [reset = 0h]

VIP_PARSER_xtra2_port_b is shown in Figure 1-613 and described in Table 1-531.

Ancillary Cropping Configuration for Input Port B

Figure 1-613. VIP_PARSER_xtra2_port_b Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-531. VIP_PARSER_xtra2_port_b Register Field Descriptions

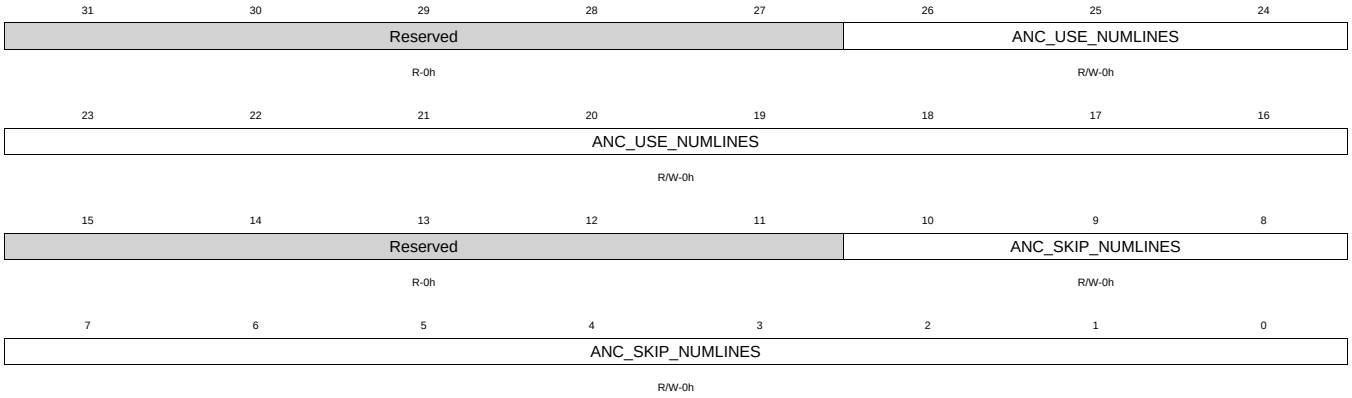
Bit	Field	Type	Reset	Description
31-28	ANC_TARGET_SRCNUM	R/W	0h	The cropping module can work on only one srcnum, specified in this field, for each dss_vip_parser output port (Ancillary data).
27	Reserved	R	0h	
26-16	ANC_USE_NUMPIX	R/W	0h	When cropping, the number of pixels to keep after the skip_numpix value. skip_numpix + use_numpix must be smaller than the original line width.
15	ANC_BYPASS_N	R/W	0h	0 : Bypass cropping module 1 : Cropping module enabled
14-11	Reserved	R	0h	
10-0	ANC_SKIP_NUMPIX	R/W	0h	The number of pixels to crop from the beginning of each line.

1.3.14.52 VIP_PARSER_xtra3_port_b Register (offset = CCh) [reset = 0h]

VIP_PARSER_xtra3_port_b is shown in Figure 1-614 and described in Table 1-532.

Ancillary Cropping Configuration for Input Port B

Figure 1-614. VIP_PARSER_xtra3_port_b Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-532. VIP_PARSER_xtra3_port_b Register Field Descriptions

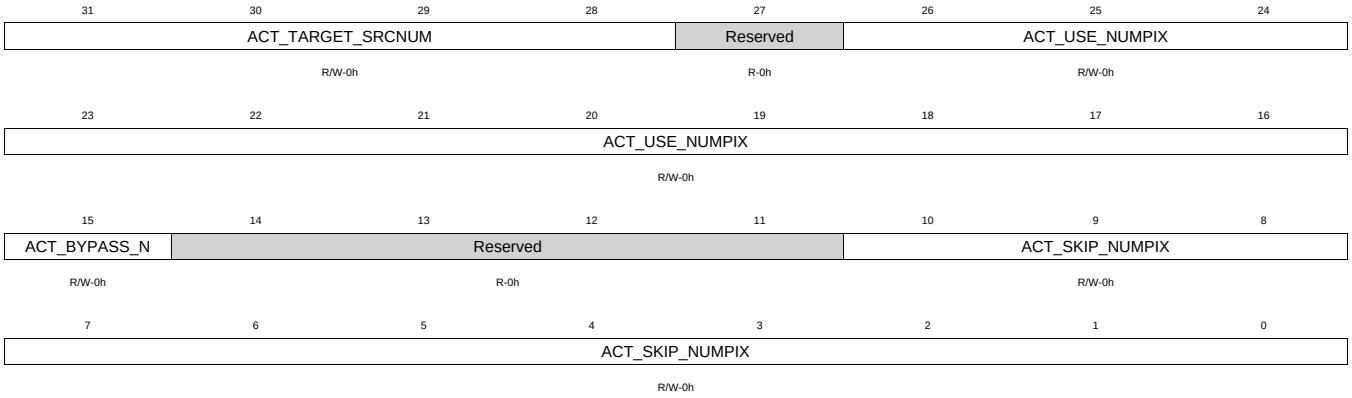
Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	ANC_USE_NUMLINES	R/W	0h	When cropping, the number of lines to keep after the skip_numlines value. Use_numlines + skip_numlines must be smaller than the total number of lines in the srcnum's ancillary data region.
15-11	Reserved	R	0h	
10-0	ANC_SKIP_NUMLINES	R/W	0h	The number of lines to crop from the top of the vertical ancillary data region.

1.3.14.53 VIP_PARSER_xtra4_port_b Register (offset = D0h) [reset = 0h]

VIP_PARSER_xtra4_port_b is shown in Figure 1-615 and described in Table 1-533.

Active Video Cropping Configuration for Input Port B

Figure 1-615. VIP_PARSER_xtra4_port_b Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-533. VIP_PARSER_xtra4_port_b Register Field Descriptions

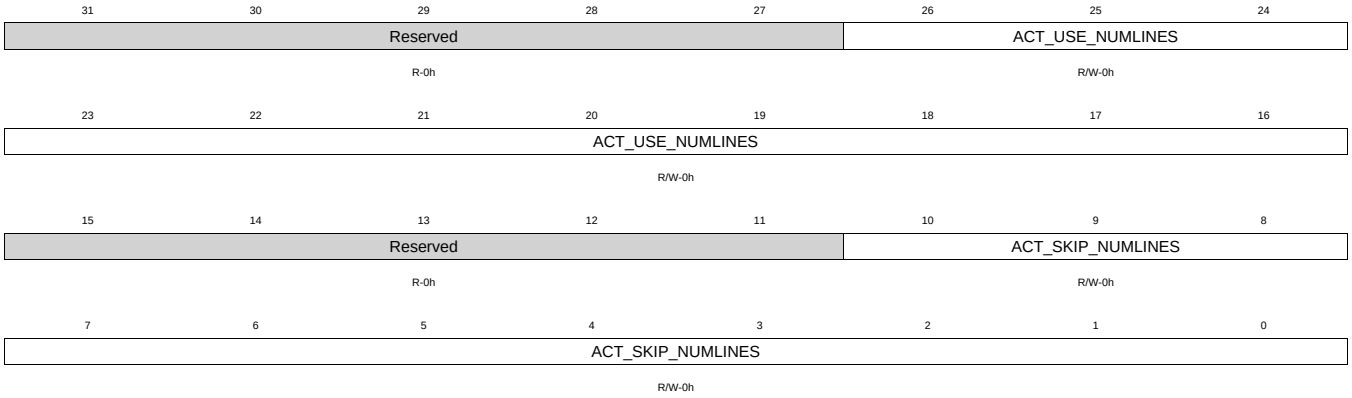
Bit	Field	Type	Reset	Description
31-28	ACT_TARGET_SRCNUM	R/W	0h	The cropping module can work on only one srcnum, specified in this field, for each dss_vip_parser output port (Active video).
27	Reserved	R	0h	
26-16	ACT_USE_NUMPIX	R/W	0h	When cropping, the number of pixels to keep after the skip_numpix value. skip_numpix + use_numpix must be smaller than the original line width.
15	ACT_BYPASS_N	R/W	0h	0 : Bypass cropping module 1 : Cropping module enabled
14-11	Reserved	R	0h	
10-0	ACT_SKIP_NUMPIX	R/W	0h	The number of pixels to crop from the beginning of each line.

1.3.14.54 VIP_PARSER_xtra5_port_b Register (offset = D4h) [reset = 0h]

VIP_PARSER_xtra5_port_b is shown in Figure 1-616 and described in Table 1-534.

Active Video Cropping Configuration for Input Port B

Figure 1-616. VIP_PARSER_xtra5_port_b Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-534. VIP_PARSER_xtra5_port_b Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	Reserved	R	0h	
26-16	ACT_USE_NUMLINES	R/W	0h	When cropping, the number of lines to keep after the skip_numlines value. Use_numlines + skip_numlines must be smaller than the total number of lines in the srcnum's active video region.
15-11	Reserved	R	0h	
10-0	ACT_SKIP_NUMLINES	R/W	0h	The number of lines to crop from the top of the vertical active video region.

1.3.14.55 VIP_PARSER_xtra6_port_a Register (offset = D8h) [reset = 0h]

VIP_PARSER_xtra6_port_a is shown in Figure 1-617 and described in Table 1-535.

Cfg Disable Active Srcnum Vector Input for Port A

Figure 1-617. VIP_PARSER_xtra6_port_a Register

31	30	29	28	27	26	25	24
yuv_srcnum_stop_immediately							
R/W-							

23	22	21	20	19	18	17	16
yuv_srcnum_stop_immediately							
R/W-							

15	14	13	12	11	10	9	8
anc_srcnum_stop_immediately							
R/W-							

7	6	5	4	3	2	1	0
anc_srcnum_stop_immediately							
R/W-							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 1-535. VIP_PARSER_xtra6_port_a Register Field Descriptions

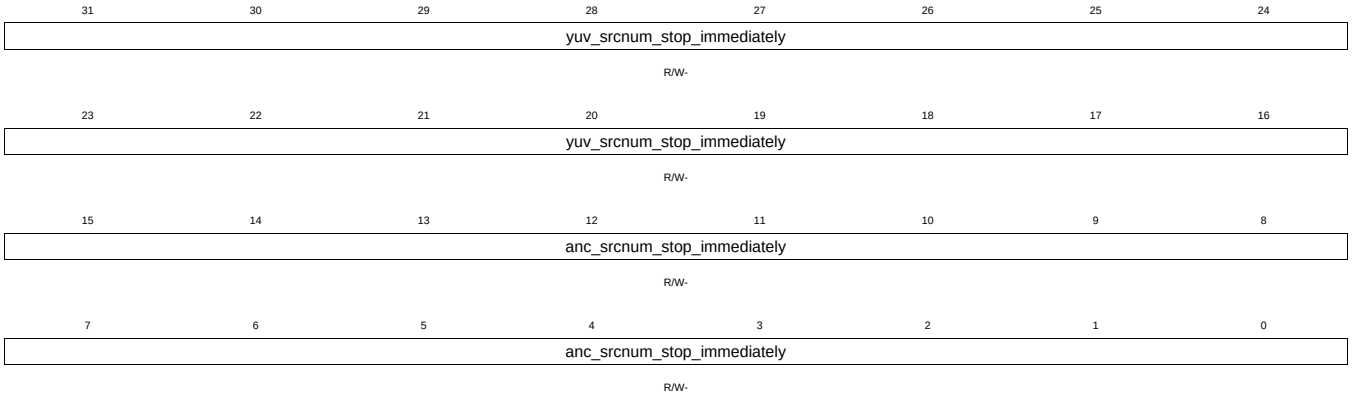
Bit	Field	Type	Reset	Description
31-16	yuv_srcnum_stop_immediately	R/W	0h	For the Active Video Port to the VPDMA, logic exists to ensure that a complete frame is sent out to the VPDMA following cfg_enable transitioning inactive for that port. Each bit in this vector represents a srcnum (remapped srcnum for TI line mux mode) going to the VPDMA. For example, bit 0 is srcnum 0, bit 1 is srcnum 1, etc. A 0 in a bit position means that the hardware will wait for that srcnum, if it is in the middle of a frame, to continue until the end of the frame before stopping. A 1 in a bit position means that it is ok for a srcnum to stop in the middle of a frame. For example, suppose a source is removed and the input will never complete sending a frame. If the bit position representing that srcnum is set to 0 , the port will never disable.
15-0	anc_srcnum_stop_immediately	R/W	0h	For the Ancillary Data Port to the VPDMA, logic exists to ensure that a complete frame is sent out to the VPDMA following cfg_enable transitioning inactive for that port. Each bit in this vector represents a srcnum (remapped srcnum for TI line mux mode) going to the VPDMA. For example, bit 0 is srcnum 0, bit 1 is srcnum 1, etc. A 0 in a bit position means that the hardware will wait for that srcnum, if it is in the middle of a frame, to continue until the end of the frame before stopping. A 1 in a bit position means that it is ok for a srcnum to stop in the middle of a frame. For example, suppose a source is removed and the input will never complete sending a frame. If the bit position representing that srcnum is set to 0 , the port will never disable.

1.3.14.56 VIP_PARSER_xtra7_port_b Register (offset = DCh) [reset = 0h]

VIP_PARSER_xtra7_port_b is shown in Figure 1-618 and described in Table 1-536.

Cfg Disable Active Srcnum Vector Input for Port B

Figure 1-618. VIP_PARSER_xtra7_port_b Register



LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 1-536. VIP_PARSER_xtra7_port_b Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	yuv_srcnum_stop_immediately	R/W	0h	For the Active Video Port to the VPDMA, logic exists to ensure that a complete frame is sent out to the VPDMA following cfg_enable transitioning inactive for that port. Each bit in this vector represents a srcnum (remapped srcnum for TI line mux mode) going to the VPDMA. For example, bit 0 is srcnum 0, bit 1 is srcnum 1, etc. A 0 in a bit position means that the hardware will wait for that srcnum, if it is in the middle of a frame, to continue until the end of the frame before stopping. A 1 in a bit position means that it is ok for a srcnum to stop in the middle of a frame. For example, suppose a source is removed and the input will never complete sending a frame. If the bit position representing that srcnum is set to 0 , the port will never disable.
15-0	anc_srcnum_stop_immediately	R/W	0h	For the Ancillary Data Port to the VPDMA, logic exists to ensure that a complete frame is sent out to the VPDMA following cfg_enable transitioning inactive for that port. Each bit in this vector represents a srcnum (remapped srcnum for TI line mux mode) going to the VPDMA. For example, bit 0 is srcnum 0, bit 1 is srcnum 1, etc. A 0 in a bit position means that the hardware will wait for that srcnum, if it is in the middle of a frame, to continue until the end of the frame before stopping. A 1 in a bit position means that it is ok for a srcnum to stop in the middle of a frame. For example, suppose a source is removed and the input will never complete sending a frame. If the bit position representing that srcnum is set to 0 , the port will never disable.

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