TMS320C242

DSP Controller

Silicon Errata

Silicon Revision 2.1

SPRZ178
October 2000

Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320C242 DSP Controller, silicon revision 2.1. The updates are applicable to:

- TMS320C242 (68-pin PLCC, FN suffix; 64-pin PQFP, PG suffix)

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature range and voltage range should not, in any way, be construed as a warranty of performance.

TMP Definition

TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

TMS Definition

Fully-qualified production device.

2 Silicon Revision 2.1 Known Design Marginality/Exceptions to Functional Specifications

Advisory	*Analog-to-Digital Converter (ADC)*

Revision(s) Affected: 2.1

Details: When the IM bit (bit 14) = 1 in ADCTRL2, the second conversion must be initiated before the first conversion is complete; otherwise, the ADC module may hang and fail to do further conversions.

Workaround: Initiate second ADC conversion before the first conversion is complete, or set this bit to zero.

CAUTION:

When the IM bit = 1, the ADCEOC bit is cleared *only* at the end of two conversions. i.e., ADCEOC is not cleared after a single conversion.

Revision(s) Affected: 2.1

Details: When the pseudo-ADC is enabled for the first time after a “power-on reset” (POR), a conversion is triggered (i.e., a conversion takes place even when no conversion has been initiated). Warm resets do not have this problem; only PORs have this problem.

Workaround: Perform a dummy conversion as part of the ADC initialization and flush the ADCFIFOs (after ensuring an EOC). After this, the ADC may be used as desired.

Advisory *SCI*

Revision(s) Affected: 2.1

Details: The TX_EMPTY bit (bit 6 in the SCICTL2 register) is supposed to get set when the transmit buffer and the shift register are ***both*** empty. However, this bit may occasionally be read as being set even when there is data in the transmit buffer.

Assuming two characters are being written back-to-back to the SCI, the TX_EMPTY bit is expected to go high after the second character is shifted out of the SCITXD pin. Occasionally, the TX_EMPTY bit goes high right after the first character is shifted out (i.e., when the second character is still in the transmit buffer). If the TX_EMPTY bit is polled to check the end-of-transmission of all characters, it may provide incorrect information about the status of the transmission.

Workaround: Follow these steps:

1. Read the TX_EMPTY bit.
2. If set, execute 2 NOPs and proceed to Step 3. Else, repeat Step 1.
3. Read the TX_EMPTY bit again.
4. If the bit is still set, then there are no more characters to be transmitted. If the bit is not set, it indicates transmission is not complete. Proceed to Step 1.

Advisory *WDFLAG bit (in WDCR Register)*

Revision(s) Affected: 2.1

Details: The power-on reset (POR) state of the WDFLAG bit is undefined. This could cause confusion if the user code attempts to differentiate a watchdog-initiated reset from a power-on reset.

Workaround: If an application implements a mechanism to differentiate a POR from other types of reset, the WDFLAG bit must be cleared after a POR. Once this is done, the WDFLAG bit can be set only by a watchdog reset.

Advisory *QEP Circuit*

Revision(s) Affected: 2.1

Details: After a DSP reset, the QEP module misses the first edge that occurs, but operates normally afterwards. This behavior manifests itself only with the first QEP edge after a reset and does not affect the QEP operation in any other way. This phenomenon also forces GP timer 2 to miss the first external clock pulse when enabled after reset.

Workaround: None

Advisory — *ILLADR Bit*

Revision(s) Affected: 2.1

Details: The ILLADR bit in the SCSR1 register may be set even though no illegal address access took place.

Workaround: This is a problem with the debugger-hardware interaction. This bit may be set on an emulation suspend such as a breakpoint or while single stepping. However, this bit works correctly in run time (i.e., this bit works correctly when the program is free-run without the JTAG connector being connected). This can be easily verified by writing a test code (running out of Flash) that copies the status of this bit to the XF bit and then monitoring the status of the XF pin using an oscilloscope.

Advisory — *PDPINT Pin Operation*

Revision(s) Affected: 2.1

Details: If the PDPINT pin is active during a device reset, it prevents the recognition of valid PDPINT interrupts in the future.

Workaround: To overcome this problem, bit PIRQR0.0 (for PDPINTA) and bit PIRQR2.0 (for PDPINTB) need to be cleared to zero. This can be achieved by writing a zero to these bits or by writing a one to the corresponding PIACKRn.0 bits. In addition to this, the EVAIFRA.0 bit (or EVBIFRA.0 bit) should be cleared as appropriate.

The PIRQRn and PIACKRn registers are ***not*** intended to be used in user applications. The workaround mentioned herein is a special case during the initialization of the device. After initialization, these registers should not be used by the user code.

3 Programming Considerations for the 24x ADC

3.1 Checking for End-of-Sequence

After a start-of-conversion (SOC) is initiated, two NOPs need to be executed before polling the ADCEOC bit. The EOC bit does not get set until 2 cycles after the write to the ADCTRL1 register (i.e., 2 cycles are needed before the correct EOC value is read). This timing is independent of the ADC clock prescale value. This (inserting 2 NOPs) does not apply if the ADCINTFLAG is polled instead. To reiterate, the NOPs are required only when polling the ADCEOC bit; interrupt-driven conversions do not have this requirement.

4 Data Sheet Updates

Advisory	*Illegal Addresses in the Data-Memory Space*

Details: Addresses 7040h–704Fh and 7100h–73FFh in the data memory are illegal and will assert an NMI if accessed. They have been incorrectly referred to as “Reserved” addresses in the *TMS320C242 DSP Controller* data sheet (literature number SPRS063C).

Workaround: These addresses will be corrected in the next revision of the data sheet (SPRS063D).

Advisory	*Bit Locations of the PIRQR0/1 and PIACKR0/1 Registers*

Details: The bit locations of the PIRQR0/1 and PIACKR0/1 registers of the TMS320C242 have been depicted incorrectly in SPRS063C. In SPRU276C, common tables have been used to depict these registers for F243/F241 and C242 DSPs. However, the bit locations of the PIRQR0/1 and PIACKR0/1 registers of the C242 are different when compared to the F243/F241 DSPs. The correct bit locations of these registers in the C242 and are outlined in Table 1. As stated in SPRU276C, the PIRQR0/1 and PIACKR0/1 registers are generally used for test purposes only and are not for user applications.

Workaround: The bit locations of the PIRQR0/1 and PIACKR0/1 registers will be corrected in the next revision of the data sheet (SPRS063D).

Table 1. PIRQR0/1 and PIACKR0/1 Registers Comparison Table

Interrupt Name (F243/F241)	Overall Priority	Bit Position in PIRQRn and PIACKRn	Interrupt Name (C242)
Reset	1		
Reserved	2		
NMI	3		
PDPINT	4	0.0	PDPINT
ADCINT	5	0.1	ADCINT
XINT1	6	0.2	XINT1
XINT2	7	0.3	XINT2
SPIINT	8	0.4	RXINT
RXINT	9	0.5	TXINT
TXINT	10	0.6	CMP1INT
CANMBINT	11	0.7	CMP2INT
CANERINT	12	0.8	CMP3INT
CMP1INT	13	0.9	TPINT1
CMP2INT	14	0.10	TCINT1
CMP3INT	15	0.11	TUFINT1
TPINT1	16	0.12	TOFINT1
TCINT1	17	0.13	TPINT2
TUFINT1	18	0.14	TCINT2
TOFINT1	19	0.15	TUFINT2
TPINT2	20	1.0	TOFINT2
TCINT2	21	1.1	CAPINT1
TUFINT2	22	1.2	CAPINT2
TOFINT2	23	1.3	CAPINT3
CAPINT1	24	1.4	RXINT
CAPINT2	25	1.5	TXINT
CAPINT3	26	1.6	ADCINT
SPIINT	27	1.7	XINT1
RXINT	28	1.8	XINT2
TXINT	29	1.9	Reserved
CANMBINT	30	1.10	Reserved
CANERINT	31	1.11	Reserved
ADCINT	32	1.12	Reserved
XINT1	33	1.13	Reserved
XINT2	34	1.14	Reserved
Reserved		1.15	Reserved
TRAP			
Phantom			

5 Errata for *TMS320C242 DSP Controller* Data Sheet (SPRS063D)

5.1 *10-Bit Dual Analog-to-Digital Converter (ADC)* Section, *Recommended Operating Conditions* Table (p. 61)

The MIN and MAX specifications for V_{AI} should be V_{REFLO} and V_{REFHI}, respectively, not V_{SSA} and V_{CCA}.

6 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com**

To access documentation on the web site:

1. Go to **http://www.ti.com**
2. Open the "**Products**" dialog box and select "**Digital Signal Processors**"
3. Scroll to the "**TMS320C2000™ Control Optimized Performance DSP Platform**" and click on **"TMS320C24X™ DSP Generation"**
4. Click on a device name and then click on the documentation type you prefer.

For further information, see the following documents:

- *TMS320F243/F241/C242 DSP Controllers Reference Guide: System and Peripherals,* literature number SPRU276
- *TMS320F/C24x DSP Controllers Reference Guide: CPU and Instruction Set,* literature number SPRU160
- *TMS320C242 DSP Controller* data sheet, literature number SPRS063

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