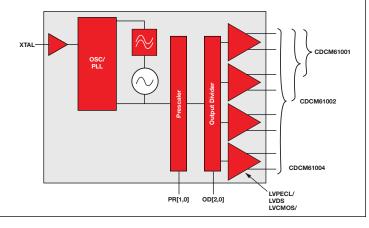
TI Clock Solutions for FPGAs



In many next-generation, high performance systems requiring FPGAs, the quality of the clock feeding these systems becomes very important. Many high-speed cores within FPGAs have stringent clocking requirements to allow for various data transmission standards. TI offers a full portfolio of clock generation devices which address this need by providing low-noise precision clocks (<1ps RMS, 10kHz – 20MHz) for these type of applications. In addition, TI also provides clock devices that can help simplify and centralize the clock tree surrounding your FPGA, with fractional-N PLL-based generators and a wide portfolio of high-performance clock distribution buffers.

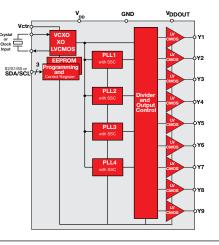
Clock Generation

CDCM6100x – Ultra-low jitter (500fs RMS typ, 10kHz – 20MHz) clock generation up to 683MHz. Provides 1, 2, or 4 outputs of LVPECL, LVDS or LVCMOS clocks with an easy-to-use pin-configurable interface. Integrated high performance VCO. Can be used to replace up to 4 low-jitter XOs in a single device. Available in a small footprint 5x5 QFN package.



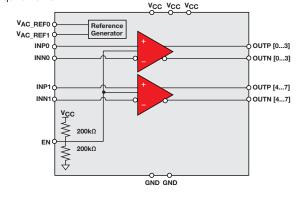
CDCE(L)9xx – Family of modular PLL-based programmable clock synthesizers. Generates up to 9 LVCMOS clocks from a single input frequency, either LVCMOS or XTAL input. Each output can be programmed for any clock frequency up to 230MHz, using up to four independent configurable fractional PLLs. Deep M/N divider ratio

allows for the generation of 0-ppm clocks. All PLLs support spreadspectrum clocking (SSC). Onboard EEPROM for easy customization of device over I²C interface. Small footprint TSSOP package help to reduce board space requirements.

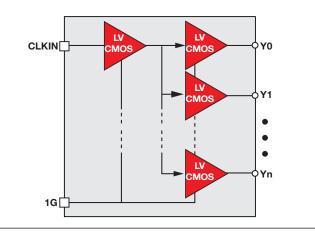


Clock Distribution

CDCLVD12xx/21xx – Family of industry's lowest additive jitter LVDS clock distribution buffers. Up to 16 low additive jitter (<300fs RMS typ, 10kHz – 20MHz), low skew clock outputs. Universal input support for LVPECL, LVDS or LVCMOS clocks. Signaling rate up to 800MHz. Small footprint QFN package help to reduce board space requirements.



CDCLVC11xx – Family of industry's lowest additive jitter LVCMOS clock distribution buffers. Up to 12 low additive jitter (<100fs RMS typ, 10kHz – 20MHz), low skew clock outputs. Signaling rate up to 250MHz. Small footprint TSSOP package help to reduce board space requirements.



Go to www.ti.com/clocks for datasheets, samples and EVMS

Clock Distribution

Device	Description	Input Level	Output Level	Frequency (MHz)	VCC (V)	Propagation Delay	Output Skew (max) (ps)	Char. Temp. (°C)	Package(s)
Fan-Out Cloci	k Buffers (Non-PLL)					-			
Differential-E	nded								
CDCLVP1102	Low-Jitter 1:2 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	10ps	-40 to 85	QFN-16
CDCLVP1204	Low-Jitter, 2-Input Selectable 1:4 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	15ps	-40 to 85	QFN-16
CDCLVP1208	Low-Jitter, 2-Input Selectable 1:8 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	20ps	-40 to 85	QFN-28
CDCLVP1212	Low-Jitter, 2-Input Selectable 1:12 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	550ps (max)	25ps	-40 to 85	QFN-40
CDCLVP1216	Low-Jitter, 2-Input Selectable 1:16 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	550ps (max)	30ps	-40 to 85	QFN-48
CDCLVP2102	Low-Jitter, Dual 1:2 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	10ps (within bank)	-40 to 85	QFN-16
CDCLVP2104	Low-Jitter, Dual 1:4 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	450ps (max)	15ps (within bank)	-40 to 85	QFN-28
CDCLVP2106	Low-Jitter, Dual 1:6 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	550ps (max)	20ps (within bank)	-40 to 85	QFN-40
CDCLVP2108	Low-Jitter, Dual 1:8 Universal-to-LVPECL Buffer	LVPECL/LVDS/LVCMOS	LVPECL	0 to 2GHz	2.5/3.3	550ps (max)	25ps (within bank)	-40 to 85	QFN-48
CDCLVD1204	Low-Jitter, 2-Input Selectable 1:4 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	-40 to 85	QFN-16
CDCLVD1208	Low-Jitter, 2-Input Selectable 1:8 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	-40 to 85	QFN-28
CDCLVD1212	Low-Jitter, 2-Input Selectable 1:12 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	-40 to 85	QFN-40
CDCLVD1216	Low-Jitter, 2-Input Selectable 1:16 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	-40 to 85	QFN-48
CDCLVD2102	Low-Jitter, Dual 1:2 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps (within bank)	-40 to 85	QFN-16
CDCLVD2104	Low-Jitter, Dual 1:4 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps (within bank)	-40 to 85	QFN-28
CDCLVD2106	Low-Jitter, Dual 1:6 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps (within bank)	-40 to 85	QFN-40
CDCLVD2108	Low-Jitter, Dual 1:8 Universal-to-LVDS Buffer	LVPECL/LVDS/LVCMOS	LVDS	0 to 800	2.5	1.5ns (typ)	20ps (within bank)	-40 to 85	QFN-48
CDCLVD1213	Low-Jitter, 1:4 Universal-to-LVDS Buffer with Selectable Output Divider	LVPECL/LVDS/CML	LVDS	0 to 800	2.5	1.5ns (typ)	20ps	-40 to 85	QFN-16
CDCLVP215	Dual 1:5 High-Speed LVPECL Clock Buffer	LVPECL	LVPECL	DC to 3.5GHz	2.5/3.3	230 to 370ps	30ps	-40 to 85	LQFP-32
Single-Ended	Ĺ								
CDCLVC1102	Low-Jitter, 1:2 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	-40 to 85	TSSOP-8
CDCLVC1103	Low-Jitter, 1:3 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	-40 to 85	TSSOP-8
CDCLVC1104	Low-Jitter, 1:4 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	-40 to 85	TSSOP-8
CDCLVC1106	Low-Jitter, 1:6 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	-40 to 85	TSSOP-14
CDCLVC1108	Low-Jitter, 1:8 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	-40 to 85	TSSOP-16
CDCLVC1110	Low-Jitter, 1:10 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2ns	50ps	-40 to 85	TSSOP-20
CDCLVC1112	Low-Jitter, 1:12 LVCMOS Fan-Out Clock Buffer	LVCMOS	LVCMOS	0 to 250	2.5/3.3	0.8 to 2 ns	50ps	-40 to 85	TSSOP-24

Clock Generation

Device	Description	Input Level	Output Level	Frequency (MHz)	VCC (V)	Jitter (Peak-to- Peak [P-P] or Cycle-to-Cycle [C-C])	Phase Error	Output Skew (max) (ps)	Char. Temp. (℃)	Package(s)
Crystal Oscill	ator (XO) Replacements - Single	e Ended								
CDCE(L)913	1.8V Programmable 1-PLL, 3 Output Clock Synthesizer with 2.5/3.3V or 1.8V Outputs	Crystal/LVCMOS	2.5/3.3V/1.8V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	-	150	-40 to 85	TSSOP-14
CDCE(L)925	1.8V Programmable 2-PLL, 5 Output Clock Synthesizer with 2.5/3.3V or 1.8V Outputs	Crystal/LVCMOS	2.5/3.3V/1.8V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	-	150	-40 to 85	TSSOP-16
CDCE(L)937	1.8V Programmable 3-PLL, 7 Output Clock Synthesizer with 2.5/3.3V or 1.8V Outputs	Crystal/LVCMOS	2.5/3.3V/1.8V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	-	150	-40 to 85	TSSOP-20
CDCE(L)949	1.8V Programmable 4-PLL, 9 Output Clock Synthesizer with 2.5/3.3V/ or 1.8V Outputs	Crystal/LVCMOS	2.5/3.3V/1.8V LVCMOS	0 to 230	1.8/3.3	60ps (typ)	-	150	-40 to 85	TSSOP-24
Mixed: Differential and Single-Ended										
CDCM61001	1:1 Low-Jitter, Integrated VCO Clock Generator	Crystal/LVCMOS	LVPECL/LVDS/2-LVCMOS	43.75 to 683.28; LVCMOS up to 250MHz	3.3	<1ps rms	-	—	-40 to 85	QFN-32
CDCM61002	1:2 Low-Jitter, Integrated VCO Clock Generator	Crystal/LVCMOS	LVPECL/LVDS/2-LVCMOS	43.75 to 683.28; LVCMOS up to 250MHz	3.3	<1ps rms	-	50	-40 to 85	QFN-32
CDCM61004	1:4 Low-Jitter, Integrated VCO Clock Generator	Crystal/LVCMOS	LVPECL/LVDS/2-LVCMOS	43.75 to 683.28; LVCMOS up to 250MHz	3.3	<1ps rms	-	60	-40 to 85	QFN-32
CDCE62002	2:2 Low-Jitter, Integrated VCO Clock Generator	Crystal/LVCMOS/ Differential	LVPECL/LVDS/2-LVCMOS	4.25 to 1175	3.3	<1ps rms	-	75	-40 to 85	QFN-32
CDCE62005	3:5 Low-Jitter, Integrated VCO Clock Generator	Crystal/LVCMOS/ Differential	LVPECL/LVDS/2-LVCMOS	4.25 to 1175	3.3	<1ps rms	-	75	–40 to 85	QFN-48

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