OMAP™

OMAP5432 Multimedia Device
Silicon Revision 2.0
Evaluation Module

Texas Instruments OMAP™ Family of Products

Reference Guide

Literature Number: SWCU130
May 2013

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Read This First

This manual should be used by software and hardware developers for evaluation of the OMAP5432 ES2.0 chipset. This document describes the OMAP5432 evaluation module (EVM) hardware. This document also gives the user information about the different interfaces on the OMAP5432 EVM. For specific support, please refer to TI recommended 3rd parties. Please note that not all hardware features are supported by the released software.

Related Documentation:

OMAP543x ES2.0 Technical Reference Manual

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History

The following table summarizes the revisions to the OMAP5432 EVM Reference Manual (SWCU130).

Version	Literature Number	Date	Notes
*	SWCU130	May 2013	See (1)

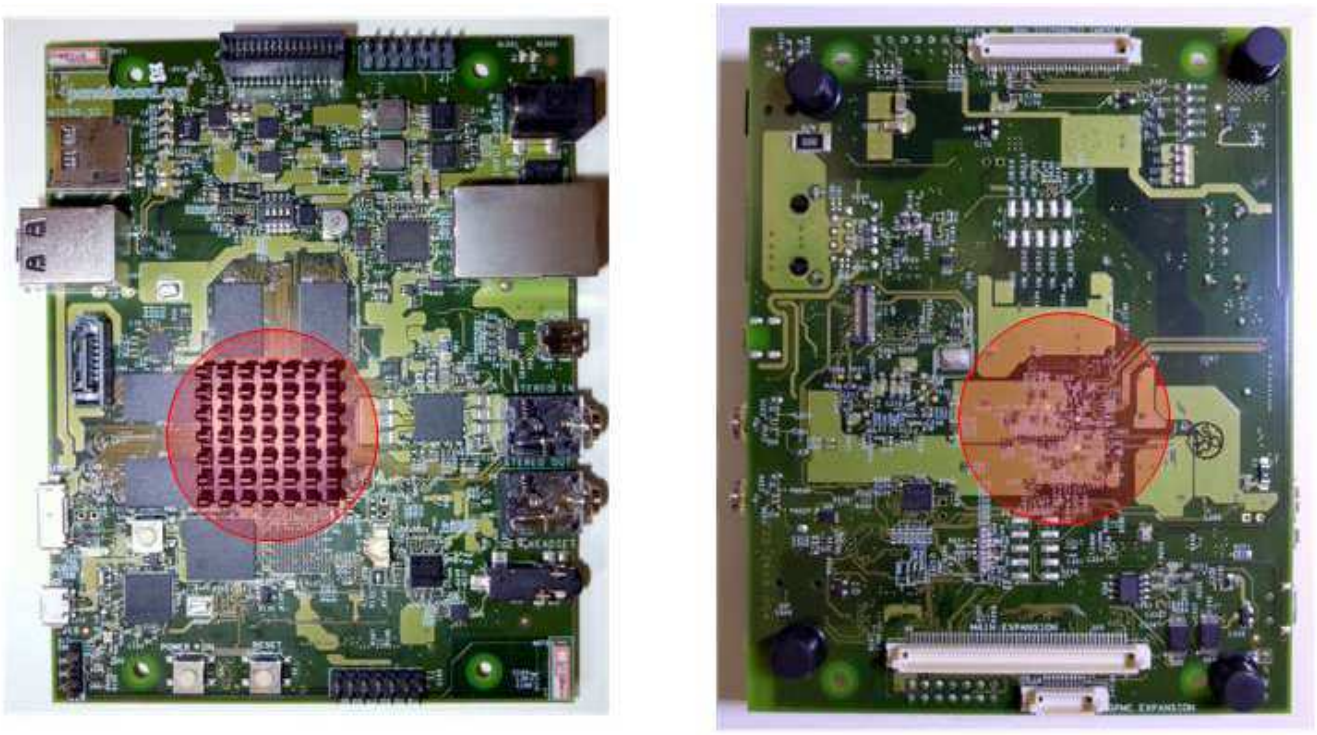
(1) *OMAP5432 Evaluation Module System Reference Module* (SWCU130) — Initial release.

OMAP5432 EVM System Reference Guide

This document is the System Reference Manual for the OMAP5432 EVM, a low cost OMAP5432 ES2.0 based board. This document provides detailed information on the overall design and usage of the OMAP5432 EVM from the System perspective.

CAUTION

The OMAP5432 EVM may reach elevated temperatures. Avoid handling the OMAP5432 EVM while power is applied, especially in areas shown in OMAP5432 High-Temperature Regions.



OMAP5432 High-Temperature Regions

1 OMAP5432 EVM Introduction

1.1 OMAP5432 EVM Overview

OMAP5432 EVM is an OMAP5432 ES2.0 platform designed to provide access to as many of the powerful features of the OMAP5432 Multimedia Processor as possible, while maintaining a low cost. This will allow the user to develop software to utilize the features of the powerful OMAP5432 processor. In addition, by providing expandability via onboard connectors, the OMAP5432 EVM supports development of additional capabilities/functionality. See Table 1 for a listing of the OMAP5432 EVM features.

Table 1. OMAP5432 EVM Features

Device or Module	Features or Description	
Processor	OMAP5432 ES2.0	
Onboard DDR3L	2GB (implemented using 4x Micron 4Gb DDR3L devices (MT41K256M16HA-125:E)	
Non-volative Memory	4GB EMMC/iNAND Ultra device (Sandisk P/N SDIN7DP2-4G)	
PMIC	TI (TWL6037 Power Management Companion IC)	
Debug Support	14-pin JTAG	GPIO Pins
	UART via micro-USB connector	LEDs
PCB	5.0” x 3.97” (127.00mm x 100.84 mm)	10 layers (8 Routing)
Indicators	2 blue LEDs (GPIO-controlled), 5 green LEDs (I2C-controlled), one tri-color RGB LED (I2C-controlled), Green Debug Power LED, Red Power Input Voltage Indicator	
HS USB 3.0 OTG Port	USB3.0 connector, supports optional plug-in of micro-USB connector	
HS USB Host Port	Three USB HS Ports, two to onboard connector, one provided via 0.1” pitch header	
Audio Connectors	3.5mm, Stereo out	3.5mm, Stereo In
	Headset Jack (earphone/microphone)	
SDIO Connector	4-bit Micro-SD card cage, push/push	
User Interface	1-User defined button	Reset Button
Video	HDMI via native OMAP HDMI interface	
	DSI Display Expansion (DSIPORTA and DSIPORTC) via 100-pin expansion connector	
	Parallel Display Expansion (DPI) via 100-pin expansion connector	
Power Connector	DC Power	
Camera	Single MIPI CSI-2 camera and/or parallel camera/dual MIPI CSI- 2 sensors supported via camera expansion connectors	
Expansion Connector(s)	For information, see Generic, Main, Camera, and GPMC Expansion sections of this document	

1.2 Overview of the OMAP5432 EVM Kit Contents

The OMAP5432 EVM kit contains the following items:

- 1 OMAP5432 EVM
- Board packing material
- 1 Shipping Box

The following items can be used with the OMAP5432 EVM, but are NOT included in the kit:

- USB Cable (micro-AB to Type A)
- HDMI Cable (Type D)
- DC wall supply (+5Vdc up to +15Vdc)

External Power Supply

The use of an external power supply is required to power this EVM. Selection should always take into consideration a power supply that provides a suitable level of protective electrical safety isolation and is certified as appropriate, to local product regulatory compliance requirements.

2 OMAP5432 EVM Architecture

This chapter explains the architecture of the OMAP5432 EVM.

2.1 Overview of the OMAP5432 EVM Architecture

The OMAP5432 EVM uses the following major components:

- M OMAP5432 ES2.0 Processor
- M TWL6037 Power Management Companion Device
- M TWL6040 Audio Companion Device
- M DDR3L Memory
- M HDMI Connector (Type D) – for OMAP5432 HDMI Transmitter output
- M Audio Input & Output Connectors (3.5mm)
- M Micro-SD Card Cage (push-push)
- M UART via micro-AB USBOTG Connector
- M WL1857 Module – 802.11b/g/n, Bluetooth, NFC

The Platform also includes connectors that can be used for additional functionality and/or expansion purposes. They are indicated by the blue blocks in Figure 1, and include: .

- M Single CSI-2 Camera Connector (J2)
- M Dual CSI-2/Parallel Camera Connector (J18)
- M Main Expansion Connector (J20)
- M GPMC Expansion Connector (J21)
- M Generic Expansion Connector (J17)
- M Power Measurement (J19)

The core components of the OMAP5432 EVM will be discussed in this section of the document. This would include the OMAP5432 ES2.0 Processor and its external DDR3L memory, the input clock circuitry, the TWL6037 Power Companion IC, and the TWL6040 Audio Companion IC. The functional interfaces will be discussed in later sections of the document.

Figure 1 is the architectural block diagram of the OMAP5432 EVM.

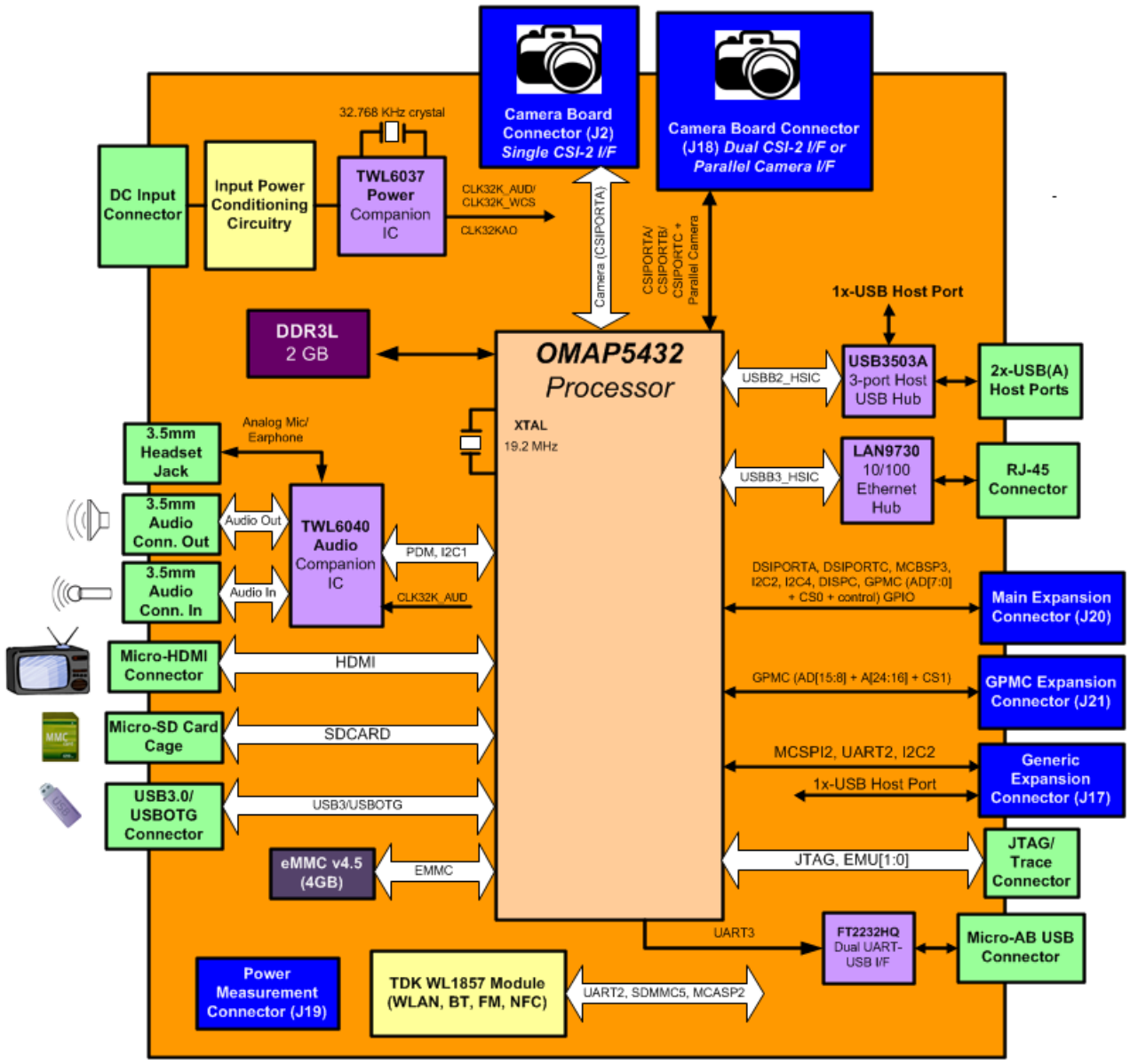


Figure 1. OMAP5432 EVM Architectural Block Diagram

Figure 2 shows the OMAP5432 EVM top view, and Figure 3 shows the bottom view.

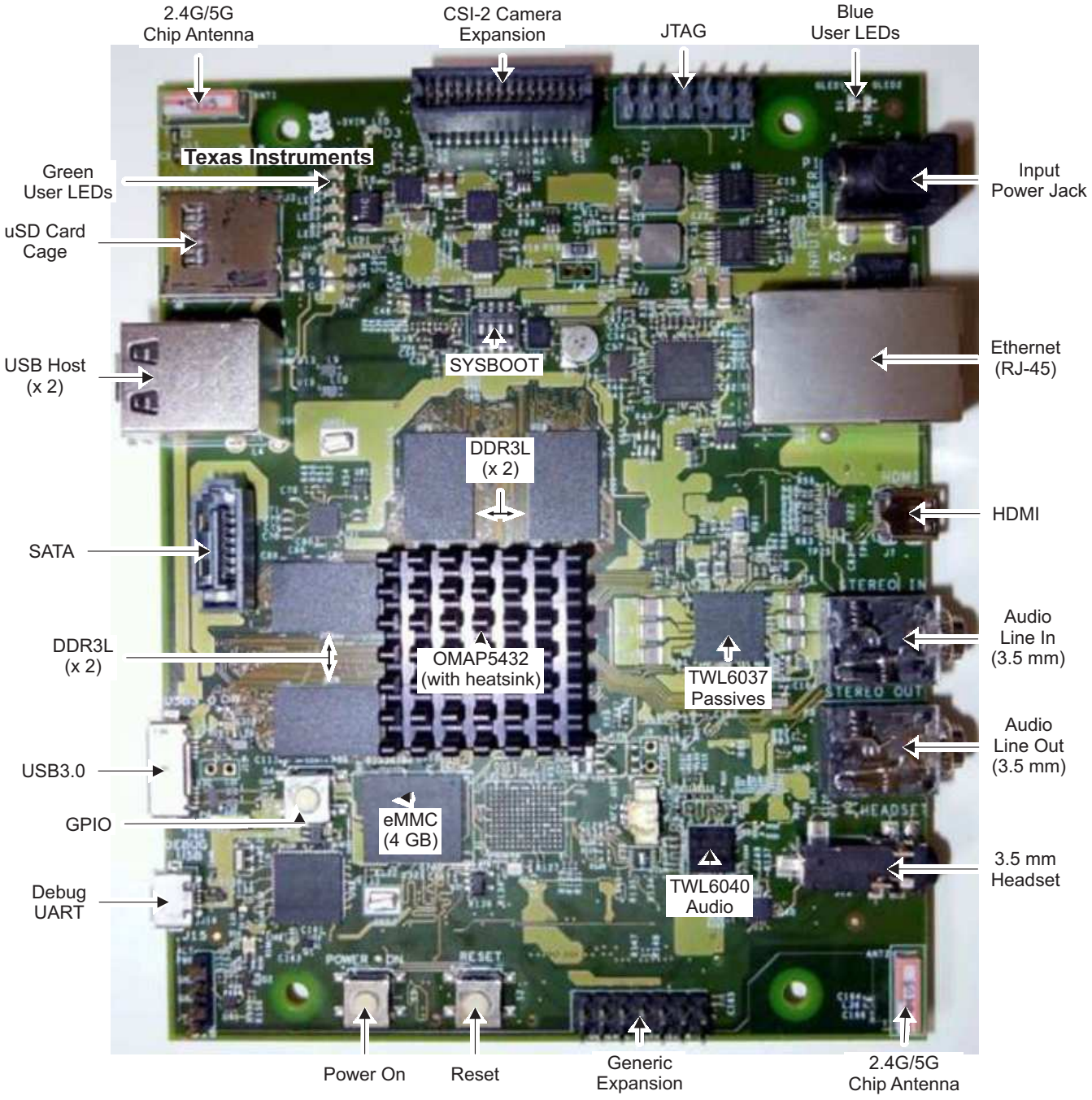


Figure 2. OMAP5432 EVM (Top View)

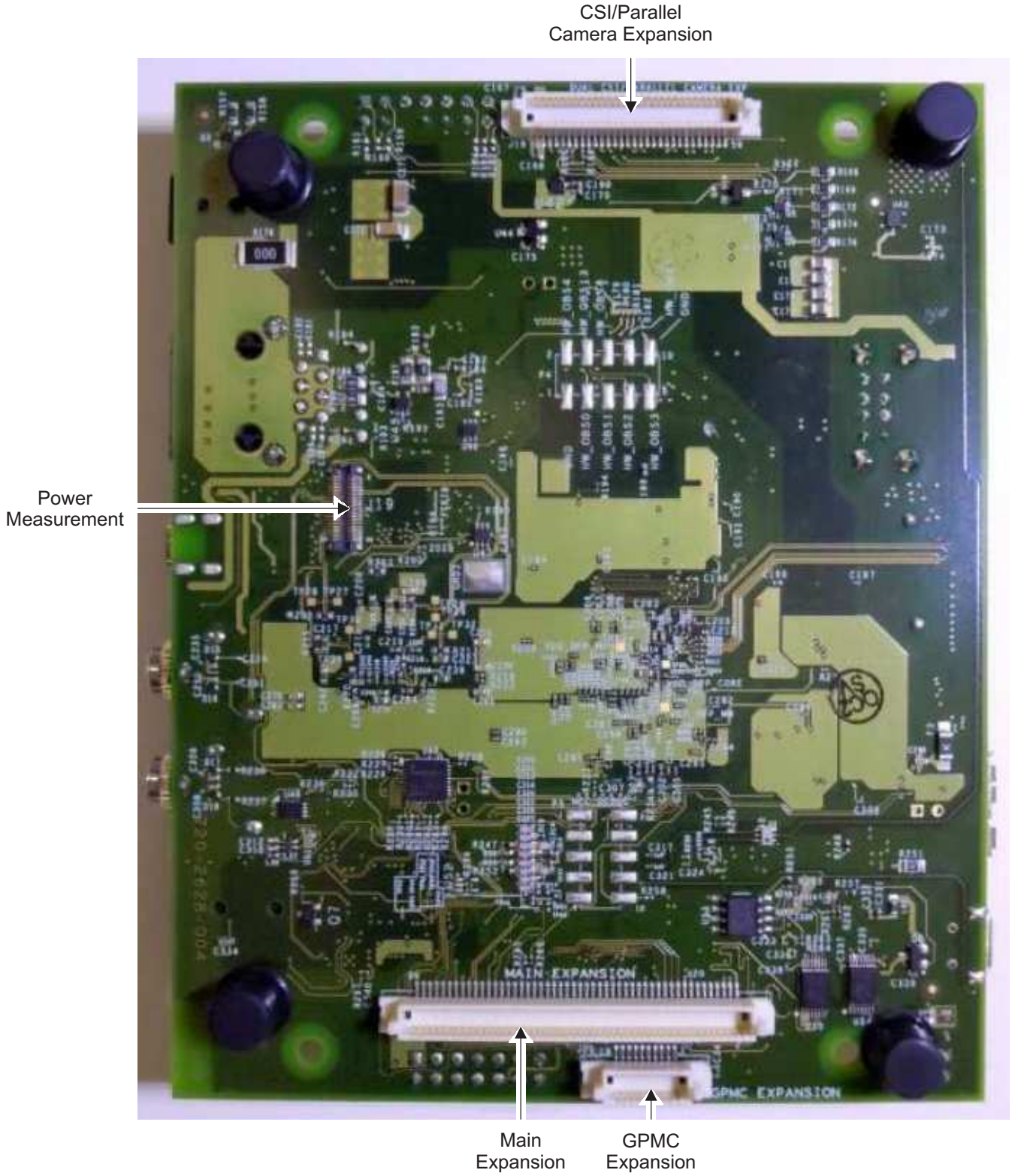


Figure 3. OMAP5432 EVM (Bottom View)

2.2 System Clock Distribution

The OMAP5432 EVM implements a 19.2 MHz crystal that directly drives the FREF_XTAL_IN ball (L32) and FREF_XTAL_OUT ball (M32) of the OMAP5432 ES2.0 processor. This clock is used as an input to the PLLs within the OMAP5432 ES2.0 processor so that it can generate all the internal clock frequencies required for system operation. The OMAP5432 generates a square wave clock output on the FREF_XTAL_CLK output (ball L33), which is used as an input to the TWL6040 Audio Companion IC. Additionally, there are two clock outputs that are programmable by system software (FREF_CLK0_OUT/ball M31 and FREF_CLK1_OUT/ball P31).

2.3 OMAP5432 ES2.0 Processor

The heart of OMAP5432 EVM is the OMAP5432 ES2.0 processor. The OMAP5432 high-performance multimedia application device is based on enhanced OMAP™ architecture and uses 28-nm technology. The architecture is designed to provide best-in-class CPU performance, video, image, and graphics processing.

The device supports high-level operating systems (OS) such as:

- Android™
- Linux® and others.

The device is composed of the following subsystems:

- Cortex™-A15 microprocessor unit (MPU) subsystem, including two ARM® Cortex-A15 cores
- Digital signal processor (DSP) subsystem
- Image and video accelerator high-definition (IVA-HD) subsystem
- Cortex-M4 image processing unit (IPU) subsystem, including two ARM Cortex-M4 microprocessors
- Display subsystem
- Audio back-end (ABE) subsystem
- Imaging subsystem (ISS), consisting of image signal processor (ISP) and still image coprocessor (SIMCOP) block
- 3D-graphics accelerator subsystem, including POWERVR™ SGX544 dual-core Debug subsystem

The device includes state-of-the-art power management techniques required for high-performance mobile products. Comprehensive power management is integrated into the device. The device also integrates:

- On-chip memory
- External memory interfaces
- Memory management
- Level 3 (L3) and level 4 (L4) interconnects
- System and connecting peripherals

2.4 TWL6037 Power Companion IC

The TWL6037 power companion IC is packaged in a 9.15mm x 9.15 mm, 108-pin QFN package that provides many functions used on the Platform. The QFN package has two rows of pads with 0.55mm pitch and 0.5mm pitch, with the package diagram shown in Figure 4. The feature list of the major functions/interfaces provided by the TWL6037 device that are utilized on the OMAP5432 EVM ES2.0 platform are listed below.

- A power management system (FSM)
- 1 HS-I2C interface (≤ 2.4Mbits/s) for all IC GP control commands (CTL-I2C)
- 1 HS-I2C interface (≤ 2.4Mbits/s) for all Smart-Reflex Class 3 control commands (SR-I2C)
- A 32kHz RC oscillator for a fast device start-up
- A high-performance crystal oscillator, for 32.768kHz external crystal
- A Real Time Clock (RTC) resource
- Power supply resources:
  - 11 Low Drop Out (LDO) regulators

  - 7 configurable step down converters
  - 1 boost converter (for generating VBUS when OTG interface is in host mode)
- 3 general-purpose enables for possible platform upgrades (REGEN1, SYSEN1, SYSEN2)

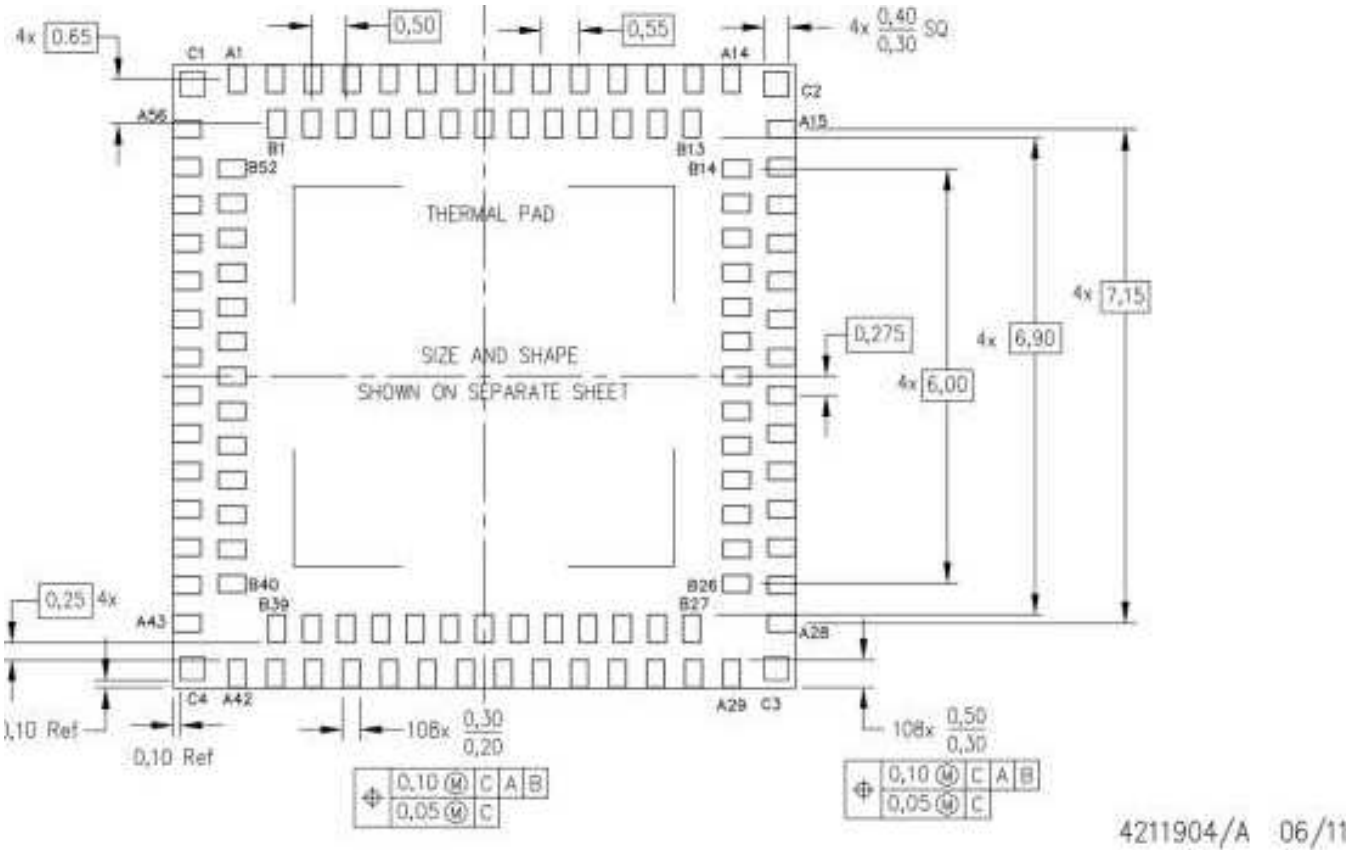


Figure 4. TWL6037 Power Companion IC Package Diagram (Bottom View)

2.4.1 TWL6037 VDD_OPP_MPU (SMPS1/2/3) Outputs

The OMAP5432 EVM board implements a triple-phase SMPS to provide the MPU voltage to the OMAP5432 ES2.0 device. This configuration connects the SMPS1, SMPS2 and SMPS3 step-down converters of the TWL6037 in parallel to provide up to 9A of current to the VDD_OPP_MPU supply pins on the OMAP5432 ES2.0 device. The default voltage of all of these supplies is 1.05V, and each should be adjusted as required by S/W for the desired processor OPP. A current measurement resistor (R213) is included on the input of this SMPS.

2.4.2 TWL6037 VDD_OPP_MM (SMPS4/5) Outputs

The OMAP5432 EVM board implements a dual-phase SMPS to provide the MM (multi-media) voltage to the OMAP5432 ES2.0 device. This configuration connects the SMPS4, and SMPS5 step-down converters of the TWL6037 in parallel to provide up to 4A of current to the VDD_OPP_MM supply pins on the OMAP5432 ES2.0 device. The default voltage of all of these supplies is 1.05V, and each should be adjusted as required by S/W for the desired processor OPP. A current measurement resistor (R211) is included on the input of this SMPS.

2.4.3 TWL6037 VDD_DDR3L (SMPS6) Output

The TWL6037 SMPS6 step down converter provides the 1.35V required for the OMAP5432 ES2.0 DDR3 power pins, as well as the supply pins on the DDR3L devices. With the TWL6037 BOOT0 line tied to a logic '0', this supply will output 1.35V, and with BOOT0 tied to a logic '1', the supply will output 1.5V. This allows the usage of either DDR3L devices or standard DDR3 parts. This supply is capable of providing up to 3A of current. A current measurement resistor (R61) is included on the output of this SMPS.

2.4.4 TWL6037 VDDS_1V8_MAIN (SMPS7) Output

The TWL6037 SMPS7 step down converter provides the 1.8V used as the main I/O voltage for the OMAP5432 EVM platform. It drives the VDDS_1V8 balls on the OMAP5432 ES2.0 device, as well as many other onboard pins requiring a 1.8V logic supply. This SMPS is capable of providing up to 2A of current.

2.4.5 TWL6037 VDD_OPP_CORE (SMPS8) Output

The OMAP5432 EVM board implements a SMPS to provide the core voltage to the OMAP5432 ES2.0 device. This configuration utilizes the SMPS8 step-down converter of the TWL6037 to provide up to 1A of current to the VDD_OPP_CORE supply pins on the OMAP5432 ES2.0 device. The default voltage of this supply is 1.05V, and should be adjusted as required by S/W for the desired processor OPP.

2.4.6 TWL6037 VDDA_2V1_AUD (SMPS9) Output

The TWL6037 SMPS9 step down converter is used solely to provide the 2.1V pre-regulated supply used by the TWL6040 audio companion IC to generate its own power outputs. This SMPS is capable of providing up to 1A of current.

2.4.7 TWL6037 Boost Converter (SMPS10) Output

The TWL6037 contains a boost converter that provides two outputs which are both +5Vdc outputs. The first output (SMPS10_OUT1) is capable of providing 500mA of current, and serves as the USB charge pump when the OMAP USBOTG port is operating a USB host. The second +5V output (SMPS10_OUT2) is capable of providing 100mA of current and is used as the input voltage to the internal 3.3V USB LDO.

2.4.8 TWL6037 LDO Power Resources

The TWL6037 power companion IC also provides 11 LDOs that are available for external use on the OMAP5432 EVM board. These LDOs are discussed in the following paragraphs.

The LDO1_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 200mA of current, and drives net VDDAPHY_CAM, which is connected to the VDDA_CSIPORTA, VDDA_CSIPORTB, and VDDA_CSIPORTC input pins (balls N3, AA7, and J5, respectively) on the OMAP5432 ES2.0 processor.

The LDO2_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 300mA of current, and drives net VCC_2V8_DISP, which is a 2.8V rail which is connected only to expansion connectors J15 and J16.

The LDO3_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 200mA of current, and drives net VDDAPHY_MDM, which is only connected to the VDDA_LLI_1 input pin (ball AJ17) on the OMAP5432 ES2.0 processor.

The LDO4_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 200mA of current, and drives net VDDAPHY_DISP, which is connected to the VDDA_DSIPORTA, VDDA_DSIPORTC, and VDDA_HDMI input pins (balls AA33, AE33, and AN25, respectively) on the OMAP5432 ES2.0 processor.

The LDO5_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 200mA of current, and drives net VDDA_1V8_PHY, which is a 1.8V rail that sources the following OMAP5432 balls:

- VDDS_USBHS18 (ball AE18)
- VDDA_USBSS18 (ball AE19)

- VDDA_SATA (ball E9)
- VDDA_DPLL_UNIPORT_LLI (ball AF17)
- VDDA_DPLL_HDMI (ball AF24)
- VDDA_DPLL_UNIPORT_CSI (ball H14)

The LDO6_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 200mA of current, and drives net VDDS_1V2_MAIN, which is only connected to the OMAP5 wakeup power pin (VDDA_LDO_EMU_WKUP, ball N25) and VDDS_HSIC ball (N26) on the OMAP5432 ES2.0 processor. For OMAP5432 EVM implementation, this rail will be enabled at powerup and set to 1.2V, and should not be changed.

The LDO7_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 200mA of current, and drives net VDD_VPP, which is only connected to the E-Fuse programming voltage input pin (VPP1, ball AD9) on the OMAP5432 ES2.0 processor.

The LDO8_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 200mA of current, and drives net VDD_3v0, which is currently not used on the OMAP5432 EVM board.

The LDO9_OUT supply is a programmable LDO that can be adjusted from 0.9V to 3.3V in 50mV steps. It can provide up to 50mA of current, and drives net VCC_DV_SDIO, which is connected to the VDDS_SDCARD input pin (ball E5) on the OMAP5432 ES2.0 processor.

The USB_OUT LDO is a fixed 3.3V, 35mA LDO that provides voltage to the OMAP5432 ES2.0 that it uses for its internal USB transceiver (net VDDA_3V_USB). The only ball powered by this LDO is the VDDA_USBHS33 ball (ball AN21).

The VRTC LDO is internal LDO that is brought out to pin B48 on the TWL6037 Power IC for decoupling. It's only connection on the OMAP5432 EVM PCB is for pull-ups tied to the TWL6037 BOOT[1:0] pins.

The VANA LDO is internal LDO that is brought out to pin A49 on the TWL6037 Power IC for decoupling. It has no other connection on the PCB.

2.4.9 TWL6037 Clock Circuitry

The TWL6037 has a 32.768 KHz crystal connected across its OSC32KIN and OSC32KOUT balls. This crystal is used by the TWL6037 to generate two output 32.768 KHz, 1.8V square wave clock outputs.

These outputs are:

- CLK32KGAO: always on clock connected to the SYS32K input of the OMAP5432 ES2.0 processor.
- GPIO_5: This clock is buffered and driven to the CLK32K input of the TWL6040 Audio Companion IC. This clock will be off by default at reset, and must be configured and enabled by software via I2C.

2.5 TWL6040 Audio Companion IC

The TWL6040 device is a small (6 x 6 mm, 0.5mm pitch) 120 ball PBGA that provides many functions, primarily audio, used on the Platform. Shown below is a feature list of the major functions/interfaces provided by the TWL6040 device.

- A audio management system
  - PDM Interface for Audio and control
  - Analog Microphone Interface
  - Headset – speaker (32 ohm) and microphone
  - Earpiece Output
  - Aux Output
  - Hands-free 8 ohm driver
  - Dual Vibrator
- Misc Control
  - GPO
  - Power on/off

- Power
  - Internal LDOs
  - Internal negative charge pump

2.6 SYSBOOT Configuration

The OMAP5432 ES2.0 Processor has five SYSBOOT inputs. These inputs are sampled after a board reset, and determine the booting and operating mode of the OMAP5432 Processor. The upper input (h_SYSBOOT_4) controls the clocking modes of the part, and is currently set to '0' through a 10Kresistor to ground and should not be changed.

The lower four inputs, h_SYSBOOT_[3:0] determine the type and order of memory or peripheral booting. h_SYSBOOT_3 determines whether memory or peripheral booting is preferred ('0' -> Peripheral, 1-> Memory). The SYSBOOT definitions may be found in the OMAP5430 TRM, but are included here for convenience. See Table 2 for the SYSBOOT definitions for the OMAP5432 EVM board.

Note that the SYSBOOT_0 switch is aligned with the '1' position on the slide switch, and that setting a switch to the "ON" position will set the corresponding SYSBOOT input high into OMAP.

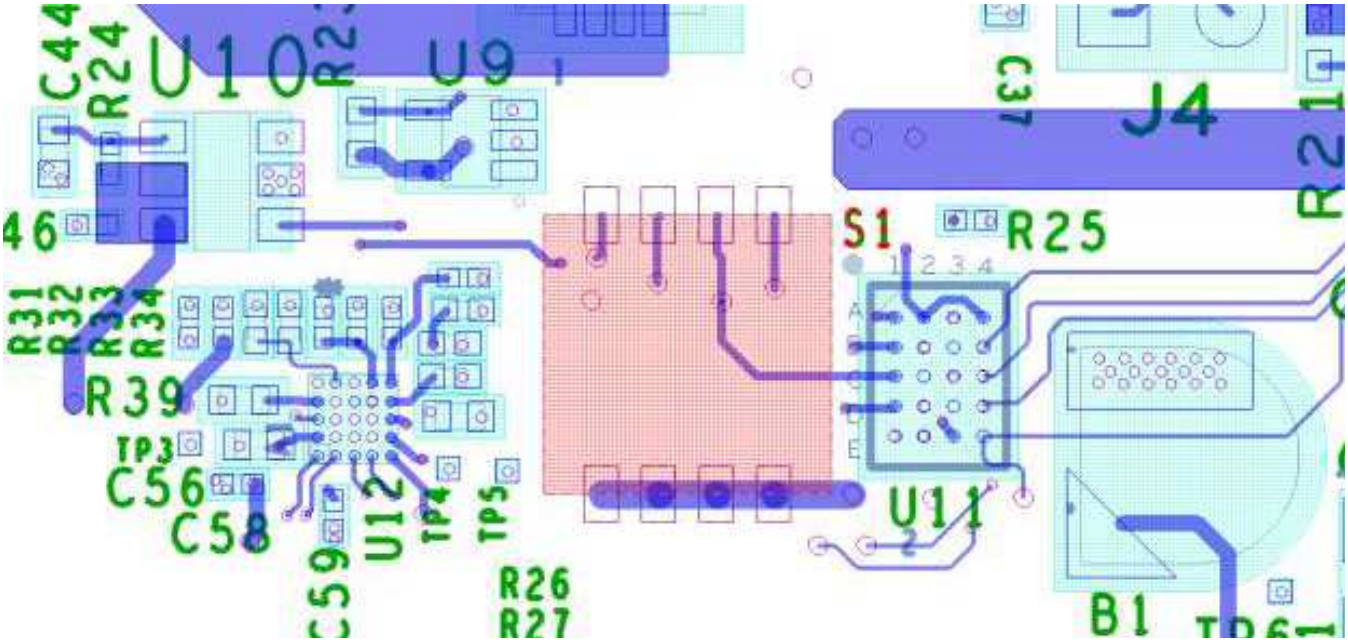


Figure 5. SYSBOOT Switch Location

Table 2. SYSBOOT[3:0] Definitions

SYSBOOT[3:0]	Booting Devices Order		
	1st	2nd	3rd
0000	USB	eMMC	N/A
0001	USB	NAND	N/A
0010	USB	SD	eMMC
0011	USB	SATA	SD
0100	USB	UART	XIP
0101	UART	OneNAND	N/A
0110	Reserved		
0111	Fast XIP (wait monitoring OFF)	UART	USB
1000	eMMC	USB	N/A
1001	NAND	USB	N/A

Table 2. SYSBOOT[3:0] Definitions (continued)

SYSBOOT[3:0]	Booting Devices Order		
	1st	2nd	3rd
1010	SD	eMMC	USB
1011	SATA	SD	USB
1100	XIP	USB	UART
1101	OneNAND	UART	N/A
1110	Reserved		
1111	Fast XIP (wait monitoring OFF)	UART	USB

2.7 Input Power Circuitry

The input power circuitry may be found on sheet 10 of the board schematic. This circuitry provides the main 3.7V and 3.3V operating voltages for the board (VSYS_BRD and VCC_3V3_MAIN, respectively). It also provides a load switch or SMPS that provides the 5V supply for the board that powers the host ports. A block diagram of this circuitry is shown in Figure 6 on the next page. The OMAP5432 EVM can be run with a DC wall supply ranging from +5Vdc to +15Vdc plugged into the input power jack at P1.

The block labeled “Input Voltage Detect/Power Enable Logic” in Figure 5 contains a supervisor IC and a comparator. This logic may be found on sheet 16 of the board schematic. The supervisor keeps both load switches (U4 and U8) disabled until the input supply has reached its valid operating voltage. The comparator is used to compare the divided down input to the internal reference of the comparator. If the input voltage from the jack is below approximately 5.60V, load switch U4 is enabled (driving the main 5V power rail DC_5V with the jack input), and if it is > 5.60V then load switch U18 is enabled (driving the main 5V power rail DC_5V with the SMPS 5V output). The enables to the load switches are complementary, so that only one may be enabled at a time (the exception to this is during the initial board power sequence, when both enables are high, which disables both load switches). The TPS54426 SMPS buck-converter at U8 is capable of providing up to 4A of output current @ 5V.

The board also provides a second TPS54426 SMPS buck-converter at U3 which is used to provide the main 3.3V supply for the board (VCC_3V3_MAIN). This rail is enabled by SYSEN1 from the TWL6037 Power Companion IC.

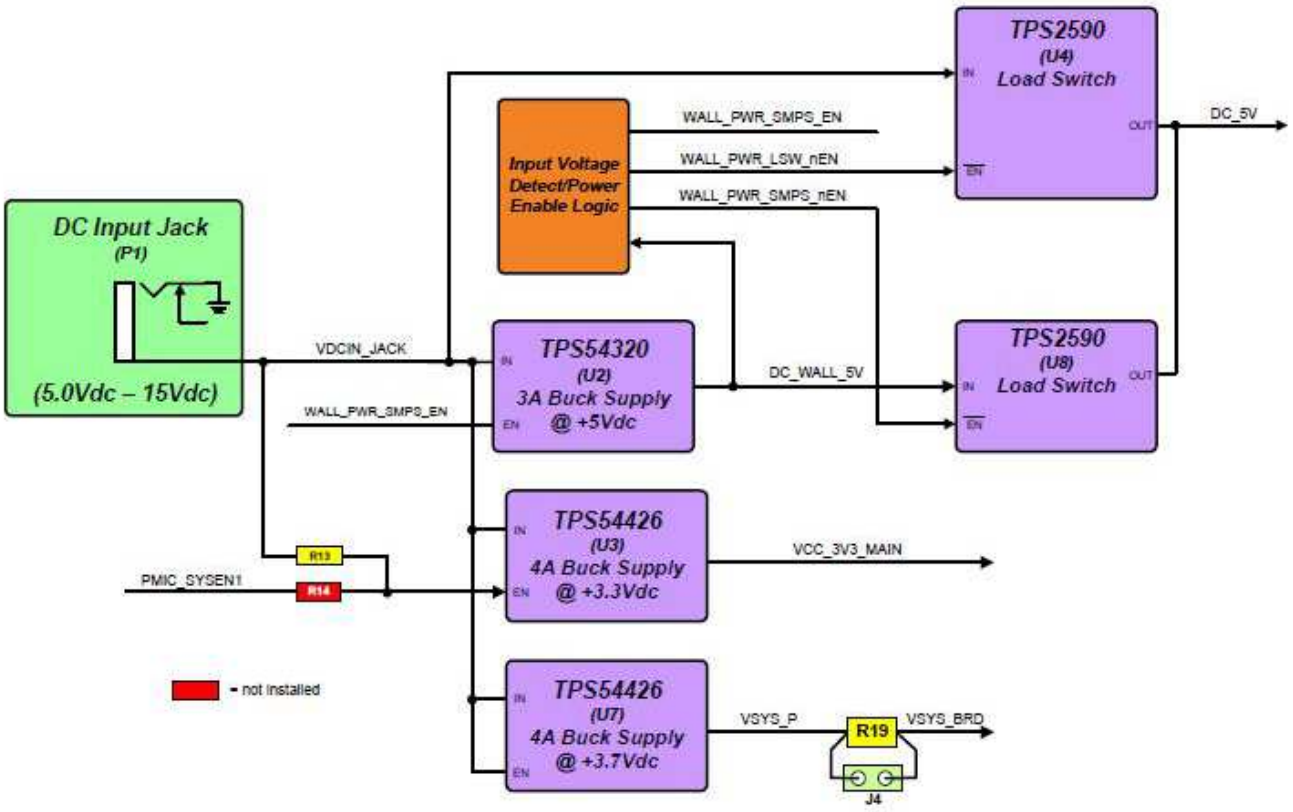


Figure 6. Input Power Circuitry Block Diagram

2.8 Standard Volatile Memory

The OMAP5432 ES2.0 processor supports two DDR3 channels, accessible only via external memory devices. Each channel supports two chip-selects, so eight memory devices are provisioned on the PCB. The memory device used is Micron P/N MT41K256M16HA-125IT:E. This device is a 4Gb device, so up to 32Gb (4GB) of DDR3 can be supported. However, the current PCB only has the devices on CS0 populated for each channel, so the total amount of DDR3 provided is 16Gb (2GB).

The Micron DDR3 memory used is DDR3L (1.35V supply voltage). Regular DDR3 memory (1.5V supply voltage) could be utilized, but the voltage divider for the feedback into the supply SMPS @ U12 would need to be changed to provide 1.5V instead of 1.35V.

2.9 Debug UART Interface

The OMAP5432 EVM provides a dual-port USART device (FTDI part number FT2232HQ). This provides up to two UART terminal interfaces out via a single USBOTG micro-AB connector located at J14. Driver software to utilize this device must be downloaded from the FTDI website. The first (lowest numbered) port of this device is connected to UART3 from the OMAP5432 ES2.0 processor, while the second port is unused. There are voltage translators provided to convert the 1.8V logic level UART signals to/from OMAP5432 ES2.0 to the 3.3V signals required by the USART.

When a micro-AB cable is plugged into J14, the VBUS from the host provides input voltage to the 3.3V LDO at U34 that powers the USART chip. Teraterm or another terminal emulation program should be used to connect to the first of the two USB serial ports found. To use this UART interface, the serial port settings should be applied as follows:

- BAUD RATE: 115200
- DATA: 8 bit

- PARITY: none
- STOP: 1bit
- FLOW CONTROL: none

See Figure 7 for a block diagram of the OMAP5432 EVM UART circuitry.

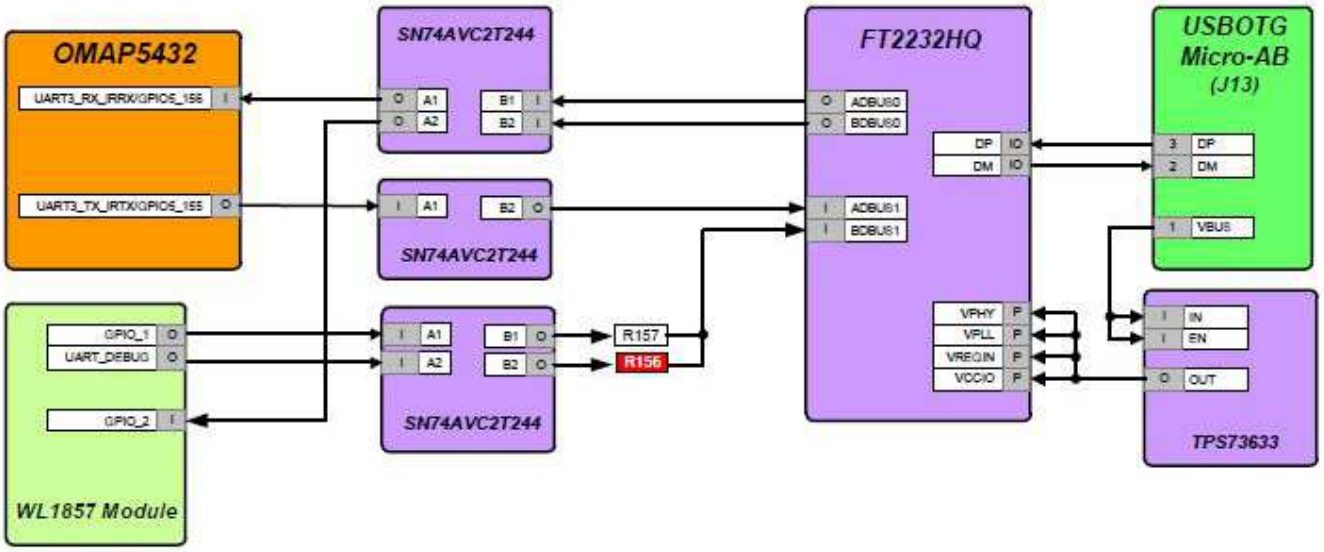


Figure 7. UART Communication Block Diagram

2.10 Micro-SD Card Connector

The OMAP5432 EVM supports removable memory storage via an onboard micro-SD card cage. It is a four-bit card cage that supports 1.8V or 3.0V cards. Card detect functionality is supported via GPIO5_152 of the OMAP5432 ES2.0 processor. See Figure 8 for a block diagram of the interface signaling to the card cage. The resistors shown in Figure 8 are 33 ohm series termination resistors.

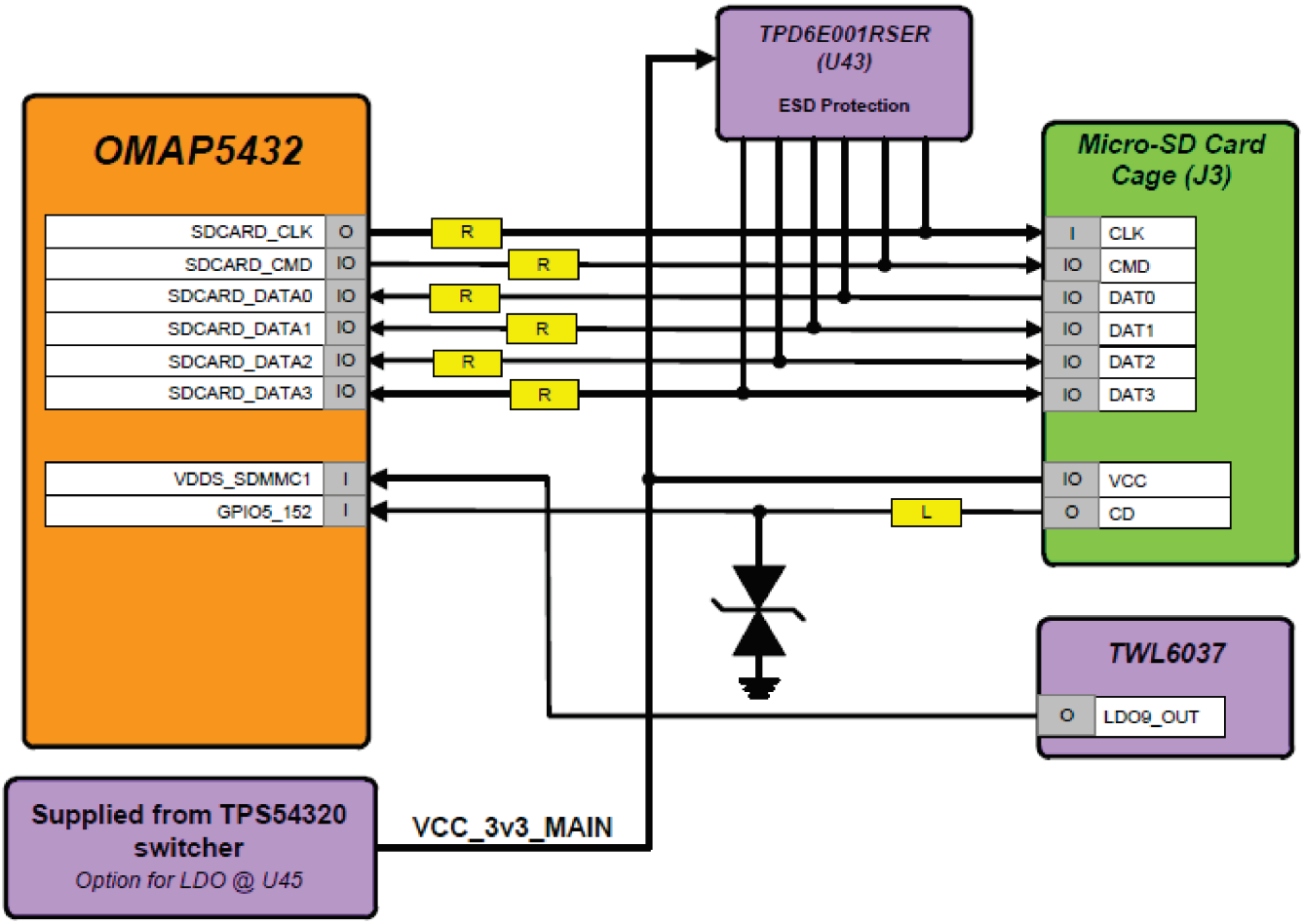


Figure 8. SDMMC1 Card Cage Block Diagram

2.11 Display Interfaces

The OMAP5432 EVM provides many options for connecting a display to the platform. These options are:

- Via the OMAP5432 ES2.0 internal HDMI phy connected to the micro-HDMI connector at J7
- Via the OMAP5432 ES2.0 DSIPORTA and/or DSIPORTC interface(s), connected via an external display PCB connected to the Main Expansion Connector J20 (Hirose P/N FX6-100P-0.8SV2)
- Via the OMAP5432 ES2.0 parallel display interface (DISPC) via Main expansion connectors J20 (Hirose P/N FX6-100P-0.8SV2)

2.11.1 HDMI connector

The OMAP5432 EVM provides a High-Definition Multimedia Interface (HDMI) via an industry-standard Type D connector at location J7. The interface is provided using the internal HDMI module provided by the OMAP5432 ES2.0. See Figure 9 for a block diagram of the OMAP5432 EVM HDMI circuitry. This interface includes a Texas Instruments TPD12S016 HDMI Port Protection/Interface device. A datasheet OMAP5432 EVM System Reference Manual Revision 0.5 April 18, 2013 DOC-21164 Page 26 of 65 for the TPD12S016RKTR may be found at http://www.ti.com/product/tpd12s016. The high-speed differential clock and data lines are connected straight from OMAP through common mode chokes to the ESD protection device, to the connector, so that any ESD event experienced at the connector will be absorbed before damaging the OMAP5432 ES2.0 device I/Os.

In addition to providing ESD protection on the signals coming from the connector, this device performs voltage translation on the control signals in the HDMI interface (SCL, SDA, CEC, and HPD) from the 1.8V levels of the OMAP5432 ES2.0 to the 5V levels required by a TV set. See Table 3 for the GPIOs used on the HDMI interface and a description of their function. These GPIOs are sourced from the GPIO expander connected to the I2C5 interface from OMAP.

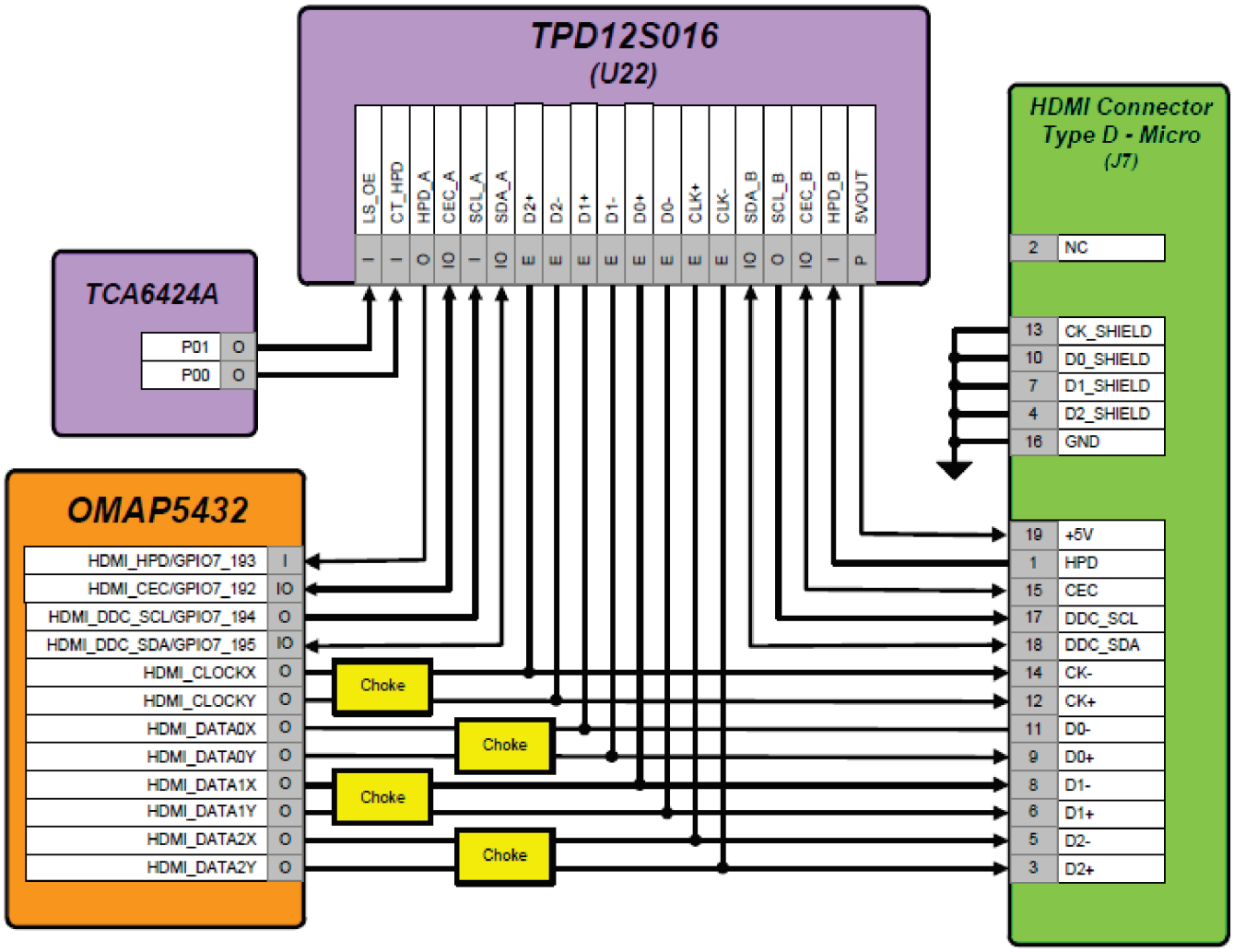


Figure 9. HDMI Interface Block Diagram

Table 3. HDMI GPIO Definitions

GPIO	Signal Name	Description
GPIO_Exp P01	HDMI_LS_OE	TPD12S016 Level Shifter Enable 1 = Enabled, 0 = Disabled
GPIO_Exp P00	CT_ HPD	TPD12S016 Load Switch Enable 1 = Enabled, 0 = Disabled

2.11.2 DSI Expansion via Expansion Connector (J20)

Another display option for the OMAP5432 EVM is via the DSIPORTA and DSIPORTC interfaces provisioned via a 100-pin Expansion Connector mounted on the backside of the PCB (J20). This connector is a Hirose part (part number FX6-100P-0.8SV91). See Figure 10 on page 28 for the pinout of DSI Expansion signals contained on this connector. This connector provides the capability to support either two separate LCD interfaces (one using DSIPORTA and the other using DSIPORTC), or a single large display panel that requires the use of both DSI interfaces.

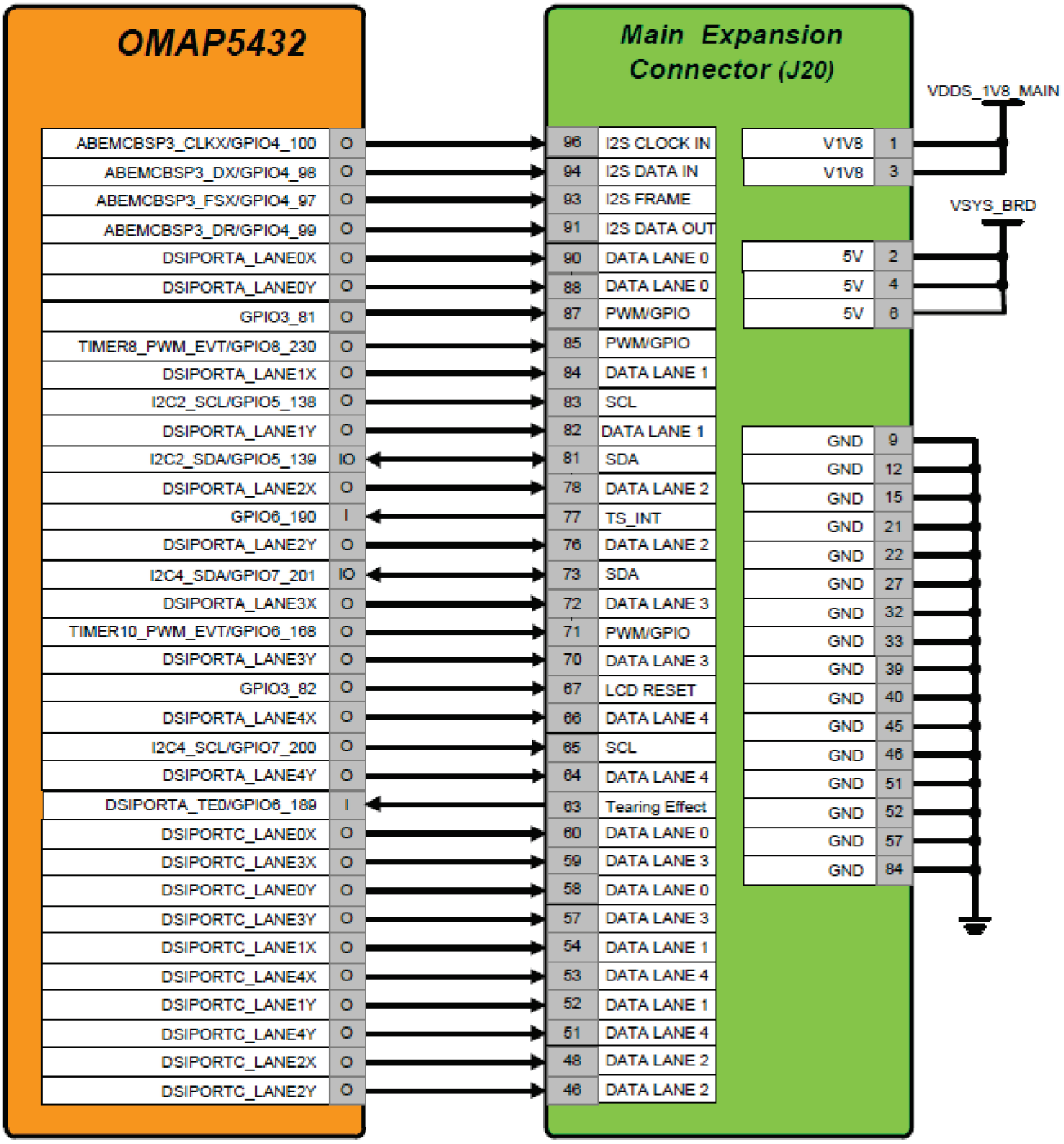


Figure 10. DSI Display on Expansion Connector (J20)

As a note to potential PCB designers using the DSI Expansion Connector to support a single large display panel using both DSI interfaces, the DSIPORTA and DSIPORTC interfaces are length matched within each interface, but due to PCB routing congestion on the OMAP5432 EVM, the interfaces were not matched to one another. On the current OMAP5432 EVM layout, the DSIPORTC interface pairs are approximately 220 mils (5.588 mm) longer than their DSIPORTA counterparts. This mismatch should be adjusted on any application board using both DSI interfaces to drive a single large display panel by making the DSIPORTA pairs longer than the DSIPORTC pairs by a similar amount.

2.11.3 Parallel Display Expansion via Expansion Connector

The final display option for the OMAP5432 EVM is through the OMAP5432 ES2.0 parallel display interface (DPI), provisioned via the 100-pin Main Expansion connector.

In Figure 11, the majority of the display signals connected to J19 are connected through zero ohm resistors (designated in Figure 11 as “Rmux”). The zero ohm resistors are provisioned so that this connector can be used to provision an alternate audio codec (replacing the onboard TWL6040 device). The details of this muxing are discussed in paragraph .

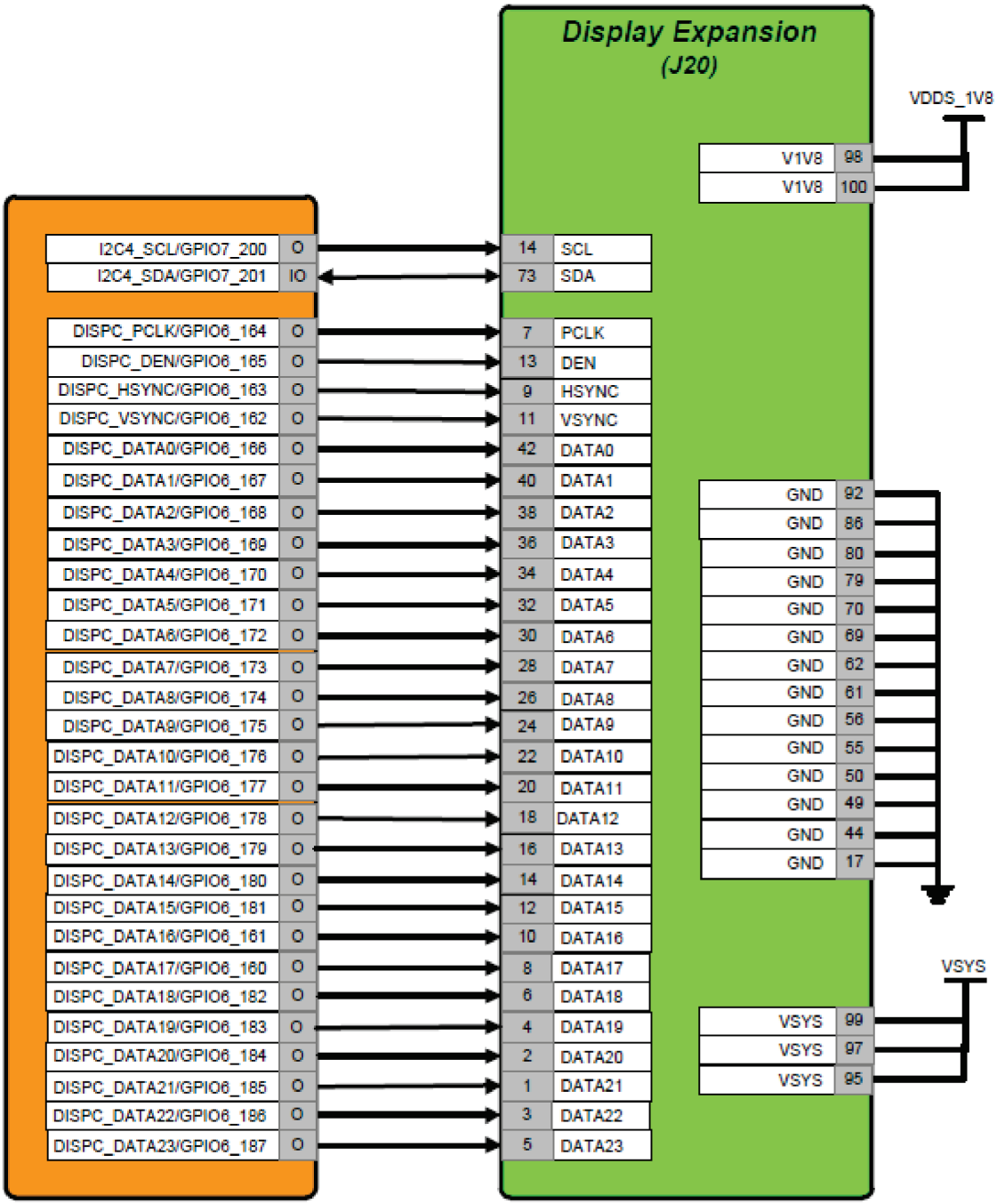


Figure 11. Parallel Display on Expansion Connector (J20)

2.12 Bluetooth/WLAN/NFC Interfaces

OMAP5432 ES2 interfaces with a module (TDK preliminary part number R078C) that provides a Bluetooth interface, a 2.4/5 GHz 802.11b/g/n interface, an NFC interface, and an FM interface. This module may be found on sheet 8 of the schematics (reference designator U33). It uses Texas Instruments' WiLinkTM 8.0 solution. Please note that this portion of the design is not currently shipped with the OMAP5432 EVM.

See Figure 12 for a diagram of the OMAP5432 ES2 connectivity to this module. See Table 4 for a description of the GPIOs used to interface to the module and their function.

The OMAP5432 interfaces are connected to the TDK WiLink™ module as follows:

- WLSDIO: WLAN SDIO interface
- UART5: Bluetooth Host Control Interface
- McBSP1: Bluetooth Audio Digital PCM Path
- McBSP2: FM I2S Interface

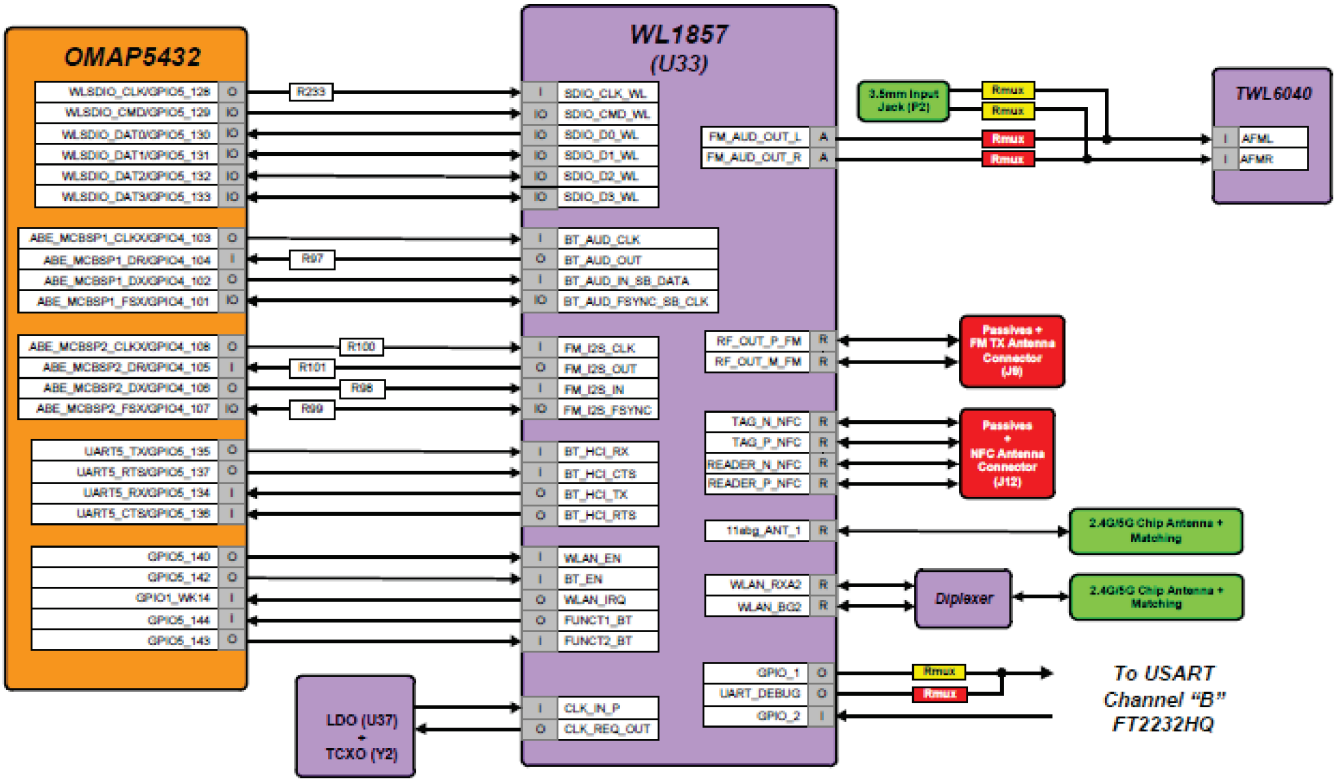


Figure 12. Pandaboard5 WLAN/Bluetooth Interface Block Diagram

Table 4. WLAN/Bluetooth Module GPIO Definitions

GPIO	Dir.	Signal Name	Description
GPIO5_140	O	WLAN_EN	802.11b/g Enable 1 = Enabled, 0 = Disabled
GPIO5_142	O	BT_EN	Bluetooth Enable 1 = Enabled, 0 = Enabled
GPIO5_143	O	BT_WAKEUP	Blutetooth Wakeup
GPIO5_144	I	HOST_WU	Host Wakeup
GPIO1_WK14	I	WLAN_nIRQ	WLAN Interrupt Input

2.13 Audio Interfaces

2.13.1 TWL6040 Audio Companion IC

See Figure 13 for a block diagram of the audio connectivity on the OMAP5432 EVM. In this block diagram, the signals with a red background in the box specifying their direction are analog I/Os while all others are 1.8V digital I/Os.

The OMAP5432 EVM provides two 3.5mm audio jack connections to provide line in and line out capability via the TWL6040 Audio Companion IC. It also provides a headset connector that supports 3.5mm headsets. There is a TS3A225ERTER device on the headset microphone lines, which performs automatic detection and swapping of the mic and ground portions of the audio jack to support all types of headsets (i.e. tip/ring/mic/sleeve as well as tip/ring/sleeve/mic). The digital path for audio back to the OMAP5432 ES2.0 processor is through the MCPDM interface.

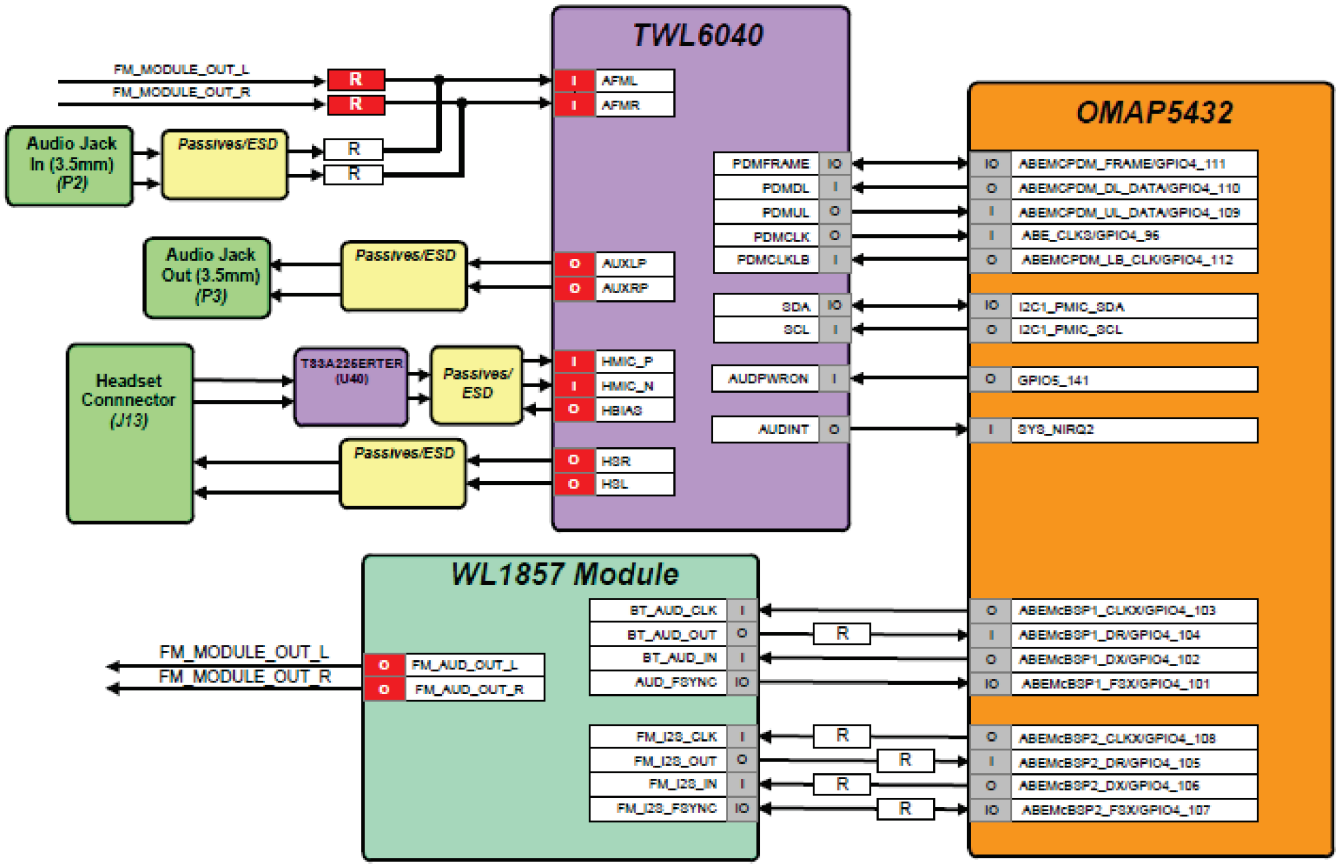


Figure 13. Audio Interface Block Diagram

2.14 USB Interfaces

The OMAP5432 EVM utilizes three USB interfaces. The first is the USB3.0 interface from the internal transceiver within OMAP to the USB3.0 connector at J11. The second interface utilizes the two-wire HSIC interface (USBB2) to an onboard phy (SMSC P/N USB3503A-1-GL-TR), which provides three DP/DM USB Host Ports (two of which are connected to the Dual Type-A connector at J6). The third interface utilizes the two-wire HSIC interface (USBB3) to an onboard phy (SMSC P/N LAN9730-ABZJ), which provides a 10/100 Ethernet interface via the RJ-45 connector at J5. Each of these interfaces will be discussed in more detail in the following paragraphs.

2.14.1 USBOTG Interface

The OMAP5432 EVM uses the USB3.0 transceiver within the OMAP5432 ES2.0 that is connected to an industry-standard USB3.0 connector (J11) as shown in Figure 14. The VBUS from the connector is connected to the TWL6037 companion Power IC, which can provide VBUS power via the SMPS10 boost converter in host mode.

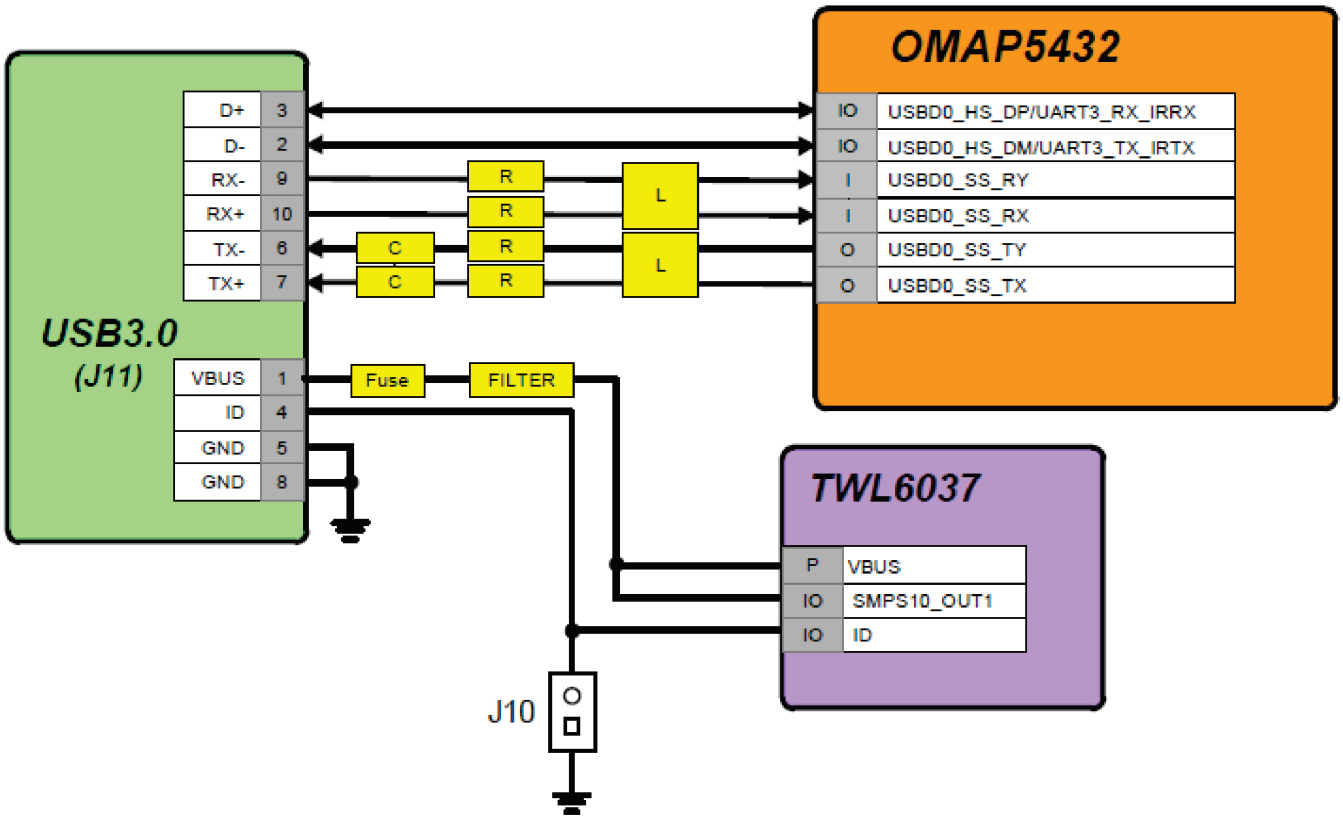


Figure 14. USBOTG Interface Block Diagram

2.14.2 USBB2 HSIC Interface (USB Host Ports)

The OMAP5432 EVM uses the two-wire OMAP5432 ES2.0 USBB2 HSIC interface connected to an SMSC USB3503A-1-GL-TR phy. This Phy converts the two-wire HSIC interface to three downstream DP/DM host port pairs. Two of these ports are connected to the dual USB Type-A connector at J6, while the third is connected to expansion connector J17. See Figure 15 for a block diagram of the OMAP5432 EVM USBB2 interface connectivity.

NOTE: The reference clock to the USB3503A is sourced from the FREF_CLK1_OUT output of OMAP5432 ES2.0, and this OMAP output must be programmed for a clock frequency of 19.2 MHz for proper operation

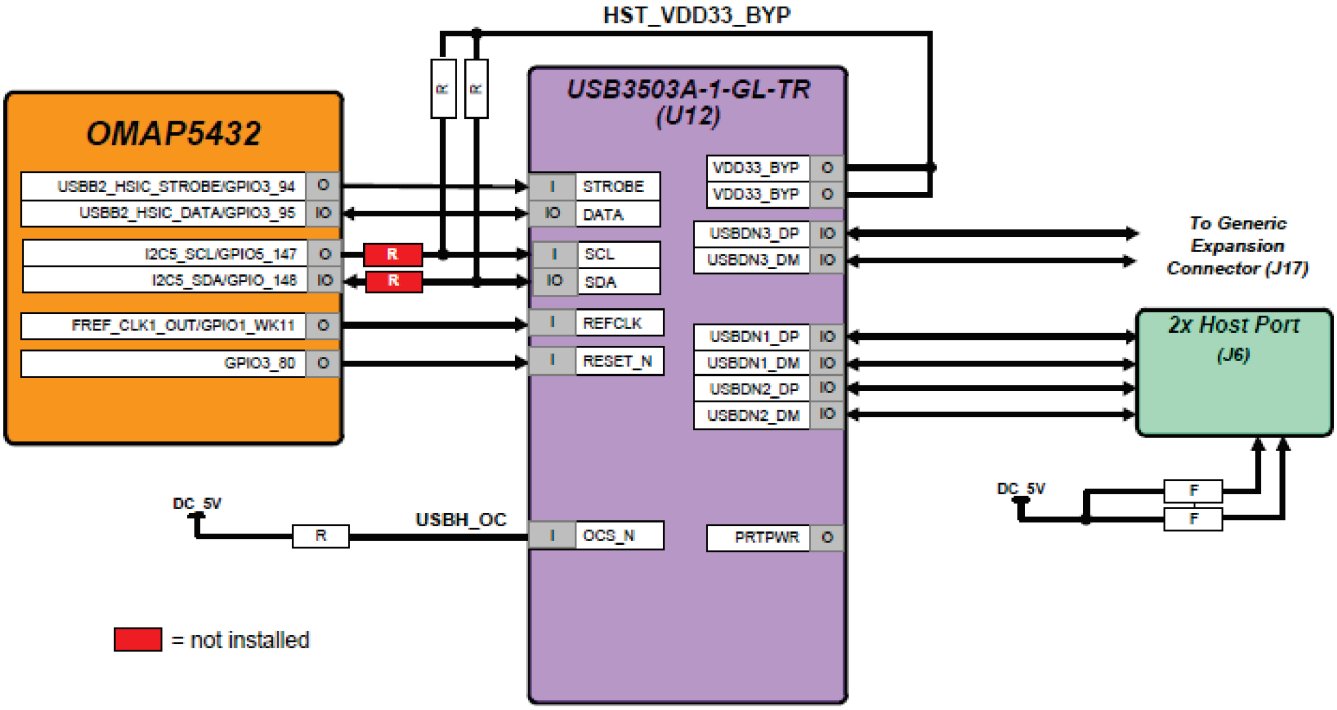


Figure 15. USBB2 Interface Block Diagram

See Table 5 for the definition of the GPIOs used to provide USB Host Port functions.

Table 5. USB Host Port GPIO Definitions

GPIO	Dir.	Signal Name	Description
GPIO3_80	O	H_USBH_NRESET	USB Host Port Hub Reset 0 = Hub and Phy held in reset 1 = Normal operation
GPIO1_WK11	O	H_FREFCLK_1	This pin needs to be used as FREF_CLK1_OUT, and programmed to output 19.2 MHz

2.14.3 USBB3 HSIC Interface (Ethernet)

The OMAP5432 EVM uses the two-wire OMAP5432 USBB3 HSIC interface connected to an SMSC Phy chip (part number LAN9730-ABZJ). This Phy uses the HSIC interface to provide a 10/100 Base-T Ethernet interface via receive/transmit pairs sourced and received through isolation transformers included inside the industry standard tab up RJ-45 connector at J5. The 93AA56AT device at U17 is a serial EEPROM that can be used to store the MAC address and other information. It is not populated on the OMAP5432 EVM board, so this information must be programmed by S/W. See Figure 16 for a block diagram of the USBB3 interface connectivity.

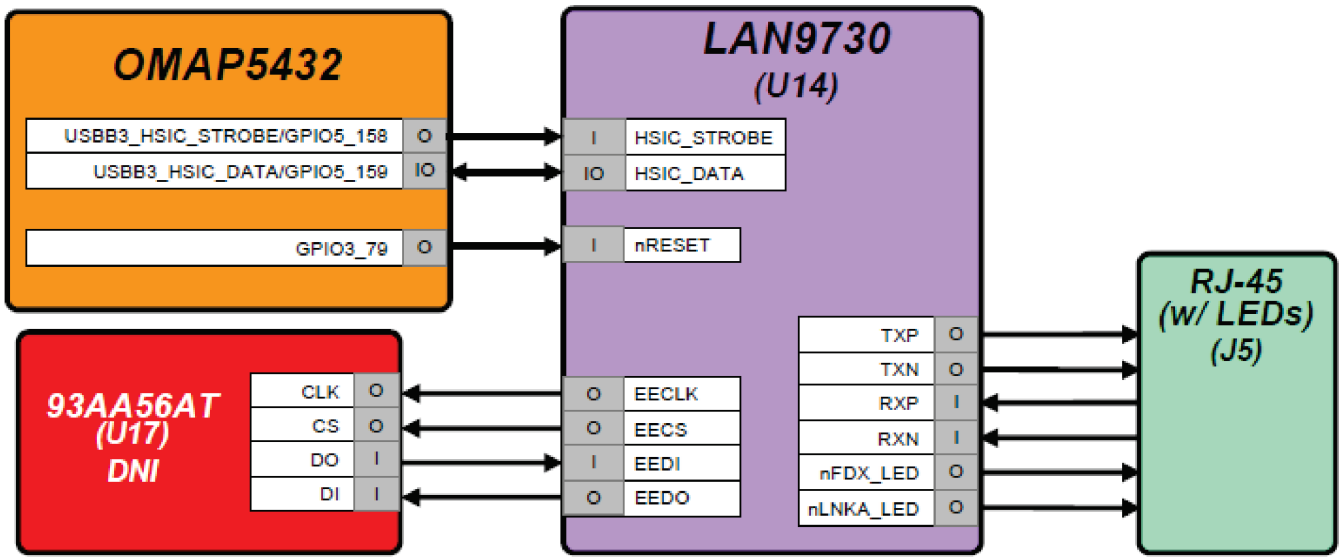


Figure 16. USBB3 Interface Block Diagram

2.15 Expansion Connectors

The OMAP5432 EVM provides 5 expansion connectors to enable users to interface custom designed or purchased peripheral boards with the OMAP5432 ES2.0 processor. These connectors consist of:

- J20 – a 100-pin, 0.8mm pitch SMT connector mounted on the back side of the PCB
- J21 – a 20-pin, 0.8mm pitch SMT connector, also mounted on the back side of the PCB
- J17 – a 14-pin, 0.1” pitch through-hole header, mounted on the top side of the PCB
- J2 – a 30-pin, 0.Xmm pitch SMT connector mounted on the top side of the PCB
- J18 – a 60-pin, 0.Xmm pitch SMT connector mounted on the top side of the PCB

These connectors will be discussed in the following paragraphs.

2.15.1 Main Expansion Connector (J20)

The OMAP5432 EVM provides a single 100-pin SMT expansion connector, which provides the majority of the platform expansion capability. This connector used on the OMAP5432 EVM is a 0.8mm pitch SMT connector (Hirose P/N FX6-100P-0.8SV91). The appropriate mating connector for an interface board should be chosen from the Hirose datasheet. The placement of this connector on the OMAP5432 EVM PCB is shown in Figure 17. On this diagram, pin 1 of the connector is located bottom left, pin 2 is top left and odds/evens go down the bottom and top of the connector, respectively.

See Table 6 for the pinout of the Main Expansion Connector. Table 6 shows the primary function that is available on the connector pin, along with the alternate function that can be selected by changing the OMAP5432 ES2.0 pin multiplexing.

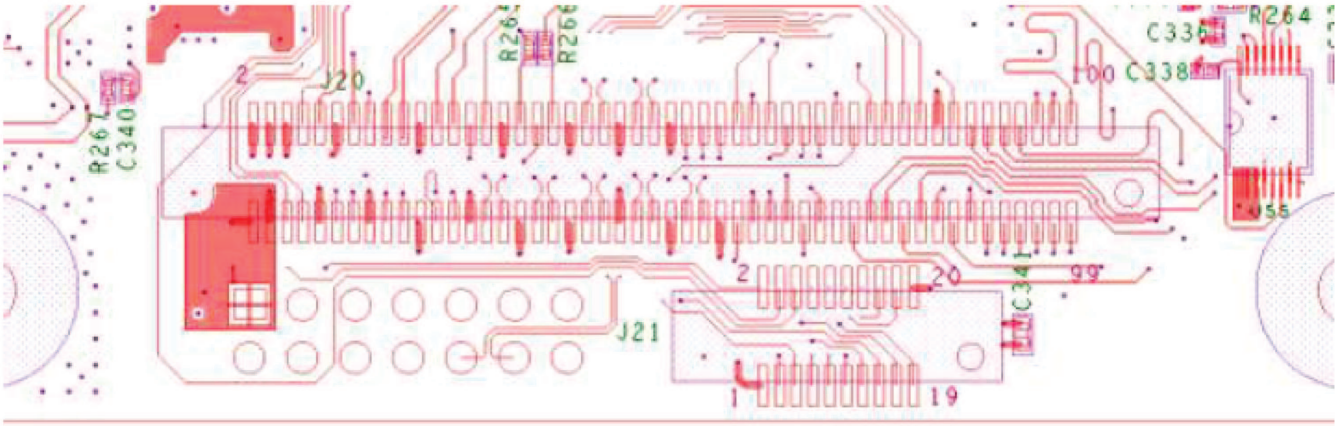


Figure 17. Expansion Connectors - J20 and J21 (Bottom Side of PCB)

Table 6. Main Expansion Connector Pin Definitions (J20)

J20 Pin #	OMAP Ball #	Primary Function	Secondary Function	Description of OMAP5432 EVM Usage
100	---	VDDS_1V8_MAIN	---	1.8V I/O Power
99	---	VSYS_BRD	---	3.7Vdc Input Power
98	---	VDDS_1V8_MAIN	---	1.8V I/O Power
97	---	VSYS_BRD	---	3.7Vdc Input Power
96	AE27	H_MCBSP3_CLKX	GPIO4_100	McBSP3 Clock/GPIO
95	---	VSYS_BRD	---	3.7Vdc Input Power
94	AE29	H_MCBSP3_DX	GPIO4_98	McBSP3 Transmit Data/GPIO
93	AF28	H_MCBSP3_FSX	GPIO4_97	McBSP3 Frame Sync/GPIO
Mult.	---	GND	---	Signal Ground (ground is on pins 17,44,49,50, 55,56,61,62,68,69,74,79,80,86, 89, and 92 of this connector
91	AE28	H_MCBSP3_DR	GPIO4_99	McBSP3 Receive Data/GPIO
90	AD31	H_DSIPORTA_LANBOX	---	DSI Port A Lane 0+
88	AD32	H_DSIPORTA_LANBOY	---	DSI Port A Lane0-
87	F14	GPIO3_81	GPMC_NCS2	GPIO or GPMC Chip select
85	AD7	GPIO8_230	TIMER8_PWM_EVT	GPIO or Display/Backlight PWM
84	AC31	H_DSIPORTA_LANE1X	---	DSI Port A Lane 1+
83	AL33	H_I2C2_SCL	---	I2C Serial Clock
82	AC32	H_DSIPORTA_LANE1Y	---	DSI Port A Lane 1-
81	AM32	H_I2C2_SDA	---	I2C Serial Data
78	AB32	H_DSIPORTA_LANE2X	---	DSI Port A Lane 2+
77	AJ33	H_TIMER9_PWM/GPIO6_190	GPIO6_190	Display/Backlight PWM or GPIO
76	AB31	H_DSIPORTA_LANE2Y	---	DSI Port A Lane2-
75	AK30	H_DSIPORTC_TE0/GPIO6_191	GPIO6_191	DSI Port C Tearing Effect or GPIO
73	AJ20	H_I2C4_SDA	---	I2C Serial Data
72	AA32	H_DSIPORTA_LANE3X	---	DSI Port A Lane 3+
71	---	H_TIMER10_PWM/GPIO6_188	GPIO6_188	Display/Backlight PWM or GPIO
70	AA31	H_DSIPORTA_LANE3Y	---	DSI Port A Lane3-

Table 6. Main Expansion Connector Pin Definitions (J20) (continued)

J20 Pin #	OMAP Ball #	Primary Function	Secondary Function	Description of OMAP5432 EVM Usage
67	G14	GPIO3_82	GPMC_NCS3	GPIO or GPMC Chip select
66	y32	H_DSIPORTA_LANE4X	---	DSI Port A Lane 4+
65	AJ21	H_I2C4_SCL	---	I2C Serial Clock
64	Y31	H_DSIPORTA_LANE4Y	---	DSI Port A Lane 4-
63	W33	H_DSIPORTA_TE0/GPIO6_189	GPIO6_189	DSI Port A Tearing Effect or GPIO
60	AJ31	H_DSIPORTC_LANE0X	---	DSI Port C Lane 0+
59	AF32	H_DSIPORTC_LANE3X	---	DSI Port C Lane3+
58	AJ32	H_DSIPORTC_LANE0Y	---	DSI Port C Lane 0-
57	AF31	H_DSIPORTC_LANE3y	---	DSI Port C Lane 3-
54	AH32	H_DSIPORTC_LANE1X	---	DSI Port C Lane 1+
53	AE32	H_DSIPORTC_LANE4X	---	DSI Port C Lane 4+
52	AH31	H_DSIPORTC_LANE1Y	---	DSI Port C Lane 1-
51	AE31	H_DSIPORTC_LANE4Y	---	DSI Port C Lane 4-
48	AG32	H_DSIPORTC_LANE2X	---	DSI Port C Lane 2+
47	N27	H_GPMC_WAIT0	GPIO2_45	GPMC Wait Input
46	AG31	H_DSIPORTC_LANE2Y	---	DSI Port C Lane2-
45	J29	H_GPMC_nWP	GPIO2-35	GPMC Write Protect
43	F13	H_GPMC_NWE	GPIO3_84	GPMC Write Enable
42	AL17	H_DISPC_DATA0	GPIO6_166	Parallel Display Data Bit 0
41	N9	H_GPMC_NOE	GPIO3_85	GPMC Output Enable
40	AM17	H_DISPC_DATA1	GPIO6_167	Parallel Display Data Bit 1
39	F25	H_GPMC_nBE0_CLE	GPIO2_34	GPMC Byte Enable/Command Latch Enable
38	AN17	H_DISPC_DATA2	GPIO6_168	Parallel Display Data Bit 2
37	E25	H_GPMC_nADV_ADV	GPIO2_33	GPMC Address Valid/Address Latch Enable
36	AL16	H_DISPC_DATA3	GPIO6_169	Parallel Display Data Bit 3
35	J28	H_GPMC_CLK	GPIO2_36	GPMC Clock
34	AM16	H_DISPC_DATA4	GPIO6_170	Parallel Display Data Bit 4
33	E26	H_GPMC_AD7	GPIO2_44	GPMC Address/Data Bit 7
32	AL15	H_DISPC_DATA5	GPIO6_171	Parallel Display Data Bit 5
31	F26	H_GPMC_AD6	GPIO2_43	GPMC Address/Data Bit 6
30	AM15	H_DISPC_DATA6	GPIO6_172	Parallel Display Data Bit 6
29	E27	H_GPMC_AD5	GPIO2_42	GPMC Address/Data Bit 5
28	AN15	H_DISPC_DATA7	GPIO6_173	Parallel Display Data Bit 7
27	E29	H_GPMC_AD4	GPIO2_41	GPMC Address/Data Bit 4
26	AL14	H_DISPC_DATA8	GPIO6_174	Parallel DIsplay Data Bit 8
25	G29	H_GPMC_AD3	GPIO2_40	GPMC Address/Data Bit 3
24	AM14	H_DISPC_DATA9	GPIO6_175	Parallel Display Data Bit 9
23	H29	H_GPMC_AD2	GPIO2_39	GPMC Address/Data Bit 2
22	AM12	H_DISPC_DATA10	GPIO6_176	Parallel Display Data Bit 10
21	H28	H_GPMC_AD1	GPIO2_38	GPMC Address/Data Bit 1
20	AL11	H_DISPC_DATA11	GPIO6_177	Parallel Display Data Bit 11
19	J27	H_GPMC_AD0	GPIO2_37	GPMC Address/Data Bit 0
18	AM11	H_DISPC_DATA12	GPIO6_178	Parallel DIsplay Data Bit 12
16	AN11	H_DISPC_DATA13	GPIO6_179	Parallel Display Data Bit 13
15	P32	H_GPMC_nCS0	GPIO2_32	GPMC Chip select 0

Table 6. Main Expansion Connector Pin Definitions (J20) (continued)

J20 Pin #	OMAP Ball #	Primary Function	Secondary Function	Description of OMAP5432 EVM Usage
14	AL10	H_DISPC_DATA14	GPIO6_180	Parallel Display Data Bit 14
13	AM18	H_DISPC_DEN	GPIO6_165	Parallel Display Data Enable
12	AM10	H_DISPC_DATA15	GPIO6_181	Parallel Display Data Bit 15
11	AL12	H_DISPC_VSYNC	GPIO6_162	Parallel Display Vertical Sync
10	AM13	H_DISPC_DATA16	GPIO6_161	Parallel Display Data Bit 16
9	AL13	H_DISPC_HSYNC	GPIO6_163	Parallel Display Horizontal Sync
8	AN13	H_DISPC_DATA17	GPIO6_160	Parallel Display Data Bit 17
7	AL18	H_DISPC_PCLK	GPIO6_164	Parallel Display Pixel Clock
6	AN9	H_DISPC_DATA18	GPIO6_182	Parallel Display Data Bit 18
5	AN7	H_DISPC_DATA23	GPIO6_187	Parallel Display Data Bit 23
4	AM9	H_DISPC_DATA19	GPIO6_183	Parallel Display Data Bit 19
3	AL8	H_DISPC_DATA22	GPIO6_186	Parallel Display Data Bit 22
2	AL9	H_DISPC_DATA20	GPIO6_184	Parallel Display Data Bit 20
1	AM8	H_DISPC_DATA21	GPIO6_185	Parallel Display Data Bit 21

2.15.2 GPMC Expansion Connector (J21)

In addition to the 100-pin SMT expansion connector on the back side of the PCB, the OMAP5432 EVM provides a 20-pin SMT expansion connector, also mounted on the back side of the PCB, which provides the capability to support the full-up GPMC bus. The 100-pin connector can support GPMC operation for 8-bit NAND flash (with the GPMC control signals, and lower 8-bits of the address/data bus), but J21 must be used to support other memory devices (e.g. NOR flash, or OneNAND). This connector is a 0.8mm pitch SMT connector (Hirose P/N FX6-20P-0.8SV91). The appropriate mating connector should be chosen from the Hirose datasheet. The placement of this connector on the OMAP5432 EVM PCB is shown in Figure 17. On this diagram, pin 1 of the connector is located bottom left, pin 2 is top left and odds/evens go down the bottom and top of the connector, respectively.

Table 7. GPMC Expansion Connector Pin Definitions (J21)

J21 Pin #	OMAP Ball#	Primary Function	Secondary FUnction	Description of OMAP5432 EVM Usage
20	---	GND	---	Signal Ground
19	G33	H_GPMC_AD15	GPIO2_63	GPMC Address/Data Bit 15
18	F20	H_GPMC_NCS1	GPIO3_77	GPMC Chip Select 1
17	G32	H_GPMC_AD14	GPIO2_62	GPMC Address/Data Bit 14
16	F17	H_GPMC_A24	GPIO3_78	GPMC Address Bit 24
15	H31	H_GPMC_AD13	GPIO2_61	GPMC Address/Data Bit 13
14	F21	H_GPMC_A23	GPIO4_120	GPMC Address Bit 23
13	G31	H_GPMC_AD12	GPIO2_60	GPMC Address/Data Bit 12
12	E21	H_GPMC_A22	GPIO4_119	GPMC Address Bit 22
11	J31	H_GPMC_AD11	GPIO2_59	GPMC Address/Data Bit 11
10	H21	H_GPMC_A21	GPIO4_118	GPMC Address Bit 21
9	H32	H_GPMC_AD10	GPIO2_58	GPMC Address/Data Bit 10
8	G21	H_GPMC_A20	GPIO4_117	GPMC Address Bit 20
7	J33	H_GPMC_AD9	GPIO2_57	GPMC Address/Data Bit 9
6	F24	H_GPMC_A19	GPIO4_116	GPMC Address Bit 19
5	J32	H_GPMC_AD8	GPIO2_56	GPMC Address/Data Bit 8
4	E24	H_GPMC_A18	GPIO4_115	GPMC Address Bit 18
3	G24	H_GPMC_A16	GPIO4_113	GPMC Address Bit 16

Table 7. GPMC Expansion Connector Pin Definitions (J21) (continued)

J21 Pin #	OMAP Ball#	Primary Function	Secondary FUnction	Description of OMAP5432 EVM Usage
2	H24	H_GPMC_A17	GPIO4_114	GPMC Address Bit 17
1	---	GND	---	Signal Ground

2.15.3 Generic Expansion Connector (J17)

There is a 14-pin 0.1” pitch through-hole connector on the top side of the board that provides a small number of miscellaneous signals for expansion use. The signals provided on this connector are:

- McSPI2
- UART2
- I^2C2
- Third USB host port from the USB3503A Hub IC

The placement of this connector on the OMAP5432 EVM PCB is shown in Figure 18 below. On this diagram, pin 1 of the connector is located top right, pin 2 is bottom right and odds/evens go down the top and bottom of the connector, respectively.

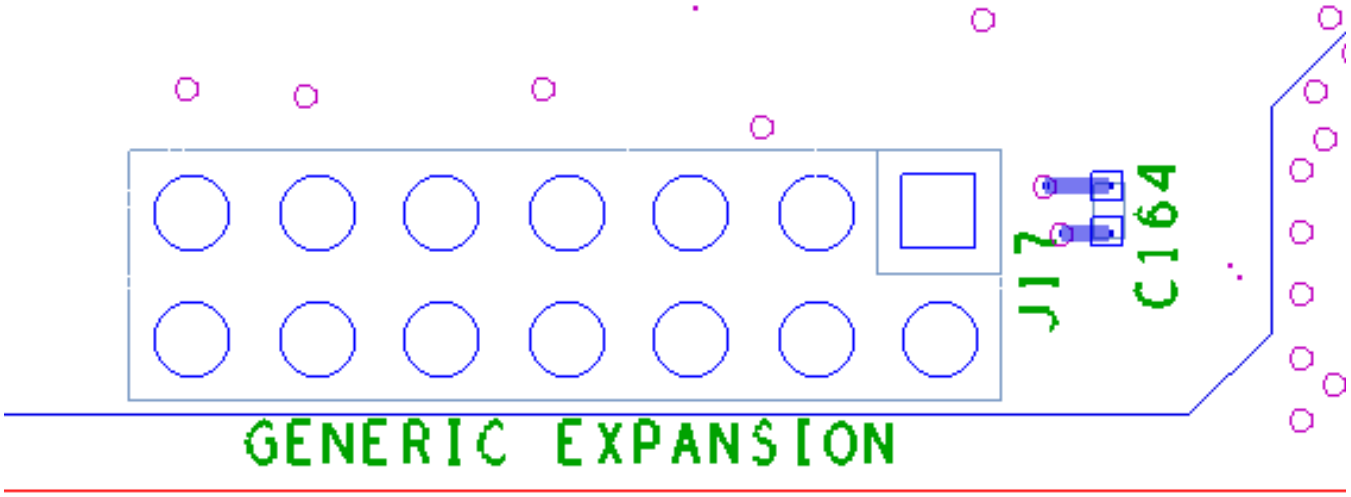


Figure 18. Generic Expansion Connector – J17 (Top Side of PCB)

Table 8. Generic Expansion Connector Pin Definitions (J17)

J17 Pin #	OMAP Ball #	Primary Function	Secondary Function	Description of OMAP5432 EVM Usage
1	---	VDDS_1V8_MAIN	---	1.8V I/O Power
2	---	VCC 3V3 MAIN	---	3.3V Power
3		H_UART2_TX		UART2 Transmit Data
4		H_I2C2_SCL		I2C2 Serial Clock
5		H_UART2_RX		UART2 Receive Data
6		H_I2C2_SDA		I2C2 Serial Data
7		H_MCSPI2_SIMO	GPIO7_198	SPI2 Slave In, Master Out
8	---	DC_5V	---	5V Power (System Power/VBUS for host port)
9		H_MCSPI2_CS0	GPIO7_196	SPI2 Chip Select 0

Table 8. Generic Expansion Connector Pin Definitions (J17) (continued)

J17 Pin #	OMAP Ball #	Primary Function	Secondary Function	Description of OMAP5432 EVM Usage
10		USBH_DP3	---	USB Host Port Data+
11		H_MCSPI2_SOMI	GPIO7_199	SPI2 Slave Out, Master In
12		USBH_DM3	---	USB Host Port Data -
13		H_MCSPI2_CLK	GPIO7_197	SPI2 Clock
14	---	GND	---	Signal Ground

2.16 Camera Expansion

The OMAP5432 EVM does not provide an onboard camera sensor, but does provision for two camera expansion connectors. One of the connectors is a 30-pin camera connector (Samtec P/N TFM-115-32-SD-A) that is pin-compatible with the OMAP4 OMAP5432 EVM ES (OMAP4460) camera connector. This connector is placed on the top side of the PCB, and provides a single CSI-2 interface (CSIPORTA) as well as GPIOs for use on a plug-in camera module. See Section 2.16.1 for a description of this connector.

The second connector is a 60-pin connector (Hirose P/N FX6-60P-0.8SV2) that provides all OMAP5432 ES2.0 CSI-2 interfaces (CSIPORTA, CSIPORTB and CSIPORTC). It can also be used to provide a dual CSI-2 camera interfaces or a single parallel camera interface (with appropriate pin multiplexing done by software).

2.16.1 Single CSI Camera Expansion Connector (J2)

See Table 9 below for the pinout of the 30-pin camera expansion connector on the top side of the PCB.

NOTE: The GPIOs listed below don't have specific functions defined yet, as there has been no camera module designed. These GPIOs will be user-definable per the camera module implementation.

Table 9. Camera Expansion Connector Pin Definitions (J2)

J2 Pin #	OMAP Ball #	Signal Name	Signal Description
1,2	---	GND	Signal Ground
3	U6	H_CSIPORTA_LANE0X	CSI Signal Lane 0 Data X
4	N5	H_CSIPORTA_LANE3X	CSI SIgnal Lane 3 Data X
5	U5	H_CSIPORTA_LANE3Y	CSI SIgnal Lane 0 Data Y
6	N6	GND	CSI Signal Lane 3 Data Y
7,8	---	H_CSIPORTA_LANE1X	Signal Ground
9	P6	H_CSIPORTA_LANE4X	CSI Signal Lane 1 Data X
10	N7	H_CSIPORTA_LANE1Y	CSI Signal Lane 4 Data X
11	P5	H_CSIPORTA_LANE4Y	CSI Signal Lane 1 Data Y
12	N8	GND	CSI SIgnal Lane 4 Data Y
13,14	---	H_CSIPORTA_LANE2X	Signal Ground
15	P7	GPIO_WK13	CSI Signal Lane 2 Data X
16	N31	GPIO_WK13	OMAP_GPIO1_WK13
17	P8	H_GPIO8_227	CSI Signal Lane 2 Data Y
18	AE7	GND	OMAP GPIO8_227
19	---	H_CAM_ RESET/GPIO8_226	Signal Ground
20	AF6	H_I2C3_SCL	Camera Global Reset or GPIO8_226
21	AJ5	H_CAM_SHUTTER/GPIO8_224	I2C3 Serial Clock
22	AE6	H_I2C3_SDA	Camera Shutter or GPIO8_224
23	AH4	H_CAM_STROBE/GPIO8_225	I2C3 Serial Data

Table 9. Camera Expansion Connector Pin Definitions (J2) (continued)

J2 Pin #	OMAP Ball #	Signal Name	Signal Description
24	AE5	H_GPIO5_154	Camera Strobe or GPIO8_225
25	AJ24	H_GPIO8_228	OMAP GPIO5_154
26	AD5	H_FREFCLK_0	OMAP GPIO8_228
27	M31	H_GPIO8_229	OMAP Camera Clock In
28	AD6	VSYS_BRD	OMAP GPIO8_229
29	---	VSYS_BRD	Battery Voltage In
30	---	VCC 2V8 CAM	Onboard LDO (U42) 2.8V input voltage

2.16.2 Dual-CSI/Parallel Camera Expansion Connector (J18)

See Table 10 below for the pinout of the 60-pin camera expansion connector (J18) mounted on the back side of the PCB. The signal description column also shows the alternate functionality of the ball, if applicable. Note that this connector pinout was chosen where the signals common to camera expansion connector J2 on the top side of the PCB are directly below them to optimize signal routing.

Table 10. Dual CSI/Parallel Camera Expansion Connector Pin Definitions (J18)

J18 Pin #	OMAP Ball #	Singal Name	Signal Description
1	---	VSYS_BRD	Battery Voltage In
2	---	VCC_2V8_CAM	Onboard LDO (U42) 2.8V input voltage
3	---	VSYS BRD	Battery Voltage IN
4	---	VCC_2V8_CAM	Onboard LDO (U42) 2.8V input voltage
5	M31	H_FREFCLK 0	OMAP Camera Clock In
6	---	VSYS_BRD	Battery Voltage In
7	---	GND	Signal Ground
8	---	VSYS_BRD	Battery Voltage In
9	AJ24	H_GPIO5_154	OMAP GPIO5_154
10	---	GND	Signal Ground
11	AF5	H_GPIO8_234	OMAP GPIO8_234 (or CPI_VSYNC)
12	AD6	H_GPIO8_229	OMAP GPIO8_229
13	AH4	H_I2C3_SDA	I2C3 Serial Data
14	AD5	H_GPIO8_228	OMAP GPIO8_228
15	AJ5	H_I2C3_SCL	I2C3 Serial Clock
16	AE5	H_CAM_STROBE/GPIO8_225	Camera Strobe or GPIO8_225
17	AG5	H_GPIO8_233	OMAP GPIO8_233 (of CPI_HSYNC)
18	AE6	H_CAM_SHUTTER/GPIO8_224	Camera Shutter or GPIO8_224
19	---	GND	Signal Ground
20	AF6	H_CAM_ RESET/GPIO8_226	Camera Global Reset or GPIO8_226
21	P8	H_CSIPORTA_LANE2Y	CSI Signal Lane 2 Data Y (or CPI_DATA2)
22	AE7	H_GPIO8_227	OMAP GPIO8_227
23	P7	H_CSIPORTA_LANE2X	CSI Signal Lane 2 Data X (or CPI_DATA3)
24,25	---	GND	Signal Ground
26	---	PIO_GPIO_20	Camera Module ID 1
27	N31	GPIO_WK13	OMAP GPIO1_WK13
28,29	---	GND	Signal Ground
30	N8	H_CSIPORTA_LANE4Y	CSI SIgnal Lane 4 Data Y (or CPI_DATA7)

Table 10. Dual CSI/Parallel Camera Expansion Connector Pin Definitions (J18) (continued)

J18 Pin #	OMAP Ball #	Singal Name	Signal Description
31	P5	H_CSIPORTA_LANE1Y	CSI Signal Lane 1 Data Y (or CPI_DATA0)
32	N7	H_CSIPORTA_LANE4X	CSI Signal Lane 4 Data X (or CPI_DATA6)
33	P6	H_CSIPORTA_LANE1X	CSI Signal Lane 1 Data X (or CPI_DATA1)
34,35	---	GND	Signal Ground
36	AM32	I2C2_SDA	I2C2 Serial Data
37	AL33	H_I2C2_SCL	I2C2 Serial Clock
38,39	---	GND	Signal Ground
40	N6	H_CSIPORTA_LANE3Y	CSI Signal Lane 3 Data Y (or CPI_DATA5)
41	U5	H_CSIPORTA_LANE0Y	CSI Signal Lane 0 Data Y (or CPI_WEN)
42	N5	H_CSIPORTA_LANE3X	CSI Signal Lane 3 Data X (or CPI_DATA4)
43	U6	H_CSIPORTA_LANE0X	CSI Signal Lane 0 Data X (or CPI_PCLK)
44,45	---	GND	Signal Ground
46	Y5	H_CPI_DATA13	Parallel Camera Bit 13 (or CSIPORTB_LANE0Y)
47	J6	H_CPI_DATA8	Parallel Camera Bit 8 (or CSIPORTC_LANE0Y)
48	Y6	H_CPI_DATA12	Parallel Camera Bit 12 (or CSIPORTB_LANE0X)
49	J7	H_CPI_DATA9	Parallel Camera Bit 9 (or CSIPORTC_LANE0X)
50,51	---	GND	Signal Ground
52	Y7	H_CPI_DATA14	Parallel Camera Bit 14 (or CSIPORTB_LANE1Y)
53	K6	H_CPI_DATA10	Parallel Camera Bit 10 (or CSIPORTC_LANE1Y)
54	Y8	H_CPI_DATA15	Parallel Camera Bit 15 (or CSIPORTB_LANE1X)
55	K5	H_CPI_DATA11	Parallel Camera Bit 11 (or CSIPORTC_LANE1X)
56,57	---	GND	Signal Ground
58	AA5	H_GPIO8_IN250	Parallel Camera_HSYNC IN (or CSIPORTB_LANE2Y)
59	---	PIO_GPIO_17	Camera Module ID 0
60	AA6	H_GPIO8_IN251	Parallel Camera VSYNC IN (or CSIPORTB_LANE2X)

2.17 JTAG Connector (J1)

The OMAP5432 EVM provides a 14-pin 0.1” (2.54mm) pitch through-hole connector at J1 as shown in Figure 19. In Figure 19, pin 1 is the upper right pin and pin 2 is directly below it. Even numbered pins are on the bottom side of the connector, and odd numbered pins are along the top. Pin 6 is removed to comply with the keying on the JTAG pods.

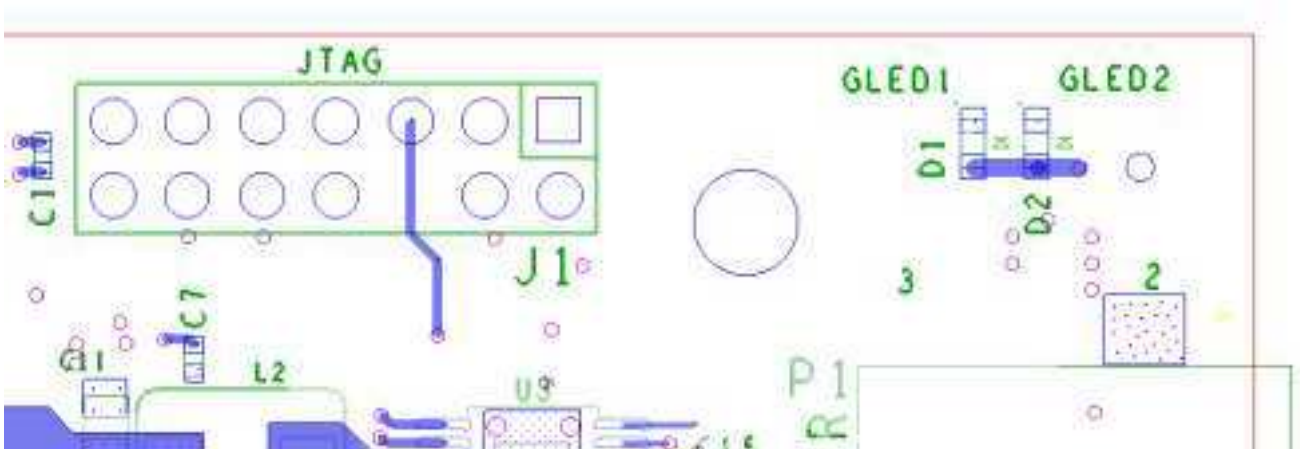


Figure 19. 14-pin JTAG Connector (J1)

See Table 11 for a description of the pins their connectivity to OMAP5432 ES2.0, and their function on this connector.

Table 11. JTAG Connector Pinout (J1)

J1 Pin #	OMAP Ball #	Signal Name	Signal Description
1	B31	J_JTAG_TMSC	JTAG Test Mode Select
2	B32	H_JTAG_NTRST	JTAG Test Reset (Active low)
3	A32	H_JTAG_TDI	JTAG Test Data In
4,8,10,12	---	GND	Signal Ground
5	---	VDDS_1V8_MAIN	1.8V JTAG Power
6	---	---	N/A
7	A33	H_JTAG_TDO	JTAG Test Data Out
9	B33	H_JTAG_RTCK	JTAG Return CLock Out
11	C31	H_JTAG_TCK	JTAG Clock In
13	K32	H_DM_EMU0	Emulator I/O 0
14	K31	H_DM_EMU1	Emulator I/O 1

2.18 LED Indicators

The OMAP5432 EVM provides multiple LED indicators. See Figure 20 for the location of these LEDs on the OMAP5432 EVM PCB.

LEDs D1 and D2 are blue LEDs that are controlled directly via OMAP5432 ES2.0 GPIOs. D1 is controlled by GPIO5_153 (ball AJ25), while D2 is controlled by GPIO1_WKOUT4 (ball V32). For both of these LED indicators, writing the respective GPIO high will turn on the LED, while writing it low will turn off the LED.

LED D3 is a red LED that will be illuminated if the board is powered from a 5V wall supply, and will be dark if the board is powered from a wall supply ranging from 6V to 15V. This LED is NOT software controllable.

LEDs D4 through D8 are green LEDs that are controlled via the I/O expander connected to the OMAP I^2C5 bus. The LEDs are controlled by the GPIO Expander as follows:

- D4 -> GPIO Expander Bit P06
- D5 -> GPIO Expander Bit P05
- D6 -> GPIO Expander Bit P04
- D7 -> GPIO Expander Bit P03
- D8 -> GPIO Expander Bit P02

Writing a high to the respective GPIO bit will turn on the LED, while writing it low will turn off the LED.

LED D13 is a green LED that is controlled automatically via onboard circuitry. This LED is illuminated when a USB cable is plugged into the micro-AB USB debug connector at J14. It indicates that 5V VBUS power is being received from the host, which is used to power the USART circuitry.

LED D14 is a tri-color LED that is controlled via the I/O expander connected to the OMAP I2C5 bus. The LEDs are controlled by the GPIO Expander as follows:

- Red LED -> GPIO Expander Bit P21
- Green LED -> GPIO Expander Bit P22
- Blue LED -> GPIO Expander Bit P23

Writing a high to the respective GPIO bit will turn on the particular color LED, while writing it low will turn off the LED.

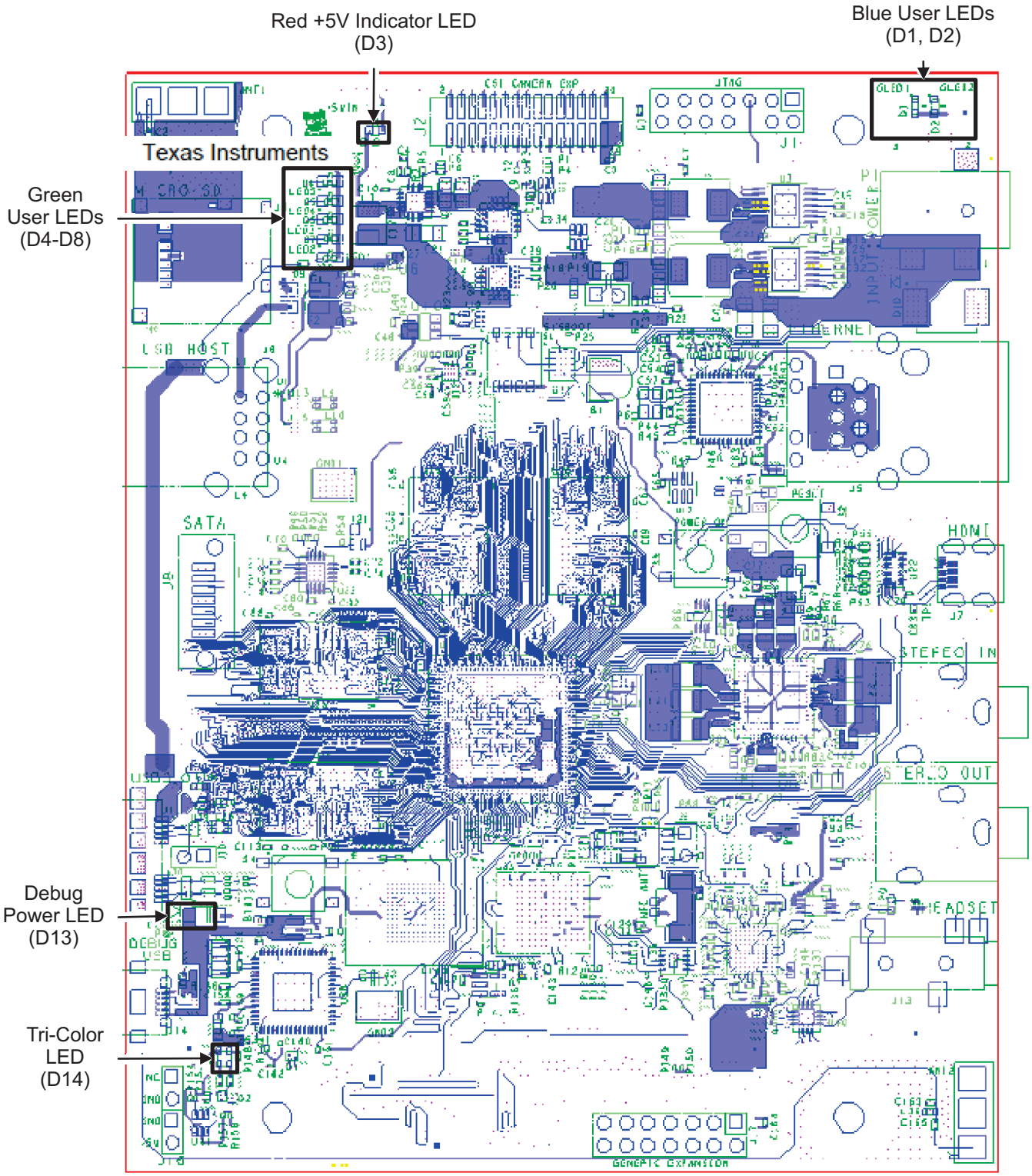


Figure 20. LED Locations

2.19 User Interface Features

Described below are the user features that are incorporated in the OMAP5432 EVM.

2.19.1 S2 - Push Button Switch

S2 is a momentary push-button switch that whose output is tied to the warm reset signal on the OMAP5432 EVM (H_SYS_NRESWARM on the schematic). Depressing this switch will initiate a warm reset of the OMAP5432 ES2.0 processor.

2.19.2 S3 – Push Button Switch

S3 is a momentary push-button switch that may be depressed to initiate a power-on reset of the OMAP5432 EVM. The output of this switch is connected to the PWRON input of the TWL6037 Power Companion IC. Depressing this button causes the TWL6037 to initiate its power-up sequence. In addition, depressing and holding this button for 12 seconds will cause the TWL6037 to power off.

2.19.3 S4 - Push Button Switch

S4 is a momentary push-button switch that whose output is tied to GPIO3_83 on the OMAP5432 EVM. Depressing this switch will momentarily ground GPIO3_83. For proper operation of this switch, the internal pull on this signal must be enabled, and it must be set to a pull-up NOT a pull-down.

2.20 I²C Device Mapping

The OMAP5432 EVM contains five different I²C busses that are provided by the OMAP5432 ES2.0 (I²C1, I²C2, I²C3, I²C4, and I²C5). The paragraphs below detail the seven bit I²C addresses for each device on the different I²C busses. The write and read addresses are derived by adding a '0' or '1' respectively, to the LSB of the address given below. (NOTE: for I²C5, the Host Port Bridge listed has resistor options to connect to the I²C5 bus, but is not connected in the default configuration).

2.20.1 OMAP I²C1

Table 12. OMAP I²C1 Device Addresses

Device	Function	I2C Address
TWL6037	Power COmpanion IC	0x48, 0x49, 0x4A
TWL6040	Phoenix Audio IC	0x4B
AT24C02C-MAHM	Board ID EEPROM	0x50

2.20.2 OMAP I²C2

Table 13. OMAP I²C2 Device Addresses

Device	Function	I2C Address
Main Expansion Connector (J20)	External LCD Control (e.g. touchscreen or backlight)	TBD
Generic Expansion Connector (J17)	Expansion Usage	TBD
Parallel/Dual-CSI Camera Expansion Connector (J18)	Camera Module I/F	TBD

2.20.3 OMAP I²C3

Table 14. OMAP I²C3 Device Addresses

Device	Function	I2C Address
Single CSI (Legacy) Camera Expansion Connector (J2)	Camera Module I/F	TBD
Parallel/Dual-CSI Camera Expansion Connector (J18)	Camera Module I/F	TBD

2.20.4 OMAP I²C4

Table 15. OMAP I²C4 Device Addresses

Device	Function	I2C Address
Main Expansion Connector (J20)	Display or Audio Expansion	TBD

2.20.5 OMAP I²C5

Table 16. OMAP I²C5 Device Addresses

Device	Function	I2C Address
TCA6424A	GPIO Expander	0x22
USB3503A	USB Host Port Bridge IC	0x08

3 OMAP5432 EVM Software Interface

This chapter provides details of interest regarding the software interface of the OMAP5432 EVM implementation.

3.1 Readable Board Revision

The OMAP5432 EVM provides a five-bit board revision that may be read by Software to determine what board is being used. These board ID bits are provided by the I2C5 GPIO Expander as shown in Table 17 below. The Pxx labels are the port of the GPIO expander that the respective Board ID bit comes from.

Table 17. Board ID Read Values

Board ID(4:0)					Description
P13	P12	P11	P10	P07	
0	0	0	0	1	OMAP5432 EVMG/H-02-01-00 5432 ES2.0, TWL6037 ES2.1, WL1857 ES2.1, 4GB EMMC
0	0	0	1	1	OMAP5432 EVMG/H-02-02-00 5432 ES2.0, TWL6037 ES2.1, No WL1857, 4GB EMMC
0	0	1	0	1	OMAP5432 EVMG/H-02-11-00 5432 ES2.0, TWL6037 ES2.2, WL1857 ES2.1, 4GB EMMC
0	0	1	1	1	OMAP5432 EVMG/H-02-12-00 5432 ES2.0, TWL6037 ES2.2, No WL1857, 4GB EMMC
X	X	X	X	X	Reserved for future use
X	X	X	X	X	Reserved for future use

3.2 Pin Multiplexing

3.2.1 Platform Pin Multiplexing

See Table 18 for a listing of the OMAP pin multiplexing required for the OMAP5432 processor on the OMAP5432 EVM. This table only includes the GPIOs that are connected and required for operation of the as-shipped configuration of the OMAP5432 EVM. Unused pins are not included here as well as any GPIOs that go to the onboard connectors

Table 18. OMAP5432 ES2.0 Pin Multiplexing

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of OMAP5432 EVM Usage
GPIO Bank 1				
WKOUT0	U31	5	----	Debug/HW Visibility (hw_wkdbg1)

Table 18. OMAP5432 ES2.0 Pin Multiplexing (continued)

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of OMAP5432 EVM Usage
WKOUT1	U32	5	----	Debug/HW Visibility (hw_wkdbg2)
WKOUT2	U33	5	----	Debug/HW Visibility (hw_wkdbg3)
WKOUT3	V31	5	----	Debug/HW Visibility (hw_wkdbg4)
WKOUT4	V32	6/5	GPIO1_WKOUT4	Blue User LED (D2) & Debug/HW Visibility (hw_wkdbg4)
WK6	K32	0/5	DRM_EMU0	EMU0 or Debug/HW Visibility (hw_wkdbg6)
WK7	K31	0/5	DRM_EMU1	EMU1 or Debug/HW Visibility (hw_wkdbg7)
WK11	P31	0	FREF_CLK1_OUT	USB Host Port Bridge Clock
WK12	M31	0	FREF_CLK0_OUT	Camera Module Clock In
WK13	N31	6	GPIO1_WK13	Camera Module GPIO
WK14	N28	6	GPIO1_WK14	WLAN Interrupt In
WK15	N29	5	GPIO1_WK15	Debug/HW Visibility (hw_wkdbg13)
GPIO Bank 2				
32	P32	4	GPMC_NCS0	GPMC Chip Select 0
33	E25	4	GPMC_nADV_ALE	GPMC Address Valid/Address Latch Enable
34	F25	4	GPMC_nBE0_CLE	GPMC Byte Enable 0/Comm. Latch Enable
35	J29	4	GPMC_nWP	GPMC Write Protect
36	J28	4	GPMC_CLK	GPMC Clock
37	J27	4	GPMC_AD0	GPMC Address/Data Bit 0
38	H28	4	GPMC_AD1	GPMC Address/Data Bit 1
39	H29	4	GPMC_AD2	GPMC Address/Data Bit 2
40	G29	4	GPMC_AD3	GPMC Address/Data Bit 3
41	E29	4	GPMC_AD4	GPMC Address/Data Bit 4
42	E27	4	GPMC_AD5	GPMC Address/Data Bit 5
43	F26	4	GPMC_AD6	GPMC Address/Data Bit 6
44	E26	4	GPMC_AD7	GPMC Address/Data Bit 7
45	N27	4	GPMC_WAIT0	GPMC Wait Input
46	AJ10	0	EMMC_CLK	EMMC Clock
47	AH10	0	EMMC_CMD	EMMC Command
48	AG10	0	EMMC_DATA0	EMMC Data Bit 0
49	AF10	0	EMMC_DATA1	EMMC Data Bit 1
50	AH9	0	EMMC_DATA2	EMMC Data Bit 2
51	AJ9	0	EMMC_DATA3	EMMC Data Bit 3
52	AG9	0	EMMC_DATA4	EMMC Data Bit 4
53	AJ8	0	EMMC_DATA5	EMMC Data Bit 5
54	AH8	0	EMMC_DATA6	EMMC Data Bit 6
55	AJ7	0	EMMC_DATA7	EMMC Data Bit 7
56	J32	4	GPMC_AD8	GPMC Address/Data Bit 8
57	J33	4	GPMC_AD9	GPMC Address/Data Bit 9
58	H32	4	GPMC_AD10	GPMC Address/Data Bit 10
59	J31	4	GPMC_AD11	GPMC Address/Data Bit 11
60	G31	4	GPMC_AD12	GPMC Address/Data Bit 12
61	H31	4	GPMC_AD13	GPMC Address/Data Bit 13
62	G32	4	GPMC_AD14	GPMC Address/Data Bit 14
63	G33	4	GPMC_AD15	GPMC Address/Data Bit 15
GPIO Bank 3				
76	G20	6	GPIO3_76	Interrupt from GPIO Expander
77	F20	4	GPMC_NCS1	GPMC Chip Select 1

Table 18. OMAP5432 ES2.0 Pin Multiplexing (continued)

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of OMAP5432 EVM Usage
78	F17	4	GPMC_A24	GPMC Address Bit 24
79	E20	6	GPIO3_79	Ethernet Reset
80	E14	6	GPIO3_80	USB Host Reset
81	F14	6	GPIO3_81	Display Port Interrupt In
82	G14	6	GPIO3_82	DSI Expansion GPIO (LCD Reset)
83	E17	6	GPIO3_83	Pushbutton Input/DSI Expansion GPIO
84	F13	4	GPMC_NWE	GPMC Write Enable
85	N9	4	GPMC_NOE_NRE	GPMC Output Enable
86	G13	0	UART2_RX	UART2 Receive Data or GPMC_NCS5
87	E13	0	UART2_TX	UART2 Transmit Data or GPMC_NCS6
94	K28	0	USBB2_HSIC_STROBE	USB HS Interchip Strobe (USB Host)
95	K29	0	USBB2_HSIC_DATA	USB High-Speed Interchip Data (USB Host)
GPIO Bank 4				
96	W32	0	ABE_CLKS	Audio Back End Reference Clock
97	AF28	4	ABEMCBSP3_FSX	MCBSP3 Frame Sync (to exp. conn)
98	AE29	4	ABEMCBSP3_DX	MCBSP3 Transmit Data (to exp. conn)
99	AE28	4	ABEMCBSP3_DR	MCBSP3 Receive Data (from exp. conn)
100	AE27	4	ABEMCBSP3_CLK	MCBSP3 Clock (to exp. conn)
101	AD29	1	ABEMCBSP1_FSX	MCBSP1 Frame Sync (to WL1857 – BT)
102	AD28	1	ABEMCBSP1_DX	MCBSP1 Transmit Data (to WL1857 – BT)
103	AF29	1	ABEMCBSP1_CLKX	MCBSP1 Clock (to WL1857 – BT)
104	AG29	1	ABEMCBSP1_DR	MCBSP1 Receive Data (from WL1857 – BT)
105	AD26	0	ABEMCBSP2_DR	MCBSP2 Receive Data (from WL1857 – FM)
106	AD27	0	ABEMCBSP2_DX	MCBSP2 Transmit Data (to WL1857 – FM)
107	AA26	0	ABEMCBSP2_FSX	MCBSP2 Frame Sync (to WL1857 – FM)
108	AA27	0	ABEMCBSP2_CLK	MCBSP2 Clock (to WL1857 – FM)
109	AA28	0	ABEMCPDM_UL_DATA	MCPDM Upload Data (from TWL6040)
110	AA29	0	ABEMCPDM_DL_DATA	MCPDM Download Data (to TWL6040)
111	Y29	0	ABEMCPDM_FRAME	MCPDM Frame Sync (to TWL6040)
112	Y28	0	ABEMCPDM_LB_CLK	MCPDM Loopback Clock (to TWL6040)
113	G24	4	GPMC_A16	GPMC Address Bit 16
114	H24	4	GPMC_A17	GPMC Address Bit 17
115	E24	4	GPMC_A18	GPMC Address Bit 18
116	F24	4	GPMC_A19	GPMC Address Bit 19
117	G21	4	GPMC_A20	GPMC Address Bit 20
118	H21	4	GPMC_A21	GPMC Address Bit 21
119	E21	4	GPMC_A22	GPMC Address Bit 22
120	F21	4	GPMC_A23	GPMC Address Bit 23
GPIO Bank 5				
128	AH25	0	WLSDIO_CLK	WLAN SDIO Clock (to WL1857)
129	AG25	0	WLSDIO_CMD	WLAN SDIO Command (to WL1857)
130	AJ26	0	WLSDIO_DATA0	WLAN SDIO Data Bit 0 (to WL1857)
131	AH26	0	WLSDIO_DATA1	WLAN SDIO Data Bit 1 (to WL1857)
132	AK28	0	WLSDIO_DATA2	WLAN SDIO Data Bit 2 (to WL1857)
133	AJ27	0	WLSDIO_DATA3	WLAN SDIO Data Bit 3 (to WL1857)
134	AL32	0	UART5_RX	BT HCI Receive Data
135	AL31	0	UART5_TX	BT HCI Transmit Data

Table 18. OMAP5432 ES2.0 Pin Multiplexing (continued)

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of OMAP5432 EVM Usage
136	AK31	0	UART5_CTS	BT HCI Clear to Send
137	AK32	0	UART5_RTS	BT HCI Request to Send
138	AL33	0	I2C2_SCL	I2C2 Serial Clock
139	AM32	0	I2C2_SDA	I2C2 Serial Data
140	AM30	6	GPIO5_140	WLAN Enable
141	AL30	6	GPIO5_141	Audio Power On (to TWL6040)
142	AL29	6	GPIO5_142	Bluetooth Enable
143	AN31	6	GPIO5_143	Bluetooth Wakeup
144	AM31	6	GPIO5_144	WL1857 Host Wakeup
147	AL28	0	I2C5_SCL	I2C5 Serial Clock
148	AM29	0	I2C5_SDA	I2C5 Serial Data
152	AN29	6	GPIO5_152	SD Card Detect
153	AJ25	6	GPIO5_153	Blue User LED (D1)
154	AJ24	6	GPIO5_154	Camera Module GPIO
155	AG24	0	UART3_TX_IRTX	UART3 Transmit Data
156	AH24	0	UART3_RX_IRRX	UART3 Receive Data
158	K26	0	USBB3_HSIC_STROBE	USB HS Interchip Strobe (USB Host)
159	K27	0	USBB3_HSIC_DATA	USB High-Speed Interchip Data (USB Host)
GPIO Bank 6				
160	AN13	3	DISPC_DATA17	Parallel Display Data Bit 17
161	AM13	3	DISPC_DATA16	Parallel Display Data Bit 16
162	AL12	3	DISPC_VSYNC	Parallel Display Vertical Sync
163	AL13	3	DISPC_HSYNC	Parallel Display Horizontal Sync
164	AL18	3	DISPC_PCLK	Parallel Display Pixel Clock
165	AM18	3	DISPC_DE	Parallel Display Data Enable
166	AL17	3	DISPC_DATA0	Parallel Display Data Bit 0
167	AM17	3	DISPC_DATA1	Parallel Display Data Bit 1
168	AN17	3	DISPC_DATA2	Parallel Display Data Bit 2
169	AL16	3	DISPC_DATA3	Parallel Display Data Bit 3
170	AM16	3	DISPC_DATA4	Parallel Display Data Bit 4
171	AL15	3	DISPC_DATA5	Parallel Display Data Bit 5
172	AM15	3	DISPC_DATA6	Parallel Display Data Bit 6
173	AN15	3	DISPC_DATA7	Parallel Display Data Bit 7
174	AL14	3	DISPC_DATA8	Parallel Display Data Bit 8
175	AM14	3	DISPC_DATA9	Parallel Display Data Bit 9
176	AM12	3	DISPC_DATA10	Parallel Display Data Bit 10
177	AL11	3	DISPC_DATA11	Parallel Display Data Bit 11
178	AM11	3	DISPC_DATA12	Parallel Display Data Bit 12
179	AN11	3	DISPC_DATA13	Parallel Display Data Bit 13
180	AL10	3	DISPC_DATA14	Parallel Display Data Bit 14
181	AM10	3	DISPC_DATA15	Parallel Display Data Bit 15
182	AN9	3	DISPC_DATA18	Parallel Display Data Bit 18
183	AM9	3	DISPC_DATA19	Parallel Display Data Bit 19
184	AL9	3	DISPC_DATA20	Parallel Display Data Bit 20
185	AM8	3	DISPC_DATA21	Parallel Display Data Bit 21
186	AL8	3	DISPC_DATA22	Parallel Display Data Bit 22
187	AN7	3	DISPC_DATA23	Parallel Display Data Bit 23

Table 18. OMAP5432 ES2.0 Pin Multiplexing (continued)

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of OMAP5432 EVM Usage
188	W31	0	TIMER10_PWM_EVT	Display Backlight PWM
189	W33	0	DSIPORTA_TE0	DSI Port “A” Tearing Effect Control
190	AJ33	0	TIMER9_PWM_EVT	Display Backlight PWM
191	AK30	0	DSIPORTC_TE0	DSI Port “C” Tearing Effect Control
GPIO Bank 7				
192	AN23	0	HDMI_CEC	HDMI Consumer Electronics Control
193	AM23	0	HDMI_HPD	HDMI Hot Plug Detect
194	AM22	0	HDMI_DDC_SCL	HDMI EDID Serial Clock
195	AL23	0	HDMI_DDC_SDA	HDMI EDID Serial Data
196	AF20	0	MCSPI2_CS0	SPI2 Chip Select
197	AH17	0	MCS9I2_CLK	SPI2 Clock
198	AG20	0	MCS9I2_SIMO	SPI2 Data (Slave In, Master Out)
199	AH20	0	MCS9I2_SOMI	SPI2 Data (Slave Out, Master In)
200	AJ21	0	I2C4_SCL	I2C4 Serial Clock
201	AJ20	0	I2C4_SDA	I2C4 Serial Data
GPIO Bank 8				
224	AE6	0	CAM_SHUTTER	Camera Shutter Control
225	AE5	0	CAM_STROBE	Camera Strobe
226	AF6	0	CAM_RESET	Camera Reset
227	AE7	6	GPIO8_227	Camera Module GPIO (TBD)
228	AD5	6	GPIO8_228	Camera Module GPIO (TBD)
229	AD6	6	GPIO8_229	Camera Module GPIO (TBD)
230	AD7	6	GPIO8_230	GPIO or DSI Display Expansion PWM
231	AJ5	0	I2C3_SCL	I2C3 Serial Clock
232	AH4	0	I2C3_SDA	I2C3 Serial Data
233	AG5	6	GPIO8_233	GPIO or parallel camera HSYNC
234	AF5	1	SYS_DRM_MSECURE	System DRAM Secure (to TWL6037)
IN236	U6	0/3	CSIPORTA_LANE0X	CSIA Data Lane 0X (or CPI_PCLK)
IN237	U5	0/3	CSIPORTA_LANE0Y	CSIA Data Lane 0Y (or CPI_WEN)
IN238	P5	0/3	CSIPORTA_LANE1Y	CSIA Data Lane 1Y (or CPI_DATA0)
IN239	P6	0/3	CSIPORTA_LANE1X	CSIA Data Lane 1X (or CPI_DATA1)
IN240	P8	0/3	CSIPORTA_LANE2Y	CSIA Data Lane 2Y (or CPI_DATA2)
IN241	P7	0/3	CSIPORTA_LANE2X	CSIA Data Lane 2X (or CPI_DATA3)
IN242	N5	0/3	CSIPORTA_LANE3X	CSIA Data Lane 3X (or CPI_DATA4)
IN243	N6	0/3	CSIPORTA_LANE3Y	CSIA Data Lane 3Y (or CPI_DATA5)
IN244	N7	0/3	CSIPORTA_LANE4X	CSIA Data Lane 4X (or CPI_DATA6)
IN245	N8	0/3	CSIPORTA_LANE4Y	CSIA Data Lane 4Y (or CPI_DATA7)
IN246	Y6	0/4	CSIPORTB_LANE0X	CSIB Data Lane 0X (or CPI_DATA12)
IN247	Y5	0/4	CSIPORTB_LANE0Y	CSIB Data Lane 0Y (or CPI_DATA13)
IN248	Y7	0/4	CSIPORTB_LANE1Y	CSIB Data Lane 1Y (or CPI_DATA14)
IN249	Y8	0/4	CSIPORTB_LANE1X	CSIB Data Lane 1X (or CPI_DATA15)
IN250	AA6	0/4	CSIPORTB_LANE2X	CSIB Data Lane 2X (or CPI_VSYNCIN)
IN251	AA5	0/4	CSIPORTB_LANE2Y	CSIB Data Lane 2Y (or CPI_HSYNCIN)
IN252	J6	0/3	CSIPORTB_LANE0Y	CSIC Data Lane 0Y (or CPI_DATA8)
IN253	J7	0/3	CSIPORTB_LANE0X	CSIC Data Lane 0X (or CPI_DATA9)
IN254	K6	0/3	CSIPORTB_LANE1Y	CSIC Data Lane 1Y (or CPI_DATA10)
IN255	K5	0/3	CSIPORTB_LANE1X	CSIC Data Lane 1X (or CPI_DATA11)

3.2.2 Camera Expansion Connector Pin Multiplexing

See Table 19 for a description of the pin multiplexing for the camera expansion board signals at connector J20. This connector may support either a parallel camera module or a dual-CSI camera module. The info shown in red is for the parallel camera module configuration. (NOTE: if H_GPIO_234 is required for the parallel camera module, the PCB will have to be reworked to remove R301 and add R300 and R302).

Table 19. Camera Expansion Connector (J20) Pin Multiplexing Options

J20 Pin #	OMAP Ball #	Mux Mode	Signal Name	Description of OMAP5432 EVM Usage
3	M31	0	h_FREFCLK_0	Input Clock
4	AD6	6	h_GPIO8_229	GPIO
5	AJ24	6	h_GPIO5_154	GPIO
6	AD5	6	h_GPIO8_228	GPIO
7	AH4	0	h_I2C3_SDA	I2C3 Serial Data
8	AE5	0	h_CAM_STROBE/ GPIO8_225	Camera Strobe
9	AJ5	0	h_I2C3_SCL	I2C3 Serial Clock
10	AE6	0	h_CAM_SHUTTER/ GPIO8_224	Camera Shutter Control
12	AF6	0	h_CAM_RESET/ GPIO8_226	Camera Global Reset
13	P8	0/3	h_CSIPORTA_LANE2Y	CSI-2A Lane 2Y/Parallel Cam Data bit 2
14	AE7	6	h_GPIO8_227	GPIO
15	P7	0/3	h_CSIPORTA_LANE2X	CSI-2A Lane 2X/Parallel Cam Data bit 3
16	N31	6	GPIO_WK13	GPIO
19	P5	0/3	h_CSIPORTA_LANE1Y	CSI-2A Lane 1Y/Parallel Cam Data bit 0
20	N8	0/3	h_CSIPORTA_LANE4Y	CSI-2A Lane 4Y/Parallel Cam Data bit 7
21	P6	0/3	h_CSIPORTA_LANE1X	CSI-2A Lane 1X/Parallel Cam Data bit 1
22	N7	0/3	h_CSIPORTA_LANE4X	CSI-2A Lane 4X/Parallel Cam Data bit 6
25	U5	0/3	h_CSIPORTA_LANE0Y	CSI-2A Lane 0Y/Parallel Cam Write Enable
26	N6	0/3	h_CSIPORTA_LANE3Y	CSI-2A Lane 3Y/Parallel Cam Data bit 5
27	U6	0/3	h_CSIPORTA_LANE0X	CSI-2A Lane 0X/Parallel Cam Pixel Clock
28	N5	0/3	h_CSIPORTA_LANE3X	CSI-2A Lane 3X/Parallel Cam Data bit 4
31	J7	0/3	h_CPI_DATA9	CSI-2C Lane 0X/Parallel Cam Data bit 9
32	Y8	0/4	h_CPI_DATA15	CSI-2B Lane 1X/Parallel Cam Data bit 15
33	J6	0/3	h_CPI_DATA8	CSI-2C Lane 0Y/Parallel Cam Data bit 8
34	Y7	0/4	h_CPI_DATA14	CSI-2B Lane 1Y/Parallel Cam Data bit 14
36	AM32	0	h_I2C2_SDA	I2C2 Serial Data
37	K6	0/3	h_CPI_DATA10	CSI-2C Lane 0Y/Parallel Cam Data bit 10
38	Y5	0/4	h_CPI_DATA13	CSI-2B Lane 0Y/Parallel Cam Data bit 13
39	K5	0/3	h_CPI_DATA11	CSI-2C Lane 0X/Parallel Cam Data bit 11
40	Y6	0/4	h_CPI_DATA12	CSI-2B Lane 0X/Parallel Cam Data bit 12
42	AL33	0	h_I2C2_SCL	I2C2 Serial Clock
43	AG5	6/3	h_GPIO8_233	GPIO/Parallel Cam Vertical Sync
44	AA5	0/4	h_GPIO8_IN250	CSI-2B Lane 2Y/Parallel Cam Horiz Sync In
45	AF5	6/3	h_GPIO8_234	GPIO/Parallel Cam Horizontal Sync
46	AA6	0/4	h_GPIO8_IN251	CSI-2B Lane 2X/Parallel Cam Vert. Sync In

3.3 OMAP5432 EVM Key Components

See Table 20 for a listing of the manufacturers and manufacturer part numbers for some of the key components used on the OMAP5432 EVM.

Table 20. Key H/W Components

Device / Interface	Under NDA?	Manufacturer P/N
Application Processor		
Processor	Yes	TI OMAP5432 ES2.0
Memories/Storage		
DDR3	Yes	Micron MT41K256M16HA-125:E
eMMC	No	Sandisk SDIN7DP2-4G
Micro-SD Card Cage (Push-Push)	No	Molex 502570-0893
Removable card ESD protection	No	Texas Instruments TPD6E001RSER
SATA Redriver (U23)	No	Texas Instruments SN75LVCP412RTJR
Vertical SATA connector	No	Molex 67800-5002
Power		
Power Management (U26)	Yes	Texas Instruments TWL6037
DC Input Connector (P1)	No	CUI, Inc. PJ-002AH-SMT
Switching Power Supply (U2)	No	Texas Instruments TPS54320RHL
Switching Power Supply (U3, U7)	No	Texas Instruments TPS54426PWPR
Load Switches (U4, U8)	No	Texas Instruments TPS2590RSA
Video/Display		
HDMI Transceiver + ESD protection	No	Texas Instruments TPD12S016RKTR
HDMI Connector (Type D)	No	Amphenol HDM-D-F191-10-2-2-TR
Expansion Interfaces		
100-pin SMT Expansion Connector (DSI & Parallel Display I/F, GPMC)	No	Hirose FX6-100P-0.8SV91
20-pin SMT Expansion Connector (GPMC)	No	Hirose FX6-20P-0.8SV91
14-pin through-hole Expansion Connector (Misc.)	No	EDAC 151-014-420-112
MCS		
WL1857 Module	No	TDK R078B
Audio		
Audio Codec	Yes	Texas Instruments TWL6040
3.5mm Audio Headset Jack	No	CUI Inc. SJ-43516-SMT
3.5mm Audio Line In/Out Jacks (P3 & P4)	No	CUI, Inc. SJ1-3513
Audio Headset Switch (U34)	No	Texas Instruments TS3A225ERTER
Ethernet		
Ethernet RJ-45 Connector w/ Integrated Magnetics	No	Pulse J1011F01PNL

Table 20. Key H/W Components (continued)

Device / Interface	Under NDA?	Manufacturer P/N
USB HSIC Phy	No	SMSC LAN9730-ABZJ
USB Host		
ESD Protection	No	Texas Instruments TPD2E001DRYR
USB HSIC Phy	No	SMSC USB3503A-1-GL-TR
Camera Expansion		
30-pin CSI-2 Camera Expansion Connector (top side)	No	Samtec TFM-115-32-S-D-A
50-pin dual CSI-2/Parallel Camera Expansion Connector (bottom side)	No	Samtec TFM-125-02-S-D-K

4 Test/Debug Information

This chapter contains information to allow easier debug access to signals on the OMAP5432 EVM.

4.1 Clock Signal Access

The following sections show where various clock signals on the OMAP5432 EVM may be accessed.

4.1.1 H_SYSCLK Probe Point

This signal is the clock from the OMAP5432 ES2.0 to the TWL6040 Audio Companion IC. It may be probed on the top side of the PCB at R86 or R87in the area at the lower right corner of the OMAP5432 device, as shown in Figure 21 below.

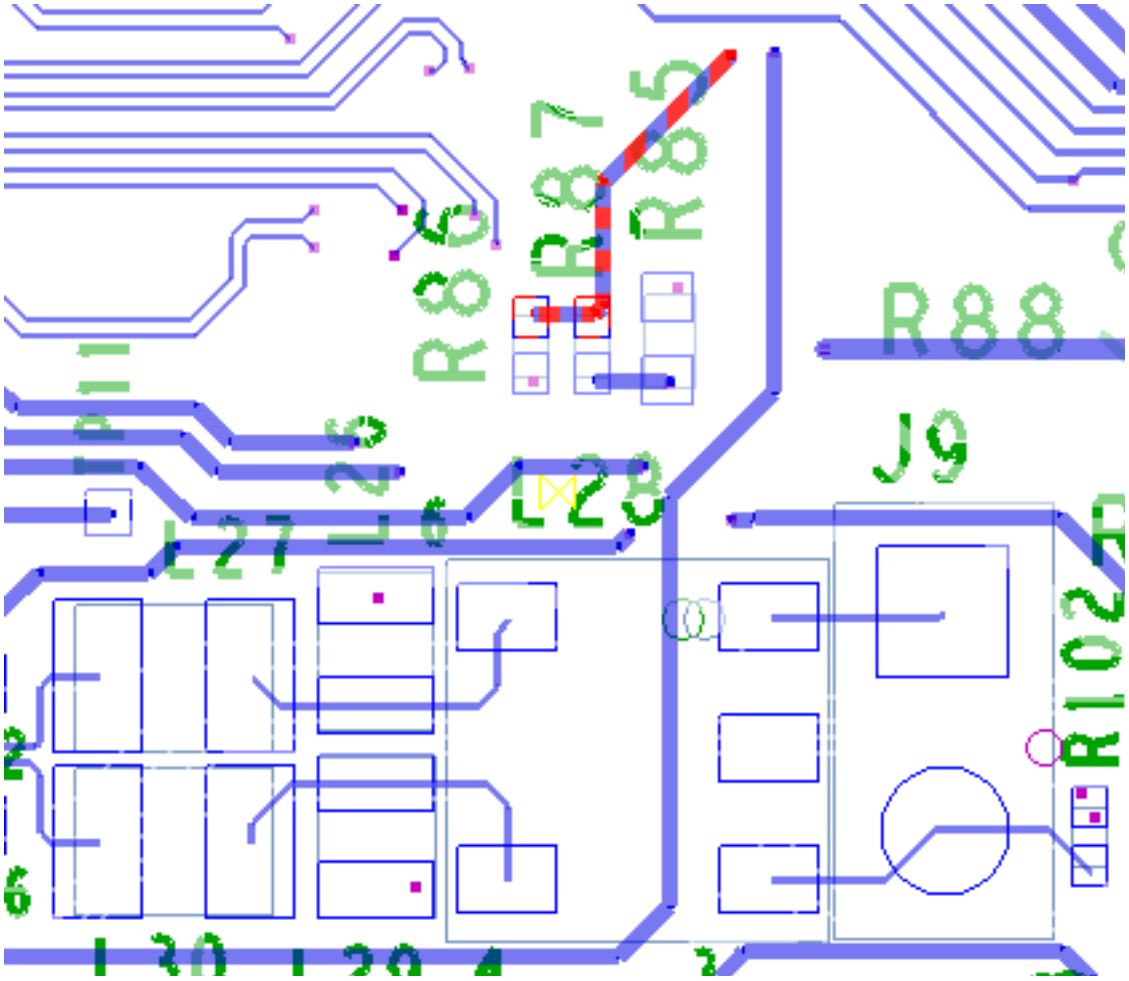


Figure 21. High-Speed Audio Clock Probe Point (h_SYSCLK)

4.1.2 USB Host Reference Clock Probe Point (H_FREFCLK_1)

The 19.2 MHz reference input clock to the USBB2 Phy device (USB3503A-1-GL-TR) may be probed on the top side of the PCB at TP3 as shown in Figure 22.

Figure 22. USB Phy Ref Clock Probe Point (H_FREFCLK_1)

4.1.3 Camera Module Input Clock Probe Point (H_FREFCLK_0)

The clock to the camera module connectors may be probed on the top side of the PCB at R77-1 as shown below in Figure 23. The frequency of this clock will depend on the camera module being used.

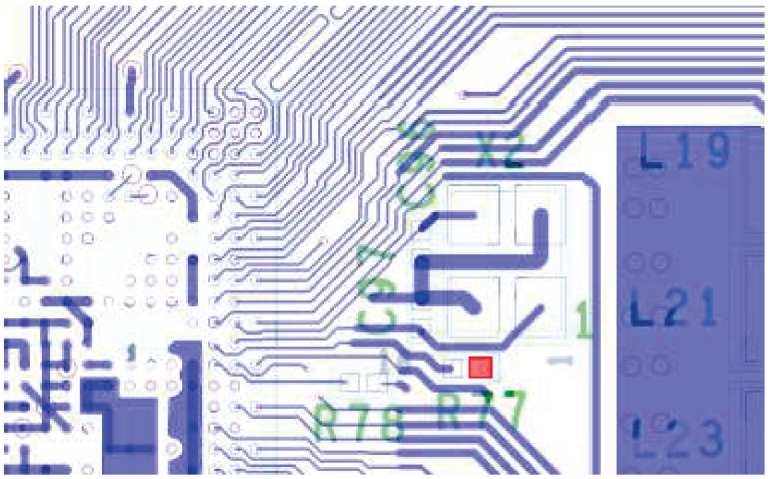


Figure 23. Camera Module Clock Probe Point (H_FREFCLK_0)

4.1.4 CLK32K_AUD Probe Point

The 32.768KHz input clock to the TWL6040 Audio Companion IC may be probed at R123-1 as shown in Figure 24. This testpoint may be located above the TWL6040 Audio Companion IC at U35.

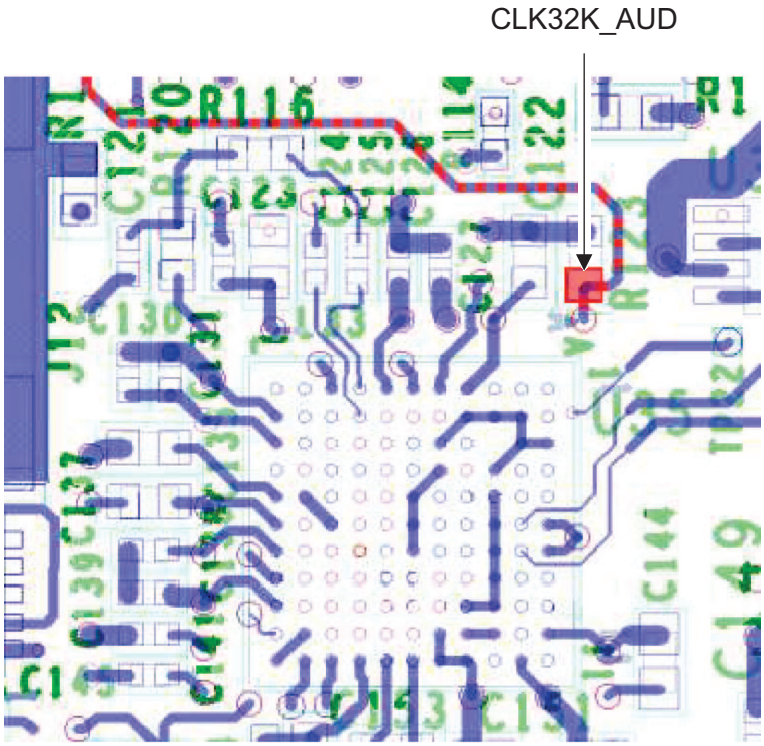


Figure 24. 32KHz Audio Clock Probe Point (CLK32K_PAUD)

4.2 Power Rail Signal Monitoring/Access

The OMAP5432 EVM provides the capability to perform current measurements on certain key PCB rails. See Table 21 for a description of the rails that are provisioned for measurement. on the input supplies to the VDD_OPP_MPU SMPS supplies (SMPS1:3), the VDD_OPP_MM SMPS supplies (SMPS4:5), and the VDD_OPP_CORE supply (SMPS8). Each of these has 30 mohm, 0.1W, 0.5% resistor on the VSYS input to the SMPS supplies. The voltage drop across each of these resistors may be measured at the testpoints on the back side of the PCB shown below in Figure 25. This voltage drop, divided by 0.03, will give the

Table 21. Power Management Capabilities

Resistor	TPs	Power Rail	DARA Conn. (J19)	Description
R205	TP28 TP27	VSYS_BRD (+) VSYS_COBRA (-)	33 35	Measurement of system supply current (all inputs into the TWL6037 Power companion IC)
R213	TP32 TP31	VSYS_COBRA (+) VSYS_MPU (-)	1 3	Measurement of the current into the TWL6037 MPU power supplies (SMPS1:3)
R211	TP30 TP34	VSYS_COBRA (+) VSYS_MM (-)	25 27	Measurement of the current into the TWL6037 multi-media power supplies (SMPS4:5)
R204	TP26 TP29	VSYS_COBRA (+) VSYS_CORE (-)	10 12	Measurement of the current into the TWL6037 core and 2.1V power supplies (SMPS8:9)
R19	N/A	VSYS_P (+) VSYS_BRD (-)	9 11	Measurement of total board current drawn from the main 3.7V supply
R203	N/A	VDDS_1V2_MAIN (+) VDDS_1V2_WKUP (-)	37 39	Measurement of total current drawn from the 1.2V wakeup rail (LDO6)
R234	N/A	VDDS_1V8_MAIN (+) VDDS_1V8_OMAP (-)	13 15	Measurement of total current drawn by OMAP only from the 1.8V VIO rail (SMPS7)
---		VDD_OPP_MPU	29/31	Measure voltage for the OMAP MPU rail(1)
---		VDD_OPP_MM	14/16	Measure voltage for the OMAP MM rail(1)

(1) The voltage is required to calculate the output current from the OMAP switcher, as the efficiency varies depending on the output voltage and current drawn.

Table 21. Power Management Capabilities (continued)

Resistor	TPs	Power Rail	DARA Conn. (J19)	Description
---		VDD_OPP_CORE	5/7	Measure voltage for the OMAP CORE rail(1)
R65	N/A	VDD_2V1 (+) VDDA_2V1_AUD (-)	17 19	Measurement of total current supplied to the Audio IC from the 2.1V rail (SMPS9)(2)
R61	N/A	VDD_DDR3_P (+) VDD_DDR3_N (-)	18 20	Measurement of output current supplied to the DDR3 devices/OMAP (SMPS6)
R220	N/A	VDDA_1V8_REF (+) VDDA_1V8_REF_O (-)	22 24	Measurement of output current from the OMAP low-noise LDO (LDOLN_OUT)

(2) Since the inputs to SMPS8 and 9 are shorted inside of the TWL6037 device, to get the CORE output current, you measure the inputs to SMPS8/9 through R204, and then subtract the current through the SMPS9 switcher (R65).

4.2.1 TWL6037 MPU/MM/Core Current Measurement Points

The OMAP5432 EVM provides current measurement resistors on the input supplies to the VDD_OPP_MPU SMPS supplies (SMPS1:3), the VDD_OPP_MM SMPS supplies (SMPS4:5), and the VDD_OPP_CORE supply (SMPS8). Each of these has 30 mohm, 0.1W, 0.5% resistors on the VSYS input to the SMPS supplies. The voltage drop, from positive to negative, may be measured across each of these resistors at the testpoints on the back side of the PCB shown below in Figure 25. This voltage drop, divided by 0.03, will give the current going into the SMPS, which along with the voltage seen by the SMPS, and the efficiency of the TWL6037 switch-mode power supply will allow the user to calculate the current being provided by the TWL6037 supply of interest.

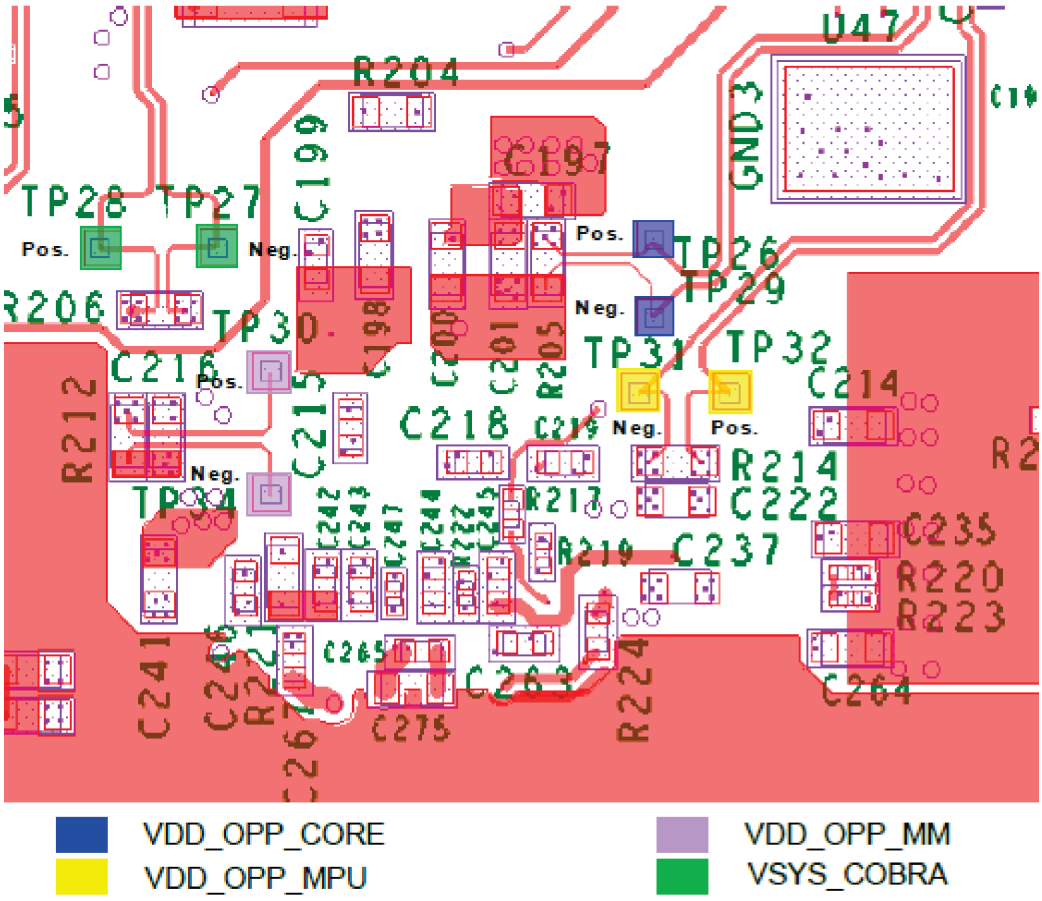


Figure 25. OMAP5432 ES2.0 Current Measurement Probe Points (Back Side of PCB)

4.2.2 TWL6037 VDD_DDR3L Current Measurement Points

The OMAP5432 EVM provides a four-terminal, 50-mohm power measurement resistor at R61 to measure the output current being provided by the DDR3 supply (SMPS6). This resistor may be found on the top of the PCB as shown in Figure 26 below.

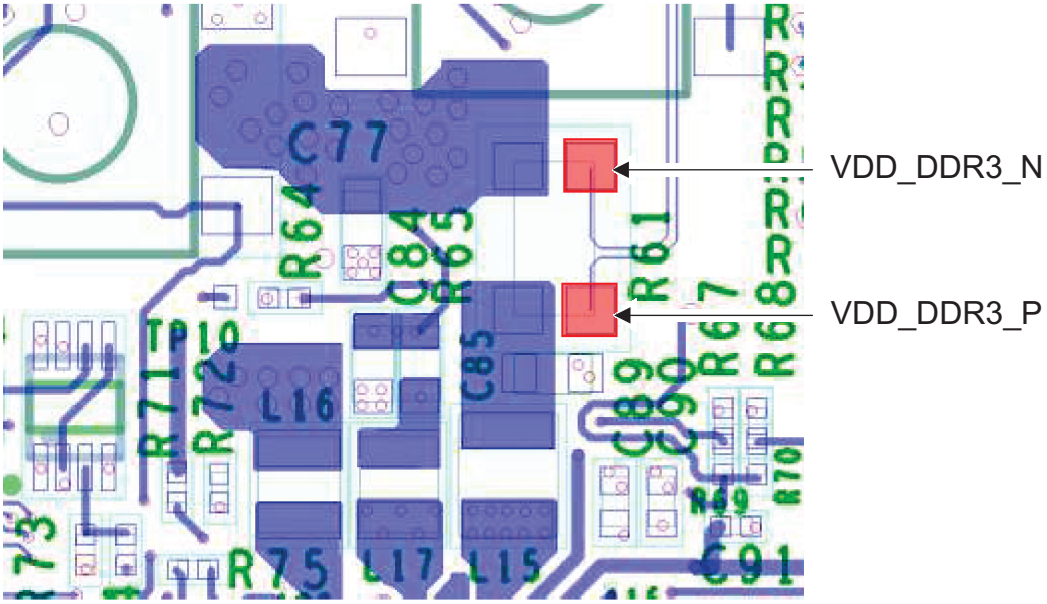


Figure 26. DDR3 Current Measurement Probe Points (Top Side of PCB)

4.2.3 TWL6037 SMPS Output Probe Points

The outputs of the TWL6037 SMPS output supplies may be probed around the TWL6037 IC at U25 as shown in Figure 27 below.

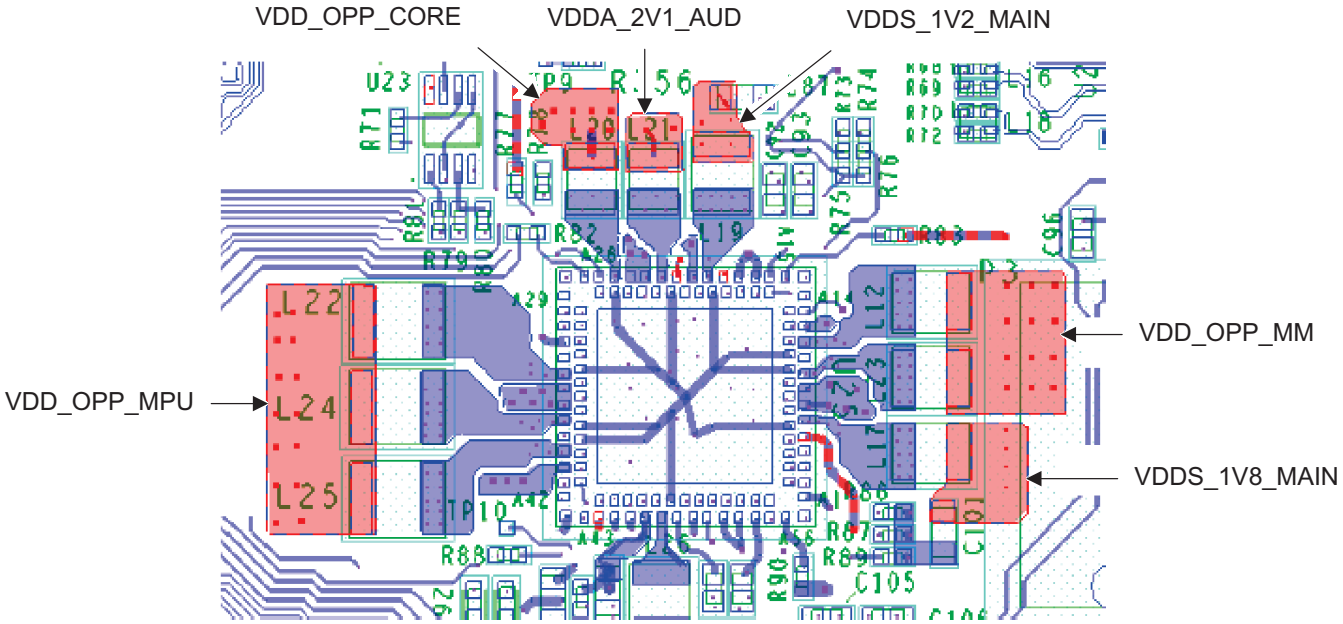


Figure 27. TWL6037 SMPS Output Probe Points

4.2.4 VCC_3v3_MAIN Output Probe Point

The output of the TPS54320 SMPS may be probed at locations U16-6, C62-2, R40-1, R43-1, C55-2, or C56-2. This is the power rail for the onboard circuitry requiring 3.3V.

4.3 OMAP5432 EVM Interface Signal Access

4.3.1 TWL6040 PDM Interface Probe Points

The PDM interface which is the digital audio interface between the OMAP5432 ES2.0 and the TWL6040 Audio Companion IC, may be probed at resistors above the TWL6040 IC at U35 as shown in Figure 28 below.

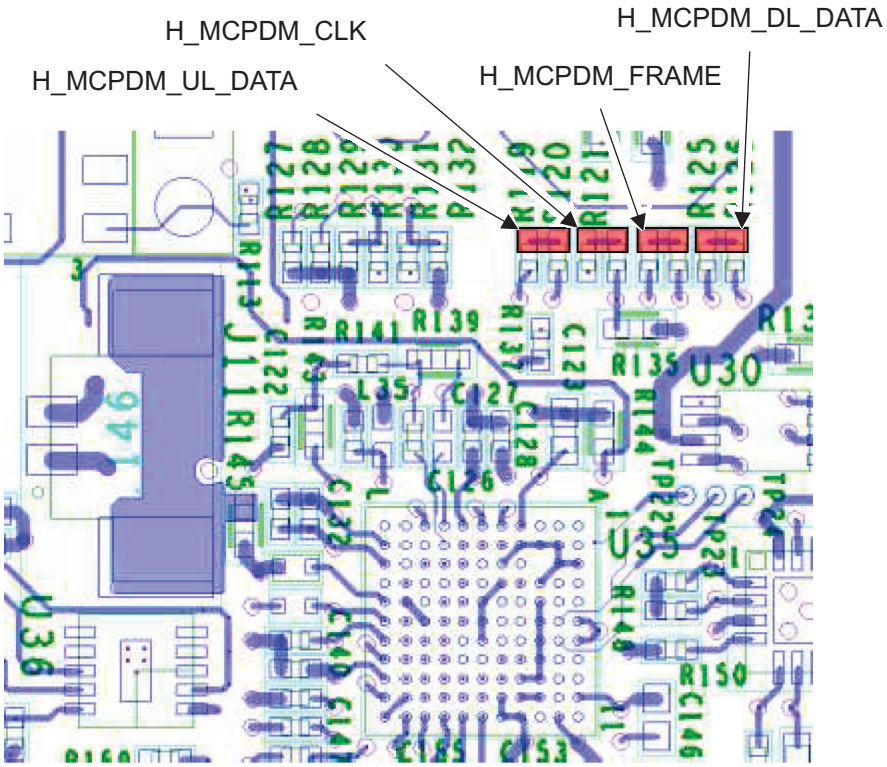


Figure 28. TWL6040 PDM Interface Probe Points

4.3.2 USBB2 HSIC Interface Probe Points

The USBB2 High-Speed Interchip USB lines which are used for the USB Host Port Hub interface may be probed at test points TP4 and TP6 on the top side of the PCB as shown in Figure 29 below.

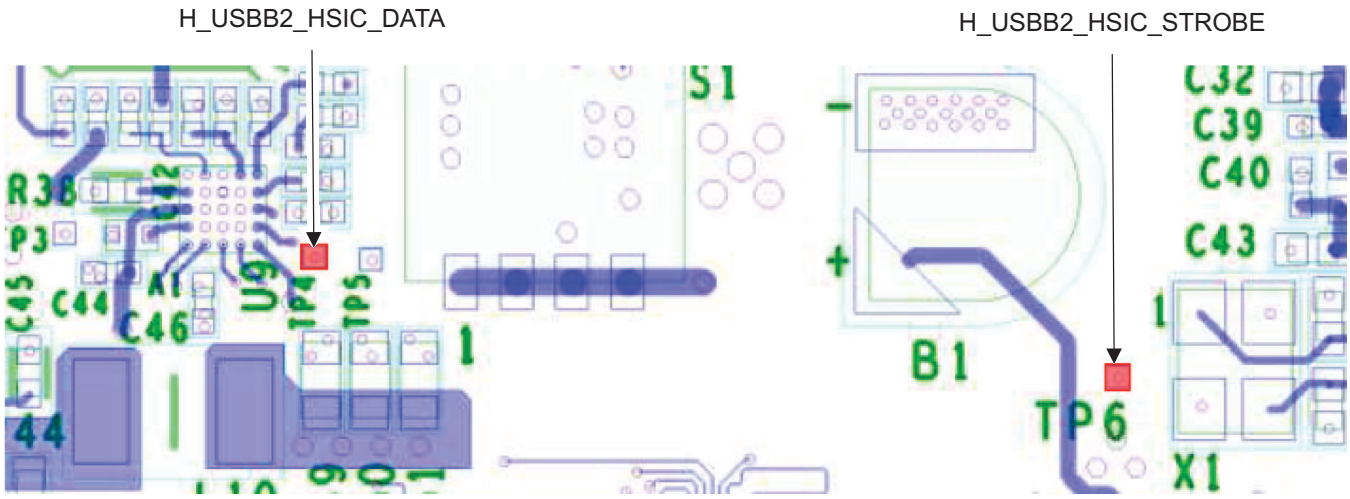


Figure 29. USBB2 HSIC Interface Probe Points

4.3.3 USBB3 HSIC Interface Probe Points

The USBB3 High-Speed Interchip USB lines which are used for the Ethernet Hub interface may be probed at test points TP1 and TP2 on the top side of the PCB as shown in Figure 30 below.

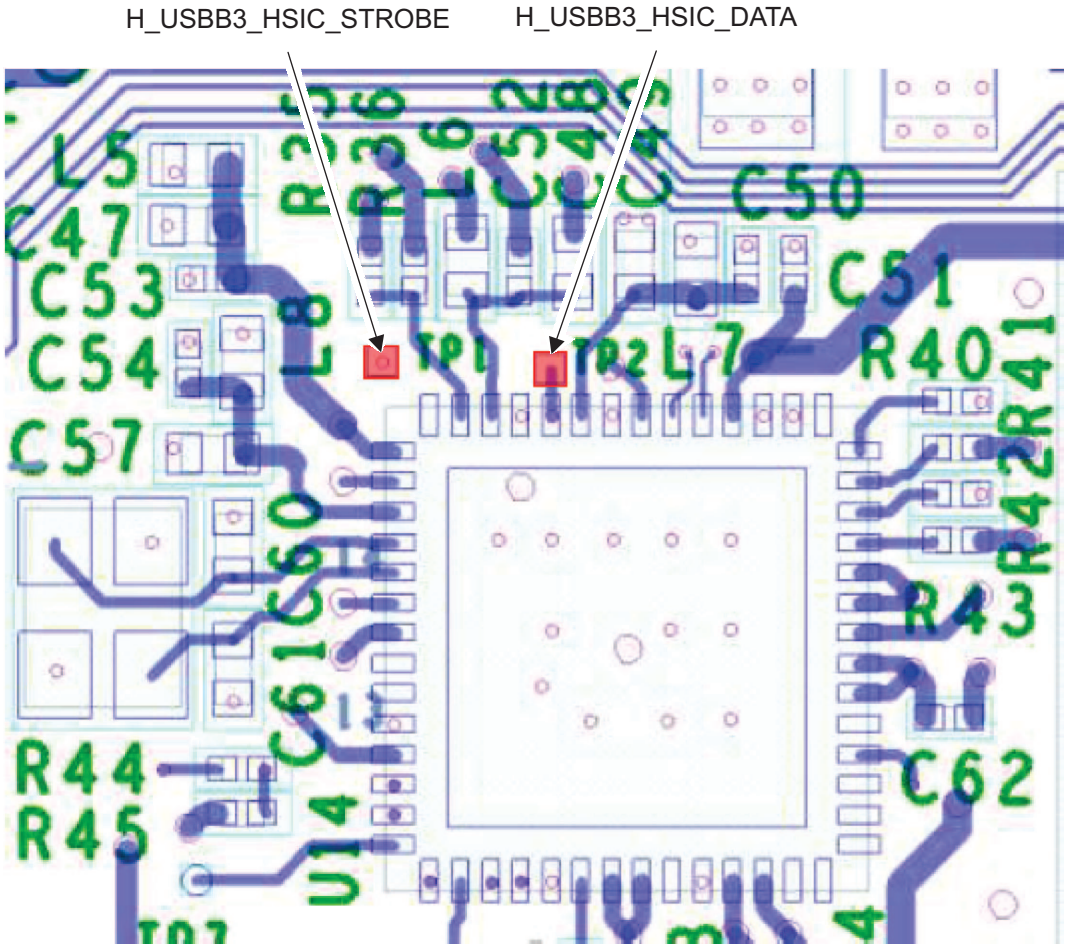


Figure 30. USBB3 HSIC Interface Probe Points

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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