OMAP™

OMAP4470 Multimedia Device
Engineering Samples ES1.0
Texas Instruments OMAP™ Family of Products

Data Manual Operating Condition Addendum
Version 1.0

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HISTORY

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Note:

1. Creation.

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1 INTRODUCTION

The aim of this document is to describe the operating conditions of the following OMAP4470 devices:

- OMAP4470-1500
- OMAP4470-1300

This document contains the description of each OPP (Operating Performance Point) for processors clocks and device core clocks.

NOTE

OPP50, OPP100, OPPTB, OPPNT and OPPNTSB may also be called OPP50, OPP100, OPP_TURBO, OPP_NITRO and OPP_NTSB in other OMAP documents.

Table 1-1 describes the supported vdd_mpu (V_{DD1}) operating performance point (OPP) for each OMAP4470 devices.

Table 1-1. OMAP4470 vdd_mpu (V_{DD1}) Operating Points(1)

OMAP4470 Devices	OPP50	OPP100	OPPTB	OPPNT	OPPNTSB
V_{DD1} (vdd_mpu)					
OMAP4470-1500 (MPU@1500MHz)	√	√	√	√	√
OMAP4470-1300 (MPU@1300MHz)	√	√	√	√	

(1) This table is specific to vdd_mpu (V_{DD1}) with AVS feature enabled.

Table 1-2 describes the supported vdd_iva (V_{DD2}) operating performance point (OPP) for each OMAP4470 devices.

Table 1-2. OMAP4470 vdd_iva (V_{DD2}) Operating Points(1)

OMAP4470 Devices	OPP50	OPP100	OPPTB	OPPNT	OPPNTSB
V_{DD2} (vdd_iva)					
OMAP4470-1500 (IVA@500MHz)	√	√	√	√	√
OMAP4470-1300 (IVA@430MHz)	√	√	√	√	

(1) This table is specific to vdd_iva (V_{DD2}) operating performance points with AVS feature enabled.

Table 1-3 describes two sets of supported vdd_core (V_{DD3}) operating performance point (OPP) for each OMAP4470 devices.

Table 1-3. OMAP4470 vdd_core (V_{DD3}) Operating Points(1)

OMAP4470 Devices	OPP50	OPP100	OPP119
V_{DD3} (vdd_core) – High Performances			
OMAP4470-1500 (SGX @384MHz, L3@233MHz)	√	√	√
OMAP4470-1300 (SGX @384MHz, L3@233MHz)	√	√	√
V_{DD3} (vdd_core) – Low Power			
OMAP4470-1500 (SGX @384MHz, L3@200MHz)	√	√	√
OMAP4470-1300 (SGX @384MHz, L3@200MHz)	√	√	√

(1) This table is specific to vdd_core (V_{DD3}) operating performance points with AVS feature enabled.

NOTE

OMAP ™ 4 processors are intended for manufacturers of smartphones and other mobile devices, as well as enterprise, industrial and consumer markets.

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1.5 About This Manual

Nominal, Minimum, Maximum Voltages Terminology

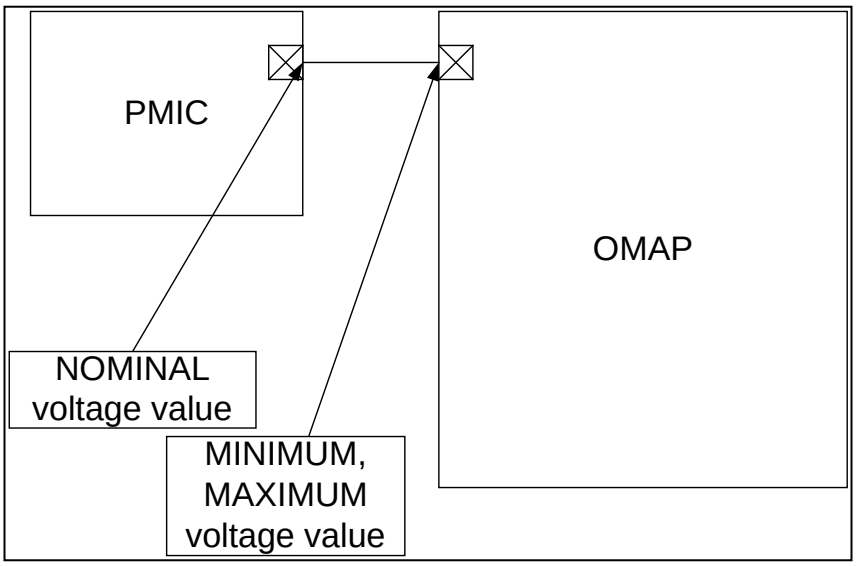

Figure 1-1. Nominal, Minimum, Maximum Voltages Terminology

The Figure 1-1 describes the location of the voltages specified in this manual.

- Board design must guaranty that the minimum pre-AVS voltage values documented in Table 2-1, Table 2-3, Table 2-5 (MPU, IVA, CORE - Initial Pre-AVS Voltages Settings) tables are met at the OMAP balls.
- The nominal voltage value documented in Table 2-1, Table 2-3, Table 2-5 tables is the recommended voltage to be applied at power IC (PMIC) level, taking into account board IR drop and PMIC tolerance.
- Maximum voltage value should not be exceeded at OMAP ball level to prevent accelerated aging of the device.

2 RECOMMENDED OPERATION

2.1 Micro Processor Unit (MPU) Clocks

CAUTION

For more information on nominal, minimum, maximum voltages location, see the Figure 1-1, *Nominal, Minimum, Maximum Voltages Terminology*.

Table 2-1 shows the recommended V_{DD1} (corresponding to vdd_mpu, MPU voltage) initial voltages settings with AVS class 1.5 enabled.

Table 2-1: MPU - Initial pre-AVS Voltages Settings (5)

	RETENTION (4)	OPPBOOT (4)			OPP50 (1)(6)			OPP100 (1)(6)			OPPTB (1)(3)			OPPNT (1)(3)			OPPNTSB (1)(3)		
	MIN	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
V_{DD1} (2)(5) (V)	0.750	0.890	0.937	0.984	0.999	1.037	1.066	1.140	1.200	1.260	1.247	1.312	1.378	1.306	1.375	1.444	1.306	1.387	1.444

(1) Enabling AVS feature is mandatory for these OPPs (OPP50, OPP100, OPPTB, OPPNT or OPPNTSB) to avoid impact on device reliability and lifetime POH (Power-On-Hours).
(2) These V_{DD1} (vdd_mpu) voltage ranges define the safe V_{DD1} (vdd_mpu) voltage ranges to be used before using AVS class 1.5 feature for OPPs calibration. The minimum voltage may be lower after calibration than this specification.
(3) ABB (adaptive body biasing polarization) feature must be enabled for OPPTB, OPPNT and OPPNTSB operating points following the ABB programming feature steps described in PRCM chapter of OMAP4470 TRM.
(4) Retention and OPPBOOT V_{DD1} (vdd_mpu) voltage ranges are defined with AVS feature disabled.
(5) Nominal voltage value documented in this table corresponds to the voltage to be applied at power IC (PMIC) level. Whereas minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(6) OPP50 or OPP100 can be used with AVS disabled for short periods of time (i.e. for ROM code or boot loader) as long as only one CPU is active. This is not applicable to OPPTB, OPPNT, OPPNTSB.

Table 2-2 describes the standard processors clocks speed characteristics vs V_{DD1} (corresponding to vdd_mpu, MPU voltage) with AVS class 1.5 enabled or disabled.

Table 2-2: MPU Clocks AC Performances (2)

		OPP50		OPP100		OPPTB		OPPNT		OPPNTSB	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**
DPLL_MPU Locked Frequency	-	1600	-	1600	-	1100	-	1300	-	1500	-
MPU_DPLL_CLK	DPLL_MPU Locked Frequency (CLKOUT_M2)	400	2 * (M2 = 2) (1)	800	2 * (M2 = 1) (1)	-	-	-	-	-	-
MPU_DPLL_CLK	DPLL_MPU Locked Frequency (CLKOUTX2_M3)	-	-	-	-	1100	(M3 = 1) (1)	1300	(M3 = 1) (1)	1500	(M3 = 1) (1)

(1) This ratio is configurable by software programming. For more information, see the Power, Reset, and Clock Management / Clock Manager Functional Description / Internal Clock Generation section of the OMAP4470 TRM.
(2) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

NOTE

The programmable divider for the asynchronous bridge to Audio Back-end (ABE) must be set to MPU_DPLL_CLK / 8 when MPU_DPLL_CLK clock frequency is above 800MHz.
It can be set to MPU_DPLL_CLK / 4 for MPU_DPLL_CLK clock running at 800MHz or lower.

The programmable divider for the asynchronous bridge to L3 and Memory Adapter (MA) interfaces to EMIF must be set to MPU_DPLL_CLK / 4 when MPU_DPLL_CLK clock frequency is above 800MHz. They can be set to MPU_DPLL_CLK / 2 for MPU_DPLL_CLK clock running at 800MHz or lower.

For more information on the programmable dividers for the asynchronous bridges, see the CM_MPU_MPU_CLKCTRL register, CLKSEL_ABE_DIV_MODE and CLKSEL_EMIF_DIV_MODE bits, in the OMAP4470 TRM.

Please make sure to set the corresponding register bits to 0x1 before increasing the MPU_DPLL_CLK clock frequency above 800MHz.
Please make sure to decrease the MPU_DPLL_CLK clock frequency at or below 800MHz before setting the corresponding register bits to 0x0.

CAUTION

During MPU DVFS sequencing to a higher OPP, please make sure to increase the voltage prior to the clocks frequencies.
During MPU DVFS sequencing to a lower OPP, please make sure to decrease the clocks frequencies prior to the voltage.
Not respecting this MPU DVFS sequencing may lead to internal timing violations.

CAUTION

When MPU requires higher voltage and higher CORE voltage, CORE voltage has be increased prior to MPU voltage, then CORE clocks frequencies have to be increased prior to MPU clocks frequencies.
When MPU allows lower voltage and lower CORE voltage, MPU clocks frequencies have to be decreased prior to CORE clocks frequencies, then MPU voltage has be decreased prior to CORE voltage.
Not respecting this MPU and CORE DVFS sequencing may lead to internal timing violations or/and insufficient OMAP interconnect throughput.

2.2 Imaging and Video Accelerator (IVA) Clocks

CAUTION

For more information on nominal, minimum, maximum voltages location, see the Figure 1-1, *Nominal, Minimum, Maximum Voltages Terminology*.

Table 2-3 shows the recommended V_{DD2} (corresponding to vdd_iva, IVA voltage) initial voltages settings with AVS class 1.5 enabled.

Table 2-3: IVA - Initial pre-AVS Voltages Settings

	RETENTION (4)	OPPBOOT (4)			OPP50 (1)(6)			OPP100 (1)(6)			OPPTB (1)(3)			OPPNT (1)(3)			OPPNTSB (1)(2)(3)		
	MIN	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
V_{DD2} (2)(5) (V)	0.750	0.879	0.925	0.971	0.902	0.962	0.997	1.080	1.137	1.194	1.223	1.287	1.351	1.306	1.375	1.444	1.306	1.38	1.444

(1) Enabling AVS feature is mandatory for these OPPs (OPP50, OPP100, OPPTB, OPPNT or OPPNTSB) to avoid impact on device reliability and lifetime POH (Power-On-Hours).
(2) These V_{DD2} (vdd_iva) voltage ranges define the safe V_{DD2} (vdd_iva) voltage ranges to be used before using AVS class 1.5 feature for OPPs calibration. The minimum voltage may be lower after calibration than this specification.
(3) ABB (adaptive body biasing polarization) feature must be enabled for OPPTB, OPPNT and OPPNTSB operating points following the ABB programming feature steps described in PRCM chapter of OMAP4470 TRM.
(4) Retention and OPPBOOT V_{DD2} (vdd_iva) voltage ranges are defined with AVS feature disabled.
(5) Nominal voltage value documented in this table corresponds to the voltage to be applied at power IC (PMIC) level. Whereas minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(6) OPP50 or OPP100 can be used with AVS disabled for short periods of time (i.e. for ROM code or boot loader) as long as only one CPU is active. This is not applicable to OPPTB, OPPNT, OPPNTSB.

Table 2-4 describes the standard processors clocks speed characteristics vs V_{DD2} (corresponding to vdd_iva, IVA voltage) with AVS class 1.5 disabled or enabled.

Table 2-4: IVA Clocks AC Performances (2)

		OPP50		OPP100		OPPTB		OPPNT		OPPNTSB	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**
DPLL_IVA Locked Frequency	-	1862	-	1862	-	992	-	1290	-	1500	-
IVAHD_ROOT_CLK	DPLL_IVA Locked Frequency (CLKOUTX2_M5)	133	(M5 = 14) (1)	266	(M5 = 7) (1)	331	(M5 = 3) (1)	430	(M5 = 3) (1)	500	(M5 = 3) (1)
DSP_ROOT_CLK	DPLL_IVA Locked Frequency (CLKOUTX2_M4)	232.8	(M4 = 8) (1)	465.5	(M4 = 4) (1)	496	(M4 = 2) (1)	430	(M4 = 3) (1)	500	(M4 = 3) (1)

(1) This ratio is configurable by software programming. For more information, see the Power, Reset, and Clock Management / Clock Manager Functional Description / Internal Clock Generation section of the OMAP4470 TRM.
(2) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

CAUTION

During IVA DVFS sequencing to a higher OPP, please make sure to increase the voltage prior to the clocks frequencies.
During IVA DVFS sequencing to a lower OPP, please make sure to decrease the clocks frequencies prior to the voltage.
Not respecting this IVA DVFS sequencing may lead to internal timing violations.

CAUTION

When IVA requires higher voltage and higher CORE voltage, CORE voltage has be increased prior to IVA voltage, then CORE clocks frequencies have to be increased prior to IVA clocks frequencies.
When IVA allows lower voltage and lower CORE voltage, IVA clocks frequencies have to be decreased prior to CORE clocks frequencies, then IVA voltage has be decreased prior to CORE voltage.
Not respecting this IVA and CORE DVFS sequencing may lead to internal timing violations or/and insufficient OMAP interconnect throughput.

2.3 Core and Peripheral Clocks

CAUTION

For more information on nominal, minimum, maximum voltages location, see the Figure 1-1, *Nominal, Minimum, Maximum Voltages Terminology*.

Table 2-5 shows the recommended VDD3 (corresponding to vdd_core, CORE and Graphic accelerator voltage at ball level) voltage ranges.
GPU and Core are in the same voltage domain.

Table 2-5: Core Voltages

	RETENTION (4)				OPPBOOT(4)			OPP50(3)			OPP100(3)			OPP119 (3)(5)		
	MIN	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
V_{DD3} (1)(2) (V)	0.750	0.879	0.925	0.971	0.93	0.98	1.03	1.069	1.126	1.181	1.12	1.19	1.24			

(1) This table defines:
- Either, the safe V_{DD3} (vdd_core) voltage ranges to be used before using a AVS class 1.5 feature for OPPs calibration. After calibration, the minimum voltage may be lower than this specification.
- Or, the safe V_{DD3} (vdd_core) voltage ranges to be used when AVS class 1.5 feature is disabled.

(2) Nominal voltage value documented in this table corresponds to the voltage to be applied at power IC (PMIC) level. Whereas minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(3) Enabling AVS feature is mandatory for these OPPs (OPP50, OPP100, OPP119) to avoid impact on device reliability and lifetime POH (Power-On-Hours).
(4) Retention and OPPBOOT V_{DD3} (vdd_core) voltage ranges are defined with AVS feature disabled.
(5) OPP119 operating point corresponds to the Overdrive mode.

Table 2-6 and Table 2-7 show the standard device speed characteristics vs V_{DD3} (vdd_core voltage).

Table 2-6: Core Clocks AC Performances – HIGH Performances - From DPLL CORE [3]

		OPP50		OPP100		OPP119 [2]	
Description	Source Clock	Max Freq. (MHz)	Ratio	Max Freq. (MHz)	Ratio	Max Freq. (MHz)	Ratio
DPLL_CORE Locked Frequency	-	1864	-	1864	-	1864	-
CORE_X2_CLK (CLKOUTX2_M5)	DPLL_CORE Locked Frequency	233	(M5 = 8) [1]	233	(M5 = 8) [1]	466	(M5 = 4) [1]
DLL_X2_CLK (CLKOUTX2_M4)	DPLL_CORE Locked Frequency	233	(M4 = 8) [1]	233	(M4 = 8) [1]	233	(M4 = 8) [1]
CORE_CLK	CORE_X2_CLK	233	1 [1]	233	1 [1]	466	1 [1]
L3_ICLK	CORE_CLK	116.5	2 [1]	116.5	2 [1]	233	2 [1]
L4_ICLK	L3_ICLK	58.25	2 [1]	58.25	2 [1]	116.5	2 [1]
PHY_ROOT_CLK (CLKOUT_M2)	DPLL_CORE Locked Frequency	466	2 * (M2 = 2) [1]	466	2 * (M2 = 2) [1]	932	2 * (M2 = 1) [1]
DDR_PHY_CLK (DDRPHY divider)	PHY_ROOT_CLK (CLKOUT_M2)	233	2 [1]	233	2 [1]	466	2 [1]
EMIF_FCLK (DDRPHY divider)	DDR_PHY_CLK	116.5	2 [1]	116.5	2 [1]	233	2 [1]
EMIF_DLL_FCLK	DLL_X2_CLK	116.5	2	116.5	2	116.5	2
GPMC_CLK	L3_ICLK	58.25	2 [1]	58.25	2 [1]	58.25	4 [1]

(1) This ratio is configurable by software programming. For more information, see the OMAP4470 TRM.
(2) OPP119 operating point corresponds to the Overdrive mode.
(3) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

Table 2-7: Core Clocks AC Performances – LOW Power - From DPLL CORE [3]

		OPP50		OPP100		OPP119 [2]	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**
DPLL_CORE Locked Frequency	-	1600	-	1600	-	1600	-
CORE_X2_CLK (CLKOUTX2_M5)	DPLL_CORE Locked Frequency	200	(M5 = 8) [1]	400	(M5 = 4) [1]	400	(M5 = 4) [1]
DLL_X2_CLK (CLKOUTX2_M4)	DPLL_CORE Locked Frequency	200	(M4 = 8) [1]	200	(M4 = 8) [1]	200	(M4 = 8) [1]
CORE_CLK	CORE_X2_CLK	200	1 [1]	400	1 [1]	400	1 [1]
L3_ICLK	CORE_CLK	100	2 [1]	200	2 [1]	200	2 [1]
L4_ICLK	L3_ICLK	50	2 [1]	100	2 [1]	100	2 [1]
PHY_ROOT_CLK (CLKOUT_M2)	DPLL_CORE Locked Frequency	400	2 * (M2 = 2) [1]	800	2 * (M2 = 1) [1]	800	2 * (M2 = 1) [1]
DDR_PHY_CLK (DDRPHY divider)	PHY_ROOT_CLK (CLKOUT_M2)	200	2 [1]	400	2 [1]	400	2 [1]
EMIF_FCLK (DDRPHY divider)	DDR_PHY_CLK	100	2 [1]	200	2 [1]	200	2 [1]
EMIF_DLL_FCLK	DLL_X2_CLK	100	2	100	2	100	2
GPMC_CLK	L3_ICLK	50	2 [1]	100	2 [1]	100	2 [1]

(1) This ratio is configurable by software programming. For more information, see the OMAP4470 TRM.
(2) OPP119 operating point corresponds to the Overdrive mode.
(3) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

2.4 Graphic Accelerator Clocks

Table 2-8 and Table 2-9 show the recommended V_{DD3} (corresponding to vdd_core, Core and Graphic accelerator voltage) standard graphic accelerator clocks speed characteristics vs V_{DD3}.

Table 2-8: Graphic Accelerator Clocks – HIGH Performances (3)

		OPP50		OPP100		OPP119(2)	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**
SGX544-SC (3D graphic accelerator)							
DPLL_PER Locked Frequency	-	1536	-	1536		1536	-
PER_SGX_FCLK	DPLL_PER Locked Frequency (CLKOUTX2_M7)	192	(M7 = 8) (1)	307	(M7 = 5) (1)	384	(M7 = 4) (1)
SGX_FCLK	PER_SGX_FCLK	192	1	307	1	384	1
BB2D (GC320 – 2D graphic accelerator)							
DPLL_PER Locked Frequency	-	1536	-	1536	-	1536	-
PER_BB2D_FCLK	DPLL_PER Locked Frequency (CLKOUTX2_M6)	192	(M7 = 8) (1)	307	(M7 = 5) (1)	384	(M7 = 4) (1)
BB2D_FCLK	PER_BB2D_FCLK	192	1	307	1	384	1

(1) This ratio is configurable by software programming. For more information, see the OMAP4470 TRM.
(2) OPP119 operating point corresponds to the Overdrive mode.
(3) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

Table 2-9: Graphic Accelerator Clocks – LOW Power (3)

		OPP50		OPP100		OPP119 (2)	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**
SGX3D							
DPLL_PER Locked Frequency	-	1536	-	1536	-	1536	-
PER_SGX_FCLK	DPLL_PER Locked Frequency (CLKOUTX2_M7)	153.6	(M7 = 10) (1)	307.2	(M7 = 5) (1)	384	(M7 = 4) (1)
SGX_FCLK	PER_SGX_FCLK	153.6	1	307.2	1	384	1
BB2D (GC320)							
DPLL_PER Locked Frequency	-	1536	-	1536	-	1536	-
PER_BB2D_FCLK	DPLL_PER Locked Frequency (CLKOUTX2_M6)	153.6	(M7 = 10) (1)	307.2	(M7 = 5) (1)	384	(M7 = 4) (1)
BB2D_FCLK	PER_BB2D_FCLK	153.6	1	307.2	1	384	1

(1) This ratio is configurable by software programming. For more information, see the OMAP4470 TRM.
(2) OPP119 operating point corresponds to the Overdrive mode.
(3) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

CAUTION

During CORE DVFS sequencing to a higher OPP, please make sure to increase the voltage prior to the clocks frequencies.
During CORE DVFS sequencing to a lower OPP, please make sure to decrease the clocks frequencies prior to the voltage.
Not respecting this CORE DVFS sequencing may lead to internal timing violations.

CAUTION

When using CORE OPP100 (or OPP119) and thus setting related CORE voltage, it is highly recommended to set also CORE clocks frequencies to their maximum allowed values for enabling best throughputs on OMAP interconnect and DDR.
Using CORE OPP50 maximum allowed clock frequencies while CORE OPP100 (or OPP119) voltage is required, may lead to random system lock-up depending on the application's throughput requirements (OMAP interconnect and DDR).
Same issues may happen in case CORE OPP100 is used while CORE OPP119 is required.

3 OPP DEPENDENCIES

CAUTION

The OPP dependencies apply only when both voltage domains are in ON state. That is:
- Any module in the domain may be powered, clocked and active
- SMPS is in active mode, delivering the voltage corresponding to current OPP
For more information on the Voltage Domain definitions, see the Power, Reset and Clock Management / Voltage Management Functional Description section in the OMAP4470 TRM

Reminder: for an OPP, the frequency corresponds to the maximum frequency allowed at a voltage (this voltage corresponds to the minimum voltage level required on a domain).
The dependencies defined in the tables below apply to the minimum voltages, the frequencies do not matter.

The following rules must be respected on OPPs between the three voltage domains:

1) If one of the MPU voltage domain or IVA voltage domain is at OPP100 or above (i.e. OPPTB, OPPNT, OPPNTSB), then the CORE voltage domain must be set to OPP100 or above (i.e. OPP119).

2) The MPU voltage domain and IVA voltage domain must be both at OPP50 for having the CORE voltage domain at OPP50.

3) If the MPU voltage domain is at OPPTB or above (i.e. OPPNT, OPPNTSB), then IVA voltage domain must be at least at OPP100 (i.e. OPP100, OPPTB, OPPNT, OPPNTSB).

Table 3-1 shows the acceptable MPU and IVA voltage domain OPPs according to the CORE voltage domain OPP.

Table 3-1: OPP Dependencies (CORE vs IVA / MPU)

CORE voltage domain OPP	OPP50	OPP100, OPP119
Acceptable MPU voltage domain OPPs	OPP50	OPP50, OPP100, OPPTB, OPPNT, OPPNTSB
Acceptable IVA voltage domain OPPs	OPP50	OPP50, OPP100, OPPTB, OPPNT, OPPNTSB

Table 3-2 shows the acceptable IVA voltage domain OPPs according to the MPU voltage domain OPP.

Table 3-2: OPP Dependencies (MPU vs IVA)

MPU voltage domain OPP	OPP50, OPP100	OPPTB, OPPNT, OPPNTSB
Acceptable IVA voltage domain OPPs	OPP50, OPP100, OPPTB, OPPNT, OPPNTSB	OPP100, OPPTB, OPPNT, OPPNTSB

4 MAXIMUM FREQUENCY BY INTERFACE

The following table summarizes the maximum frequencies supported by OMAP4470 interfaces, and by OPPs.

Table 4-1. Maximum Frequency By Interface

Interfaces	Modes	External I/O Clocks	CORE Voltage Domain		
			OPP119 (MHz)	OPP100 (MHz)	OPP50 (MHz)
General-Purpose Memory Controller (GPMC)					
GPMC/NOR Flash Interface—Synchronous Mode	100MHZ	gpmc_clk	100	100	50
	66MHZ	gpmc_clk	66	66	33
	58MHZ	gpmc_clk	58.25	58.25	58.25
External Memory Interface (EMIF)					
EMIF—LP**DDR SDRAM**	DDR mode – 466MHz	lpddr2x_ck, lpddr2x_nck (clocks) lpddr2x_dqs, lpddr2x_ndqs (strobes)	466	233	233
	DDR mode – 400MHz	lpddr2x_ck, lpddr2x_nck (clocks) lpddr2x_dqs, lpddr2x_ndqs (strobes)	400	400	200
Camera					
CSI21 and CSI22 - High-Speed Mode	Up to 3 Data Lanes	One pair of lanes	500	500	400
	4 data lanes	One pair of lanes	412	412	400
Camera Serial Interface (CCP2—CSI22)	CCP2 – Class 0	One pair of lanes	208	208	208
	CCP2 – Class 1	One pair of lanes	208	208	208
	CCP2 – Class 2	One pair of lanes	325	325	325
Parallel Camera Interface (CPI)	Video and Graphics Digitizer 1.8-V Mode	cam2_pclk	148.5	148.5	NA
Display					
DSS—Display Controller (DISPC)	QXGA SDR Mode	dispc2_pclk	170	170	NA
DSI1 and DSI2	Up To 3 Data Lanes	One pair of lanes	450	450	450
DSI1	4 Data Lanes	One pair of lanes	412	412	412
McBSP					
McBSP1 and McBSP2—I2S/PCM Full and Half Cycle— Master Mode—24 MHz	Master Mode	abe_mcbspx_clk, x=[1,2,3]	24.57	24.57	12.28
McBSP1 and McBSP2—I2S/PCM Full and Half Cycle— Slave Mode—12 MHz	Slave Mode	abe_mcbspx_clk, x=[1,2,3]	12.288	12.288	6.144
McBSP1, McBSP2, and McBSP3 Set#1— TDM / Half-Cycle - 12MHz, 5-pF Load Capacitance	Master Mode	abe_mcbspx_clk, x=[1,2,3]	12.288	12.288	6.144
	Slave Mode	abe_mcbspx_clk, x=[1,2,3]	12.288	12.288	6.144
McBSP1, McBSP2, and McBSP3 Set#1— TDM / Half-Cycle - 6MHz, 40-pF Load Capacitance	Master Mode	abe_mcbspx_clk, x=[1,2,3]	6.144	6.144	3.072
	Slave Mode	abe_mcbspx_clk, x=[1,2,3]	6.144	6.144	3.072
McBSP3—I2S/PCM Full and Half Cycle— Master Mode—24 MHz	Master Mode	abe_mcbspx_clk, x=[1,2,3]	24.57	24.57	12.28
McBSP3—I2S/PCM Full and Half Cycle— Slave Mode—12 MHz	Slave Mode	abe_mcbspx_clk, x=[1,2,3]	12.288	12.288	6.144
McBSP4—I2S/PCM—Full Cycle— 48-MHz Master Mode	Master Mode	mcbsp4_clk	48	48	24
McBSP4—I2S/PCM—Full Cycle— 24-MHz Slave Mode	Slave Mode	mcbsp4_clk	24	24	12

Interfaces	Modes	External I/O Clocks	CORE Voltage Domain		
			OPP119 (MHz)	OPP100 (MHz)	OPP50 (MHz)
McBSP4—I2S/PCM—Half-Cycle—24-MHz Master and 12-MHz Slave	Master Mode	mcbsp4_clk	24	24	12
	Slave Mode	mcbsp4_clk	12	12	6
McASP		abe_mcasp_ahclkx / abe_mcasp_aclkx	24.57	24.57	24.57
McSPI					
McSPI1, McSPI2, McSPI3 and McSPI4	Slave Mode	mcspix_clkx, x=[1,2,3,4]	16	16	8
McSPI1 and McSPI2—Master Mode	Master - 24-MHz Frequency Clock	mcspix_clkx, x=[1,2,3,4]	24	24	24
McSPI2, McSPI3, and McSPI4—Master Mode	Master - 48-MHz Frequency Clock	mcspix_clkx, x=[1,2,3,4]	48	48	48
DMIC	Master/Receive Mode	abe_dmic_clk[3:1]	3.84	3.84	3.84
McPDM		abe_clks / abe_pdm_lb_clk	19.2	19.2	19.2
ABE SlimBus1, SlimBus2	SLIMBUS SDR 24.6 MHz	slimbusx_clock, x=[1,2]	24.57	24.57	12.28
ABE SlimBus1, SlimBus2	SLIMBUS SDR 19.2 MHz	slimbusx_clock, x=[1,2]	19.2	19.2	9.6
High-Speed Synchronous Interface					
High-Speed Synchronous Interface 1	Transmit Mode—1.2V	hsi1_acdata, hsi1_acflag	192	192	96
	Receive Mode—1.2V	hsi1_cadata, hsi1_caflag	225	225	112
	Transmit Mode—1.8V	hsi1_acdata, hsi1_acflag	192	192	96
	Receive Mode—1.8V	hsi1_cadata, hsi1_caflag	225	225	112
High-Speed Synchronous Interface 2	Transmit Mode—1.2V	hsi2_acdata, hsi2_acflag	192	192	96
	Receive Mode—1.2V	hsi2_cadata, hsi2_caflag	225	225	112
	Transmit Mode—1.8V	hsi2_acdata, hsi2_acflag	192	192	96
	Receive Mode—1.8V	hsi2_cadata, hsi2_caflag	225	225	112
USB					
Universal Serial Bus (USB)—USBA0	ULPI SDR—Slave Mode—1.8V	usba0_ulpiphy_clk	60	60	NA
Universal Serial Bus (USB)—USBB1	HSIC DDR Transmit Mode—1.2V	usbb1_hsic_strobe	240	240	NA
	HSIC DDR Receive Mode—1.2V	usbb1_hsic_strobe	240	240	NA
	ULPI TLL Mode—Master Mode—1.8V	usbb1_ulpiphy_clk	60	60	60
	ULPI SDR Mode—Slave Mode—1.8V	usbb1_ulpiphy_clk	60	60	NA
Universal Serial Bus (USB)—USBB2	HSIC DDR Transmit Mode—1.2V	usbb2_hsic_strobe	240	240	NA
	HSIC DDR Receive Mode—1.2V	usbb2_hsic_strobe	240	240	NA
	ULPI TLL Mode—Master Mode	usbb2_ulpitll_clk	60	60	60
	ULPI SDR Mode—Slave Mode	usbb2_ulpiphy_clk	60	60	NA
I2C & SmartReflex					
	Standard Mode I2C & SR	i2cx_scl, x=[1,2,3,4,5]	0.1	0.1	0.1
	Fast Mode I2C & SR	i2cx_scl, x=[1,2,3,4,5]	0.4	0.4	0.4
	High Speed I2C	i2cx_scl, x=[1,2,3,4]	3.4	3.4	3.4
	High Speed SR	i2cx_scl, x=[5]	2.13	2.13	2.13
SDMMC					
MMC/SD/SDIO 1 Interface	SD Identification Mode	sdmmc1_clk	0.4	0.4	0.4
	(1.8V IO) Standard SD Mode	sdmmc1_clk	24	24	24
	(3.3V IO) Standard SD Mode	sdmmc1_clk	24	24	24
	High-Speed SD Mode – SR25	sdmmc1_clk	48	48	48
	High-Speed SD Mode – SR50	sdmmc1_clk	64	64	32
	High-Speed SD Mode-DDR50	sdmmc1_clk	48	48	24

Interfaces	Modes	External I/O Clocks	CORE Voltage Domain		
			OPP119 (MHz)	OPP100 (MHz)	OPP50 (MHz)
MMC/SD/SDIO 2 Interface	Standard SDR JC64 Mode	sdmmc2_clk	24	24	24
	High-Speed SDR JC64 Mode	sdmmc2_clk	48	48	48
	High-Speed DDR JC64 Mode	sdmmc2_clk	48	48	48
MMC/SD/SDIO 3, 4, and 5 Interfaces	High-Speed SDIO Mode	sdmmcx_clk, x=[3,4,5]	48	48	48
Digital Processing Manager Interface (DPM)					
Trace Port Interface Unit (TPIU)	TPIU PLL DDR Mode – 160 MHz	atpiu_clk	160	160	160
System Trace Module Interface (STM)	Lauterbach DDR Transmit Mode	astm_clk	100	100	100
	MIPI DDR Transmit Mode	astm_clk	100	100	100
	MIPI SDR Transmit Mode	astm_clk	100	100	100
JTAG					
JTAG	Free-Running Clock Mode	jtag_tck / jtag_rtck	20	20	15
	Adaptive Clock Mode	jtag_tck / jtag_rtck	20	20	15
cJTAG	For MMC PADs	jtag_tck	17.5	17.5	14
	For JTAG PADs	jtag_tck	20	20	19

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