Public Version

OMAP4460 Multimedia Device
Silicon Errata
Silicon Revision 1.1, 1.0

Texas Instruments OMAP™ Family of Products

Version L

Errata

Literature Number: SWPZ017L
September 2011–Revised September 2013

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Note :OMAP™ 4 processors are intended for manufacturers of Smartphones and other mobile devices.

Revision History

The following table summarizes the OMAP4460 Public Silicon Errata versions.

Version	Literature Number	Date	Notes
A	SWPZ017	September 2011	See (1)
B	SWPZ017	December 2011	See (2)
C	SWPZ017	January 2012	See (3)
D	SWPZ017	February 2012	See (4)
E	SWPZ017	March 2012	See (5)

(1) Initial release.

(2) Added:
- CBUFF Ready Window Event in Write Mode
- CSI-2 Receiver Executes SW Reset Unconditionally
- USB Host TLL Bitstuffing Feature Is Broken
- ISP H3A Hangs Due to Unstable Vertical Sync Signal
- GPIO IRQ not generated after MPU Idle if irqstatus bits not cleared
- DSI PLL signal is not available on HW observability pads
- Blending Calculation error when Premultiply Alpha is used
- DSS block in “idle transition” state when using RFBI I/F
- Deadlock between Smart Reflex and Voltage Processor
- i705: SDMMC1 interface latch-up issue
- EMIF: 8Gbit (single die) support
- Refresh rate issue after warm reset
- System May Hang after warm reset
- DDR Access Hang After Warm Reset

Updated:
- i699:DMA4 channel fails to continue with descriptor load when Pause bit is cleared through config port access while in Standby
- i688:Async Bridge Corruption

Removed:
- i680: RM_MPU_MPU_CONTEXT:LOSTCONTEXT_RFF reset

(3) Added:
- i733: DSS Configuration Registers Access Through the L4 Interconnect Removed
- i734: LCD1 Gamma Correction Is Not Working When GFX Pipe Is Disabled
- i735: Power Management Timer Value For Self-Refresh (SR_TIM)

Updated:
- i688: Async Bridge Corruption
- i525: Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0 in command mode

Removed:
- i684: I/O Incorrectly Trimmed

(4) Added:
- i736: Leakage Increase On LPDDR2 IOs
- i738: Change In OMAP4xx Off Mode Sequence For a TPS62361B Based Platform
- i739: MMC1 Booting May Be Bypassed Depending On VDD Ramp-up Delay
- i740: Disconnect Protocol Violation

Updated:
- i631:Wrong Access In 1D Burst For YUV4:2:0-NV12 Format

(5) Added:
- i741: High-Speed Image Capture Use Case
- i743: LPDDR2 Power-Down State is Not Efficient
- i745: MPU-EMIF Static Dependency Needed Around MPU WFI
- i746: SYSEN Usage for an OMAP44xx Platform Based on TWL6030/TWL6032 and TPS62361B

Updated:
- i728: System May Hang During EMIF Frequency Change
- i727: Refresh Rate Issue After Warm Reset
- i729: DDR Access Hang After Warm Reset
- i704: LPDDR2 High Temperature Operating Limit Exceeded
- i682: DDR PHY Must be Reset After Leaving OSWR

Version	Literature Number	Date	Notes
F	SWPZ017	April 2012	See (6)
G	SWPZ017	May 2012	See (7)
H	SWPZ017	July 2012	See (8)
I	SWPZ017	August 2012	See (9)
J	SWPZ017	October 2012	See (10)
K	SWPZ017	November 2012	See (11)
L	SWPZ017	September 2013	See (12)

(6) Added:
- i752: ECD3 Fails To Decode Bitstreams Having Mismatch Between CBP and CBF
- i754: ULPI RxCmds Convey the Wrong ID Bit After Save-and-Restore Sequence
- i755: PRCM Hang at Frequency Update During DVFS
- i760: Programming of CM_CLKSEL_DPLL_CORE[20]DPLL_CLKOUTHIF_CLKSEL

Updated:
- i700: MPU clock glitches at OPP change

(7) Added:
- i761: Card Error Interrupt May Not Be Set Sometimes
- i762: In AutoCMD12 mode, the CMD12 Command Is Not Issued On Write Transfer Completion
- i763: TV Overlay Blending Limitation
- i764: SRAM LDO Output Voltage Value Software Override in RETENTION is Not Functional
- i765: I/O Glitch Issue When Entering Off Mode

(8) Added:
- i103: Delay needed to read some GP timer, WD timer and sync timer registers after wakeup

(9) Added:
- i719: HS USB: Multiple OFF Mode Transitions Introduce Corruption
- i774: HS USB Host HSIC Remote Wakeup Is Not Functional
- i776: Power Delivery Network Verification
- i779: ISP Pattern Generator Is Not Functional

Updated:
- i734: LCD1 Gamma Correction Is Not Working When GFX Pipe Is Disabled

(10) Added:
- i796: I2C FIFO Draining Interrupt Not Generated
- i797: PRCM Voltage Controller Uses MPU Slave Address

(11) Added:
- i800: McPDM Downlink Data Corrupted With TWL604x
- i804: Read Accesses to GP Timer TCRR Can Report Random Value When In Posted Mode

(12) Added:
- i817: Voltage Drop Observed On CSI PHY Pad In GPI mode

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	i705: SDMMC1 interface latch-up issue
	i739: MMC1 Booting May Be Bypassed Depending On VDD Ramp-up Delay
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	i738: Change In OMAP4xx Off Mode Sequence For a TPS62361B-Based Platform
	i740: Disconnect Protocol Violation
	i745: MPU-EMIF Static Dependency Needed Around MPU WFI
	i755: PRCM Hang at Frequency Update During DVFS
	i760: Programming of CM_CLKSEL_DPLL_CORE[20]DPLL_CLKOUTHIF_CLKSEL
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Bugs

1.1 Delay needed to read some GP timer, WD timer and sync timer registers after wakeup

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i103

CRITICALITY

Low

DESCRIPTION

If a General Purpose Timer (GPTimer) is in posted mode (TSICR.POSTED=1), due to internal resynchronizations, values read in TCRR, TCAR1 and TCAR2 registers right after the timer interface clock (L4) goes from stopped to active may not return the expected values. The most common event leading to this situation occurs upon wake up from idle.

GPTimer non-posted synchronization mode is not impacted by this limitation.

This limitation also impacts read from Watchdog timers WCRR registers.

All the watchdog timers support only POSTED internal synchronization mode. There is no capability to change the internal synchronization scheme to NON-POSTED by software.

The 32KSYNCNT_CR register is also impacted by this limitation, since the 32K sync timer is always in posted synchronization mode.

WORKAROUND

Software has to wait at least (2 timer interface clock cycles + 1 timer functional clock cycle) after L4 clock wakeup before reading TCRR, TCAR1 or TCAR2 registers for GPTimers in POSTED internal synchronization mode, and before reading WCRR register of the Watchdog timers . The same workaround must be applied before reading 32KSYNCNT_CR register of the 32K sync module.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.2 MDR1 access can freeze UART module

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i202

CRITICALITY

Medium

DESCRIPTION

Because of a glitchy structure inside the UART module, accessing the MDR1 register may create a dummy underrun condition and freeze the UART in IrDa transmission. In UART mode, this may corrupt the transferred data(received or transmitted).

WORKAROUND

To ensure this problem does not occur, the following software initialization sequence must be used each time MDR1 must be changed:

1. If needed, setup the UART by writing the required registers, except MDR1
2. Set appropriately the MDR1.MODE_SELECT bit field
3. Wait for 5 L4 clock cycles + 5 UART functional clock cycles
4. Clear TX and RX FIFO in FCR register to reset its counter logic
5. Read RESUME register to resume the halted operation

Step 5 is for IrDA mode only and can be omitted in UART mode.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.3 DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i339

CRITICALITY

Low

DESCRIPTION

Minimum number of pixels for MIPI command mode from the video port should be greater than 1 (at least 2). Image with less than 2 pixels is not expected to be used in a real applicative use case.

WORKAROUND

If sending a single pixel is needed, the OCP L4 slave port can be used (through CPU or sDMA).

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.4 DSI: Cancel Tearing Effect Transfer

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i340

CRITICALITY

Low

DESCRIPTION

Transfer using tearing effect cannot be cancelled (writing TE_SIZE to 0). Writing TE_SIZE would have no effect and transfer would continue.

WORKAROUND

Always wait for tearing effect to complete before changing any configuration.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.5 DSI: RX FIFO Fullness

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i341

CRITICALITY

Low

DESCRIPTION

RX FIFO fullness can be incorrect just after a FIFO read. FIFO fullness should be read only once at the beginning of the transfer. Other accesses during a transfer are not guaranteed.

WORKAROUND

Use only programming model provided in Programming Model section in the TRM.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.6 DSI: Access Restriction On DSI_TIMING2 Register

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i342

CRITICALITY

Low

DESCRIPTION

This register must not be written twice when TxByteClkHS is stopped to avoid L4 OCP port deadlock.

WORKAROUND

User must check that the TxByteClkHS clock is activated before initiating any write access to DSI_TIMING2 register.

To ensure the TxByteClkHS clock is active, the user must check:

1. PLL is locked (DSI_PLL_STATUS register; DSI_PLL_LOCK bit)
2. DSIPHY must be in ON power state (PWRCMDON).
3. Clock/Data lane positions are correctly set (DSI_COMPLEXIO_CFG1.xxx_POSITION).

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.7 DSI: Tx FIFO Flush Is Not Supported

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i343

CRITICALITY

Low

DESCRIPTION

Executing a FIFO flush does not properly clean the logic, thus resulting in unpredictable behavior of the module.

WORKAROUND

User must perform module software reset when a transfer is aborted.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.8 sDMA Channel Is Not Disabled After A Transaction Error

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i378

CRITICALITY

Medium

DESCRIPTION

In case of destination synchronized transfer on the write port (or source sync with SDMA.DMA4_CCRi[25] BUFFERING_DISABLE = 1), if a transaction error is reported at the last element of the transaction, the channel is not automatically disabled by DMA.

WORKAROUND

Whenever a transaction error is detected on a transaction on the write side of the channel i, software must disable the channel(i) by setting the DMA4_CCRi[7] ENABLE bit to 0.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.9 DSI SOF Packet Not Send

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i422

CRITICALITY

Low

DESCRIPTION

The first packet in command mode is not sent due to inaccurate clock gating.

Root cause description: In command mode when DDR_CLK_ALWAYS_ON and IF_EN are set to 1, DDR clock is not present immediately after the IF_EN bit is set to 1 but when the first HS packet from OCP is ready to be sent to PPI HS link.

The DDR_CLK_PRE field is used between the start of the DDR clock and the assertion of the data request signal. After the time defined by the DDR_CLK_PRE field, the clock lane is always present until the IF_EN bit is set to 0. So, there is a delay between IF_EN set to 1 and assertion of the clock lane.

WORKAROUND

In case of command mode where DDR clock should be provided to peripheral before data, the workaround is to program DDR_CLK_PRE =! 0. The value of DDR_CLK_PRE must take into account the different timings: TCLK_PREPARE, TCLK_ZERO.

Sequence to enable the DSI:

1. Set the ForceTxStopMode bit to 1 (DSI_TIMING1 register). This asserts the ForceTxStopMode.
2. Enable virtual channel in command mode / Enable DSI interface.
3. Poll the ForceTxStopMode bit to 0 (DSI_TIMING1 register) until deassertion of the ForceTxStopMode bit. The hardware resets this bit at the end of the counter value.
4. Send SOF(0x00000000) packet in command mode.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.10 SIMCOP Lens Distortion Correction issue

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i487

CRITICALITY

Medium

DESCRIPTION

SIMCOP LDC module doesn't reach 100 MPix/s target in bilinear mode for YUV420 data.

WORKAROUND

Use LDC in YUV422 mode.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.11 ISS: SOFTRESET Bit Status Not Working For Circular Buffer

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i488

CRITICALITY

Low

DESCRIPTION

The SOFTRESET bit of the SYSCONFIG register inside CBUFF (CBUFF_HL_SYSCONFIG[0] SOFTRESET) is set to 0x0 (reset done state) after reset only if CBUFF is out of IDLE.

While CBUFF slave data port is in IDLE, the SOFTRESET bit is always set to 0x1 (status bit gives an ongoing reset, but reset is finished).

WORKAROUND

Ignore status of the the SOFTRESET bit. After a software reset, wait a few cycles before using the module.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.12 ISS: SOFTRESET Bit Status Not Working For Burst Translation Engine

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i489

CRITICALITY

Low

DESCRIPTION

The SOFTRESET bit of the SYSCONFIG register inside BTE (BTE_HL_SYSCONFIG[0] SOFTRESET) is set to 0x0 (reset done state) after reset only if BTE is out of IDLE.

While BTE slave data port is in IDLE, the SOFTRESET bit is always set to 0x1 (status bit gives an ongoing reset, but reset is finished).

WORKAROUND

Ignore the status of the SOFTRESET bit. After a software reset, wait a few cycles before using the module.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.13 ISS State Can Be Corrupted During Debug Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i496

CRITICALITY

Medium

DESCRIPTION

Debug read operations should not impact the internal state of the module.

That cannot be guaranteed because debug reads of some locations can impact DMA requests. Also, some read accesses may be stalled for a long time while ISP operation is ongoing.

WORKAROUND

To avoid read access from being stalled, the CPU must have the priority. This can be configured in the ISP5_MPSR register. Dummy accesses during frame processing lead to data corruption however response is given immediately. This register can be used to avoid stalling debug accesses. Dummy data is returned in that case but does not hurt functionality because debug accesses do not make sense while ISP5 is processing data.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.14 DSI VSYNC HSYNC Detection In Video Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i483

CRITICALITY

High

DESCRIPTION

DSI engine is not always detecting the first VSYNC HSYNC signals received on the video port in video mode.

WORKAROUND

Because before first VSYNC rising edge, one HSYNC is transmitted and clock is transmitted during that HSYNC period, the workaround is to have the HSYNC period of DISPC longer than the timing described below:

- Configuration with line buffers: 3 VP_PCLK + 6 VP_CLK + 6 DSI_CLK
- Configuration without line buffers: 3 VP_PCLK + 2 VP_CLK

There is no need to take care of some timings related to enabling the IF_EN, VC_EN, LCD output of the DSIPC.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.15 Dual Video Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i524

CRITICALITY

High

DESCRIPTION

When two video ports are available at the input of the DSI protocol engine, the two streams are interleaved by the DSI protocol engine. Only one video mode is supported by the current implementation on VP1 only. VP2 cannot be in video mode even if VP1 is not in video mode.

WORKAROUND

No

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.16 Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i525

CRITICALITY

High

DESCRIPTION

The buffer handshake feature in the DISPC avoids underflow of the DISPC DMA FIFO. The fullness of the DISPC DMA FIFO is checked before providing data to the pipeline when STALL signal is inactive. When the FIFO hand check feature is activated, the pixel transfer to the DSI module during STALL inactivity period can be stopped (no DISPC_PCLK pulse) and restarted when there is enough data in the FIFO. The DSI protocol engine is configured in command mode.

On video port 1 in command mode, when DISPC_DIVISOR1.PCD = 2, DISPC_CONFIG1.BUFFERHANDCHECK = 1 and DSI_CTRL.VP_CLK_RATIO = 0, the FRAMEDONE IRQ might not be triggered and TE_SIZE counter might not be decremented to 0. This is caused by a deadlock between the DISPC and DSI modules during the transfer of the last pixel of a line

On video port 2 in command mode, when DISPC_DIVISOR2.PCD = 2, DISPC_CONFIG2.BUFFERHANDCHECK = 1 and DSI_CTRL2.VP_CLK_RATIO = 0, the FRAMEDONE IRQ might not be triggered and TE_SIZE counter might not be decremented to 0. This is caused by a deadlock between the DISPC and DSI modules during the transfer of the last pixel of a line.

The DSI protocol engine sends a STALL to the DISPC (stall mode); in parallel the DISPC stops the pixel clock to the DSI because it is waiting for its FIFO DMA to be refilled (buffer handcheck feature). When FIFO DMA is refilled, the DISPC being in stall mode does not provide back the pixel clock to the DSI to deassert the stall and it does not send the last pixel to the DSI.

WORKAROUND

DISPC_DIVISORi[7:0] PCD = 2 is not supported, where i = 1 to 3. DISPC should be set to DISPC_DIVISORi[7:0] PCD = 3 or above and DSI_CTRLi[4] VP_CLK_RATIO to 0x1.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.17 Deep Power-Down Support During Off Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i603

CRITICALITY

Medium

DESCRIPTION

When coming out of off mode, the memory controllers assume connected SDRAMs to be in self-refresh mode.

The EMIF receives a DEVICE_OFFWKUP_CORERSTACTST signal from the PRCM defining if an EMIF cold reset was due to a global reset or to exiting off mode;

- In case of a global cold reset, the full SDRAM init phase is performed.
- In case of off mode exit, only the self-refresh exit sequence is performed and auto-refresh commands are immediately sent.

If the memory was in deep power-down state during the chip off mode, the sequence performed by EMIF could result in an unexpected behavior on the memory side. Exit from DPD actually requires the same full init sequence as after a global cold reset.

WORKAROUND

Software workaround:

- Before getting into off mode, force the value stored in the control module EMIF_SDRAM_REF_CTRL.REG_INITREF_DIS to 1.
  - This forces the value for the EMIF register to 1 when its content is restored when returning from off mode.
- When returning from off mode, and before making any access to the memory in DPD state:
  1. Put CORE PLL in MN bypass mode CM_CLKMODE_DPLL_CORE.DPLL_EN = 0x4.
  2. Program the DLL override CM_DLL_CTRL.DLL_OVERRIDE = 1.
  3. Force the configuration field EMIF_SDRAM_CONFIG.REG_SDRAM_TYPE register to 0x1 (reserved), then back to 0x4 (LPDDR2-S4) or 0x5 (LPDDR2-S2) according to memory configuration. This forces the controller back into its init state instead of self-refresh state.
  4. Reconfigure EMIF_SDRAM_REF_CTRL.REG_INITREF_DIS to 0.
  5. Perform normal init phase as from global cold reset.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.18 RTA Feature Is Not Supported

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i608

CRITICALITY

High

DESCRIPTION

RTA (retention till access) feature is not supported and leads to device stability issues when enabled.

The following modules are embedding memories with RTA support:

- MPU subsystem (cache memories)
- OCM RAM
- SGX
- Display subsystem
- HS USB OTG
- IVA-HD subsystem
- Face detect
- Imaging subsystem
- DMM
- DSP subsystem
- AESS

WORKAROUND

PRM_LDO_SRAM_<Memory Voltage Domain>_SETUP[0] DISABLE_RTA_EXPORT default value is loaded by an eFuse value. The fuse value disables this RTA feature, so these bits must be kept at default value.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.19 MMCHS_HCTL.HSPE Is Not Functional

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i626

CRITICALITY

High

DESCRIPTION

Due to design issue MMCHS_HCTL.HSPE bit does not work as intended. This means that the configuration must always be the normal speed mode configuration (MMCHS_HCTL.HSPE=0).

WORKAROUND

None

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.20 Wrong Access In 1D Burst For YUV4:2:0-NV12 Format

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i631

CRITICALITY

Low

DESCRIPTION

When in YUV4:2:0 format in 1D burst, the DISPC DMA skips lines when fetching Chroma sampling.

WORKAROUND

If YUV4:2:0-1D burst is required:

- Set DISPC_VIDp_ATTRIBUTES[22]DOUBLESTRIDE to 0x0 and DISPC_VIDp_ATTRIBUTES[13:12]ROTATION to 0x1 or 0x3

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.21 Status of DSI LDO Is Not Reported to DSI Protocol Engine

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i643

CRITICALITY

Low

DESCRIPTION

The DSI-PHY has an internal LDO. This LDO is used to convert 1.8V coming from VDDS_DSI input into 1.2V for appropriate DSI voltage level.

An internal LDOPWRGOOD signal output by the DSI_PHY indicates the status of the LDO (LDO is up or is down). This signal should be connected to the DSI protocol engine for IRQ reporting (LDO_POWER_GOOD_IRQ).

This signal is not connected to the DSI protocol engine and input of protocol engine is tied to 0x0.

WORKAROUND

There is no workaround to check HW status of DSI LDO.

The LDO_POWER_GOOD_IRQ should be disabled by keeping or setting DSI_IRQENABLE.LDO_POWER_GOOD_IRQ_EN to 0x0.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.22 HSI Break Frame Corrupt OnGoing Transfer

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i645

CRITICALITY

Medium

DESCRIPTION

When a break frame is sent in the middle of data transfers (DMA based),in pipelined flow or synchronized flow, one Tx data frame will be overwritten at the transmitter side by an all-zeros frame (break is received correctly).

Table 1-1. Data Corruption Example

Transmitted Data:	**Received Data:**
0x77CFA0B0	0x77CFA0B0
0xDFFC7B49	0x00000000 <- break frame and data last
0x5BE7AD07	0x5BE7AD07
0x7F7F1BC8	0x7F7F1BC8
....	....

WORKAROUND

No workaround identified.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.23 HSI Error Counters Cannot Be Disabled

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i646

CRITICALITY

High

DESCRIPTION

The counter configuration capabilities include start (begin counting), stop (halt counting), and load (set time-out period).

It is not possible to disable the frame time-out and tailing bit error counters. Setting value 0 in HSR counters (HSR_COUNTERS_Pp[23:20]TB = 0x0 and HSR_COUNTERS_Pp[19:0]FT = 0x0) disables those counters, whereas errors keep being generated with this value.

In transient setup phases where TX and RX data rates are still not aligned, false errors may be reported by HSR. Because HSR halts the reception upon an error (until the error is acknowledged) communication will be broken. In such circumstances, inability to disable error detection may be a critical problem.

WORKAROUND

To disable error reporting:

- Set HSR_COUNTERS_Pp[19:0] FT counter to max value (0xFFFFF)
- Set HSR_COUNTERS_Pp[23:20] TB error to min value (0x0)

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.24 McPDM/DMIC Issue With Software Reset With SW_xx_RST

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i653

CRITICALITY

Medium

DESCRIPTION

When transferring a data on McPDM uplink path, if the McPDM uplink path is reset by MCPDM_CTRL.SW_UP_RST, uplink FIFO is correctly reset but the dma pending signal is kept asserted. This can result in an invalid access by the host DMA to uplink FIFO.

The same applies to DMIC if reset by DMIC_CTRL.SW_DMIC_RST.

WORKAROUND

Follow the programming model below to disable and enable the channels:

- Disable the channels:
  - Set the MCPDM_CTRL.SW_xx_RST bit to 1.
  - Disable all channels.
  - Set the MCPDM_CTRL.SW_xx_RST bit to 0.
- Enable the channels:
  - Set the MCPDM_CTRL.SW_xx_RST bit to 1
  - Enable necessary channels.
  - Set the MCPDM_CTRL.SW_xx_RST bit to 0.

Note: SW_xx_RST is either MCPDM_CTRL_SW_UP_RST, CPDM_CTRL_SW_DN_RST, or DMIC_CTRL.SW_DMIC_RST.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.25 UART: Extra Assertion of UARTi_DMA_TX Request

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i659

CRITICALITY

Medium

DESCRIPTION

UART TX with a DMA THRESHOLD default configuration of 64 bytes would result in extra DMA Req assertion when FIFO tx_full is switched from high to low.

This is because of the TX THRESHOLD added in ES2.0 compared to ES1.0.

WORKAROUND

Use TX_THRESHOLD+TRIGGER_LEVEL <= 63 (TX FIFO Size - 1).

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.26 USB OTG Software Initiated ULPI Accesses To PHY Registers Can Halt the Bus

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i661

CRITICALITY

Medium

DESCRIPTION

Software initiated read/write accesses to the PHY ULPI registers (that is, when using USB OTG ULPIReg registers) may be wrongly mixed up with USB OTG Tx traffic. Due to this corruption the USB OTG will detect a Vbus error or a Babble error (logged in IntrUSB register), and halts the communication.

Hardware initiated accesses to the PHY ULPI registers are not impacted because they occur during connect, disconnect, suspend, and resume, when there is no USB traffic. Only software initiated accesses are impacted, and only when there is on-going USB Tx transfers.(including SOF in host mode) Software initiated accesses during connect, disconnect, suspend, and resume are not impacted. Host and peripheral modes are impacted.

WORKAROUND

If possible do not use software initiated reads/writes to access the PHY ULPI registers. Depending on the PHY, there may be a possibility to access these registers by I2C.

If the USB OTG is host, another workaround consist in putting the bus in suspend mode with low-power mode disabled when willing to read/write an ULPI PHY register:

- Disable PHY low-power mode (Power:EnableSuspendM=0)
- Execute USB SUSPEND.
- Do the ULPI register read/write
- Execute USB RESUME
- Restore Power:EnableSuspendM.

If the USB OTG is peripheral, another workaround consists in using the 1-2us time frame after reception of SOF, before any transfer begins on the bus:

- Enable the SOF interrupt
- Program the ULPIReg registers except the ULPIRegControl:D0 bit
- When the SOF interrupt fires, set the ULPIRegControl:D0 bit to make the access
- Disable the SOF interrupt

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.27 ISS-SIMCOP: ISS-LSC Not Transparent After Prefetch Error Event

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i662

CRITICALITY

Low

DESCRIPTION

The prefetch error event (PREFETCH_ERROR) is triggered when the gain table is read too slowly from SDRAM. When this event is pending the module should go into transparent mode, meaning LSC should copy input pixels to output pixels (output=input). Actually, when the prefetch error event occurs the LSC module outputs black pixels.

WORKAROUND

None

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.28 UART: In an RX Wake-up Mechanism, the First Received Character Can be Lost

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i676

CRITICALITY

Medium

DESCRIPTION

When an RX wake-up mechanism is used for the UART module, the first character received can be lost.

WORKAROUND

This is a known behavior and is dependant on the speed of response of the PRCM module to a wakeup. The CTS wake-up mechanism should be preferred when it is possible.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.29 Platform Hangs When CPU Tries To Configure The EMIF Firewall

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i677

CRITICALITY

High

DESCRIPTION

The issue occurs during concurrent accesses of CPU0 and CPU1 as described below. If one CPU fetches code from external RAM while the other CPU requires the access to the EMIF firewall (configuring its register REGUPDATE_CONTROL), then both CPUs hang.

The issue occurs because when REGUPDATE_CONTROL.BUSY_REQ is activated, the interconnect blocks the accesses. Because the two CPUs of the MPUSS use the same bridge before the L3 interconnect, this bridge is saturated if one CPU is accessing external RAM.

WORKAROUND

The workaround is to make sure that the other CPU is not doing external accesses through EMIF when a CPU is updating the EMIF firewall.

The issue does not occur with the other initiators because they do not share the bridge before the L3 interconnect.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.30 DDR PHY Must be Reset After Leaving OSWR

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i682

CRITICALITY

Low

DESCRIPTION

If bus keeper mode is used (programmed through CONTROL_LPDDR2IO*_*.LPDDR2IO*_GR*_WD) after leaving open switch retention, it is necessary to reset the DDR PHY. Otherwise the LPDDR2 memory cannot be accessed.

WORKAROUND

If bus keeper mode is used, issue a PHY reset after leaving OSWR, set bit [10] to 1 at the following address (using read modify write to this register to keep other bits):

- Assert PHY reset for EMIF1 @ x 4C00 0060
- Assert PHY reset for EMIF2 @ x 4D00 0060

Because this resets the command line, this reset must be done when memory is in self-refresh mode.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.31 Async Bridge Corruption

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i688

CRITICALITY

Medium

DESCRIPTION

If data is stalled inside an asynchronous bridge because of back pressure, it may be accepted multiple times, thus creating pointer misalignment that corrupts next transfers on that data path until the next reset of the system (no recovery procedure once the issue is hit, the path remains consistently broken).

The async bridge can be found on the path between MPU to L3 interconnect (to EMIF) and Cortex M3 to L3 interconnect (to EMIF).

In the OMAP4460 and OMAP4470 devices, direct path from MPU to EMIF (through memory adapter in MPU-SS) is replacing MPU-to-DMM path, which was taking place in the OMAP4430. Hence, in an OMAP4460 or OMAP4470 device, this bug is not impacting the direct path from MPU to EMIF (through memory adapter in MPU-SS).

This situation can happen only when the idle is initiated by a master request disconnection (which is trigged by software when executing WFI).

WORKAROUND

All the initiators connected through async bridge must ensure that data path is properly drained before issuing WFI. This condition is met if one strongly ordered access is performed to the target right before executing the WFI.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.32 Keyboard Key Up Event Can Be Missed

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i689

CRITICALITY

Medium

DESCRIPTION

When a key is released for a time shorter than the debounce time, in-between 2 key press (KP1 and KP2), the keyboard state machine will go to idle mode and will never detect the key release (after KP1, and also after KP2), and thus will never generate a new IRQ indicating the key release.

From the operating system standpoint, only a key press as been detected, and the key will keep on being printed on the screen until another or the same key is pressed again.

When the failing state has been reached, the KBD_STATEMACHINE register will show "idle state" and the KBD_FULLCODE register won't be empty, this is the signature of the bug.There is no impact on the power consumption of the system as the state machine goes to IDLE state.

WORKAROUND

First thing is to program the debounce time correctly:

If X (us) is the maximum time of bounces when a key is pressed or released, and Y (us) is the minimum time of a key release that is expected to be detected, then the debounce time should be set to a value in-between X and Y.

In case it is still possible to get shorter than debounce time key-release events, then the only solution is to implement a software workaround:

Before printing a second character on the screen, the software must check if the keyboard has hit the failing condition (cf signature of the bug above) or if the key is still really pressed and then take the appropriate actions.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.33 L2 Cache Corruption Issue

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i690

CRITICALITY

High

DESCRIPTION

Due to a design issue of power control signals of the L2 Cache, the content of the memory can be corrupted.

WORKAROUND

No SW workaround.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Not impacted

1.34 USB HOST - Impossible To Attach a FS Device To An EHCI Port. Handoff To OHCI Is Not Functional

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i692

CRITICALITY

Low

DESCRIPTION

It is not possible to perform USB transactions with a FS device on port USB_B1/B2.

EHCI is able to detect the device, reset it and find that it is a FS device. SW will then hand off the port to OHCI by setting PORTSC[5]:PO (PORT OWNER) bit.

OHCI is able to detect the connection, but then cannot communicate with the device.

When the PHY switches to FsLsSerialMode, the ULPI DIR signal will go to 1 forever.

In HS mode, if DIR is 1, then the ULPI DATA switch to "input only" mode. This input only configuration is wrongly kept after switching to FsLsSerialMode, hence USB transactions cannot occur.

Attaching a FS device directly to an OHCI port is working fine.

WORKAROUND

Only attach FS devices to OHCI ports, or use a HS hub to interface between EHCI ports and LS/FS/HS devices.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.35 USB HOST EHCI - Port Resume Fails On Second Resume Iteration

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i693

CRITICALITY

Low

DESCRIPTION

When entering USB suspend mode, the EHCI will automatically ask the PHY to enter low power mode (PHY function control register bit suspendM is reset).

The PHY will then cut the ULPI_CLK after a minimum of 5 clock cycles.(no maximum specified).

On the other hand, the EHCI embeds a counter counting up to 18 before cutting the internal clock after suspend signal is asserted.

Since the PHY cuts the clock prematurely, the counter is not reaching 18. However, the first suspend and resume will work correctly.

At the second suspend sequence, since the counter has maintained the value (thanks to retention flops), the counter reaches 18 and cuts the clock internally.

As a consequence, the internal state machine does not transition to the correct state causing the next resume to fail.

Both host initiated resume and remote wakeup are impacted by this issue.

WORKAROUND

After setting the suspend bit, switch the internal clock supply from the external ULPI_CLK provided by the PHY to the internal 60 MHz clock.

This will allow the internal counter to reach 18. Then after 1ms, switch back to the external ULPI_CLK. This switch can be done thanks to the CM_L3INIT_HSUSBHOST_CLKCTRL[25:24]:CLKSEL_UTMI_P1/2 bits.

During the application of the WA, the CM_L3INIT_HSUSBHOST_CLKCTRL[9:8]OPTFCLKEN_UTMI_P1/2_CLK optional clocks need to be enabled.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.36 System I2C hang due to miss of Bus Clear support

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i694

CRITICALITY

Low

DESCRIPTION

There is no H/W mechanism preventing violating below I2C Bus clear standard requirement.

If the data line (SDA) is stuck LOW, the master should send 9 clock pulses. The device that held the bus LOW should release it sometime within those 9 clocks. If not, then use the HW reset or cycle power to clear the bus.

Sys_Warmreset doesn't reset the I2C IP at Phoenix level, it does at IC level.

Resetting the IP at Phoenix PMIC would avoid such situation, but this is partial answer as many other I2C slave devices could be addressed during Warm reset without any sensitivity to this sys_warmreset pin.

No other reset source possible at Phoenix level to reset the I2C controller (only Cold Reset).

So, once the situation is reached, IC is seeing bus busy status bit.

WORKAROUND

I2C SW handler could be programmed to detect such a locked situation. In this case, it will check the Bus Busy bit and issue the needed clock pulses.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.37 HSI: Issues In Suspending and Resuming Communication (HSR and HST)

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i695

CRITICALITY

Medium

DESCRIPTION

There are some fails while suspending then resuming on going HSI communication on both HST and HSR initiatives.

If this is the HST initiative:

1. It is possible to suspend then resume communication by disabling then enabling active HST FIFOs through HST_MAPPINGf [0] ENABLE bit. Transmission stops as soon as TX FIFO is disabled (ENABLE bit equal to 0x0) and resumes as soon as TX FIFO is re-enabled (ENABLE bit equal to 0x1).
2. It is not possible to suspend then resume safely by setting HST mode to SLEEP. Writing HST_MODE_Pp[1:0] MODE_VAL = 0x0 (SLEEP) does not have any impact on transmission that continues.

If it is the HSR initiative:

1. It is not possible to suspend then resume communication by disabling then enabling active HSR FIFOs through HSR_MAPPINGf [0] ENABLE bit. Disabling the RX FIFO does not stop the transmission (by dropping the READY line). The data keeps being sent by HST and HSR simply discards it. By the way, no RX mapping error is generated. Transmission did not actually stop and frame is lost by HSR.
2. It is not possible to suspend then resume safely by setting HSR mode to SLEEP. Writing HSR_MODE_Pp[1:0] MODE_VAL = 0x0 (SLEEP) stops any ongoing transfer unconditionally which may result in loss of frame(s) once the transfer is resumed.

WORKAROUND

If this is the HST initiative:

It is not possible to configure MODE_VAL bit to SLEEP with active data transfers because it has no impact.

The only way to suspend then resuming a HSI communication with HST is to disable then re-enables active TX FIFOs.

If this is the HSR initiative:

There is no way to suspend then resume the receiver without data loss.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.38 HSI: Issue with SW reset

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i696

CRITICALITY

Low

DESCRIPTION

There is a bug in HSI IP;once the SW reset bit is set through the HSI_SYSCONFIG[1] SOFTRESET bit, the SW reset is not propagated well if there is an on-going reception.

If the reception never ends (synchronization loss, interrupted transmission from transmitter...), then this is a deadlock, the SW reset is not propagated and there is no OCP access possible.

WORKAROUND

Use the HW reset from the PRCM instead of the local SW reset.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.39 DMA4 generates unexpected transaction on WR port

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i698

CRITICALITY

Medium

DESCRIPTION

The DMA4 channel generates an unexpected transaction on WR port under the following 2 scenarios :

- Scenario 1
  1. Software synchronization : Bit fields SYNCHRO_CONTROL and SYNCHRO_CONTROL_UPPER are set to 0 in register DMA4_CCRi

     Channel element number : Bit field CHANNEL_ELMNT_NBR is set to 0x9 in register DMA4_CENi

     Channel frame number : Bit field CHANNEL_FRAME_NBR is set to 0x1 in register DMA4_CFNi

     Element size : Bit field DATA_TYPE is set to 0x2 in register DMA4_CSDPi

     Destination addressing mode : Bit field DST_AMODE is set to 0x1 in register DMA4_CCRi

     Destination is packed : Bit field DST_PACKED is set to 0x1 in register DMA4_CSDPi

     Destination endianism : Bit field DST_ENDIAN is set to 0x0 in register DMA4_CSDPi

     Destination burst enable : Bit field DST_BURST_EN is set to 0x1 in register DMA4_CSDPi

     Destination start address : Register DMA4_CDSAi is set to 0xabcd0000

     Disable graphics operation : Bit fields CONSTANT_FILL_ENABLE and TRANSPARENT_COPY_ENABLE are set to 0x0 in register DMA4_CCRi

     The channel has got an ERR response on the WR port before the end of block transfer. The channel has gone for clean abort and got disabled. The same channel has been configured with soft-sync and included in the channel chaining (This channel is not the head of the chain). When this channel gets enabled through the link, the channel is writing the data out as soon as it fetches the data from Read side. It is expected that the channel should go with burst transfer, but it is going for single transfers

     This results in a performance issue as DMA is executing single transfers instead of burst transfers. This performance issue is also observed while using the channel with destination synchronization and prefetch enabled.
  2. Destination sync with Prefetch enabled : Bit field SEL_SRC_DST_SYNC is set to 0x0 ; Bit fields SYNCRO_CONTROL_UPPER and SYNCRO_CONTROL should not be set to 0x0 ; Bit field PREFETCH is set to 0x1 in register DMA4_CCRi The other settings remain same as in use case #a described above
- Scenario 2

  The channel has got an ERR response on the WR port before the end of block transfer. The channel has gone for clean abort and got disabled. The same channel has been configured with destination-sync with prefetch enabled and included in the channel chaining (This channel is not the head of the chain). When this channel gets enabled through the link, the read port will start its transaction. If the HWR request to this channel comes before the channel gets its first response, the channel will start a WR transaction with byte enable 0. Also, the internal data counters get updated and the corresponding data will never come out of DMA4. The Data FIFO locations are also not recovered.

  This results in a Data Integrity issue.

WORKAROUND

There is a software workaround to solve this issue

1. Work around to resolve both Data Integrity and Performance issue :

- Dummy enable-disable for an aborted Channel. i.e. On abort, configure the channel as soft sync with No of frames = 0 and enable the channel by writing 0x1 into the ENABLE bitfield of register DMA4_CCRi. Wait for the Address Misaligment Interrupt. The channel is now ready for reuse.
- Ensure that clean drain happens for a channel that is or is to be used as part of a channel chain. i.e. ensure that the abort conditions never occur for this channel
- If a channel gets aborted, do not reuse the channel in a chain
- Don't use channel chaining

2. Work around to resolve the data integrity only.

   Disable prefetch in all channels that are part of a channel chain

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.40 DMA4 channel fails to continue with descriptor load when Pause bit is cleared

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i699

CRITICALITY

Low

DESCRIPTION

This Bug can occur only in a channel that is part of a channel chain. If channel chaining is not used, this bug is never seen.

An exact corner case sequence of events must occur. The sequence is:

- The channel is enabled and then aborted*.
- This same channel is now configured as part of a channel chain (it should not be the head of the channel chain).
- The channel is configured as "software synchronized" or "hardware synchronized at destination with prefetch enabled"
- The channel gets enabled through linking.

* Following is the subset of abort conditions for this scenario:

- The channel is disabled in the middle of transaction and channnel is not a drain candidate.
- The channel gets a transaction error on write port but not at the end-of-block transaction.
- The channel gets a read transaction error and is not a drain candidate.

WORKAROUND

The software workaround is to configure DMA4 to be in no-standby or force-standby mode before clearing the PAUSE bit. The DMA4 can be reverted back to smart-standby mode after a certain period (after detecting DMA4_CSR[15:15] of corresponding channel to be 0 or ensuring DMA4_CCR[7:7] bit of corresponding channel to be 0. This ensures descriptor load completion or channel termination.)

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.41 MPU clock glitches at OPP change

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i700

CRITICALITY

High

DESCRIPTION

CPU random hang can happen during 1.2 and 1.5 GHz OPP changes. Hang are due to MPU clock glitch or shrink pulses created at DPLL MPU enable/disable with DCC (Duty Cycle Correction) used.

DCC is required for DPLL lock frequency higher than 2Ghz.

OPPs lower than 920 MHz use DPLL clock divided by 2, DCC is not used and so there is no issue at OPP change.

1.2 and 1.5GHz OPPs use the direct clock output from the DPLL and so this clock passes through a Duty Cycle Corrector. Random hang can happen at OPP change.

Enable signal of DCC from the PRCM is not resynchronized with the output clock of the DCC and so glitches can occur at the output of the clock switch when enable signal toggles. This can create hang of the system.

WORKAROUND

The Software should lock the DPLL at 2 x the OPP frequency and disable the DCC for all OPPs:

- Locking MPU DPLL at 2.4GHz for 1.2GHz unitsand at 3GHz for 1.5GHz units. (See the table below for DPLL_MPU recommended settings.) As DM never mentioned DCC used, these lock frequencies are already documented.
- Disabling DCC: CM_CLKSEL_DPLL_MPU[22] DCC_EN=0.

Table 1-2. DPLL_MPU Recommended Settings

SysClk (MHz)	MPU OPPs		MPU DPLL			MPU			
	OPPs	VDD_MPU (V)	DPLL locked Freq (MHz)	M	N	M2		M3	MPU Actual Freq (MHz)
38.4	NITRO+SB	1.35	2995.2	39	0	1	Use M2 Output	0	1497.6
	NITRO	1.35	2400	125	3	1		0	1200
26	NITRO+SB	1.35	2998.7	173	2	1	Use M2 Output	0	1499.3
	NITRO	1.35	2402.4	231	4	1		0	1201.2
19.2	NITRO+SB	1.35	2995.2	78	0	1	Use M2 Output	0	1497.6
	NITRO	1.35	2400	125	1	1		0	1200
16.8	NITRO+SB	1.35	3001.6	268	2	1	Use M2 Output	0	1500.8
	NITRO	1.35	2402.4	143	1	1		0	1201.2
12	NITRO+SB	1.35	3000	125	0	1	Use M2 Output	0	1500
	NITRO	1.35	2400	100	0	1		0	1200

Units are trimmed in production to support those frequencies, new trimming bits are added to give this information: CONTROL_STD_FUSE_OPP_DPLL_1 [19:18] = 00 for 2Ghz, 01 for 2.4GHz and 11 for 3GHz.

For material trimmed at 2.0GHz only (CONTROL_STD_FUSE_OPP_DPLL_1[19:18] = 00), trimming override at a fix value is required to achieved performances at 2.4 and 3Ghz (write 0x29 in register CONTROL_DPLL_NWELL_TRIM_0). This trimming override is needed only for non production material.

The new trimming bits CONTROL_STD_FUSE_OPP_DPLL_1 [19:18] will not give information of silicon performance type. To know the silicon performance type software sill need to read STD_FUSE_PROD_ID_1[17:16] SILICON_TYPE.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.42 HSI: DSP Swakeup generated is the same than MPU Swakeup. System can't enter in off mode due to the DSP.

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i702

CRITICALITY

High

DESCRIPTION

There is a silicon bug in HSI IP.

The wakeup dependency from HSI towards DSP is by default enabled and the register bit controlling this dependency is read only. There is no option to disable this dependency.

As a result when the MPU Wakeup is generated, a false DSP wakeup is also generated.

When below scenario happens:

1. Modem interface (HSI is enabled)
2. The system is allowed to suspend
3. When CAWAKE signal has activity, it will wake-up MPU; it also wakes up DSP incorrectly.

Consequences of this bug in previous scenario is

4. The DSP is not able to handle this wake up correctly
5. Next suspend, system can't enter in off-mode because DSP remains active

WORKAROUND

- While in the suspend path:
  1. DSP is forced through SW to wake-up: - CM_DSP_CLKSTCTRL [1:0] CLKTRCTRL = 0x2
  2. When CAWAKE signal has an activity, it will wake-up MPU and DSP; the DSP domain becomes active
  3. Program DSP through SW to transition to low power state: change the HW_AUTO, sleep and wake up are based upon hardware conditions - CM_DSP_CLKSTCTRL [1:0] CLKTRCTRL = 0x3
- This will forcefully clear DSP wakeup-gen and will allow DSP to go idle.
- No impact of this workaround on power/performance is seen after doing measurements

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.43 CBUFF Ready Window Event in Write Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i708

CRITICALITY

Low

DESCRIPTION

The next CBUFF ready window event (IRQ_CTXx_READY) is generated once CPU clears the CBUFF ready (IRQ_CTXx_READY)and after the CPU writes in the current ended window (setting the CBUFF_CTX_CTRL_i [10] DONE bit to 0x1).

WORKAROUND

The number of CBUFF windows to use in write mode for a given context is two windows.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.44 CSI-2 Receiver Executes Software Reset Unconditionally

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i709

CRITICALITY

Low

DESCRIPTION

Ongoing transactions may be interrupted when a software reset is performed while there is still active traffic generated by the CSI-2 receiver. Interruption of ongoing transactions typically leads to a general OMAP hang that can only be recovered by a device reset.

WORKAROUND

Software must ensure that there is no ongoing traffic before performing a software reset. In particular, the CSI-2 receiver must be reset to resume normal operation after a CSI-2 FIFO overflow. There may be remaining data in the FIFO, and therefore ongoing traffic, when the software driver receives the overflow interrupt. To avoid creating a system hang, software must either:

- Wait for several 1000s of L3 cycles before performing the software reset after an overflow or
- Use the ISS level software reset

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.45 USB Host TLL Bit-stuffing Feature Is Broken

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i710

CRITICALITY

High

DESCRIPTION

The TLL bit-stuffing emulation feature (enabled by default after reset in the TLL_CHANNEL_CONF_i[11] ULPINOBITSTUFF bit) is broken. It must be disabled, that is, bit-stuffing must be disabled on all enabled TLL channels.

However, disabling bit-stuffing on a TLL channel induces an asymmetry in the number of transmitted bits between the TLL channel and the other ports (ULPI or HSIC), which may result in an underrun or overrun errors. This could be the case while transferring data pattern where bit-stuffing is heavily used, like a white image (full of 11111...).

WORKAROUND

Disable TLL bit-stuffing on all enabled TLL channels: TLL_CHANNEL_CONF_i[11] ULPINOBITSTUFF = 1 and do not use at the same time one TLL port and one ULPI port or one HSIC port.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.46 ISP H3A Hangs Due to Unstable Vertical Sync Signal

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i712

CRITICALITY

Low

DESCRIPTION

If unexpected VD, Start of frame signal, caused by noise comes before finishing the previous frame statistics, the H3A module hangs.

WORKAROUND

ISP full reset is necessary to exit from H3A hang state.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.47 GPIO IRQ Not Generated After MPU Idle if IRQSTATUS Bits Not Cleared

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i714

CRITICALITY

Medium

DESCRIPTION

After the GPIO is configured in smart-idle (or smart-idle with wake-up) and the system goes into MPU inactive mode (idle), the GPIO does not generate any IRQ again if any of the register bits of both interrupt line raw status registers (GPIO_IRQSTATUS_RAW_0 or GPIO_IRQSTATUS_RAW_1) is set. In the case of a GPIO configured in smart-idle wake-up mode (GPIO_SYSCONFIG[4:3]=0x3), the wake-up associated to the GPIO IRQ event will not even occur.

WORKAROUND

Note: In the below paragraph, 'x' stands for 0 or 1 being the 1st interrupt to be handled, either MPU or DSP, 'y' refers to the other interrupt line.

Upon an interrupt reported through GPIO_IRQSTATUS_x, do the following:

- Read out GPIO_IRQSTATUS_x => status_value_x
- Write status_value_x to GPIO_IRQSTATUS_x (clear the enabled status bits)
- Read out GPIO_IRQSTATUS_SET_y=> enable_value_y
- Write status_value_x and NOT enable_value_y to GPIO_IRQSTATUS_y

By doing so, user clears the unused interrupt status bits for the other interrupt line.

An extension to this workaround is to clear GPIO_IRQSTATUS_y (all the bits) when the corresponding interrupt line (most of the time the DSP, that is, 2nd interrupt line) is not used, at each time GPIO_IRQSTATUS_x is cleared.

Note: Clearing GPIO_IRQSTATUS_0 (respectively 1) is done by writing 0xFFFFFFFF to this register. It will automatically clear GPIO_IRQSTATUS_RAW_0 (respectively 1) consequently.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.48 DSI PLL Signal is Not available on Hardware Observability Pads

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i716

CRITICALITY

Low

DESCRIPTION

When DSI PLL is under locking, SYS_CLK can be observed on the hardware observability but once PLL is locked the hardware observability signal does not change and still show SYS_CLOCK. DSI PLL is not available on hardware observability.

WORKAROUND

No workaround is available.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.49 Blending Calculation Error When Premultiply Alpha is Used

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i717

CRITICALITY

Low

DESCRIPTION

The equation for layer blending when upper layer is a premultiplied with a global alpha:

LYR(result) = A(global) * LYR(upper) + (1 -“ (A(global) * A(pixel))) * LYR(lower)

Where:

- A(global) is alpha of upper layer
- A(pixel) is pixel alpha of upper layer
- (1 -“ (A(global) * A(pixel))) is the first complement of A(global * A(pixel))
- When A(global) = 0

  P(result) should be P(lower). Calculation leads to 0xff * P(lower) which can have 1-bit error if P(lower) > (full range)/2 (0x80 for 8-bit)
- When A(global) = 0xff

  P(result) should be P(upper). Calculation leads to 0xff * P(upper) + (1-A(pixel)) * P(lower)

For example, 8-bit multiplication-with-rounding leading to 1-bit error in case Operand > (full range) / 2.

0x8c * 0xff = 0x8B74 final resulting after rounding is 0x8B instead of 0x8C.

WORKAROUND

No workaround is available.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.50 HS USB: Multiple OFF Mode Transitions Introduce Corruption

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i719

CRITICALITY

Medium

DESCRIPTION

When the system enters off mode, the save-and-restore (SAR) process comes into play. During the save sequence, the USB host content must be saved (even if the module was not in use). The saved content is automatically restored upon the next wakeup from off mode.

When the save of the USB context occurs, an extra pulse of UTMI_root clock coming from USB DPLL is entering the IP, and generates a minor corruption. This corrupted context is saved and restored later. Upon each save thereafter, the corrupted context is corrupted further. This is a cumulative process. At least three consecutive saves (with no wakeup of USB in-between) are needed for introducing a fatal corruption.

This corruption will impact the next use of the USB module: it could be while resuming a suspended device, or it could be upon the enumeration of a new device. The exact failure is not predictable: disconnection or stalls have been observed.

TLL and external PHY modes are impacted.

WORKAROUND

The workaround is to only perform the SAR-save of the USB registers if the USB bus has been resumed since the last wakeup from OFF mode.

If the USB has been left untouched in-between the previous wakeup from OFF, and the next OFF mode entry, then do not perform the USB registers SAR-save. (However the regular SAR-save is still needed for PRCM and other registers. Just skip the USB part)

By doing so, the SAR-restore process is always restoring valid data.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.51 DSS Block in "Idle Transition" State when using RFBI I/F

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i722

CRITICALITY

Medium

DESCRIPTION

DISPC and RFBI are configured in smart-idle mode. After sending an image to the panel through the RFBI interface, the DISPC end-of-frame interrupt and RFBI end of transfer occur. After software sets the DSS in off state but no off state is not reached, DSS CM stays in idle transition, CM_DSS_DSS_CLKCTRL[17:16] IDLEST = 0x1 because RFBI is not acknowledging idle request.

WORKAROUND

After transfer of image completes, set the RFBI mode into bypass mode by setting the DISPC_CONTROL1[16] GPOUT1 and DISPC_CONTROL1[15] GPOUT0 bits to 0x1.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.52 Deadlock Between SmartReflex™ and Voltage Processor

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i724

CRITICALITY

High

DESCRIPTION

A protocol violation between SmartReflex and voltage processor can happen when a global warm reset occurs during a transaction. Consequences are:

- VP_xx_TRANXDONE_ST interrupt from the PRCM is no longer generated when a force update voltage from VP is performed.
- SmartReflex does not request voltage change anymore.

SmartReflex and voltage processor have a handshake protocol. SmartReflex indicates to voltage processor when voltage update is valid. Voltage processor acknowledges this request. Protocol violation appears when warm reset is asserted before acknowledge. This is because SmartReflex is warm reset-sensitive while voltage processor is cold reset-sensitive.

WORKAROUND

SmartReflex must be disabled before a software-controlled warm reset.

For other warm resets, the issue cannot be avoided, but during reboot the following sequence can be performed to recover:

- Initiate a Force Update and check TRANXDONE interrupt success (optional). If it is not successful then:
- Initiate a software global cold reset.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.53 Refresh Rate Issue After Warm Reset

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i727

CRITICALITY

Medium

DESCRIPTION

The refresh rate is programmed in the EMIF_SDRAM_REF_CTRL[15:0] REG_REFRESH_RATE parameter taking into account frequency of the device.

When a warm reset is applied on the system, the OMAP processor restarts with another frequency and so the frequency is not the same. Due to this frequency change, the refresh rate will be too low and could result in an unexpected behavior on the memory side.

WORKAROUND

The workaround is to force self-refresh when coming back from the warm reset with the following sequence:

- Set EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE to 0x2
- Set EMIF_PWR_MGMT_CTRL[7:4] REG_SR_TIM to 0x0
- Do a dummy read (loads automatically new value of sr_tim)

This will reduce the risk of memory content corruption, but memory content can't be guaranteed after a warm reset.

When OMAP is back to active mode with correct OPP configuration, EMIF registers need to be re-program according to the OPP and respect workaround for i735 bug.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.54 System May Hang During EMIF Frequency Change

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i728

CRITICALITY

Medium

DESCRIPTION

When the EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field is set to 0x2, self-refresh mode is activated. In that case, EMIF puts the SDRAM into self-refresh mode if no access is performed during EMIF_PWR_MGMT_CTRL[7:4] REG_SR_TIM number of DDR clock cycles.

If during a small window the following three events occur:

- The EMIF_PWR_MGMT_CTRL[7:4] REG_SR_TIM counter expires
- And frequency update is requested (CM_SHADOW_FREQ_CONFIG1[0] FREQ_UPDATE set to 1)
- And OCP access is requested

Then it causes unstable clock on the DDR interface.

WORKAROUND

To avoid the occurrence of the three events, the workaround is to disable the self-refresh when requesting a frequency change.

Before requesting a frequency change the software must program EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE to 0x0.

When the frequency change has been done, the software can reprogram EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE to 0x2.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.55 DDR Access Hang After Warm Reset

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i729

CRITICALITY

Medium

DESCRIPTION

When the EMIF is going in IDLE state and the following three events occur:

- Frequency update is requested (CM_SHADOW_FREQ_CONFIG1[0] FREQ_UPDATE set to 1).
- And a warm reset occurs.
- And a system access is requested.

Then the EMIF will not properly reset internal FIFO. The EMIF may answer to the request when returning from reset not expected by the system; it creates protocol error or data corruption.

WORKAROUND

In case of software warm reset, software can check that no frequency change is ongoing before initiating the warm reset.

In case of watchdog timer reset, there is no workaround to recover, a cold reset is needed.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.56 DSS Configuration Registers Access Through the L4 Interconnect

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i733

CRITICALITY

High

DESCRIPTION

Due to wrong timings, all register accesses transitioning through the L4 interconnect toward DSS are not reliable.

DSS registers access done through the L4 interconnect are not supported

WORKAROUND

DSS register access should be addressed through the L3 interconnect.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.57 LCD1 Gamma Correction Is Not Working When GFX Pipe Is Disabled

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i734

CRITICALITY

High

DESCRIPTION

LCD1 output supports gamma correction. The color look-up table (CLUT) is shared between the BITMAP to RGB conversion module on GFX pipeline and Gamma correction on the LCD1 output. LUT table can be loaded by SW through DISPC slave port (interconnect) or by DISPC master port using the DISPC DMA.

However, LCD1 gamma correction LUT loading is not working properly and require to enable GFX pipeline for LUT loading. Depending on the load mode (DISPC_CONFIG1[2:1] LOADMODE) used, GFX pipeline can then be disabled after 1st frame.

WORKAROUND

There are two workaround treatments depends on the load mode for gamma correction LUT and frame data (see Table x-xx Workaround/Load mode settings)

Table 1-3. Workaround/Load mode settings

Load Mode (DISPC_CONFIG1[2:1]LOADMODE)	GFX Enable Condition	Workaround
0x0 (load LUT and data every frame)	Always Enabled	WA1
0x1 (load LUT for first frame and change loadmode to 2)	Enable required for first frame only	WA2
0x2 (load frame data only)	Enable required for first frame only.	WA2
0x3 (load LUT and data for first frame and change loadmode to 2)	Enable required for first frame only.	WA2

WA1

To use gamma correction on LCD1 output, software must:

1. Enable the GFX pipeline by setting DISPC_GFX_ATTRIBUTES[0] ENABLE to 0x1.
2. Set the GFX base address (DISPC_GFX_BA_i[31:0] BA) to an accessible frame buffer.
3. Set the GFX window to minimum size by configuring the DISPC_GFX_SIZE[27:16] SIZEY and DISPC_GFX_SIZE[11:0] SIZEX bits.
4. If the GFX pipeline is not to be displayed, set GFX LYR to bottom LYR in LCD1 overlay by setting appropriate DISPC_GFX_ATTRIBUTES[27:26] ZORDER bit field and make GFX fully transparent by setting the global alpha of the GFX to 0x00 in the DISPC_GLOBAL_ALPHA[7:0] GFXGLOBALALPHA bit field.

WA2

To use gamma correction on LCD1 output, software must:

1. Enable the GFX pipeline by setting DISPC_GFX_ATTRIBUTES[0] ENABLE to 0x1.
2. Set the GFX base address (DISPC_GFX_BA_i[31:0] BA) to an accessible frame buffer.
3. Set the GFX window to minimum size by configuring the DISPC_GFX_SIZE[27:16] SIZEY and DISPC_GFX_SIZE[11:0] SIZEX bits.
4. If the GFX pipeline is not to be displayed, set GFX LYR to bottom LYR in LCD1 overlay by setting appropriate DISPC_GFX_ATTRIBUTES[27:26] ZORDER bit field and make GFX fully transparent by setting the global alpha of the GFX to 0x00 in the DISPC_GLOBAL_ALPHA[7:0] GFXGLOBALALPHA bit field.
5. When DISPC_IRQSTATUS[8]PALETTEGAMMALOADING_IRQ =0x1 then disable GFX pipeline

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.58 Power Management Timer Value For Self-Refresh (SR_TIM)

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i735

CRITICALITY

High

DESCRIPTION

LPDDR2 memories could be put in self-refresh mode for power savings. The number of cycles after which EMIF can start a self-refresh entry is software programmable (thanks to the power management timer for self-refresh: EMIF_PWR_MGMT_CTRL[7:4] REG_SR_TIM register bit field).

When exiting self-refresh mode, it is required that at least one refresh command is issued before entry into a subsequent self-refresh (as defined in the JEDEC LPDDR2 Specification)

When this timer value is set to a value less than 0x6 (for VDD_CORE_L OPP100) or less than 0x5 (for VDD_CORE_L OPP50), the time between a self-refresh exit to the next immediate self-refresh entry does not allow the EMIF to perform a refresh command.

As a consequence, data in LPDDR2 memory is not refreshed properly, and then data is corrupted in LPDDR2.

WORKAROUND

Using a value of EMIF_PWR_MGMT_CTRL[7:4] REG_SR_TIM >= 6 for VDD_CORE_L OPP100 and a value of REG_SR_TIM >= 5 for VDD_CORE_L OPP50 avoid the occurrence of the issue.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.59 Leakage Increase On LPDDR2 I/Os

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i736

CRITICALITY

Medium

DESCRIPTION

Following a bug in the integration of I/Os cell for LPDDR2 clocks, a leakage increase can be observed on vddca_lpddr2 when OMAP is in open switch retention mode.

WORKAROUND

To prevent an increase in leakage, it is recommended to disable the pull logic for these I/Os except during off mode.

So the default state of the I/Os (to program at boot) will have pull logic disable:
CONTROL_LPDDR2IO1_2[18:17]LPDDR2IO1_GR10_WD = 00
CONTROL_LPDDR2IO2_2[18:17]LPDDR2IO2_GR10_WD = 00

When entering off mode, these I/Os must be configured with pulldown enable:
CONTROL_LPDDR2IO1_2[18:17]LPDDR2IO1_GR10_WD = 10
CONTROL_LPDDR2IO2_2[18:17]LPDDR2IO2_GR10_WD = 10

When resuming from off mode, pull logic must be disabled.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.60 MMC1 Booting May Be Bypassed Depending On VDD Ramp-up Delay

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i739

CRITICALITY

High

DESCRIPTION

If the sys_boot[5:0] pins are configured for booting from MMC1, then the boot on MMC1 may not happen (board dependency) and the ROM code jumps to the next device of the boot sequence.

Indeed, depending on the voltage ramp, the ROM code may not wait long enough for SDMMC1_VDDS voltage to be stabilized at 3 V before checking the voltage level supplied to OMAP.

In that case, the ROM code checks the SDMMC1_VDDS voltage too early, reads a bad level, and then jumps to 1.8-V configuration while the PMIC was configured to 3 V.

The MMC1_PBIAS cell is in a bad state and prevents the sending of commands to the MMC1 bus.

The ROM code switches to the next boot sequence.

WORKAROUND

No

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.61 Disconnect Protocol Violation

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i740

CRITICALITY

High

DESCRIPTION

A bug has been identified in the interconnect agent handling the connect-disconnect protocol between an initiator and interconnect. When the disconnect protocol violation occurs, there is a dead lock and a system lockup is observed.

The issue can occur in a corner case when the impacted module has started a transition to standby, for the L3 initiator on which it is attached, exactly at the time the initiator gets an event for exiting idle state. Such a situation can occur when the impacted initiator is generating short MStandby pulses (pulse durations less than one L4 clock cycle).

DSS and ISS are the only initiators that are impacted.

WORKAROUND

L3_CLK1 must be kept in NO-IDLE when the DSS clock domain is ON. It can be switched back to HW_AUTO when the DSS clock domain is IDLE.

L3_CLK2 must be kept in NO-IDLE when the ISS clock domain is ON. It can be switched back to HW_AUTO when the ISS clock domain is IDLE.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.62 ULPI RxCmds Convey the Wrong ID Bit After Save-and-Restore Sequence

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i754

CRITICALITY

Medium

DESCRIPTION

ULPI RxCmds, from OMAP to USB device, convey the wrong ID bit after the save-and-restore sequence.

When OMAP is in a low-power mode scenario (chip-OFF), in high-speed transceiverless link (TLL) connection, after the SAR phase, every RxCmd from the TLL to the peripheral conveys wrong ID field (for example, 0x0D instead of 0x4D), that is, the ID bit is 0 instead of 1. This is due to the TLL losing the value of ID during the SAR process. As long as the peripheral does not resample the ID (by toggling OTG_CTRL_i[0] IDPULLUP) after the restore, the ID bit keeps the wrong value 0 instead of 1. This results in sending the wrong RxCmd to the peripheral.

Depending on the peripheral device design, it may consider or disregard the ID bit. The behavior and consequences depend on the device design.

WORKAROUND

Ensure that the OTG_CTRL_i [0] IDPULLUP bit is set to 1 before the SAR-save. By doing so, this bit is restored to 1 after every off mode. Then the ID bit is sampled and the Rxcmd is correct.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.63 PRCM Hang at Frequency Update During DVFS

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i755

CRITICALITY

Low

DESCRIPTION

During DVFS transitions, the PRCM controller can hang if CORE DPLL dividers M2 and M5 are updated at once.

WORKAROUND

The recommended sequence is:

- Update CM_SHADOW_FREQ_CONFIG2[7:3]DPLL_CORE_M5_DIV.
- Set CM_SHADOW_FREQ_CONFIG2[0]GPMC_FREQ_UPDATE to 0x1.
- Wait until CM_SHADOW_FREQ_CONFIG2[0]GPMC_FREQ_UPDATE becomes 0x0.
- Update CM_SHADOW_FREQ_CONFIG1[15:11]DPLL_CORE_M2_DIV.
- Set CM_SHADOW_FREQ_CONFIG1[0]FREQ_UPDATE to 0x1.
- Wait until CM_SHADOW_FREQ_CONFIG1[0]FREQ_UPDATE becomes 0x0.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.64 Card Error Interrupt May Not Be Set Sometimes

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i761

CRITICALITY

Medium

DESCRIPTION

Due to a bad behavior of an internal signal, the Card Error interrupt bit MMCHS_STAT[28] CERR may not be set sometimes when an error occurred in the card response.

WORKAROUND

After responses of type R1/R1b for all cards and responses of type R5/R5b/R6 for SD and SDIO cards, software must read two registers: MMCHS_RSP10 and MMCHS_CSRE. When a MMCHS_CSRE[i] bit is set to 1, if the corresponding bit at the same position in the response MMCHS_RSP0[i] is set to 1, the host controller indicates a card error and software should proceed in the same way as if a CERR interrupt would have been detected in the MMCHS_STAT register.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.65 In AutoCMD12 mode, the CMD12 Command Is Not Issued On Write Transfer Completion

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i762

CRITICALITY

Medium

DESCRIPTION

When using AutoCMD12 mode in write transfer with ADMA and MMCHS_CMD[1] BCE is disabled, then the CMD12 command is not issued automatically after write transfer completion.

WORKAROUND

Instead of setting the MMCHS_CMD[2] ACEN bit to 0x1 to enable AutoCMD12 mode, software sends the CMD12 command at the end of write transfers (after the MMCHS_STAT [1] TC bit goes High).

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.66 SRAM LDO Output Voltage Value Software Override in RETENTION is Not Functional

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i764

CRITICALITY

Low

DESCRIPTION

Software override of EFUSE SRAM LDO output voltage value in retention mode is not functional and will have no effect. Retention voltage will be the one set by the EFUSE even if:

CONTROL_LDOSRAM_xxx_VOLTAGE_CTRL[26] LDOSRAMxxx_ RETMODE_MUX _CTRL is set to 1 and CONTROL_LDOSRAM_xxx_VOLTAGE_CTRL[20:16] LDOSRAMxxx_ RETMODE_VSET_OUT contains a valid value.

WORKAROUND

None

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.67 I/O Glitch Issue When Entering Off Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i765

CRITICALITY

Medium

DESCRIPTION

Following a design issue on I/O muxing compiler, a glitch can occur on I/Os when switching them from the active mode to the off-mode override value.

The glitch is present:

- if the feature for pin state override during off mode is used CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y [25,9] OFFMODEENABLE = 1
- and the override value CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[27,11] OFFMODEOUTVALUE = 1 and the IO value when going to off mode was 1.

There is no issue

- if the override feature CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[25,9] OFFMODEENABLE = 0 is not used,
- or if it is used to force a value which is different from the value before going to off mode.
- or if it is used to force a 0 and the value before going to off mode was 0.

WORKAROUND

CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[25,9] OFFMODEENABLE = 1 should not be used on pad output pins driving glitch-sensitive signals if the same value is driven during active mode and off mode and is equal to 1.

If CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[25,9] OFFMODEENABLE = 1, it is necessary to ensure that the CONTROL_(CORE/WKUP)_PAD0_X_PAD1_Y[27,11] OFFMODEOUTVALUE is equal to 0 or is different from the value of the I/Os when going to off mode.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.68 HS USB Host HSIC Remote Wakeup Is Not Functional

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i774

CRITICALITY

Medium

DESCRIPTION

This problem impacts the HS USB Host HSIC interface. TLL and ULPI interfaces are not impacted.

For this issue to occur, the following conditions must exist:

- A USB device is attached to an OMAP HSIC interface.
- The USB bus is suspended.
- The PRCM asserts idle_req, and the USB host answers idle_ack.
- The PRCM hardware automatically stops the interface clocks (ICLK).
- Software disables the module by setting the CM_L3INIT_HSUSBHOST_CLKCTRL[1:0]:MODULEMODE bit fields to 0x0.
- The PRCM automatically stops the mandatory functional clocks (FLCK).
- Software stops the optional FCLK.
- The module is then idle. The clock domain can possibly enter idle, then the power domain also can enter a low-power mode, and even the full OMAP.
- The device generates a remote wakeup.

The USB Host detects the remote wakeup condition asynchronously and generates a USBHOST_SWAKEUP to the PRCM.

The PRCM deasserts idle_req, and restarts ICLK and mandatory FCLK, but not the optional FCLK.

However, in the case of HSIC, the optional FCLK (CM_L3INIT_HSUSBHOST_CLKCTRL[10/9/8].OPTFCLKEN_UTMI_P3/2/1_CLK) is needed to generate the interrupt indicating to the system that the USB HOST is the wake-up source.

Consequently, OMAP is woken up but does not acknowledge who is the wake-up source.

WORKAROUND

Do not rely on the asynchronous wake-up feature of the USB host module, but rather on the daisy-chain for detecting a remote wakeup.

Set the wakeup-enable feature of the HSIC pads and enable the daisy-chain to generate a wakeup and an interrupt to the PRCM.

Upon wakeup and interrupt from the daisy chain, if the wakeupevent bit is set for the HSIC pads, then restart the USB Host module and the UTMI_Px clock and resume the device.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.69 I2C FIFO Draining Interrupt Not Generated

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i796

CRITICALITY

Medium

DESCRIPTION

When I2C module is used in HS master receive mode, and when smart-idle wakeup mode is set:

- If reconfiguration of I2C_BUF[13:8] RXTRSH value is done while I2C_CON[15] I2C_EN = 0x1, and with no clearing of the RX buffer pointer.
- I2C module does not wakeup from idle mode due to wrong pointers of RX Buffer (as RXTRSH was reconfigured with no actual cleaning of RX FIFO pointers from a previous transfer).

As a consequence, I2C FIFO draining interrupt is not generated in Idle/WakeUp scenario.

WORKAROUND

Before reconfiguring the RXTRSH (Threshold value for FIFO buffer in RX mode):

- Disable I2C controller by setting the I2C_CON[15] I2C_EN bit to 0x0 (this puts the controller in reset, clears the FIFOs, and sets the status bits to their default value)
- Once the I2C module reconfiguration is done, reactivate the I2C controller by setting the I2C_CON[15] I2C_EN bit to 0x1 (module enabled).

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

1.70 Read Accesses to GP Timer TCRR Can Report Random Value When In Posted Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i804

CRITICALITY

Low

DESCRIPTION

General-purpose (GP) timers in posted mode (GPT_TSICR[2] POSTED bit set to 0x1) with GPTi_ICLK (timer interface clock) and GPTi_FCLK (timer functional clock) clock frequency not respecting the ICLK < 4*FCLK ratio, can periodically report a random time from read accesses to counter register GPT_TCRR.

WORKAROUND

If ICLK < 4*FCLK ratio is not respected, then software should make sure that the posted mode is inactive (the GPT_TSICR[2] POSTED bit is set to 0x0) before any read access to the GPT_TCRR register.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

Limitations

2.1 Issue with Transfer Of Multiple Command Packets Coming From Interconnect

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i575

CRITICALITY

Low

DESCRIPTION

In video mode, the command mode packets, provided through the DSI protocol engine OCP port, can be interleaving during the blanking periods vertical and/or horizontal blanking periods of the video stream sequence.

When TX FIFO on the OCP slave port is empty and if the first packet written to TX FIFO is less than 13 words when 1 data lane is active or 17 words when 2 data lanes are active or 25 words when 3 or 4 data lanes are active, only this packet will be sent on the HS link during the next blanking period enabled for command packet transfer.

This is the only sent packet, because this packet is the only completely written packet when the FSM has read the last location of this packet from TX FIFO. Even if more packets are written in TX FIFO before the interleaving starts, these packets will not be sent during that blanking period.

WORKAROUND

No workaround is available. The impact is minor because:

- When interleaving is done on a vertical blanking period (VSA, VFP, VBP), as these blanking are expressed in a number of lines, the remaining packet(s) in TX FIFO are sent on HS link during the next line blanking interval within the same blanking period or during the next one.
- When interleaving is done on a horizontal blanking period (HSA, HFP, HBP), the remaining data in TX FIFO is sent on the next blanking period.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.2 Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking.

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i576

CRITICALITY

Medium

DESCRIPTION

The DSI protocol engine is based on the MIPI DSI ver. 1.01 specification.

However the video mode using sync pulses is implemented using the timing described in MIPI DSI ver. 1.00 and not ver. 1.01:

- The DSI protocol engine sends only HE packets (when enabled) during VACT and not during VSA, VFP, and VBP.
- The DSI protocol engine sends VE (noted as VSE in MIPI DSI ver. 1.01 specification) during VSA and not during VBP.

Figure 2.1 represents actual implementation and Figure 2.2 represents MIPI DSI ver. 1.01 specification.

Figure 2-1. MIPI DSI 1.00 (Implemented) - Video Mode Interface Timing: Nonburst Transmission With Sync Start And End.

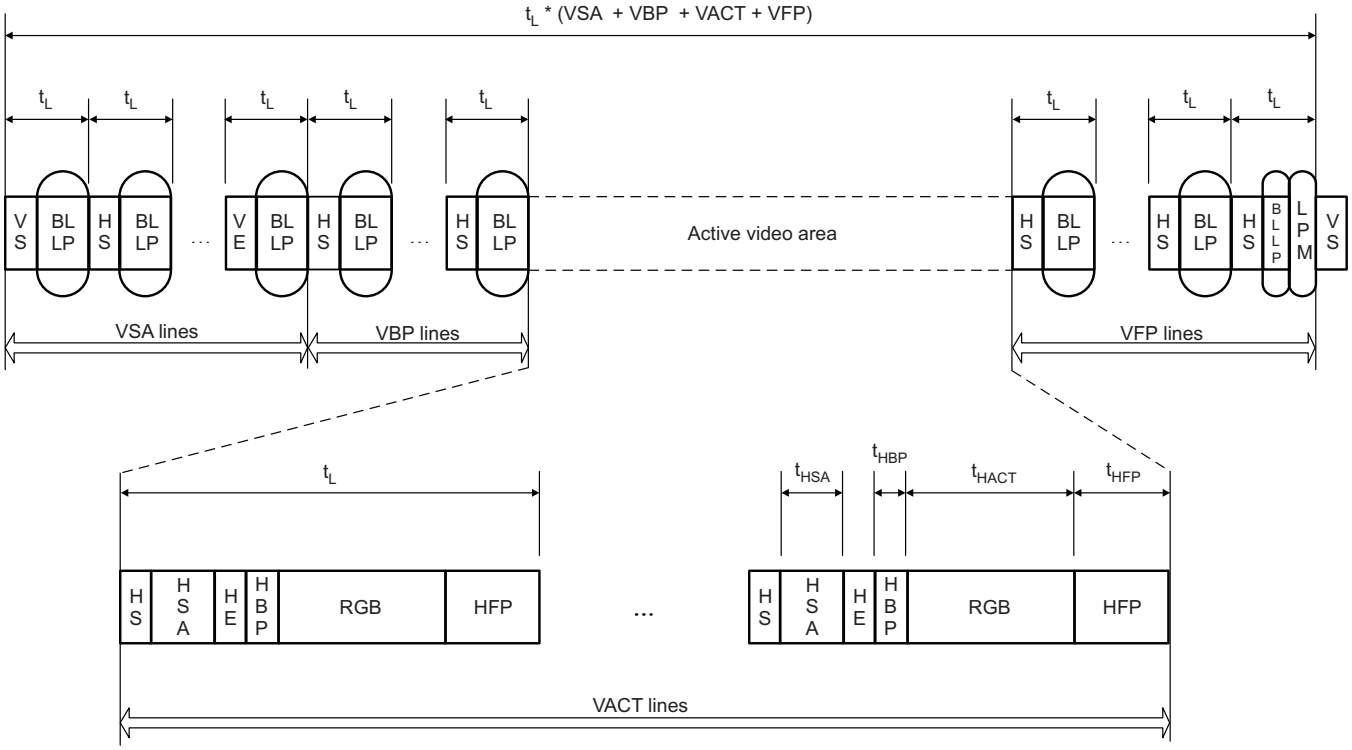
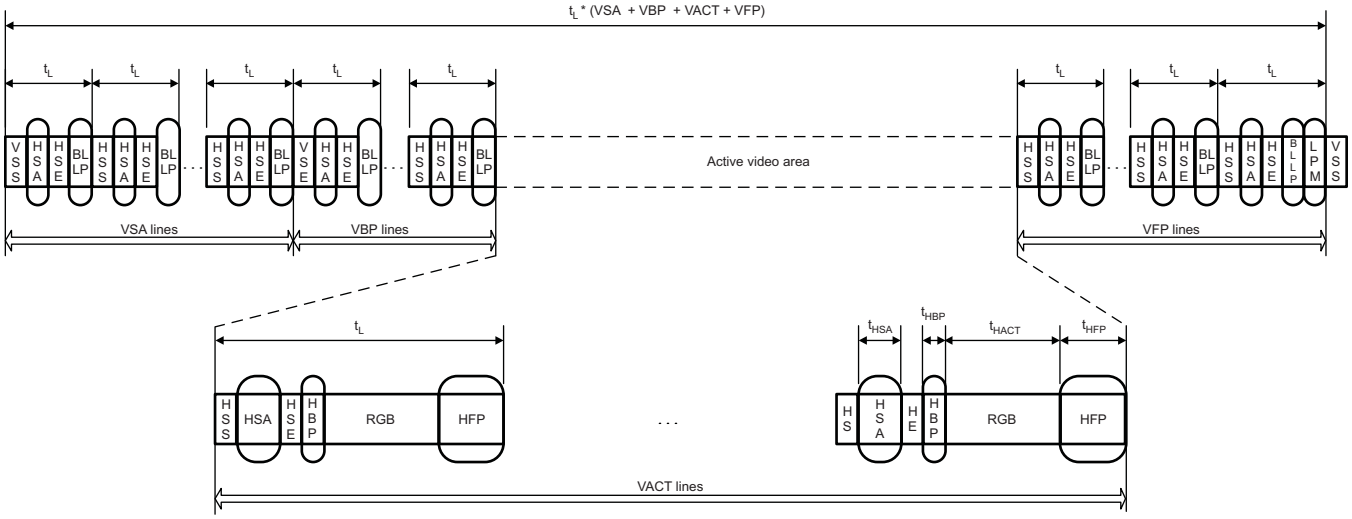


Figure 2-2. MIPI DSI 1.01 (Not Supported) - Video Mode Interface Timing: Nonburst Transmission With Sync Start And End.



WORKAROUND

NA

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.3 BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i596

CRITICALITY

Low

DESCRIPTION

BITMAP1, BITMAP2, and BITMAP4 are not supported by the graphics pipeline.

WORKAROUND

No workaround is available.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.4 Limitation On DISPC Dividers Settings When Using BITMAP Format

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i597

CRITICALITY

Low

DESCRIPTION

When Graphics pipeline input pixel is in BITMAP format, it cannot output pixel at the rate of one pixel per each clock cycle when LCD = 1 and PCD = 1.

The limitation is not applicable if PCD is greater than or equal to 2.

WORKAROUND

No workaround is available.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.5 HDQ™/1-Wire® Communication Constraints

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i621

CRITICALITY

Medium

DESCRIPTION

HDQ/1-Wire protocols use a return-to-1 mechanism and it requires an external pullup resistor on the line. There is a timing limitation on this return-to-1 mechanism that requires a constraint on the external pullup resistor(R) and the capacitive load(C) of the wire.

WORKAROUND

There is a constraint in the design for the maximum allowed rise time of the wire. After writing data to the wire, the HDQ/1-Wire module samples the logic value of the wire 1 FSM (finite state machine) clock cycle later. The FSM expects to read back 1 value from the wire. This constraint must be taken into account, when calculating the pullup resistor(R) according to the capacitive load(C) of the wire.

The maximum RC (pullup resistor and capacitive load) value should be calculated as follow:

R <1200ns/(10e-12 + C)

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.6 Presence of a Floor Noise on Audio Band When Multiple McPDM Downlink Enabled

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i635

CRITICALITY

Medium

DESCRIPTION

Depending on McPDM FIFO value, a floor Noise in audio band at ~-80dB_fullscale may appear with one of these two following configurations:

- Case 1: AESS is used for the McPDM transfers, 6 downlink channels of McPDM are enabled and McPDM downlink FIFO threshold is set to 1.
- Case 2: AESS is not used for the McPDM transfers, 4 downlink channels of McPDM are enabled and McPDM downlink FIFO threshold is set to 1 or 2.

WORKAROUND

Case 1 workaround:

- Set McPDM downlink FIFO threshold to 2 (floor noise goes back to ~ -130dB_fullscale)

Case 2 workaround:

- Set McPDM downlink FIFO threshold to 4 (floor noise goes back to ~ -130dB_fullscale)

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.7 Overlay Optimization Limitations

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i641

CRITICALITY

Low

DESCRIPTION

Overlay optimization does not work when resize processing is enabled on any 'Enabled' layer.

When any of the 'Enabled' layers has bit field DISPC_p_ATTRIBUTES.RESIZEENABLE as nonzero it will neither be optimized nor participate in optimization of layers below.

WORKAROUND

For optimization to occur for a particular layer, make RESIZEENABLE as 0x0. With multiple layers enabled, make RESIZEENABLE for all the layers as 0x0 for every layer to participate in overlay optimization of itself or for the layers below it.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.8 VID /GFX Pipeline Underflow Interrupt Generated When In WB Memory-to-memory Operation

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i642

CRITICALITY

Low

DESCRIPTION

In memory-to-memory operation, it is possible for WB pipe to write out pixel data faster than the rate at which VID/GFX DMA is fetching the pixel data. Under such a condition, the WB pipe should slow down by itself (by inserting necessary stalls) and should not cause an underflow at the VID DMA. The required behavior is: when VID/GFX pipelines are connected to WB in memory-to-memory mode (connected either directly or through overlay), there should not be any buffer underflow and no underflow interrupt should be generated.

However the DISPC module deviates from this behavior and generates sporadic underflow interrupt. But buffer underflow never happens; there is no corruption of the data written back to the memory. Only undesired interrupts are generated due to this defect.

WORKAROUND

Software should disable the VID/GFX pipeline underflow interrupt by writing 0x0 in DISPC_IRQENABLE[20-12-10-6] bit if it is connected to the WB pipeline in memory-to-memory mode.

Software should not consider the underflow interrupt generated in DISPC_IRQSTATUS[20-12-10-6] bit when in memory-to-memory mode

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.9 HSI: Run-time Change Of HSR Counter Values Damages Communication

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i647

CRITICALITY

Low

DESCRIPTION

The MIPI HSI specification explicitly requires run-time configurability to be supported for these HSR Frame Burst, HSR Frame Time-out, and HSR Tailing Bit counters.

Update of HSR counters with new values while data traffic is ongoing results in spurious errors and/or data loss/corruption:

- HSR Frame Burst Counter update: Spurious FT/TB errors and/or data loss/corruption
- HSR Frame Timeout Counter update : Spurious FT/TB errors and/or data loss/corruption (observed only in pipelined flow)
- HSR Tailing Bit Counter: Spurious FT/TB errors and/or data loss/corruption (observed only in pipelined flow)

WORKAROUND

No workaround is identified.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.10 HSI Does Not Send Break Frame In Some Scenario

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i648

CRITICALITY

Medium

DESCRIPTION

From the MIPI HSI spec; the transmitter shall be able to transmit a break transmission regardless of the state of the READY signal.

- Break frame will not be sent if the READY line is low and Tx FIFO is not empty. Inserting a break frame, in this configuration, will also override a frame in Tx FIFO. Refer to "Break frame corrupt ongoing transfer" errata.
- Break frame will be sent if TX FIFO is empty and READY line is low.

WORKAROUND

No workaround is identified.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.11 EMIF: Refresh rate programmation issue

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i686

CRITICALITY

High

DESCRIPTION

The refresh rate is programmed in the EMIF_SDRAM_REF_CTRL.REG_REFRESH_RATE parameter. To ensure some bandwidth is still available to the system, a low threshold has been implemented in hardware; if the programmed value is lower than the threshold, the threshold value is programmed instead of the requested value.

Assuming 1x is the refresh rate of the LPDDR at 85C, JEDEC requirement is to have 4x refresh rate between 85C and 105C.

For die up to 1 Gb, Trefi is 15.6us or 7.8us, even with the threshold limitation OMAP will support a 4x refresh rate.

For 2Gb and 4Gb die, Trefi = 3.9us, the threshold allows only a 3x refresh rate. For 8 Gbit the threshold will limit to a 2x refresh rate.

WORKAROUND

For 2 Gbit and 4 Gbit, between 85C and 95C the recommendation is to use this 3x refresh rate. Most of memory vendors have confirmed that this is acceptable.

Customer must ensure the LPDDR2 junction temperature will never exceed 95C. This can be achieved by:

- Full device level thermal simulations on the worst case thermal use case. TI can provide flotherm model to enable these types of simulations.
- And/or instrumentation of the phone placing a thermocouple on the LPDDR2 top case and measuring the temperature thru a comprehensive set of use cases

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Not impacted

2.12 EMIF: 8-Gbit (Single Die) Support

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i726

CRITICALITY

Medium

DESCRIPTION

The refresh requirements for an LPDDR2 8-Gbit (single die) memory at high temperature (>85°C) conflicts with the current EMIF refresh policy and may result in a lock-up situation. This issue does not exist with 2-Gbit and 4-Gbit memories due to their lower t RFC(130 ns versus 210 ns).

WORKAROUND

There is no workaround.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Not impacted	Impacted

2.13 ECD3 Fails To Decode Bitstreams Having Mismatch Between CBP and CBF

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i752

CRITICALITY

Medium

DESCRIPTION

ECD3 fails to decode the bitstreams having the mismatch between CBP and CBF generated by non-TI encoder. The mismatch violates the H.264 CBP rule. But the mismatch can be correct in-practice / real-life /De-facto.

It wrongly decodes the bitstream as error stream (instead of normal stream), but it never results in hang or crash. The decoded output have visual noticeable artifacts as many good slices are concealed.

The issue occurs for H.264 MP/HP decoder decoding bitstream generated by non-TI encoder violating H.264 CBP rule. It does not occur for H.264 BP/MP/HP encoder as well as H.264 BP decoder.

WORKAROUND

No Workaround

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.14 TV Overlay Blending Limitation

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i763

CRITICALITY

Low

DESCRIPTION

The overlay determine the blending effect by the following:

```
If (Ae > 0x3fc)
    Result = Upper layer
Elsif (Ae == 0x0)
        Result = Lower Layer
    Else
        Ae = Ap×(Upper layer) + (1-Ap)×(Lower layer)
```

where Ae represents the effective Alpha, input of overlay.

Ae is determined by two inputs parameters: Ap (pixel alpha) and Ag (global alpha). The Ap available at the input of overlay can come through two paths:

1. The scaler (in which case the highest and second highest values are 0x3ff and 0x3fb, respectively).
2. The parallel bypass path (in which case we can get pixel alpha values between 0x3fc and 0x3fe).

The effective alpha value can only be in the range of 0x3fc – 0x3fe if the global alpha value is programmed as 0xff. As an inference from the above if Ae value (resulting as a multiplication of global alpha [Ag] and pixel alpha[Ap]) inside the TV overlay is between 0x3fc and 0x3fe, the blending logic treats this layer as opaque and blending does not occur.

WORKAROUND

None

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.15 ISP Pattern Generator Is Not Functional

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i779

CRITICALITY

Low

DESCRIPTION

The ISP pattern generator, which implements an internal data generation mechanism to test the external pins and can generate RAW data without the need for an external image sensor, is not functional.

WORKAROUND

None

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

2.16 Voltage Drop Observed On CSI PHY Pad In GPI mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i817

CRITICALITY

Low

DESCRIPTION

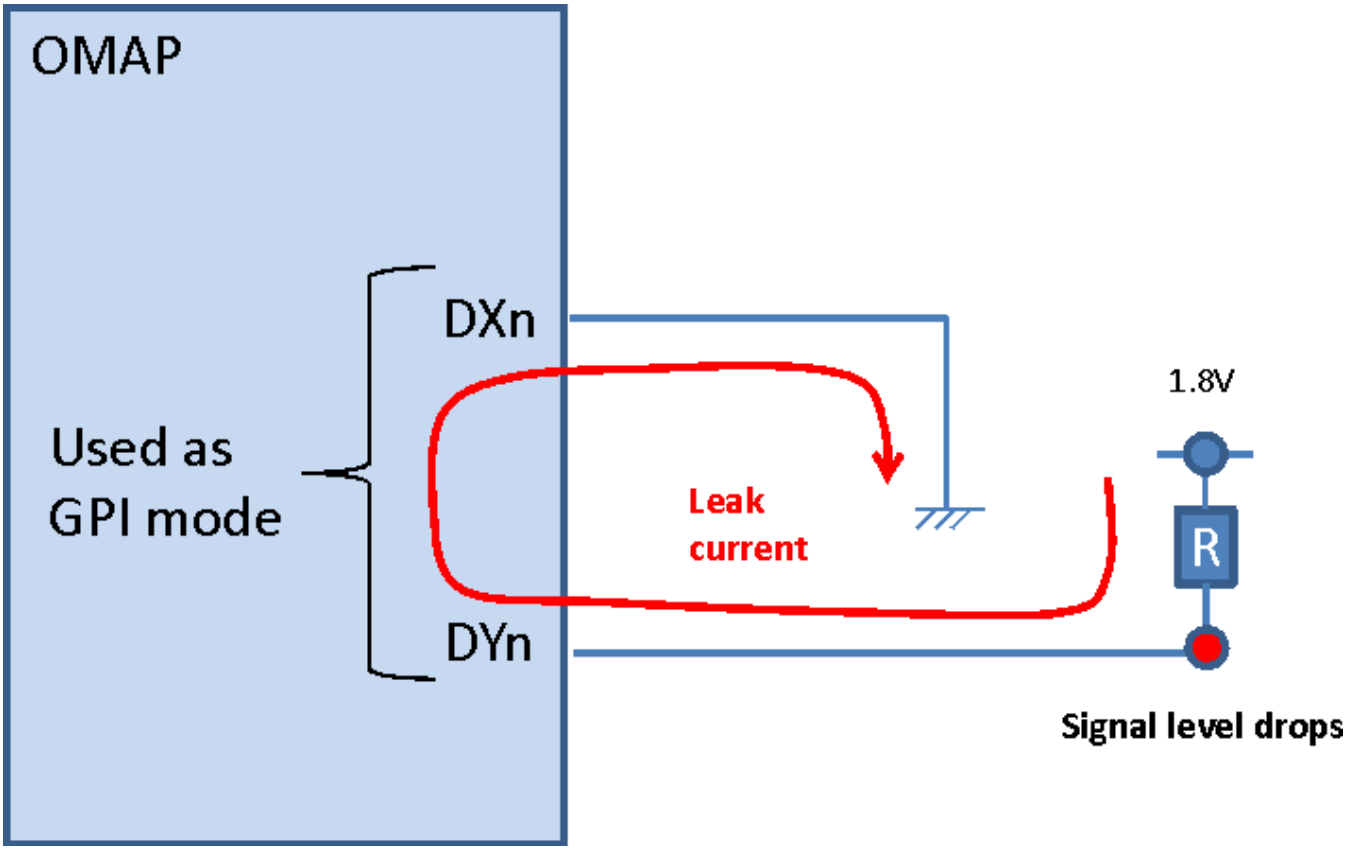
Voltage drop can be observed when following conditions are met:

- csix_dx/y_ pad pair(DXn, DYn on the figure below) is used in GPI mode (CONTROL_CAMERA_RX[20:19]/[17:16] CAMERARX_CSIx_CAMMODE=0x3)
- One of the pair is connected to GND and another is pulled-up to High

The signal level of the pad which is pulled-up is dropped due to the leakage of the component used in the off switch for the on-die termination between DXn and DYn. The leakage current (and the voltage drop) varies depending on PVT condition.

Under the worst case condition, the leakage can be high enough to drop the signal level under VIH of the GPI buffer and causes functional failure.

Figure 2-3. CSI PHY pad in GPI mode



WORKAROUND

1. Use different pad for GPI.
2. Use the pull-up resistor value smaller than or equal to 9k Ohm. It avoids the voltage drop and keeps the signal level above VIH. However this will be at the expense of increased current (up to 70uA in the worst case), as long as DXn and DYn are opposite in polarity.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

Cautions

The purpose of this section is to alert OMAP users about sensitive silicon concern. Items described in the following section are compliant with specification (neither bug nor limitation), but it is mandatory to carefully respect guidelines to ensure correct OMAP behavior.

3.1 LPDDR2 High Temperature Operating Limit Exceeded

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i704

CRITICALITY

High

DESCRIPTION

The mode register MR4 gives a status of the LPDDR2 device temperature. If the value of MR4 [2:0] = 0x111 the LPDDR2 might not operate properly.

GUIDELINES

The EMIF supports automatic temperature monitoring. The temperature monitoring can be enabled per chip-select by setting the EMIF_TEMP_ALERT_CONFIG[31] REG_TA_CS1EN and EMIF_TEMP_ALERT_CONFIG[30] REG_TA_CS0EN bits.

The EMIF periodically polls the temperature of LPDDR2 (issues an MRR command to mode register 4) every time EMIF_TEMP_ALERT_CONFIG[21:0] REG_TA_REFINTERVAL expires.

If during this read operation the value 0x111 is returned by the memory this means that temperature operating limit is exceeded. In that case, the recommendation is to do a power-off sequence to cool of the memory.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.2 SDMMC1 interface latch-up issue

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i705

CRITICALITY

High

DESCRIPTION

GUIDELINES

To prevent latch-up on this interface customer must ensure injected current is lower than above values during SD card plug/unplug and during functional IO switching. No work around is needed if mmc1 interface supply voltage is 1.8V.

If Card Detection feature is needed to avoid card hot plug/unplug (SD card is accessible without battery removal): VDDS_SDMMC1 supply must be turned OFF before any card insertion/extraction. SDMMC1 IOs must be correctly powered down before supply ramp up/down.

Note: in case TWL6030 companion chip is used for card detection, TWL6030 automatic shutdown of VMMC LDO feature must not be used as it can't be sequenced properly with OMAP SDMMC IOs power down. Only SW sequence must be used to power down IOs then supply when card extraction is detected.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.3 Undesired McBSP slave mode behavior during reset without CLKR/CLKX

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i706

CRITICALITY

Low

DESCRIPTION

As described in the Technical Reference Manual, the McBSP port requires two clock cycles of CLKR/CLKX during reset to synchronize the interface configuration. When the McBSP is configured in slave mode, the necessary clock is provided by the other device (the interface master). If the master device does not provide the necessary clock before the first frame pulse then undesired behavior of the McBSP port will occur since it will only be properly initialized during the first two clock cycles of CLKR/CLKX. Impacts of this situation include:

- McBSP port does not receive the first frame of data from the master
- Undefined output (i.e. glitch) on McBSP transmit line during the first frame pulse

GUIDELINES

If possible, the master should provide CLKR/CLKX before the first frame pulse (during McBSP initialization) to avoid this issue. No other workaround is available.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.4 Use Smartreflex class 1.5 for Ice Cream Sandwich

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i730

CRITICALITY

Medium

DESCRIPTION

During Ice Cream Sandwich development, the SmartReflex Voltage Control techniques have been reviewed.

Conclusion is that using Class 1.5 is better for power comsumption on ICS. This is also better for software stability as it is simpler to develop.

GUIDELINES

Recommendation is to use class 1.5 for Ice Cream Sandwich.

This Voltage Control Technique is explained in the TRM Chapter "AVS Overview". For class 1.5, as the reference value for a given OPP of the device is configured by efuse for a class 3 technique, software needs to add extra margin for the voltage requested to the power IC after calibration. The DM operating condition addendum document gives details on this extra margin per OPP and voltage domain.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.5 Change In OMAP4xx Off Mode Sequence For a TPS62361B-Based Platform

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i738

CRITICALITY

Medium

DESCRIPTION

In a TPS62361B-based OMAP44xx platform used to power the VDD_MPU supply of OMAP44xx, the EN pin of TPS62361B is driven by the SYSEN pin of the TWL6030 PMIC.

The minimum voltage at the output of TPS62361B while EN = 1 is 0.5 V.

As part of existing OMAP44xx off mode sequence the OMAP44xx voltages ramp down in the following order:

- VDD_IVA ramps down to 0 V
- VDD_MPU ramps down to 0.5 V
- VDD_CORE ramps down to 0 V

This creates a window where the VDD_CORE voltage rail is 0 V and the VDD_MPU voltage is 0.5 V. This condition affects the reliability of the device, thereby reducing the lifetime of the device.

GUIDELINES

The following changes must be made in the OMAP4xx off mode sequence:

1. The OFF command value must be changed to match the RETENTION command value for the CORE power domain (PRM_VC_VAL_CMD_VDD_CORE_L).

(a) As a consequence, OMAP sends the retention voltage I2C command to the PMIC for VDD_CORE voltage domain during off mode entry.

(b) This ensures that VDD_CORE = 0.75 V and VDD_MPU = 0.5 V during entry into off mode.

2. VCORE1 LDO of PMIC, which supplies VDD_CORE supply of OMAP, must be associated to PREQ1 (driven by sys_pwr_req from the OMAP side) by writing 0x1 in PMIC register VCORE1_CFG_GRP.
3. The SYSEN pin of the PMIC, which controls the EN pin of TPS62361B, must be associated to PREQ1 by writing 0x1 in PMIC register SYSEN_CFG_GRP.
4. Registers VCORE1_CFG_TRANS and SYSEN_CGF_TRANS must be programmed to 0x1
5. The discharge pulldown of the VCORE1 LDO in TWL6030 must be disabled in CFG_SMPS_PD:VCORE1, so that the ramp down curves of VDD_MPU and VDD_CORE are matching. (When this pulldown, is enabled, it only becomes active when PREQ1 goes down. So there is no need to re-enable it after the off mode sequence.)
6. When sys_pwr_req transitions from 1 to 0, both VDD_CORE and VDD_MPU voltages ramp down to 0 V due to the association done with PREQ1 as mentioned above.
7. When OMAP wakes up from off mode, VDD_MPU and VDD_CORE ramp up automatically to 0.5 V and 0.75 V, respectively.
8. Later VDD_CORE, VDD_MPU, and VDD_IVA ramp up to their respective ON voltage defined in PRM_VC_VAL_CMD_VDD_MPU_L, PRM_VC_VAL_CMD_VDD_IVA_L and PRM_VC_VAL_CMD_VDD_CORE_L registers when I2C commands are sent by OMAP to PMIC.

   This helps to avoid the window where VDD_CORE = 0 V and VDD_MPU = 0.5 V during entry into and exit from OMAP off mode.

   The original OMAP44xx OFF-wakeup sequence without the Guidelines is shown below.

Figure 3-1. Original OMAP4xx OFF-Wakeup Sequence

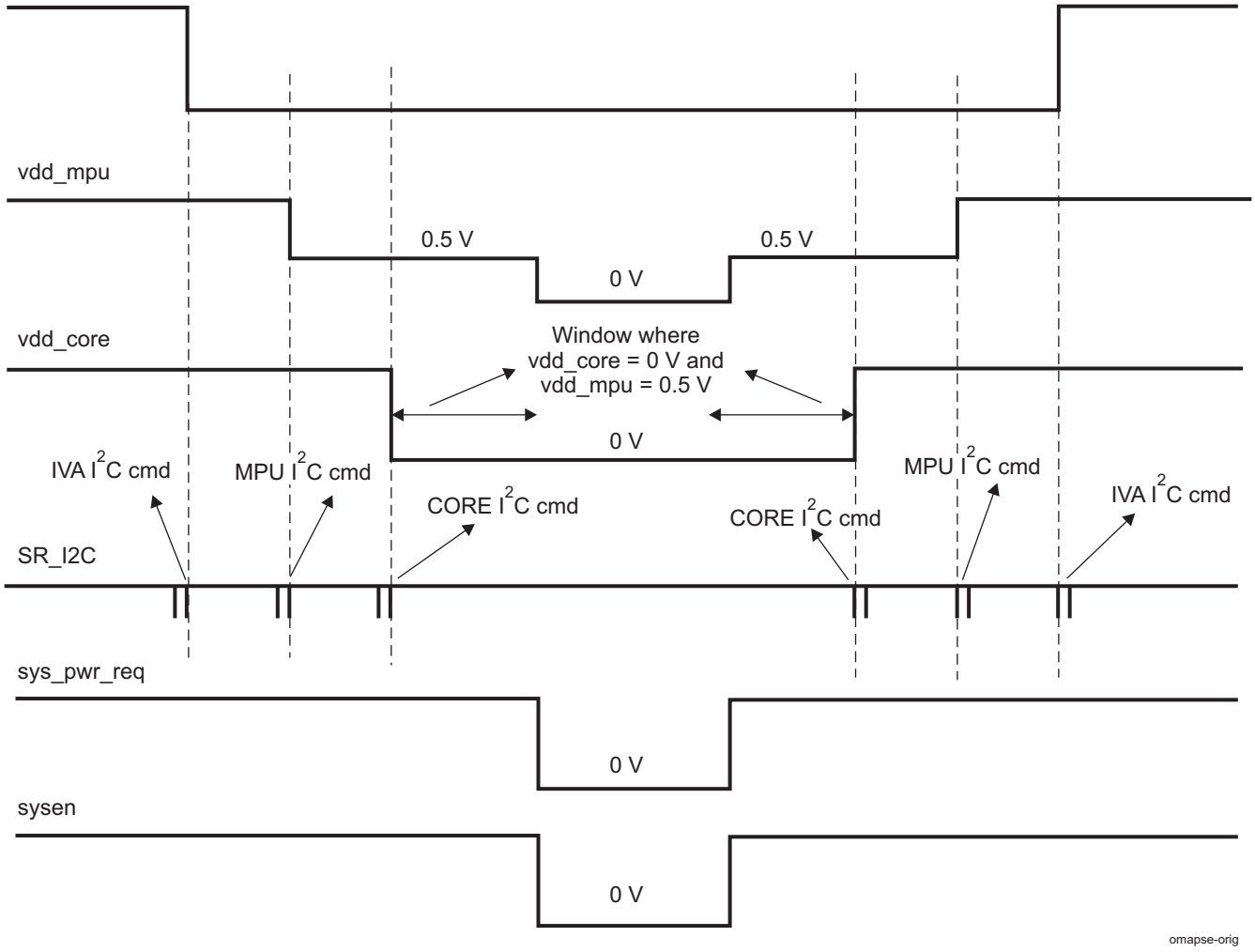
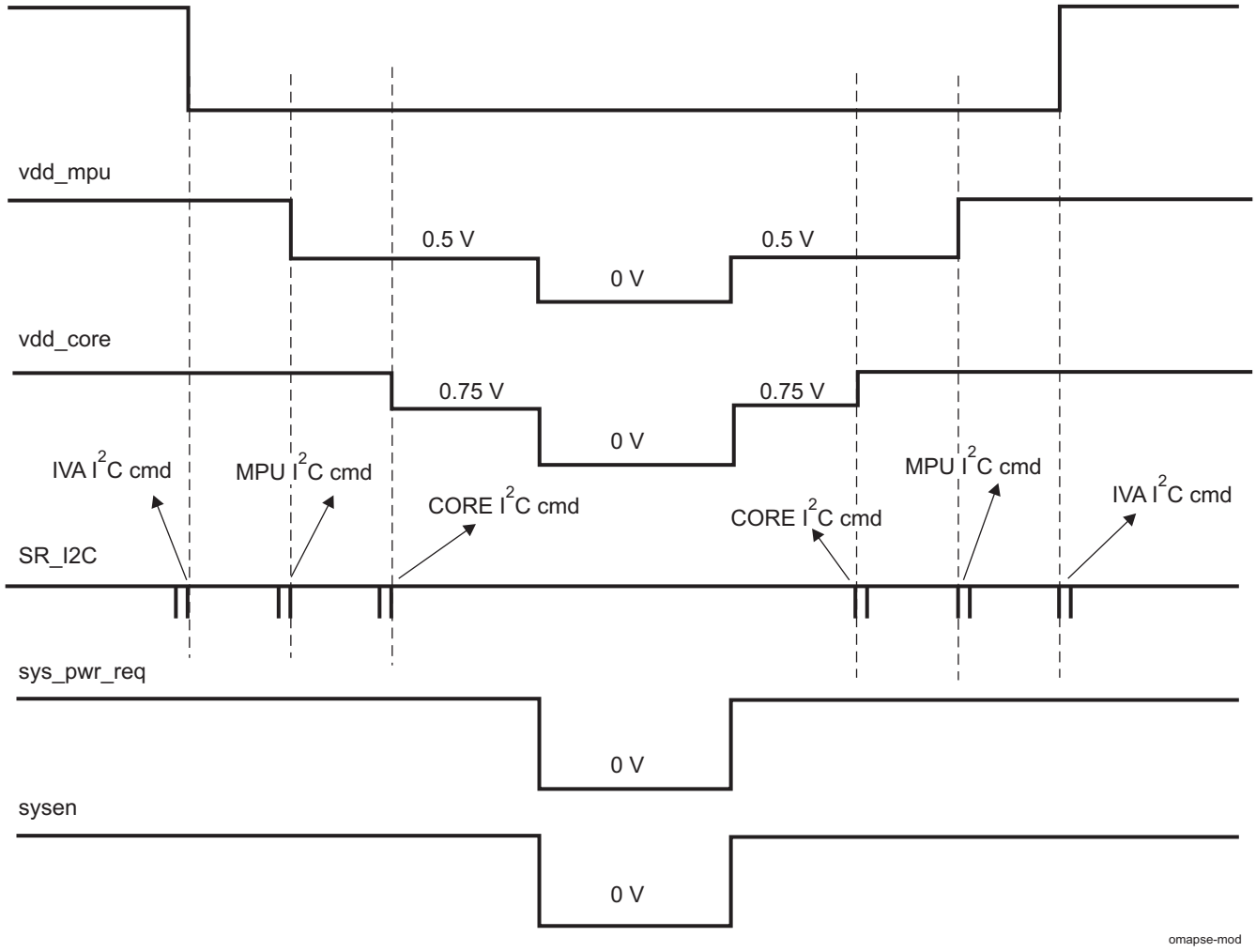


Figure 3-2. Modified OMAP4xx OFF-Wakeup Sequence



REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.6 High-Speed Image Capture Use Case

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i741

CRITICALITY

Medium

DESCRIPTION

The data flow for High-Speed Image capture use case is as follows: CSI2 RAW10 packed -> SDRAM -> ISP RSZ -> SL2 -> SIMCOP -> SDRAM. In this use case it is mandatory not to use DPLL lock/unlocked sequence for DPLL_ IVA during CD_IVAHD clock domain sleep stage.

The clock gating management in automatic mode (CM_AUTOIDLE_DPLL_IVA[2:0] AUTO_DPLL_MODE is different than 0x0 and HW auto mode is enabled CM_IVAHD_CLKSTCTRL[1:0] CLKTRCTRL = 0x3) results in DPLL_IVA relocking stage when SL2 write memory accesses are needed by ISP RSZ. The lock delay, bypass clock is not supplied when DPLL is managed in automatic mode, is resulting in backpressure for CSI2 side which leads to CSI2 overflow.

GUIDELINES

During the above use case, it is mandatory to use the DPLL_IVA in manual bypass in HW auto mode (CM_IVAHD_CLKSTCTRL[1:0] CLKTRCTRL set to 0x3); that is, CM_AUTOIDLE_DPLL_IVA[2:0] AUTO_DPLL_MODE is set to 0x0. It is possible to select CORE_X2_CLK divisor as 1, 2, 4, or 8 for the bypass clock of DPLL_IVA as IVA-HD does not make any computation. CM_CLKSEL_DPLL_IVA[23] DPLL_BYP_CLKSEL should be set to 1.

CORE_X2_CLK clock must be divided compliant with IVA OPP maximum clock frequency. It can be done through the CM_BYPCLK_DPLL_IVA[1:0] CLKSEL bit field.

In this way, SL2 clock can be quickly gated or ungated to meet CSI2 latency requirements.

PRCM register set configuration to allow in time the SL2 ungating clock on accesses request:

1. CM_AUTOIDLE_DPLL_IVA[2:0] AUTO_DPLL_MODE set to 0x0
2. CM_IVAHD_CLKSTCTRL[1:0] CLKTRCTRL set to 0x3
3. CM_CLKMODE_DPLL_IVA[2:0] DPLL_EN set to 0x5
4. CM_BYPCLK_DPLL_IVA[1:0] CLKSEL set to 0x1
5. CM_CLKSEL_DPLL_IVA[23] DPLL_BYP_CLKSEL set to 0x1

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.7 LPDDR2 Power-Down State is Not Efficient

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i743

CRITICALITY

Medium

DESCRIPTION

The EMIF supports power-down state for low power. The EMIF automatically puts the SDRAM into power-down after the memory is not accessed for a defined number of cycles and the EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field is set to 0x4.

As the EMIF supports automatic output impedance calibration, a ZQ calibration long command is issued every time it exits active power-down and precharge power-down modes. The EMIF waits and blocks any other command during this calibration.

The EMIF does not allow selective disabling of ZQ calibration upon exit of power-down mode. Due to very short periods of power-down cycles, ZQ calibration overhead creates bandwidth issues and increases overall system power consumption. On the other hand, issuing ZQ calibration long commands when exiting self-refresh is still required.

GUIDELINES

Because there is no power consumption benefit of the power-down due to the calibration and there is a performance risk, the guideline is to not allow power-down state and, therefore, to not have set the EMIF_PWR_MGMT_CTRL[10:8] REG_LP_MODE bit field to 0x4.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.8 MPU-EMIF Static Dependency Needed Around MPU WFI

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i745

CRITICALITY

High

DESCRIPTION

If static dependency from the MPU clock domain toward the MEMIF clock domain is disabled to save power (CM_MPU_STATICDEP[4] MEMIF_STATDEP = 0x0), the platform may lockup when exiting MPU WFI.

GUIDELINES

Recommended software: To prevent the occurrence of this issue, static dependency from the MPU clock domain toward the MEMIF clock domain must be enabled before MPU enters WFI (CM_MPU_STATICDEP[4] MEMIF_STATDEP set to 0x1). When exiting WFI, static dependency should be disabled to benefit again from dynamic power savings (CM_MPU_STATICDEP[4] MEMIF_STATDEP = 0x0).

Please make sure to use the recommended sequence described in the TRM for static dependency enabling and disabling (See Enable/Disable Software-Programmable Static Dependency section in PRCM Chapter).

The software sequence when changing static dependency from the MPU clock domain toward the MEMIF clock domain is:

1. Force destination domain (EMIF) to be awake by programming a forced wakeup transition: CM_MEMIF_CLKSTCTRL[1:0] CLKTRCTRL = 0x2 :SW_WKUP.
2. Ensure that the power domain which encloses the destination domain is ON: PM_CORE_PWRSTST[1:0] POWERSTATEST = 0x3: ON-ACTIVE.
3. Change the static dependency setting: CM_MPU_STATICDEP[4] MEMIF_STATDEP bit.
4. Put destination domain back to automatic transition mode: CM_MEMIF_CLKSTCTRL[1:0] CLKTRCTRL = 0x3 : HW_AUTO.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.9 SYSEN Usage for an OMAP44xx Platform based on TWL6030/TWL6032 and TPS62361B

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i746

CRITICALITY

Medium

DESCRIPTION

If TPS62361B is used to power the VDD_MPU supply of OMAP44xx, the EN pin of TPS62361B is driven by the SYSEN pin of the TWL6030/6032 PMIC.

The minimum voltage that can be supplied by TPS62361B while EN = 1 is 0.5 V.

The output voltage of TPS62361B is 0V only when EN = 0. Thus, when OMAP44xx enters off mode, the SYSEN pin of TWL6030/6032 toggles to 0, which ensures that VDD_MPU = 0 when OMAP44xx is in off mode. This control is required to maintain the normal OMAP44xx off mode condition where VDD_MPU = 0V.

If the SYSEN pin is used to control the reset (active low signal) or enable (active high signal) of any peripheral (for example, modem, WLAN chip and so forth) which is required to be active when OMAP44xx is in off mode, the peripheral is not active due to this implementation.

This prevents the peripheral from waking up OMAP44xx when it is in off mode.

This caution does not apply if TWL6030/6032 is used to supply the VDD_MPU rail of OMAP44xx and SYSEN is not used to control the TPS62361B EN pin.

GUIDELINES

- If TPS62631B is used to power VDD_MPU rail in a platform, the SYSEN pin should not be used to control any peripheral reset or enable if it is one of the sources of wakeup when OMAP44xx is in off mode.
- Instead, one should use a logical AND of an OMAP GPIO and NRESPWRON signal of TWL6030 to drive the peripheral enable or reset pin.

The figure below shows the modem.

Figure 3-3. Original Implementation

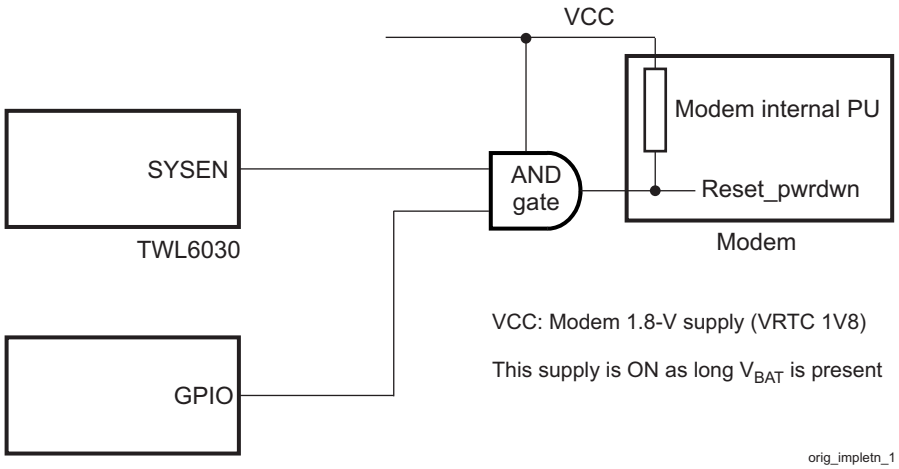
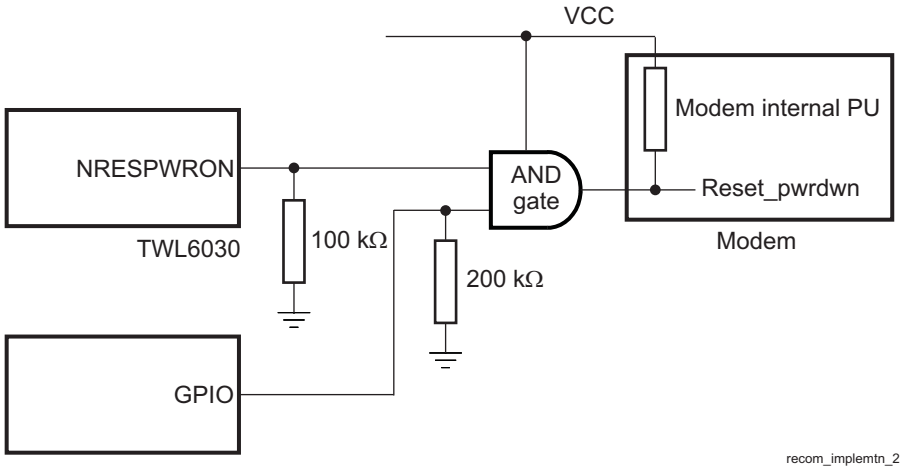


Figure 3-4. Recommended Implementation



VCC: It is the modem 1.8-V VRTC supply which is ON as long as VBATis present.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.10 Programming of CM_CLKSEL_DPLL_CORE[20]DPLL_CLKOUTHIF_CLKSEL

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i760

CRITICALITY

Medium

DESCRIPTION

CM_CLKSEL_DPLL_CORE[20].DPLL_CLKOUTHIF_CLKSEL allows muxing in the DPLL between DPLL oscillator and BYP_CLK_M3 (that is, DPLL_ABE for DPLL_CORE).

If CM_CLKSEL_DPLL_CORE[20].DPLL_CLKOUTHIF_CLKSEL = 1 and if BYP_CLK_M3 is gated (that is, in case DPLL_ABE is not Locked) then update of M3 divider which is after previous mux does not complete correctly. The incorrect update of M3 divider is impacting other dividers update; this would lead to inconsistent frequency scaling from CORE DPLL versus voltage change during DVFS transitions and ultimately lead to platform crash.

The BYP_CLK_M3 is only mapped for DPLL_CORE, this issue does not impact the other DPLLs programming.

GUIDELINES

SW should never set CM_CLKSEL_DPLL_CORE[20].DPLL_CLKOUTHIF_CLKSEL bit to 1. Having DPLL_ABE clock as a source clock for DPLL_CORE is not necessary.

Note: This guideline applies also for CM_CLKSEL_DPLL_CORE_RESTORE[20].DPLL_CLKOUTHIF_CLKSEL which should never set to 1.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.11 Power Delivery Network Verification

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i776

CRITICALITY

High

DESCRIPTION

Operating the OMAP at OPP_NITRO or OPP_NTSB creates strict power requirements on the system (OMAP + Power Management IC + Power Distribution Network).

The OMAP requires carefully controlled system margin validation and verification.

In GHz systems, instability could result from marginal board design, component selection, power supply transients, susceptibility to noise, and so forth.

Developers must optimize PDN board designs to ensure stable operation at GHz frequencies across all conditions and over the lifetime of the phone. The necessary steps to follow to ensure robust operation are listed in the following Guidelines section.

GUIDELINES

- Software guidelines:

1. It is mandatory to use SmartReflex technology for the three power rails (MPU, IVA, CORE): use of AVS is required; not using AVS would lead to abnormal aging and consumption of the system.
2. For IVA and MPU power rails, ABB (adaptative body bias) must be engaged in:
   - ABB Set1 mode (PRM_LDO_ABB_MPU/IVA_SETUP[2] ACTIVE_FBB_SEL = 0x1)

   or

   - ABB Set2 mode (PRM_LDO_ABB_MPU/IVA_SETUP[1] ACTIVE_RBB_SEL = 0x1)

   For OPP_NITRO and OPP_NTSB, ABB Set1 must be enabled

   For OPP_TURBO, ABB Set1 or ABB Set2 must be enabled.

   Software should enable ABB Set2 mode or ABB Set1 mode depending on the following fused bits for OPP_TURBO:
   - CONTROL_STD_FUSE_OPP_DPLL_1[20] MPU_RBB_TB
   - CONTROL_STD_FUSE_OPP_DPLL_1[21] IVA_RBB_TB

- PCB guidelines:

The Power Delivery Network should be optimized to match OPP_NITRO and OPP_NTSB requirements. All PCB Design requirements for PDN optimization can be found in Appendix A of the Data Manual.

It is mandatory for the PCB developer to align the PCB with the described guidelines and to meet TI requirements.

If you do not achieve TI requirements, contact your TI representative.

If any competence or tool issue is needed to perform the verification of the simulation of the PCB, contact your TI representative.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.12 PRCM Voltage Controller Uses MPU Slave Address

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i797

CRITICALITY

Low

DESCRIPTION

When MPU, IVA, and CORE voltage rails are tied together, the PRCM voltage controller uses MPU slave address programmed in the PRM_VC_SMPS_SA[22:16] SA_VDD_MPU_L bit field.

GUIDELINES

Program correct address in the PRM_VC_SMPS_SA[22:16] SA_VDD_MPU_L bit field.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

3.13 McPDM Downlink Data Corrupted With TWL604x

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i800

CRITICALITY

High

DESCRIPTION

Some noise issue can occur when OMAP MCPDM downlink path is used with TWL604x audio chip. Depending on the delay between abe_clks provided by TWL604x and the loopback clock abe_pdm_lb_clk from OMAP, the data transmitted to TWL604x DACs can be corrupted. As a result, the output noise of the analog output stages can increase. Refer to TWL6040/41 silicon errata for more bug details.

GUIDELINES

An inverter is placed on the board between TWL604x.PDMCLK and the OMAP abe_clks pad. The inverter (for example, SN74AUC1G04DCK) must be placed close to TWL604x on the PCB.

REVISIONS IMPACTED

OMAP4460	
1.0	**1.1**
Impacted	Impacted

Errata per Chip Revision

A.1 Errata Impacting Revision 1.0 (98 Sections)

A.1.1 Bugs (70 Sections)

i103: Delay needed to read some GP timer, WD timer and sync timer registers after wakeup

i202: MDR1 access can freeze UART module

i339: DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port

i340: DSI: Cancel Tearing Effect Transfer

i341: DSI: RX FIFO Fullness

i342: DSI: Access Restriction On DSI_TIMING2 Register

i343: DSI: Tx FIFO Flush Is Not Supported

i378: sDMA Channel Is Not Disabled After A Transaction Error

i422: DSI SOF Packet Not Send

i487: SIMCOP Lens Distortion Correction issue

i488: ISS: SOFTRESET Bit Status Not Working For Circular Buffer

i489: ISS: SOFTRESET Bit Status Not Working For Burst Translation Engine

i496: ISS State Can Be Corrupted During Debug Mode

i483: DSI VSYNC HSYNC Detection In Video Mode

i524: Dual Video Mode

i525: Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0

i603: Deep Power-Down Support During Off Mode

i608: RTA Feature Is Not Supported

i626: MMCHS_HCTL.HSPE Is Not Functional

i631: Wrong Access In 1D Burst For YUV4:2:0-NV12 Format

i643: Status of DSI LDO Is Not Reported to DSI Protocol Engine

i645: HSI Break Frame Corrupt OnGoing Transfer

i646: HSI Error Counters Cannot Be Disabled

i653: McPDM/DMIC Issue With Software Reset With SW_xx_RST

i659: UART: Extra Assertion of UARTi_DMA_TX Request

i661: USB OTG Software Initiated ULPI Accesses To PHY Registers Can Halt the Bus

i662: ISS-SIMCOP: ISS-LSC Not Transparent After Prefetch Error Event

i676: UART: In an RX Wake-up Mechanism, the First Received Character Can be Lost

i677: Platform Hangs When CPU Tries To Configure The EMIF Firewall

i682: DDR PHY Must be Reset After Leaving OSWR

i688: Async Bridge Corruption

i689: Keyboard Key Up Event Can Be Missed

i690: L2 Cache Corruption Issue

i692: USB HOST - Impossible To Attach a FS Device To An EHCI Port. Handoff To OHCI Is Not Functional

i693: USB HOST EHCI - Port Resume Fails On Second Resume Iteration

i694: System I2C hang due to miss of Bus Clear support

i695: HSI: Issues In Suspending and Resuming Communication (HSR and HST)

i696: HSI: Issue with SW reset

i698: DMA4 generates unexpected transaction on WR port

i699: DMA4 channel fails to continue with descriptor load when Pause bit is cleared

i700: MPU clock glitches at OPP change

i702: HSI: DSP Swakeup generated is the same than MPU Swakeup. System can't enter in off mode due to the DSP.

i708: CBUFF Ready Window Event in Write Mode

i709: CSI-2 Receiver Executes Software Reset Unconditionally

i710: USB Host TLL Bit-stuffing Feature Is Broken

i712: ISP H3A Hangs Due to Unstable Vertical Sync Signal

i714: GPIO IRQ Not Generated After MPU Idle if IRQSTATUS Bits Not Cleared

i716: DSI PLL Signal is Not available on Hardware Observability Pads

i717: Blending Calculation Error When Premultiply Alpha is Used

i719: HS USB: Multiple OFF Mode Transitions Introduce Corruption

i722: DSS Block in "Idle Transition" State when using RFBI I/F

i724: Deadlock Between SmartReflex™ and Voltage Processor

i727: Refresh Rate Issue After Warm Reset

i728: System May Hang During EMIF Frequency Change

i729: DDR Access Hang After Warm Reset

i733: DSS Configuration Registers Access Through the L4 Interconnect

i734: LCD1 Gamma Correction Is Not Working When GFX Pipe Is Disabled

i735: Power Management Timer Value For Self-Refresh (SR_TIM)

i736: Leakage Increase On LPDDR2 I/Os

i739: MMC1 Booting May Be Bypassed Depending On VDD Ramp-up Delay

i740: Disconnect Protocol Violation

i754: ULPI RxCmds Convey the Wrong ID Bit After Save-and-Restore Sequence

i755: PRCM Hang at Frequency Update During DVFS

i761: Card Error Interrupt May Not Be Set Sometimes

i762: In AutoCMD12 mode, the CMD12 Command Is Not Issued On Write Transfer Completion

i764: SRAM LDO Output Voltage Value Software Override in RETENTION is Not Functional

i765: I/O Glitch Issue When Entering Off Mode

i774: HS USB Host HSIC Remote Wakeup Is Not Functional

i796: I2C FIFO Draining Interrupt Not Generated

i804: Read Accesses to GP Timer TCRR Can Report Random Value When In Posted Mode

A.1.2 Limitations (15 Sections)

i575: Issue with Transfer Of Multiple Command Packets Coming From Interconnect

i576: Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking.

i596: BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline

i597: Limitation On DISPC Dividers Settings When Using BITMAP Format

i621: HDQ™/1-Wire® Communication Constraints

i635: Presence of a Floor Noise on Audio Band When Multiple McPDM Downlink Enabled

i641: Overlay Optimization Limitations

i642: VID /GFX Pipeline Underflow Interrupt Generated When In WB Memory-to-memory Operation

i647: HSI: Run-time Change Of HSR Counter Values Damages Communication

i648: HSI Does Not Send Break Frame In Some Scenario

i686: EMIF: Refresh rate programmation issue

i752: ECD3 Fails To Decode Bitstreams Having Mismatch Between CBP and CBF

i763: TV Overlay Blending Limitation

i779: ISP Pattern Generator Is Not Functional

i817: Voltage Drop Observed On CSI PHY Pad In GPI mode

A.1.3 Cautions (13 Sections)

i704: LPDDR2 High Temperature Operating Limit Exceeded

i705: SDMMC1 interface latch-up issue

i706: Undesired McBSP slave mode behavior during reset without CLKR/CLKX

i730: Use Smartreflex class 1.5 for Ice Cream Sandwich

i738: Change In OMAP4xx Off Mode Sequence For a TPS62361B-Based Platform

i741: High-Speed Image Capture Use Case

i743: LPDDR2 Power-Down State is Not Efficient

i745: MPU-EMIF Static Dependency Needed Around MPU WFI

i746: SYSEN Usage for an OMAP44xx Platform based on TWL6030/TWL6032 and TPS62361B

i760: Programming of CM_CLKSEL_DPLL_CORE[20]DPLL_CLKOUTHIF_CLKSEL

i776: Power Delivery Network Verification

i797: PRCM Voltage Controller Uses MPU Slave Address

i800: McPDM Downlink Data Corrupted With TWL604x

A.2 Errata Impacting Revision 1.1 (97 Sections)

A.2.1 Bugs (69 Sections)

i103: Delay needed to read some GP timer, WD timer and sync timer registers after wakeup

i202: MDR1 access can freeze UART module

i339: DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port

i340: DSI: Cancel Tearing Effect Transfer

i341: DSI: RX FIFO Fullness

i342: DSI: Access Restriction On DSI_TIMING2 Register

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i422: DSI SOF Packet Not Send

i487: SIMCOP Lens Distortion Correction issue

i488: ISS: SOFTRESET Bit Status Not Working For Circular Buffer

i489: ISS: SOFTRESET Bit Status Not Working For Burst Translation Engine

i496: ISS State Can Be Corrupted During Debug Mode

i483: DSI VSYNC HSYNC Detection In Video Mode

i524: Dual Video Mode

i525: Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0

i603: Deep Power-Down Support During Off Mode

i608: RTA Feature Is Not Supported

i626: MMCHS_HCTL.HSPE Is Not Functional

i631: Wrong Access In 1D Burst For YUV4:2:0-NV12 Format

i643: Status of DSI LDO Is Not Reported to DSI Protocol Engine

i645: HSI Break Frame Corrupt OnGoing Transfer

i646: HSI Error Counters Cannot Be Disabled

i653: McPDM/DMIC Issue With Software Reset With SW_xx_RST

i659: UART: Extra Assertion of UARTi_DMA_TX Request

i661: USB OTG Software Initiated ULPI Accesses To PHY Registers Can Halt the Bus

i662: ISS-SIMCOP: ISS-LSC Not Transparent After Prefetch Error Event

i676: UART: In an RX Wake-up Mechanism, the First Received Character Can be Lost

i677: Platform Hangs When CPU Tries To Configure The EMIF Firewall

i682: DDR PHY Must be Reset After Leaving OSWR

i688: Async Bridge Corruption

i689: Keyboard Key Up Event Can Be Missed

i692: USB HOST - Impossible To Attach a FS Device To An EHCI Port. Handoff To OHCI Is Not Functional

i693: USB HOST EHCI - Port Resume Fails On Second Resume Iteration

i694: System I2C hang due to miss of Bus Clear support

i695: HSI: Issues In Suspending and Resuming Communication (HSR and HST)

i696: HSI: Issue with SW reset

i698: DMA4 generates unexpected transaction on WR port

i699: DMA4 channel fails to continue with descriptor load when Pause bit is cleared

i700: MPU clock glitches at OPP change

i702: HSI: DSP Swakeup generated is the same than MPU Swakeup. System can't enter in off mode due to the DSP.

i708: CBUFF Ready Window Event in Write Mode

i709: CSI-2 Receiver Executes Software Reset Unconditionally

i710: USB Host TLL Bit-stuffing Feature Is Broken

i712: ISP H3A Hangs Due to Unstable Vertical Sync Signal

i714: GPIO IRQ Not Generated After MPU Idle if IRQSTATUS Bits Not Cleared

i716: DSI PLL Signal is Not available on Hardware Observability Pads

i717: Blending Calculation Error When Premultiply Alpha is Used

i719: HS USB: Multiple OFF Mode Transitions Introduce Corruption

i722: DSS Block in "Idle Transition" State when using RFBI I/F

i724: Deadlock Between SmartReflex™ and Voltage Processor

i727: Refresh Rate Issue After Warm Reset

i728: System May Hang During EMIF Frequency Change

i729: DDR Access Hang After Warm Reset

i733: DSS Configuration Registers Access Through the L4 Interconnect

i734: LCD1 Gamma Correction Is Not Working When GFX Pipe Is Disabled

i735: Power Management Timer Value For Self-Refresh (SR_TIM)

i736: Leakage Increase On LPDDR2 I/Os

i739: MMC1 Booting May Be Bypassed Depending On VDD Ramp-up Delay

i740: Disconnect Protocol Violation

i754: ULPI RxCmds Convey the Wrong ID Bit After Save-and-Restore Sequence

i755: PRCM Hang at Frequency Update During DVFS

i761: Card Error Interrupt May Not Be Set Sometimes

i762: In AutoCMD12 mode, the CMD12 Command Is Not Issued On Write Transfer Completion

i764: SRAM LDO Output Voltage Value Software Override in RETENTION is Not Functional

i765: I/O Glitch Issue When Entering Off Mode

i774: HS USB Host HSIC Remote Wakeup Is Not Functional

i796: I2C FIFO Draining Interrupt Not Generated

i804: Read Accesses to GP Timer TCRR Can Report Random Value When In Posted Mode

A.2.2 Limitations (15 Sections)

i575: Issue with Transfer Of Multiple Command Packets Coming From Interconnect

i576: Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking.

i596: BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline

i597: Limitation On DISPC Dividers Settings When Using BITMAP Format

i621: HDQ™/1-Wire® Communication Constraints

i635: Presence of a Floor Noise on Audio Band When Multiple McPDM Downlink Enabled

i641: Overlay Optimization Limitations

i642: VID /GFX Pipeline Underflow Interrupt Generated When In WB Memory-to-memory Operation

i647: HSI: Run-time Change Of HSR Counter Values Damages Communication

i648: HSI Does Not Send Break Frame In Some Scenario

i726: EMIF: 8-Gbit (Single Die) Support

i752: ECD3 Fails To Decode Bitstreams Having Mismatch Between CBP and CBF

i763: TV Overlay Blending Limitation

i779: ISP Pattern Generator Is Not Functional

i817: Voltage Drop Observed On CSI PHY Pad In GPI mode

A.2.3 Cautions (13 Sections)

i704: LPDDR2 High Temperature Operating Limit Exceeded

i705: SDMMC1 interface latch-up issue

i706: Undesired McBSP slave mode behavior during reset without CLKR/CLKX

i730: Use Smartreflex class 1.5 for Ice Cream Sandwich

i738: Change In OMAP4xx Off Mode Sequence For a TPS62361B-Based Platform

i741: High-Speed Image Capture Use Case

i743: LPDDR2 Power-Down State is Not Efficient

i745: MPU-EMIF Static Dependency Needed Around MPU WFI

i746: SYSEN Usage for an OMAP44xx Platform based on TWL6030/TWL6032 and TPS62361B

i760: Programming of CM_CLKSEL_DPLL_CORE[20]DPLL_CLKOUTHIF_CLKSEL

i776: Power Delivery Network Verification

i797: PRCM Voltage Controller Uses MPU Slave Address

i800: McPDM Downlink Data Corrupted With TWL604x

A.3 Errata Impacting All ICs Revision

Table A-1. Errata general table

Section	1.0	1.1
i103: Delay needed to read some GP timer, WD timer and sync timer registers after wakeup	Impacted	Impacted
i202: MDR1 access can freeze UART module	Impacted	Impacted
i339: DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port	Impacted	Impacted
i340: DSI: Cancel Tearing Effect Transfer	Impacted	Impacted
i341: DSI: RX FIFO Fullness	Impacted	Impacted
i342: DSI: Access Restriction On DSI_TIMING2 Register	Impacted	Impacted
i343: DSI: Tx FIFO Flush Is Not Supported	Impacted	Impacted
i378: sDMA Channel Is Not Disabled After A Transaction Error	Impacted	Impacted
i422: DSI SOF Packet Not Send	Impacted	Impacted
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i677: Platform Hangs When CPU Tries To Configure The EMIF Firewall	Impacted	Impacted
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i688: Async Bridge Corruption	Impacted	Impacted
i689: Keyboard Key Up Event Can Be Missed	Impacted	Impacted
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