TEXAS INSTRUMENTS

Evaluation and Demonstration of the TRF3040 Frequency Modulator/Synthesizer

Application Report

June 1999

Mixed Signal Products

SWRA014

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Trademarks

AMP is a trademark of AMP Incorporated.

Bourns is a trademark of Bourns, Inc.

Coilcraft is a trademark of Coilcraft, Inc.

Components Corporation is a trademark of Components Corporation.

EFJohnson is a trademark of Transcrypt International.

Hitachi is a trademark of Hitachi, Ltd.

IBM is a trademark of International Business Machines Corporation.

Motorola is a trademark of Motorola Inc.

Murata is a trademark of Murata Manufacturing Co., Ltd.

Panasonic is a trademark of Matsushita Electric Corporation of America.

TI is a trademark of Texas Instruments Incorporated.

Toko is a trademark of Toko Inc.

Toyocom is a trademark of Toyo Communication Equipment Co, Ltd.

Vari-L is a trademark of Vari-L Company, Inc.

Venkel is a trademark of Venkel Corporation.

Contents

List of Figures

List of Tables

Evaluation and Demonstration of the TRF3040 Frequency Modulator/Synthesizer

ABSTRACT

This document describes the TRF3040 evaluation board and associated software driver, which allow the evaluation and demonstration of the Texas Instruments (TI™) TRF3040 Frequency Modulator/Synthesizer using common radio frequency (RF) bench test equipment.

1 Introduction

The TRF3040 frequency modulator/synthesizer is used with the Texas Instruments single-chip digital baseband platform. This document describes the TRF3040 evaluation board components and the software used to evaluate the device.

1.1 Digital Baseband Platform

The TI single-chip digital baseband platform, shown in Figure 1, combines two high-performance core processors—a digital signal processor (DSP) designed for digital wireless applications and a microcontroller designed specifically for low-power embedded systems.

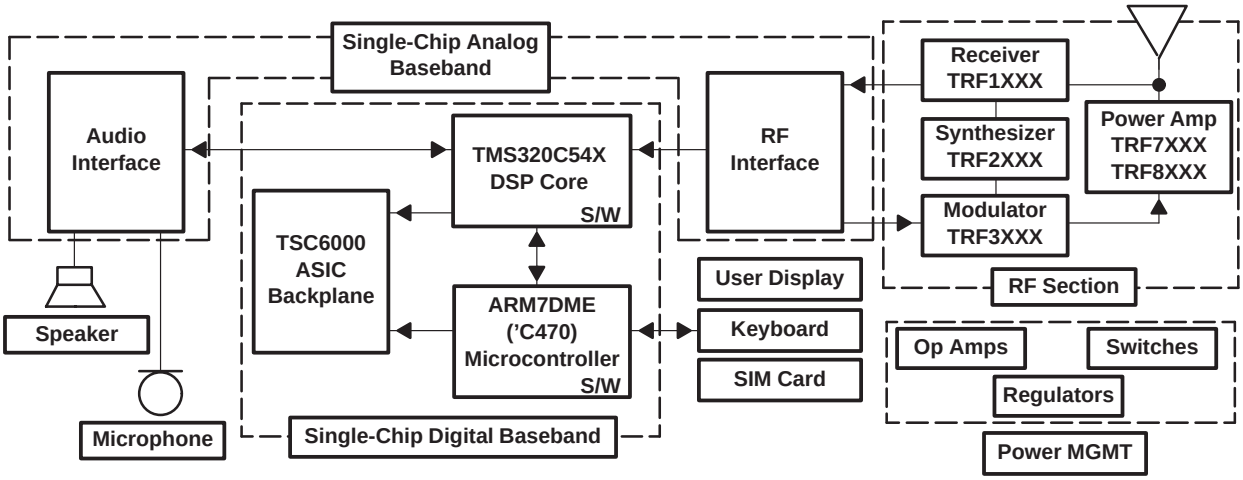


Figure 1. Single-Chip Digital Baseband Platform

The customizable platform helps wireless digital telephone manufacturers achieve lower component counts, save board space, reduce power consumption, introduce new features, save development costs, and achieve faster time to market, while still giving them the flexibility and performance to support any standard worldwide.

1.2 Analog Baseband Components

TI analog baseband components provide a mixed-signal bridge between the world of analog signals and digital signal processors, the key technology of the digital wireless industry. Using a seamless architecture for wireless communications technology, TI matches its baseband interfaces, radio frequency integrated circuits (ICs), and power management ICs to digital signal processing engines to create complete DSP solutions for digital wireless systems.

1.3 Power Management

Texas Instruments provides power management solutions with integration levels that meet the needs of a wide range of wireless applications. From discrete low drop-out (LDO) voltages and voltage supervisors to complete power supplies for the baseband section, TI power management solutions play an important role in increasing wireless battery life and system functionality and decreasing time to market.

For more information, visit the TI Wireless Communications web site at www.ti.com/sc/docs/wireless/home.htm.

1.4 Evaluation Board

The TRF3040 evaluation board consists of a multilayer printed circuit board (PCB) with all the required components. The following information is included in this document to aid in the assessment of this device:

- TRF3040 functional block diagram
- TRF3040 evaluation board mechanical outline
- TRF3040 evaluation board schematic
- TRF3040 evaluation board parts list
- TRF3040 engineering notes
- TRF3040 test results
- TRF3040 software driver

A DOS-based software driver is supplied with the evaluation board. When the program is executed, the program screen divides into five main sections:

- Main Loop
- Auxiliary Loop
- Modulator
- Device
- Editing

A variety of external test equipment can be used with the TRF3040 evaluation board, such as the following:

- IBM™ computer or compatible PC with a parallel port
- Linear dc power supply
- Differential in-phase/quadrature (I/Q) signal generator

- Spectrum analyzer
- Vector signal analyzer

The TRF3040 evaluation board is described in Section 2, *TRF3040 Evaluation Board*.

1.5 Related Documentation

The following list specifies product names, part numbers, and literature numbers of related TI documentation.

*TRF3040 Modulator/Synthesize*r data sheet, literature number SLWS057

1.6 WorldWide Web

The TI WorldWide Web site at www.ti.com contains the most up-to-date product information including revisions and additions. You can register with TI&ME to build custom information pages and receive new product updates automatically via email.

1.7 E-mail

For technical issues or clarification on switching products, please send a detailed E-mail to sc-infomaster@ti.com. Questions receive prompt attention and are usually answered within one business day.

2 TRF3040 Evaluation Board

The TRF3040 evaluation board consists of a multilayer printed circuit board, a TRF3040 device, main channel and auxiliary channel voltage-controlled oscillators (VCO), an opto-isolated serial interface, voltage regulators, and necessary peripheral discrete components.

The main synthesizer circuit layout supports a Panasonic™ VCO or similar device. The auxiliary synthesizer circuit layout supports a Vari-L™ VCO190 Series VCO or similar device.

Figure 2 describes the TRF3040 device general functional block and related input/output terminals of the device; Figure 3 and Figure 4 present the functional block diagram of the frequency synthesizer and the modulator within the TRF3040 device, respectively. Figure 5 and Figure 6 show the mechanical outline of the TRF3040 evaluation board, and Figure 7 details the TRF3040 evaluation board schematic. Table 1 is a detailed parts list for the TRF3040 evaluation board.

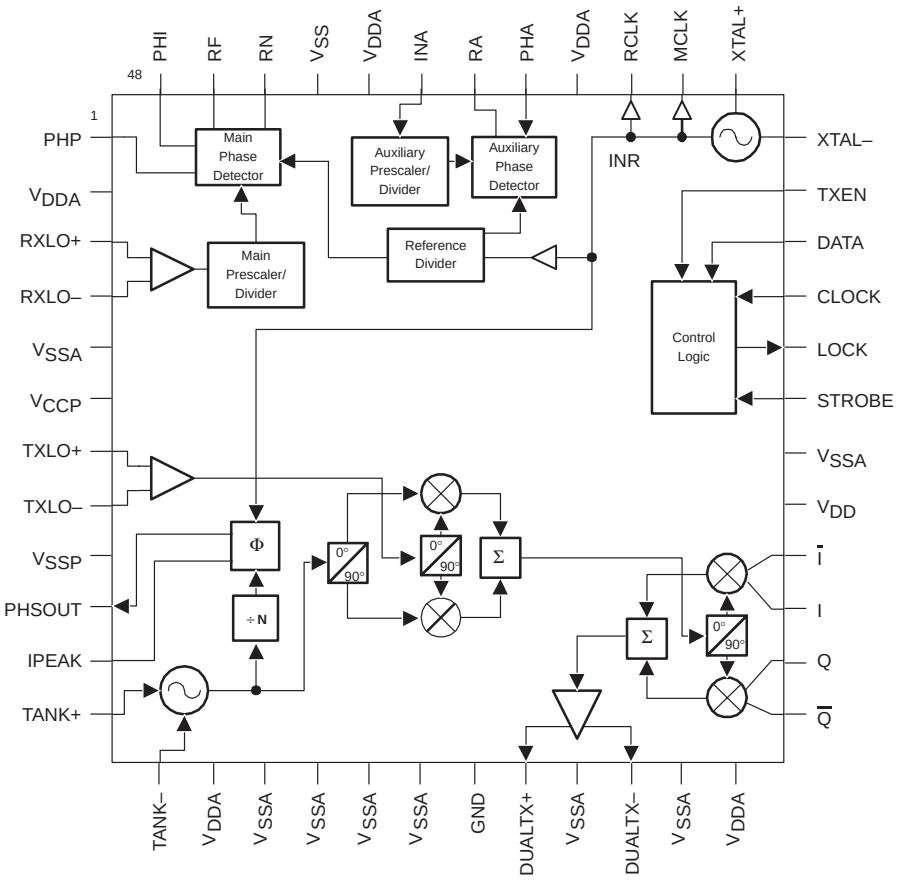


Figure 2. TRF3040 Functional Block Diagram

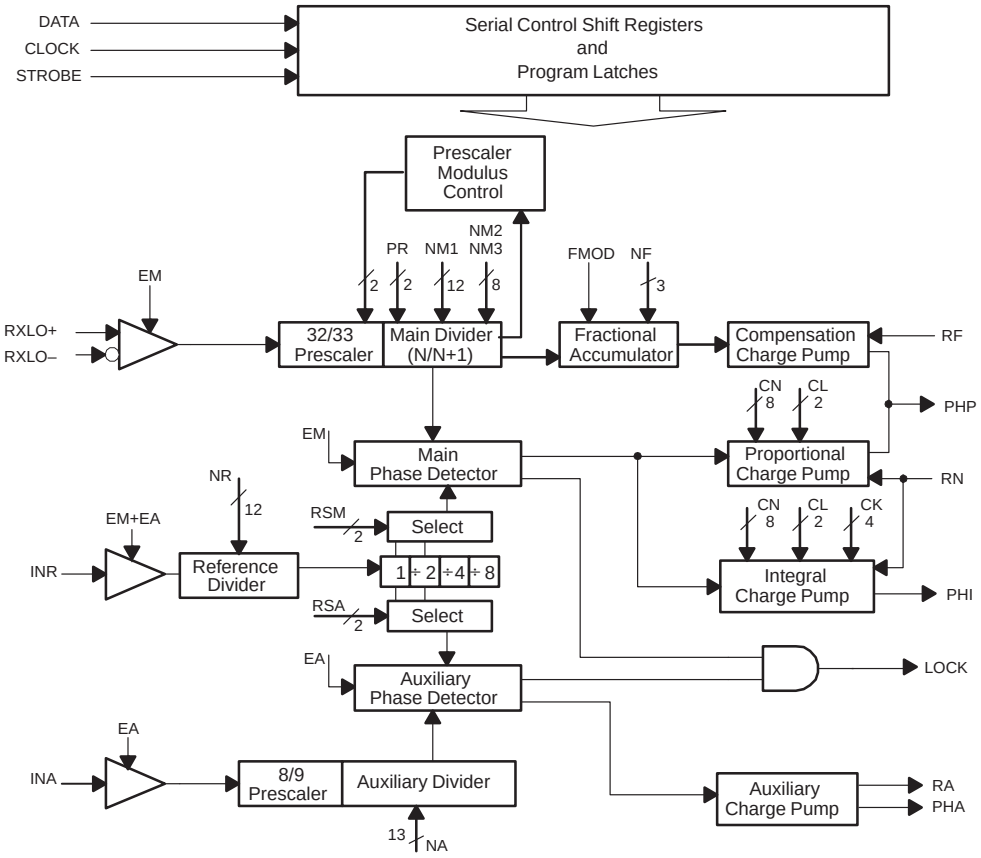


Figure 3. TRF3040 Synthesizer Functional Block Diagram

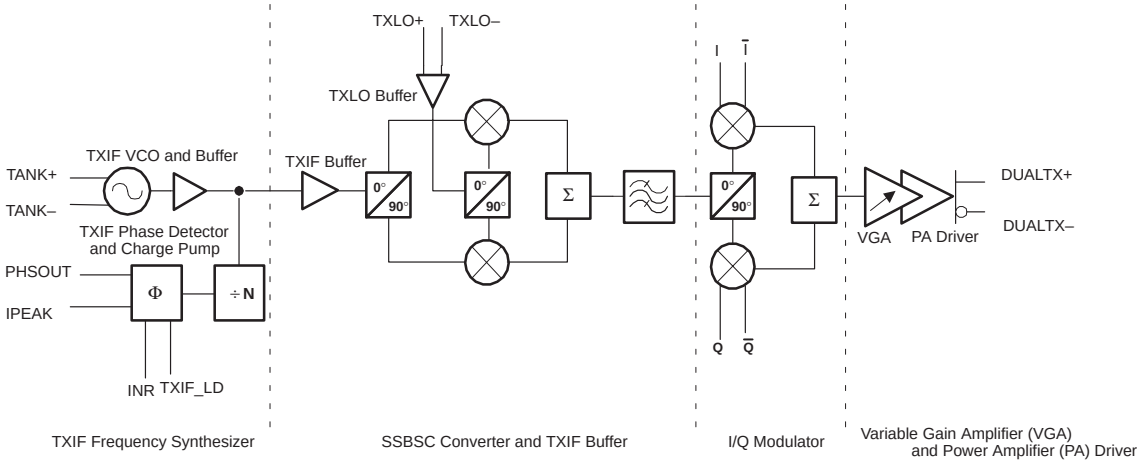
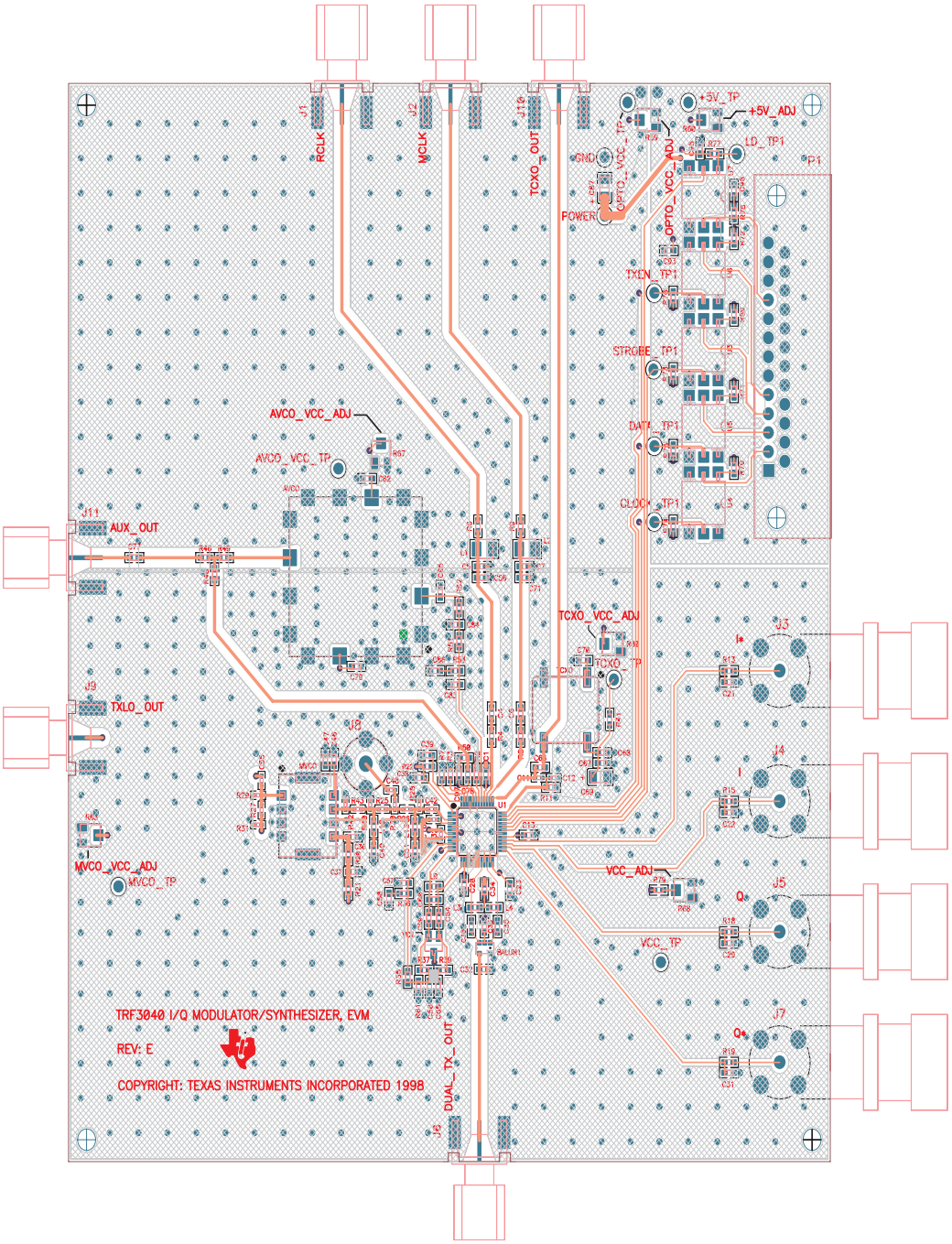
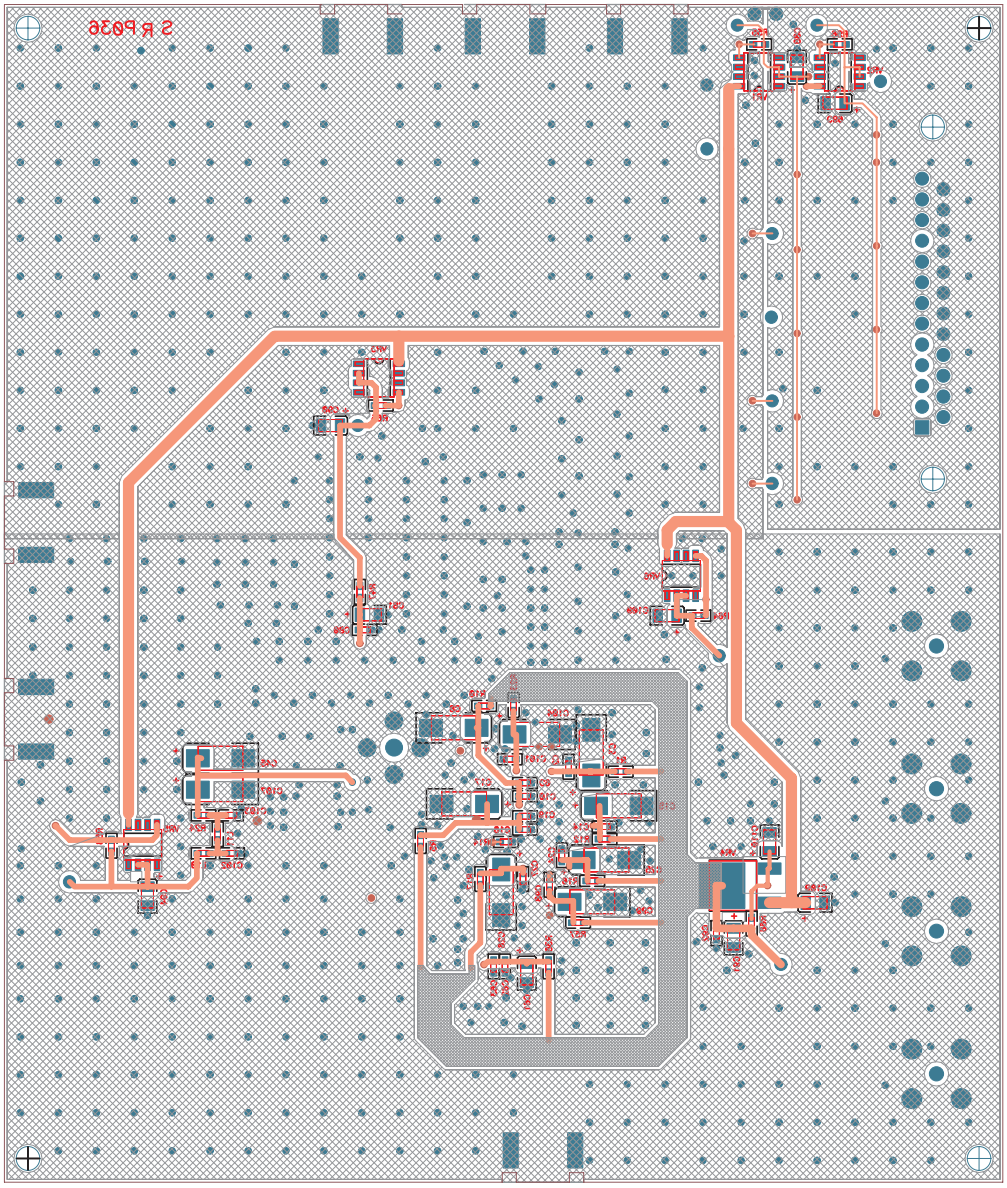


Figure 4. TRF3040 Modulator Functional Block Diagram



TRF3040 I/Q Modulator/Synthesizer, EVM Rev. E Copyright: Texas Instruments Incorporated, 1998
Top Side Silkscreen

Figure 5. TRF3040 Evaluation Board Layout (Component Side)



TRF3040 I/Q Modulator/Synthesizer, EVM Bottom Side Silkscreen

Rev. E

Figure 6. TRF3040 Evaluation Board Layout (Back Side)

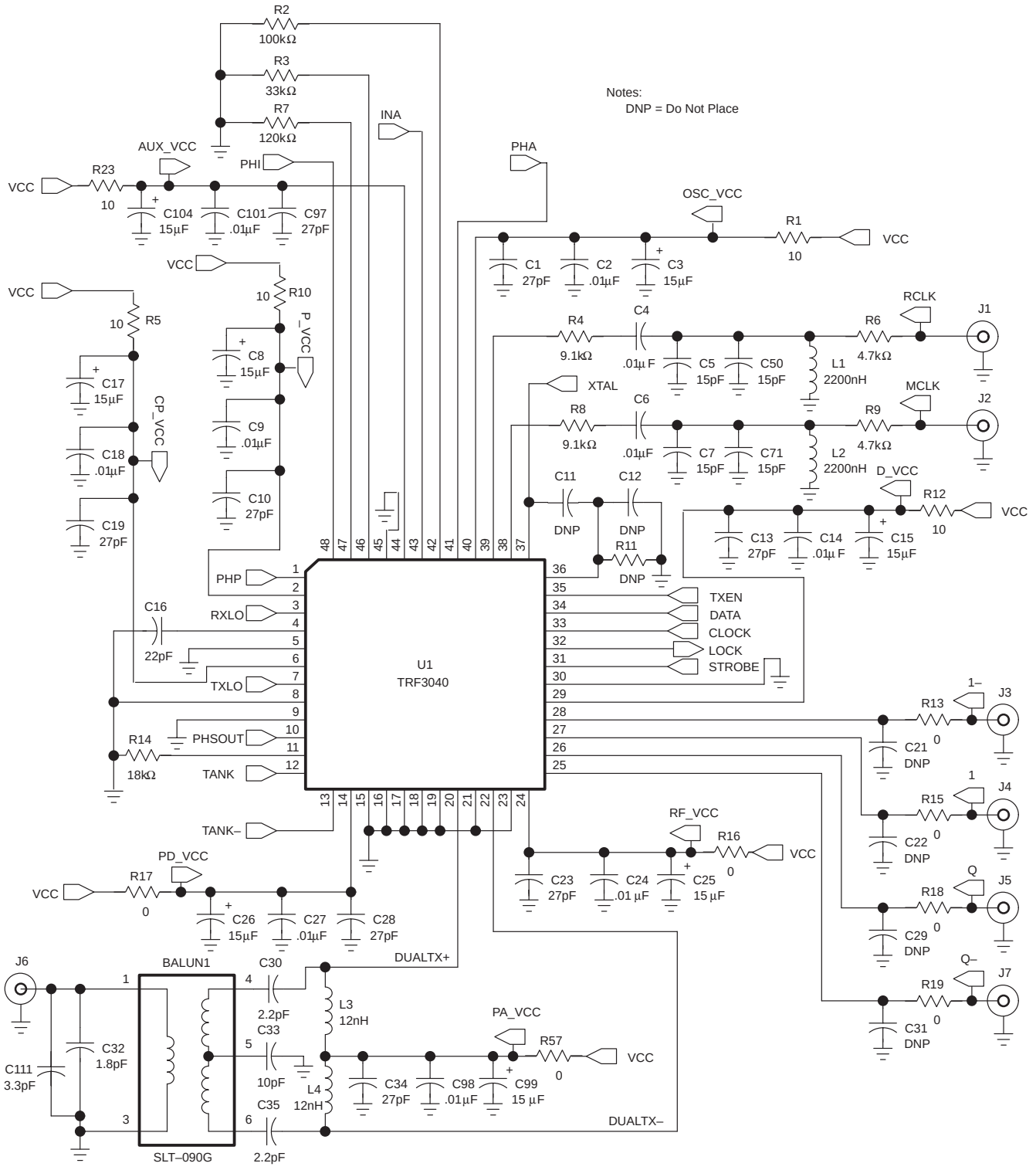


Figure 7. TRF3040 Evaluation Board Schematic (1 of 4)

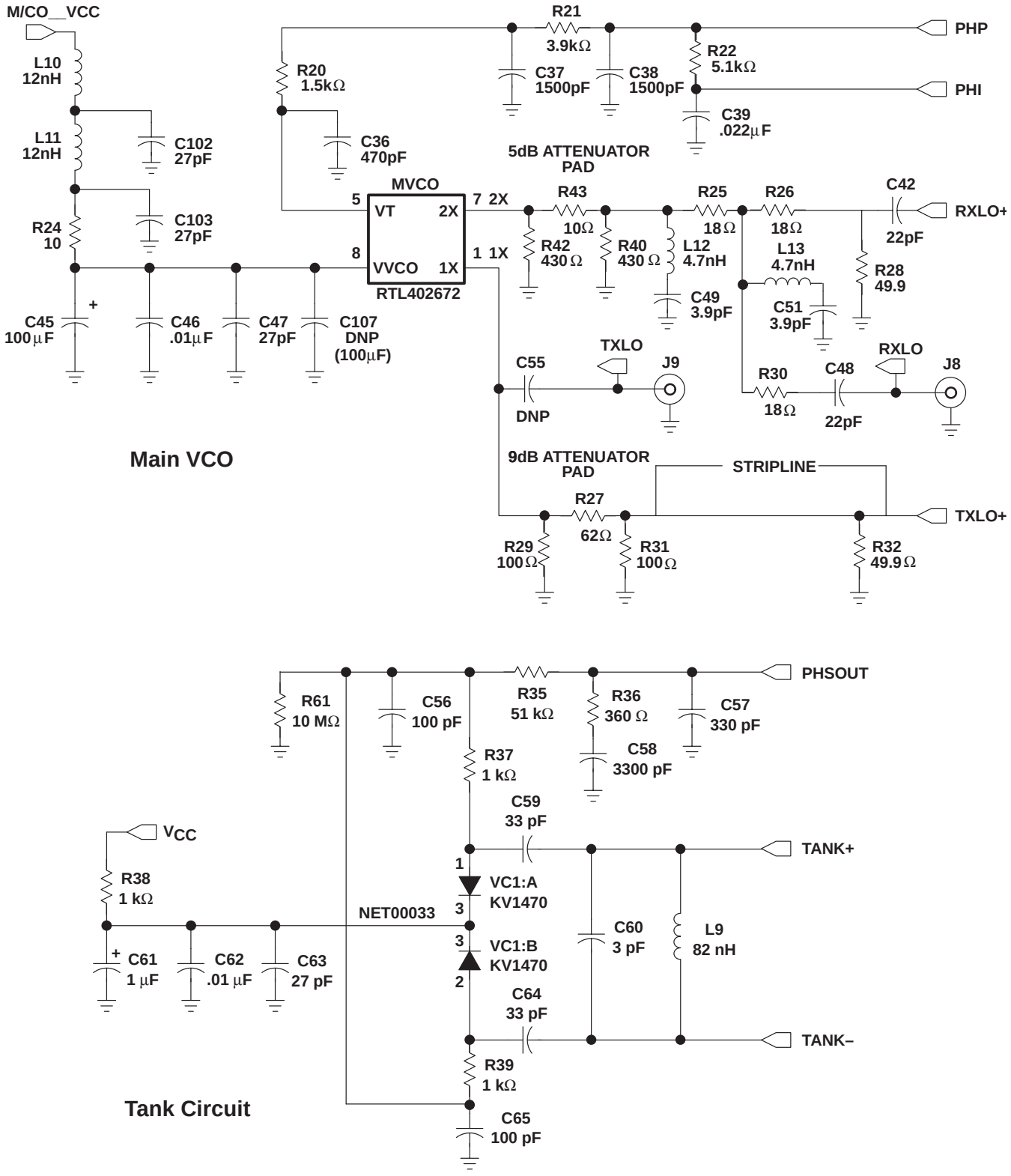


Figure 7. TRF3040 Evaluation Board Schematic (2 of 4) (Continued)

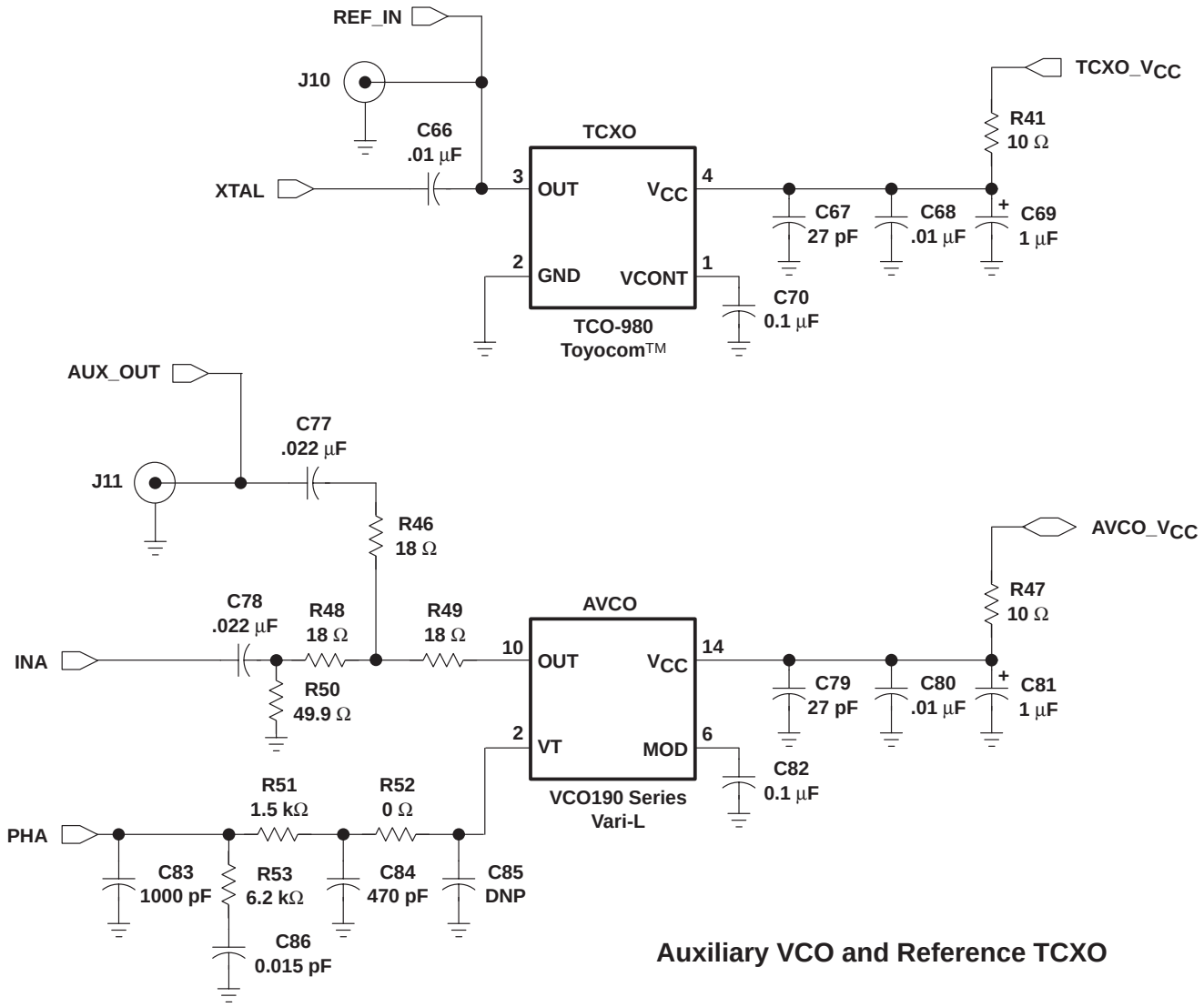


Figure 7. TRF3040 Evaluation Board Schematic (3 of 4) (Continued)

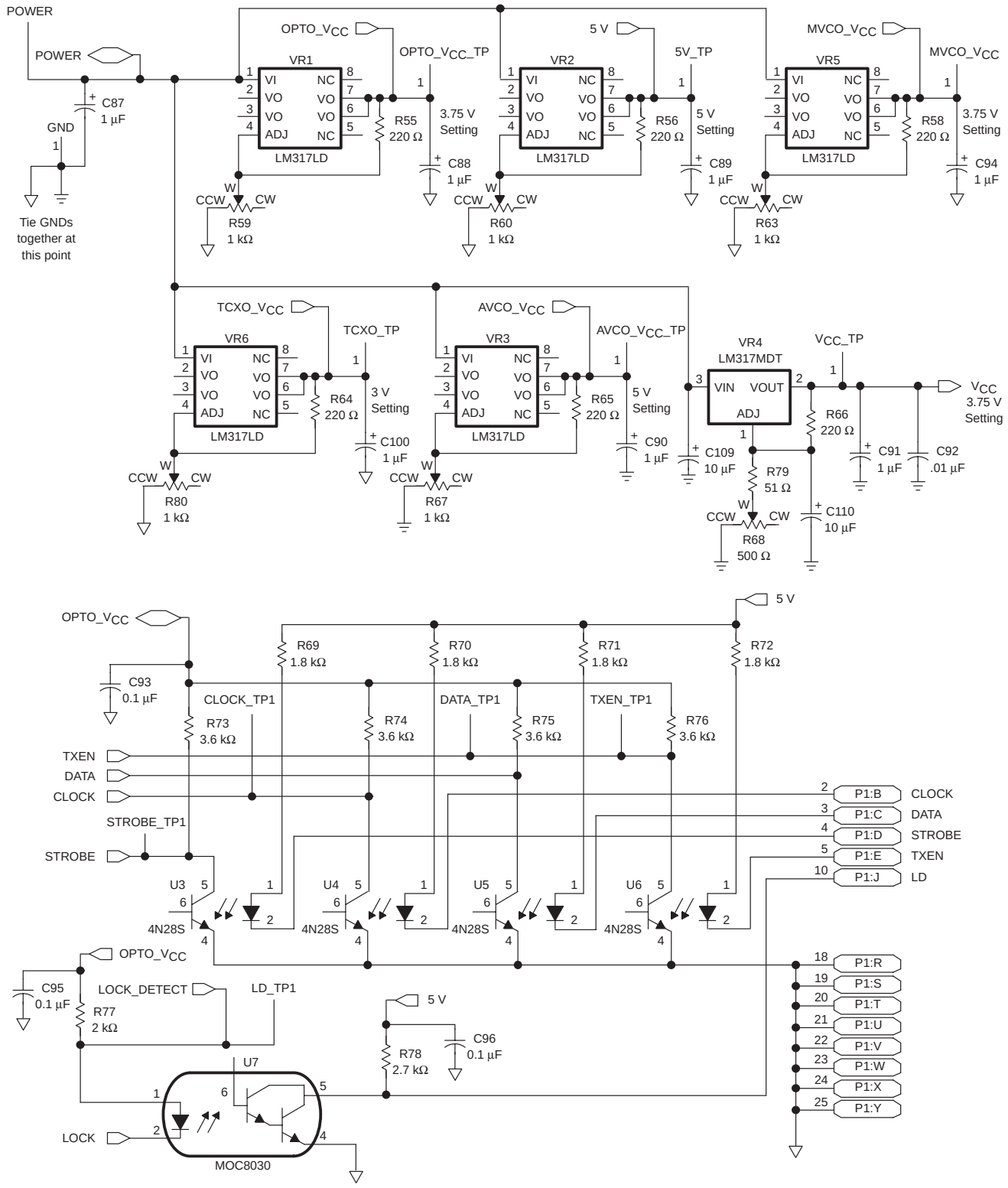


Figure 7. TRF3040 Evaluation Board Schematic (PC Interface and Evaluation Board DC Supply Circuitry Only) (4 of 4) (Continued)

Table 1. TRF3040 Evaluation Board Parts List

Designators	Description	Value	Qty	Size (mm)	Manufacturer	Manufacturer Part Number (P/N)
C 1, 10, 13, 19, 23, 28, 34, 47, 63, 67,79, 97, 102, 103	Capacitor	27 pF	14	0603	Murata™	GRM39COG series
C 2, 4, 6, 9, 14, 18, 24, 27,46, 62, 66, 68, 80, 92, 98, 101	Capacitor	0.01 μF	16	0603	Murata	GRM39COG series
C 3, 8, 15, 17, 25, 26, 99, 104	Tantalum capacitor	15 μF	8	6032–C	Venkel™	TA010TCM series
C 5, 7, 50, 71	capacitor	15 pF	4	0603	Murata	GRM39COG series
C 11, 12, 21, 22, 29, 31, 55, 85, 107	Capacitor	DNP	9			
C 16, 42, 48	Capacitor	22 pF	3	0402	Murata	GRM39COG series
C 30, 35	Capacitor	2.2 pF	2	0603	Murata	GRM39COG series
C 32	Capacitor	1.8 pF	1	0603	Murata	GRM39COG series
C 33	Capacitor	10 pF	1	0603	Murata	GRM39COG series
C 36, 84	Capacitor	470 pF	2	0603	Murata	GRM39COG series
C 37, 38	Capacitor	1500 pF	2	0603	Murata	GRM39COG series
C 39, 77, 78	Capacitor	0.022 μF	3	0603	Murata	GRM39COG series
C 45	Tantalum capacitor	100 μF	1	6032-C	Venkel	TA010TCM series
C 49, C51	Capacitor	3.9 pF	1	0603	Murata	GRM39COG series
C 55	Capacitor	DNP	1	0402		
C 56, 65	Capacitor	100 pF	2	0603	Murata	GRM39COG series
C 57	Capacitor	330 pF	1	0603	Murata	GRM39COG series
C 58	Capacitor	3300 pF	1	0603	Murata	GRM39COG series
C 59, 64	Capacitor	33 pF	2	0603	Murata	GRM39COG series
C 60	Capacitor	3 pF	1	0603	Panasonic	ECU-V1 series
C 61, 69, 81, 87, 88, 89, 90, 91, 94, 100	Tantalum capacitor	1 μF	10	3216-A	Venkel	TA010TCM series
C 70, 82, 93, 95, 96	Capacitor	0.1 μF	5	0603	Murata	GRM39COG series
C 83	Capacitor	1000 pF	1	0603	Murata	GRM39COG series
C 86	Capacitor	0.015 μF	1	0603	Murata	GRM39COG series
C 109, 110	Tantalum capacitor	10 μF	2	3216-A	Venkel	TA010TCM series
C 111	Capacitor	3.3 pF	1	0603	Murata	GRM39COG series
J 8	SMA-V		1		EFJohnson™	142-0701-201
L 1, 2	Inductor	2200 nH	2	1008	Coilcraft™	0603HS series
L 3, 4, 10, 11	Inductor	12 nH	4	0603	Coilcraft	0603HS series
L 12, 13	Inductor	4.7 nH	1	0603	Coilcraft	0603HS series
L 9	Inductor	82 nH	1	0603	Coilcraft	0603HS series
R 1, 5, 10, 12, 23, 24, 41, 47	Resistor	10 Ω	8	0603	Panasonic	ERJ-3GSYJ series
R 2	Resistor	100K	1	0603	Panasonic	ERJ-3GSYJ series

Table 1. TRF3040 Evaluation Board Parts List (Continued)

Designators	Description	Value	Qty	Size (mm)	Manufacturer	Manufacturer Part Number (P/N)
R 3	Resistor	33 kΩ	1	0603	Panasonic	ERJ-3GSYJ series
R 4, 8	Resistor	9.1 kΩ	2	0603	Panasonic	ERJ-3GSYJ series
R 6, 9	Resistor	4.7 kΩ	2	0603	Panasonic	ERJ-3GSYJ series
R 7	Resistor	120 kΩ	1	0603	Panasonic	ERJ-3GSYJ series
R 11	Resistor	DNP	1	0603	Panasonic	ERJ-3GSYJ series
R 13, 15, 16, 17, 18, 19, 52, 57	Resistor	0	8	0603	Panasonic	ERJ-3GSYJ series
R 14	Resistor	18 kΩ	1	0603	Panasonic	ERJ-3GSYJ series
R 20, 51	Resistor	1.5 kΩ	2	0603	Panasonic	ERJ-3GSYJ series
R 21	Resistor	3.9 kΩ	1	0603	Panasonic	ERJ-3GSYJ series
R 22	Resistor	5.1 kΩ	1	0603	Panasonic	ERJ-3GSYJ series
R 25, 26, 30	Resistor	18 Ω	3	0402	Panasonic	ERJ-2GEJ series
R 27	Resistor	62 Ω	1	0402	Panasonic	ERJ-2GEJ series
R 28, 32	Resistor	49.9 Ω	2	0402	Panasonic	ERJ-2GEJ series
R 29, 31	Resistor	100 Ω	2	0402	Panasonic	ERJ-2GEJ series
R 40, 42	Resistor	430 Ω	2	0402	Panasonic	ERJ-2GEJ series
R 46, 48, 49	Resistor	18 Ω	3	0603	Panasonic	ERJ-3GSYJ series
R 50	Resistor	49.9 Ω	1	0603	Panasonic	ERJ-3GSYJ series
R 35, 79	Resistor	51 Ω	2	0603	Panasonic	ERJ-3GSYJ series
R 36	Resistor	360 Ω	1	0603	Panasonic	ERJ-3GSYJ series
R 37, 38, 39	Resistor	1 kΩ	3	0603	Panasonic	ERJ-3GSYJ series
R 43	Resistor	10 Ω	1	0402	Panasonic	ERJ-2GEJ series
R 53	Resistor	6.2 kΩ	1	0603	Panasonic	ERJ-3GSYJ series
R 55, 56, 58, 64, 65, 66	Resistor	220 Ω	6	0603	Panasonic	ERJ-3GSYJ series
R 59, 60, 63, 67, 80	Trimming potentiometer	1 kΩ	5	3313J	Bourns™	3313J-1-102E
R 61	Resistor	10 MΩ	1	0805	Panasonic	ERJ-3GSYJ series
R 68	Trimming potentiometer	500 Ω	1	3313J	Bourns	3313J-1-102E
R 69, 70, 71, 72	Resistor	1.8 kΩ	4	0603	Panasonic	ERJ-3GSYJ series
R 73, 74, 75, 76	Resistor	3.6 kΩ	4	0603	Panasonic	ERJ-3GSYJ series
R 77	Resistor	2 kΩ	1	0603	Panasonic	ERJ-3GSYJ series
R 78	Resistor	2.7 kΩ	1	0603	Panasonic	ERJ-3GSYJ series
U 1	Integrated circuit		1	0603	Texas Instruments	TRF3040
U 3, 4, 5, 6	Optocoupler		4	0603	Motorola™	4N28S
U 7	Optocoupler		1	0603	Motorola	MOC8030
VC 1	Varactor		1		Toko™	KV1470
VR 1, 2, 3, 5, 6	Voltage regulator		5		Motorola	LM317LD
VR 4	Voltage regulator		1		Motorola	LM317MDT
BALUN 1	Transformer	4:1	1		Hitachi™	SLT-090G
P 1	DB25M		1		AMP™	747238-4
J 1, 2, 6, 9, 10, 11	SMA_H		7		EFJohnson	142-0701-831
J 3, 4, 5, 7	BNC-90		4		AMP	413631-1

Table 1. TRF3040 Evaluation Board Parts List (Continued)

Designators	Description	Value	Qty	Size (mm)	Manufacturer	Manufacturer Part Number (P/N)
MVCO	Voltage-controlled oscillator		1		Panasonic	RTL402672
AVCO	Voltage-controlled oscillator		1		Vari–L	VCO190 Series
TCXO	Temperature-compensated Crystal oscillator		1		Toyocom™	TCO-980 series
CLOCK_TP1 DATA_TP1 LD_TP1 TXEN_TP1 STROBE_TP1 MVCO_TP OPTO_VCC_TP +5V_TP AVCO_VCC_TP TXCO_TP VCC_TP POWER GND	Test Probe Connector		13		Components Corporation™	TP-105-01 series

2.1 External Power

External power is connected to the evaluation board at the test points POWER and GND. TI recommends that you use a linear power supply set at 8.6 VDC for external power.

2.2 Voltage Regulators

The on-board adjustable regulators provide independent, linear voltage regulation to the TRF3040 device, the main VCO, the auxiliary VCO, and the serial interface optocouplers. Tantalum capacitors are used to enhance ripple and noise rejection in the regulators.

The voltage regulators are factory set as follows:

VR1 (OPTO_VCC) = 3.75 VDC
VR2 (+5 V) = 5.0 VDC
VR3 (AVCO_VCC) = 5.0 VDC
VR4 (VCC) = 3.75 VDC
VR5 (MVCO_VCC) = 3.75 VDC
VR6 (TCXO_VCC) = 3.0 VDC

2.3 Serial Interface

A DB25M connector, P1, is provided for connection to a standard PC parallel port using a 25-pin conductor cable. The PC parallel port is used to emulate a synchronous serial data interface consisting of CLOCK, DATA, and STROBE. The LOCK signal is fed back to the PC parallel port to indicate synthesizer loop lock status of the TRF3040 board. The TXEN signal is controlled by the emulated microprocessor signal from the PC parallel port. The three serial interface signals, the LOCK signal, and the TXEN signal are all opto-isolated from the PC parallel port. In this manner, the TRF3040 device may be operated at a supply voltage that is different from the standard 5-VDC voltage level of the PC parallel port.

The serial interface signals are routed to the P1 connector as follows:

CLOCK: P1–2

DATA: P1–3

STROBE: P1–4

LOCK: P1–10

TXEN: P1–5

2.4 External Reference

A temperature-compensated crystal oscillator (TCXO) is factory installed on the TRF3040 evaluation board. Alternately, an external signal generator can be used to provide the reference signal (XTAL+) via the SMA connector J10 (TCXO_OUT). Typically, a low-phase noise, stable, synthesized signal generator such as an HP8665 or similar device should be used as an external reference. For typical Advanced Mobile Phone Service (AMPS)/Digital Advanced Mobile Phone Service (DAMPS) applications, a 19.44-MHz signal at –6 dBm is suitable.

3 TRF3040 Evaluation Board Engineering Notes

The TRF3040 evaluation board is designed for a single-band/dual-mode system, as suggested in Figure 8; however, it is possible to use the TRF3040 board in a dual-band system with an external high-band converter in the transmitter path. Figure 9 outlines a dual-band system architecture block diagram using the TRF3040 modulator/synthesizer with the TRF1500 dual-band receiver and the TRF700X/TRF761X power amplifier (PA) families from Texas Instruments Incorporated.

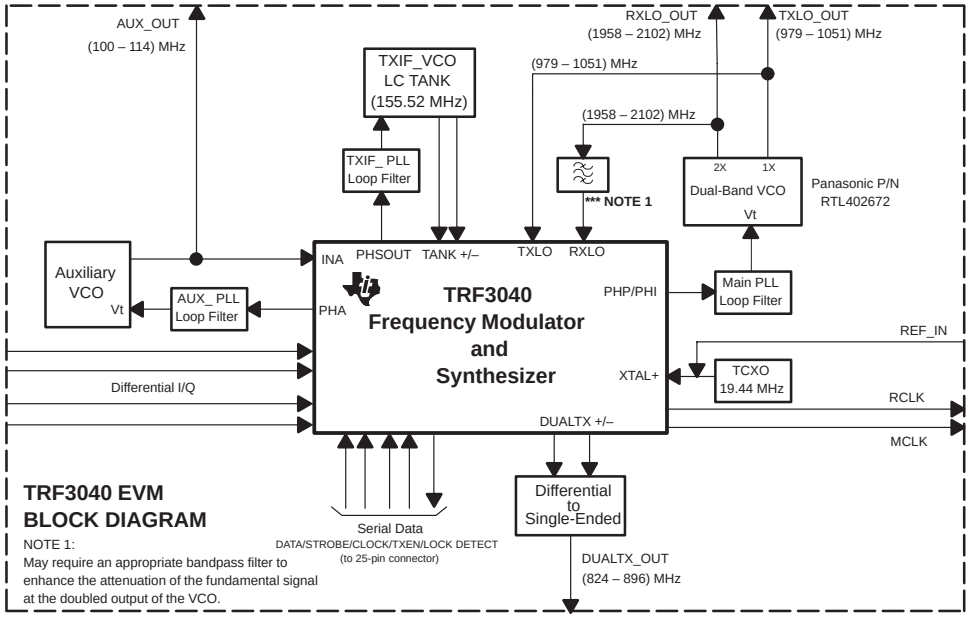


Figure 8. Single-Band System Using the TRF3040 Device

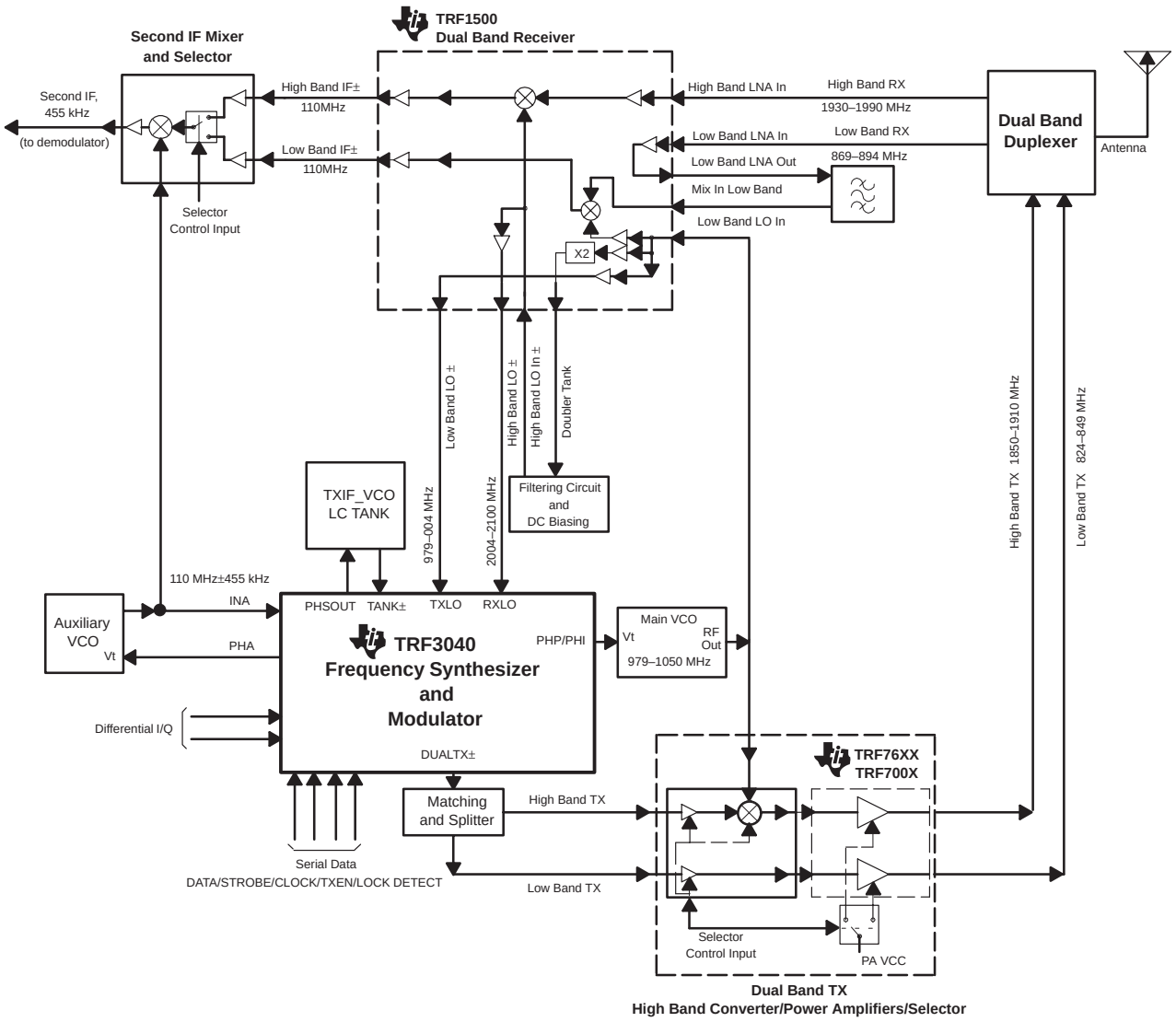


Figure 9. Dual-Band System Using the TRF3040 Device

3.1 TRF3040 Frequency Synthesizer

The TRF3040 frequency synthesizer consists of a 2.2-GHz main synthesizer and a 200-MHz auxiliary synthesizer. The main synthesizer incorporates a dual-mode 32/33 and 64/65 prescaler for integer-N and/or fractional-N operation. Fractional spur suppression is optimized through the programmable compensation.

3.1.1 Voltage-Control Oscillator (VCO)

Because the TRF3040 frequency synthesizer operates up to 2.16-GHz, TI recommends that you select or design a stable and low-phase noise VCO for a high-performance phase-locked loop (PLL).

3.1.2 Synthesizer Input RXLO+/–

The synthesizer input RXLO+/– can use a differential or a single-ended input. For simplicity, TI recommends a nominal –17 dBm at the RXLO+ port for single-ended configuration.

3.1.3 Loop Filters

This section details the main and auxiliary loop filter design equations for the TRF3040 device.

3.1.3.1 Main Loop Filter Design

Fractional spurs, phase noise, and lock time are some of the many concerns of the PLL performance. These concerns depend not only on the phase detector and the VCO characteristics, but on the loop filter performance as well. Figure 10 describes the main loop filter configuration used on the TRF3040 evaluation board.

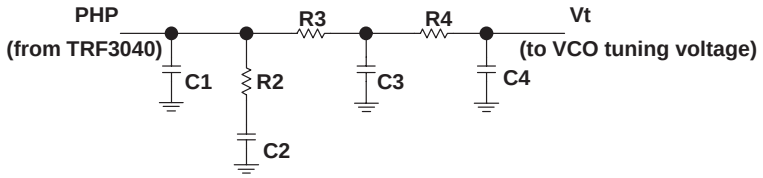


Figure 10. Main Loop Filter Configuration Used on the TRF3040 Board

The component values for the main loop filter are calculated based on the formulas derived by Wing S. Djen [2], as follows:

Requirements and Conditions:

f_{VCO} = 2051 to 2101 MHz VCO operating frequency

f_{CH} = 30 kHz channel spacing

f_{REF} = 240 kHz reference frequency

K_{VCO} = 80 MHz/V VCO gain

K_{PD} = 550 μA/2π radian phase detector gain

Frequency error after settling ≤ 1 kHz

Lock time (t_{SW}) ≈ 1 ms for a transition of 50 MHz

Calculations:

The divide ratio is calculated as:

$$N = f_{VCO} \div f_{REF} \quad (1)$$

$$= (2051 \text{ to } 2101) \text{ MHz} \div 240 \text{ kHz}$$

$$= (8545 \text{ to } 8758)$$

Let N = 8758 because transitioning from the high end to the low end of the band requires more time than transitioning from the low end to the high end of the band.

The final frequency resolution after settling is calculated as:

$$\delta = \text{Frequency error after settling} \div \text{Transition step} \quad (2)$$

$$= 1^{e3} \div 50^{e6} = 20^{e-6}$$

Choosing the damping factor, ξ, to be 0.707, the natural frequency is:

$$\varpi_N = -\ln(\delta \times \xi) \div (\xi \times t_{sw}) \quad (3)$$
$$= -\ln\left(20^{e-6} \times 0.707\right) \div \left(0.707 \times 1^{e-3}\right) = 15.794^{e+3}$$

NOTE: The damping factor of the loop, ξ, is not exactly 0.707; therefore, some empirical tuning may be required to avoid under-damped or over-damped situations.

The capacitor C_2 is calculated as:

$$C_2 = \left(K_{PD} \times K_{VCO}\right) \div \left(N \times \varpi_N^2\right) \quad (4)$$
$$= \left(550^{e+6} \times 80^{e+6}\right) \div \left(8758 \times \left(15.794^{e+3}\right)^2\right) = 20.14^{e-9}\ \text{F}$$

And the resistor R_2 is calculated as:

$$R_2 = 2 \times \xi \times \text{SQRT}\left(N \div \left(K_{PD} \times K_{VCO} \times C_2\right)\right) \quad (5)$$
$$= 2 \times 0.707 \times \text{SQRT}\left(8758 \div \left(550^{e-6} \times 80^{e+6} \times 20.14^{e-9}\right)\right)$$
$$= 4.45\ \text{k}\Omega$$

When $C_1 \leq 1/10 \times C_2$; therefore:

$$C_1 \leq 2000\ \text{pF} \quad (6)$$

For further attenuating the spur at $f_{VCO} \pm f_{CH}$ and $f_{VCO} \pm f_{REF}$, the values of C_3, R_3, C_4, and R_4 are calculated with resonant frequencies at least five times greater than the natural frequency, ω_N, in order to avoid interaction between poles that would cause oscillation. Choosing R_3 = 3.9 kΩ, the value of C_3 is calculated as:

$$\varpi_{30K} = 1 \div \left(R_3 \times C_3\right) \quad (7)$$
$$C_3 = 1 \div \left(2 \times \pi \times 30^{e+3} \times 3.9^{e+3}\right) = 1360\ \text{pF}$$

Similarly, choosing R_4 = 1.5 kΩ, the value of C_4 is calculated as:

$$\varpi_{240K} = 1 \div \left(2 \times \pi \times 240^{e+3} \times 1.5^{e+3}\right) = 442\ \text{pF} \quad (8)$$

Because most calculated values are not available as standard values, the closest value is selected. Finalized component values for the main loop filter are summarized in Table 2.

Table 2. Main Loop Filter Component Values

Reference Designator	Loop Filter Component Value (Lock Time ≈ 1 ms)
C1	1500 pF
C2	0.022 µF
C3	1500 pF
C4	470 pF
R2	5.1 kΩ
R3	3.9 kΩ
R4	1.5 kΩ

3.1.3.2 Auxiliary Loop Filter Design

Similar to the main loop filter, the auxiliary loop filter is defined as follows:

Assumptions:

The auxiliary PLL uses the Vari-L VCO190-150 with K_{VCO} = 7.8 MHz/V.

The phase-detector gain, $K_{PD,}$ is set to 250 mA/2π radians.

The operating frequency, $f_{VCO,}$ is 108 MHz.

The reference frequency, $f_{REF,}$ is 240 kHz.

The frequency error after settling is ≤ 1 kHz.

The lock time, $t_{SW,}$ is 1 ms for a transition of 50 MHz.

All reference designators are illustrated in Figure 7, the TRF3040 EVM schematic.

Calculations:

The divide ratio is calculated as follows:

$$N = f_{VCO} \div f_{REF} \quad (9)$$

$$= 108\ \text{MHz} \div 240\ \text{kHz} = 450$$

The final frequency resolution after settling is:

$$\delta = \text{Frequency error after settling} \div \text{Transition step} \quad (10)$$

$$= 1^{e+3} \div 50^{e+6} = 20^{e-6}$$

Choose the damping factor, ξ, to be 0.707. The natural frequency is:

$$\varpi_N = -\ln(\delta \times \xi) \div (\xi \times t_{sw}) \quad (11)$$

$$= -\ln\left(20^{e-6} \times 0.707\right) \div \left(0.707 \times 1^{e-3}\right)$$

$$= 15.794^{e+3}$$

The capacitor C_{86} is calculated as:

$$C_{86} = \left(K_{PD} \times K_{VCO}\right) \div \left(N \times \varpi_N^2\right) \quad (12)$$

$$= \left(250^{e-6} \times 7.8^{e+6}\right) \div \left(450 \times \left(15.794^{e+3}\right)^2\right)$$

$$= 17.37\ \text{nF}$$

And the resistor R_{53} is calculated as:

$$R_{53} = 2 \times \xi \times \text{SQRT}\left(N \div \left(K_{PD} \times K_{VCO} \times C_{86}\right)\right) \quad (13)$$

$$= 2 \times 0.707 \times \text{SQRT}\left(450 \div \left(250^{e-6} \times 7.8^{e+6} \times 17.37^{e-9}\right)\right)$$

$$= 5.15^{e+3}\Omega$$

When $C_{83} \le 1/10 \times C_{86}$; therefore:

$$C_{83} \le 1737\ \text{pF} \quad (14)$$

For further attenuating the spur at $f_{VCO} \pm f_{REF}$, the values of C_{84} and R_{51} are calculated with the resonant frequencies at least 10 times greater than the natural frequency ω_N. For example, R_{51} = 1.5 kΩ. The value of C_{84} is calculated as:

$$\varpi_{240K} = 1 \div R_{51} \times C_{84} \quad (15)$$

$$C_{84} = 1 \div \left(2 \times \pi \times 240^{e+3} \times 1.5^{e+3}\right) = 442 \text{ pF}$$

Because most calculated values are not the ones available by the standard, the closest value is selected. Table 3 summarizes the values used on the TRF3040 evaluation board.

Table 3. Auxiliary Loop Filter Component Values

Reference Designator	Loop Filter Component Value
C83	1000 pF
C86	0.015 μF
C84	470 pF
R53	6.2 kΩ
R51	1.5 kΩ

3.1.4 Fractional Compensation and Charge Pump Current Setting

Assuming that a main PHP charge pump current of 288 μA and a current setting factor, CN, of 128 are desired, the value of the charge pump setting resistor is calculated as follows (the 3040 evaluation board RN resistor is 33 kΩ):

$$\text{RN(k}\Omega) = \left(18.75 \times \frac{128}{256} \times \frac{1}{\text{I(mA)}}\right) - 0.75 = 32.55 \text{ k}\Omega \quad (16)$$

Depending on the operating frequency bandwidth, the fundamental fractional-N pulse-width and the magnitude of the fundamental compensation charge pump current can be calculated. With a desired charge pump current of 288 μA, the fractional compensation charge pump current setting resistor, RF, of 120 kΩ is selected (see the *TRF3040 Modulator/Synthesizer* data sheet, literature number SLWS057).

3.2 TRF3040 Modulator

The transmitter modulator generates a modulated RF signal in the 900-MHz range at a maximum power level of 9 dBm, which can be controlled over a 50-dB range. The single sideband suppressed carrier (SSBSC) converter and I/Q modulator are designed with highly linear mixers to implement modulation schemes that meet spectral purity requirements of AMPS and DAMPS cellular systems. The TXLO frequency is controlled by the main synthesizer, and the transmit intermediate frequency (TXIF) synthesizer provides the TXIF signal needed to translate the TXLO to the proper RF carrier signal. The I/Q modulator modulates the I/Q baseband signal and feeds it to the variable gain amplifier (VGA) and power amplifier (PA) driver.

3.2.1 Transmit IF VCO (TXIF_VCO)

The TXIF_VCO generates a signal in the 150-MHz range, which is used by the SSBSC converter to produce the carrier. To synthesize the TXIF_VCO signal, a simple varactor-controlled LC tank circuit is realized in conjunction with the on-chip ÷6/7/8/9 prescaler and phase detector to complete the synthesizer function. Figure 11 suggests a possible implementation.

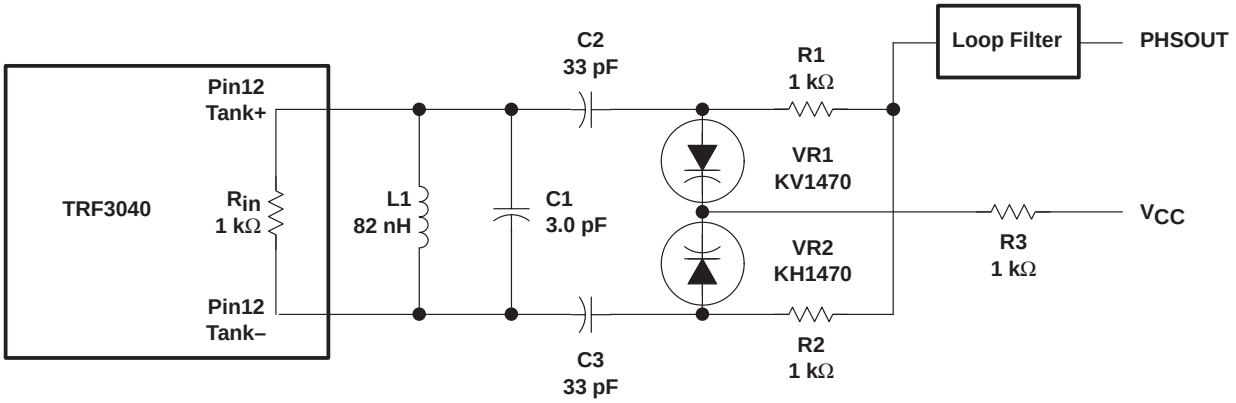


Figure 11. Typical Varactor-Controlled LC Tank Configuration

The tank resonant frequency is defined by the following formula:

$$f_{resonance} = \frac{1}{2\pi\sqrt{L1C1}} = 168.7\ \text{MHz} \quad (17)$$

Where:

$$C = C_1 + \left[\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_{VR1}} + \frac{1}{C_{VR2}}\right]^{-1},\ C_{VR} = \text{Varactor capacitance}$$

On the EVM board, the TXIF synthesizer operates with a 19.44-MHz reference frequency in a divide-by-8 prescaler mode. This operation yields a frequency of 155.52 MHz. The calculated tank resonant frequency is:

$$C_{VR1} = C_{VR2} = 60\ \text{pF (at 2.5 V measured on the EVM board)} \quad (18)$$

$$C = 3.0\ \text{pF} + \left[\frac{1}{33\ \text{pF}} + \frac{1}{33\ \text{pF}} + \frac{1}{30\ \text{pF}} + \frac{1}{30\ \text{pF}}\right]^{-1} = 10.68\ \text{pF} \quad (19)$$

$$L = 82\ \text{nH} \quad (20)$$

$$f_{resonance} = \frac{1}{2\pi\sqrt{L1C1}} = 168.7\ \text{MHz} \quad (21)$$

The oscillator frequency tuning range is approximately 42 MHz and is controlled by the varactor capacitance change when adjusted from 0 V to 3.75 V, as shown in Table 4.

Table 4. Oscillator Frequency Tuning Range

Varactor VR (V)	Varactor Capacitance (pF)	TXIF Calculated (MHz)	TXIF Measured (MHz)
0	120	139	130.52
2.50	30	169	155.52
3.75	23	178	173.80

The difference in frequency between the calculated and measured resonant frequency is attributed to the actual varactor capacitance, component tolerance, and board layout. High quality factor (Q) components are required because they affect the impedance seen by the TRF3040 modulator/synthesizer. The Q of inductor L1, the capacitors, and the varactors is critical because the selection of these components affects the attenuation that the tank circuit provides as it is loaded by the TRF3040 1-kΩ differential input impedance. An increase in attenuation reduces the tank resonant signal level and, if not designed properly, degrades the oscillator start-up properties.

An example of a loaded tank circuit is shown in Figure 12. The inductor and varactor have the lowest Q and therefore control the attenuation level.

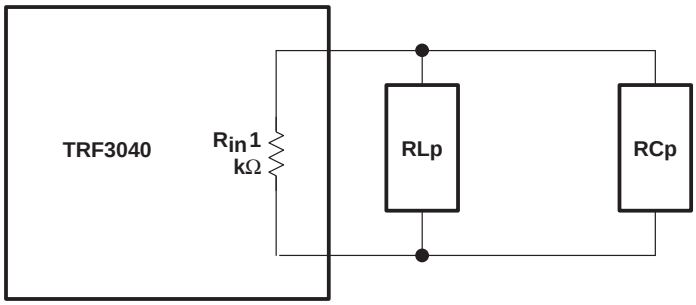


Figure 12. Example of a Loaded Tank Circuit

RL_p and RC_p are the equivalent parallel resistance of the inductor and the combined capacitance of the fixed capacitor and varactors for the condition when the tank is at resonance. The equivalent parallel resistance is defined as follows:

$$\text{If } Q > 10, \text{then } R_p = Q_2 R_S \tag{22}$$

Where:

R_p = Equivalent parallel resistance of the device at the resonant frequency

Q = Q of the device

R_S = Device series resistance = Reactance/Q

$R_{parallel}$ = Parallel resistance of RL_p and RC_p

$$\text{Attenuation, dB} = 20 \log\left[\frac{R_{parallel}}{R_{in} + R_{parallel}}\right] \tag{23}$$

As the component's Q decreases, R_p decreases and the attenuation increases. This effect reduces the tank oscillator signal which could affect the start-up. On the TRF3040 EVM board, the parameters of the tank circuit components are shown in the following equations:

$$R_S = \frac{X_L}{Q} = \frac{2\pi \times 155^{e+6} \times 82^{e-9}}{35} = 2.282\ \Omega \tag{24}$$

$$R_p = Q^2 R_S = 35^2 \times 2.28 = 2795.08\ \Omega \tag{25}$$

$$Q = \frac{X_C}{R_S} = \frac{1}{2\pi \times 155^{e+6} \times 60^{e-12} \times 35} = 34.227 \quad (26)$$

$$R_p = Q^2 R_S = 34.2^2 \times 0.5 = 585.74\ \Omega \quad (27)$$

$$R_S = \frac{X_C}{Q} = \frac{1}{2\pi \times 155^{e+6} \times 3^{e-12} \times 460} = 0.744\ \Omega \quad (28)$$

$$R_p = Q^2 R_S = 460^2 \times 0.74 = 157.443\ k\Omega \quad (29)$$

$$R_S = \frac{X_C}{Q} = \frac{1}{2\pi \times 155^{e+6} \times 33^{e-12} \times 1000} = 0.031\ \Omega \quad (30)$$

$$R_p = Q^2 R_S = 460^2 \times 0.74 = 31\ k\Omega \quad (31)$$

$$\text{Attenuation, dB} = 20 \log\left[\frac{RL_p}{RL_p + R_{in}}\right] = 20 \log\left[\frac{2795}{2795 + 1000}\right] = 2.6\ \text{dB} \quad (32)$$

The combined equivalent parallel resistance for the series capacitors and the varactors is much greater than the equivalent resistance for the shunt inductor. This analysis concludes that the total amount of attenuation is dependent upon the inductor's Q since R_{in} for the TRF3040 is fixed at 1 kΩ differential. The tank circuit in the TRF3040 EVM board is designed with high Q components to ensure reliable operation of the TXIF oscillator.

3.2.2 Single Sideband Suppressed Carrier Converter

A 900-MHz to 1100-MHz TXLO signal is mixed with the TXIF_VCO signal at the SSBCS converter. Here, the lower sideband is generated to be the carrier, while the TXLO and the upper sideband are suppressed by an on-chip bandpass filter, as shown in the following equation:

$$\text{Carrier} = \text{TXLO–TXIF\_VCO} \quad (33)$$

3.2.3 I/Q Modulator

The carrier signal generated at the SSBSC converter is modulated with the baseband I/Q signals. Any type of complex modulation signal is therefore possible. The I/Q signals should have a common mode voltage of approximately VDDA/2.

3.2.4 Variable Gain Amplifier and the Power Amplifier Driver

The output of the I/Q modulator is fed to the DUALTX VGA and PA driver, which have a maximum power out of 9 dBm and a 50-dB dynamic range. There are 7 bits corresponding to 128 states. State 0 corresponds to maximum RF power, and state 127 corresponds to minimum power.

The DUALTX+/– outputs of the PA driver are configured as 200 Ω differential. For testing purposes, the DUALTX+/– outputs can be converted into a 50-Ω single-ended output with a 4:1 BALUN and the matching network, as shown in Figure 13.

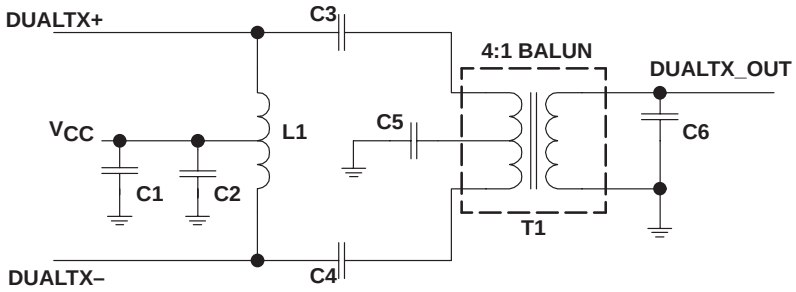


Figure 13. Typical Differential-to-Single-Ended Configuration

4 Typical Performance

Figure 14 illustrates the typical test setup for the TRF3040 device.

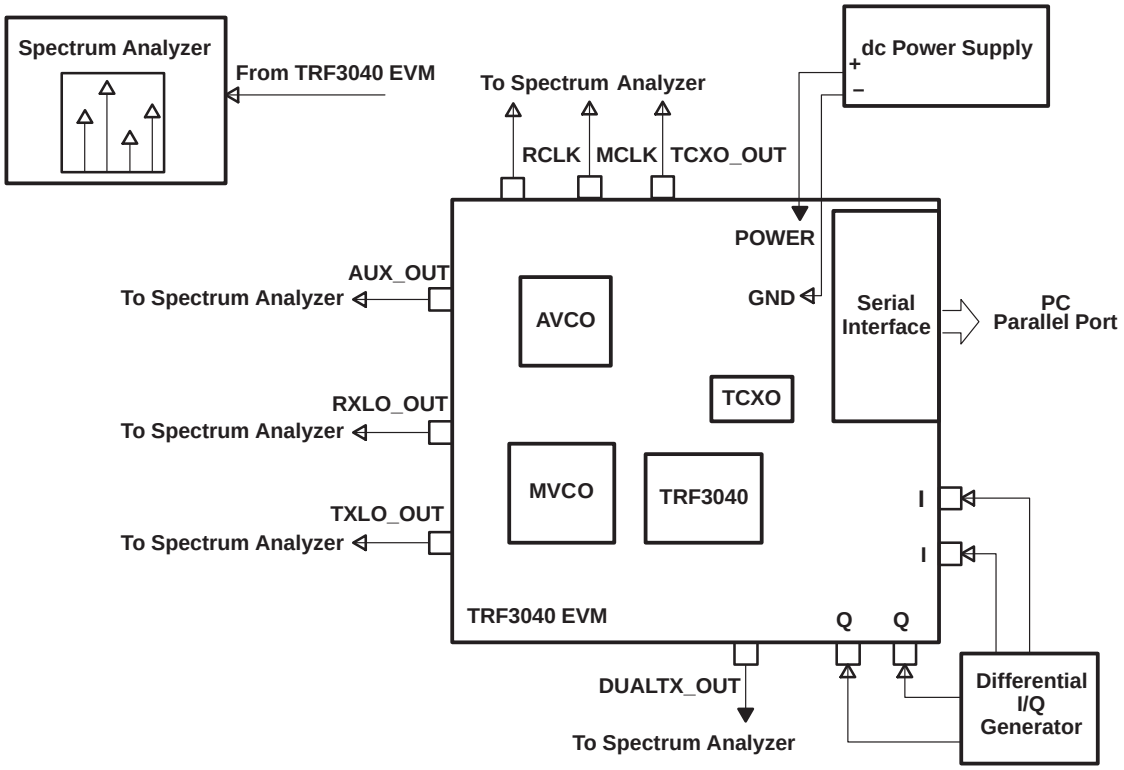


Figure 14. Typical Test Setup for the TRF3040 Evaluation Board

4.1 Settings

The following settings are recommended to demonstrate the capabilities of the TRF3040 device:

Serial interface signals: TTL level

I/Q signals: common mode voltage = 1.70 V; amplitude = 0.90 Vp-p

Dual-band VCO: 2 GHz, P_{out} = –7 dBm typical

1 GHz, P_{out} = –3 dBm typical

Auxiliary VCO: 200 MHz, 0.2 VPP maximum

TXCO: 19.44 MHz

These tests are performed at room temperature.

VCC = VCCP = VDD = VDDA = 3.75 V

The main and auxiliary synthesizer capabilities are limited by the operation of available VCOs.

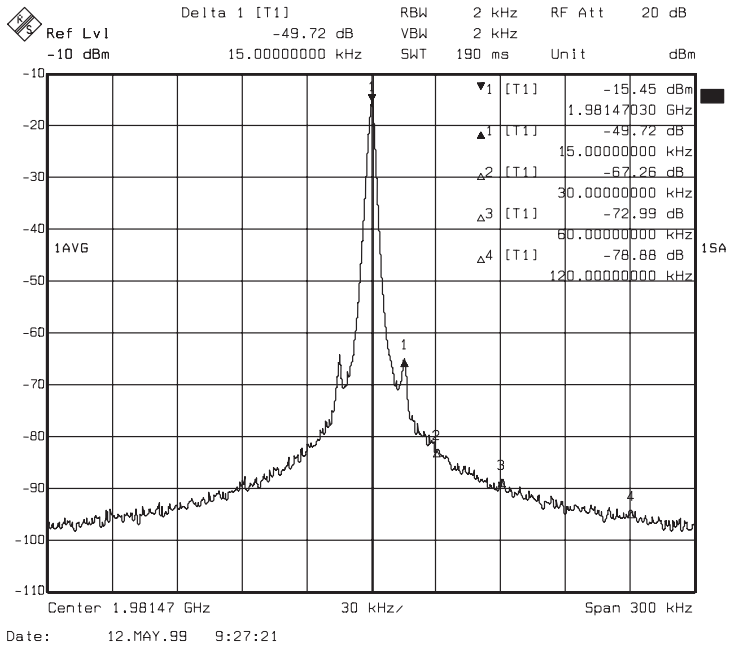
The main VCO frequency range is 1958 MHz to 2102 MHz, and the auxiliary VCO range is 100 MHz to 200 MHz. Due to the tuning range of the TRF3040 device, which is limited by the VCC, the maximum frequency is approximately 114 MHz.

4.2 Performance Graphs

Performance graphs are provided in this section with regard to:

- Main synthesizer
  - Spur suppression
  - Lock time
- Modulator measurements
  - Output level
  - Carrier and sideband suppression
  - Output driver linearity

Spur suppression for the main fractional synthesizer is shown in Figure 15 through Figure 21.



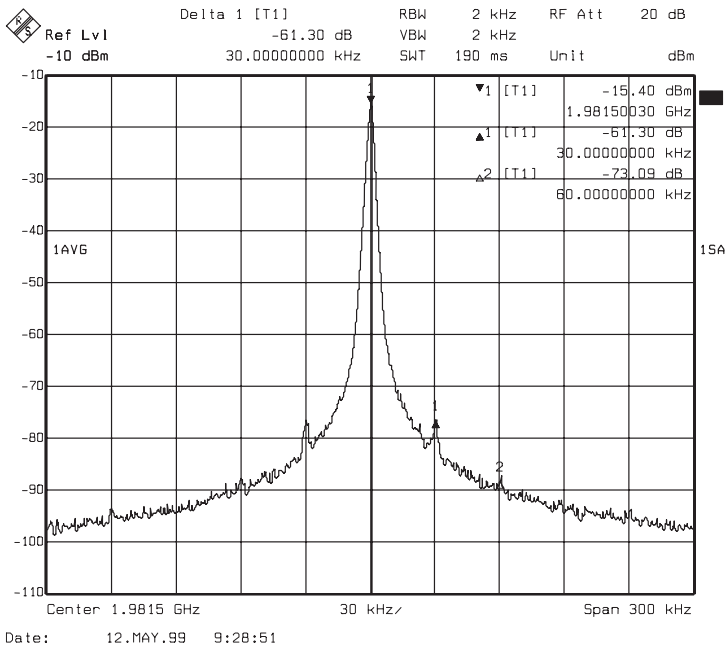
1/8 Channel

CN = 117

Freq = 1981.47 MHz

15 kHz spur = 50 dBc
30 kHz spur = 67 dBc
60 kHz spur = 73 dBc
120 kHz spur = 79 dBc

Figure 15. Spur Suppression on 1/8 Channel



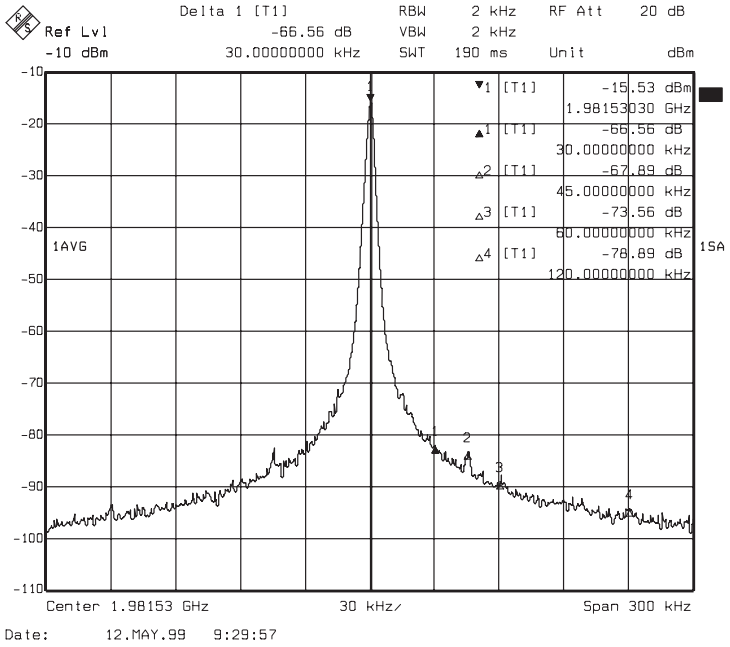
2/8 Channel

CN = 117

Freq = 1981.50 MHz

30 kHz spur = 61 dBc
60 kHz spur = 73 dBc

Figure 16. Spur Suppression on 2/8 Channel



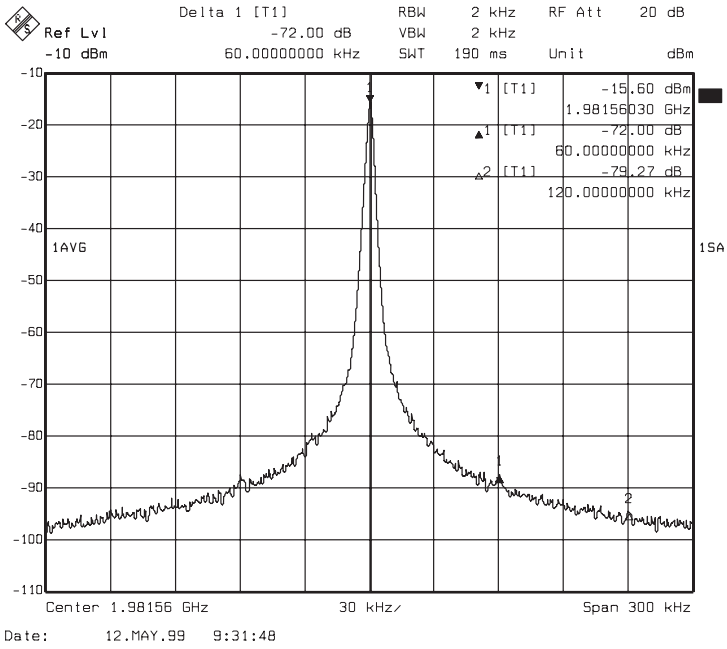
3/8 Channel

CN = 117

Freq = 1981.53 MHz

30 kHz spur = 66 dBc
45 kHz spur = 68 dBc
60 kHz spur = 73 dBc
120 kHz spur = 79 dBc

Figure 17. Spur Suppression on 3/8 Channel



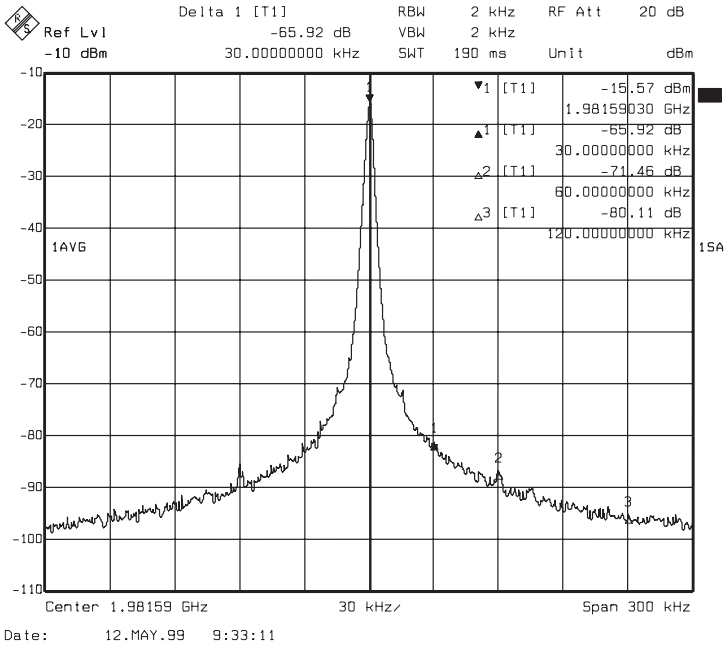
4/8 Channel

CN = 117

Freq = 1981.56 MHz

60 kHz spur = 72 dBc
120 kHz spur = 79 dBc

Figure 18. Spur Suppression on 4/8 Channel



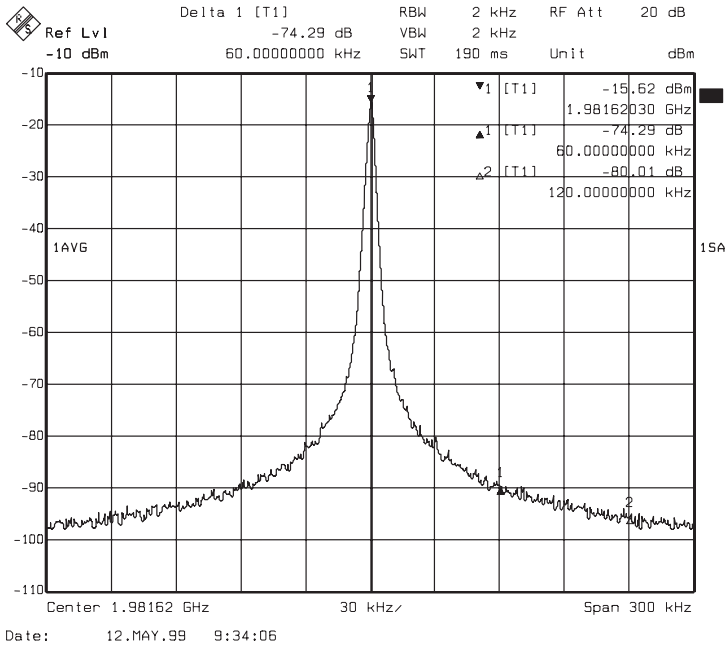
5/8 Channel

CN = 117

Freq = 1981.59 MHz

30 kHz spur = 66 dBc
60 kHz spur = 71 dBc
120 kHz spur = 80 dBc

Figure 19. Spur Suppression on 5/8 Channel



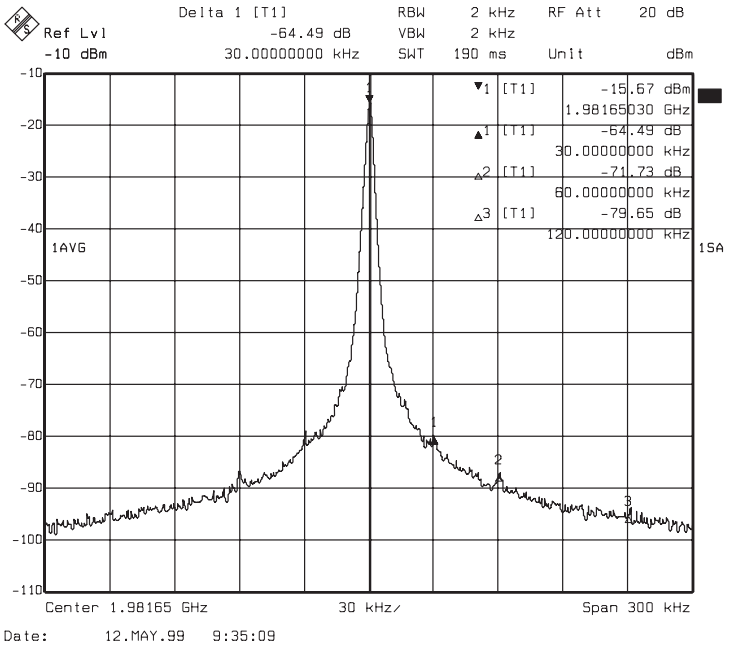
6/8 Channel

CN = 124

Freq = 1981.62 MHz

60 kHz spur = 74 dBc
120 kHz spur = 80 dBc

Figure 20. Spur Suppression on 6/8 Channel



7/8 Channel

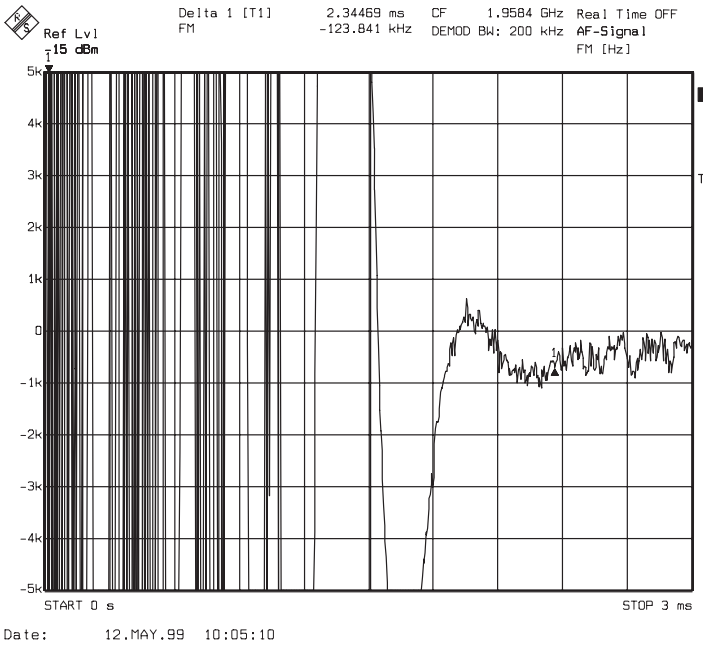
CN = 117

Freq = 1981.65 MHz

30 kHz spur = 64 dBc
60 kHz spur = 72 dBc
120 kHz spur = 80 dBc

Figure 21. Spur Suppression on 7/8 Channel

Figure 22 illustrates lock time.



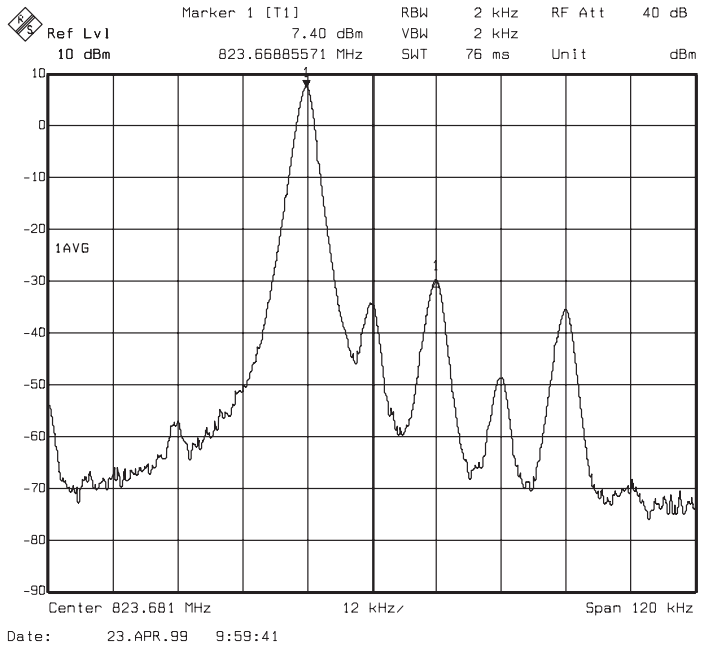
Frequency step of 142.11 MHz from 2100.51 MHz to 1981.4 MHz

K_{PD} = 288 μA/2π

Note: Faster lock times can be achieved by increasing the K_{PD} to 550 μA/2π as indicated in Section 3.1.3.1.

Figure 22. Lock Time

Figure 23 through Figure 28 illustrate modulator performance.

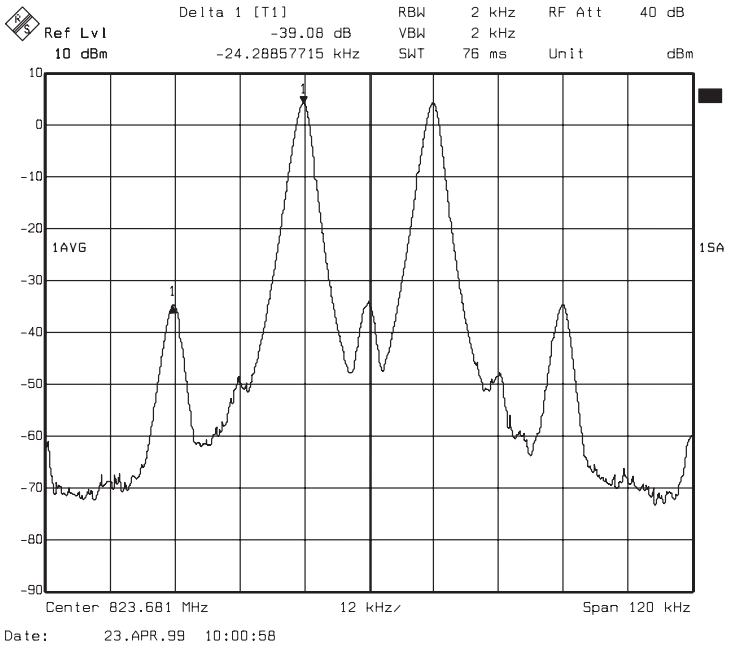


Low band

1958.40 MHz
Cable loss = 0.7 dB

P_{OUT} = 8.0 dBm@PC = 5
Carrier suppression = 43 dBc
Sideband suppression = 38 dBc

Figure 23. Low-Band Carrier/Sideband Suppression

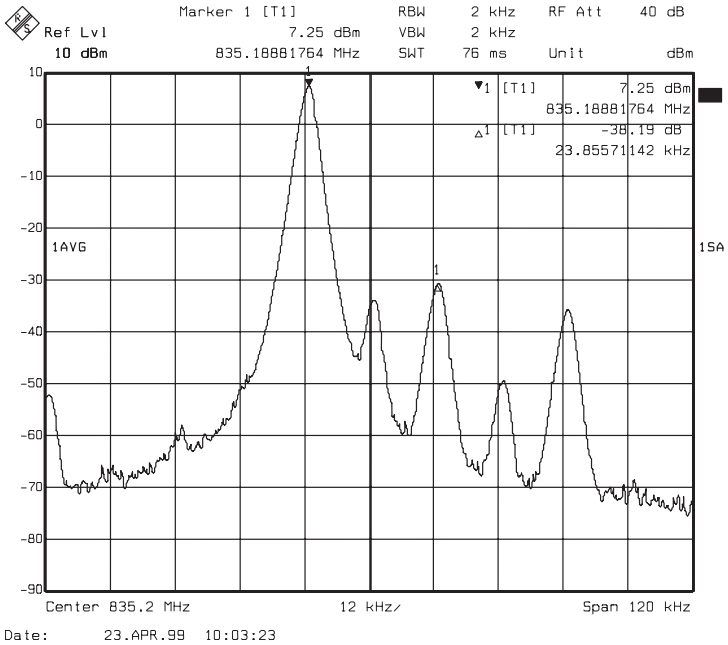


Low band

1958.40 MHz
Cable loss = 0.7 dB

Linearity = 39 dBc

Figure 24. Low-Band PA Driver Linearity

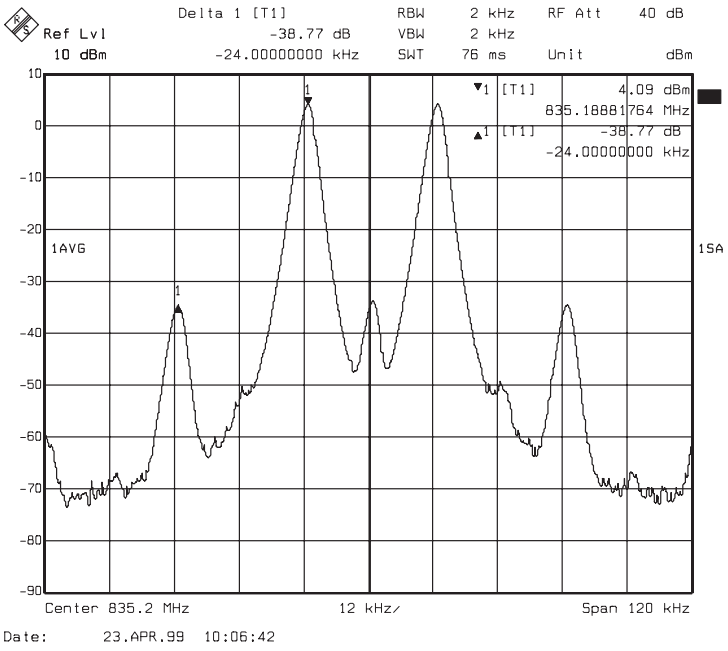


Mid band

1981.44 MHz
Cable loss = 0.7 dB

P_{OUT} = 7.95 dBm@PC = 6
Carrier suppression= 41 dBc
Sideband suppression= 39 dBc

Figure 25. Mid-Band Carrier/Sideband Suppression

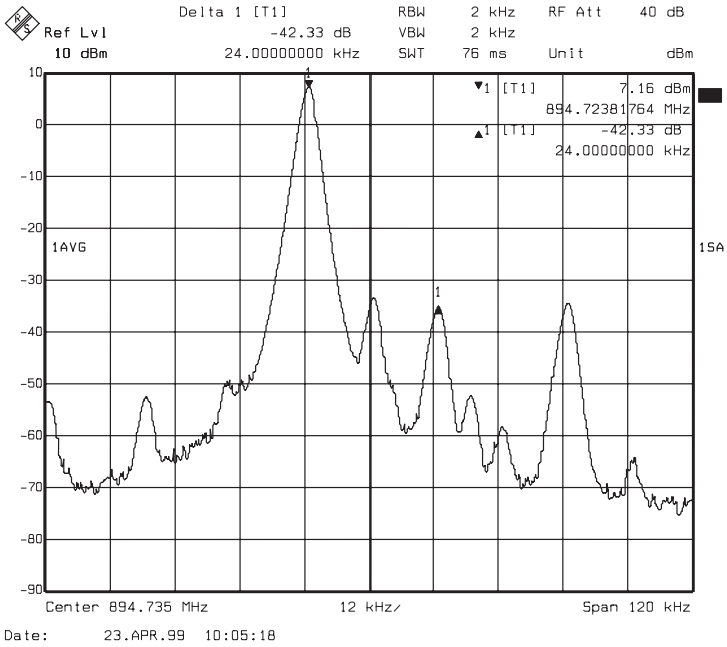


Mid band

1981.44 MHz
Cable loss = 0.7 dB

P_{OUT} = 7.95 dBm@PC = 6
Linearity = 38 dBc

Figure 26. Mid-Band PA Driver Linearity

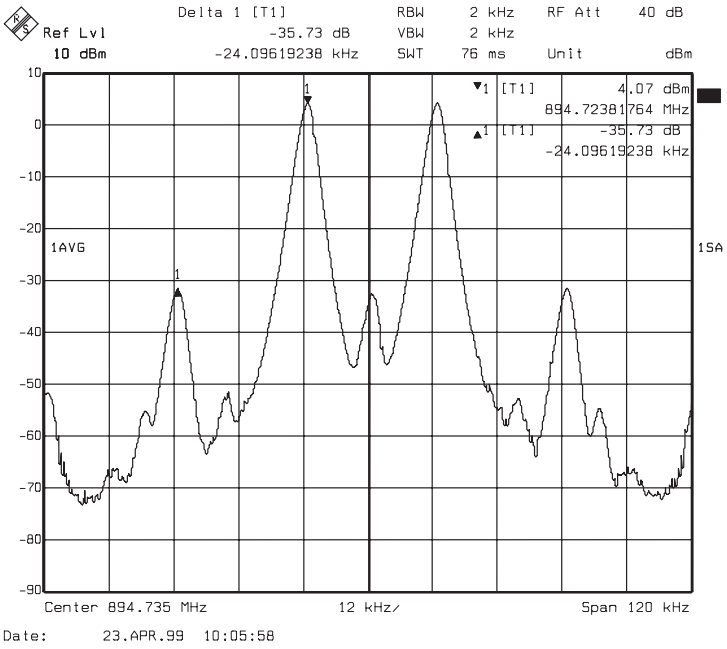


High band

2100.51 MHz
Cable loss = 0.7 dB

P_{OUT} = 7.9 dBm@PC = 4
Carrier suppression = 41 dBc
Sideband suppression = 42 dBc

Figure 27. High-Band Carrier/Sideband Suppression



High band

2100.51 MHz
Cable loss = 0.7 dB

P_{OUT} = 7.9 dBm@PC = 4
Linearity = 35.7 dBc

Figure 28. High-Band PA Driver Linearity

5 Software Driver

A DOS-based software driver is supplied with the evaluation board. The software is intended for use in an MS-DOS environment. No special memory is required to use the software. Two files are contained on the provided disk: TRF3040.EXE and INIT.CFG. Both of these files should be placed in the same directory on a fixed disk, or the program may be executed from the disk provided. To execute the program from the disk provided, type the following:

A:\TRF3040 ↵ (*Enter)*

The program executes from the TRF3040.EXE file. The INIT.CFG file is read by the program to set up the program parameters. The INIT.CFG file may be changed to suit your needs; see the F9 Save File description in Table 5.

5.1 Program Screen

The program screen is divided into five main sections:

- Main Loop

  The Main Loop section displays all of the pertinent parameters concerning the main synthesizer.
- Auxiliary Loop

  The Auxiliary Loop section displays all of the pertinent parameters concerning the auxiliary synthesizer.
- Modulator

  The Modulator section displays all of the pertinent parameters concerning the modulator.
- Device

  The Device section displays all of the pertinent parameters concerning the device enables, modes, and reference frequency.
- Editing

  The bottom two lines of the display suggest appropriate keys to use or actions to take based on the user inputs.

5.1.1 Main Loop Section

The Main Loop section displays the current main synthesizer loop parameters. All parameters displayed in the Main Loop section can be modified except for *Phase Detector Freq* and *Channel Spacing,* which are informative only. These two parameters are calculated from the reference frequency (*Reference Freq*) and reference counter (*Reference Count NR*) parameters in the Device section and the fractional modulus (*Frctnl Modulus FMOD*) parameter in the Main Loop section.

5.1.1.1 Main VCO Frequency

The *Main VCO Frequency* parameter is not actually a TRF3040 device parameter, but it may be used to cause the program to automatically find a solution, if possible, for *N* (*ENHANCED* mode only), *NM1–NM3* (*STANDARD* mode only), and *NF* based on the entered *Main VCO Frequency* parameter and others. Enter the correct reference frequency (*Reference Freq)*, reference count (*NR*), and fractional modulus (*FMOD*) parameters before you use the *Main VCO Frequency* parameter to calculate a channel solution.

5.1.1.2 Prescaler (PR)

The *PR* field selects the desired main synthesizer prescaler configuration when the device is operated in *STANDARD* mode. The choices are:

PR = 1 64/65 modulus prescaler

PR = 2 64/65/72 modulus prescaler

When the device is operated in *ENHANCED* mode, the *PR* field is not programmable, and the prescaler is configured as a 32/33 modulus prescaler.

5.1.1.3 Fractional Numerator (Frctnl Numerator NF)

The *NF* field selects the numerator value for the fractional accumulator circuit of the main synthesizer. This value can be manually programmed to any valid desired value. NF is also automatically updated when the *Main VCO Frequency* field is used to enter the desired main synthesizer channel frequency or when the *FMOD* field is changed.

5.1.1.4 Fractional Modulus (Frctnl Modulus FMOD)

The *FMOD* field selects the desired main synthesizer fractional accumulator denominator modulo value. The valid choices based on the operation mode of the TRF3040 device are as follows:

FMOD = 0	Modulo–5	*STANDARD* mode
FMOD = 1	Modulo–8	*STANDARD* mode
FMOD = 1–16	Modulo–1–16	*ENHANCED* mode

When the *FMOD* field is changed, the routine to calculate the proper main synthesizer channel coefficients is called.

5.1.1.5 Main Charge Pump Current (Main Chrgpmp I CN)

The *CN* field selects the main synthesizer charge pump current gain coefficient.

5.1.1.6 Reference Select RSM (Main Ref Select RSM)

The *RSM* field selects the main synthesizer reference postscaler select as follows:

RSM = 0	Reference ÷ 1
RSM = 1	Reference ÷ 2
RSM = 2	Reference ÷ 4
RSM = 3	Reference ÷ 8

5.1.1.7 NM1-3 (STANDARD Mode)

The *NM1-3* fields can be programmed manually to any valid number. These fields are also automatically updated when the *Main VCO Frequency* field is used to enter the desired main synthesizer channel frequency or when the *FMOD* field is changed.

5.1.1.8 N (ENHANCED Mode)

The *N* field can be programmed manually to any valid number. This field is also automatically updated when the *Main VCO Frequency* field is used to enter the desired main synthesizer channel frequency or when the *FMOD* field is changed.

5.1.1.9 Proportional Charge Pump Current (Prprtnl Chrgpmp I CL)

The *CL* field selects the main synthesizer speed-up mode, proportional charge pump current gain coefficient.

5.1.1.10 Integral Charge Pump Current (Intgrl Chrgpmp I CK)

The *CK* field selects the main synthesizer speed-up mode, integral charge pump current gain coefficient.

5.1.1.11 Charge Pump Polarity (CHRGPMP PLRTY MCP) (ENHANCED Mode)

The *MCP* field selects the main synthesizer charge pump current polarity in *ENHANCED* mode as follows:

MCP = 0 Positive polarity

MCP = 1 Negative polarity

5.1.1.12 Strobe Pulse Width (Strobe PWth) (STANDARD Mode)

The *Strobe PWth* field may be used to vary the pulse width of the serial interface STROBE signal. This feature is used to regulate speed-up mode when the device is operating in *STANDARD* mode. A value of approximately 7500–9500 for the strobe pulse width provides for a 600-μs STROBE pulse width, which varies according to the microprocessor speed of the PC executing the program.

5.1.1.13 Speed-up Time G (ENHANCED Mode)

The *G* field selects the duration of speed-up mode when the device is in *ENHANCED* mode. The duration of speed-up mode is determined as follows:

$$\text{Duration} = \frac{G \times 16}{\text{Reference frequency}} \tag{34}$$

where reference frequency is typically 240 kHZ.

5.1.2 Auxiliary Loop Section

The Auxiliary Loop section displays the current auxiliary loop parameters. All parameters displayed in the Auxiliary Loop section can be modified except *Phase Detector Freq*. This parameter is calculated from the reference frequency (*Reference Freq*) and reference counter (*Reference Count NR*) parameters in the Device section.

5.1.2.1 Auxiliary VCO Frequency

The *Aux*iliary *VCO Frequency* parameter is not actually a TRF3040 device parameter, but it may be used to cause the program to automatically find a solution, if possible, for *NA* based on the entered *Aux VCO Frequency* parameter and others. Enter the correct reference frequency (*Reference Freq)* and reference count (*NR*) before you use the *Aux VCO Frequency* parameter to calculate a channel solution.

5.1.2.2 Reference Select (Aux Ref Select RSA)

The *RSA* field selects the reference postscaler for the auxiliary synthesizer as follows:

RSA = 0	Reference ÷ 1
RSA = 1	Reference ÷ 2
RSA = 2	Reference ÷ 4
RSA = 3	Reference ÷ 8

5.1.2.3 Auxiliary Divider Ratio (Count NA)

The *NA* field selects the auxiliary synthesizer divider ratio. It consists of a 13-bit NA field counter. The total NA division is 0 to 8191.

5.1.2.4 Charge Pump Polarity (Chrgpmp Plrty ACP) (ENHANCED Mode)

The *ACP* field selects the auxiliary synthesizer charge pump current polarity when the device is in *ENHANCED* mode as follows:

ACP = 0	Positive polarity
ACP = 1	Negative polarity

5.1.3 Modulator Section

The Modulator section displays the current modulator parameters. You can modify all parameters displayed in the Modulator section except *Transmit Mode (TM).*

5.1.3.1 VGA Power Control (Pwr Control PC)

The *PC* field selects the variable gain amplifier setting. The maximum power is set to 0, and the minimum power is set to 127.

5.1.3.2 Transmit Mode (TM)

This parameter is not available with the TRF3040 device and should be set to 0.

5.1.3.3 Sleep Mode (SM)

The *SM* field enables/disables the synthesizer section and the modulator section as follows:

SM = 0	Disable sleep mode.
SM = 1	Enable sleep mode.

5.1.3.4 Digital/Analog Mode (Dig/Ana MODE)

The *MODE* field defines the modulator operating modes.

MODE = 0	Analog (AMPS)
MODE = 1	Digital (DAMPS)

5.1.3.5 TXIF Divide-by-Divider (Offset VCO/N)

The *N* field selects the divider ratio of the transmit intermediate frequency (TXIF) synthesizer. This parameter is defined as the following:

N = 0	Divide-by-6
N = 1	Divide-by-7
N = 2	Divide-by-8
N = 3	Divide-by-9

5.1.3.6 TXIF Synthesizer Enable (Synth Enbl SE)

The *SE* field enables/disables the TXIF synthesizer as follows:

SE = 0	Disable TXIF synthesizer.
SE = 1	Enable TXIF synthesizer.

5.1.3.7 Transmit Enable (Transmit Enbl TE)

The *TE* field enables/disables the modulator output as follows:

TE = 0	Modulator output is OFF.
TE = 1	Modulator output is ON.

This parameter defines the TXEN signal. It is a static control switch rather than a data bit. It does not require sending data action to activate its functionality.

5.1.4 Device Section

The Device section displays the current device parameters. You can modify all parameters displayed in the Device section except *Synthesizer Status,* which is a read-back from the *LOCK* terminal on the TRF3040 device.

5.1.4.1 Main Divider Enable (EM)

The *EM* field enables/disables the main synthesizer as follows:

EM = 0	Disable main synthesizer.
EM = 1	Enable main synthesizer.

5.1.4.2 Auxiliary Divider Enable (EA)

The *EA* field enables/disables the auxiliary synthesizer as follows:

EA = 0	Disable auxiliary synthesizer.
EA = 1	Enable auxiliary synthesizer.

5.1.4.3 Device Mode ALT

The *Device Mode* parameter selects the fundamental operating mode of the TRF3040 device. Additional features are available in the *Enhanced Performance Mode (ENHANCED*). Note the changes in the Main Loop section when you change device modes.

ALT = 0	*STANDARD* mode
ALT = 1	*ENHANCED* mode

5.1.4.4 Device Test T

The *Device Test T* field is reserved for TI internal use and should remain set to zero. When this field is set to zero, the LOCK terminal operates normally. Otherwise, the *LOCK* terminal is connected to internal nodes in the TRF3040 device.

5.1.4.5 Reference Frequency (Reference Freq)

Enter the external reference frequency used with the evaluation board in this field so that other parameters, such as the phase detector reference frequency and channel spacing, can be properly calculated and displayed.

5.1.4.6 Reference Count NR

The *NR* field selects the division ratio of the reference frequency counter.

5.1.4.7 A-Word Mode Long

The *Long* field selects between two A-word bit-length programming schemes as follows:

Long = 0	A-word = 24 bits
Long = 1	A-word = 32 bits; not available with the TRF3040

5.1.4.8 Synthesizer Status

Synthesizer Status is a read-back only field that reflects the current status of the LOCK terminal.

5.1.5 Editing Section

To edit any one of the program parameters displayed, first select an appropriate function key (see Table 5) to select a section. Use the arrow *(←, ↑, →, ↓)* and tabulation (*Tab*) keys to move the cursor to the parameter to be edited. When the cursor is located properly, press *Enter* (or *Return*) to select the parameter. Next, enter the new value and press *Enter* again. When all of the parameters within a particular section of the display have been edited, press *Esc* to return to the main menu.

For example, to edit the *Strobe PWth* parameter in the Main Phase-Locked Loop #1 section from the main menu in *STANDARD* mode, perform the following keystrokes:

F1	Select the Main Loop section.
→	Move to the right column.
↓	Move down the right column
↓	Move down the right column.
↓	Move down the right column.
↓	Move down the right column.
↓	Move down the right column.
Enter	Select the *Strobe Pwth* field.
Data	Enter the desired data, such as 9500.
Enter	Complete the field edit.
Esc	Exit the Main Loop section and return to the main menu.
u	Increments CN by 1.
j	Decrements CN by 1.
U	Increments CN by 5.
J	Decrements CN by 5.

5.1.5.1 Function Keys

Use the function keys in Table 5 to select sections of the display for editing or to perform a program function.

Table 5. Function Keys

Function Key	Definition	Description
F1	Edit phase-locked loop 1	Selects the Main Loop section of the display for editing
F2	Edit phase-locked loop 2	Selects the Auxiliary Loop section of the display for editing
F3	Edit modulator	Selects the Modulator section of the display for editing
F4	Edit device	Selects the Device section of the display for editing
F5	View bit map	Views the current multiword bitmap
F7	Select port	Selects the PC parallel port. This function looks at the ROM BIOS to find all parallel ports. Follow the directions to select a particular port if more than one is found.
F8	Load file	Loads a configuration file to reset the program parameters to a user-specified condition. This function looks for the entered file on the same disk and in the same directory from which the program is executing. Any existing, allowable DOS name can be used. You can also load the INIT.CFG file using this function to restore the original program configuration.
F9	Save file	Saves a configuration file containing the current program parameters to a user-specified file. This function writes the program parameters to the specified file name on the same disk and in the same directory from which the program is executing. Any allowable DOS name can be used. You can rewrite the INIT.CFG file using this function to change the boot program configuration.
F10	Send to device	Programs the TRF3040 device. When F10 is selected, the current bitmap is displayed, and you can enter the letter (A, B, C, D, G, E) of the word to be sent to the TRF3040 device. You can send the default sequence of G, D, C, B, and A (in this order) to the TRF3040 device by pressing *Enter* without first selecting a letter.
Ctrl–Q	Quit	Press the *Control* (*Ctrl*) key and hold while pressing the *Q* key to exit the program and return to the DOS prompt.

5.2 Special Notes

The *FMOD* field in the Main Loop section of the screen must be modified when you change between *STANDARD* and *ENHANCED* modes. You should also re-enter the desired main VCO frequency in the Main Phase-Locked Loop section after switching between *STANDARD* and *ENHANCED* modes, and after correctly setting the *FMOD* field to ensure that the *NM1-NM3 (STANDARD)* and *N (ENHANCED)* parameter calculations are current.

References

1. Best, Roland E., *Phase-Locked Loops—Design, Simulation, & Applications*, 3rd edition, McGraw-Hill, New York, 1997.
2. Djen, Wing S., *Philips Semiconductors: AN1890, Using the SA7025 and SA8025A for Narrow Band Systems*, August 1997.
3. Brennan, P. V., *Phase-Locked Loops: Principles and Practice*, 1st edition, McGraw-Hill, New York, 1996.
4. Rohde, Ulrich L., *Microwave and Wireless Synthesizers—Theory and Design*, 1st edition, John Wiley & Sons, Inc., New York, 1997.