TEXAS INSTRUMENTS

Application Report

1998

MicroStar BGA

TEXAS INSTRUMENTS

Printed in U.S.A
11/98

SZZA005

MicroStar BGA™ *Semiconductor Group Package Outline Application Report*

Kevin Lyne and Charles Williams
Prepared by: Tanvir Raquib

SZZA005
November 1998

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Contents

List of Figures

List of Tables

MicroStar BGA

ABSTRACT

1 Introduction

During 1996/1997 there was a great deal of interest in the chip scale package (CSP). Most CSPs are offered in the form of a BGA. Texas Instruments has developed such a package, which is called MicroStar BGA™ (µStar BGA™).

This package is ideally suited to low-cost, high-volume applications, where package size is of major importance. Such applications include:

- Mobile telephone handset
- High density disk drive
- Camcorder
- Other space and/or weight sensitive products

Use of CSPs in BGA format have multiple advantages over, for example, fine pitch QFP packages.

- CSPs are usually smaller.
- CSPs have larger pitch.
- CSPs have no fragile leads, causing yield and rework problems.
- Surface mount yields are significantly improved.
- Board inspection can be reduced.
- CSPs have better thermal and electrical properties.
- CSPs can easily be supplied in tape and reel format.

This document:

- Provides guidelines for surface mounting
- Shows the reliability of the package, and in particular, the temperature cycle performance
- Provides thermal and electrical data
- Covers MicroStar BGA packages with 0.80 mm ball pitch. However, the principles (for example, board design guidelines) can also be applied to MicroStar BGAs with other pitches.

With this information, the user should quickly be able to assess the suitability of MicroStar BGA for the intended application and be able to start the necessary development required to put the package into production.

The experience of Texas Instruments is that some process development and board design study is necessary before CSPs can be used effectively. This is however a relatively low-cost development, and usually does not involve the purchase of any new surface-mounting equipment. Thus, in size sensitive applications, the benefits of using a CSP in place of a QFP will normally be seen very clearly.

2 Reliability

CSPs have many advantages over QFPs. However, in one area, CSPs have certain limitations. This is the area of reliability of the solder joints used to connect the package to the board on which the package is mounted.

These small solder joints are subject to solder joint fatigue during temperature cycling. This is due to the difference in the coefficient of thermal expansion (CTE) between the package and the board. Since, by definition, a major component of the package is the silicon chip, the CTE of the package is effected by the silicon. The CTE of a typical FR4 board is dominated by the CTEs of epoxy resin, glass fibre, and copper. Below are typical CTE values at room temperature. This clearly demonstrates that the CTEs are very different, and that consequently there will be stress concentrated on the connections (solder balls) between the package and board.

Table 1. Coefficient of Expansions of Typical Materials Used

MATERIAL	CTE AT 25°C (PPM/°C)
Silicon	3
FR4	16–18

To control this solder joint fatigue mechanism and maintain it within acceptable limits, it is important to design PCBs and surface mount processes that minimize this effect. See Sections 3 and 4.

If the optimum conditions described in this application report are used, then 0.80 pitch MicroStar BGA components can withstand up to 1000 cycles of –40/125°C temperature cycling without failure when mounted on an FR4 PCB. Some tests have already demonstrated zero joint failures over 1000 cycles of –40/125°C.

Texas Instruments continues to improve the board-mounted reliability of MicroStar BGA. More details of reliability test results are available upon request. Before being released to production, each MicroStar BGA device/package combination is subjected to rigorous qualification testing. These tests include preconditioning the package according to J-STD-20 guidelines to determine the moisture sensitivity of the device being qualified. Other tests include Autoclave, temperature cycling, thermal shock, 150°C storage life, and 85/85 bias/humidity testing. Table 2 gives typical data.

Table 2. Package-Level Reliability Testing

TEST ENVIRONMENTS	CONDITIONS	READ POINTS
HAST	85%RH/85°C	600 hrs. 1000 hrs
Autoclave	121°C, 15 psig	96 hrs 240 hrs
Temperature cycle	–55°C/125°C –65°C/150°C	500 cycles 750 cycles 1000 cycles
Thermal shock	–65°C/150°C	200 cycles 500 cycles 750 cycles 1000 cycles
HTOL	125°C, Op. voltage	500 hrs 600 hrs 1000 hrs
HTOL†	140°C, Op. voltage 155°C, Op. voltage	500 hrs 240 hrs
Bake†	150°C 170°C	600 hrs 1000 hrs 420 hrs
HAST†	130°C	96 hrs

† Optimal tests. One or more of them may be added to meet customer requirements.

All samples used in these tests are preconditioned according to Joint Electronic Device Committee (JEDEC) A113 at various levels.

Table 3. Package-Level Reliability Testing Results

PACKAGE TYPES							
LEADS: BODY; DEVICE; DIE (mm):		**64 8×8 mm MSP 5.3×5.8**	**80 10×10 mm ASP 7.5×7.5**	**100 11×11 mm ASP 7.5×7.5**		**144 12×12 mm DSP 9.3×9.3**	
Test Environments (Sample Size/Failures)	**LEVEL:**	**4**	**2**	**2**	**3**	**2a**	**4**
Autoclave (240 hrs)		70/0	78/0	78/0	78/0	77/0	77/0
Temp cycle –55°C/125°C	(1000 cycles)	116/0	78/0	78/0	78/0	77/0	77/0
Temp cycle –65°C/150°C	(500 cycles) (750 cycles) (1000 cycles)	116/0	78/0	78/0	78/0	77/0	77/0
HAST, 85/85	(1000 hrs) (1250 hrs)	115/0			77/0	77/0	
150°C storage	(600 hrs) (1000 hrs)	43/0	78/0	78/0	78/0		77/0
HTOL	(1000 hrs)	116/0	0		129/0		

Table 4. Board-Level Reliability Summary

CONDITIONS (with solder paste)						REQUIREMENTS				EXTENDED RANGE		
PACKAGE	TI MFG SITE TEST SITE	BODY (mm)	PITCH (mm)	DIE (mm)	TEMP CY (°C)	500 CYC	800	1000	1100	1200	1300	1500
GGU 144 balls	TI HIJI TI HIJI	12 × 12	0.8	8.8 × 8.8	–40/125	0/85	0/85	0/85	4/85	5/77	5/72	15/39
GGU 144 balls	TI Philippines TI HIJI	12 × 12	0.8	8.8 × 8.8	–40/125	0/36	0/36	0/36	0/36	0/36	0/36	1/35
GGF 100 balls	TI HIJI TI HIJI	10 × 10	0.5	6.6 × 6.6	–25/125	0/32	0/32	0/32	0/32	0/32	0/16	6/16
GHC 196 balls	TI TIPI TI HIJI	15 × 15	1.0	8.8 × 8.8	–40/125	0/62	0/62	0/62	0/62	0/62	0/62	4/62
GGU 144 balls	TI Philippines Customer A	12 × 12	0.8	8.8 × 8.8	–40/100	0/180	0/180	0/180	0/180	–	–	–
GGW 176 balls	TI HIJI Customer B	15 × 15	0.8	6.6 × 6.6	–25/125	0/35	0/35	0/35	0/35	0/35	0/35	1/35
GGM 80 balls	TI HIJI Customer C	10 × 10	0.8	5.0 × 5.0	–40/125	0/12	0/12	0/12	–	–	–	0/10

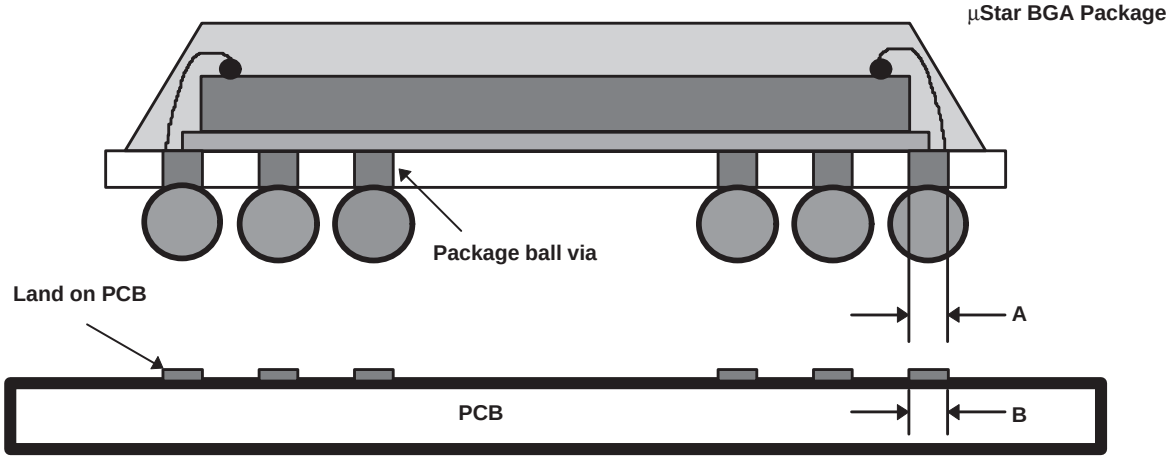
Table 5. Summary of Significant Improvements

CONDITION	IMPROVED BLR	
Die size	Larger	Smaller
Die edge	Over balls	Within ball matrix
Ball count	Smaller	Larger
Ball size	Smaller	Larger
PCB pad size	Over/Undersized	Matches package via
	(for NSMD ~ 90% of via)	
Solder paste	None or insufficient	Thickness 0.15 nom.
	(type matches reflow)	

3 Board Design

3.1 Land Size

Design of both the BGA itself and the PCB on which the BGA is mounted is critical in achieving good manufacturability and optimum reliability. In particular, the diameter of package vias and board lands are key. The actual sizes of these dimensions are of course important, but their ratio is also of critical importance. See Figure 1.



A = Land diameter on package
B = Land diameter on PCB
Ratio A/B should equal 1.0 for optimum reliability

Figure 1. Board Land Design Guidelines

Optimum land diameters are as follows:

Solder mask defined. This is where the copper pad is made larger than the desired land area, and the opening size is defined by the opening in the solder mask material. The advantages normally associated with this technique are that the size is more closely controlled and that copper adhesion to the laminate is promoted. The size control is the result of the stencils for masks being photo imaged. The chief disadvantage of this method is that the larger copper spot can make routing more difficult.

Non-solder mask defined. Here, the land area is etched inside the solder mask area. While the size control is dependent on copper etching and is not as accurate as the solder mask method, the overall pattern registration is dependent on the copper artwork, which is quite accurate. The tradeoff is between accurate dot placement and accurate dot size. The potential advantage in routability with this method was discussed previously.

Solder Mask Defined Land

Pitch	A Diameter	B Diameter
0.5 mm	0.25 mm	0.35 mm
0.8 mm	0.38 mm	0.48 mm
1.0 mm	0.45 mm	0.55 mm

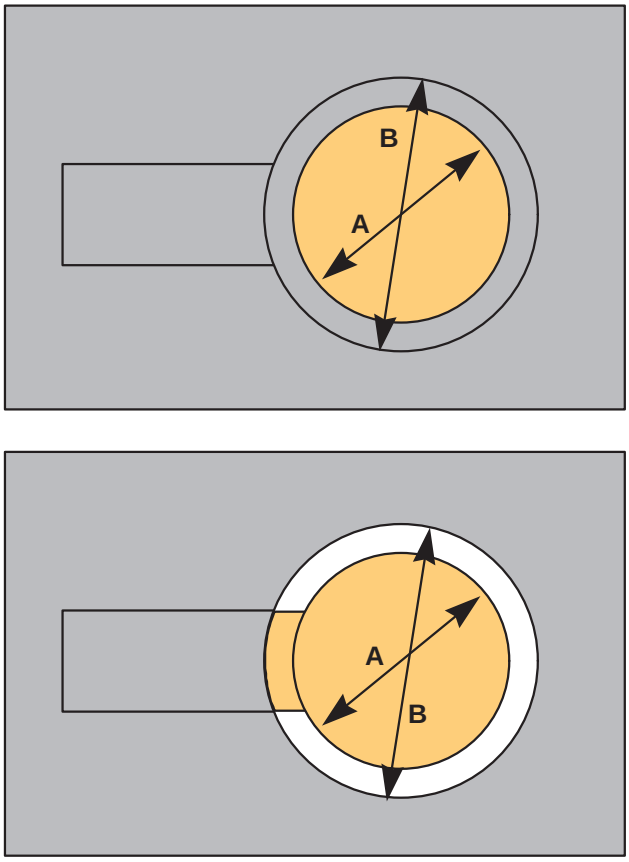
Non-Solder Mask Defined Land

Pitch	A Diameter	B Diameter
0.5 mm	0.22 mm	0.37 mm
0.8 mm	0.35 mm	0.50 mm
1.0 mm	0.4 mm	0.55 mm

In practice optimum land diameters are as follows:

Solder mask defined pads: 0.375 mm
Non-solder mask defined pads: 0.350 mm

See Figure 2 for more detail.



- **Solder mask defined land**

  A: 0.375 mm

  B: 0.475 mm

- **Non-solder mask defined land**

  A: 0.350 mm

  B: 0.500 mm

Figure 2. Typical Land and Solder Mask Geometry 0.8 mm Pitch MicroStar BGA

Experience has shown that solder lands can be either solder mask defined, or non-solder mask defined. However, non-solder mask defined designs ease routing limitations, and are thus the favored option.

The MicroStar BGA packages are fine pitch, with ball spacing ranging from 1 mm to 0.5 mm. This may present the board designer with layout challenges, especially in high-density boards. Because conventional BGA packages require space for both the package and the vias around the chip periphery, circuit board layout based on 8-mil conductor lines and 8-mil spaces will not fit between the balls of a MicroStar BGA of 0.8 mm pitch or less, which have a pitch of roughly 15 mils between ball pads. PCB capabilities are now routinely in the 4-mil conductor/4- to 5-mil spacing range, and this at least allows one signal to be routed between ball pads. The 15-mil ball spacing is worst case and is calculated by assuming the diameter of the solder ball land is 16 mils (0.41 mm).

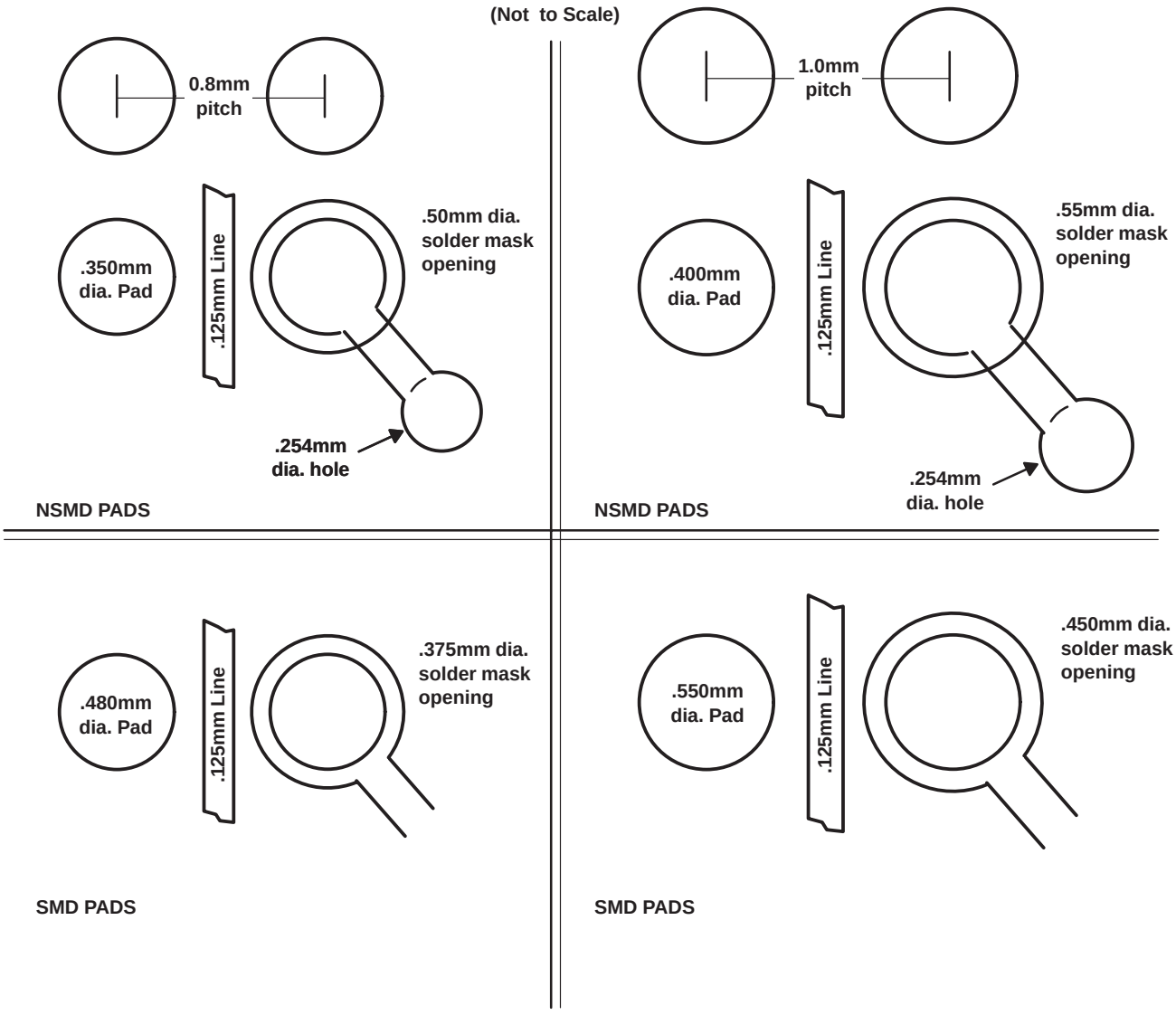


Figure 3. Solder Masked Versus Non-Solder Masked Defined Pads

3.2 High Density Techniques

Designing boards with BGA packages is not a difficult task. Designing high-density boards that maximize board space can be tricky. A common problem when designing with BGA packages is the total area required for the package and via density around the chip periphery. The total space for mounting a BGA can approach the area needed for a TQFP (Thin-Quad-Flat-Pack). Why go through the pain of changing packages if there are no space-saving benefits? Actually, companies that have migrated to BGAs, find that BGAs are not the hassle once thought. By using a few high-density techniques, the PCB designer can find that BGA's offer an opportunity for high-density boards with the design and manufacturing ease of a TQFP.

3.3 MicroStar BGA Packages

MicroStar BGA packages are all considered fine-pitch. This application report will focus on the GGU (144 pins) and GGW (176 pins) packages. Both packages have 0.8 mm pitch, but each is distinctly different in array style. The GGW ball array has wide channels in the four corners providing the inner balls with space for routing and VCC connectivity. See Appendix A for mechanical drawings of the MicroStar BGA packages.

3.4 Conductor Width/Spacing

As a general default, many of today's circuit board layouts are based on at most an 8-mil conductor (line) width and 8-mil spacing. To route between the balls and give the MicroStar BGA pin pitch roughly 15 mils between ball pads, it is impossible to satisfy both line width and spacing requirements. PCB manufacturers can now reduce the line width to 4 mils with 4- to 5-mil spacing. This at least allows one signal to be routed between ball pads. The 15-mil ball spacing is worst case and calculated by assuming the diameter of the solder ball land is 16 mils (0.41 mm).

3.5 Via Density

Via density, as mentioned earlier, can be a limiting factor when designing high-density boards. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the routability of the board by requiring less board space and increasing via density. The invention of the microvia, shown in Figure 4, has solved many of the problems associated with via density.

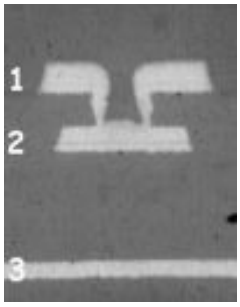


Figure 4. Laser-Drilled 4-Mil Microvia

Microvias are often created using a laser to penetrate the first few layers of dielectric. The laser can penetrate a 4-mil thick dielectric layer creating a 4-mil microvia (Figure 4). The layout designer can now route to the first internal board layer. Two layers (each 4 mils thick) can be laser-drilled creating an 8-mil microvia diameter. In this case, routing to the first two internal layers is possible.

3.6 Optimal Layers

The number of board layers increases as board chip density and functional pin count increases. As an example, the TMS320VC549GGU digital signal processor (DSP) is in a 144-pin GGU package and uses 32 pins for power and ground. Routing of roughly 112 signals can be accomplished on 3 layers. The power and ground planes increase the board to 5 layers. The sixth layer can be used on the bottom-side to place discrete components. Furthermore, by increasing the board layer stack-up to 8 layers, high-density applications are possible with only 10 to 15 mils between the chips.

Mounting two TMS320VC549 DSPs on directly opposite sides of the board is estimated to take 14 layers, assuming the sharing of V_{CC} and ground planes. Double-sided boards will have double the functionality if a DSP is on each side. Unfortunately, the placement of bypass capacitors on power pins is required and can slightly reduce the board's overall chip density. See paragraph 3.10, Placing Discrete Components, for information on placement of bypass capacitors.

3.7 Designing Vertically

The relatively large via density on the chip periphery, mentioned earlier, is caused by limited options when routing the signal from the ball. To reduce or eliminate the via density problem on the periphery of the chip, design the PCB vertically from the BGA pad through the internal layers of the board as in Figure 5. Mechanical drilling of 10-mil vias between the pads on the board and working vertically creates a pick-and-choose method–pick your layer and choose your route. A dog bone method connects the thru-hole via and the pad.

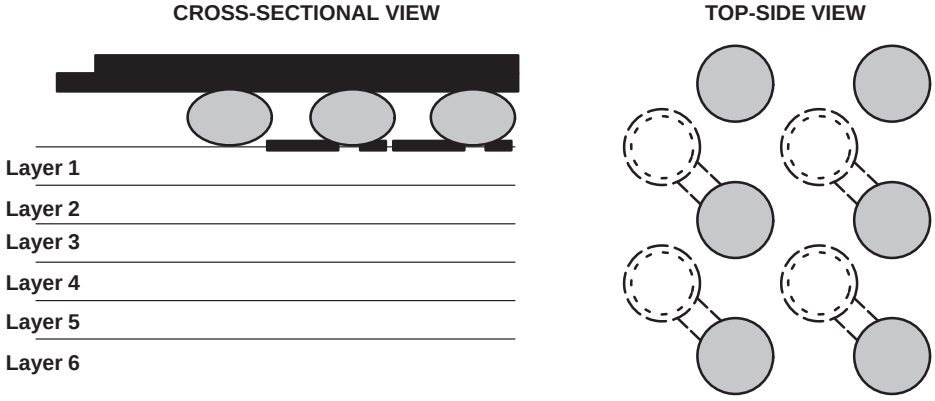


Figure 5. Dog Bone Connecting Thru-Hold Via

This time-consuming method requires a very small mechanical drill to create the 144 or 176 vias for 1 package. Although this method is the least expensive, a disadvantage is that the vias go through the board creating a matrix of vias on the bottom side of the board. Ideally, the bottom layer is used to place the bypass capacitors close to the power pins. Another disadvantage is the clearance of these vias, which can reduce, and in some case eliminate, the copper between the pads. The area of copper between the pads is critical for the connection between power plane and power pins that are not located on the outside row of the grid array. Furthermore, the thru-hole via is bare copper, which can exacerbate problems with solder ball collapse.

3.8 Burying the Dog Bone

The other option, which is the purpose of this application report, is to use a combination of blind and buried vias. Blind vias connect either the top or bottom side of the board to inner layers. Buried vias usually connect only the inner layers. Figure 6 illustrates this method using 4-mil laser-drilled microvias in the center of the pads and burying the dog bone on layer 2. This technique minimizes the probability of complications from solder ball collapse.

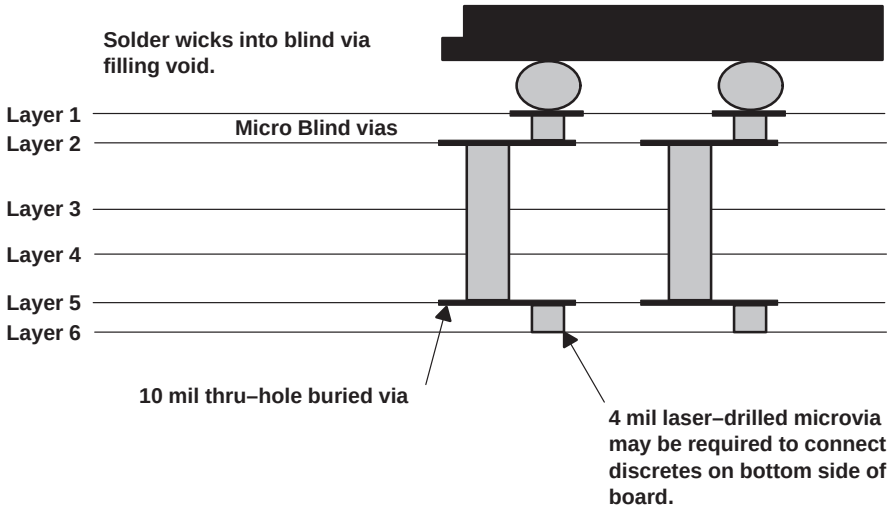


Figure 6. Burying the Dog Bone on Layer 2

Furthermore, since the buried via does not extend through the underside of the board, the designer can use another set of laser-drilled blind microvias (if needed) to connect the bypass capacitors and other discrete components to the bottom-side. The buried via is a 10-mil (can reduce to 8-mil) mechanical drilled hole with 9-mil annular ring. This corresponds to a 10+9+9= 28 mil area diameter.

It is recommended designers use non-solder masked defined (NSMD) solder lands where the balls adhere to the PCB. The diameter of the solder land can range from 14 to18 mils. A solder land of 16 mils was chosen for the referenced board in this application report.

3.9 Power Plane Considerations

Ideally power pins should be connected to as much uniform copper on the plane as possible. However, because mechanically drilled vias (i.e., buried and thru-hole) are much larger than microvias, copper width and spacing requirements can become marginal. Consequently, there is no guarantee that solder lands dedicated to the device's power pins will connect to the power plane. Power pins most effected by this problem are the internal balls (pins not on the outer row) that are adjacent to pins with buried vias. Figure 7 shows the clean (V_{CC}=2.5 V) and dirty (V_{DD}=3.3 V) power pins of the TMS320VC549GGU and their location relative to signal and ground pins.

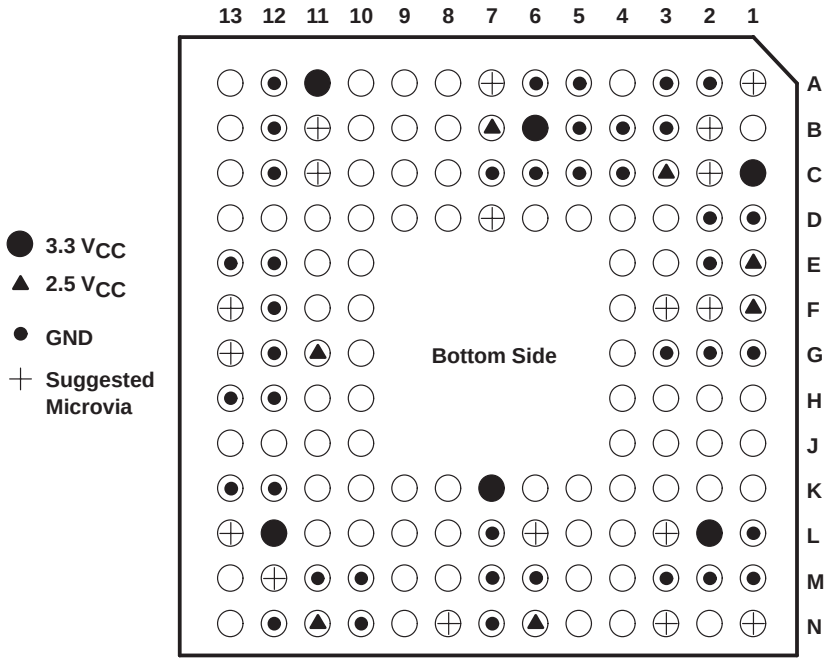


Figure 7. Clean Power, Dirty Power and Ground Pin-Out

Carefully selecting the pins that are routed on layers one and two can dramatically increase the routability of power pins. Using laser-drilled microvias, route signals that are adjacent to power pins and the signals that lead to the periphery of the chip on layers one and two. These signals do not require buried vias, creating a wider copper channel between the balls on the power planes. As an example, Figure 7 shows specific balls (balls with black dots) that should be considered for microvia routing on layers one or two.

Layer stack-up can also help power plane routability. Power planes that reside on the first (4-mil microvias) or first two (8-mil microvias) layers can be routed easier since the buried vias start on the next layer. The same design rule applies to the bottom-side of the board.

3.10 Placing Discrete Components

With the advent of buried capacitance and buried resistance, future discrete components, like bypass capacitors and pull-up resistors, will not require physical surface space. Until then, board layout and component density will be limited by certain physical form factors. The board x-ray in Figure 8, oriented from bottom side looking towards the top layer, shows a TMS320VC549GGU (144-pin BGA) package mounted on top. The bypass capacitors are mounted directly underneath the package on the underside of the board. Depending on the required capacitive loading, all the bypass capacitors may fit within the physical form factor of the GGU package (12 mm x 12 mm). The dark rectangles are the bypass capacitors connected to the power pins.

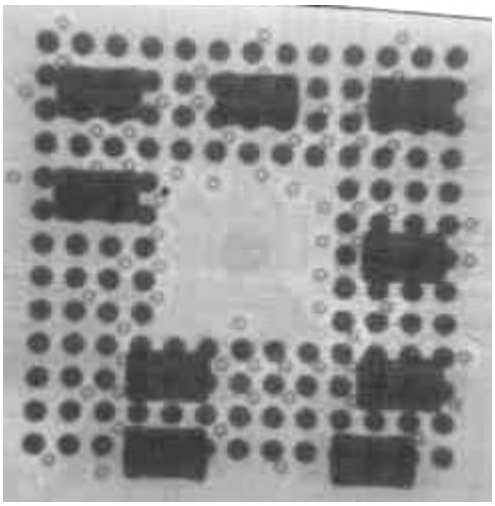


Figure 8. X-Ray of TMS320VC549GGU Alignment

An alternative is to populate the topside of the board with bypass capacitors around the periphery of the chip, leaving the underside for other discretes and ICs. In either solution some component density is lost.

4 Surface Mounting Process

Surface-mount technology has evolved over the past decade from an art into a science with the development of design guidelines and rules. While these guidelines are specific enough to incorporate many lessons learned, they are still general enough to allow an almost infinite variety of board layouts, solder pastes, stencils, fixturing and reflow profiles. From experience, most assembly operations have found MicroStar BGA packages to be robust, manufacturing-friendly packages which fit easily within existing processes and profiles plus do not require special handling. However, as ball pitch becomes smaller, layout methodology and placement accuracy becomes more critical. A review of some of the more important aspects of surface-mount technology is presented below with the objectives of looking to see how CSPs affect them and to provide suggestions that may aid efficient, cost-effective production.

4.1 Design for Manufacturability

A well-designed board that follows the basic surface-mount technology (SMT) considerations greatly reduces the cost and cycle time, and improves quality of the end product. Board design should comprehend the SMT automated equipment they will be assembled on, including minimum and maximum dimensional limits and placement accuracy. Many board shapes can be accommodated, but the front of the board should have a straight and square edge to help machine sensors detect it. While odd shaped or small boards can be assembled, they require panelization or special tooling to process in–line. The further a board gets from rectangular with no cutouts, the higher costs go for it.

Fiducials, (the optical alignment targets that align the module to the automated equipment) should allow vision-assisted equipment to accommodate the shrink and stretch of the raw board during processing. They also define the coordinate system for all automated equipment, such as printing and pick-and-place. The following guidelines have been found to be most helpful:

- Automated equipment requires a minimum of two and preferably three fuducials.
- The most useful configuration for the fiducials is an L which is orthogonal to optimize the stretch/shrink algorithms. When possible, the lower left fiducial should be the design origin (coordinate 0,0).
- All components should be within 4 inches of a fiducial to guarantee placement accuracy. For large boards or panels, a fourth fiducial should be added.
- A wide range of fiducial shapes and sizes can be used. Among the most useful is a circle 0.064 inches in diameter with an annulus of 0.126ID/0.146OD. The outer ring is optional, but no other feature may be within 0.031 inches of the fiducial.

If the edges of the boards are to be used for conveyer transfer, then a cleared zone of at least 0.125 inches should be allowed. Normally, the longest edges of the board are used for this purpose, and the actual width is dependent on equipment capability. While no component lands or fudicals can be in this area, breakaway tabs may be.

Interpackage spacing is a key aspect of DFM, and the question of how close you can safely put components to each other is a critical one. The following list of component layout considerations is recommendations based on TI experience:

- A minimum of 0.02 inches should exist between land areas of adjacent components to reduce the risk of shorting.
- The recommended minimum spacing between SMD component bodies is equal to the height of the tallest component. This allows for a 45 degree soldering angle in case manual work is needed.
- Polarization symbols need to be provided for discrete SMDs (diodes, capacitors, etc.) next to the positive pin.
- Pin one indicators or features are needed to determine the keying of SMD components.
- Space between lands (under components) on bottom side discrete components should be a minimum of 0.013 inches. No open vias may be in this space.
- Direction of bottom side discretes for wave solder should be perpendicular to direction through the wave.
- Do not put SMT components on the bottom side that exceed 200 grams per square inch of contact area with the board.
- Space permitting, symbolize all reference designators within the land pattern of the respective components.
- It is preferred to have all components oriented in well-ordered columns and rows.
- Group similar components together whenever possible.
- Allow room for testing.

4.1.1 Solder Paste

It is recommended to use solder paste when mounting MicroStar BGA, although it is possible to omit the paste, and only use a flux. The advantages of using paste are:

- Paste acts as a flux and aids wetting of the solder ball to the PCB land.
- Paste, being sticky, helps hold the component in place during reflow.
- Paste helps to overcome any minor variation in planarity of the solder balls.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.

Typically, the solder paste diameter and thickness as screened onto the board are as follows :

- Stencil diameter 350–375 microns.
- Stencil thickness 125–150 microns.

Paste selection is normally driven by overall system assembly requirements and a wide range of pastes has been found to work well. In general, the no-clean compositions are preferred due to the difficulty in cleaning under the mounted component. Most assembly operations have found that no changes in existing pastes are required by the addition of MicroStar BGA, but due to the large variety of board designs and tolerances, it is not possible to say this will be true for any specific application.

Very nearly as critical as paste selection is stencil design. A proactive approach to stencil design can pay large dividends in assembly yields and lower costs. In general, MicroStar BGA packages are special cases of BGA packages and the general design guidelines for BGA package assembly applies to them as well. There are some excellent papers on BGA assembly, so only a brief overview of issues especially important to MicroStar BGA packages will be presented here.

The typical stencil hole diameter needs to be the same size as the land area, and 125- to 150-micron thick stencils have been found to give the best results. Good release and consistent solder paste amounts and shapes is critical, especially as ball pitches decrease. The use of metal squeegee blades, or at the very least, high durometer poly blades, has been found to be very important in achieving this. Paste viscosity and how it varies during screening is another variable that requires close control.

4.2 Solder Ball Collapse

In order to produce the optimum solder joint, it is important to understand the amount of collapse of the solder balls, and the overall shape of the joint. These are a function of:

- The diameter of the package solder ball via
- The volume and type of solder paste screened onto the PCB
- The diameter of the PCB land
- The board assembly reflow conditions
- The weight of the package

The original ball height on the package is 0.40 mm. After the package is mounted, this typically drops to 0.35 mm. See Figure 9.

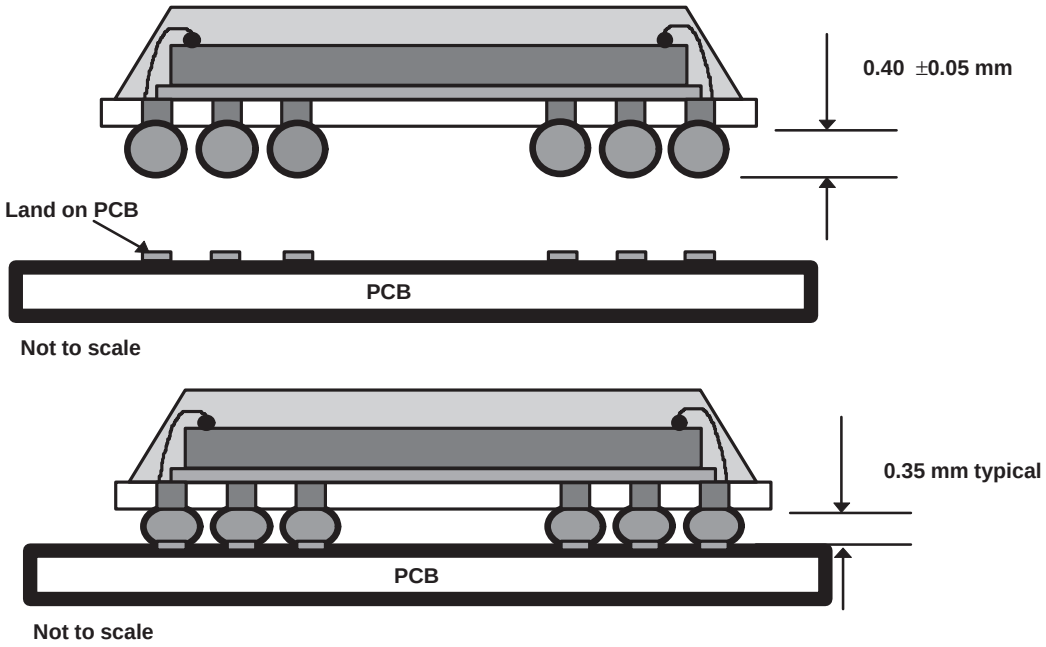


Figure 9. Solder Ball Collapse During Surface Board Mounting

Controlling this collapse, and thus defining the package standoff, is critical in order to obtain the optimum joint reliability. Generally a larger standoff gives better solder joint fatigue strength, but this should not be achieved by reducing the board land diameter. Reducing the land diameter will increase the standoff, but will also reduce the minimum cross-section area of the joint. This, in turn, will increase the maximum shear force at the PCB side of the solder joint. Thus, a land diameter reduction will normally result in a worse fatigue life and should be avoided unless the consequences are well understood. See paragraph 3.1, Land Size, for the optimum land diameter. Figure 10 shows the effect of differences between PCB land diameter size and package land size.

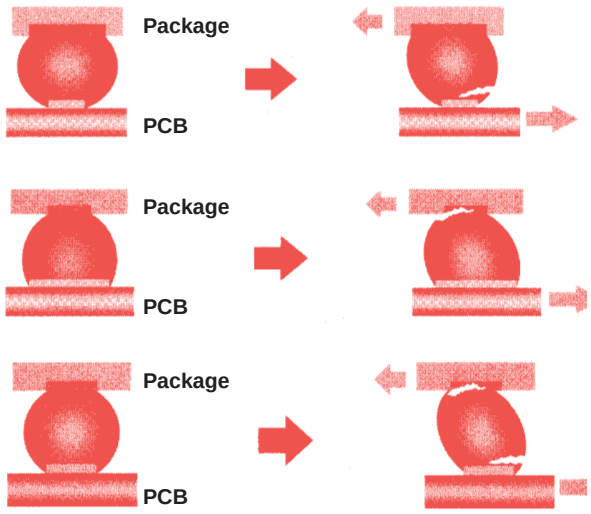


Figure 10. Package Land Size vs PCB Land Size

In the top view, the package via is larger and the solder ball is prone to crack prematurely at the PCB interface. In the middle view, the PCB via is larger leading to cracks at the package surface. In the bottom view where the ratio is almost one-to-one, the stresses are equalized and neither site is more susceptible to cracking than the other.

4.3 Surface Mount Reflow

Solder reflow conditions are the next critical step in the mounting process. During reflow, the solvent in the solder paste evaporates, the flux cleans the metal surfaces, the solder particles melt, wetting of the surfaces takes place by wicking of molten solder, the solder balls collapse, and finally solidification of the solder into a strong metallurgical bond completes the process. The desired end result is a uniform solder structure strongly bonded to both the PCB and the package with few or no voids and a smooth, even fillet at both ends. Conversely, when all the steps do not carefully fit together, voids, gaps, uneven thickness, discontinuities, and insufficient fillet can occur. While the exact cycle used depends on the reflow system and paste composition, there are several key points all successful cycles have in common.

The first of these is a warm-up period sufficient to safely evaporate the solvent. This can be done with a preheat or a bake, or, more commonly, a hold in the cycle at evaporation temperatures. If there is less solvent in the paste (such as in a high viscosity, high metal content paste), then the hold can be shorter. However, when the hold is not long enough to get all of the solvent out or too fast to allow it to evaporate, many negative things happen. These range from solder ball formation to heating too fast to allow trapped gases to escape, which can cause voids at best and embrittlement in the worst case. A significant number of reliability problems with solder joints can be solved with the warm-up step, so it needs careful attention.

The second thing successful cycles have in common is uniform heating across the package and the board. Solder will wick to the hottest spot, so uneven solder thickness may be an indicator that the profile needs adjusting. There can also be a problem when different sized components are reflowed at the same time. Care needs to be taken when profiling an oven to be sure that the indicated temperatures are representative of what the most difficult to reflow parts are seeing. These problems are more pronounced with some reflow methods, such as infrared (IR) reflow than with others, such as forced hot-air convection.

The type of reflow method used will also affect the third thing successful cycles have in common: a balance between too low, too late or too short and too long, too hot or too fast. The latter cycle may lead to excessive fluxing activation, oxidation or even damage to the package. Heating the paste too hot too fast before it melts can also dry the paste, which leads to poor wetting.

The profile shown in Figure 11 is ideal for use in a forced air convection furnace, which is the most highly recommended type. The best results have been found in a nitrogen atmosphere.

MicroSTAR BGA Reflow Profile

RT to 140°C	60 – 90 sec.
140°C to 180°C	60 – 120 sec.
Time above 183°C	60 – 75 sec.
Peak Temp.	230°C ±5°C
Time within 5 degrees Peak temp: 10–20 sec.	
Ramp down rate	6°C/sec. Max.

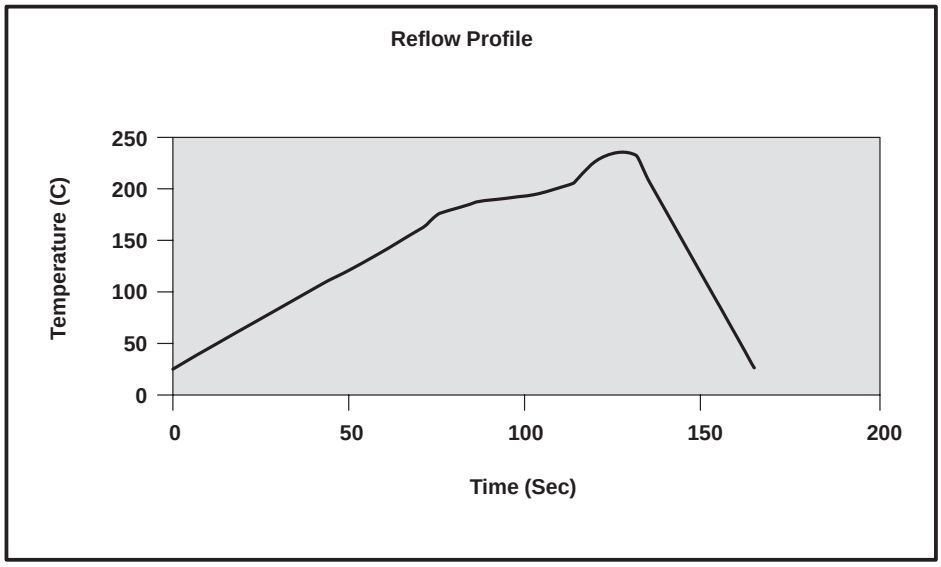


Figure 11. Ideal Reflow Profile for MicroStar BGA

It should be noted that at the time of producing this application report many MicroStar BGA packages are moisture sensitive, and the time out of a dry environment should be controlled according to the label on the packing material. This will prevent moisture absorption problems with the ICs such as popcorning or delamination.

Other problems frequently seen with BGA packages are those caused by the PCB bowing or twisting during reflow. As PCBs get thinner, this problem will become more significant. Potential problems from these effects will show up as open pins, hourglass solder joints, or solder discontinuities. Proper support of the PCB through the furnace, balancing the tab attachments to a panel, and, in worst cases, using a weight to stiffen the PCB are actions that can be used to prevent this.

4.4 Inspection

MicroStar BGA has been designed to be consistent with very high yielding assembly processes. It is recommended that you inspect the solder joint quality during process development. Once a quality process has been developed, inspection should not be necessary. If desired, inspection can be done with either transmission x-ray or laminographic x-ray techniques.

5 Thermal Properties

The thermal performance of most packages is very dependant on the type of board on which they are mounted and on the ambient conditions around the board. This is also true for MicroStar BGA.

Texas Instruments has extensive package characterization capabilities, including an electrical measurements lab with TDR LRC and network analysis capabilities, a thermal measurements lab with JEDEC standard test conditions up to 1000 watts, and extensive electrical, thermal, and mechanical modeling capability. Modeling was implemented at TI starting in 1984. Stress analysis is done with the Ansys Analysis tool, which provides full linear, nonlinear, 2D and 3D capabilities for solder reliability, package warpage, and stress analysis studies. An internally developed tool (PACED) is used for electrical modeling that gives 2.5D and full 3D capability for LRC models, transmission lines, lossy dielectrics, and SPICE deck outputs. The thermal modeling tool is also internally developed (ThermCAL) and it provides full 3D automatic mesh generation for most packages. Complex geometries, transient analysis, and anisotropic materials can be modeled with it. With these capabilities, a full range of modeling from device level through system level can be provided. Package modeling is used to predict package performance at the design stage, to provide a package development tool, to aid qualification by similarity, and as a failure analysis tool.

5.1 Thermal Modeling

Figure 12 outlines the thermal modeling process. Data for each package is included in paragraph 6.1, Package Information.

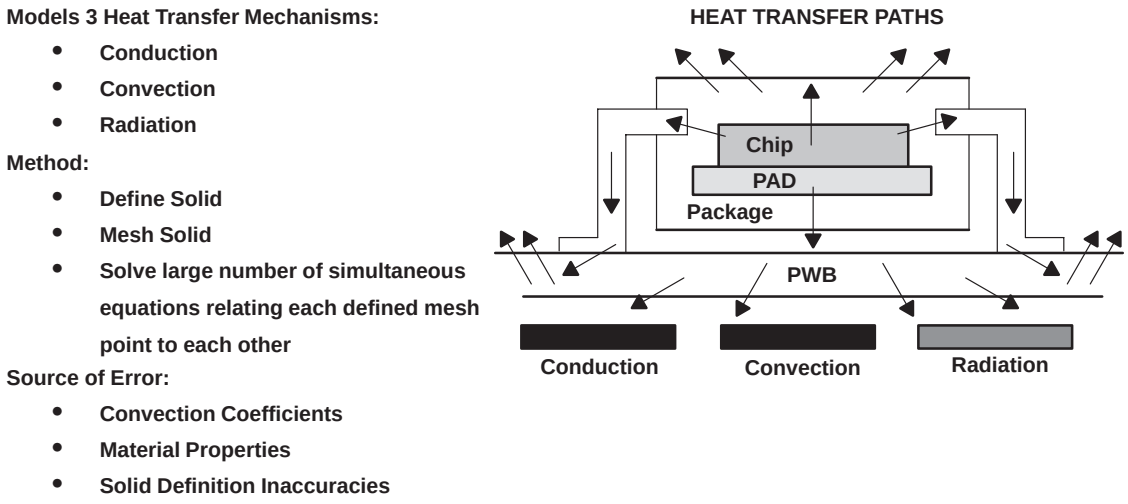


Figure 12. Outline of the Thermal Modeling Process

6 Electrical Properties

Figure 13 outlines the electrical modeling process. Data for each package is included in paragraph 6.1, Package Information.

- **Calculates inductances, capacitances, resistances, transmission line characteristics of package geometries**
- **Uses as loads for circuit simulation**
- **Process**
  - **– select solution algorithm for problem domain**
  - **– identify package structures to be modeled**
  - **– generate spice deck of package parameters**
  - **– simulate impact on driver output waveforms**
  - **– calculate ground/power bounce**

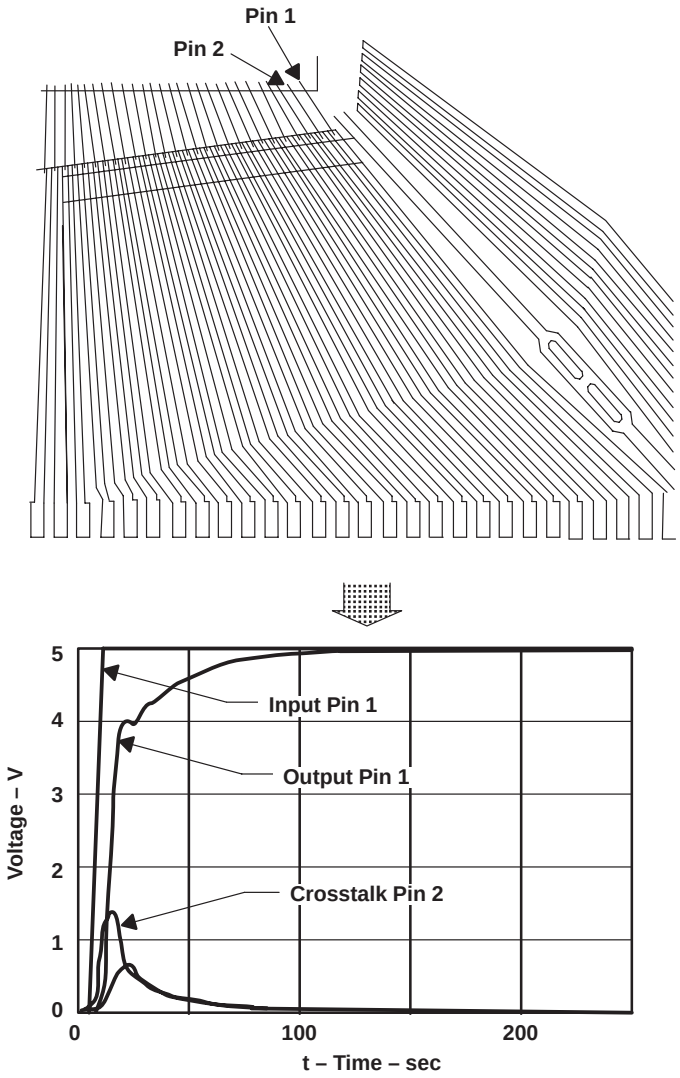


Figure 13. Outline of the Electrical Modeling Process

The following is a table of resistance, self inductance, and self capacitance.

Table 6. RLC Data for 256-Pin MicroStar BGA (12×12 body, 0.80 pitch)

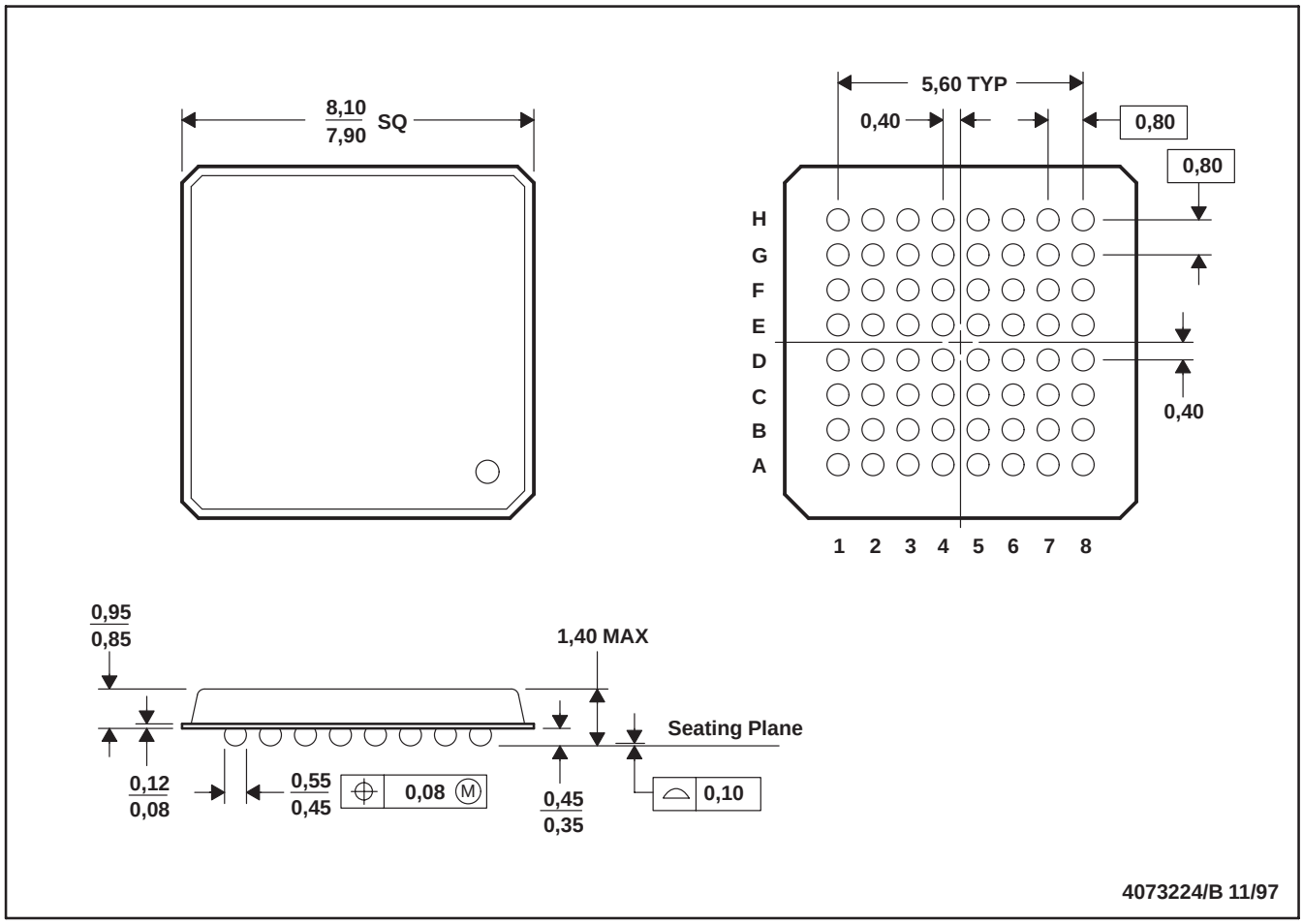
	R (Ohms)	L (nH)	C (pF)
Minimum	0.052	1.438	0.215
Mean	0.055	1.958	0.305
Maximum	0.062	3.095	0.563

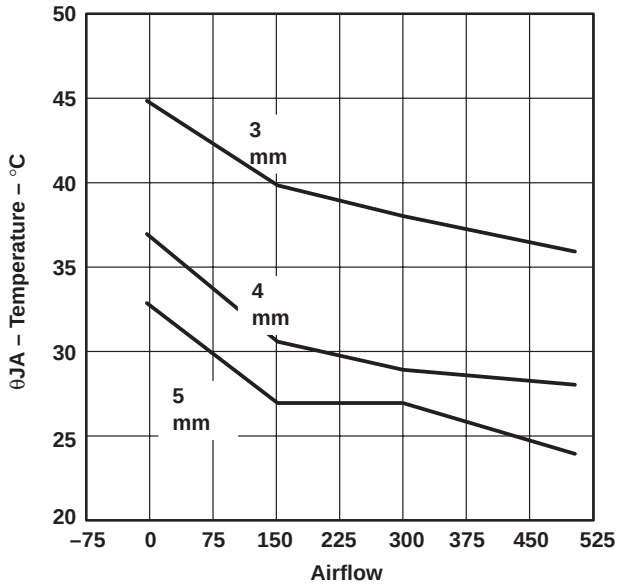
Table 7. RLC Data for 208-Pin MicroStar BGA (12×12 body, 0.80 pitch)

	R (Ohms)	L (nH)	C (pF)
Minimum	0.070	1.824	0.217
Mean	0.075	2.266	0.278
Maximum	0.079	3.416	0.433

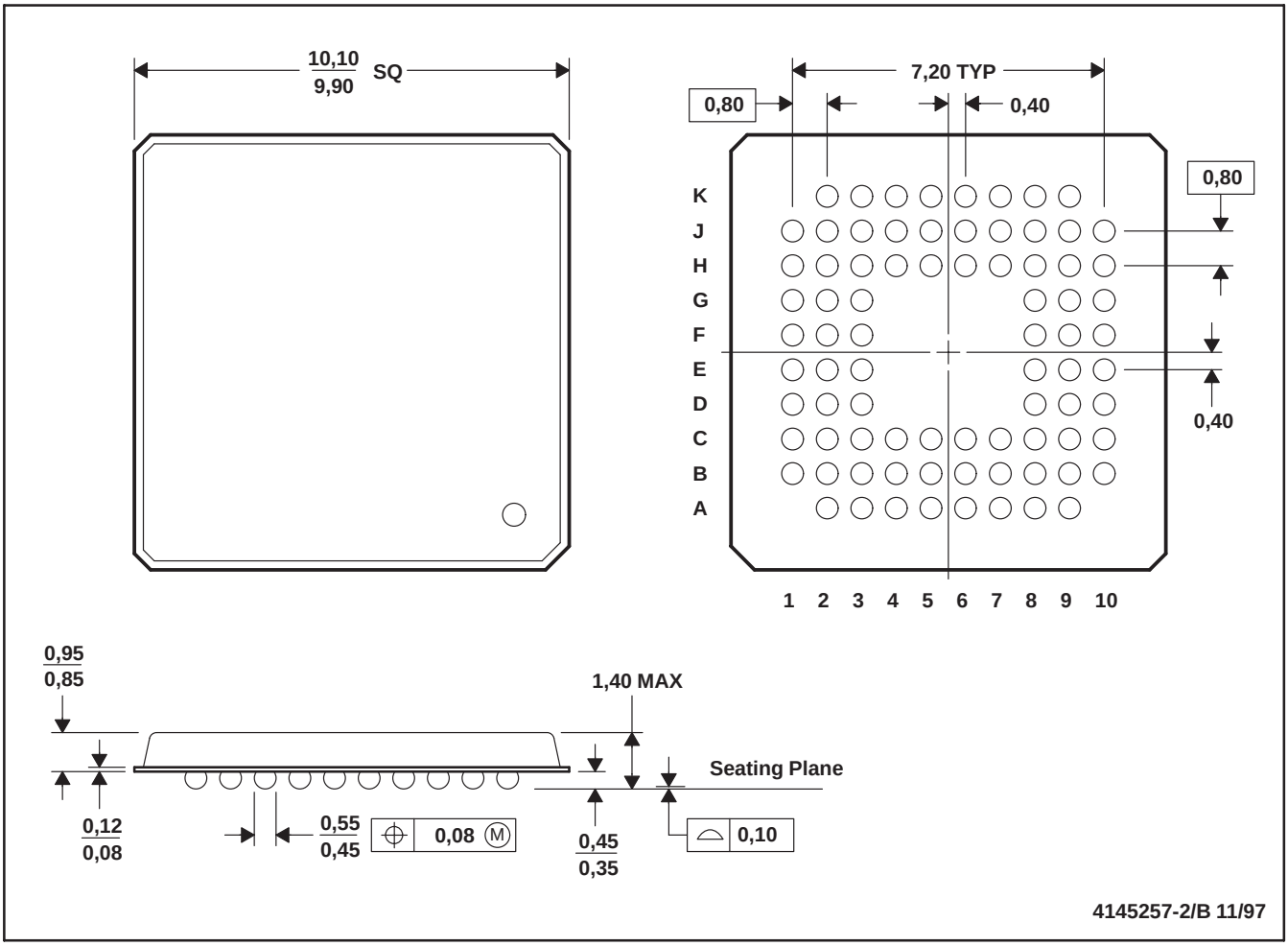
6.1 Package Information

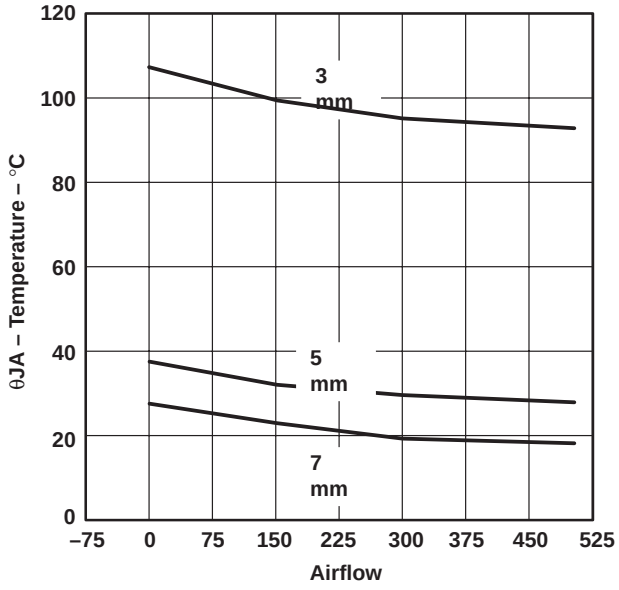
GGV (S-PBGA-N64) PLASTIC BALL GRID ARRAY



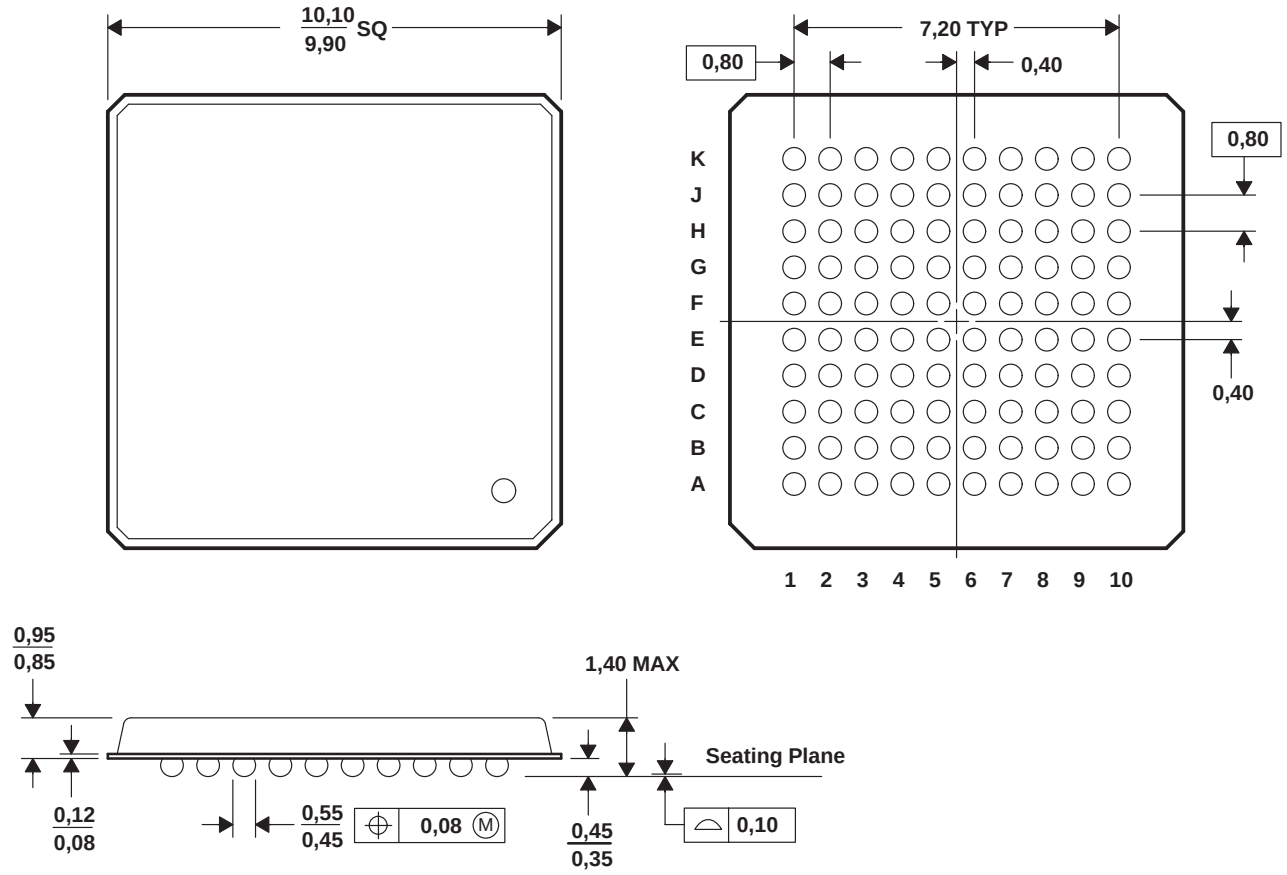


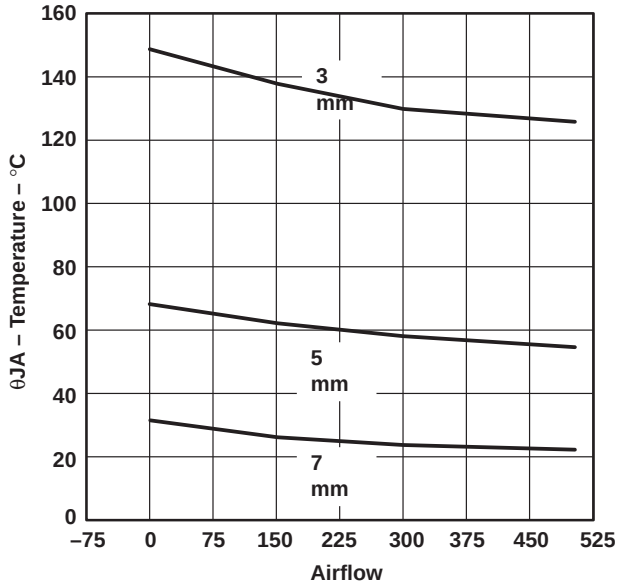
GGM (S-PBGA-N80) PLASTIC BALL GRID ARRAY



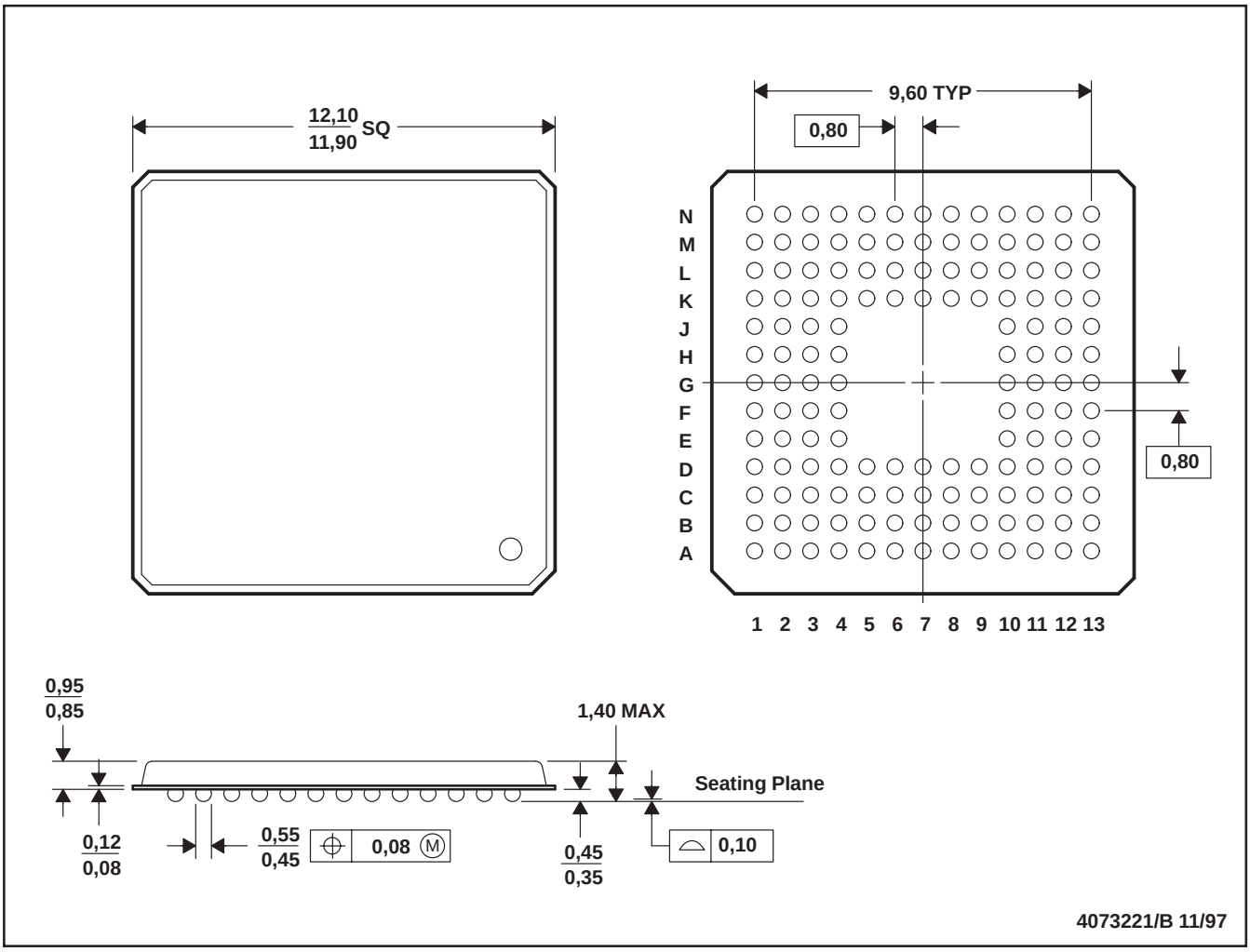


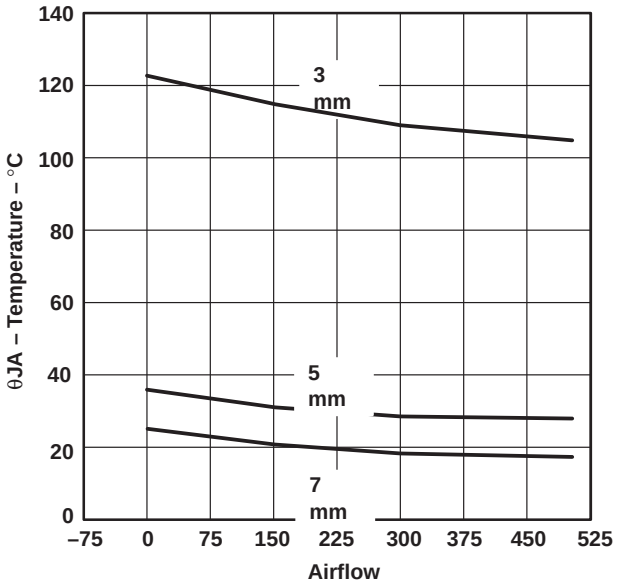
GGM (S-PBGA-N100) PLASTIC BALL GRID ARRAY



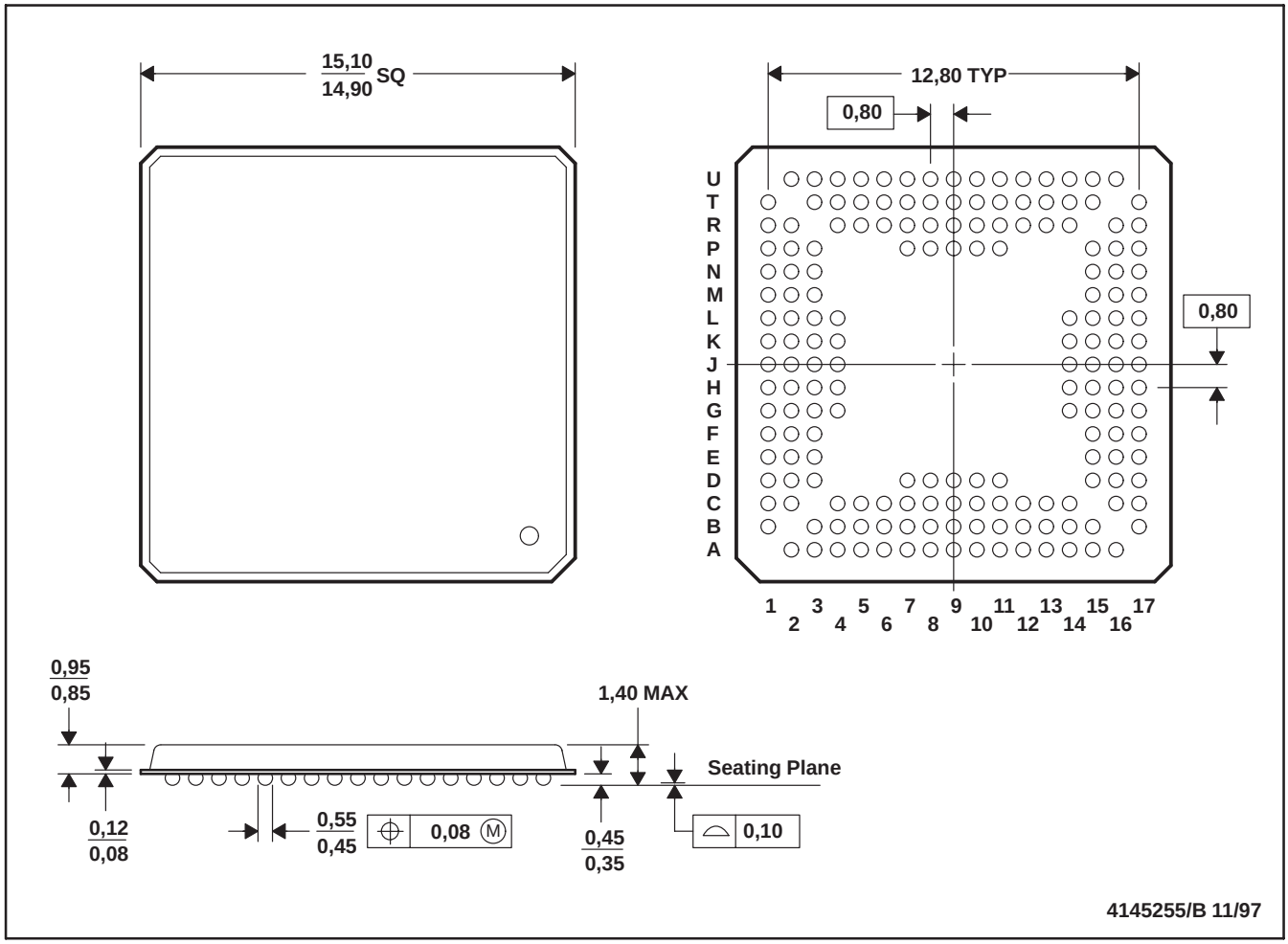


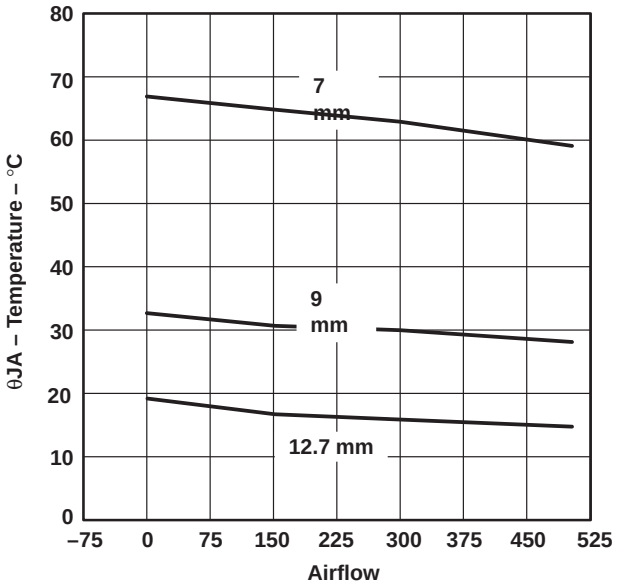
GGU (S-PBGA-N144) PLASTIC BALL GRID ARRAY



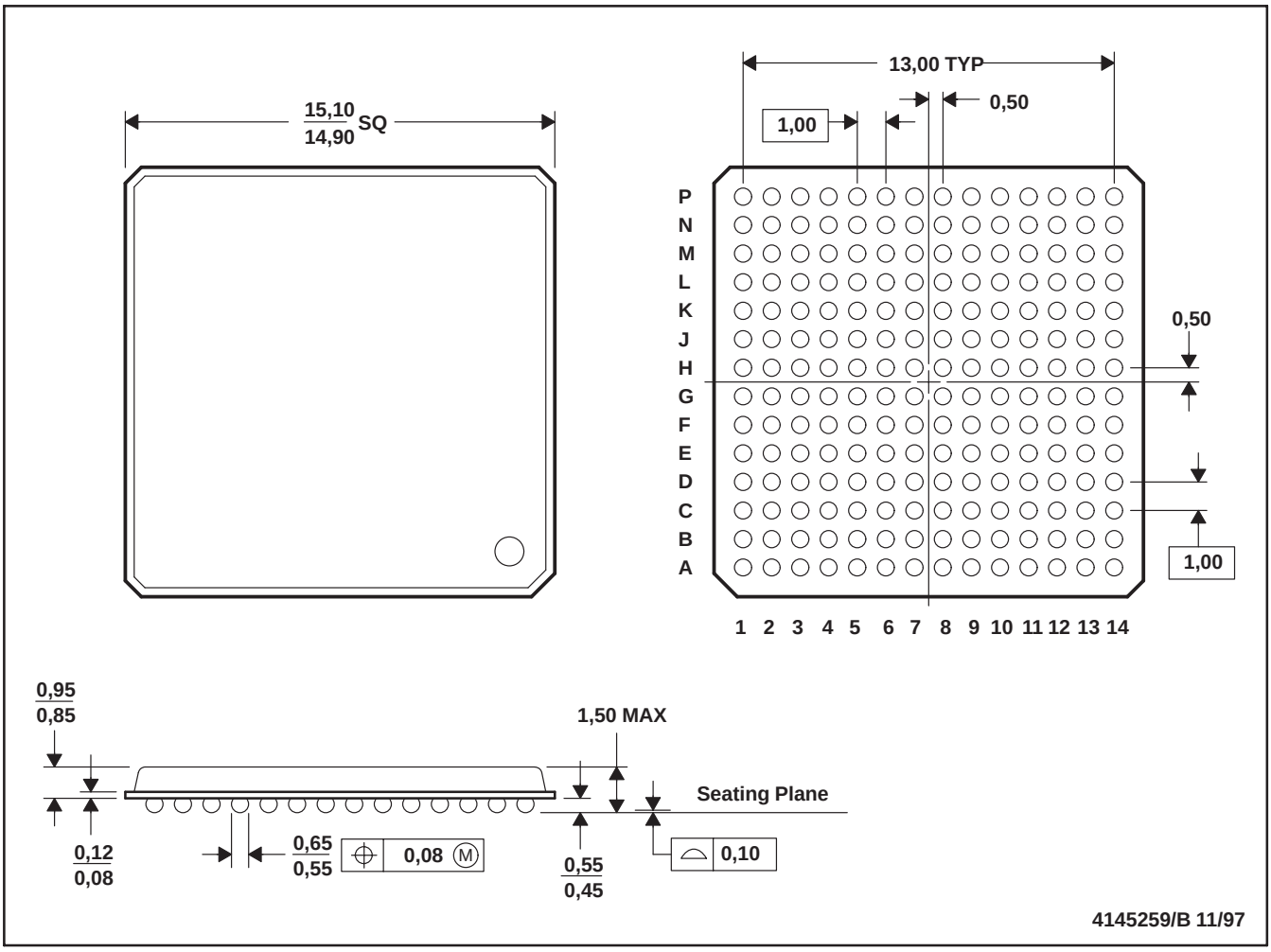


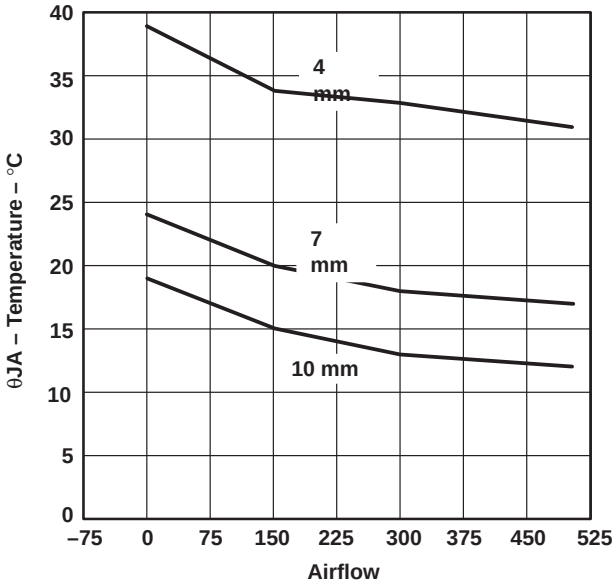
GGW (S-PBGA-N176) PLASTIC BALL GRID ARRAY



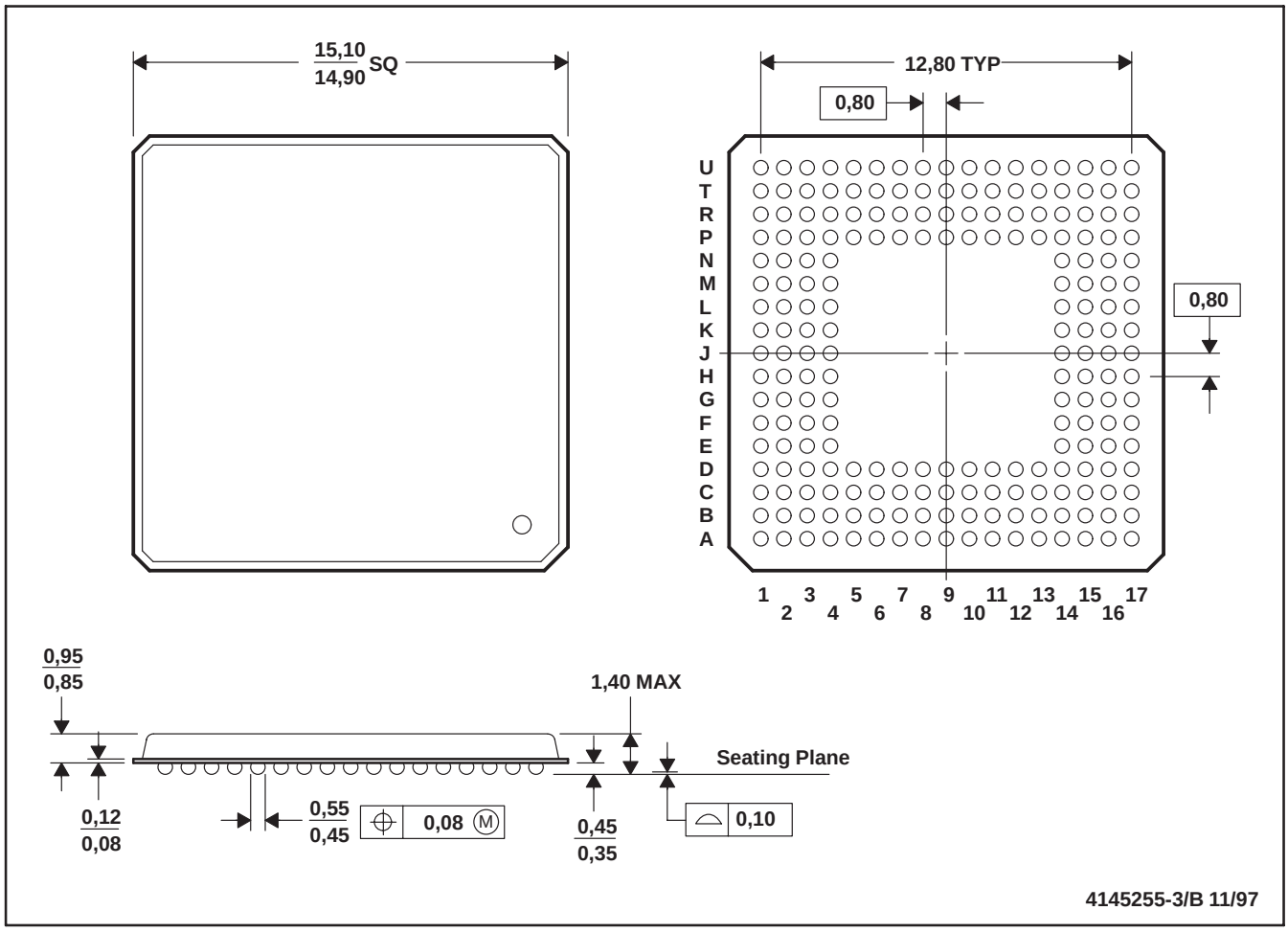


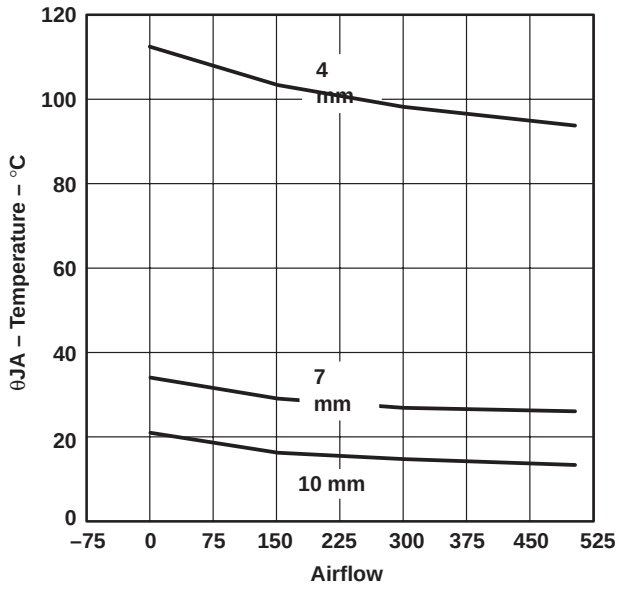
GHC (S-PBGA-N196) PLASTIC BALL GRID ARRAY



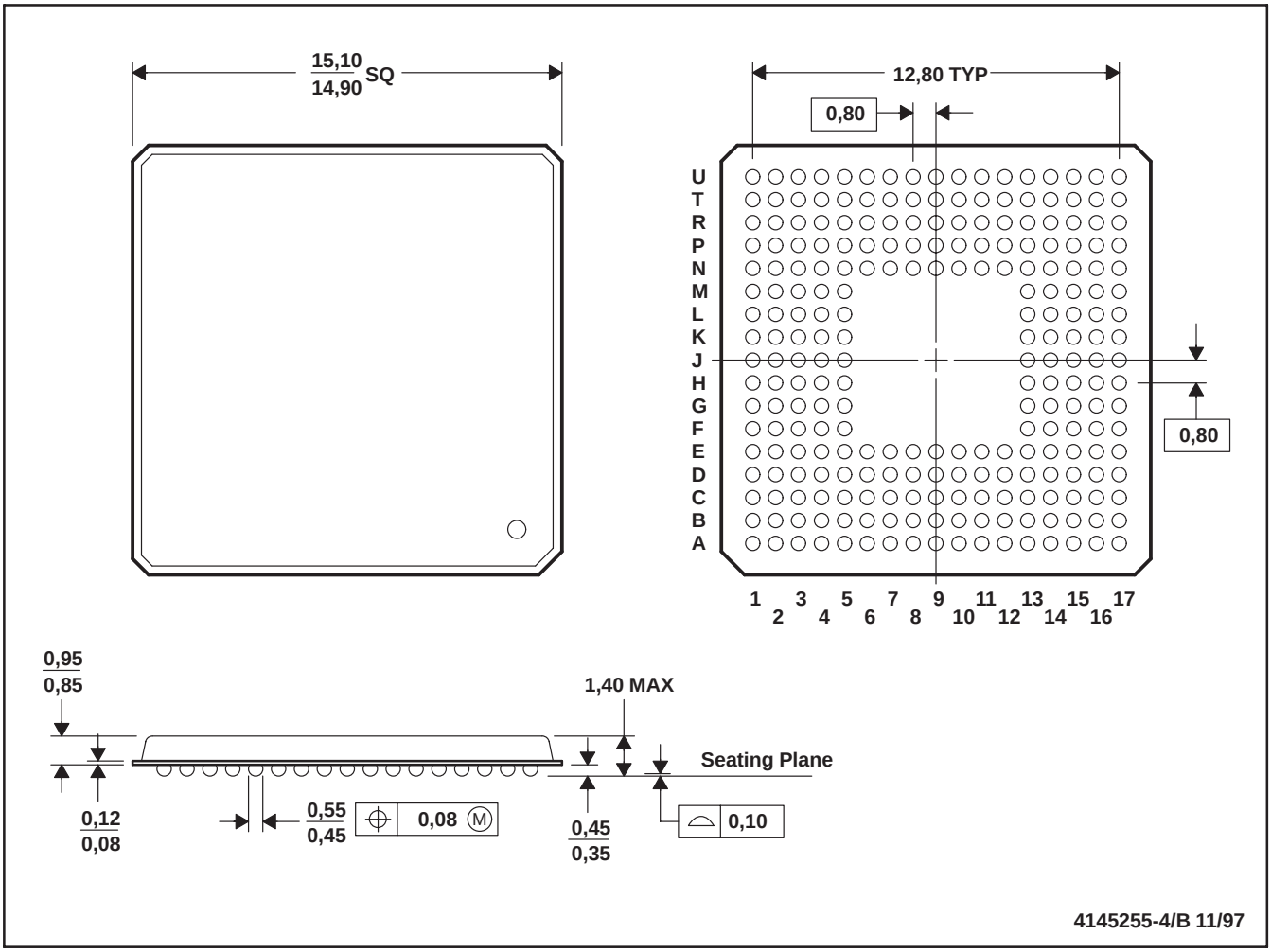


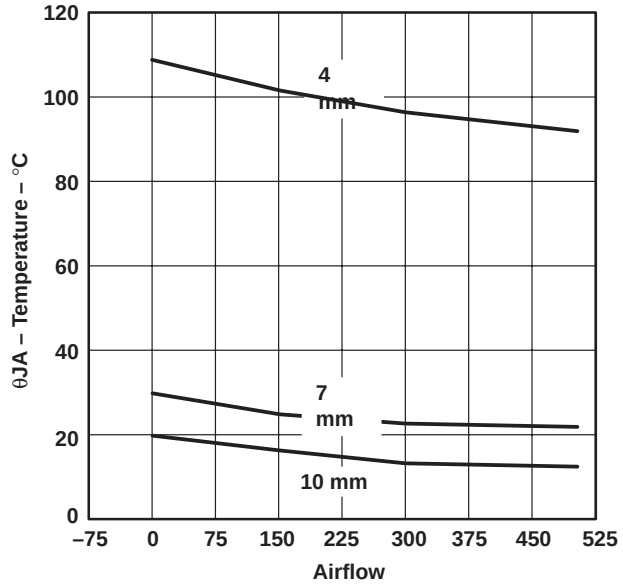
GGW (S-PBGA-N208) PLASTIC BALL GRID ARRAY





GGW (S-PBGA-N240) PLASTIC BALL GRID ARRAY





Appendix A MicroStar BGA Package Layers

Sample routing from PCI1450 MicroStar BGA package to the equivalent TQFP footprint.

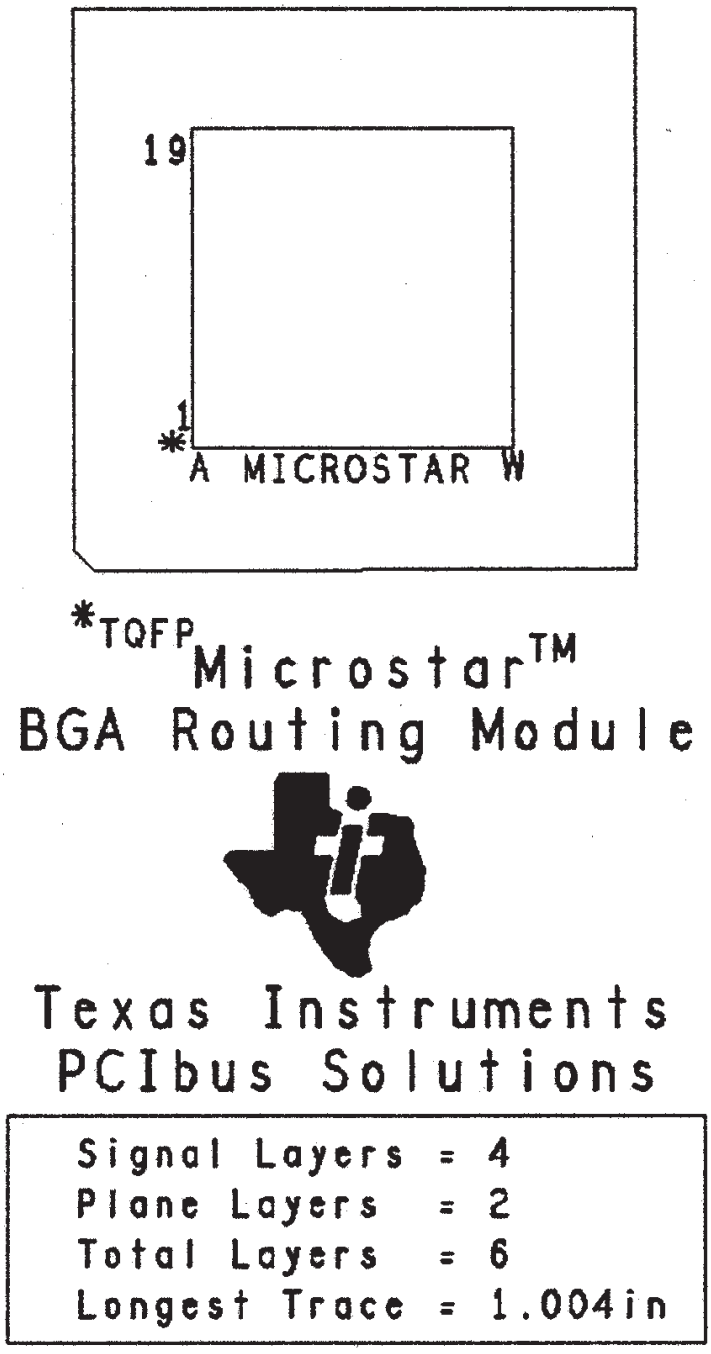


Figure B–1. MicroStar BGA Silkscreen

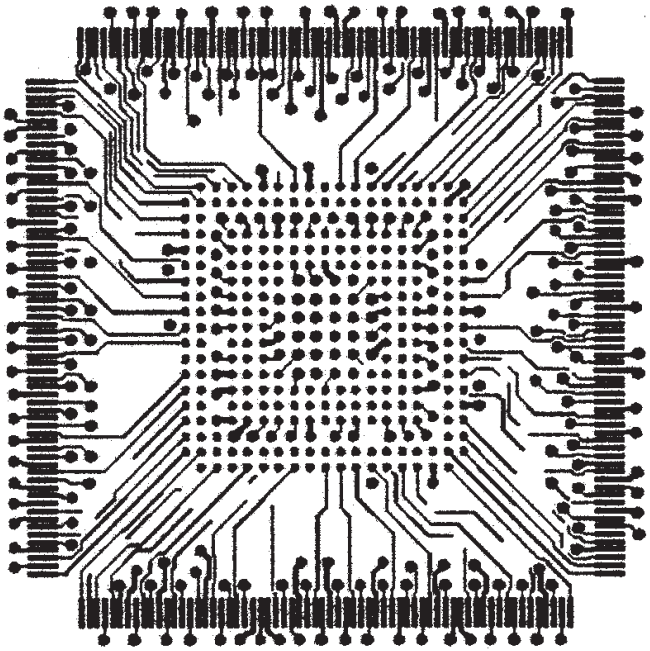


Figure B–2. MicroStar BGA Top Layer

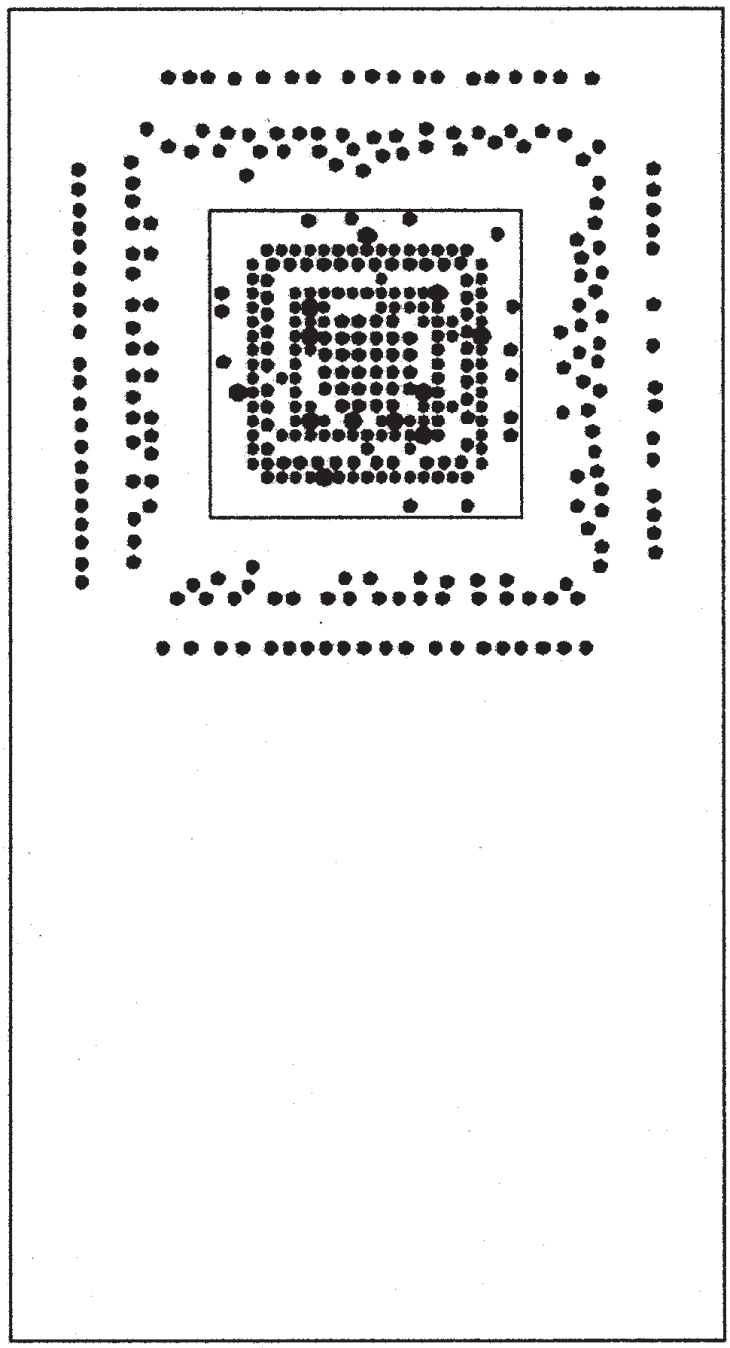


Figure B–3. MicroStar BGA Layer 2 – Power Plane

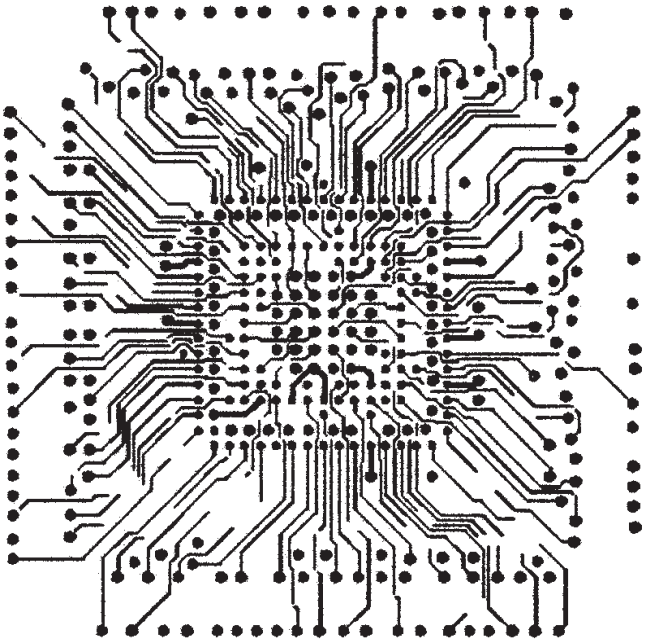


Figure B–4. MicroStar BGA Layer 3 – Signal

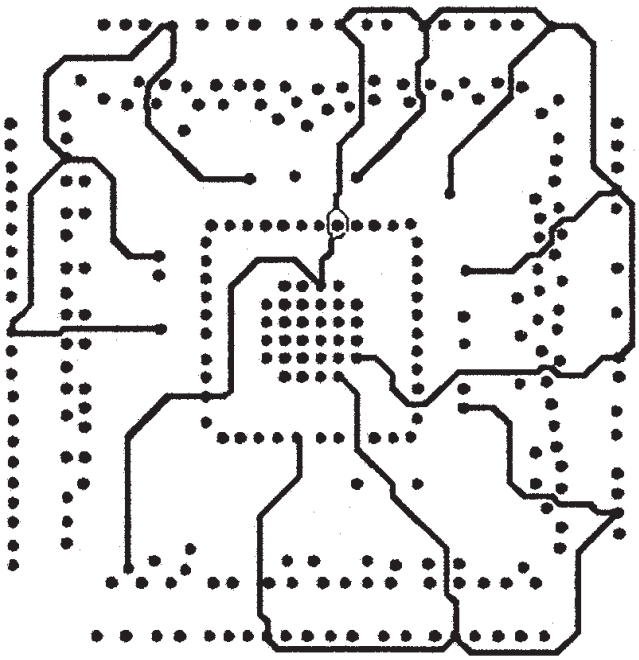


Figure B–5. MicroStar BGA Layer 4 – Signal

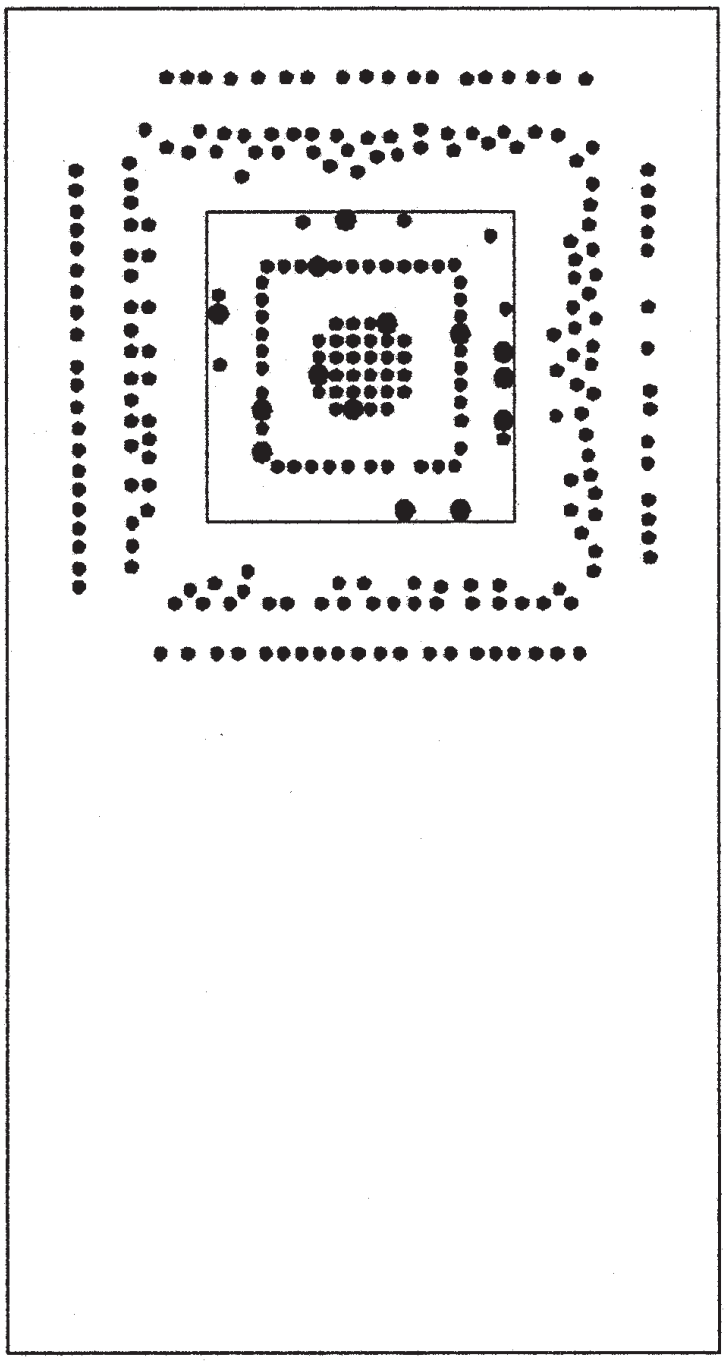


Figure B–6. MicroStar BGA Layer 5 – Ground Plane

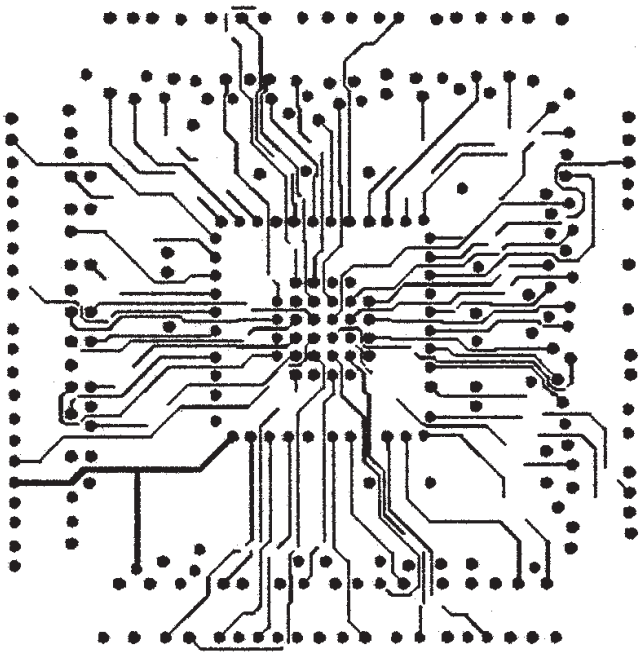


Figure B–7. MicroStar BGA Bottom Layer