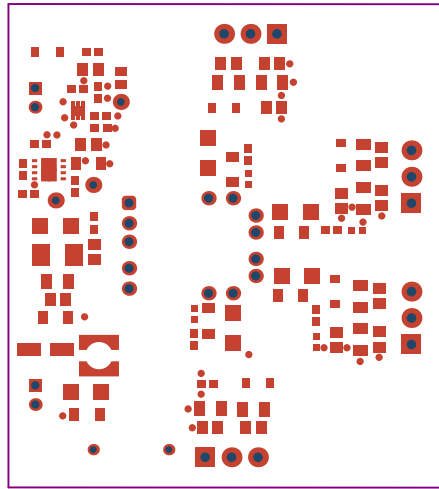
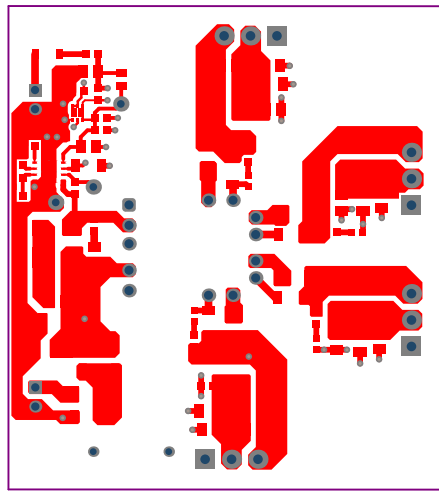


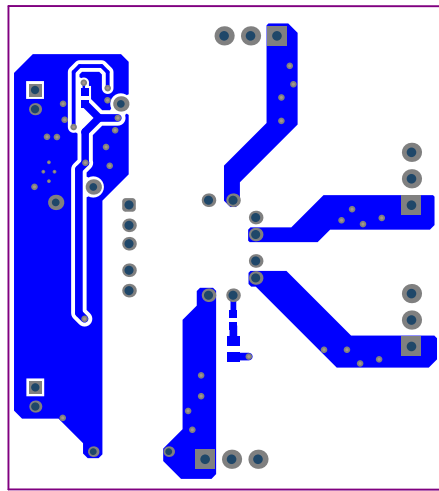
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010006	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Overlay	TID #: 010006		
PLOT NAME = Top Overlay	GENERATED : 2/28/2019 2:44:30 PM	TEXAS INSTRUMENTS	



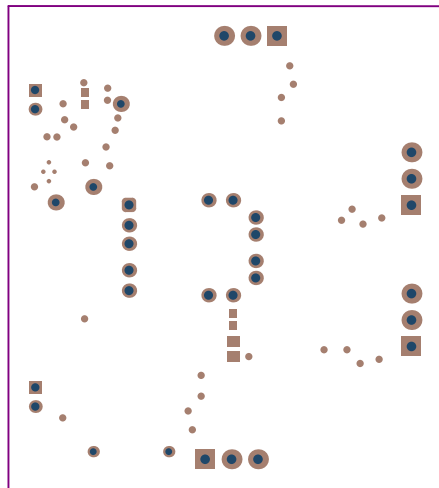
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010006	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Solder	TID #: 010006		
PLOT NAME = Top Solder Mask	GENERATED : 2/28/2019 2:44:30 PM	TEXAS INSTRUMENTS	



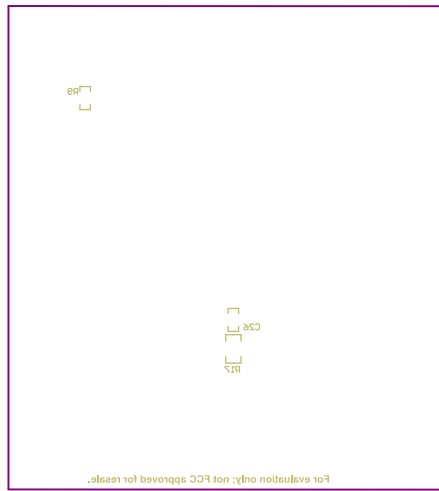
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010006	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Layer	TID #: 010006		
PLOT NAME = Top Layer	GENERATED : 2/28/2019 2:44:31 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010006	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Bottom Layer	TID #: 010006		
PLOT NAME = Bottom Layer	GENERATED : 2/28/2019 2:44:31 PM	TEXAS INSTRUMENTS	

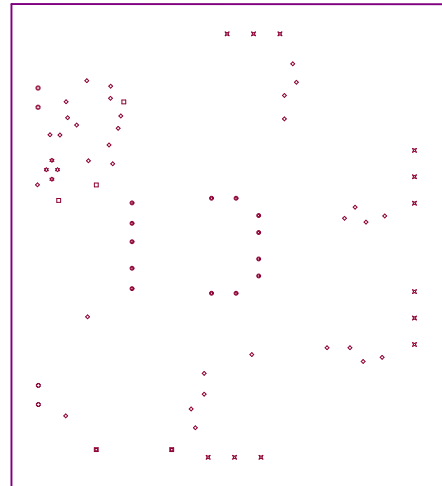


ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010006	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Bottom Solder	TID #: 010006		
PLOT NAME = Bottom Solder Mask	GENERATED : 2/28/2019 2:44:31 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010006	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Bottom Overlay	TID #: 010006		
PLOT NAME = Bottom Overlay	GENERATED : 2/28/2019 2:44:31 PM	TEXAS INSTRUMENTS	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 High Tg	59.20mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				



Symbol	Quantity	Finished Hole Size	Plated	Hole Type
☆	4	7.87mil (0.200mm)	PTH	Round
◇	33	16.00mil (0.406mm)	PTH	Round
■	2	35.43mil (0.900mm)	PTH	Round
□	3	40.00mil (1.016mm)	PTH	Round
⊙	4	43.31mil (1.100mm)	PTH	Round
⊗	13	47.24mil (1.200mm)	PTH	Round
⊠	12	50.00mil (1.270mm)	PTH	Round
	71 Total			

Drill tolerances:
 For 7.87mil drill via +0/-7.87 mil
 For 16 mil drill via +0/-16 mil
 For PTH +/- 3 mil

NOTE:
 1. vias are non tented
 2. This not an impedance controlled board

DESIGN INFORMATION

MIN. TRACK WIDTH: 10 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 19.685 MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 63 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



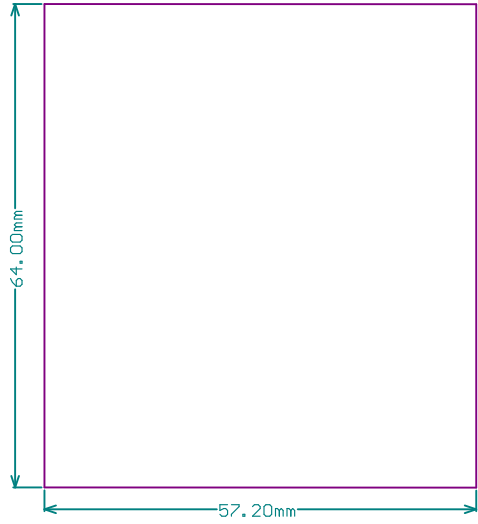
PROJECT TITLE:
 Isolated IGBT Gate-Drive Power Supply Reference Design

DESIGNED FOR:
 Public Release

FILE NAME:
 TIDA-010006-E2.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010006	REV: E2	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = Drill Drawing	TID #: 010006			
PLOT NAME = Drill Drawing	GENERATED : 2/28/2019 2:44:31 PM	TEXAS INSTRUMENTS		

ENGINEER: Vaibhavi	LAYOUT BY: Avinash N
SCALE: 1.00	ALTIM DESIGNER VERSION: 18.1.9.240



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010006	REV: E2	SUN REV: Not In VersionControl
LAYER NAME =	TID #: 010006		
PLOT NAME = Board Dimensions	GENERATED : 2/28/2019 2:44:31 PM	TEXAS INSTRUMENTS	

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated