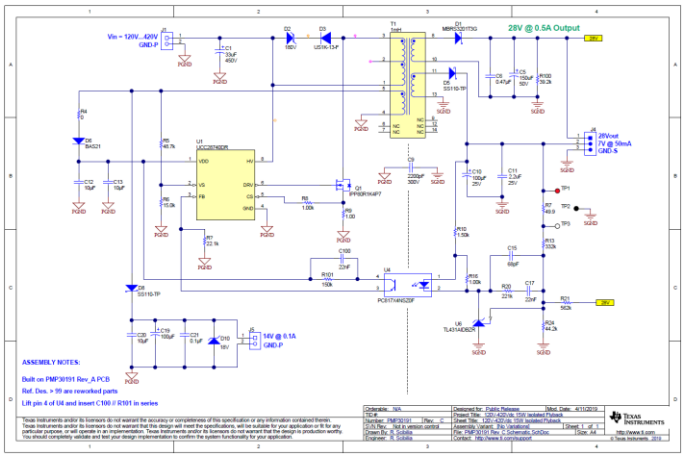
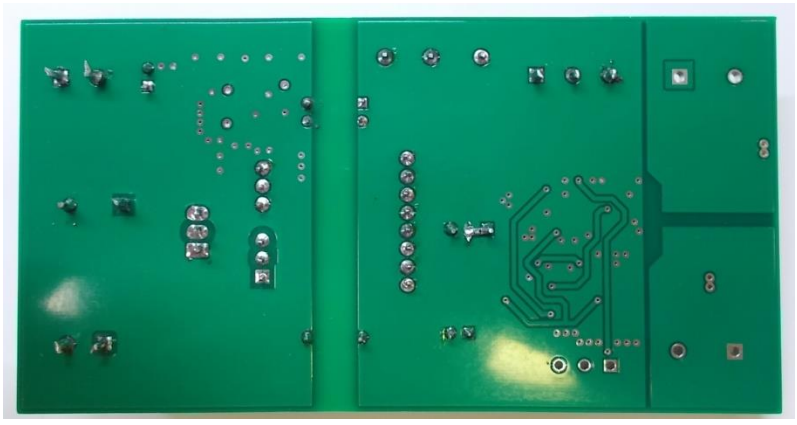
Test Report: PMP30191

15-W Opto-Regulated Multi-Output Flyback Converter Reference Design for Auxiliary Supply

Description

This reference design is an isolated opto-regulated, multi-output, 15-W flyback converter. Both 28-V and 7-V outputs are contributing to the voltage regulation on secondary side, while a third output (14 V at 100 mA) is referenced to the primary side ground. This converter has low stand-by power, between 45 mW and 61 mW in the whole Vin range, and has good efficiency at full load (88.8% to 89.6%). The PMP30191 Rev_C Reference Design has been built on PMP30191 Rev_A PCB.





1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage	120 - 420 VDC
Output #1, Voltage	28 V
Output #1, Current	500 mA
Output #2, Voltage	7 V
Output #2, Current	50 mA
Output #3, Voltage	14 V
Output #3, Current	100 mA

1.2 Required Equipment

- 0…450 V, (min. 200 mA), constant voltage source (VS1)
- 0…40 V, (0…1A), constant current electronic load
- 0…10 V, (0…100 mA), constant current electronic load
- 0…20 V, (0…200 mA), constant current electronic load
- Oscilloscope (min. 100 MHz bandwidth)

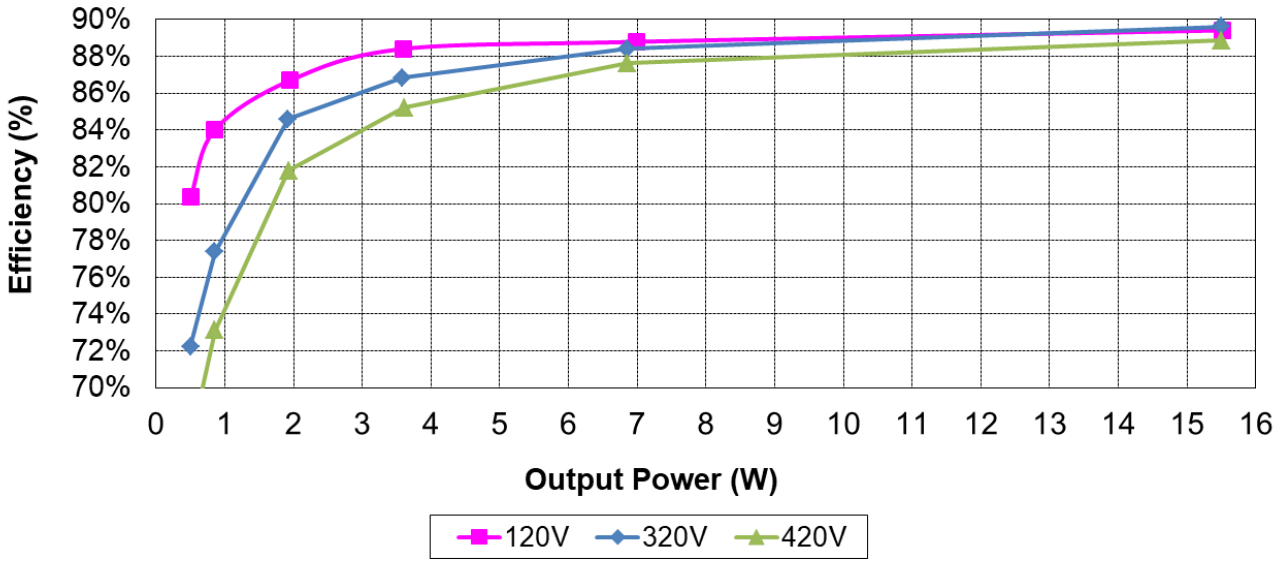
1.3 Considerations

a) Connect the source VS1 to pin 1 & 2 of J1.
b) Connect two loads to J4 (pin 1 & 2) with common ground to pin 3, set to CC mode.
c) Connect one load to J5 (pin 1 & 2) with primary ground to pin 2, set to CC mode.
d) Connect oscilloscope probes to Q1-Drain and D1-Anode versus primary and secondary grounds. For testing purposes it is possible to connect primary and secondary grounds, when an isolated constant voltage source is used (bench power supply VS1).
e) Connect oscilloscope probes to all outputs in AC coupling to measure ripple and noise.

2 Testing and Results

2.1 *Efficiency Graphs:*

The efficiency graph, versus total output power, is shown below. The voltage of power source has been set to 120 V, 320 V and 420 V.



2.2 *Efficiency Data:*

The efficiency graph reports the data from the tables shown below:

Vin(V)	Iin(mA)	Pin (W)	V14 (V)	V28 (V)	V7 (V)	I14 (mA)	I28 (mA)	I7 (mA)	Pout (W)	Efficiency (%)
120	0.376	0.045	14.73	28.23	6.284	0	0	0	0	0%
120	5.19	0.623	13.58	28.27	6.263	6.7	11.2	14.8	0.501	80.37%
120	8.43	1.012	13.47	28.05	6.387	10.3	21.9	15.1	0.850	84.00%
120	18.72	2.246	13.48	28.11	6.353	23.3	51.3	30.1	1.947	86.69%
120	33.84	4.061	13.38	27.93	6.459	40.4	102.1	30.6	3.590	88.40%
120	65.58	7.870	13.29	27.91	6.467	81.5	200.9	46.0	6.988	88.79%
120	144.62	17.35	13.41	27.68	6.603	100.3	500.8	46.9	15.52	89.41%

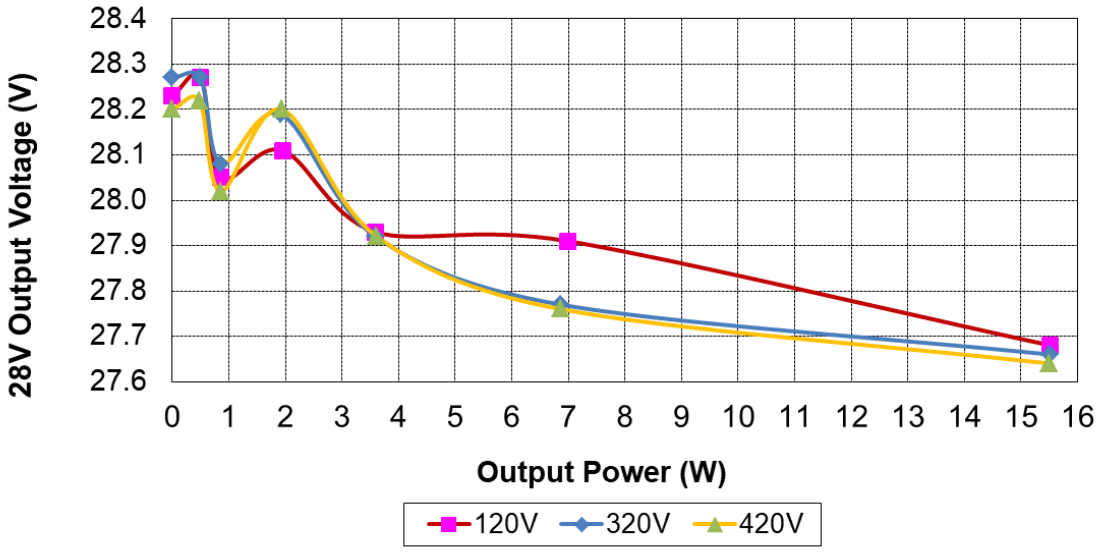
Vin(V)	Iin(mA)	Pin (W)	V14 (V)	V28 (V)	V7 (V)	I14 (mA)	I28 (mA)	I7 (mA)	Pout (W)	Efficiency (%)
320	0.1606	0.051	15.51	28.27	6.262	0	0	0	0	0%
320	2.17	0.694	13.75	28.27	6.261	6.7	11.2	14.8	0.502	72.24%
320	3.46	1.107	13.60	28.08	6.368	10.7	21.9	15.1	0.857	77.36%
320	7.08	2.266	13.55	28.19	6.305	20.8	51.3	29.9	1.916	84.59%
320	12.91	4.131	13.36	27.92	6.463	40.3	102.1	30.6	3.587	86.83%
320	24.25	7.760	13.20	27.77	6.552	81.7	200.9	31.1	6.861	88.41%
320	54.07	17.30	13.39	27.66	6.616	100.3	500.8	47.0	15.51	89.62%

Vin(V)	Iin(mA)	Pin (W)	V14 (V)	V28 (V)	V7 (V)	I14 (mA)	I28 (mA)	I7 (mA)	Pout (W)	Efficiency (%)
420	0.1442	0.061	14.64	28.20	6.304	0	0	0	0	0%
420	1.71	0.718	13.63	28.22	6.286	5.1	11.2	14.9	0.479	66.72%
420	2.78	1.168	13.48	28.02	6.402	10.6	21.9	15.2	0.854	73.11%
420	5.61	2.356	13.51	28.20	6.301	21.6	51.3	29.9	1.927	81.77%
420	10.09	4.238	13.36	27.92	6.463	41.9	102.2	30.6	3.611	85.21%
420	18.64	7.829	13.20	27.76	6.555	81.8	200.9	31.1	6.860	87.63%
420	41.52	17.44	13.39	27.64	6.623	100.2	500.8	47.1	15.50	88.86%

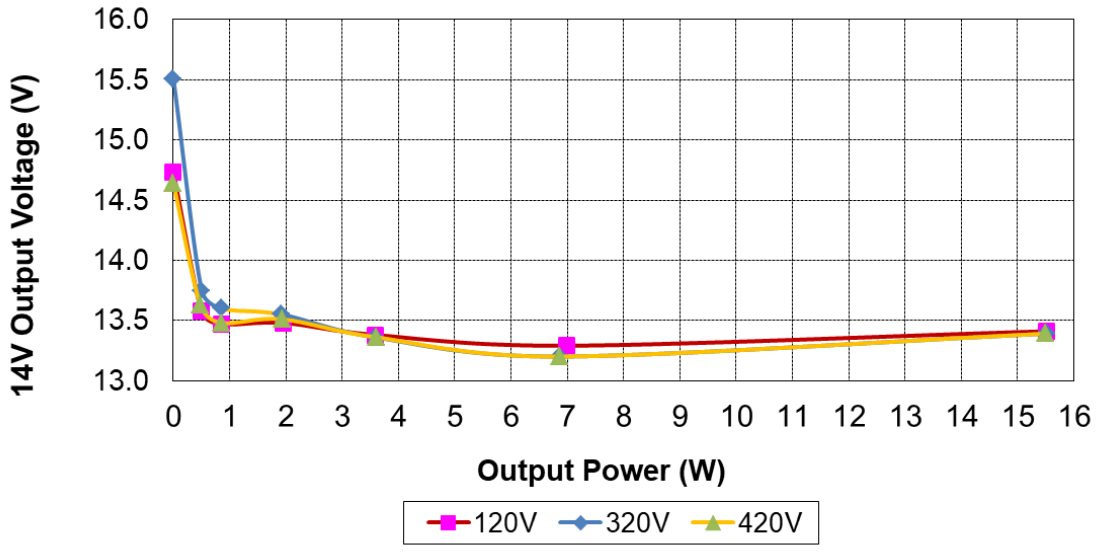
2.3 *Output Voltage Regulation*

The output voltage regulation graphs, for each output, are shown below.
All outputs have been loaded with the same percent, at the same time, of their nominal currents.

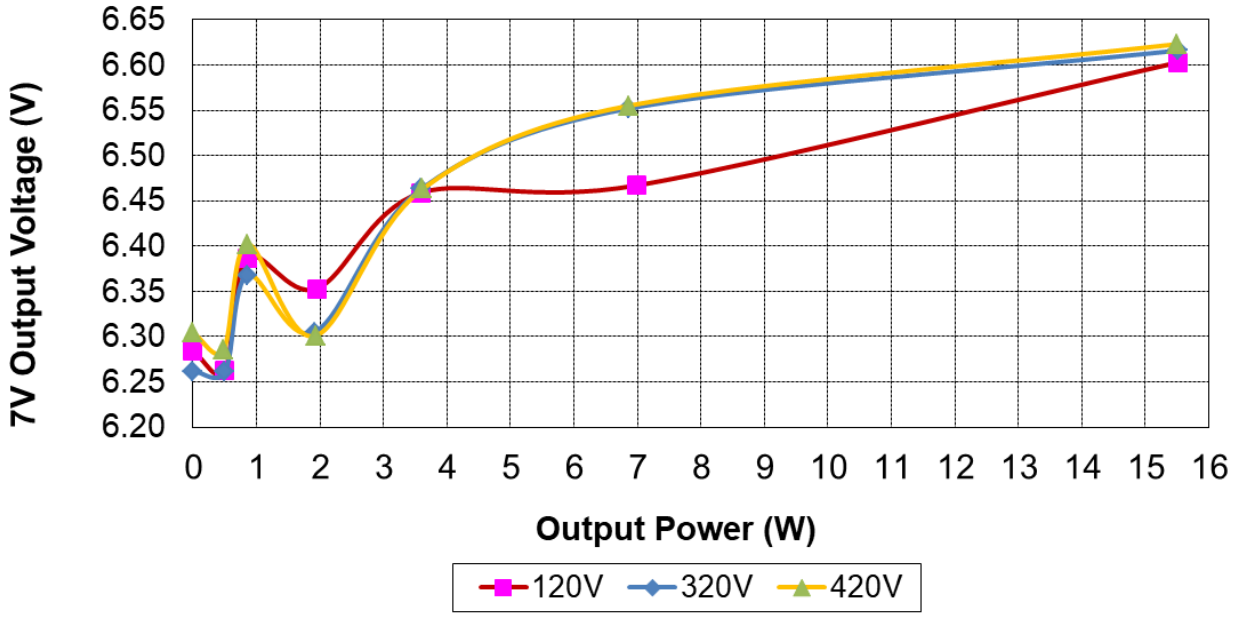
28 V output:



14 V output:



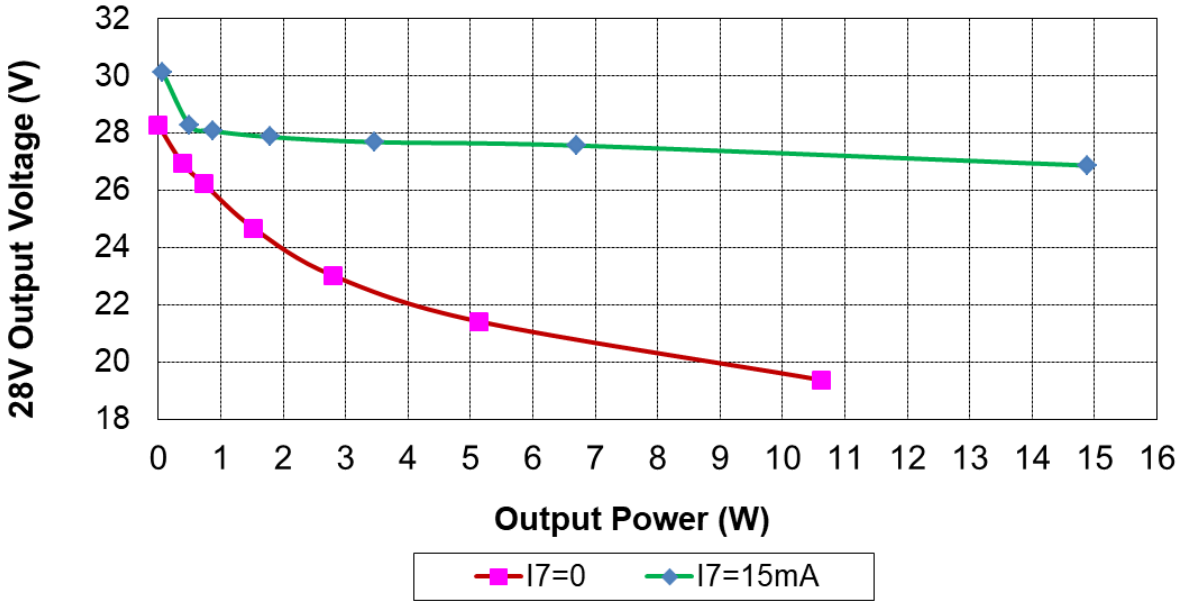
7 V output:



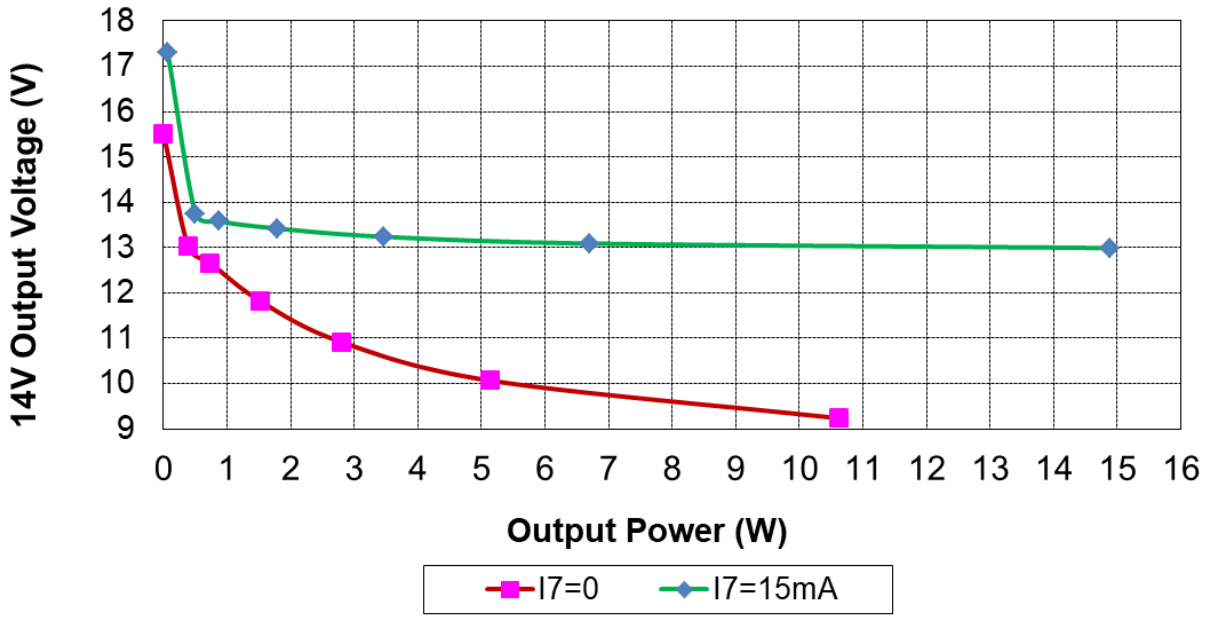
2.4 Cross Regulation

While the 7 V output of the converter was loaded at constant fixed current (0 and 15mA), the load current in the other two outputs have been varied from zero to nominal value. The cross-regulation performance has been measured by supplying the converter at 320 VDC. It is possible to see that if the 7 V output is loaded at least with 15 mA, all output voltages are well regulated.

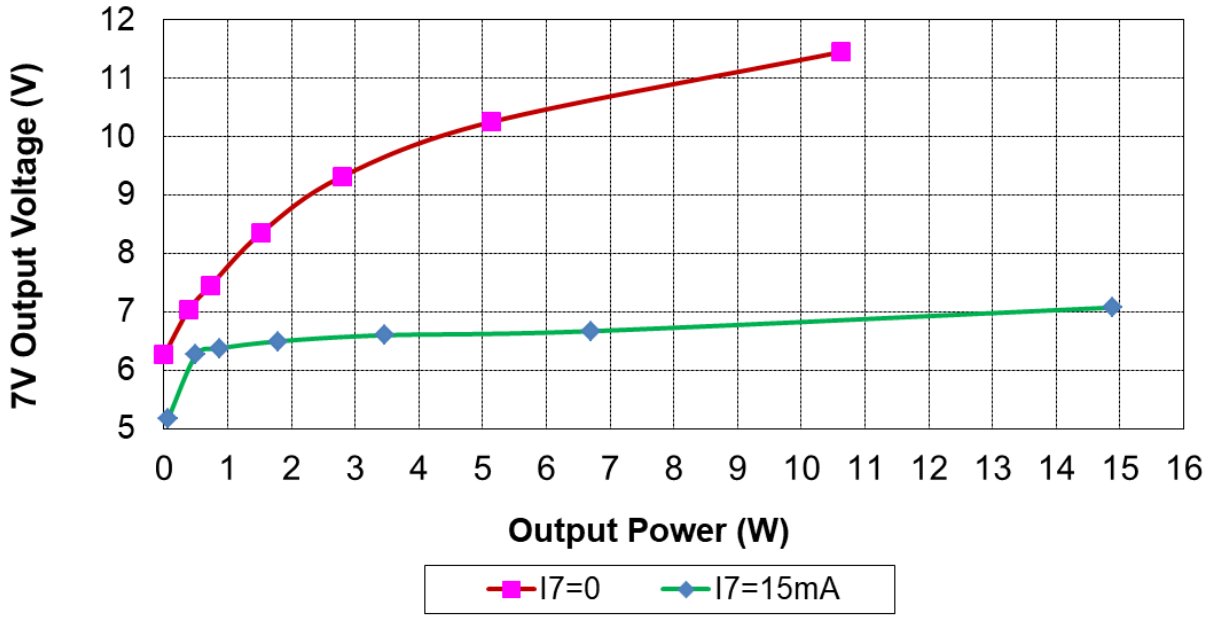
28 V output:



14 V output:



7 V output:



2.5 Dimensions

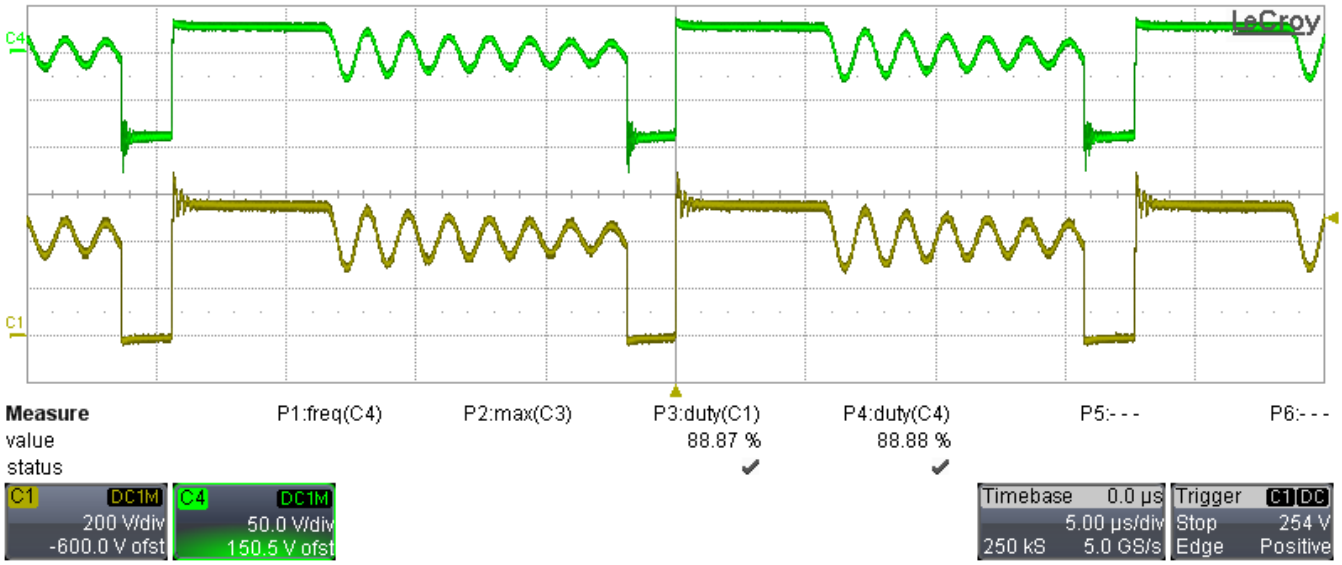
The board dimensions are 104.78 mm x 54.61 mm, height = 22 mm.

3 Waveforms

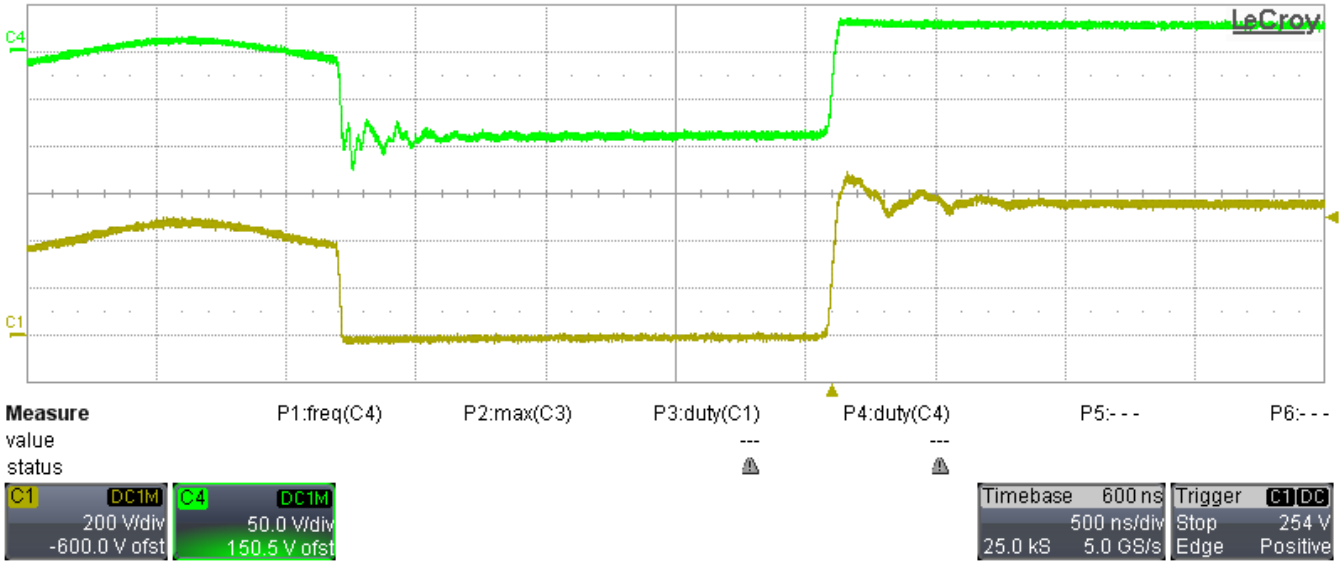
3.1 Switching

The switching waveforms have been measured by supplying the converter at 420 V input, in full load condition for each output.

C1: Drain-Source voltage of Q1 (200 V/div, 5 usec/div, no BWL)
C4: D1-Anode voltage vs secondary ground (50 V/div, no BWL)



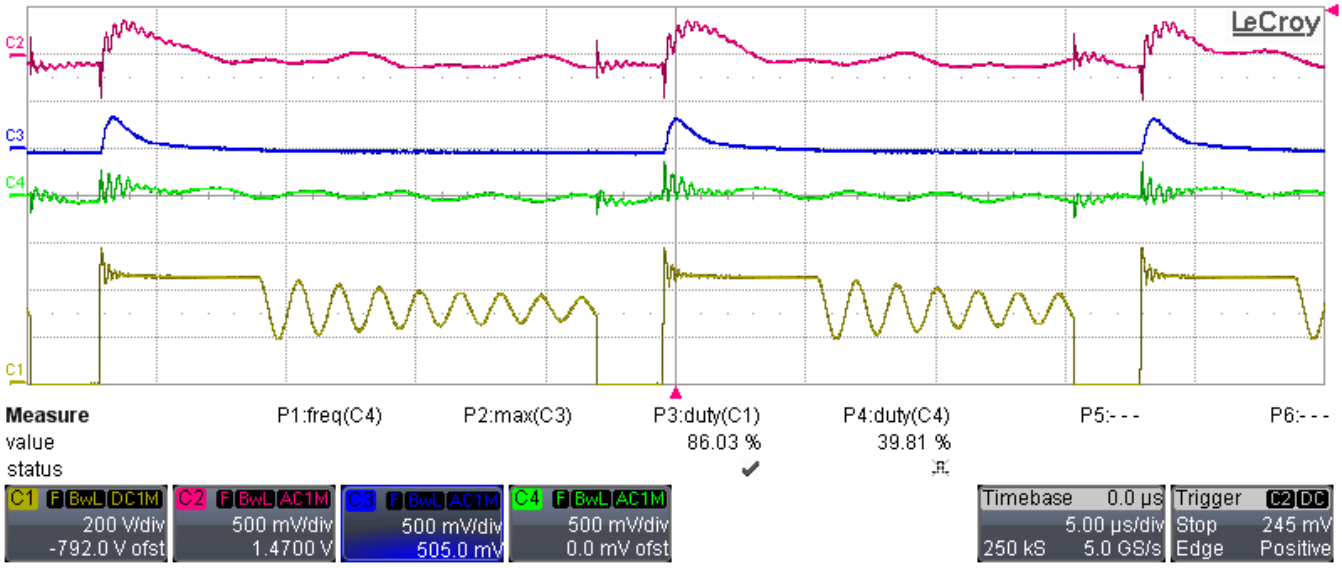
Same waveforms and setup as above, but with time division = 500 nsec /div.



3.2 Output Voltage Ripple and Q1 V_{DS} Voltage

The output voltage ripples, and the switch-node of Q1 have been measured by supplying the converter at 320 V, in full-load condition.

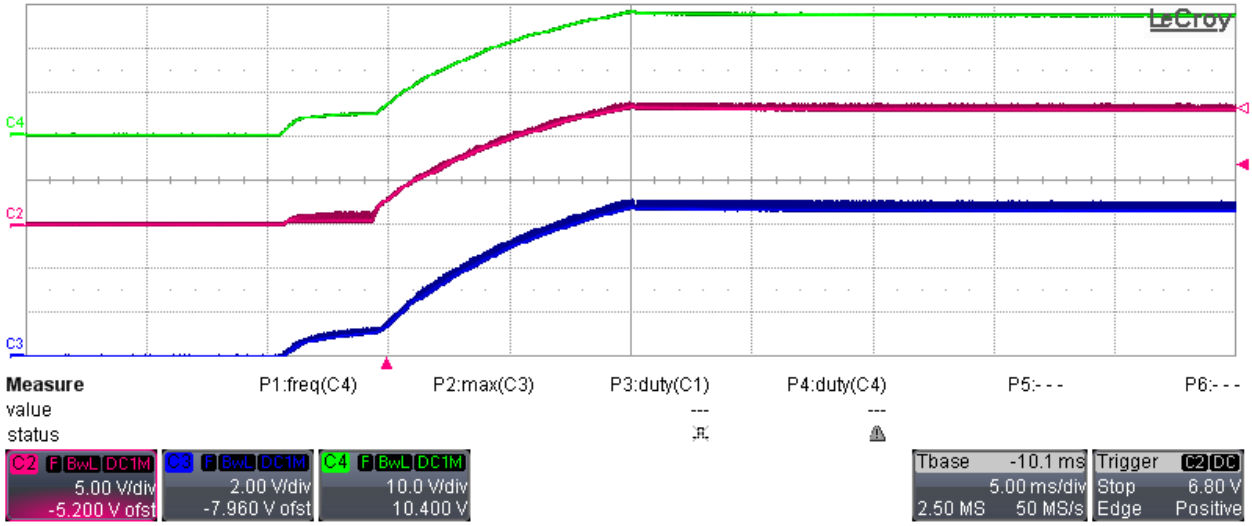
C1: Drain-Source voltage of Q1 (200 V/div, 5 usec/div, 200 MHz BWL)
C2: 14V output voltage (500 mV/div, AC coupling, 20 MHz BWL)
C3: 7V output voltage (500 mV/div, AC coupling, 20 MHz BWL)
C4: 28V output voltage (500 mV/div, AC coupling, 20 MHz BWL)



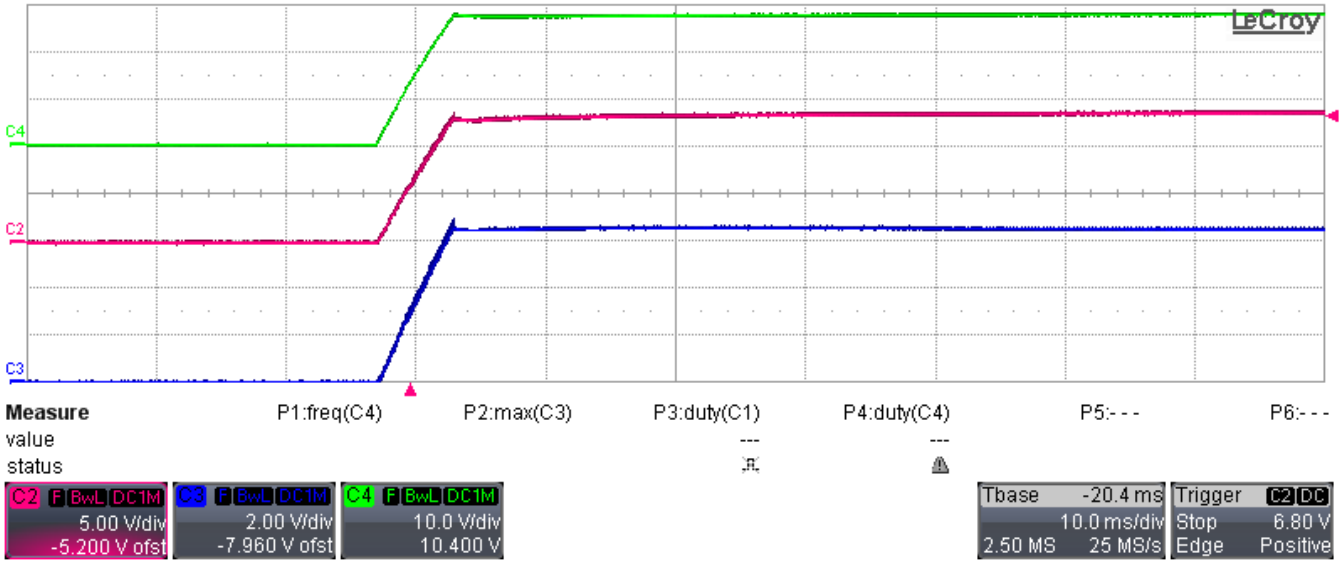
3.3 Startup

The behavior of the converter at startup, showing all output voltages, is shown below.

Conditions: Vin = 320 V, all outputs fully loaded; all waveforms taken with 20 MHz BWL
C2: 14V output voltage (5 V/div, 5 msec/div)
C3: 7V output voltage (2 V/div, DC coupling)
C4: 28V output voltage (10 V/div, DC coupling)



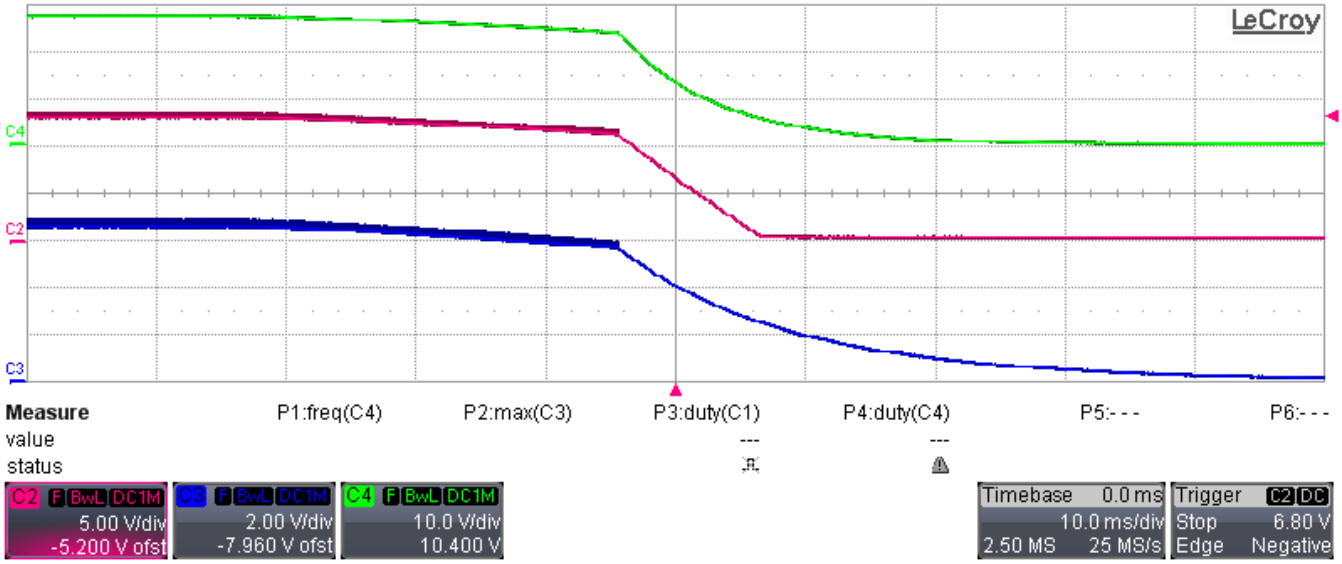
Conditions: Vin = 320 V, all outputs unloaded; all waveforms taken with 20 MHz BWL
C2: 14V output voltage (5 V/div, 10 msec/div)
C3: 7V output voltage (2 V/div, DC coupling)
C4: 28V output voltage (10 V/div, DC coupling)



3.4 Shut Down

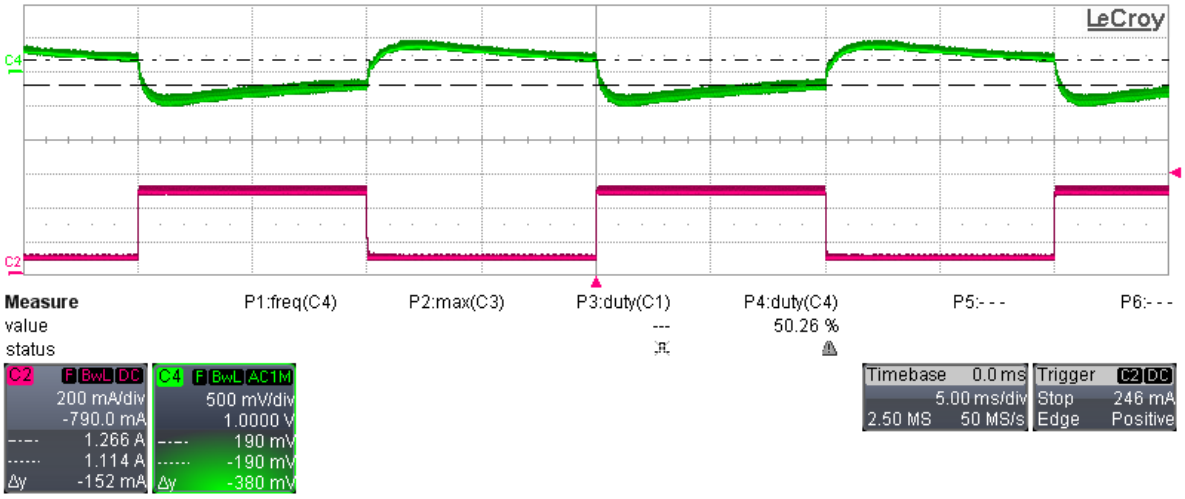
The behavior of the converter, during shut down, has been measured and shown below.

Conditions: Vin = 320 V, all outputs fully loaded; all waveforms taken with 20 MHz BWL
C2: 14V output voltage (5 V/div, 10 msec/div)
C3: 7V output voltage (2 V/div, DC coupling)
C4: 28V output voltage (10 V/div, DC coupling)



3.5 Load Transient Response

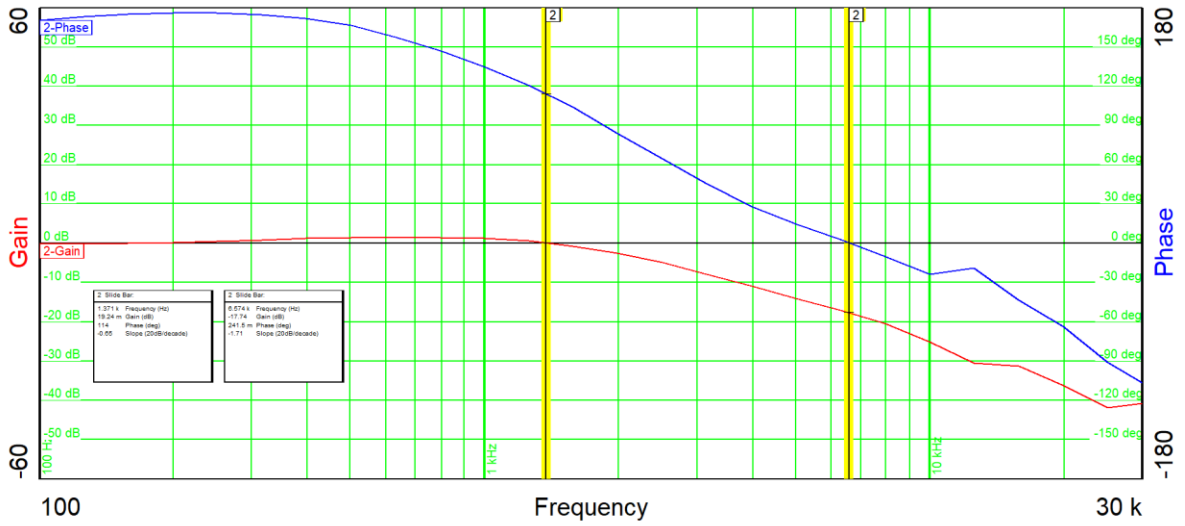
The load transient response of the converter has been measured by keeping constant (maximum) load to 7V and 14V outputs and by switching 28V output current between 100 mA and 500 mA.
Conditions: Vin = 320 V, load current on 7V = 50 mA, load current on 14V = 100 mA, 28V switched from 100 mA to 500 mA. BWL for all channels = 20 MHz.
C2: 28V output current (200 mA/div, 5 msec/div, DC coupling)
C4: 28V output voltage (500 mV/div, AC coupling)



4 Bode Plot

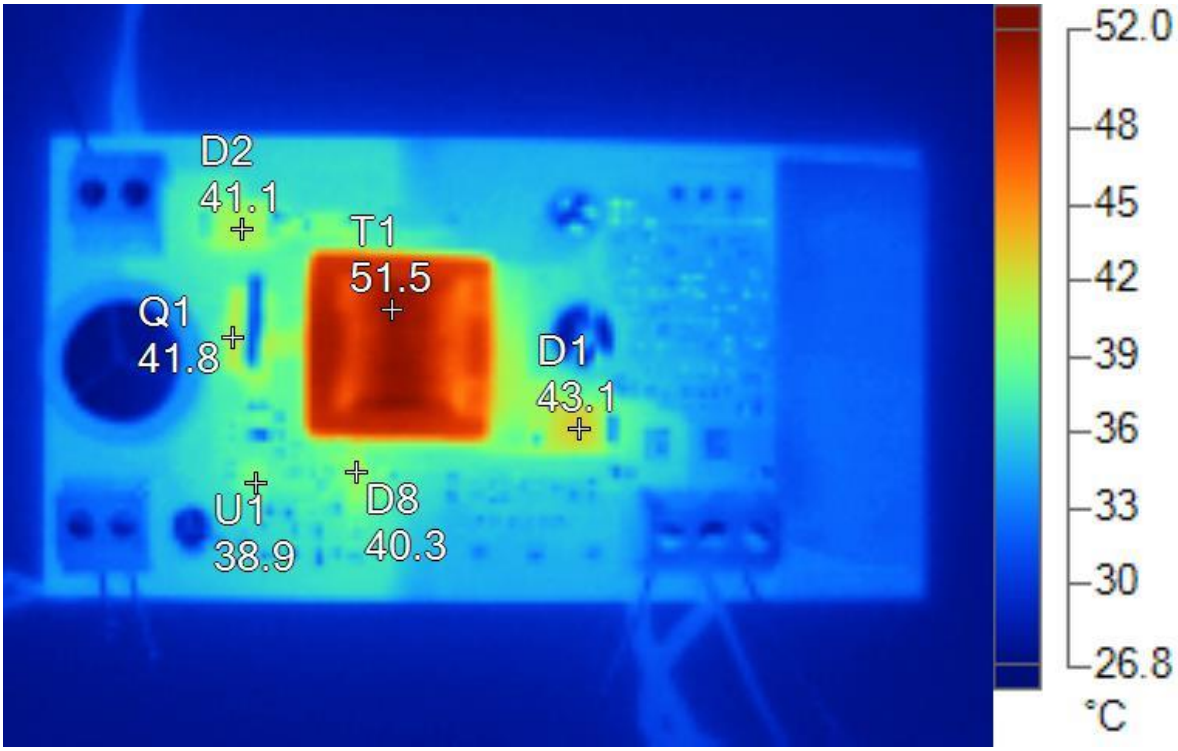
The following graph shows the bode plot of the converter, when supplied at 320 V and fully loaded. Here is the result, in terms of crossover frequency, phase margin and gain margin:

Parameter	Value
Crossover frequency:	1.371 KHz
Phase margin:	114 deg.
Gain margin:	17.74 dB



5 Thermal Image

The graph and table below show the thermal pictures of the converter supplied at 320 V. The images have been taken after the board was running for 30 minutes, placed horizontal on the bench, with all outputs fully loaded, at ambient temperature of 26 °C and in still air condition.



Main Image Markers

Name	Temperature	Emissivity	Background
T1	51.5°C	0.96	26 °C
D1	43.1°C	0.96	26 °C
Q1	41.8°C	0.96	26 °C
D2	41.1°C	0.96	26 °C
U1	38.9°C	0.96	26 °C
D8	40.3°C	0.96	26 °C

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