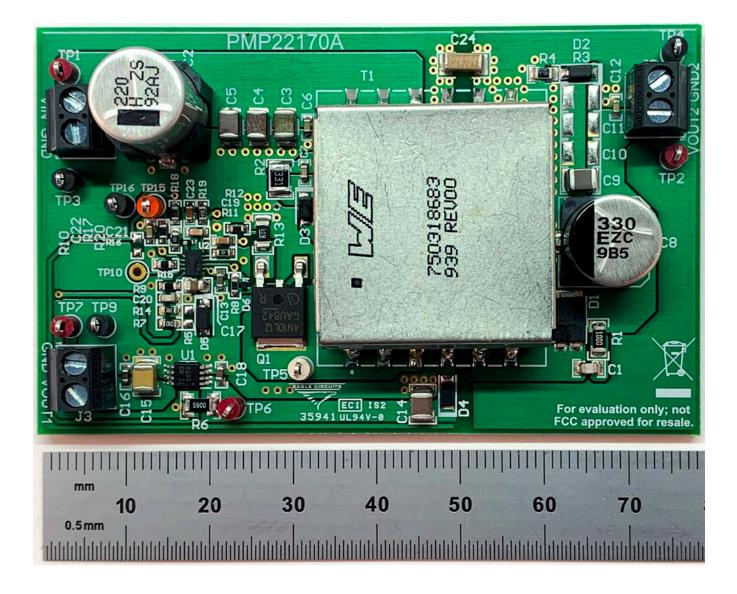
Test Report: PMP22170

Two Output Flyback Power Supply Reference Design for EV Motor/Generator Inverter Applications

Texas Instruments

Description

This flyback converter supplies a non-isolated 5 V/0.25 A regulated output and an isolated 10 V/1.5 A unregulated output voltage. It uses primary-side regulation to reduce component count and operates over a wide automotive input voltage range of 5 V - 40 V.





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1

1 Test Prerequisites

1.1 Voltage and Current Requirements

 Table 1.
 Voltage and Current Requirements

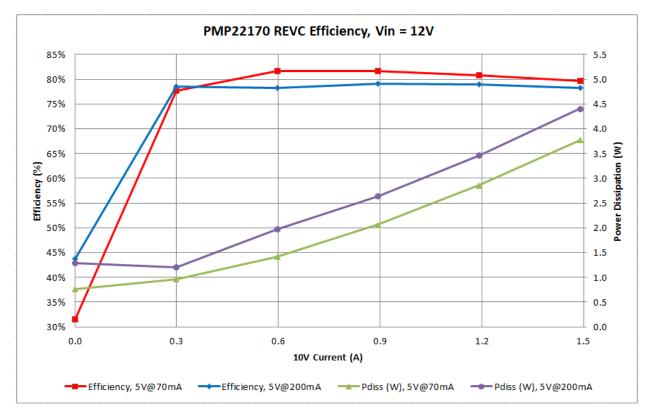
PARAMETER	SPECIFICATIONS				
	6 V – 18V, typical				
Input voltage range	(5 V – 40 V transient)				
	5 V/0.25 A, regulated, non-isolated				
Output voltage and current	10 V/0.8 A (typical)/1.5 A (peak), unregulated, isolated				
Switching frequency	300kHz				
Isolation	10 V/1.5 A, 700VDC (1 sec)				

1.2 Required Equipment

- Two electronic loads (15W and1.25W minimum) and/or power resistors (resistor decade boxes)
- Power supply capable of 50V and 5A (minimum)
- Oscilloscope and probes
- Digital Multimeters
- Stability measurement device (Venable or Bode100)



2 Testing and Results

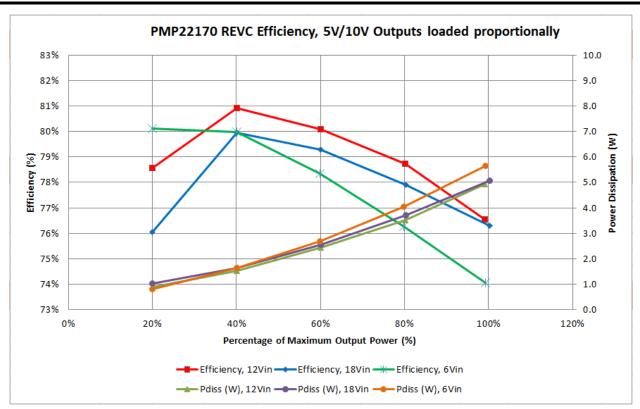


2.1 Efficiency and Power Dissipation Graphs

Vin	lin	Vout1	lout1	Vout2	lout2	Po	Pin	Efficiency, 5V@70mA	Pdiss (W), 5V@70mA
12.2204	0.0908	5.000	0.0699	10.853	0.0000	0.350	1.110	31.5%	0.760
12.1937	0.3541	5.000	0.0699	10.067	0.2984	3.354	4.318	77.7%	0.964
12.1659	0.6328	5.000	0.0699	9.954	0.5965	6.287	7.699	81.7%	1.412
12.1363	0.9261	5.000	0.0699	9.870	0.8944	9.177	11.239	81.7%	2.062
12.1070	1.2296	5.000	0.0699	9.795	1.1924	12.029	14.887	80.8%	2.858
12.0768	1.5418	5.000	0.0699	9.720	1.4908	14.840	18.620	79.7%	3.780
								Efficiency,	Pdiss (W),
Vin	lin	Vout1	lout1	Vout2	lout2	Po	Pin	5V@200mA	5V@200mA
12.2110	0.1880	4.998	0.2011	11.357	0.0000	1.005	2.296	43.8%	1.291
12.1847	0.4561	4.998	0.2011	11.248	0.2984	4.362	5.557	78.5%	1.196
12.1574	0.7414	4.999	0.2009	10.134	0.5965	7.049	9.013	78.2%	1.964
12.1281	1.0420	4.999	0.2008	10.060	0.8944	10.001	12.637	79.1%	2.636
12.0994	1.3537	4.998	0.2009	9.996	1.1924	12.923	16.379	78.9%	3.456
12.0696	1.6749	4.998	0.2008	9.933	1.4905	15.809	20.215	78.2%	4.406

The above graph displays the efficiency and power dissipation of the converter with the 5V output loaded to either 70mA or 200mA as the 10V load is varied. The input voltage was set to 12V.





Vin	lin	Vout1	lout1	Vout2	lout2	Po	Pin	Efficiency, 12Vin	Pdiss (W), 12Vin	Percentage of Maximum Pout
12.1476	0.3408	5.000	0.0501	10.014	0.2998	3.253	4.140	78.6%	0.887	20%
12.0237	0.6691	5.000	0.0992	10.011	0.6008	6.511	8.045	80.9%	1.534	40%
12.0949	1.0076	4.999	0.1494	10.009	0.9005	9.760	12.187	80.1%	2.427	60%
12.0187	1.3771	4.999	0.2032	10.002	1.2014	13.032	16.551	78.7%	3.519	80%
12.0371	1.7475	4.998	0.2552	9.886	1.4995	16.100	21.035	76.5%	4.935	99%
Vin	lin	Vout1	lout1	Vout2	lout2	Po	Pin	Efficiency, 18Vin	Pdiss (W), 18Vin	Percentage of Maximum Pout
18.0711	0.2367	5.000	0.0501	10.011	0.2999	3.253	4.277	76.0%	1.025	20%
18.0069	0.4524	5.000	0.0992	10.014	0.6008	6.512	8.146	79.9%	1.634	40%
18.0392	0.6827	4.999	0.1494	10.017	0.9002	9.764	12.315	79.3%	2.551	60%
18.0187	0.9296	4.998	0.2031	10.016	1.2013	13.047	16.750	77.9%	3.703	80%
18.0480	1.1829	4.997	0.2552	10.009	1.4997	16.286	21.349	76.3%	5.063	100%
						_		Efficiency,	Pdiss (W),	Percentage of
Vin	lin	Vout1	lout1	Vout2	lout2	Po	Pin	6Vin	6Vin	Maximum Pout
6.0059	0.6762	5.001	0.0501	10.017	0.2998	3.254	4.061	80.1%	0.808	20%
6.0488	1.3452	5.000	0.0992	10.006	0.6008	6.508	8.137	80.0%	1.629	40%
6.0457	2.0550	4.999	0.1494	9.981	0.9002	9.732	12.424	78.3%	2.692	60%
6.0370	2.8160	4.998	0.2031	9.948	1.2014	12.967	17.000	76.3%	4.034	80%
6.0262	3.6130	4.997	0.2550	9.903	1.4997	16.126	21.773	74.1%	5.647	99%

The above graph displays the efficiency and power dissipation of the converter with the 5V and 10V outputs loaded proportionally. The input voltage was set to 6V, 12V or 18V.

4



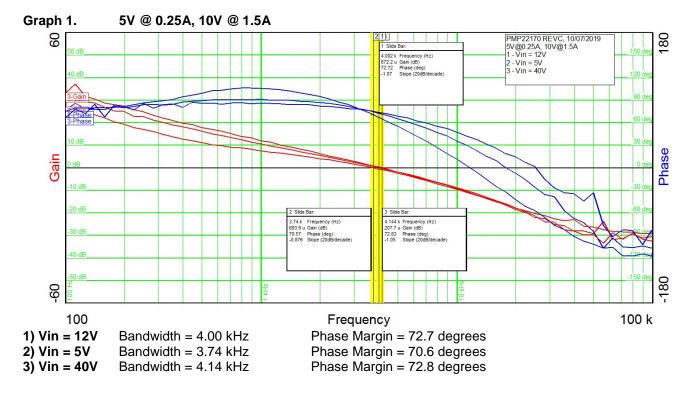
2.2 Cross Regulation

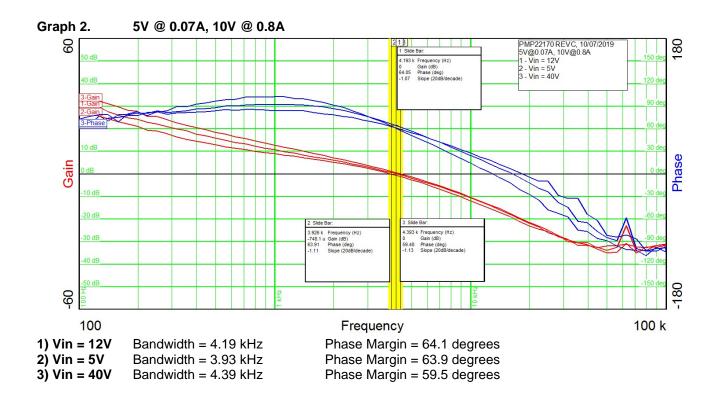
		Ve	oltage Regulatio	on Data				
VIN (V)	I IN(A)	VREG (V)	VOUT 5V (V)	IOUT 5V (A)	VOUT 10V (V)	IOUT 10V (A)		
No Load Conditions								
5.2087	0.0565	7.057	5.002	0.0000	10.3070	0.0000		
12.2261	0.0348	7.057	5.001	0.0000	10.3200	0.0000		
40.0380	0.0117	7.057	5.001	0.0000	10.4440	0.0000		
			Typical Load Cond	itions				
5.2087	1.9906	7.059	5.000	0.0700	9.8370	0.8008		
5.1370	2.3310	7.059	4.999	0.2015	10.1040	0.8006		
5.1820	3.7650	7.058	5.000	0.0700	9.4777	1.5011		
5.1752	4.1600	7.058	4.998	0.2014	9.7800	1.5011		
12.0550	0.8418	7.059	5.000	0.0700	9.9052	0.8006		
12.0643	0.9542	7.059	4.999	0.2013	10.0900	0.8008		
12.0406	1.5694	7.058	4.999	0.0699	9.7170	1.5011		
12.0779	1.6967	7.058	4.998	0.2015	9.9280	1.5009		
40.0640	0.2751	7.058	5.000	0.0700	9.9315	0.8006		
40.0080	0.9452	7.059	4.999	0.2011	10.0820	0.8007		
40.0510	1.5694	7.059	4.999	0.0699	9.8390	1.5011		
40.1060	1.6967	7.058	4.997	0.2013	10.0030	1.5010		
			Full Load Condit	ions				
5.1530	4.3130	7.057	4.998	0.2470	9.8500	1.5010		
12.0609	1.7425	7.057	4.998	0.2490	9.9820	1.5010		
40.0070	0.5833	7.055	4.997	0.2470	10.0310	1.5010		
			Cross Loading	5				
5.2000	3.1770	7.057	5.002	0.0000	8.3310	1.5010		
5.2165	0.5019	7.057	4.998	0.2470	11.5150	0.0000		
12.0935	1.4124	7.057	5.002	0.0000	9.0467	1.5010		
12.2073	0.2183	7.057	4.998	0.2490	11.5030	0.0000		
40.0180	0.4970	7.056	5.001	0.0000	9.4770	1.5010		
40.0340	0.0840	7.056	4.998	0.2470	11.5320	0.0000		

This table shows the voltage regulation of the 5V and 10V outputs under various load conditions.



2.3 Loop Gain

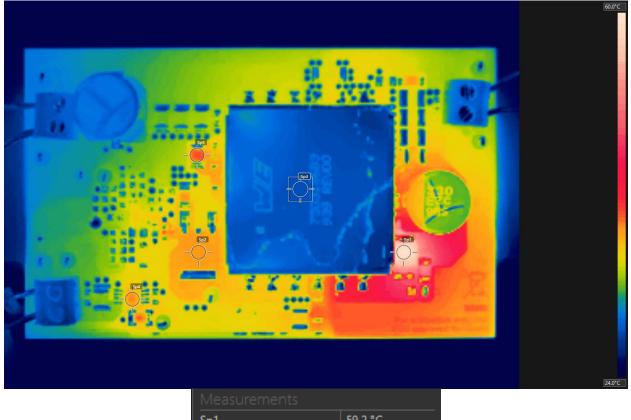




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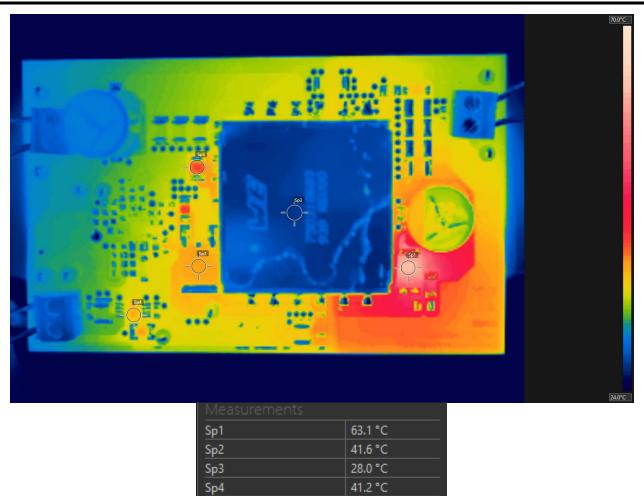
2.4 Thermal Images



59.2 °C
39.8 °C
29.3 °C
40.4 °C
41.6 °C

This thermal image shows the operating temperature of the board with 12V input and 5V@0.07A and 10V@0.8A. The image was captured at room temperature after operating for 30 minutes.



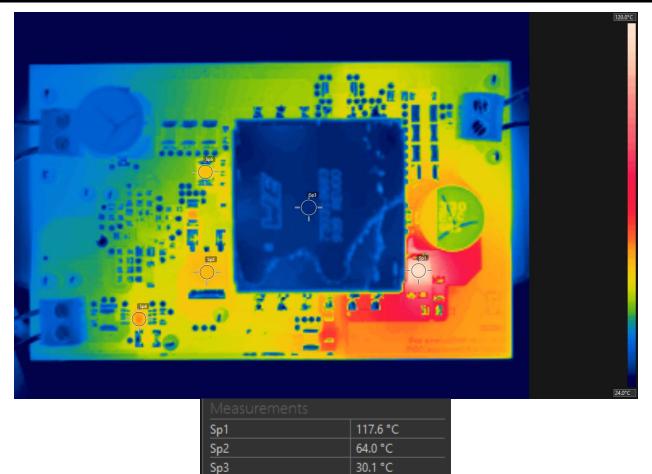


This thermal image shows the operating temperature of the board with 6V input and 5V@0.07A and 10V@0.8A. The image was captured at room temperature after operating for 30 minutes.

44.6 °C

Sp5





This thermal image shows the operating temperature of the board with 12V input and 5V@0.25A and 10V@1.5A. The image was captured at room temperature after operating for 30 minutes.

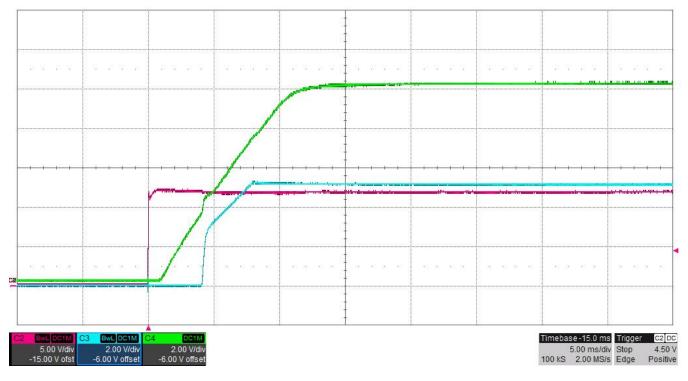
Sp4 Sp5 69.2 °C

63.3 °C

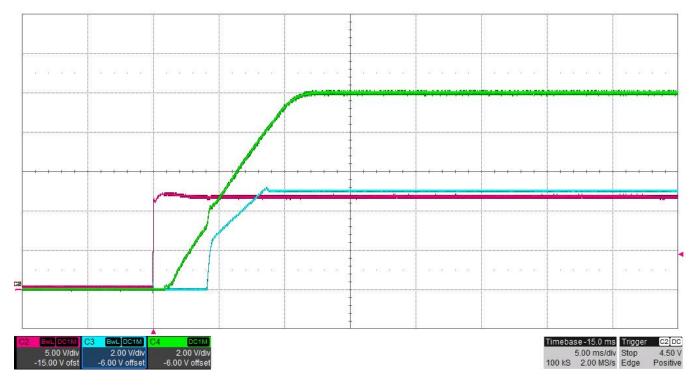


Waveforms 3

3.1 Startup Sequence



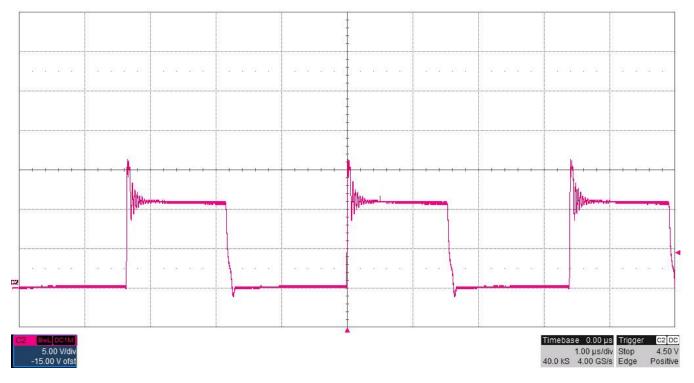
Start-up sequence for Vin = 12V (Red), 5V @ 0A (Blue), 10V @ 0A (Green)



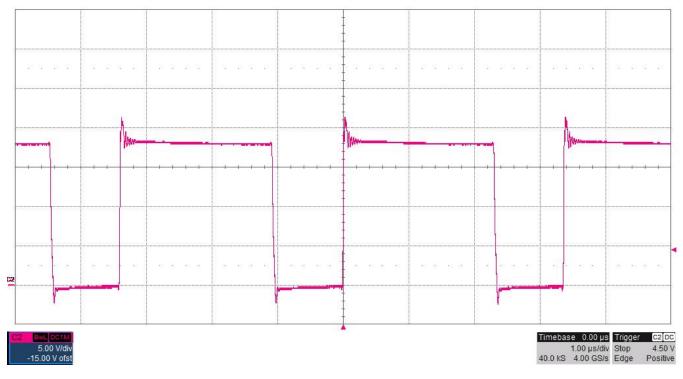
Start-up sequence for Vin = 12V (Red), 5V @ 0.25A (Blue), 10V @ 1.5A (Green)



3.2 FET Switch Node

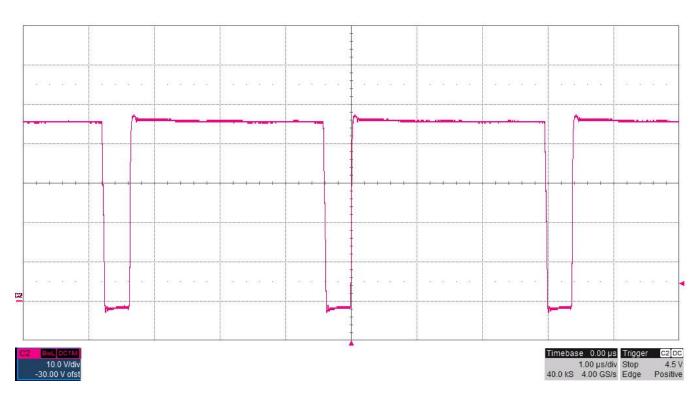


Switch node of FET with Vin = 5V, 5V @ 0.25A, 10V @ 1.5A

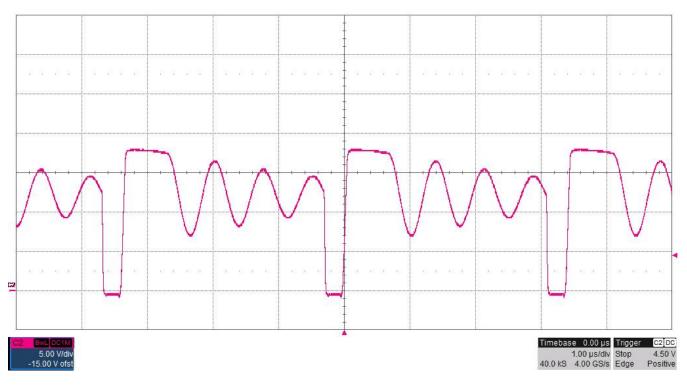


Switch node of FET with Vin = 12V, 5V @ 0.25A, 10V @ 1.5A



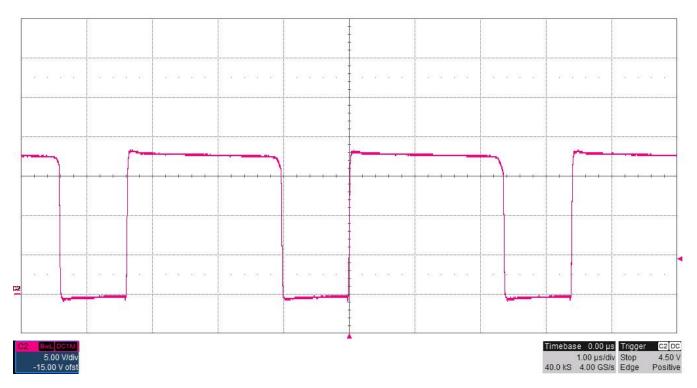


Switch node of FET with Vin = 40V, 5V @ 0.25A, 10V @ 1.5A

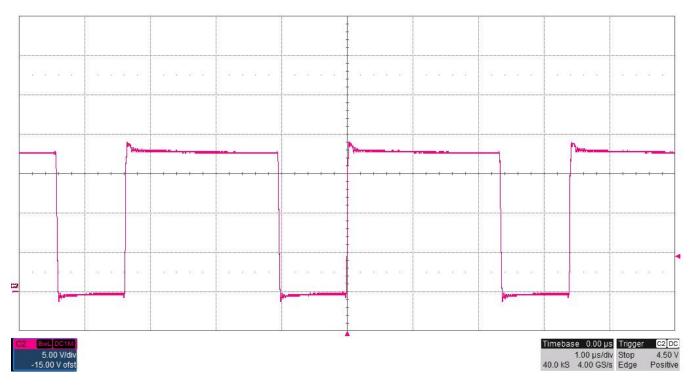


Switch node of FET with Vin = 12V, 5V @ 0A, 10V @ 0A (DCM operation)





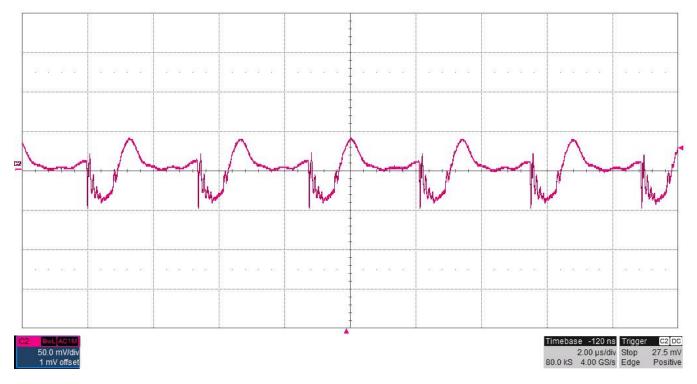
Switch node of FET with Vin = 12V, 5V @ 0.05A, 10V @ 0.22A (DCM operation threshold)



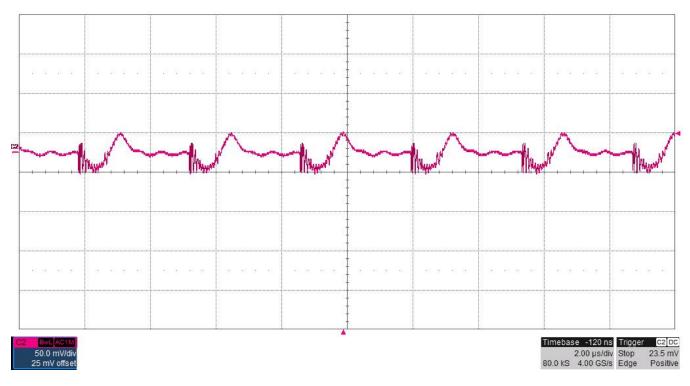
Switch node of FET with Vin = 12V, 5V @ 0.1A, 10V @ 0.8A (typical load)



3.3 Output Voltage Ripple

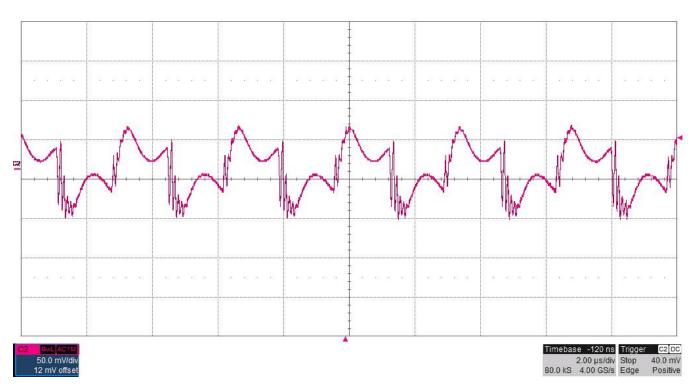


¹⁰V ripple voltage with Vin = 18V, 5V @ 0.25A, 10V @ 1.5A, Bandwidth = 20MHz

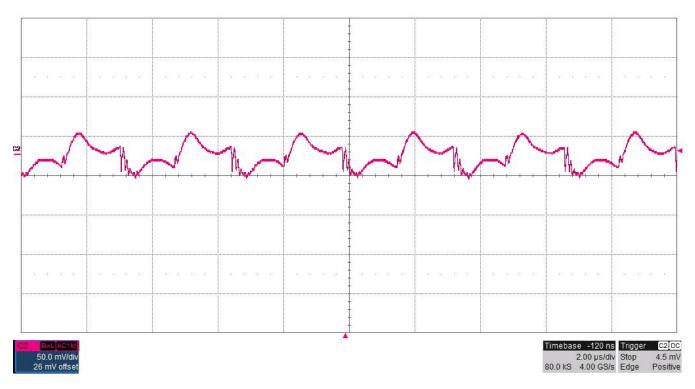


10V ripple voltage with Vin = 18V, 5V @ 0.07A, 10V @ 0.8A, Bandwidth = 20MHz



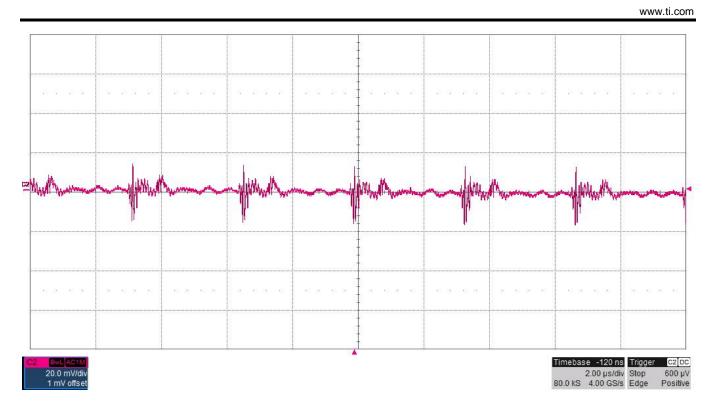


10V ripple voltage with Vin = 6V, 5V @ 0.25A, 10V @ 1.5A, Bandwidth = 20MHz

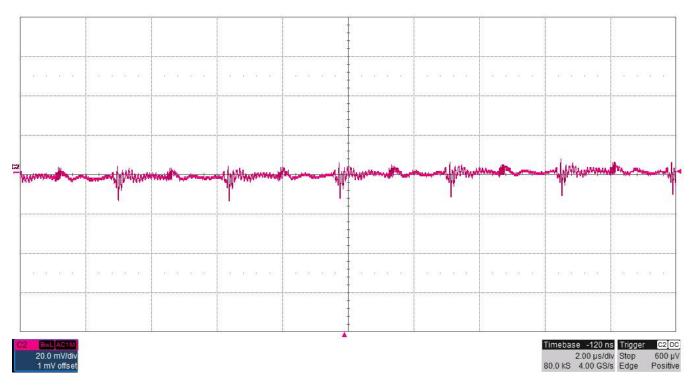


10V ripple voltage with Vin = 6V, 5V @ 0.07A, 10V @ 0.8A, Bandwidth = 20MHz





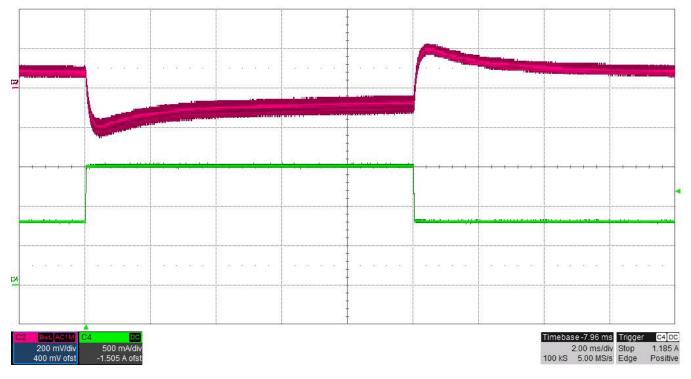
5V ripple voltage with Vin = 18V, 5V @ 0.25A, 10V @ 1.5A, Bandwidth = 20MHz



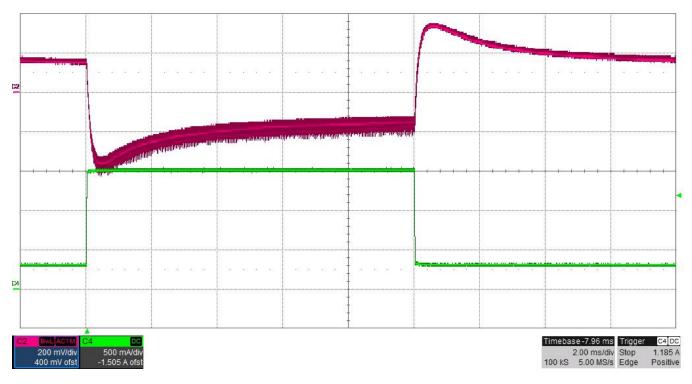
5V ripple voltage with Vin = 6V, 5V @ 0.25A, 10V @ 1.5A, Bandwidth = 20MHz



3.4 Load Transients

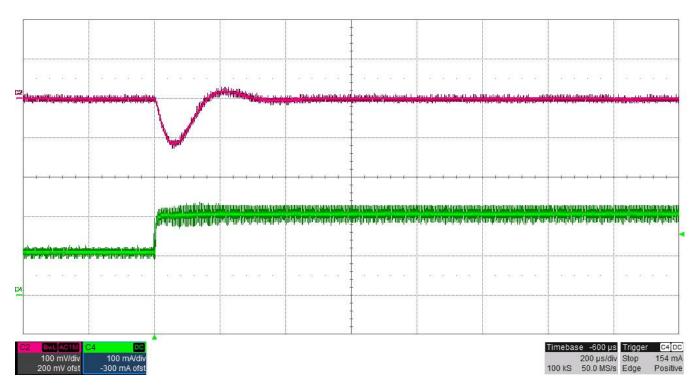


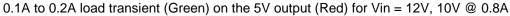
0.8A to 1.5A load transient (Green) on the 10V output (Red) for Vin = 12V, 5V @ 0.25A

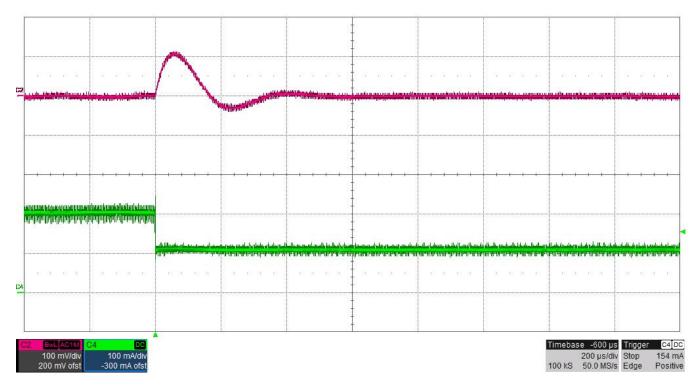


0.3A to 1.5A load transient (Green) on the 10V output (Red) for Vin = 12V, 5V @ 0.25A









0.2A to 0.1A load transient (Green) on the 5V output (Red) for Vin = 12V, 10V @ 0.8A

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