TI Designs

Parallel Camera Interface for Sitara Processors Design Guide

TEXAS INSTRUMENTS

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TI Designs provide the foundation, including methodology, testing, and design file, for quickly evaluating and customizing your system. TI Designs help accelerate your time to market.

Design Description

This camera interface design connects to a 10-bit parallel interface to the AM335x general purpose memory controller (GPMC) 16-bit multiplexed address/data bus. This design consumes roughly 150mW less power than typical USB solutions, and is ideal for applications like portable data terminals, ruggedized handhelds, portable consumer, industrial handhelds and others. The reference design is based on the QuickLogic 3.1 MP Camera Sensor (using an Aptina 3.1 MP sensor) connected to a camera expansion board. Together, they connect to the BeagleBone platform. The BeagleBone and the QuickLogic 3.1 MP camera add-on board are available for purchase.

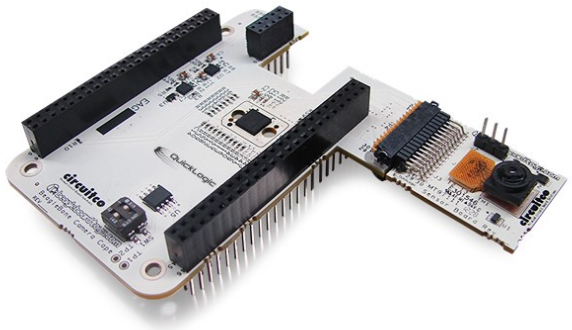
Design Features

- Supports up to 5MP camera at 10fps with DMA
- Up to 30 frames per second (fps) at VGA (640 x 480) resolution
- Reduces system power consumption up to 150mW
- No software effort required for OEM
- 6x6mm, non-HDI rules package
- This is an example sub-system design that includes schematics, BOM, Gerbers and other design files.

Design Resources

QuickLogic	More information on QuickLogic
BeagleBone	More information on BeagleBone
QuickLogic Camera Board	User Guide, Design Files, Software
System Reference Manual	Camera Board Reference Manual
BeagleBoardToys	Buy Camera Board

TI E2E™ Community — Ask The Experts



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