## PMP10555 Test Report

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1) Block Diagram

## FPGA Power Supply for Mobile Radio Basestation



Figure 1. Block Diagram

## 2) Board Photos



Figure 2. Board Photo Top


Figure 3. Board Photo Bottom

## 3) Startup Waveforms

Two LM3880's are used for power sequencing as shown in figures 4, 5, and 6. The power up sequence is in the following order: VCCINT, MGTAVCC, MGTAVTT, VCCAUX, VCCO_PSDDR, MGTVCCAUX, VCCO_PSIO. The power down sequence is the reverse order of power up.


Ch.1: VIN
Ch.2: VCCINT
Ch.3: MGTAVCC
Ch.4: MGTAVTT
Figure 4. Startup Waveform


Ch.1: VIN
Ch.2: VCCAUX
Ch.3: VCCO_PSDDR
Ch.4: MGTVCCAUX

Figure 5. Startup Waveform


Ch.1: VIN
Ch.2: VCCO_PSIO

Figure 6. Startup Waveform

## 4) Efficiency

The efficiency of the converters is shown in the figures below. The input voltage is set to 12 V .


Figure 7. VIN $=12 \mathrm{~V}$, VOUT $=0.9 \mathrm{~V}$; VCCINT Efficiency


Figure 8. VIN $=12 \mathrm{~V}$, VOUT $=0.9 \mathrm{~V}$; MGTAVCC Efficiency


Figure 9. VIN = 12V, VOUT = 1.2V; MGTAVTT Efficiency


Figure 10. VIN = 12V, VOUT = 1.8V; VCCAUX Efficiency


Figure 11. VIN = 12V, VOUT = 1.35V; VCCO_PSDDR Efficiency


Figure 12. VIN = 12V, VOUT = 1.8V; MGTVCCAUX Efficiency


Figure 13. VIN $=12 \mathrm{~V}$, VOUT $=3.3 \mathrm{~V}$; VCCO_PSIO Efficiency

## 5) Load Regulation

The images below show the output load regulation. The input voltage is 12 V .


Figure 14. VIN $=12 \mathrm{~V}$, VCCINT Load Regulation


Figure 15. VIN = 12V, MGTAVCC Load Regulation


Figure 16. VIN = 12V, MGTAVTT Load Regulation


Figure 17. VIN = 12V, VCCAUX Load Regulation


Figure 18. VIN = 12V, VCCO_PSDDR Load Regulation


Figure 19. VIN = 12V, MGTVCCAUX Load Regulation


Figure 20. VIN $=12 \mathrm{~V}, \mathrm{VCCO}$ PSIO Load Regulation

## 6) Output Voltage Ripple

The images below shows the output voltage ripple when load is fully applied. The input voltage is 12 V .


Figure 21. VIN = 12V, VCCINT Output Ripple @ IOUT = 20A


Figure 22. VIN = 12V, MGTAVCC Output Ripple @ IOUT=2A


Figure 23. VIN = 12V, MGTAVTT Output Ripple @ IOUT = 1A


Figure 24. VIN $=12 \mathrm{~V}, \mathrm{VCCAUX}$ Output Ripple @ IOUT $=3 \mathrm{~A}$


Figure 25. VIN = 12V, VCCO_PSDDR Output Ripple @ IOUT = 2A


Figure 26. VIN = 12V, MGTVCCAUX Output Ripple @ IOUT $=2.5 \mathrm{~A}$


Figure 27. VIN = 12V, VCCO_PSIO Output Ripple @ IOUT $=500 \mathrm{~mA}$

## 7) Load Transients

The transient response of the converters is shown below. The input voltage is 12 V . The output current is pulsed from 0 to $50 \%$ load.


Figure 28. VIN = 12V, VCCINT Load Transient


Figure 29. VIN = 12V, MGTAVCC Load Transient


Figure 30. VIN = 12V, MGTAVTT Load Transient


Figure 31. VIN = 12V, VCCAUX Load Transient


Figure 32. VIN = 12V, VCCO_PSDDR Load Transient


Figure 33. VIN = 12V, MGTVCCAUX Load Transient


Figure 34. VIN = 12V, VCCO_PSIO Load Transient

## 8) Thermal Image

Thermal images at full load of each device are shown below, the remaining rails are not drawing any current during these tests unless otherwise noted. The input voltage is 12 V .


Figure 35. VIN = 12V, VCCINT Thermal Image @ Full Load


Figure 36. VIN = 12V, MGTAVCC Thermal Image @ Full Load


Figure 37. VIN = 12V, MGTAVTT Thermal Image @ Full Load


Figure 38. VIN = 12V, VCCAUX Thermal Image @ Full Load


Figure 39. VIN = 12V, VCCO_PSDDR Thermal Image @ Full Load


Figure 40. VIN = 12V, MGTVCCAUX Thermal Image @ Full Load


Figure 41. VIN = 12V, VCCO_PSIO Thermal Image @ Full Load



Figure 43. VIN = 12V,
MGTVCCAUX (2.5A), MGTAVTT (1A), VCCO_PSIO (0.5A) Thermal Image @ Full Load

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