PMP10927 Rev. A Test Results

1. PHOTO OF THE PROTOTYPE:

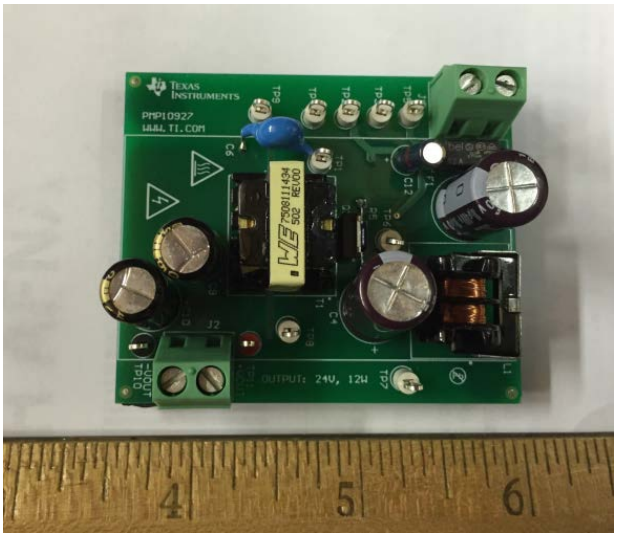

Figure 1. Front image of tested board

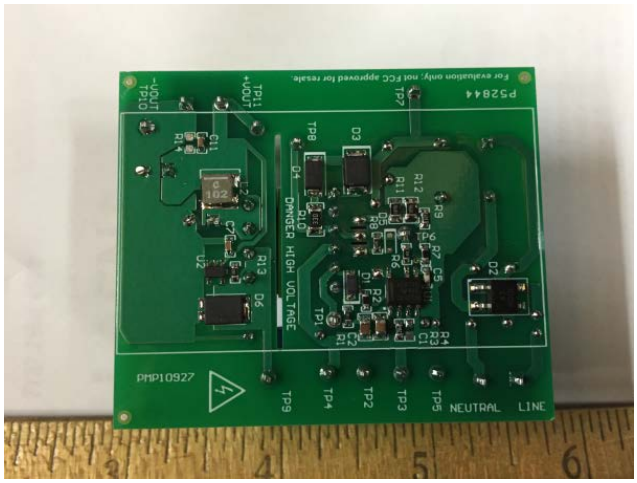

Figure 2. Back image of tested board

The PMP10927 is a 12-W off-line discontinuous mode (DCM) flyback converter that provides constant-voltage (CV) and constant-current (CC) output regulation without the use of an optical coupler. The controller uses primary side regulation (PSR) and detects a wake-up signal from the UCC24650 secondary-side voltage-droop monitor for improved transient response to large load steps. This reference design shows how the UCC28730 can provide ultra-low standby power without sacrificing start-up time or output transient response with an internal 700-V start-up switch, dynamically controlled operating states, and a tailored modulation profile. The UCC28730 uses frequency modulation, peak primary current modulation, valley switching and valley skipping in its control algorithm in order to maximize efficiency over the entire operating range. The PMP10927 reference design exceeds Level VI and CoC Tier 2 specifications , effective 2016, for no-load stand-by power, average efficiency, and 10% load effeiciency for Energy-Efficiency Criteria for Active Mode (excluding low voltage external power supplies). **Note that this reference design is not an orderable device from TI, but shows the performance of a UCC28730/UCC24650 in a constant voltage/ constant current controller in a typical 12-W adapter application.**

2. Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Input Characteristics					
Voltage range, V_{IN}		85	115/230	265	V_{RMS}
Maximum input current	$V_{IN} = V_{INmin}$, $I_{OUT} = I_{OUTmax}$			0.290	A_{RMS}
Line frequency		47	60/50	63	Hz
No-load power consumption	$V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = 0A$			5	mW
Output Characteristics					
Output voltage, CV mode, V_{OUT}	$V_{INmin} \le V_{IN} \le V_{INmax}$, $0A \le I_{OUT} \le I_{OUTmax}$	22.8	24	25.2	V
Output load current, CV mode, I_{OUTmax}	$V_{INmin} \le V_{IN} \le V_{INmax}$	0.475	0.50	0.525	A
Output voltage regulation	Line Regulation: $V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = I_{OUTmax}$			5	%
	Load Regulation: $0A \le I_{OUT} \le I_{OUTmax}$			5	%
Output voltage ripple	$V_{INmin} \le V_{IN} \le V_{INmax}$, $0A \le I_{OUT} \le I_{OUTmax}$			80	mVpp
Output over current, I_{OCC}	$V_{INmin} \le V_{IN} \le V_{INmax}$			0.58	A
Minimum output voltage, CC mode	$V_{INmin} \le V_{IN} \le V_{INmax}$, $I_{OUT} = I_{OCC}$		9		V
Turn-off voltage	$I_{OUT} = I_{OUTmax}$		65		V_{RMS}
	$I_{OUT} = 10\%\ I_{OUTmax}$		26		
Systems Characteristics					
Switching frequency, f_{SW}		0.200		50	kHz
Average efficiency	25%, 50%, 75%, 100% load average	83.26			%
10% efficiency	10% load	73.26			%
Operating temperature			25		ºC

3. Efficiency

V_{IN} V_{RMS}	P_{IN} W	V_{OUT} V	I_{OUT} A	P_{OUT}	EFFFICIENCY
85V, 60Hz	1.410	24.090	0.0501	10%	0.8559
	3.463	24.083	0.125	25%	0.8692
	7.104	24.102	0.251	50%	0.8515
	10.853	24.134	0.377	75%	0.8383
	14.526	24.166	0.503	100%	0.8368
115V, 60Hz	1.4063	24.101	0.0501	10%	0.8586
	3.452	24.067	0.125	25%	0.8714
	6.938	24.095	0.249	50%	0.8647
	10.633	24.129	0.377	75%	0.8555
	14.187	24.167	0.503	100%	0.8568
230V, 50Hz	1.4571	24.103	0.0501	10%	0.8287
	3.494	24.069	0.125	25%	0.8610
	6.919	24.099	0.249	50%	0.8672
	10.495	24.128	0.377	75%	0.8667
	14.035	24.171	0.503	100%	0.8662
265V, 50Hz	1.4836	24.100	0.0501	10%	0.8138
	3.528	24.072	0.125	25%	0.8528
	6.953	24.097	0.249	50%	0.8629
	10.518	24.128	0.377	75%	0.8648
	14.060	24.17	0.503	100%	0.8646

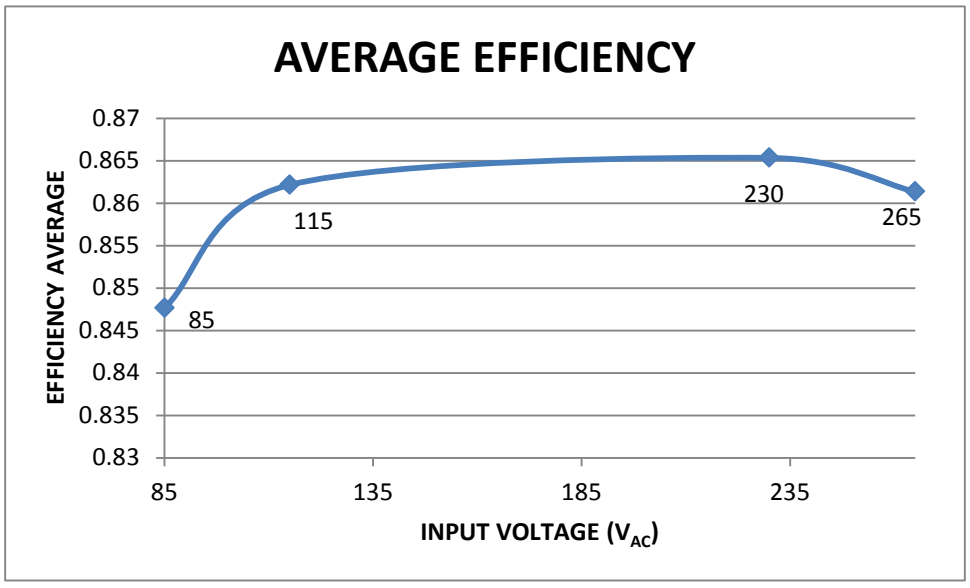

Figure 3. Four-point average efficiency in active mode with respect to input voltage

According to the European Commision Code of Conduct (CoC) on Energy Efficiency of External Power Supplies, Version 5, Tier 2 and DoE Level VI, a single output power supply with a rated output power of 12-W and greater than 6 V should have a four-point average efficiency greater than 83.2%.

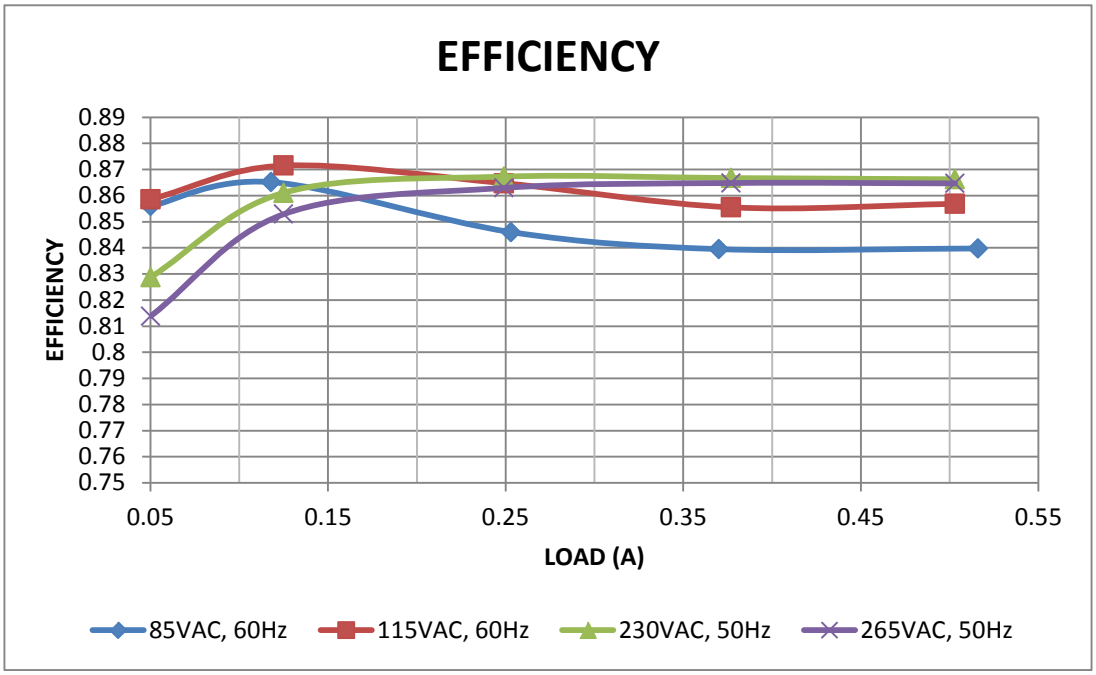

Figure 4. Efficiency over line and load

At 10% load, or 0.05 A output, PMP10927 exceeds the CoC,Tier 2 minimum requirement of 0.7326 for a single output power supply with a rated output power of 12-W and greater than 6 V.

4. No-Load Power Consumption

INPUT VOLTAGE	INPUT POWER
85 VRMS, 60Hz	2.483 mW
115 VRMS, 60Hz	2.554 mW
230 VRMS, 50Hz	2.674 mW
265 VRMS, 50Hz	3.265 mW

The PMP10927 meets “Zero-Power” requirements by having less than 5-mW of no-load power consumption at 230 Vac.

5. Output Voltage vs Output Current

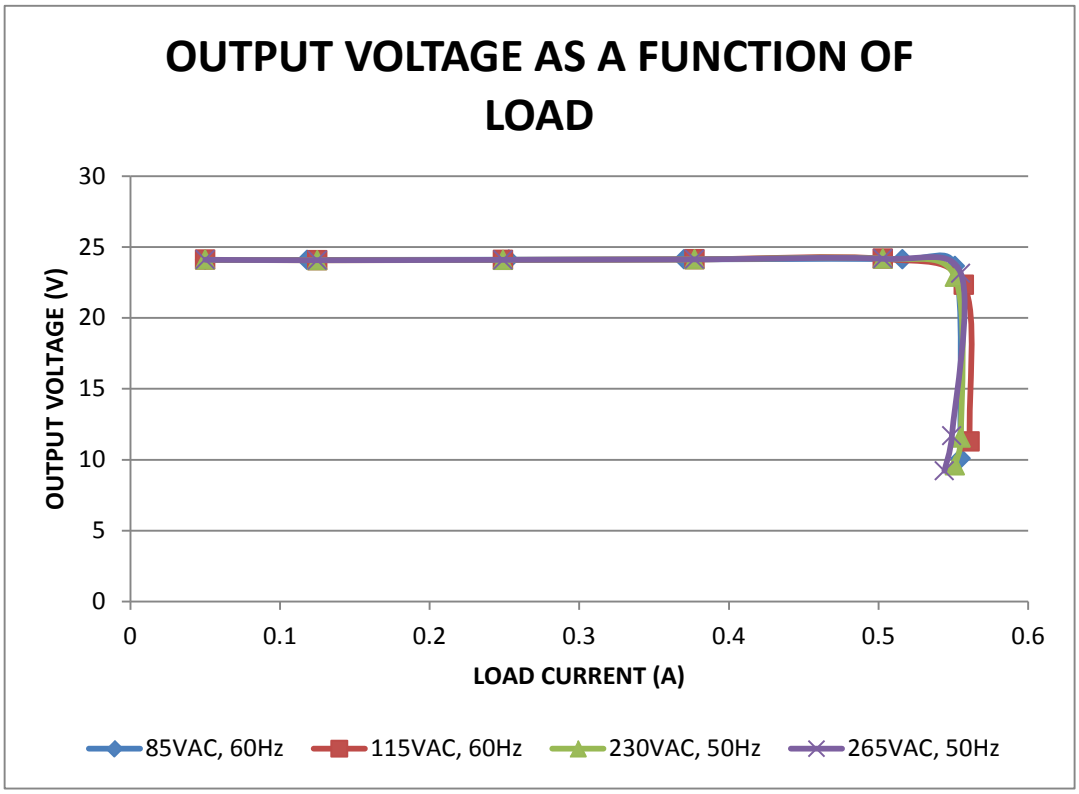

Figure 5. Constant-Voltage, Constant-Current operating modes.

The converter is in constant-voltage operating mode from 0 A load up to approximately 0.55 A. Once reaching this output over-current threshold, the converter transitions into constant-current mode where the load current remains constant until the output voltge falls below 10 V, at which point the converter enters shutdown/restart. If the load demand is decreased to the constant current operating region, the converter will automatically re-start.

6. Transient Response and WAKE Function

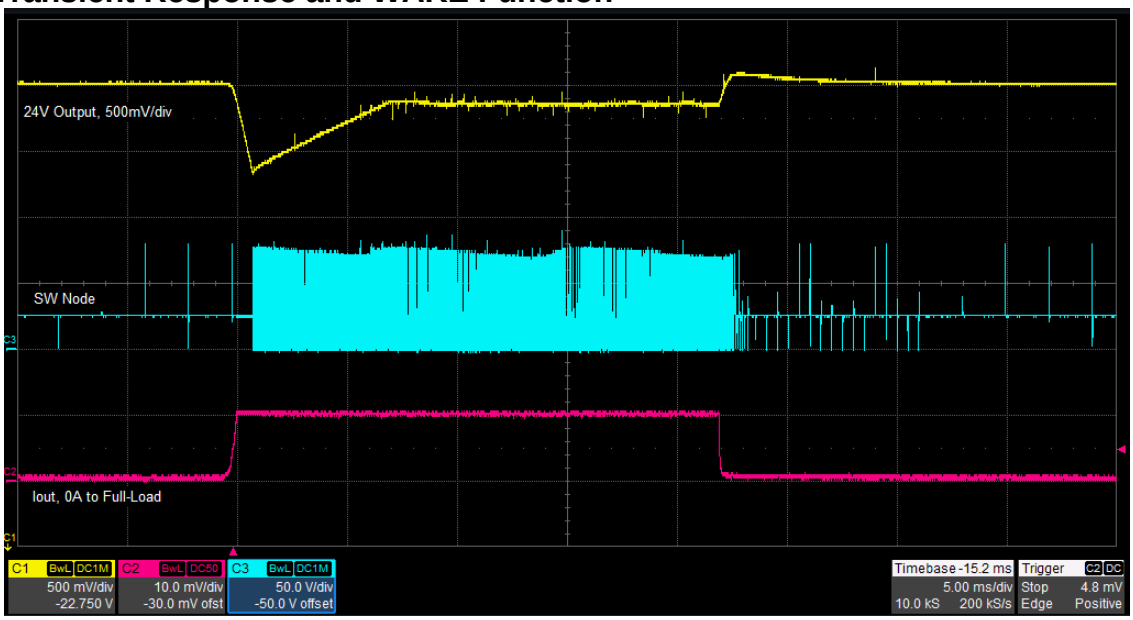

Figure 6. Load transient from No-Load to Full-Load

The transient response shown was taken with a 115 VAC, 60 Hz input voltage and a load transition from 0 A to full load. Channel 2 is the load current on a scale of 0.50 A per division, channel 1 is the output voltage on a scale of 500 mV per division, offset from the center line by -22.75 V, channel 3 I the secondary side switch node. Output voltage undershoot may vary dependent upon the specific time the transient occurs during the switching cycle.

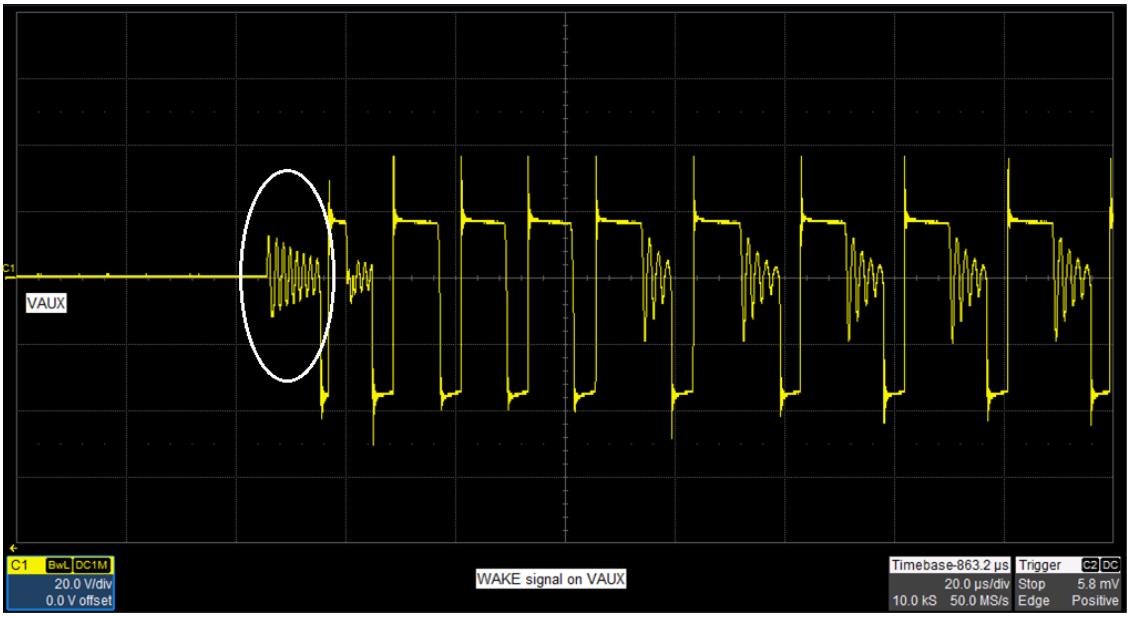

Figure 7. WAKE Signal Transmitted to the AUX Winding

Figure 7 shows the wake-up alert signal transmitted to the PSR controller on the AUX winding.

7. Output Ripple

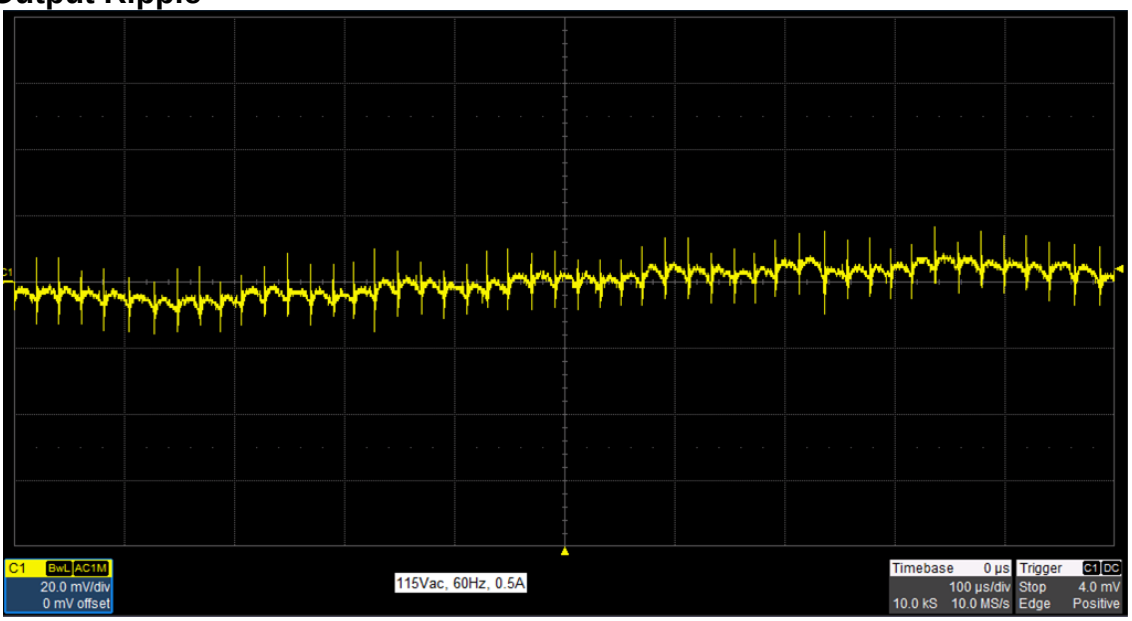

Figure 8. Output Ripple at Full-Load, 115Vin

Figure 8 shows the output voltage ripple taken at full load with an input voltage of 115 VAC, 60 Hz and the waveform is AC coupled, with 20 MHz bandwidth limit. The ripple pattern seen is characteristic of the EMI dithering method used by the UCC28730 controller.

8. Turn On Waveform

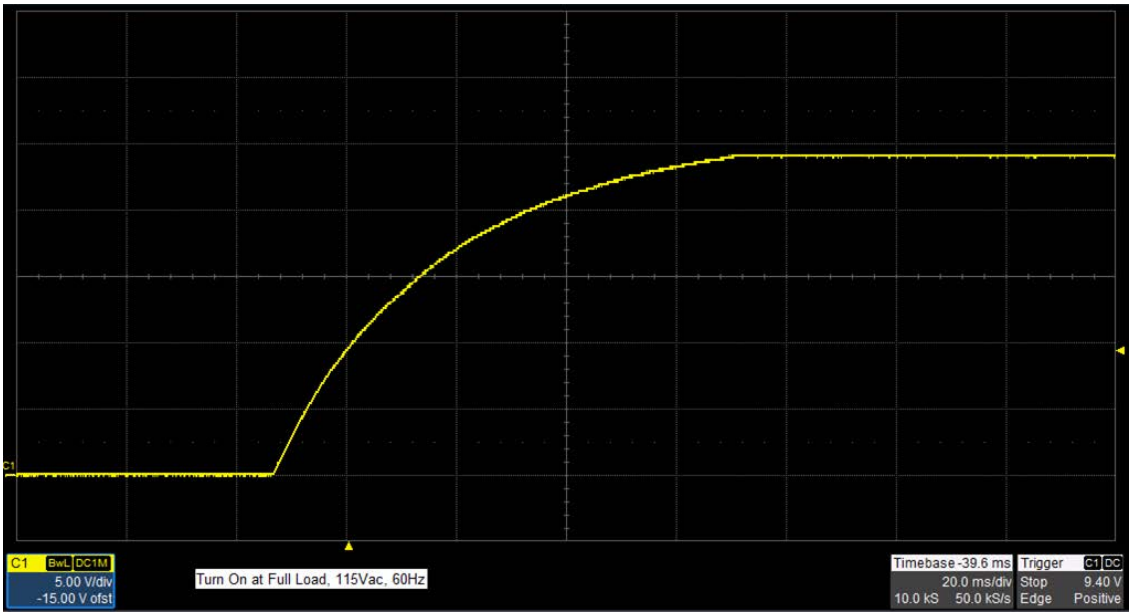

Figure 9. Output Voltage Turn On Waveform

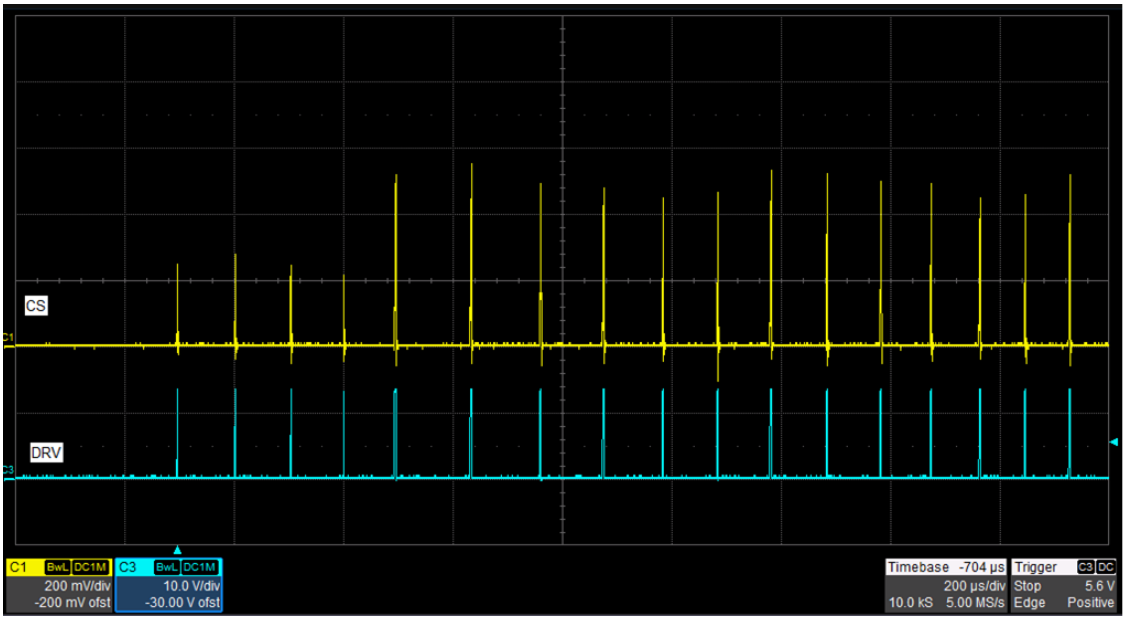

Figure 10. CS and DRV at Turn On

Figure 10 shows how the UCC28730 limits the first four switching-cycle current peaks to $I_{PP(min)}$ in order to monitor for any initial input or output faults with limited power delivery. After these initial four pulses, the controller will limit the amplitude of the peak primary current to approximately 0.67 x $I_{PP(max)}$. Modifications are also made to D_{MAGCC}, increasing it from 0.432 to 0.650. These modifications during startup allow high frequency charge-up of the output capacitor to avoid audible noise. Once the VS signal is greater than 1.36 V (approximately 1.45 V on the output), D_{MAGCC} is restored to its normal value and the peak primary current resumes at $I_{PP(max)}$.

9. Switching Waveform

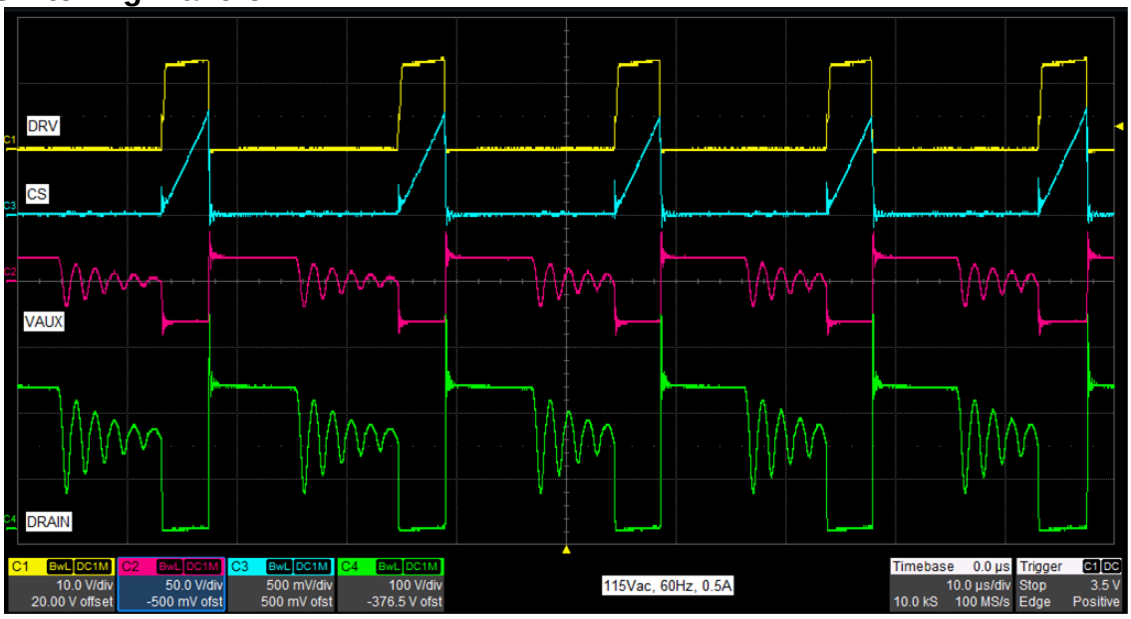

Figure 11. Primary Side Switching Waveform

The typical switching waveform can be seen in Figure 11. Channel 1 shows the gate drive at 10 V per division, channel 2 shows the AUX winding at 50 V per division, channel 3 is the CS waveform at 500 mV per division, and channel 4 shows the MOSFET drain to source voltage at 100 V per division. The scan was taken at 0.5 A load, 115 V_{AC}, 60 Hz input voltage. At this operating point, the switching frequency is dithering between 50 kHz and 45 kHz due to valley skipping. Figure 12 shows the switching waveforms on the secondary side.

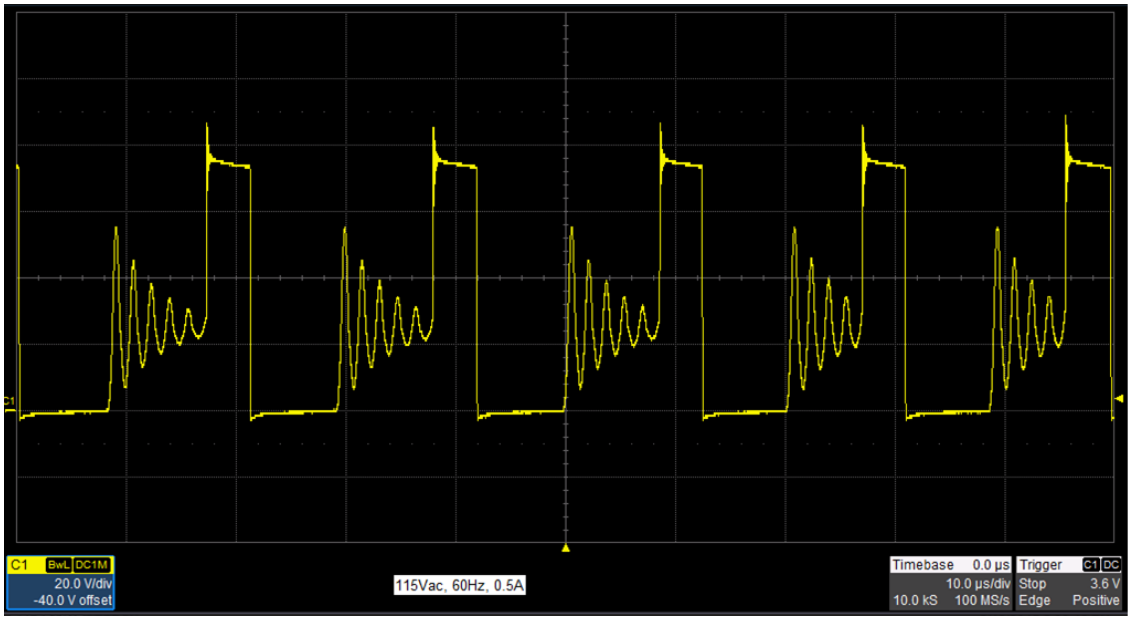

Figure 12. Secondary Side Switching Waveform

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