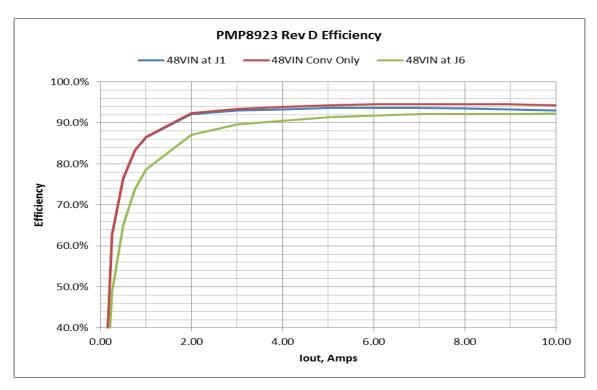
All testing performed with a 48V input, 10A load, and 20MHz BW unless otherwise noted.

Efficiency

The efficiency is shown below:

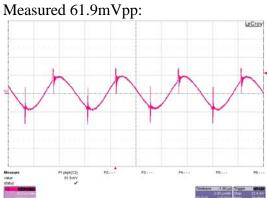
					Iin at J1				
			TP2/3		VDD/PWRGND				
	TP6/7	J1	J1	J1	Conv	Conv	J6	J 6	J 6
<u>Iout</u>	Vout	<u> Iin</u>	Vin	<u>Eff</u>	Vin	Eff	<u> Iin</u>	<u>Vin</u>	<u>Eff</u>
0.00	5.063	0.016	48.00	0.0%	48.00	0.0%	0.028	48.00	0.0%
0.25	5.063	0.042	48.00	62.8%	47.98	62.8%	0.054	48.00	48.8%
0.50	5.063	0.069	48.00	76.4%	47.96	76.5%	0.081	48.00	65.1%
0.75	5.063	0.095	48.00	83.3%	47.94	83.4%	0.107	48.00	73.9%
1.00	5.063	0.122	48.00	86.5%	47.92	86.6%	0.134	48.00	78.7%
2.00	5.062	0.229	48.00	92.1%	47.88	92.3%	0.242	48.00	87.2%
3.00	5.062	0.340	48.00	93.1%	47.80	93.4%	0.353	48.00	89.6%
4.00	5.061	0.452	48.00	93.3%	47.72	93.9%	0.466	48.00	90.5%
5.00	5.061	0.563	48.00	93.6%	47.67	94.3%	0.577	48.00	91.4%
6.00	5.060	0.675	48.00	93.7%	47.60	94.5%	0.689	48.00	91.8%
7.00	5.060	0.788	48.00	93.6%	47.54	94.6%	0.801	48.00	92.1%
8.00	5.060	0.902	48.00	93.5%	47.46	94.6%	0.915	48.00	92.2%
9.00	5.059	1.017	48.00	93.3%	47.39	94.5%	1.029	48.00	92.2%
10.00	5.059	1.133	48.00	93.0%	47.33	94.3%	1.143	48.00	92.2%



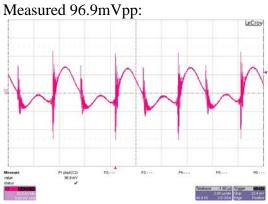
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Ripple and Noise

Output Ripple (C34), 20mV/div

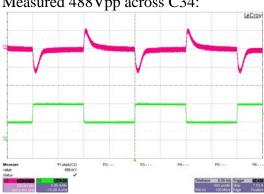


Input Ripple (C24), 20mV/div

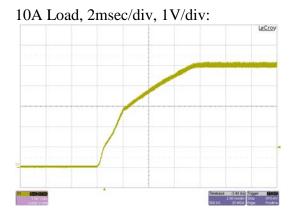


Dynamic Loading

Output Load Step; 5A to 10A load step; 500mA/usec; 200mV/div, 5A/div, 500usec/div Measured 488Vpp across C34:



Turn On Response

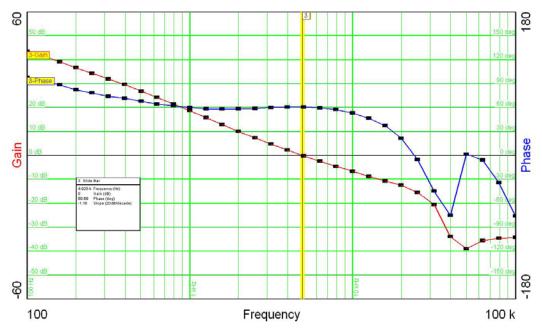






Loop Stability

The measured Bode plot of the converter with a 10A load is shown below:



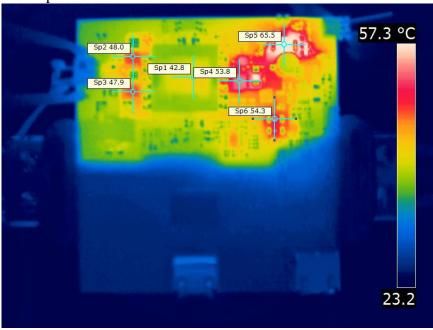
Bandwidth: 4.9KHz Phase Margin: 60 degrees Gain Margin: 15dB

Thermal Plots

PoE Input at J1:



48V input at J6:



Photo



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