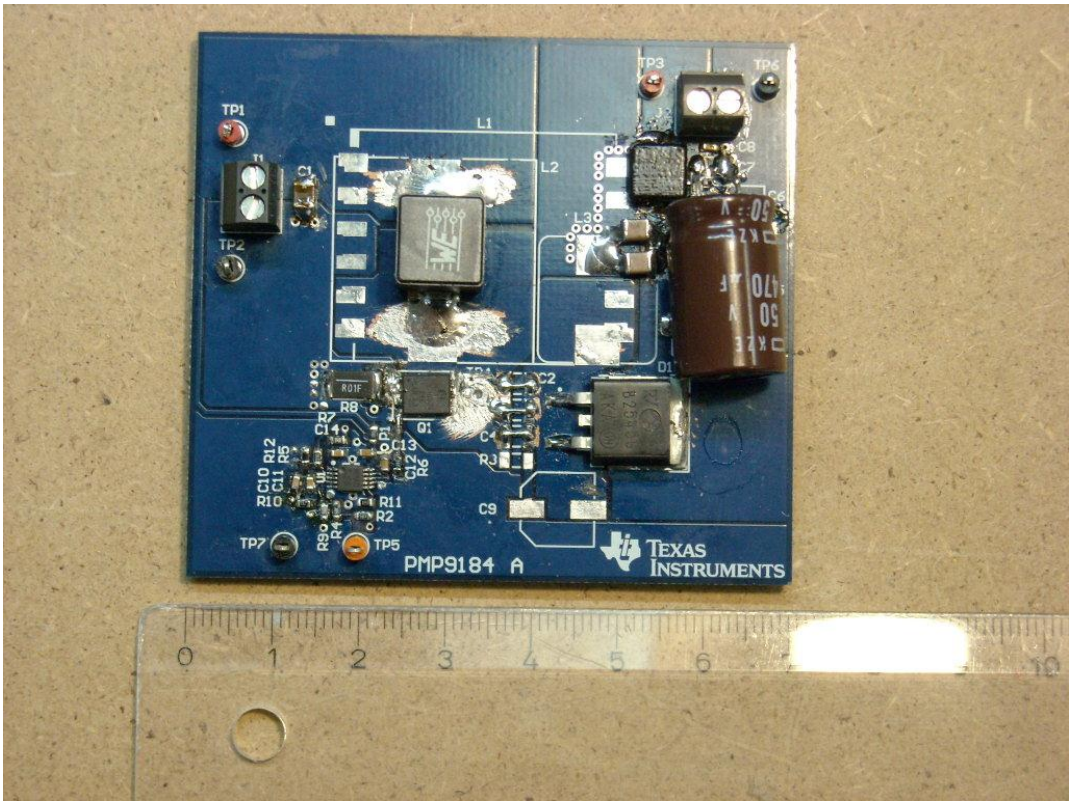
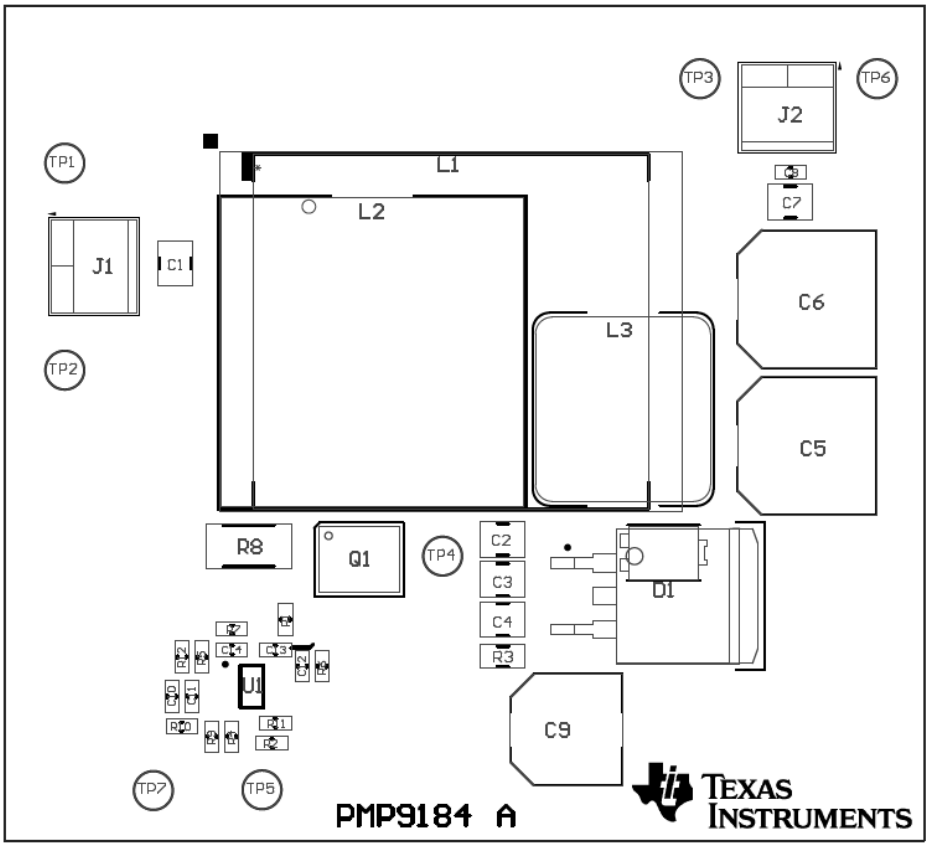
## PHOTO OF THE PROTOTYPE:



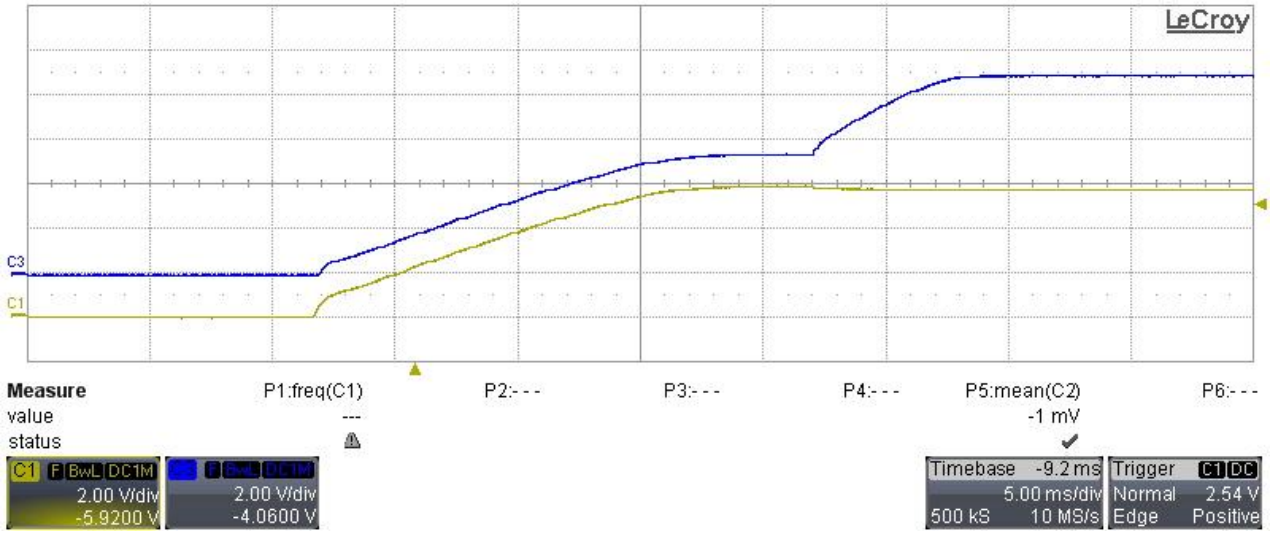



# 1 Startup

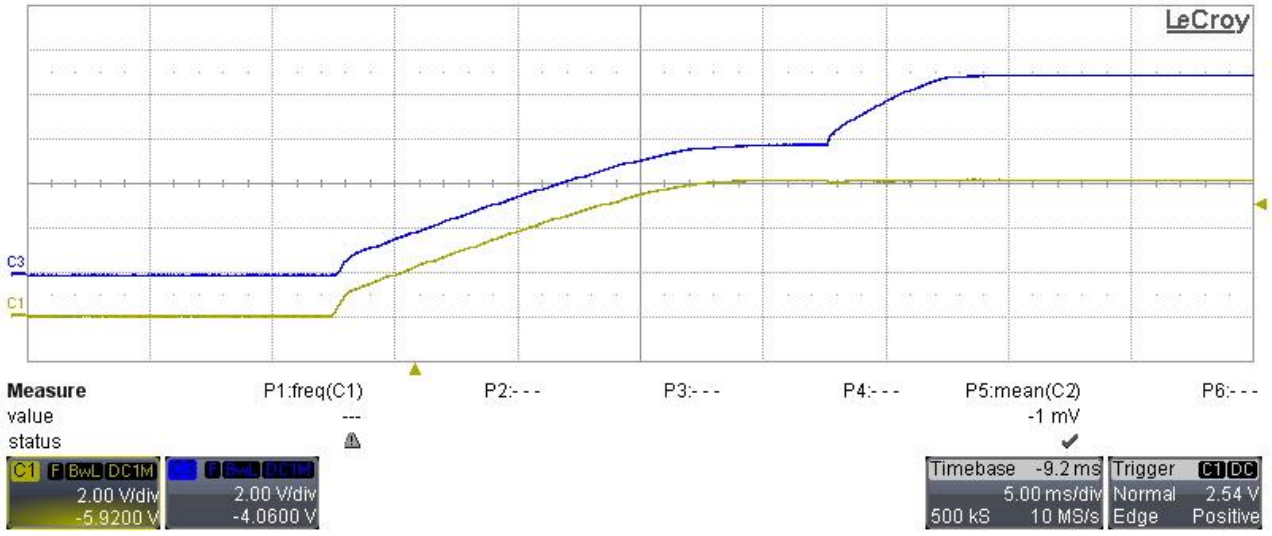
The output voltage behavior at startup is shown in the images below.
The output was loaded @ 3.3A in constant current mode for the first screenshot and unloaded for the second one. The input voltage was set to 6V.

**Ch.1: Input voltage (2V/div, 5ms/div, 20MHz BWL)**
**Ch.3: Output voltage (2V/div, 20MHz BWL)**

**Iout = 3.3A**

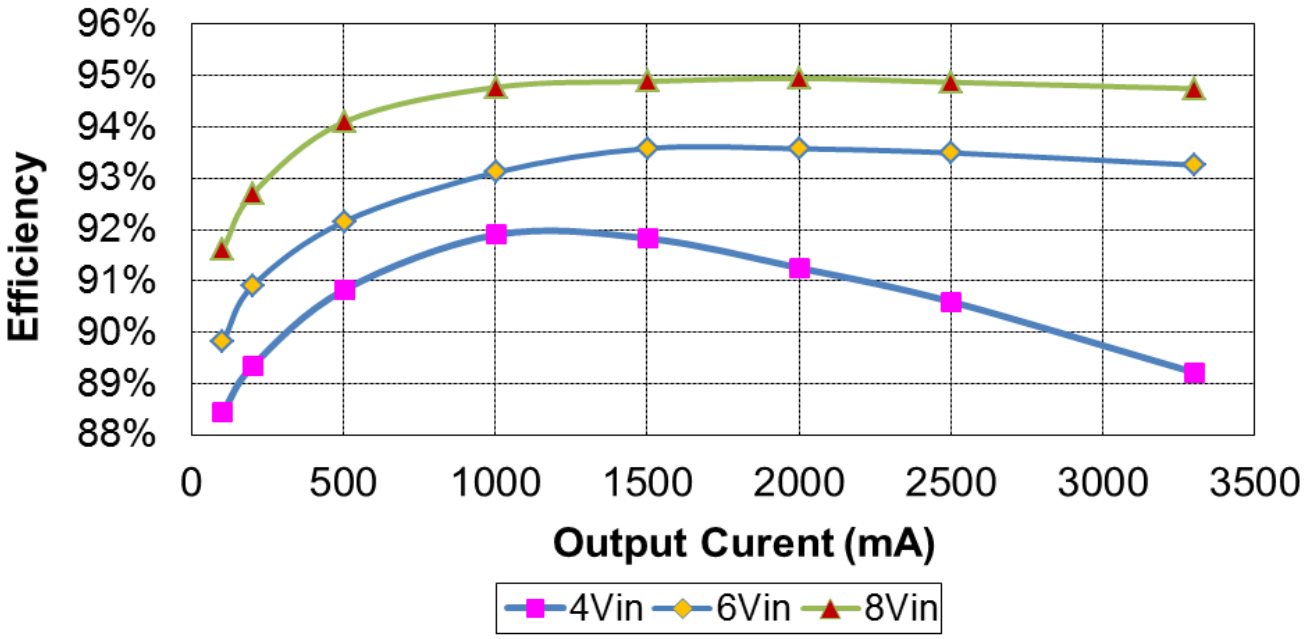



**Iout = 0**



## 2 Efficiency

The efficiency data are shown in the tables and graph below. The input source has been set to 4V, 6V and 8V, while the load has been varied between 0 and 3.3A.



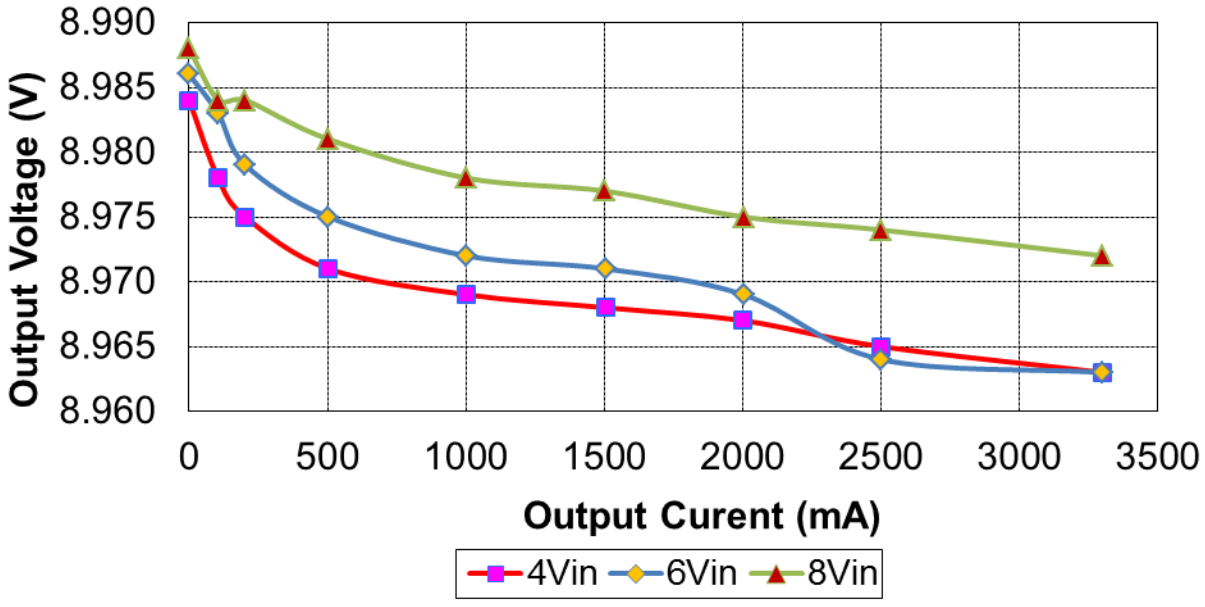

| Iout (mA) | Vout (V) | Pout (W) | Iin (mA) | Vin (V) | Pin (W) | Ploss (W) | Eff. (%) |
|---|---|---|---|---|---|---|---|
| 0.0 | 8.984 | 0.00 | 2.60 | 4.089 | 0.01 | 0.01 | 0.0% |
| 104.4 | 8.978 | 0.94 | 261.6 | 4.051 | 1.06 | 0.12 | 88.4% |
| 203.2 | 8.975 | 1.82 | 508.1 | 4.017 | 2.04 | 0.22 | 89.4% |
| 503.2 | 8.971 | 4.51 | 1229 | 4.044 | 4.97 | 0.46 | 90.8% |
| 1003.3 | 8.969 | 9.00 | 2437 | 4.018 | 9.79 | 0.79 | 91.9% |
| 1504 | 8.968 | 13.49 | 3652 | 4.022 | 14.69 | 1.20 | 91.8% |
| 2002 | 8.967 | 17.95 | 4872 | 4.038 | 19.67 | 1.72 | 91.3% |
| 2500 | 8.965 | 22.41 | 6116 | 4.045 | 24.74 | 2.33 | 90.6% |
| 3301 | 8.963 | 29.59 | 8235 | 4.027 | 33.16 | 3.58 | 89.2% |

| Iout (mA) | Vout (V) | Pout (W) | Iin (mA) | Vin (V) | Pin (W) | Ploss (W) | Eff. (%) |
|---|---|---|---|---|---|---|---|
| 0.0 | 8.986 | 0.00 | 2.80 | 6.009 | 0.02 | 0.02 | 0.0% |
| 104.5 | 8.983 | 0.94 | 173.0 | 6.041 | 1.05 | 0.11 | 89.8% |
| 203.3 | 8.979 | 1.83 | 333.6 | 6.019 | 2.01 | 0.18 | 90.9% |
| 503.2 | 8.975 | 4.52 | 813 | 6.025 | 4.90 | 0.38 | 92.2% |
| 1003.3 | 8.972 | 9.00 | 1604 | 6.027 | 9.67 | 0.67 | 93.1% |
| 1504 | 8.971 | 13.49 | 2393 | 6.025 | 14.42 | 0.93 | 93.6% |
| 2003 | 8.969 | 17.96 | 3186 | 6.026 | 19.20 | 1.23 | 93.6% |
| 2500 | 8.964 | 22.41 | 3985 | 6.015 | 23.97 | 1.56 | 93.5% |
| 3301 | 8.963 | 29.59 | 5251 | 6.042 | 31.73 | 2.14 | 93.3% |

| Iout (mA) | Vout (V) | Pout (W) | Iin (mA) | Vin (V) | Pin (W) | Ploss (W) | Eff. (%) |
|---|---|---|---|---|---|---|---|
| 0.0 | 8.988 | 0.00 | 2.70 | 8.030 | 0.02 | 0.02 | 0.0% |
| 104.6 | 8.984 | 0.94 | 128.0 | 8.013 | 1.03 | 0.09 | 91.6% |
| 203.4 | 8.984 | 1.83 | 245.8 | 8.019 | 1.97 | 0.14 | 92.7% |
| 503.4 | 8.981 | 4.52 | 601 | 8.001 | 4.80 | 0.28 | 94.1% |
| 1003.5 | 8.978 | 9.01 | 1188 | 8.002 | 9.51 | 0.50 | 94.8% |
| 1503 | 8.977 | 13.49 | 1775 | 8.011 | 14.22 | 0.73 | 94.9% |
| 2003 | 8.975 | 17.98 | 2365 | 8.006 | 18.93 | 0.96 | 94.9% |
| 2500 | 8.974 | 22.44 | 2952 | 8.011 | 23.65 | 1.21 | 94.9% |
| 3301 | 8.972 | 29.62 | 3906 | 8.003 | 31.26 | 1.64 | 94.7% |

## 3 Output voltage regulation vs. load

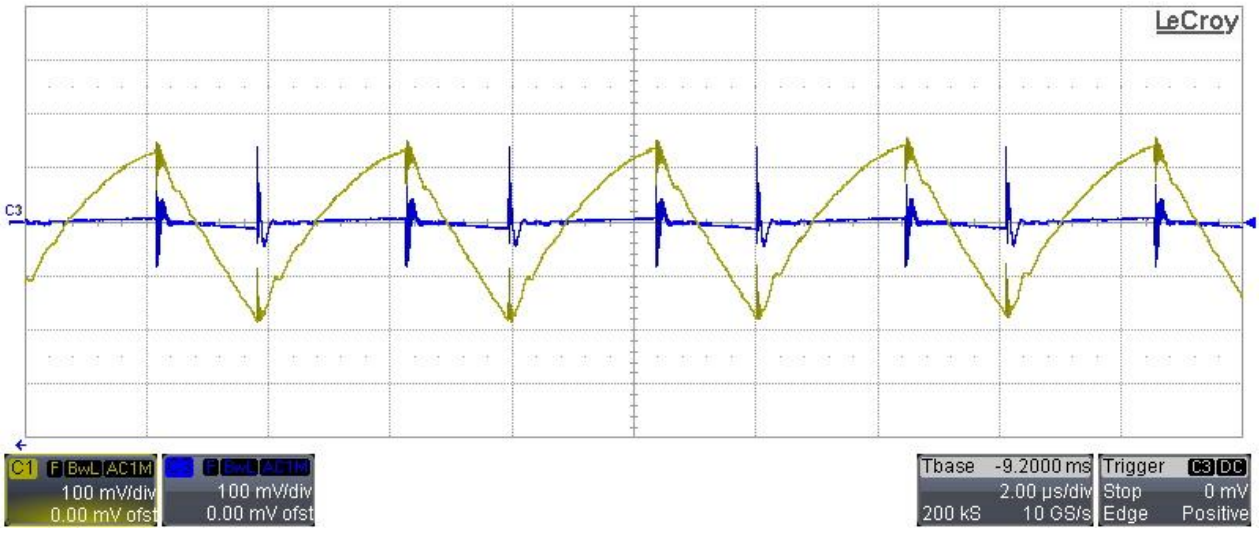
The output voltage variation versus load current, for the three input voltages, is plotted below.



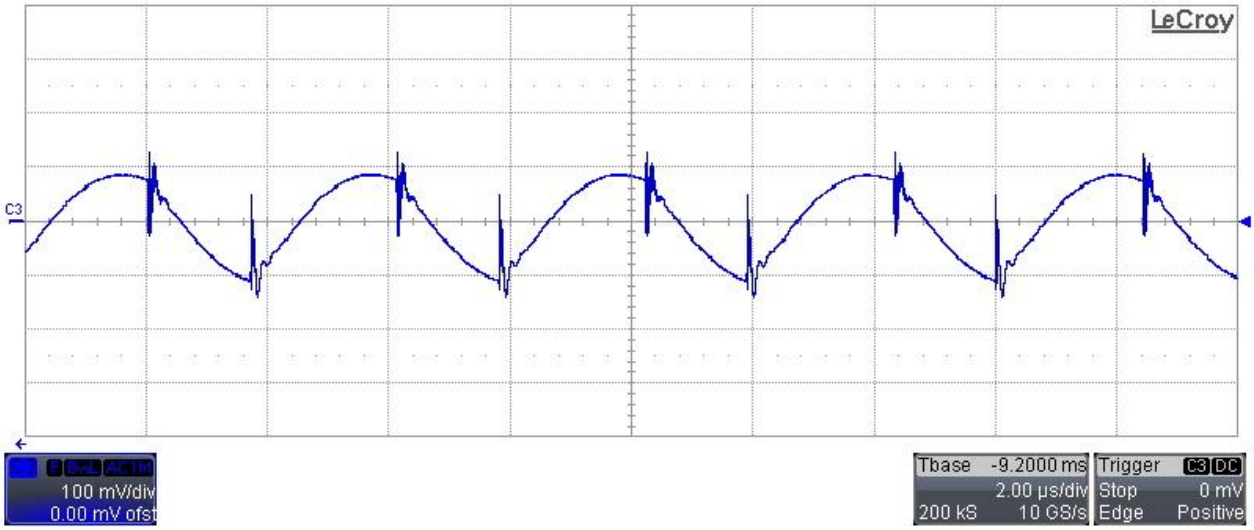
## 4 Output ripple voltage

The output ripple voltage has been measured by supplying the converter @ 6Vdc and full load. In the following measurements, the filter inductor L100 was populated (see upper picture) while for the bottom picture it has been shorted. The measurement conditions were the same.

**Ch.1: Ripple voltage on C5, C6 (100mV/div, 2us/div, 20MHz BWL, AC coupling)**
**Ch.3: Ripple voltage on C100 (100mV/div, 20MHz BWL, AC coupling)**
**L100 populated, full load:**



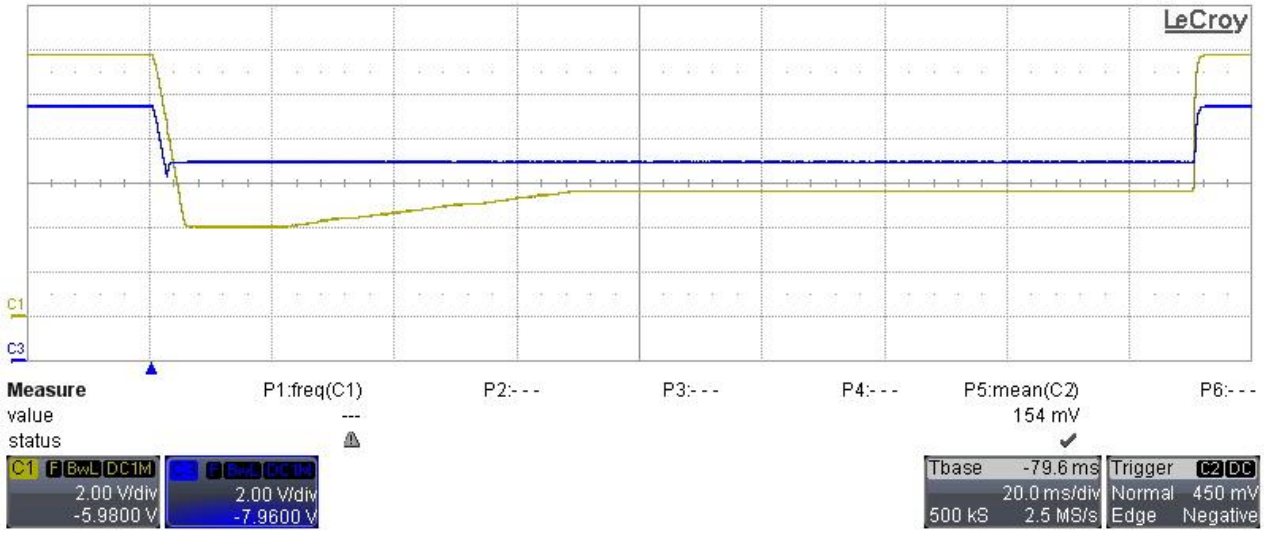

**Ch.3: Ripple voltage on C100 (100mV/div, 2us/div, 20MHz BWL, AC coupling)**
**L100 shorted, full load:**



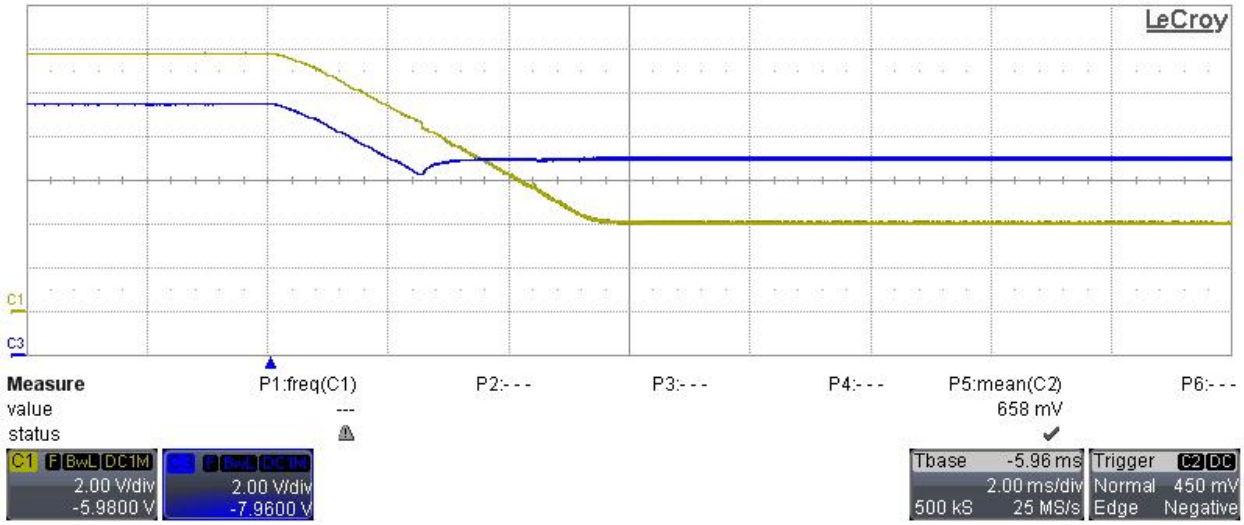
## 5 Cold crank simulation

In the pictures below are shown the output voltage variation, at full load and by applying the "cold crank" profile to input terminals.

**Ch.1: Input voltage (2V/div, 20msec/div, 20MHz BWL, DC coupling)**
**Ch.3: Output voltage (2V/div, 20MHz BWL, DC coupling)**



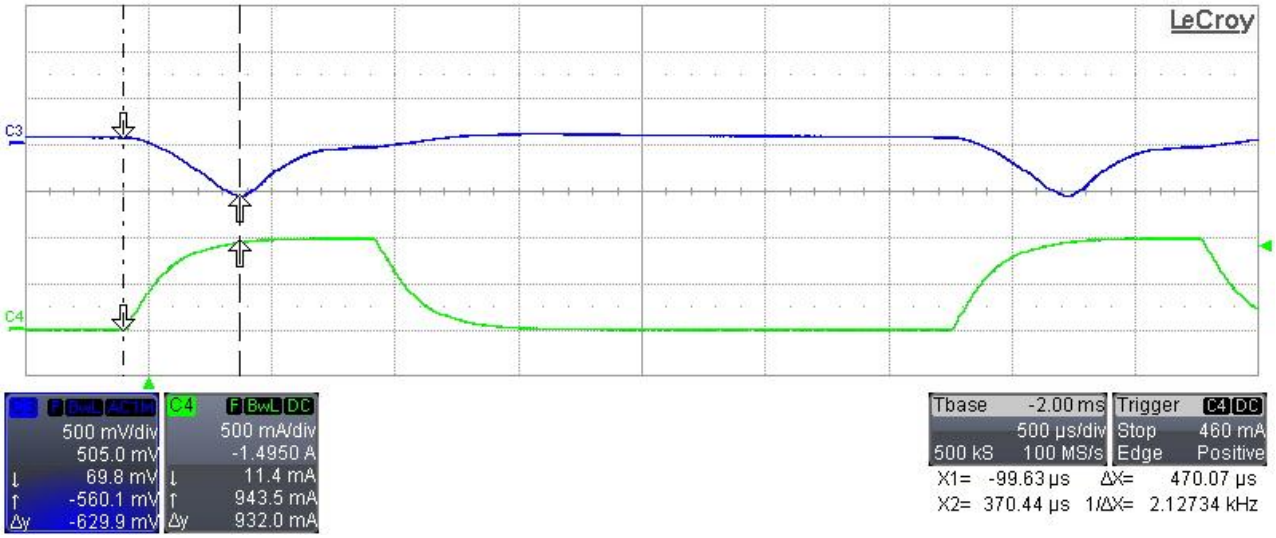

In picture below we see the same test but magnified at the downslope of the input voltage:
The time division in this case is 2msec/div.



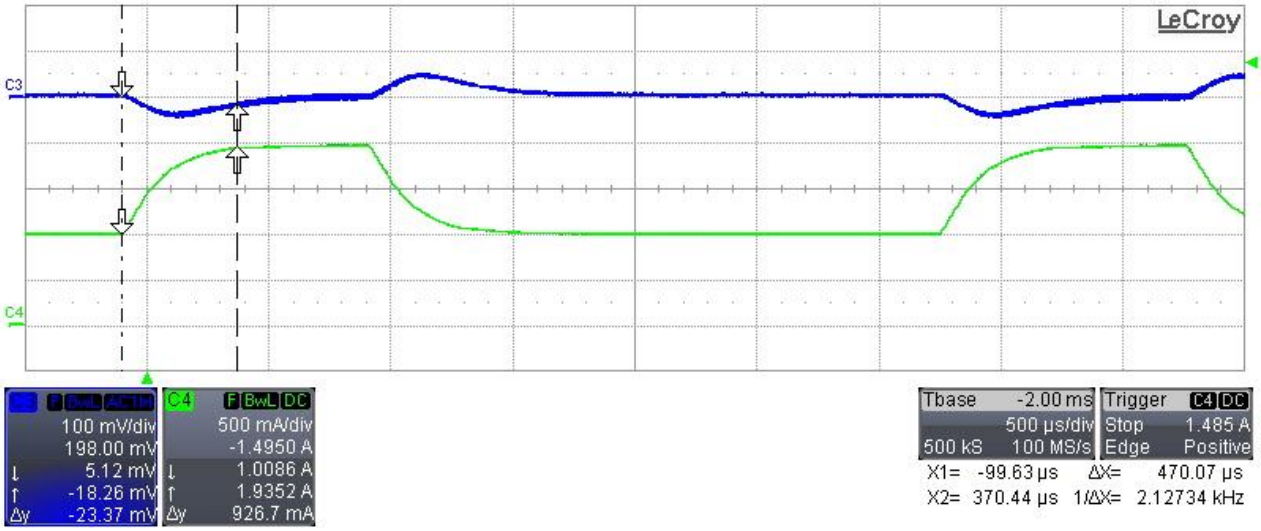
## 6 Transient response on load variations

In the pictures below are shown the output voltage variation during transients on the output current. The input voltage has been set to the minimum value of 4V, while the output current switched between 0 and 1A (upper picture) and 1A to 2A (bottom picture).

**Ch.3: Output voltage (500mV/div, 500usec/div, 20MHz BWL, AC coupling)**
**Ch.4: Output current (500mA/div, 20MHz BWL, DC coupling)**
**Iout = 0A → 1A → 0A**



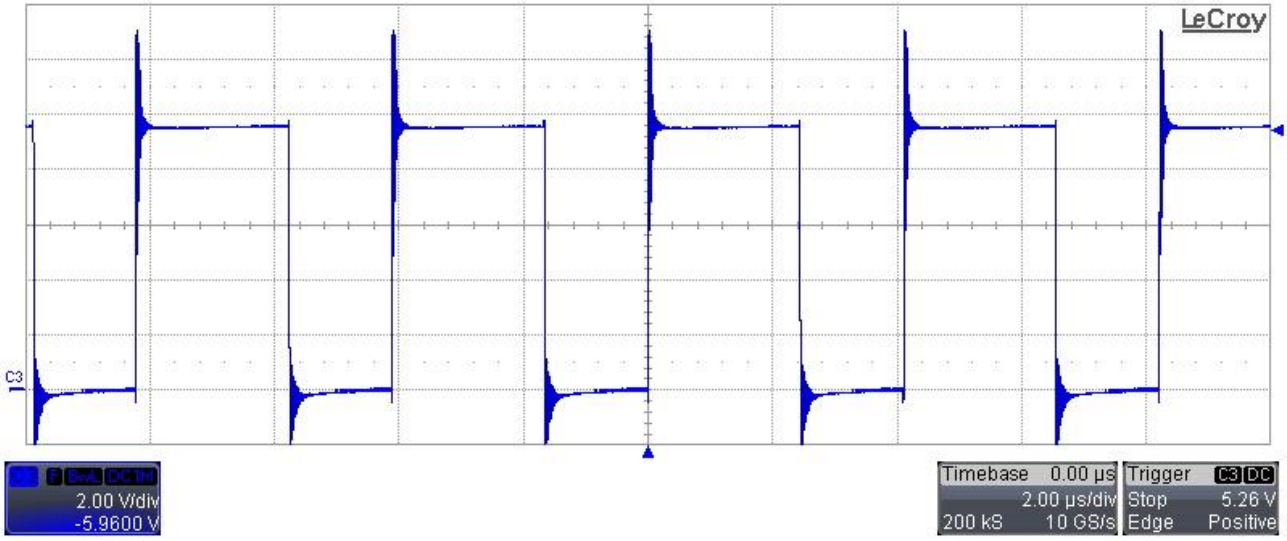

**Ch.3: Output voltage (100mV/div, 500usec/div, 20MHz BWL, AC coupling)**
**Ch.4: Output current (500mA/div, 20MHz BWL, DC coupling)**
**Iout = 1A → 2A → 1A**



## 7 Switch-node

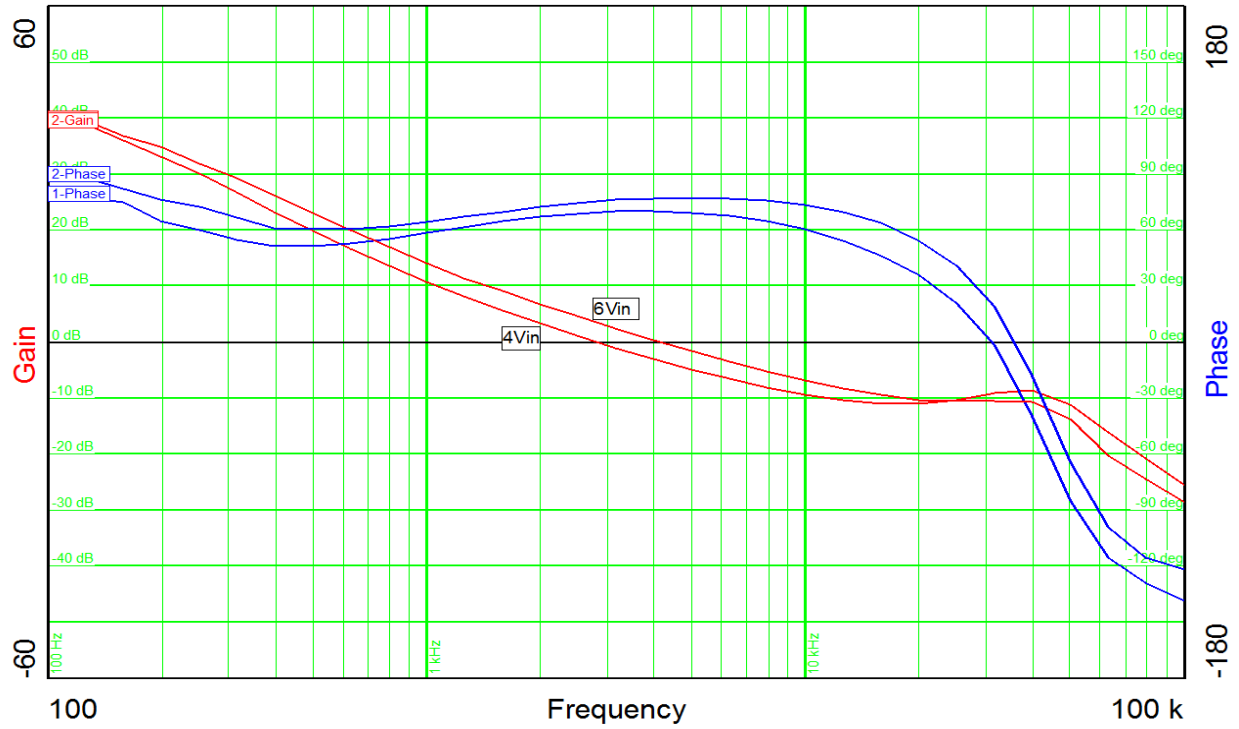
The image below shows the switch-node waveform (drain of Q1) at 6Vdc input and full load.

**Ch.3: Q1 drain voltage (2V/div, 2us/div, No BWL, 3-bit filter, DC coupling)**




## 8 Loop Response

The picture below shows the loop response of the converter measured at 4V and 6V input voltage and full load. The crossover frequency Fco, at 4Vin, was 2.83 KHz and the phase margin 69.6 deg., while at 6Vin we had Fco = 4.17KHz and Pm = 77.2 deg.



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