TI Designs 3-W Non-ISO Bias Power Supply With up to 80% Efficiency, 15-dB Margin EMI Performance Reference Design

Design Overview

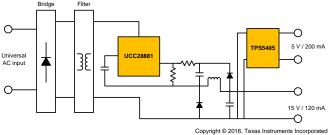
The TIDA-00940 is a 3-W, non-isolated bias power supply with up to 80% efficiency and excellent EMI performance, designed for motor control and drive subsystems in major appliances to save system costs and other benefits including:

- Non-isolated buck topology design saves system BOM cost with limited external components for AC/DC stage
- Excellent EMI performance with 15-dB margin meets EN-55022 Class B requirements (conducted emission)
- Provide reliable start-up for applications of high load capacitance
- No external cooling needed up to 85°C ambient operation
- Supports 700-V self-powered start-up with no an auxiliary bias winding needed

This reference design provides two non-isolated outputs with buck topology and is implemented using TI's UCC28881 and TPS5405 controllers to provide full protection. The hardware is designed and tested to pass EN-55022 Class B requirements for household appliances.

Design Resources

TIDA-00940Design FolderUCC28881Product FolderTPS5405Product Folder



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Design Features

- Wide Operating Input Range 85- to 270-V AC With Full Power Delivery Over Entire Range
- High Convert Efficiency up to 80% at Full Load
- Competitive BOM Cost With Few External Components
- Low Current Consumption for Standby and Full-Load Operation
- Robust Short-Circuit and Overload Protections With Intelligent Current Limit Design
- Switching Node Anti-Ringing Helps Get Excellent EMI Performance
- Start-up With High-Load Capacitance
- Small PCB Form Factor (77 mm × 30 mm)

Featured Applications

- Refrigerators and Freezers
- Washing Machines
- Air Conditioners
- Home Appliances
- Kitchen Hoods

TI E2E™

Community

Vacuum Cleaners



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Key System Specifications



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1 **Key System Specifications**

Table 1. Key System Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNITS	
INPUT CHARACTERISTICS		1	I	ŀ			
Input voltage	V _{IN}	—	85	230	270	V AC	
Frequency	F _{AC}	-	47	—	64	Hz	
Minimum voltage to start-up	/linimum voltage to start-up V _{HVIN(min)} —		—	30	—	V AC	
Input current	I _{IN}	V _{IN} = nom, I _{OUT} = max	—	0.1	—	А	
OUTPUT CHARACTERISTICS	DUTPUT CHARACTERISTICS						
Output voltage	V _{OUT1}	V_{IN} = nom, I_{OUT} = min to max	14.5	15	16	V	
	V _{OUT2}	$V_{IN} = nom, I_{OUT} = min to max$	—	5	—	V	
Output current	I _{OUT1}	V _{IN} = min to max	25	120	—	mA	
Output current	I _{OUT2}	V _{IN} = min to max	—	200	_	mA	
Output power	Pout	V _{IN} = min to max	—	—	3	W	
Line regulation	+15V	V_{IN} = min to max, I_{OUT} = nom	—	1	_	%	
	+5V	V_{IN} = min to max, I_{OUT} = nom	—	1	—	%	
Load regulation	+15V	$V_{IN} = nom, I_{OUT} = min to max$	—	10	—	%	
Load regulation	+5V	$V_{IN} = nom, I_{OUT} = min to max$	—	1	—	%	
Output voltage ripple	V_{OUT1_RIPPLE}	V _{IN} = nom, I _{OUT} = max	_	50	—	mV	
Output voltage ripple	V_{OUT2_RIPPLE}	$V_{IN} = nom, I_{OUT} = max$	—	60	_	mV	
SYSTEM CHARACTERISTICS	3	·					
Peak efficiency	η_{PEAK}	V _{IN} = 115-V AC	—	80	—	%	
Operation temperature	T _{NOM}	_	-25	—	65	°C	



2 System Description

Home appliance equipment such as refrigerators, air conditioners, dishwashers, and kitchen hoods use three-phase, pulse-width modulated (PWM) brushless DC (BLDC) electric motor drives or permanent magnet synchronous motor (PMSM) drives. These drives are typically fractional or low horsepower types with power ratings from 0.25 hp (186 W) to 2 hp (1,500 W). The motor drive circuits consist of an intelligent power module (IPM) or discrete insulated-gate bipolar transistors (IGBTs) with gate drivers for DC to AC conversion; a low-cost microcontroller for variable speed, torque control, or both; and current measurement and control feedback sensing circuits for closed loop control. These systems require low-watt power supplies to convert high-voltage DC to the multiple low-voltage rails required to provide bias for control circuits. These systems need electromagnetic interference (EMI) filters to reduce EMI and a 50-Hz DC choke to shape the line current and reduce harmonics. Hence, the bias power supply is a high-voltage input DC-DC converter. Typically, these applications require a non-isolated power supply, as each of the circuits operates at the same potential.

This reference design is a simple high-voltage buck regulator and is configured for appliances that require a non-isolated 3-W power supply. The design meets the key challenges of a bias power supply for appliances to provide safe and reliable power while delivering a high performance with low power consumption and a low Bill of Materials (BOM) cost.

The reference design is a multiple output (15 V and 5 V), 3-W power supply that uses the UCC28881, a low-cost flyback controller. The design can be used for converting a high-voltage DC input with a wide range from 90- to 380-V DC, or converting an AC input ranging from 85- to 270-V AC, to standard power rails of 15 V and 5 V. As per the requirements of appliances, the design meets the requirements of high efficiency (> 75%) and a low standby power of < 100 mW when the system is in idle mode. The reference design offers the following key benefits:

- Works for a wide input range for both a DC input (90- to 380-V DC) or an AC input (85- to 270-V AC)
- Integrated high-voltage current source for internal device bias power
- Combination of frequency and peak current modulation causes high conversion efficiency

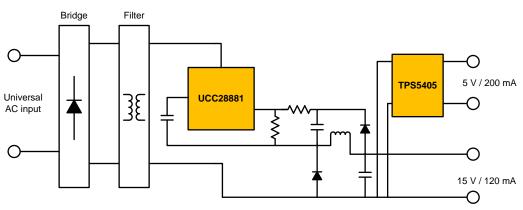
The controller has an inherent safety feature that detects feedback for open loop or loss of feedback detection, during which the controller turns off the MOSFET to safeguard the low-voltage system components from high-voltage intrusion. In addition, the design offers protection for the output from short-circuit, overcurrent, and overvoltage conditions. This design demonstrates the high-performance DC-DC operation in a small form factor (77 mm × 30 mm) and provides flexibility for voltage settings through simple resistor changes. The reference design includes a rectifier, EMI filter, and bus capacitor to power directly from an AC input. This ability to power directly from an AC input provides flexibility for users to use the design as an independent bias power supply module. Various parameters of the design like regulation, efficiency, EMI signature, output ripple, startup, and switching stresses were tested and documented.

3

System Description



3 Block Diagram



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Figure 1. Block Diagram of PFC Regulator

3.1 Highlighted Products and Key Advantages

The following subsections detail the highlighted products used in this reference design, including the key features for their selection. See their respective product datasheets for complete details on any highlighted device.

3.1.1 UCC28881—700-V Lowest Quiescent Current Off-Line Switcher

The UCC28881 integrates the controller and a $14-\Omega$, 700-V power MOSFET into one monolithic device. The device also integrates a high-voltage current source, enabling start-up and operation directly from the rectified mains voltage. The UCC28881 is from the same family as the UCC28880 with higher current handling capability.

The low quiescent current of the device enables excellent efficiency. With the UCC28881, the most common converter topologies such as buck, buck-boost and flyback can be built using a minimum number of external components.

The UCC28881 incorporates a soft-start feature for controlled startup of the power stage, which minimizes the stress on the power-stage components.

Other key features that make the device ideal for this application are:

- Integrated 14-Ω, 700-V power MOSFET
- Integrated high-voltage current source for internal device bias power
- Integrated current sense
- Internal soft start
- Self-biased switcher (start-up and operation directly from rectified mains voltage)
- · Supports buck, buck-boost and flyback topologies
- <100-μA device quiescent current
- · Robust current protection during load short circuit
- Protection
 - Current limit
 - Overload and output short circuit
 - Over temperature



3.1.2 TPS5405—Non-Synchronous Step-Down Regulator With Integrated MOSFET

The TPS5405 is a 28-V, 2-A, step-down (buck) converter with an integrated high-side N-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current-mode control, which reduces output capacitance and simplifies external frequency compensation design.

The switching frequency of the TPS5405 is adjustable with an external resistor or fixed by connecting the frequency program pin to GND or leaving it unconnected.

The TPS5405 starts switching at V_{IN} equal to 3.5 V. The operating current is 100 μ A typically when not switching and under no load. When the device is disabled, the supply current is 1 μ A typically. The integrated 120-m Ω high-side MOSFET allows for high efficiency power supply designs with continuous output currents up to 2 A.

The TPS5405 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically.

By adding an external capacitor, the slow start time of the TPS5405 can be adjustable, which enables flexible output filter selection. To improve the efficiency at light load conditions, the TPS5405 enters a special pulse skipping mode when the peak inductor current drops below 300 mA typically. The frequency foldback reduces the switching frequency during start-up and overcurrent conditions to help control the inductor current. The thermal shutdown gives the additional protection under fault conditions.

Other key features that make the device ideal for this application are:

- Fixed 5-V output
- 6.5- to 28-V wide input voltage range
- Up to 2-A maximum continuous output loading current
- · Pulse skipping mode to achieve high light load efficiency
- Over 80% efficiency at 10-mA loading
- Adjustable 50-kHz to 1.1-MHz switching frequency set by an external resistor (leave pin ROSC floating, set frequency to 120 kHz)
- Peak current-mode control
- Cycle-by-cycle overcurrent protection
- Switching node anti-ringing to ease EMI issue
- External soft start
- Available in SOIC8 package



System Design Theory

4 System Design Theory

This TI Design is a non-isolated buck regulator operating in discontinuous mode, implemented using the UCC28881 controller, and specifically tailored for the needs of home appliance applications. This design serves as a simple power supplies with integrated MOSFET technology. This design is intended for a wide range of input voltages between 90- to 380-V DC or 85- to 270-V AC. The system efficiency is over 80% with a 125-V DC input and 79% with a 325-V DC input under full load conditions. Low EMI, high efficiency, low component count, and compact size are the main focus of this design for targeted applications.

4.1 Detailed Design Procedure

This procedure outlines the steps to design a non-isolated power supply based on the UCC28881 controller, where the UCC28881 is connected in a high-side buck configuration having an output voltage that is positive with respect to the negative high-voltage input (VIN–). The output voltage is set to 15 V in this example, but it can easily be changed by changing the value of R_{FB1} . See Figure 2 for component names and network locations. The design procedure equations use terms that are defined in the following subsections.

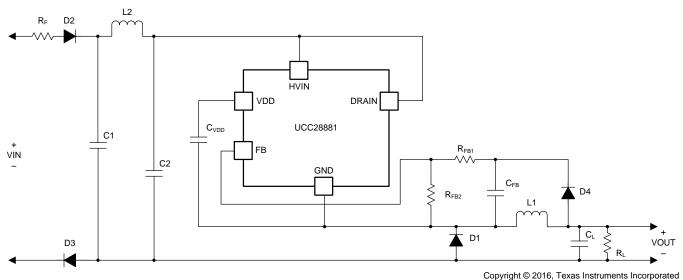


Figure 2. Universal Input, 15-V, 200-mA Output High-Side Buck

where:

- R_F—Flame proof fusible resistor. RF limits the inrush current and also provide protection in case any
 component failure causes a short circuit
- D2, D3—Half-wave rectifier diode
- C1, L2, C2-EMI filter also act as storage capacitors
- R_{FB1}, R_{FB2}—Output voltage feedback divided resister
- D1—Freewheeling diode
- C_L—Output capacitor
- R₁—Pre-load resistor
- L1—Buck inductor

(1)

4.2 Input Stage (D2, D3, C1, C2, L2)

Based on Figure 2:

- A half-wave rectifier is chosen and implemented by diode D2 and D3 (1N4007) are general purpose 1-A, 1-kV rated diode with standard reverse recovery time (> 500 ns), and is added for improved common-mode-conducted EMI noise performance. If not needed, D3 can be removed and replaced by a short.
- EMI filtering is implemented by using a single differential-stage filter (C1-L2-C2).

Capacitors C1 and C2 in the EMI filter also act as storage capacitors for the high-voltage input DC voltage (V_{IN}). The required input capacitor size can be calculated with Equation 1:

$$C_{BULK(min)} = \frac{\frac{2 \times P_{IN}}{f_{LINE(min)}} \times \frac{1}{RCT} - \frac{1}{2 \times \pi} \times \cos^{-1} \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} - \frac{1}{2 \times V_{IN(min)}^{2} - V_{BULK(min)}^{2}} \right)$$

where

- C_{BULK(min)} is minimum value for the total input capacitor value
- RCT = 1 in case of half wave rectifier and RCT = 2 in case of full-wave rectifier
- P_{IN} is the converter input power
- V_{IN(min)} is the minimum RMS value of the AC input voltage
- V_{BULK(min)} is the minimum allowed voltage value across bulk capacitor during converter operation
- $f_{LINE(min)}$ is the minimum line frequency when the line voltage is $V_{IN(min)}$

The converter input power can be easily calculated as follows:

- The converter maximum output power is $P_{OUT} = I_{OUT} \times V_{OUT} = 0.2 \text{ A} \times 15 \text{ V} = 3 \text{ W}$
- Assuming the efficiency η = 75% the input power is $P_{IN} = P_{OUT} / \eta = 4 W$

Using the following values for the other parameters:

- V_{BULK(min)} = 80 V
- $V_{IN(min)} = 85 V_{RMS}$ (from Table 1)
- $f_{\text{LINE(min)}} = 57 \text{ Hz}$
- C_{BULK(min)} = 15.6 μF

Considering those electrolytic capacitors, generally used as bulk capacitors, have 20% of tolerance in value, the minimum nominal value required for C_{BULK} is 20 µF. Select C1 and C2 to be 10 µF each. Using a full-wave rectifier allows a smaller capacitor for C1 and C2, which is almost 50% smaller.

4.3 Regulator Capacitor (C_{VDD})

Capacitor C_{VDD} acts as the decoupling capacitor and storage capacitor for the internal regulator. A 100-nF, 10-V rated ceramic capacitor is enough for proper operation of the device's internal LDO.

System Design Theory

4.4 Freewheeling Diode (D1)

The freewheeling diode has to be rated for high voltage with as short as possible reverse-recovery time (trr). The maximum reverse voltage that the diode must experience in the application, during normal operation, is given by Equation 2:

$$V_{D1(max)} = \sqrt{2} \times V_{IN(max)} = \sqrt{2} \times 265 \text{ V} = 375 \text{ V}$$

A margin of 20% is generally considered.

The use of a fast recovery diode is required for the buck-freewheeling rectifier. When designed in continuous conduction mode (CCM), the diode trr must be less than 35 ns to keep low reverse recovery current and the switching loss. For example, the STTH1R06A provides a 25-ns trr. When designed in discontinuous conduction mode (DCM), a slower diode can be used, but the trr must be kept less than 75 ns. The MURS160 can fit this requirement.

4.5 Output Capacitor (C_L)

The value of the output capacitor impacts the output ripple. Depending on the combination of capacitor value and equivalent series resistor (R_{ESR}). A larger capacitor value also has an impact on the start-up time. For a typical application, the capacitor value can start from 47 μ F to hundreds of μ F. A guide for sizing the capacitor value can be calculated by Equation 3:

$$C_{L} > 20 \times \frac{I_{LIMIT} - I_{OUT}}{f_{SW(max)} \times \Delta V_{OUT}} = 20 \times \frac{440 \text{ mA} - 200 \text{ mA}}{62 \text{ kHz} \times 350 \text{ mV}} = 220 \text{ }\mu\text{F}$$
(3)

Take into account that both C_L and R_{ESR} contribute to the output voltage ripple. Select afirst pass capacitance value and evaluate the contribution of C_L and R_{ESR} to the output voltage ripple. If the total ripple is too high, the capacitance value has to increase or R_{ESR} value must be reduced. The formula that calculates C_L is based on the assumption that the converter operates in burst of 20 switching cycles. The number of bursts per cycle could be different; the formula for C_L is a first approximation.

4.6 Pre-Load Resistor (R_L)

8

The pre-load resistor connected at the output is required for the high-side buck topology. Unlike low-side buck topology, the output voltage is directly sensed in high-side buck topology, the output is sampled and estimated.

At no-load condition, because the feedback loop runs with its own time constant, the buck converter operates with a fixed minimum switching frequency. Select the pre-load resistor or use a Zener diode to prevent the output voltage from increasing too high at no-load condition.

A simple Zener diode is be a good choice without going through the calculation. Besides simplifying the calculation, a Zener diode does not consume power at heavy-load condition, which helps to improve the heavy-load efficiency of the converter.

A simple resistor can also limit the output voltage at no-load condition. However, this resistor connects to the output all the time and it reduces the full-load efficiency. Calculate the pre-load resistor with Equation 4 or based on experiments. In Equation 4, V_{MAX} is the allowed maximum output voltage, and V_{REG} is the regulated output voltage.

$$R_{L} = \frac{4 \times V_{MAX}^{2} \times (V_{MAX} - V_{REG})}{V_{MAX} + V_{REG}} \times \frac{C_{FB} \times (R_{FB1} + R_{FB2})}{L_{1} \times I_{LIMIT}^{2}}$$
(4)

(2)



4.7 Inductor (L1)

(5)

Calculate half of the peak-to-peak ripple current at full load with Equation 5:

$$\Delta I_{L} = 2 \times (I_{LIMIT} - I_{OUT})$$

When operating in DCM, the peak-to-peak current ripple is the peak current of the device. The average MOSFET conduction minimum duty cycle at CCM is:

$$\mathsf{D}_{\mathsf{MIN}} = \frac{\mathsf{V}_{\mathsf{OUT}} + \mathsf{V}_{\mathsf{d}}}{\mathsf{V}_{\mathsf{IN}(\mathsf{max})} - \mathsf{V}_{\mathsf{d}}}$$
(6)

If the converter operates in DCM:

$$D_{MIN} = 2 \times \frac{I_{OUT}}{I_{LIMIT}} \times \frac{V_{OUT} + V_{d}}{V_{IN(max)} - V_{d}}$$
(7)

The maximum allowed switching frequency at V_{IN(max)} and full load is:

$$f_{SW_VIN(max)} = \frac{D_{MIN}}{t_{ON_TO}}$$
(8)

The switching frequency has a maximum value limit of $f_{SW(max)}$. The worst case is $I_{LIMIT} = 315$ mA, but assuming $\Delta I_L = 180$ mA. The converter works in CCM ($\Delta I_L < I_{LIMIT}$), so based on $V_{OUT} = 15$ V, $V_d = 0.5$ V and $V_{IN(max)} = 375$ V:

$$D_{MIN} = \frac{V_{OUT} + V_{d}}{V_{IN(max)} - V_{d}} = 4.13\%$$

The maximum allowed switching frequency is 62 kHz because the calculated value exceeds it.

$$f_{SW_VIN(max)} = \frac{D_{MIN}}{t_{ON_TO}} = \frac{0.0413}{450 \times 10^{-9}} = 91.7 \text{ kHz} > f_{SW(max)} = 62 \text{ kHz}$$

The duty cycle does not force the MOSFET on time to go below $t_{ON_{TO}}$. If $D_{MIN} / T_{ON_{TO}} < f_{SW(max)}$, the switching frequency is reduced by current runaway protection. If the maximum average switching frequency is lower than $f_{SW(max)}$, the converter cannot support a full load.

The minimum inductance value satisfies the following conditions:

$$L > \frac{V_{OUT} + V_{d}}{\Delta I_{L} \times f_{SW} VIN(max)} = 1 \text{ mH}$$
(9)

In the application example, 1 mH is selected as the minimum inductance value.

(11)

4.8 Feedback Path (C_{FB}, R_{FB1}, and R_{FB2})

In low-side buck converter applications, the output voltage is always sensed by the FB pin, and the UCC28881 internal controller can turn on the MOSFET on V_{OUT}. In high-side buck converter applications, the information on the output voltage value is stored on the C_{FB} capacitor. This information is not updated in real time. The information on the C_{FB} capacitor is updated just after MOSFET turnoff event. When the MOSFET is turned off, the inductor current forces the freewheeling diode to turn on and the GND pin of the UCC28881 goes negative at $-V_{d1}$ (where V_{d1} is the forward drop voltage of diode D1) with respect to the negative terminal of bulk capacitor. When D1 is on, through diode D4, the C_{FB} capacitor is charged at $V_{OUT} - V_{d4} + V_{d1}$. Set the output voltage regulation level using Equation 10:

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT_T} - V_{d4} + V_{d1} - V_{FB_TH}}{V_{FB_TH}} \cong \frac{V_{OUT_T} - V_{FB_TH}}{V_{FB_TH}}$$
(10)

where

- $V_{FB TH}$ is the FB pin reference voltage
- $V_{OUT T}$ is the target output voltage
- R_{FB1} , R_{FB2} is the resistance of the resistor divider connected with FB pin (see Figure 16)
- The capacitor C_{FB} after D1 is discharged with a time constant that is $\tau_{FB} = C_{FB} \times (R_{FB1} + R_{FB2})$

Select the time constant τ_{FB} , given in Equation 11:

$$\tau_{FB} = C_{FB} \times \left(R_{FB1} + R_{FB2} \right) = 0.1 \times C_{L} \times R_{LOAD}$$

In this equation, R_{LOAD} is the full load resistor value.

The time constant selection leads to a slight output-voltage increase in no-load or light-load conditions. In order to reduce the output-voltage increase, increase τ_{FB} . The drawback of increasing τ_{FB} is t in high-load conditions V_{OUT} could drop.

Because of the nature of sample and hold of output voltage feedback, the feedback loop components need some adjustments after the initial design. The larger time constant of the feedback components leads to lower the no-load switching frequency. As a result, the no-load standby power and light-load voltage regulation are improved.

Because of the larger time constant at a heavier load, the load regulation starts to worsen. On the contrast, decreasing the time constant makes the heavy-load regulation better but increases the no-load standby power and makes the light-load voltage regulation worse. Some trade-off is required to make the regulation and standby power. Table 2 summarizes the relationship between the feedback loop time constant and the load regulation. This can be used for an easy guideline for fine tuning the circuit performance.

FEEDBACK LOOP TIME CONSTANT (τ _{FB})	NO LOAD REGULATION	HEAVY LOAD OUTPUT VOLTAGE RIPPLE	STANDBY POWER
Increase	Better	Worse	Better
Decrease	Worse	Better	Worse

Table 2. Feedback Loop Time Constant Adjustment



5 Getting Started Hardware

5.1 Test Conditions

For the input, the power supply source (V_{IN}) can support from 85- to 270-V AC universal input. Set the input current limit of the input AC source to 1 A.

For the output, use an electronic variable load or a variable resistive load, which must be rated for ≥ 20 V and must vary the load current from 0 mA to 2 A.

5.2 Required Equipment

Use the following recommended test equipment:

- Fluke 287C (multimeter)
- Chroma 61605 (AC source)
- Chroma 63102 (DC electronic load)
- Voltech PM100 / WT210 (power analyzer)
- Tektronix DPO 3054 (oscilloscope)

5.3 Procedure

- 1. Connect input terminals (J1) of the reference board to the AC power source.
- 2. In series the power analyzer between the AC source and input of reference board.
- 3. Connect output terminals (J6) to the electronic load, maintaining correct polarity (Pin 1 is the 15-V DC output, Pin 2 is the 5-V DC output, and Pin 3 is the GND terminal).
- 4. Gradually increase the input voltage from 0 V to turn on the voltage of 85-V AC.
- 5. Turn on the load to draw current from the output terminals.
- 6. Observe the startup conditions for smooth-switching waveforms.

6 **Test Results**

The following test results are divided in multiple sections that cover the steady-state performance measurements, functional performance waveforms and test data, transient performance waveforms, thermal measurements, and conduction emission test.

6.1 Performance Data

6.1.1 Efficiency and Regulation With Load Variation

Table 3 and Table 4 show the efficiency data at 115-V AC and 230-V AC input, respectively.

V _{INAC} (V)	P _{INAC} (W)	V ₁₅ (V)	I ₁₅ (mA)	V ₅ (V)	I₅ (mA)	P _{out} (W)	EFFICIENCY (%)
115	0.49	16.54	14.3	5.05	23.6	0.36	72.60
115	0.94	15.33	29.3	5.06	49.6	0.70	74.47
115	1.34	14.97	44.3	5.06	74.4	1.04	77.58
115	1.75	14.77	59.3	5.06	98.6	1.38	78.57
115	2.18	14.66	74.3	5.06	123.9	1.72	78.74
115	2.60	14.56	89.3	5.06	150.1	2.06	79.23
115	3.00	14.51	104.3	5.06	173.4	2.39	79.70
115	3.50	14.47	119.3	5.06	198.9	2.73	78.08

Table 3. Efficiency Data Under 115-V AC Input	Table 3. E	fficiency	Data	Under	115-V	AC Input
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Table 4. Efficiency Data Under 230-V AC Input

V _{INAC} (V)	P _{INAC} (W)	V ₁₅ (V)	I ₁₅ (mA)	V ₅ (V)	l₅ (mA)	Р _{оит} (W)	EFFICIENCY (%)
230	0.50	16.59	14.3	5.05	23.6	0.36	71.29
230	0.95	15.36	29.3	5.06	49.6	0.70	73.80
230	1.35	14.99	44.3	5.06	74.6	1.04	77.17
230	1.78	14.77	59.3	5.06	99.1	1.38	77.37
230	2.18	14.67	74.3	5.06	123.9	1.72	78.76
230	2.60	14.58	89.3	5.06	150.1	2.06	79.29
230	3.00	14.52	104.3	5.06	173.4	2.39	79.73
230	3.50	14.48	119.3	5.06	198.9	2.73	78.13



6.1.2 Efficiency and Regulation With Load Variation

Table 5 and Table 6 show the load regulation of a 15-V output under 230-V AC input and 115-V AC input, respectively.

V _{INAC} (V)	P _{INAC} (W)	V ₁₅ (V)	I ₁₅ (mA)	V ₅ (V)	I₅ (mA)	Р _{оит} (W)	EFFICIENCY (%)
230	0.27	19.32	0	5.06	0	0	0
230	0.38	17.46	0	5.06	49.6	0.25	66.06
230	0.70	15.83	0	5.06	99.1	0.50	71.65
230	1.04	15.25	0	5.06	150.1	0.76	73.04
230	1.37	14.97	0	5.06	199.6	1.01	73.74
230	0.65	16.01	29.3	5.06	0	0.47	72.17
230	1.15	15.13	59.3	5.06	0	0.90	78.02
230	1.68	14.81	89.3	5.06	0	1.32	78.73
230	2.20	14.66	119.3	5.06	0	1.75	79.52
230	0.95	15.36	29.3	5.06	49.6	0.70	73.80
230	1.80	14.77	59.3	5.06	99.1	1.38	76.51
230	2.60	14.58	89.3	5.06	150.1	2.06	79.29
230	3.50	14.47	119.3	5.06	199.5	2.74	78.16

Table 5. Load Regulation of 15-V Output Under 230-V AC Input

Table 6. Load Regulation of 15-V Output Under 115-V AC Input

V _{INAC} (V)	P _{INAC} (W)	V ₁₅ (V)	I ₁₅ (mA)	V ₅ (V)	I₅ (mA)	P _{out} (W)	EFFICIENCY (%)
115	0.24	19.31	0	5.06	0	0	0
115	0.37	17.39	0	5.06	49.6	0.25	67.84
115	0.69	15.78	0	5.06	99.1	0.50	72.69
115	1.03	15.21	0	5.06	150.1	0.76	73.75
115	1.36	14.94	0	5.06	199.5	1.01	74.24
115	0.62	15.96	29.3	5.06	0	0.47	75.42
115	1.14	15.10	59.3	5.06	0	0.90	78.55
115	1.70	14.79	89.3	5.06	0	1.32	77.69
115	2.20	14.65	119.3	5.06	0	1.75	79.45
115	0.94	15.33	29.3	5.06	49.6	0.70	74.47
115	1.80	14.75	59.3	5.06	99.1	1.38	76.45
115	2.60	14.56	89.3	5.06	150.1	2.06	79.23
115	3.50	14.45	119.3	5.06	199.5	2.73	78.10



Test Results

6.2 Performance Curves

6.2.1 Efficiency Curves

Figure 3 shows the efficiency with load variation.

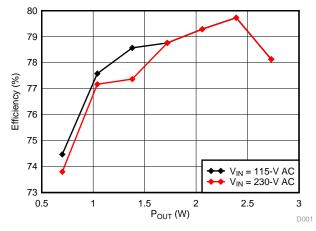


Figure 3. Efficiency With Load Variation

6.2.2 Load Regulation

Figure 4 shows the measured regulation of the 15-V output with load variation.

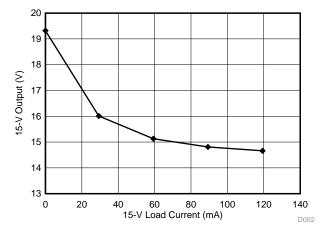


Figure 4. Load Regulation of 15-V Output Under 230-V AC Input

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6.3 **Functional Waveforms**

6.3.1 Start-up and Shutdown Waveform

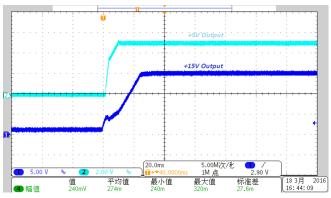


Figure 5. Start-up With 85-V AC Input and 5-V/0.2-A Output

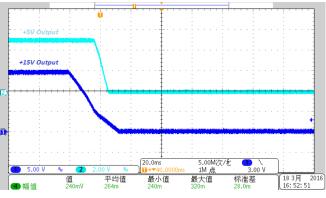


Figure 7. Shutdown With 85-V AC Input and Full Load

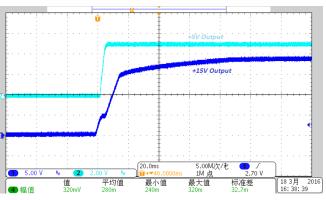


Figure 6. Start-up With 270-V AC Input and No Load

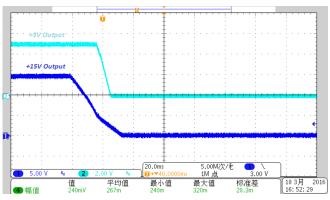


Figure 8. Shutdown With 270-V AC Input and Full Load



Test Results

6.3.2 Output Ripple

As Figure 9 and Figure 10 show, the ripple was observed at a 5-V DC output with no load and full load. Figure 11 and Figure 12 were observed at a 15-V DC output with no load and full load.

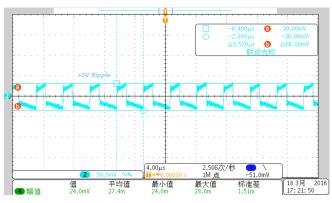


Figure 9. 5-V Output Ripple Under Full Load

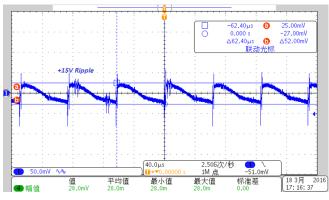


Figure 11. 15-V Output Ripple Under Full Load

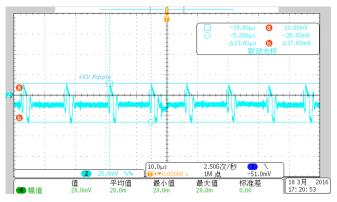


Figure 10. 5-V Output Ripple With No Load

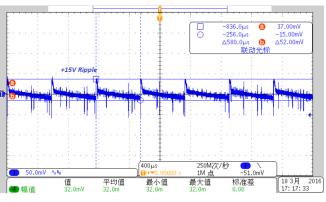
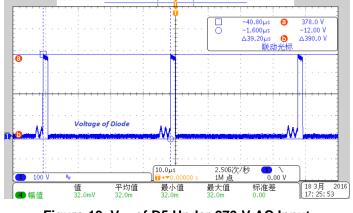
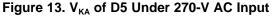


Figure 12. 15-V Output Ripple With No Load

6.3.3 Switching Node Waveform

Figure 13 shows the waveform at the switching node with a 270-V AC input and full-load conditions.







6.3.4 **Transient Waveform**

The load transient performance was observed with the load switched at a 0.2-m wire length. The output load is switched using an electronic load.

Figure 14 and Figure 15 show the load transient waveforms for V_{IN} = 230-V AC and a step-load transient from no load to full load at a 5-V output. Figure 16 show the load transient waveforms for V_{IN} = 230-V AC, and Figure 17 shows a step-load transient from no load to full load at a 15-V output.

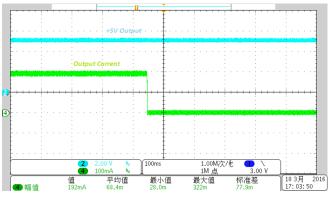


Figure 14. 5-V Output Transient Response From Full Load to No Load

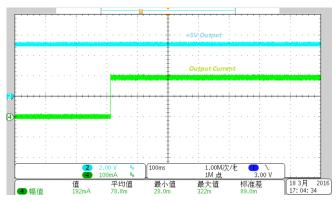


Figure 15. 5-V Output Transient Response From No Load to Full Load

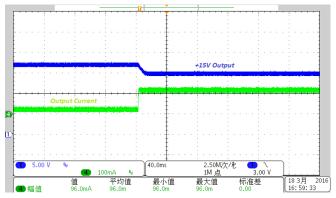


Figure 16. 15-V Output Transient Response From Full Load to No Load

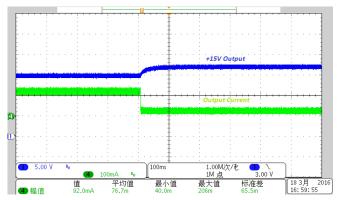


Figure 17. 15-V Output Transient Response From No Load to Full Load

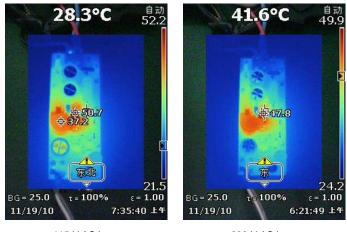


Test Results

6.4 Thermal Measurements

To better understand the temperature of power components and maximum possible operating temperature, the thermal images were plotted at room temperature (25°C) with a closed enclosure, no airflow, and at full-load conditions. The board was allowed to run for 30 minutes before capturing a thermal image.

Figure 18 shows the temperature of the power components at an input voltage of 115- and 230-V AC with the full-load output.



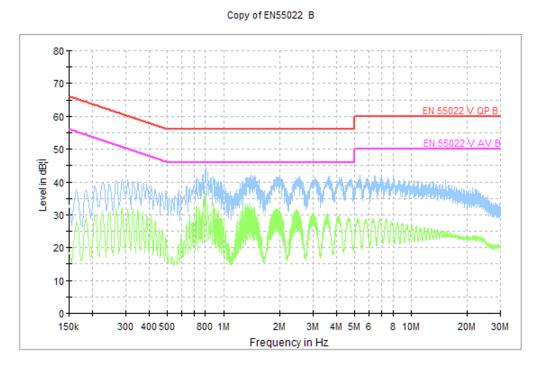
115-V AC input

230-V AC input

Figure 18. Top-Side Temperatures Test Under Full Load

6.5 Conducted Emission Test Results

Figure 19 shows the test results and the board passes the EN-55022 class B limits with more than a 15-dB margin.







7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00940.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00940.

7.3 Layout Prints

To download the layer plots, see the design files at TIDA-00940.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00940.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00940.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00940.

8 References

1. Texas Instruments, UCC28180 Programmable Frequency, Continuous Conduction Mode (CCM), Boost Power Factor Correction (PFC) Controller, UCC28180 Datasheet (SLUSBQ5)

9 About the Author

YUAN (JASON) TAO is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Yuan brings to this role his extensive experience in power electronics, high-frequency DC-DC, AC-DC converter, and analog circuit design. Yuan earned his master of IC design & manufacture from Shanghai Jiao Tong University in 2007.

Design Files



Revision A History

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Ch	anges from Original (May 2016) to A Revision	Pag	je
•	Changed from preview page		1

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