# PMP8671RevB2 Test Results

Texas Instruments

Topology: SEPIC
Device: TPS40210

This sepic design works w/ high switching frequency Fsw close to 400kHz (measured 394kHz) and ultrafast optiMOS on universal board PCB 2773B. Using a layout rooted w/ polygons will improve switching performance, will reduce EMI. The proposal for this layout as follows (noncoupled inductors):

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TEXAS
INSTRUMENTS
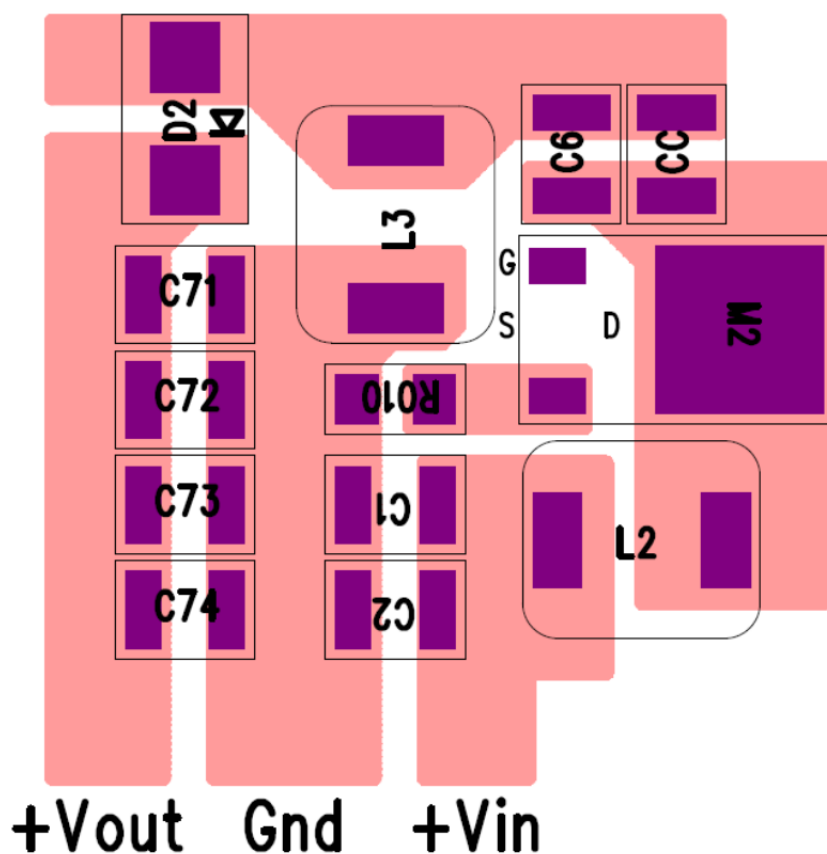
1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 5V, with 1A load at the output.

Ch1=> input voltage 2V/div

Ch2=> output voltage 2V/div

10ms/div

20MHz bw
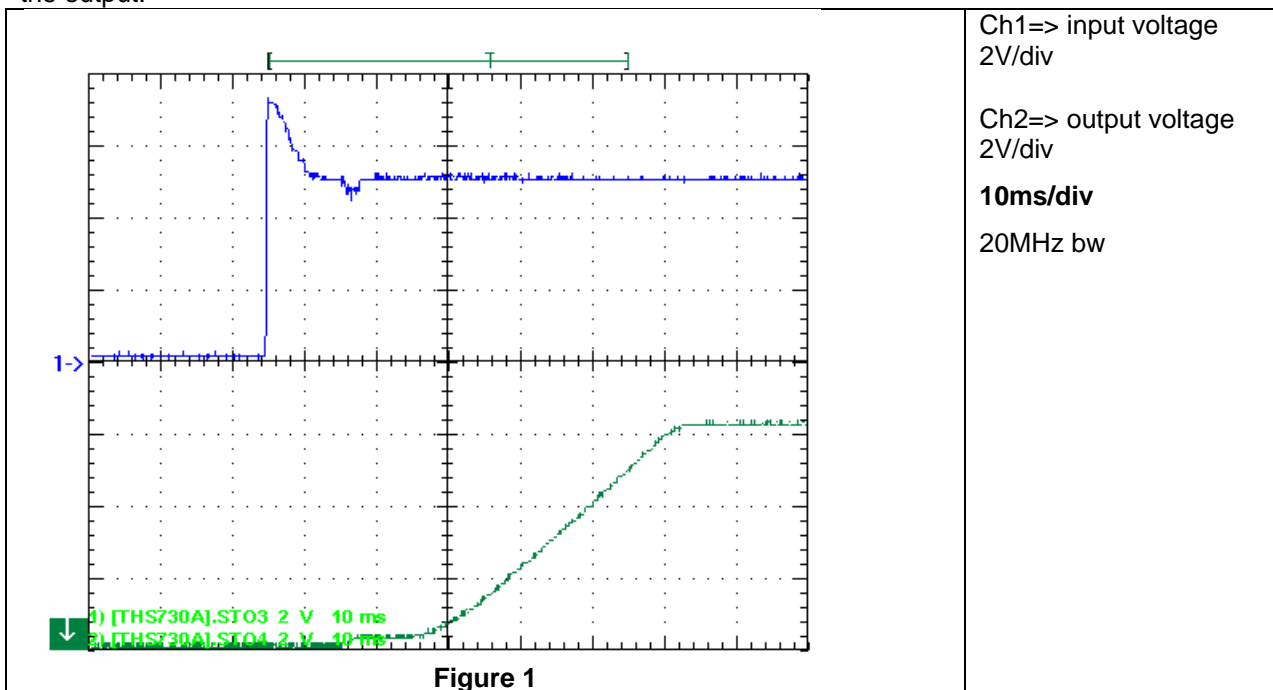
Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set at 13.8V, with 1.2A load at the output.

Ch1=> input voltage 5V/div

Ch2=> output voltage 2V/div

5ms/div

20MHz bw

Figure 2

Power Management Solutions
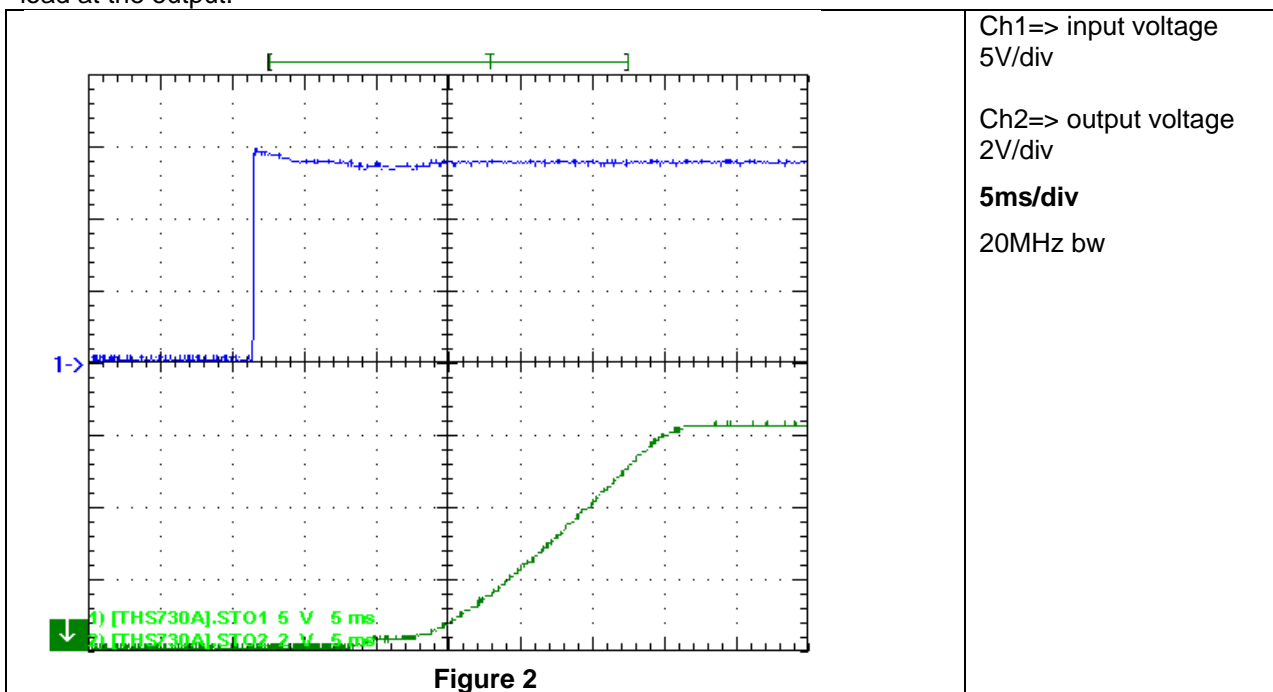
2   Shutdown

The shutdown waveform is shown in the Figure 3. The input voltage was set at 3V, with 1A load on the output. The power supply was switched off.

	Ch1=> input voltage 1V/div
	Ch2=> output voltage 2V/div
	1ms/div
	20MHz bw
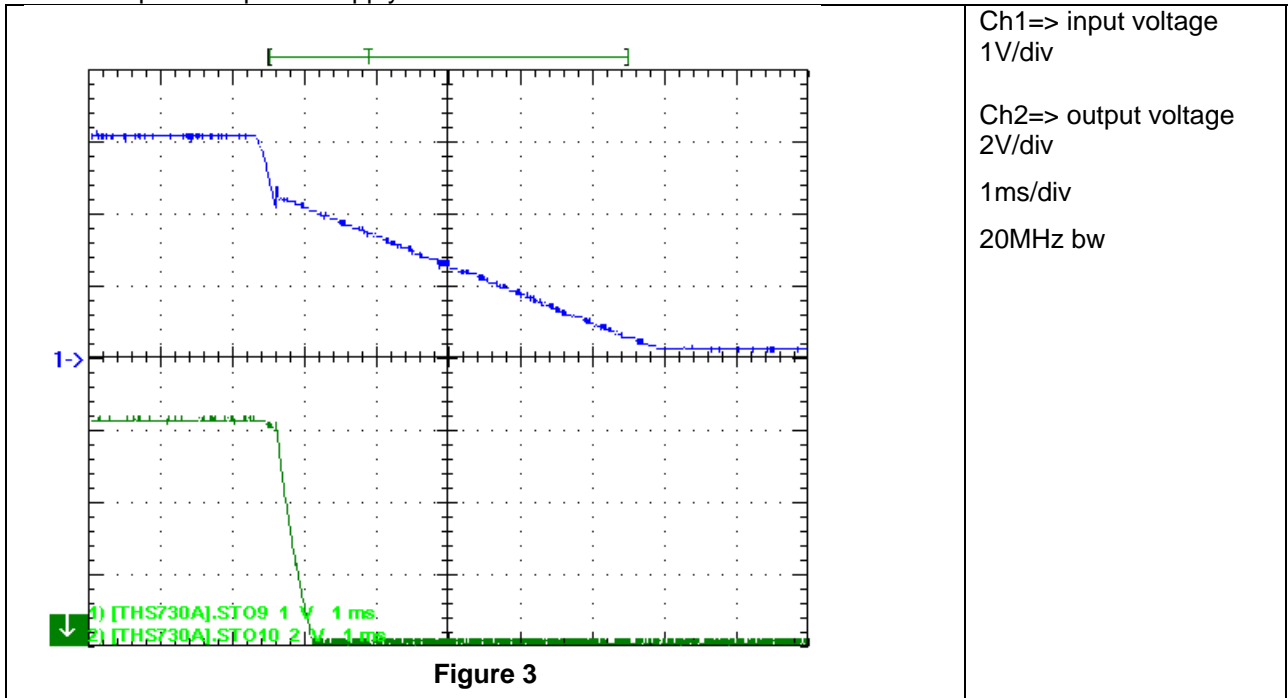
Figure 3

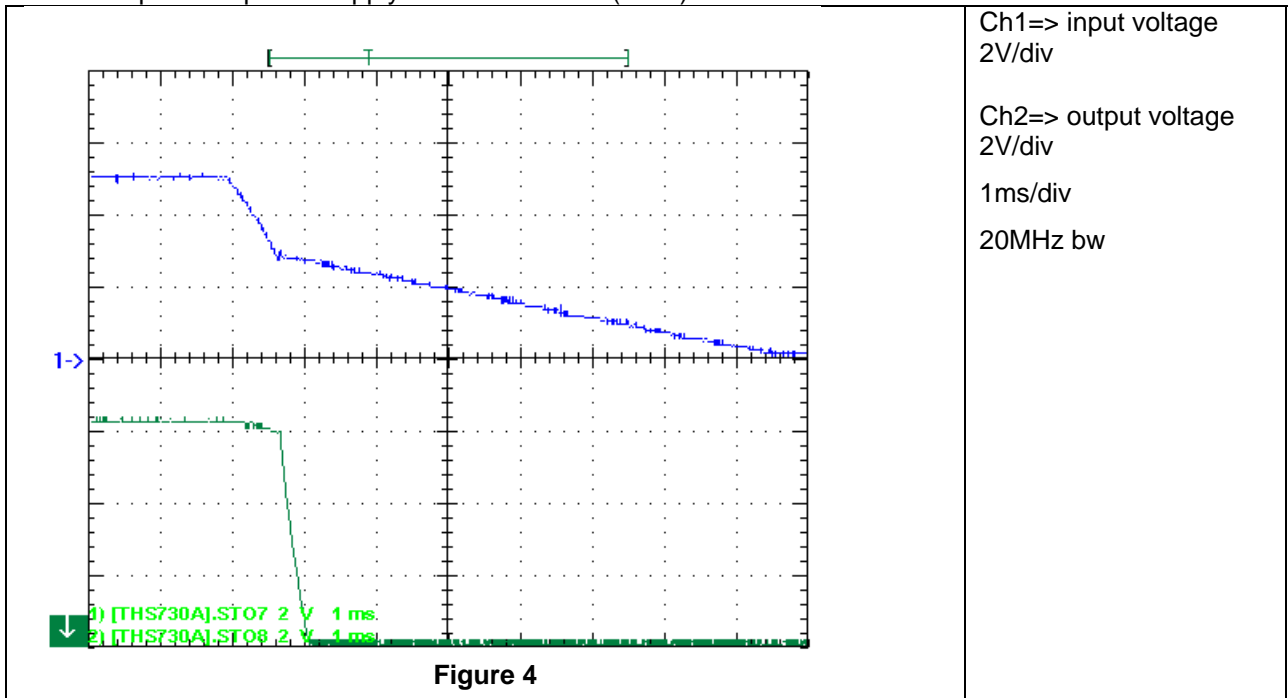The shutdown waveform is shown in the Figure 4. The input voltage was set at 5V, with 1.2A load on the output. The power supply was switched off (short).

	Ch1=> input voltage 2V/div
	Ch2=> output voltage 2V/div
	1ms/div
	20MHz bw

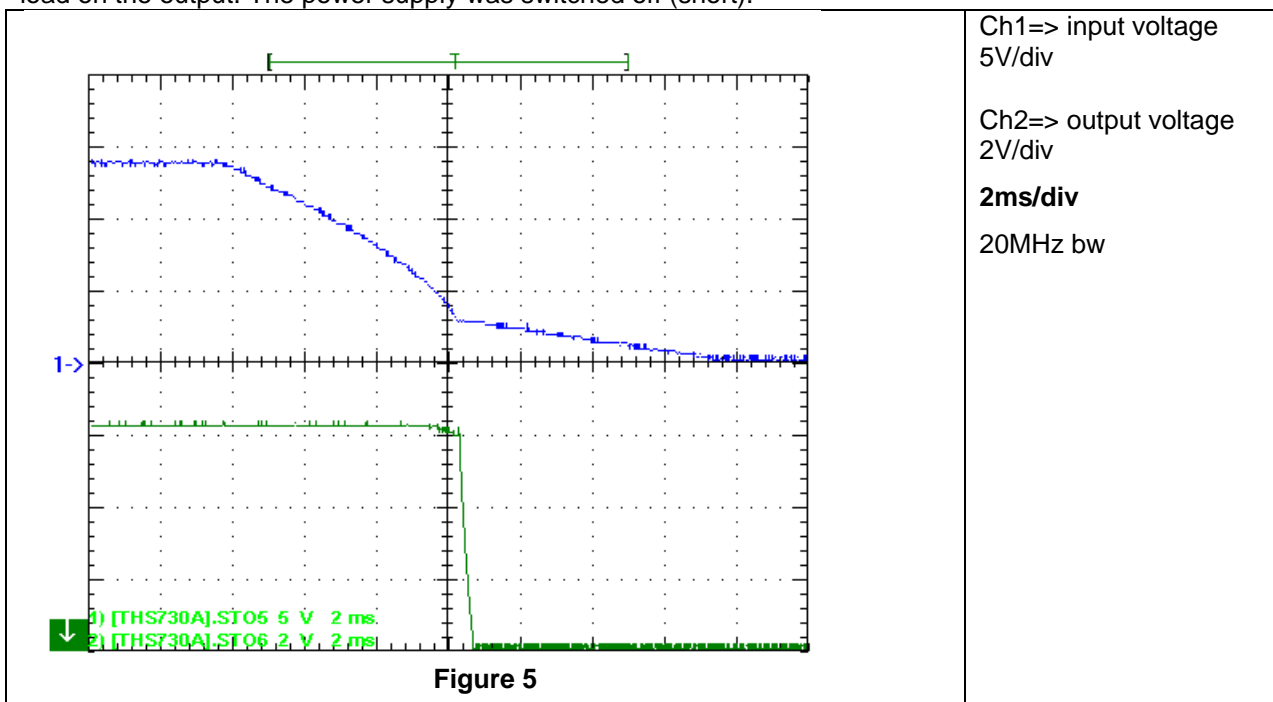**Figure 4**

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The shutdown waveform is shown in the Figure 5. The input voltage was set at 13.8V, with 1.2A load on the output. The power supply was switched off (short).

	Ch1=> input voltage 5V/div Ch2=> output voltage 2V/div **2ms/div** 20MHz bw
Figure 5	

3 Efficiency

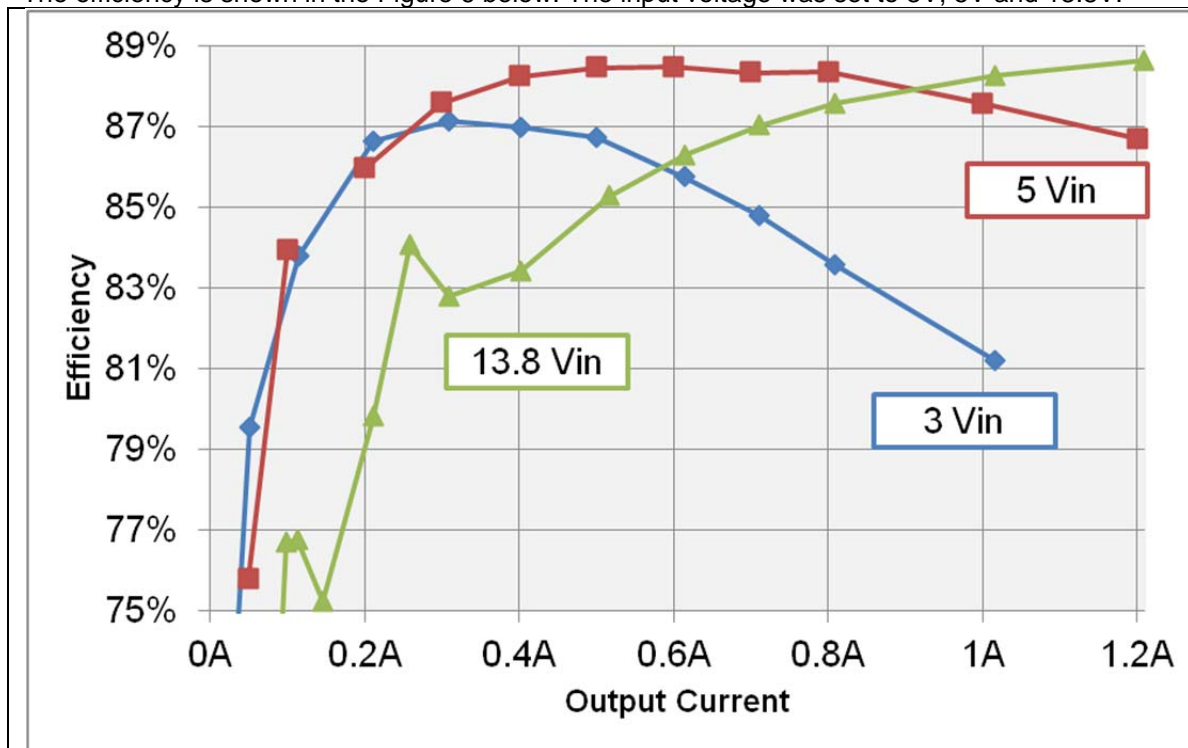The efficiency is shown in the Figure 6 below. The input voltage was set to 3V, 5V and 13.8V.

Figure 6

The design could handle 1.2Amps load at input 3V statically, current limitation trips hard at 1.2Amps load.

4   Load Regulation

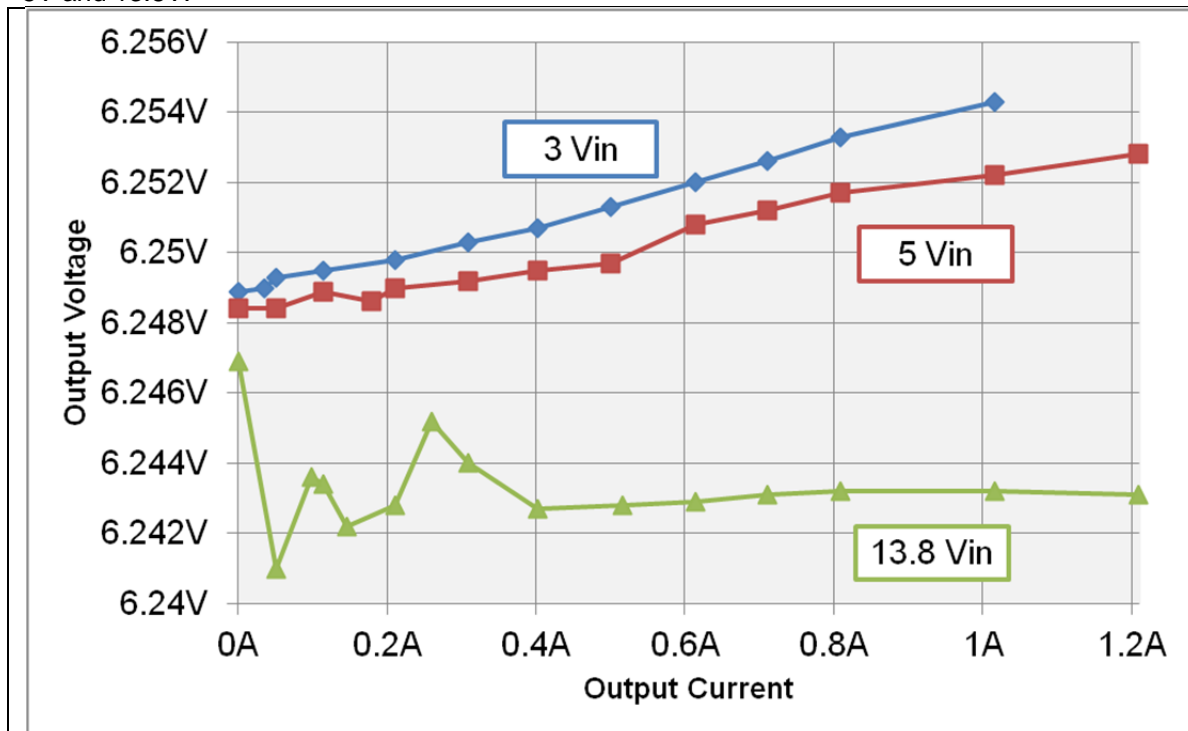The load regulation of the output is shown in the Figure 7 below. The input voltage was set to 3V, 5V and 13.8V.

Figure 7

5   Line Regulation

The line regulation is shown in Figure 8. The output current was set about 1A.

Figure 8

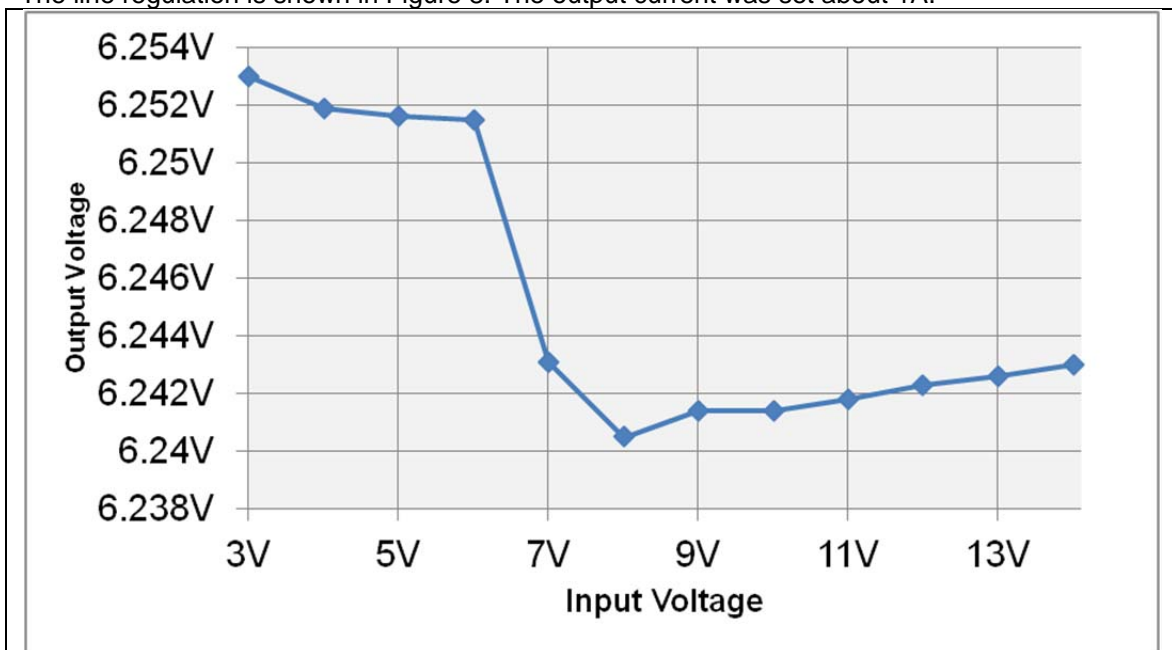With the same setup the efficiencies are shown in Figure 9.

Figure 9

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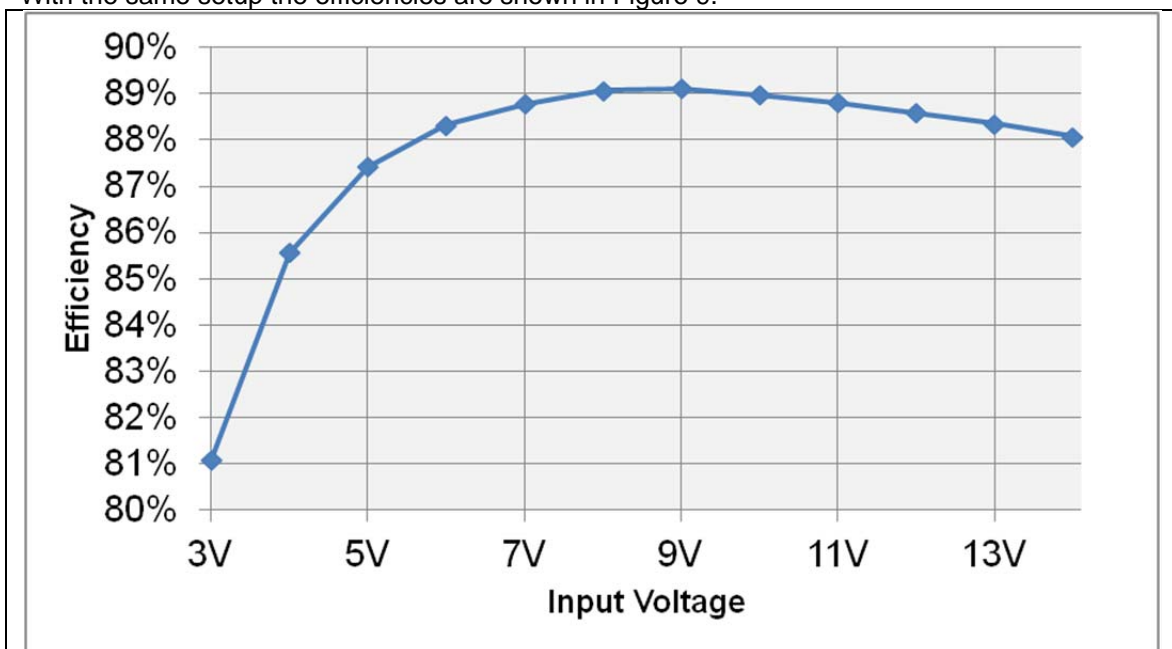
6   Output Ripple Voltage

The output ripple voltage is shown in Figure 10.

	Ch1 => output voltage@13.8 Vin/1.2Aout
	Ch2 => output voltage@5Vin/ 1.2Aout
	Ch3 => output voltage@3Vin/ 1.0Aout
	Vin 50mV/div
	AC coupled
	20MHz bw
	1µs/div
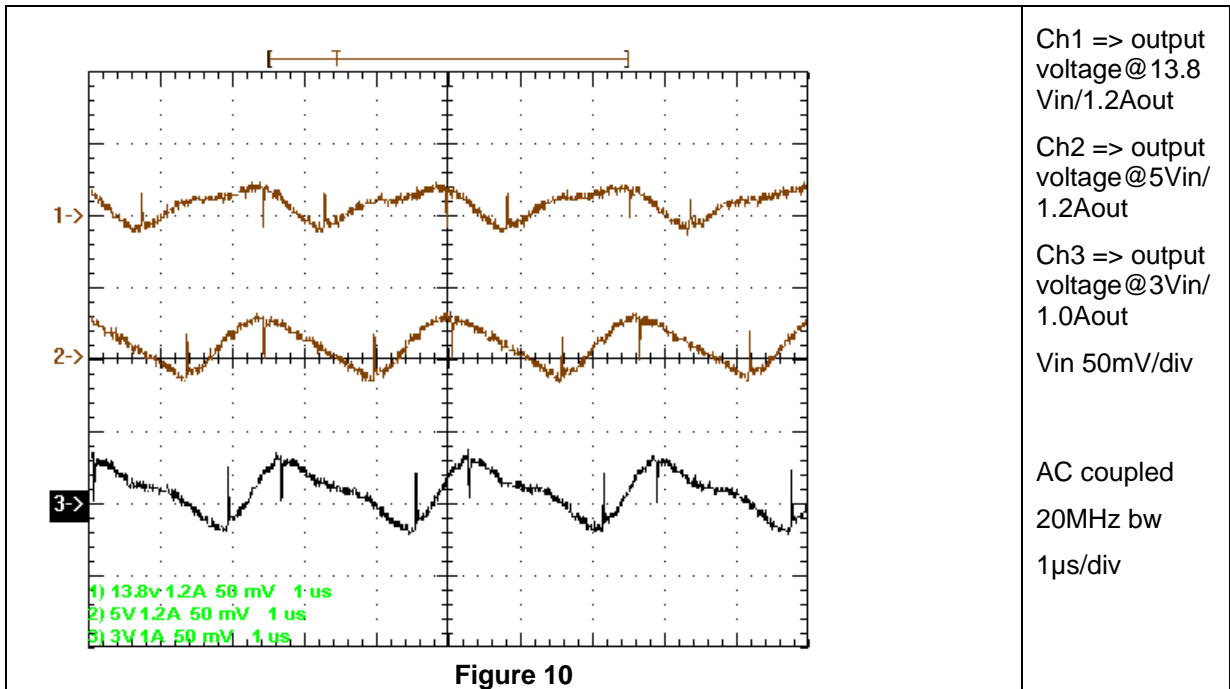
Figure 10

7 Load Transients

The Figure 11 shows the response to load transients. The load is switching from 0.5A to 1A with a frequency of 100Hz. The input voltage was set to 3V

Ch1 => output voltage
200mV/div

20MHz bandwidth setting

Ch2 => output current 500mA/div

2ms/div

Figure 11

The Figure 12 shows the response to load transients. The load is switching from 0.6A to 1.2A with a frequency of 100Hz. The input voltage was set to 5V

Ch1 => output voltage
100mV/div

20MHz bandwidth setting
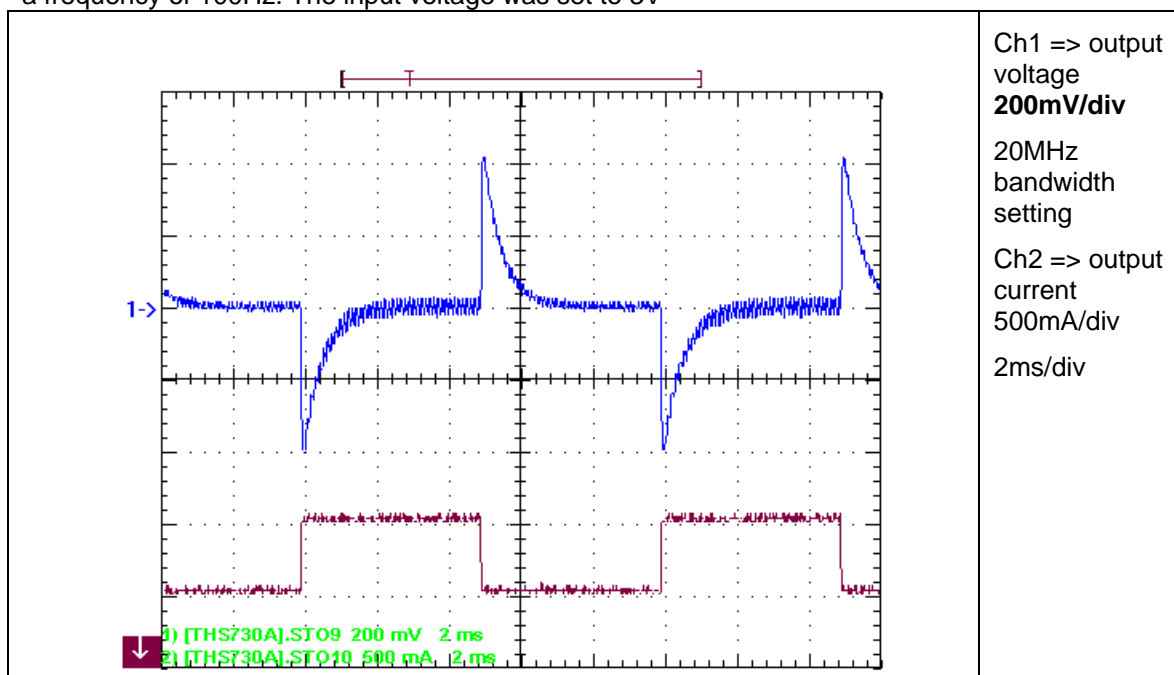
Ch2 => output current 500mA/div

2ms/div

Figure 12

The Figure 13 shows the response to load transients. The load is switching from 0.6A to 1.2A with a frequency of 100Hz. The input voltage was set to 13.8V
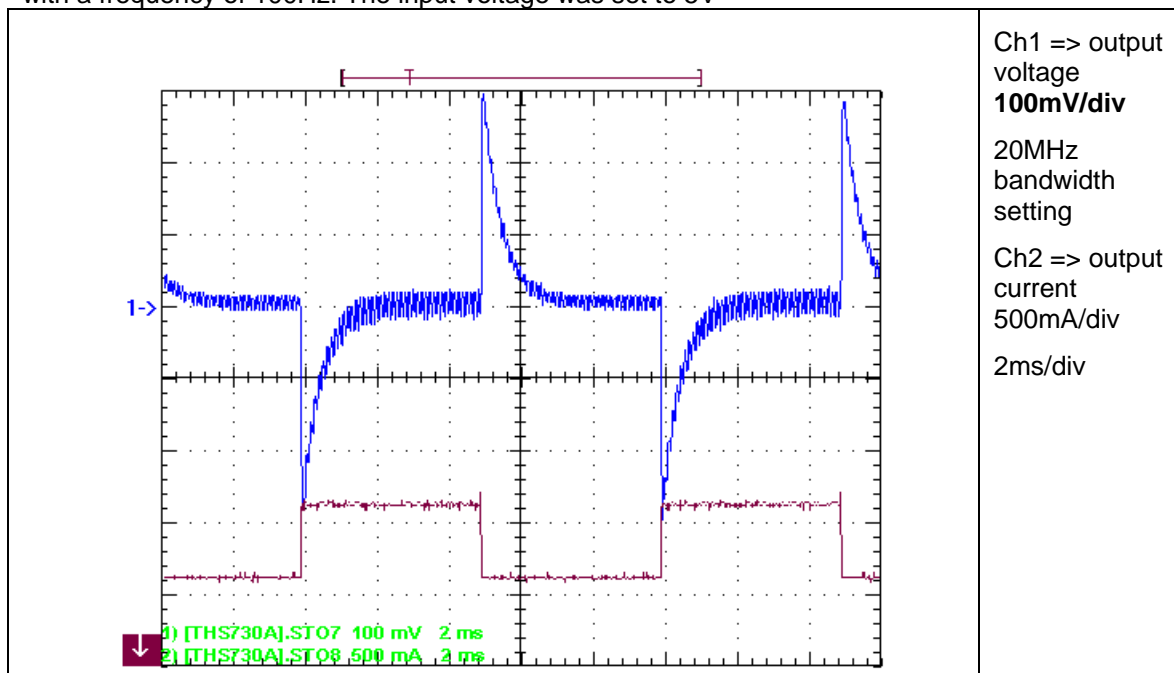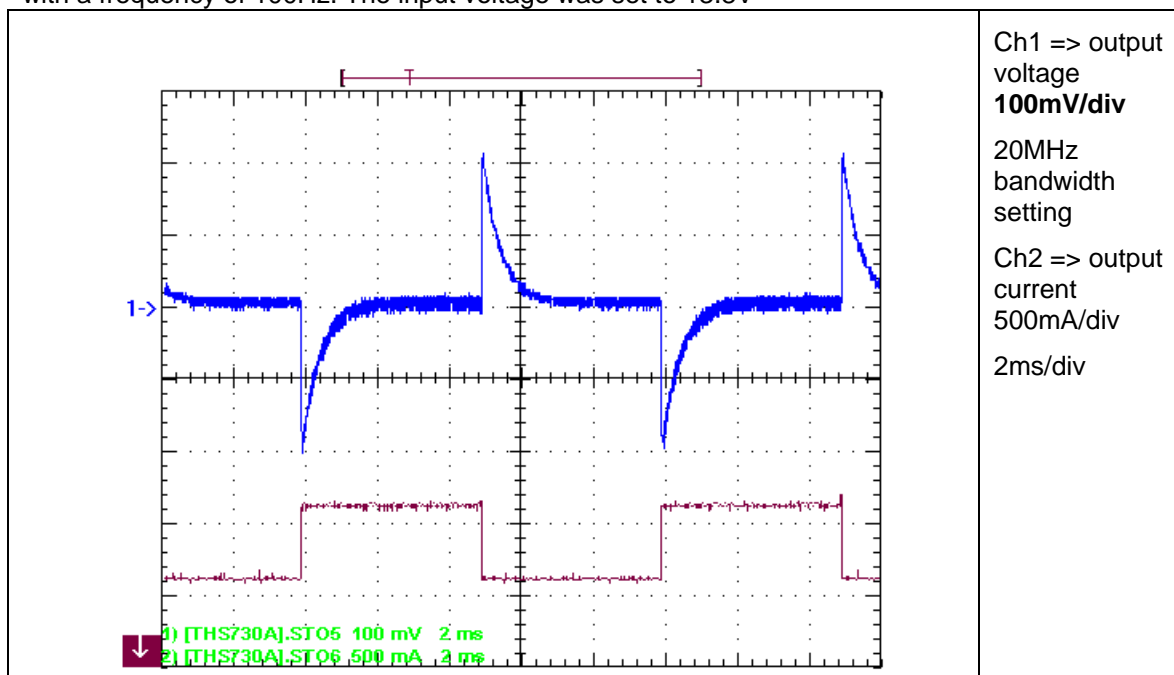

Ch1 => output voltage
100mV/div

20MHz bandwidth setting

Ch2 => output current 500mA/div

2ms/div
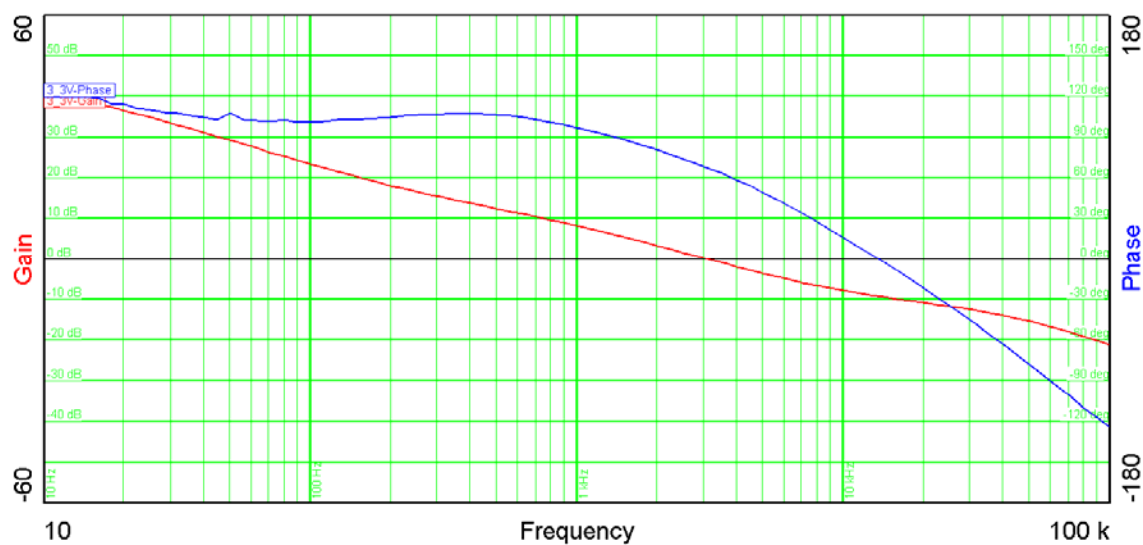
Figure 13

Due to the small output capacitance the dynamic performance is limited; transient response at large signal analysis shows du 400mV, so 6.4% worst case on standard transient 50%.
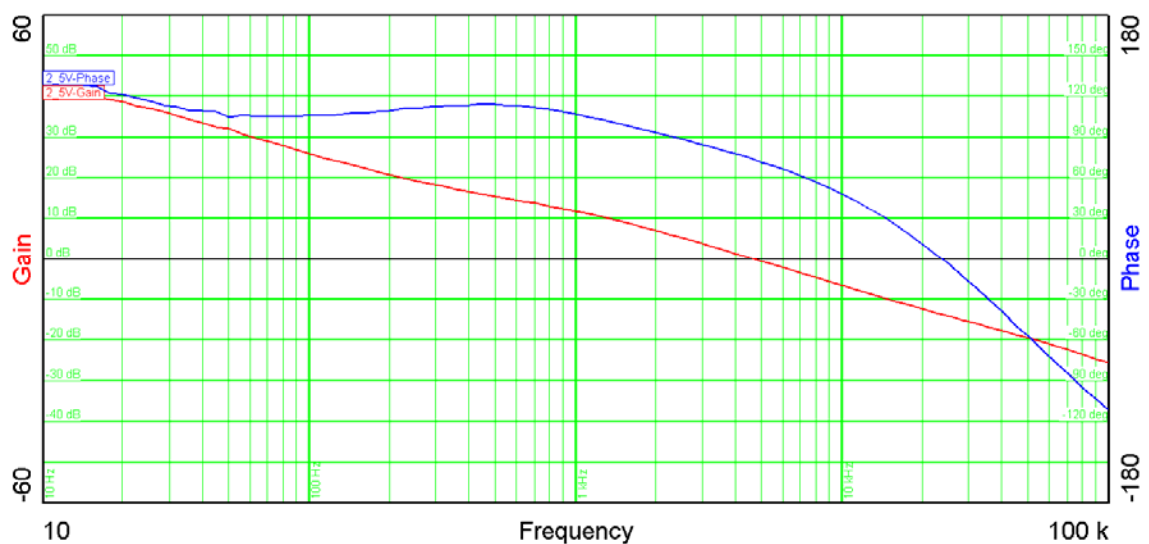For nominal input 13.8V the deviation is 210mV, so 3.36%.

8 Control Loop Frequency Response

Figure 14 shows the loop response. 1A-load applied. The input voltage was set to 3V.
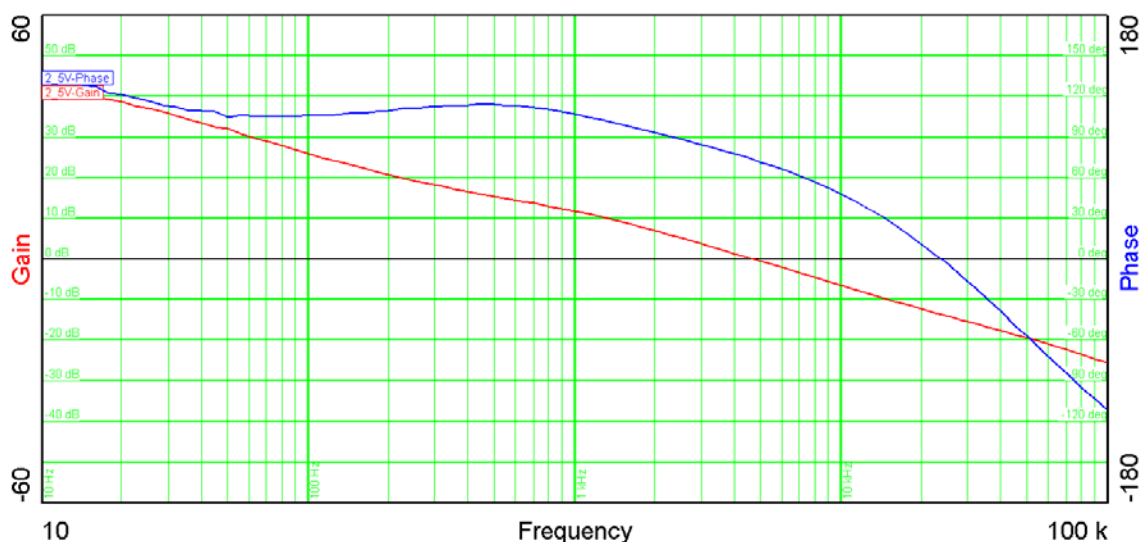

Figure 14

Figure 15 shows the loop response. 1.2A-load applied. The input voltage was set to 5V.

Figure 15

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Figure 16 shows the loop response. 1.2A-load applied. The input voltage was set to 13.8V.

Figure 16

Table 1 summarizes the results from Figure 14 Figure 15 and Figure 16.

Vin	3V	5V	13.8V
Bandwidth (kHz)	3.08	4.7	7
Phase margin	67.7°	73.6	71.5
slope (20dB/decade)	-0.89	-1	-1
gain margin (dB)	-9.2	-13.7	-17.2
slope (20dB/decade)	-0.493	-0.9	-1.6
freq (kHz)	13.6	23.7	34.7

Table 1

Due to small output capacitance the bandwidth was tuned to a maximum of 3kHz at minimum input voltage (=maximum duty cycle). That's the limit by RHPZ.

9 Miscellaneous Waveforms

The waveform of the voltage on switchnode is shown in Figure 17. Input voltage was set to 3V and output current to 1A.

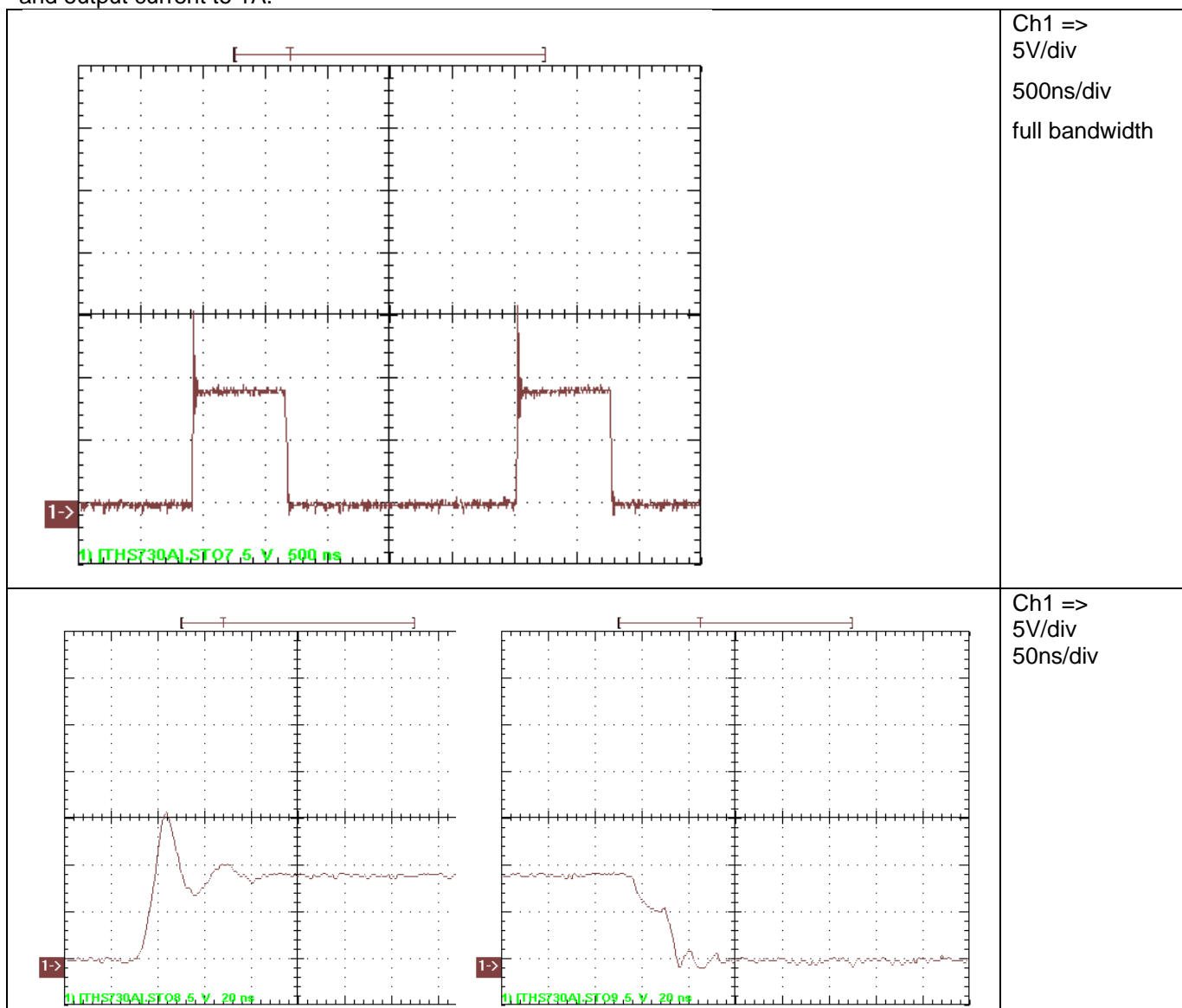**Figure 17**

The waveform of the voltage on the gate to ground is shown in Figure 18. Input voltage was set to 3V and output current to 1A.

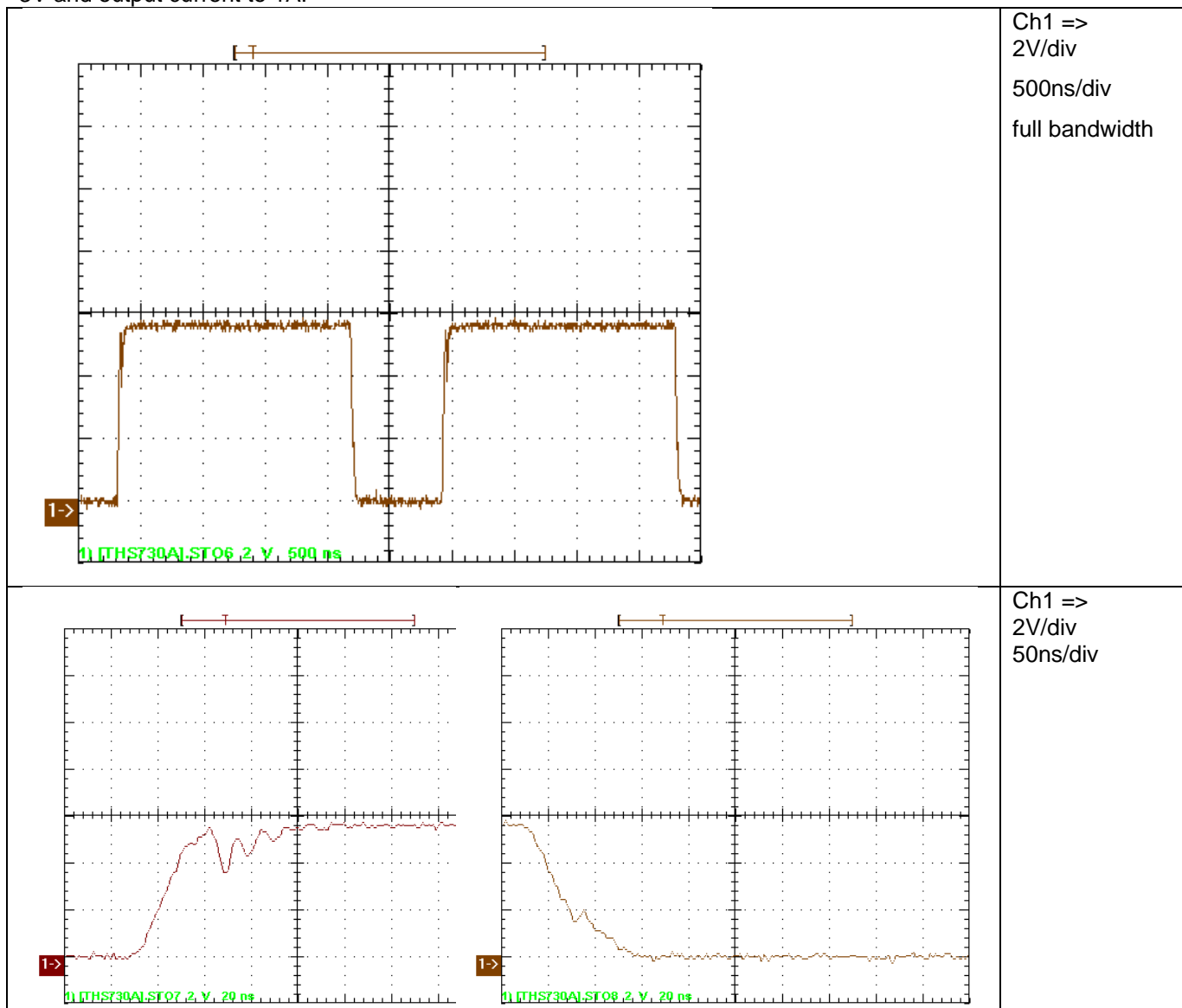|	Ch1 => 2V/div
	500ns/div
	full bandwidth

Ch1 => 2V/div
50ns/div

Figure 18

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The waveform of the voltage on switchnode is shown in Figure 19. Input voltage was set to 5V and output current to 1A.
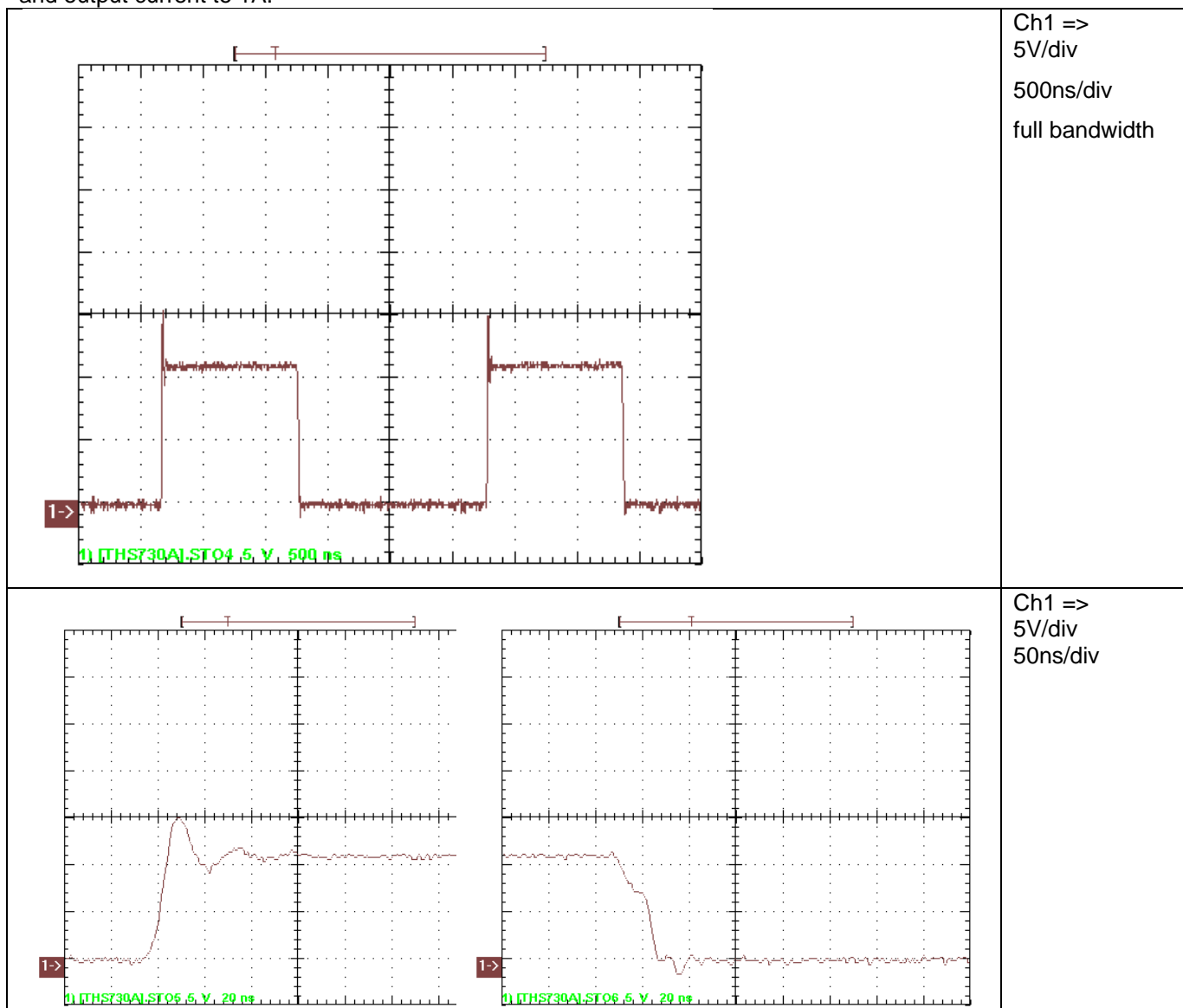
	Ch1 => 5V/div
	500ns/div
	full bandwidth

Figure 19

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The waveform of the voltage on the gate to ground is shown in Figure 20. Input voltage was set to 5V and output current to 1A.

	Ch1 => 2V/div
	500ns/div
	full bandwidth
	Ch1 => 2V/div 50ns/div

Figure 20

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The waveform of the voltage on switchnode is shown in Figure 21. Input voltage was set to 13.8V and output current to 1A.
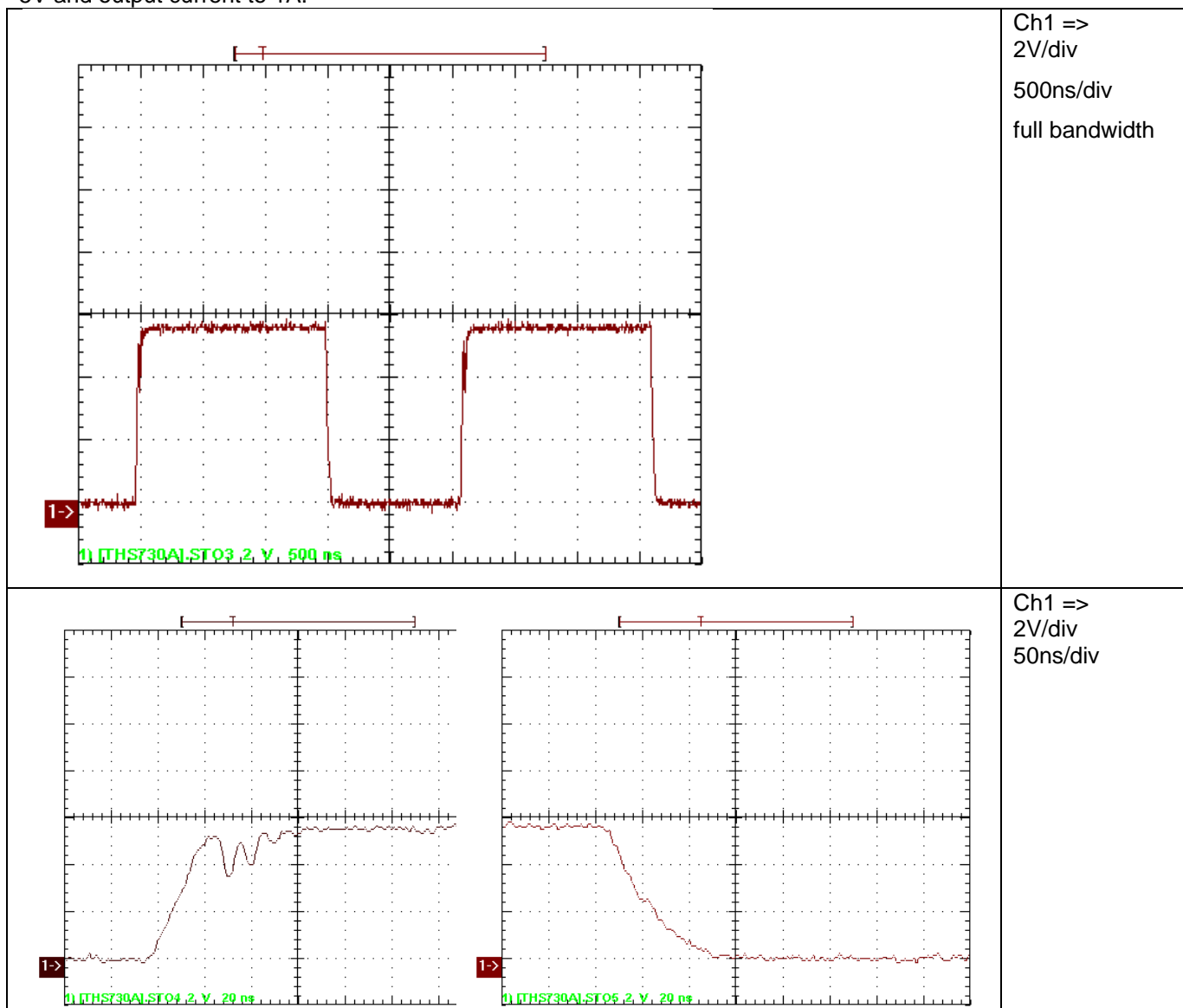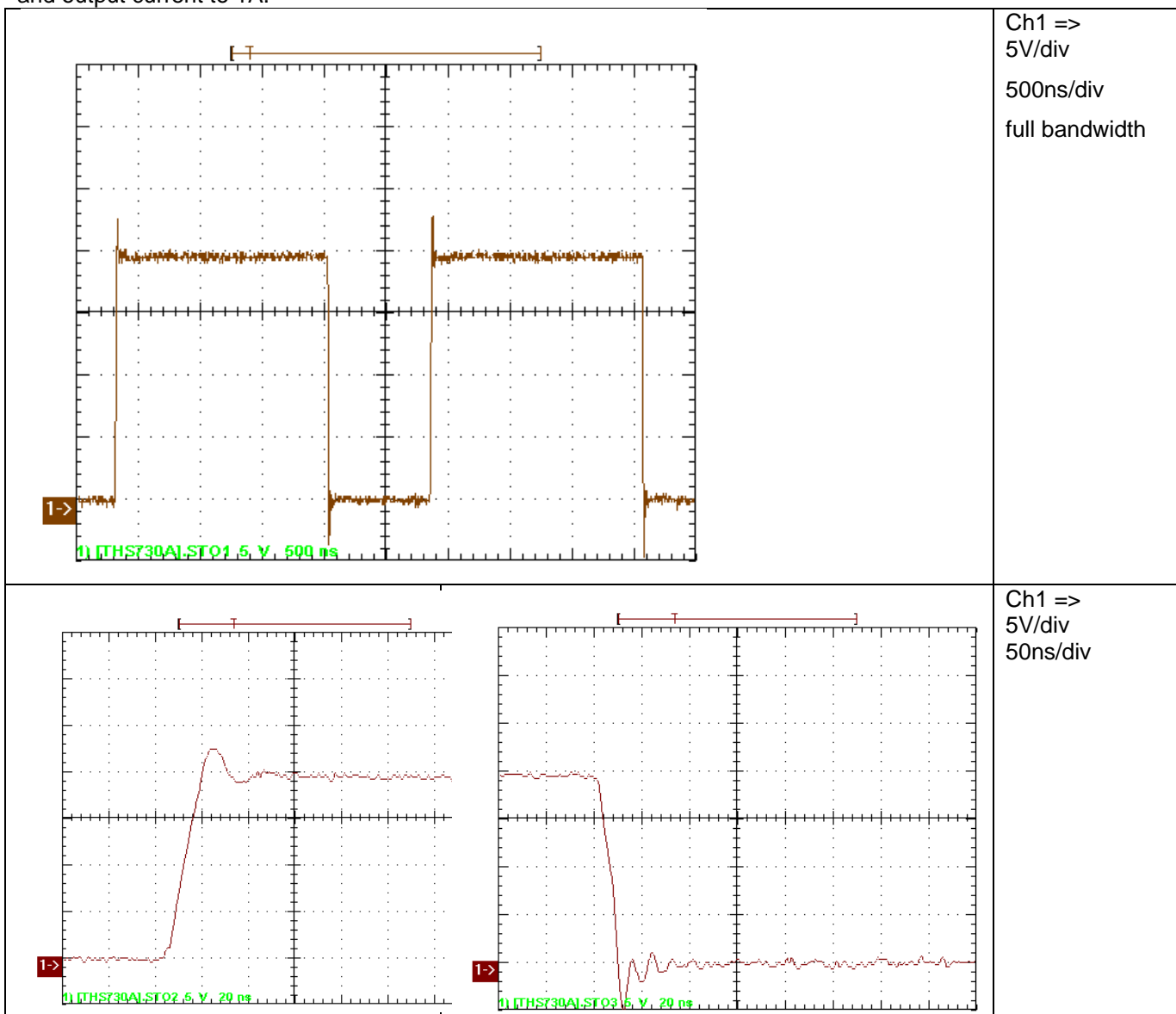

Ch1 =>
5V/div

500ns/div

full bandwidth

Ch1 =>
5V/div
50ns/div

Figure 21

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The waveform of the voltage on the gate to ground is shown in Figure 22. Input voltage was set to 13.8V and output current to 1A.

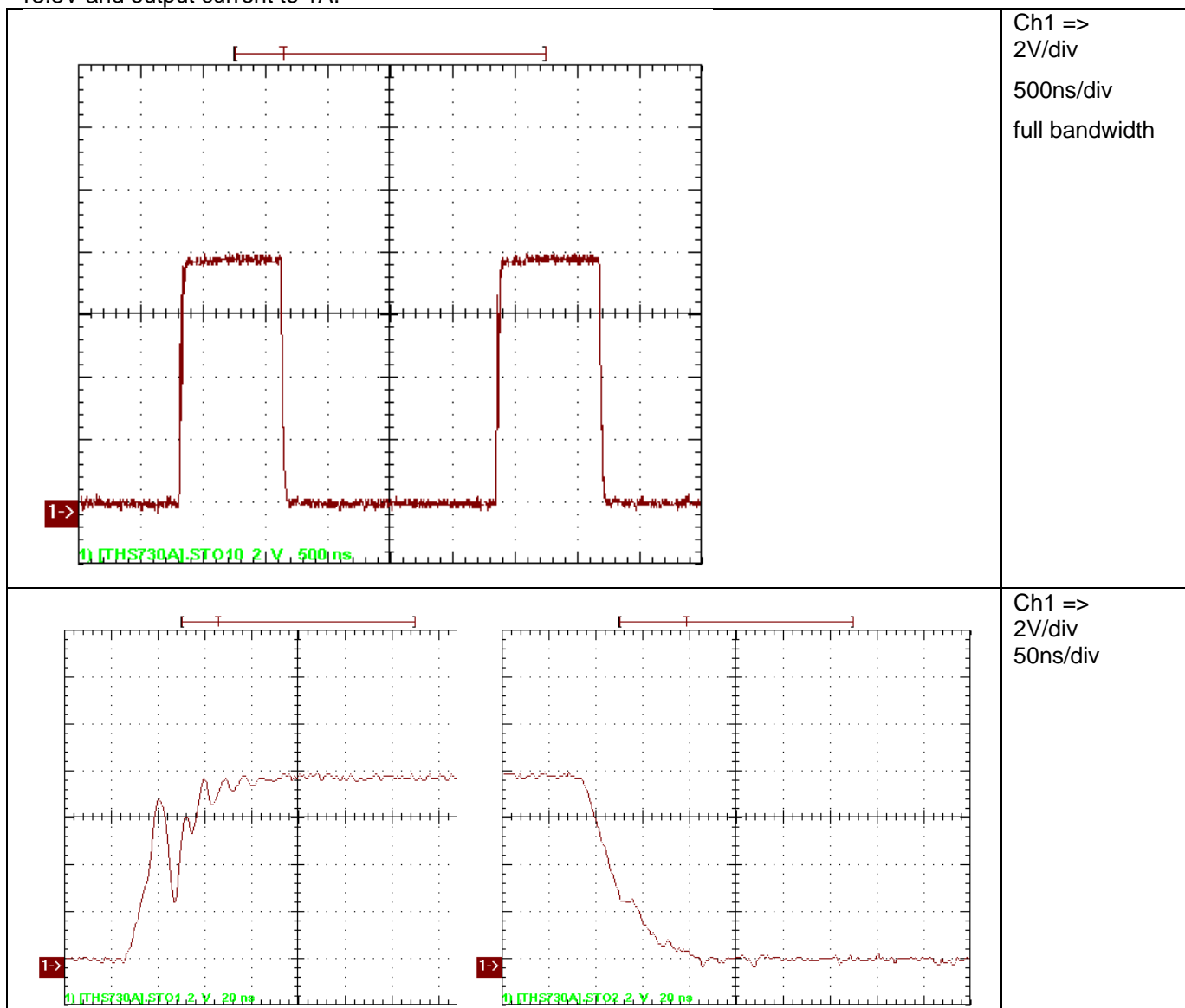|	Ch1 => 2V/div
	500ns/div
	full bandwidth
	Ch1 => 2V/div 50ns/div

Figure 22

10 Thermal Image

Figure 23 shows the thermal image at 3V input voltage and 1.2A maximum output current.
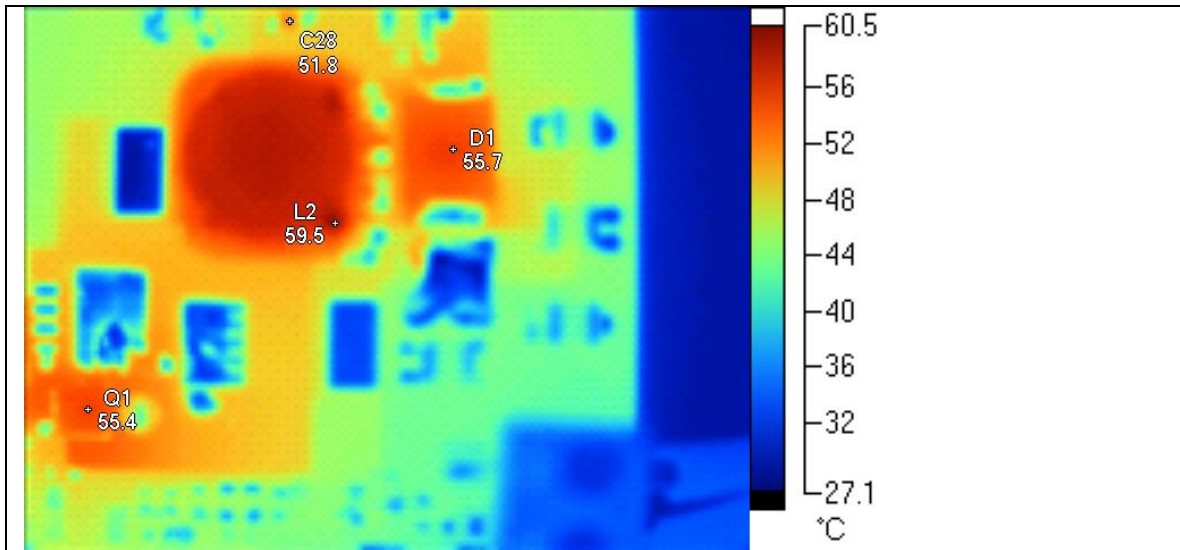

Figure 23

Name	Temperature
L2	59.5°C
Q1	55.4°C
D1	55.7°C
C28	51.8°C

Figure 24 shows the thermal image at 13.8V input voltage and 1.2A output current.
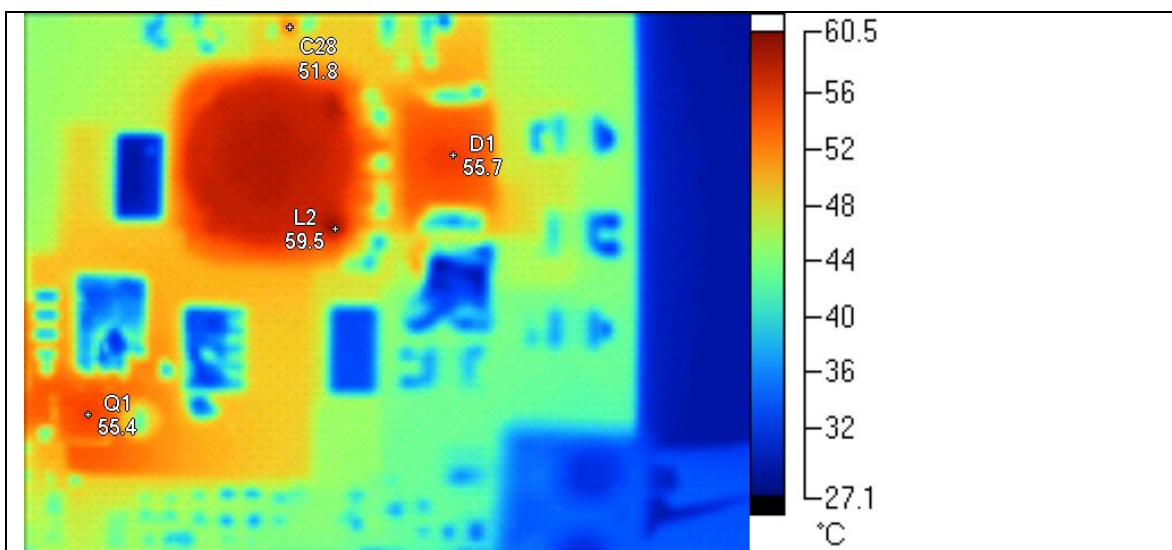

Figure 24

Name	Temperature
D1	45.4°C
R11	40.0°C
L2	41.0°C
Q1	38.8°C
R101	40.8°C
U1	39.1°C
C28	38.4°C

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