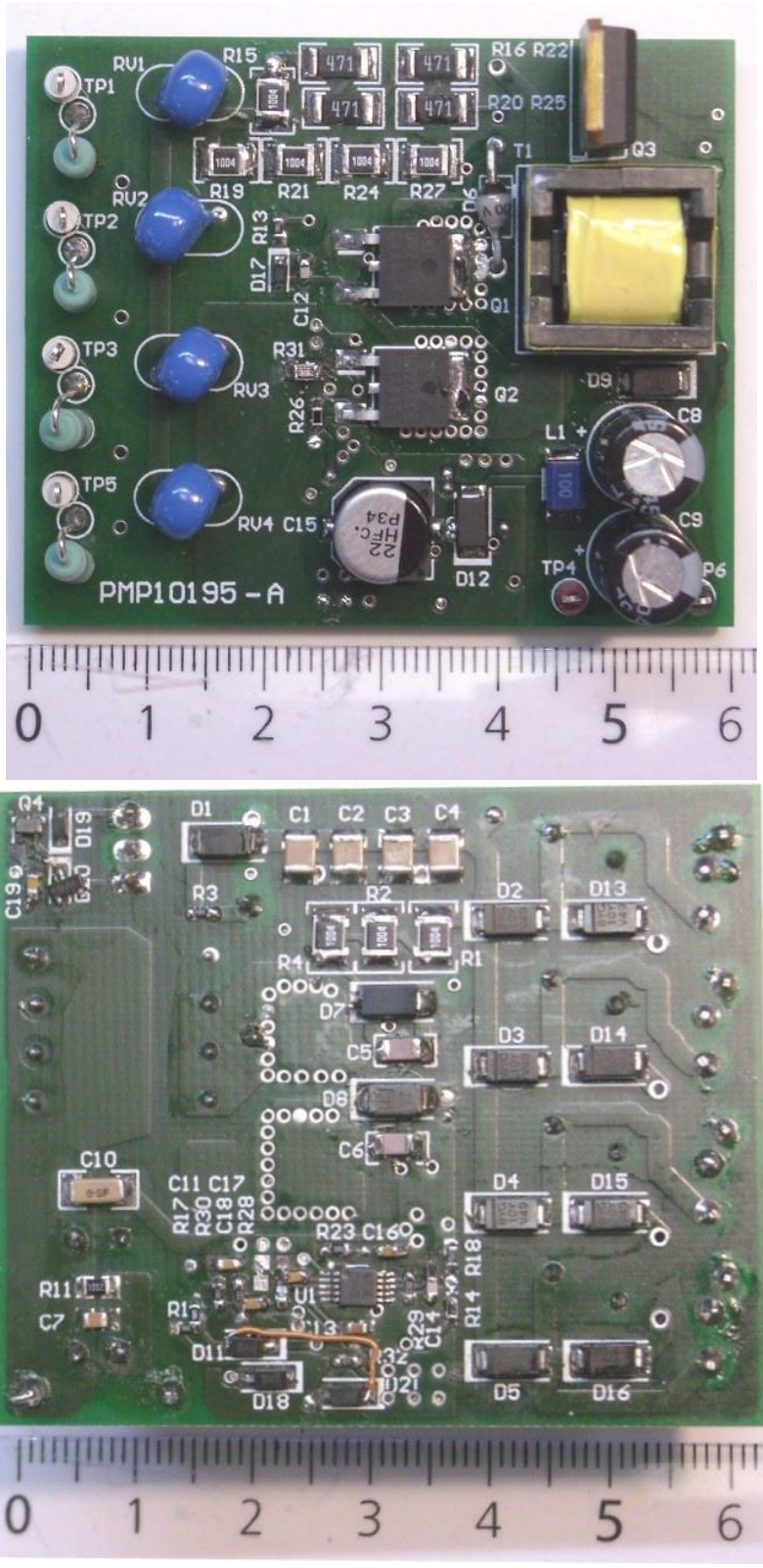
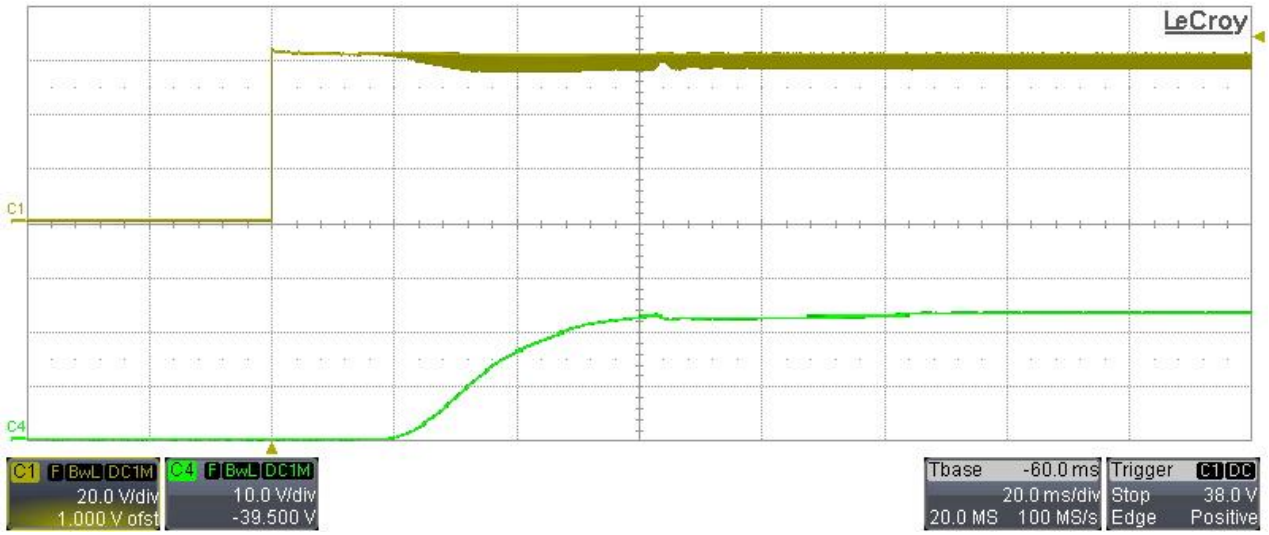
1 Photo of the Prototype:



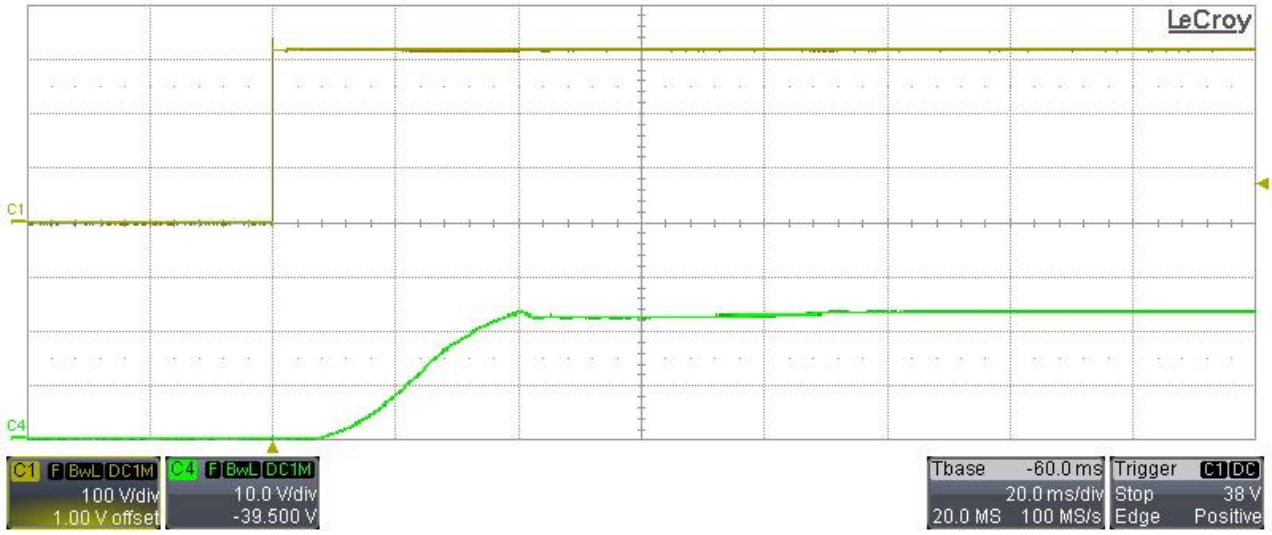
2 Startup

The output voltage behavior, for different input voltages, is shown in the images below. The input voltage was set respectively to 65Vdc, 320Vdc as well as 56Vac @ full load.

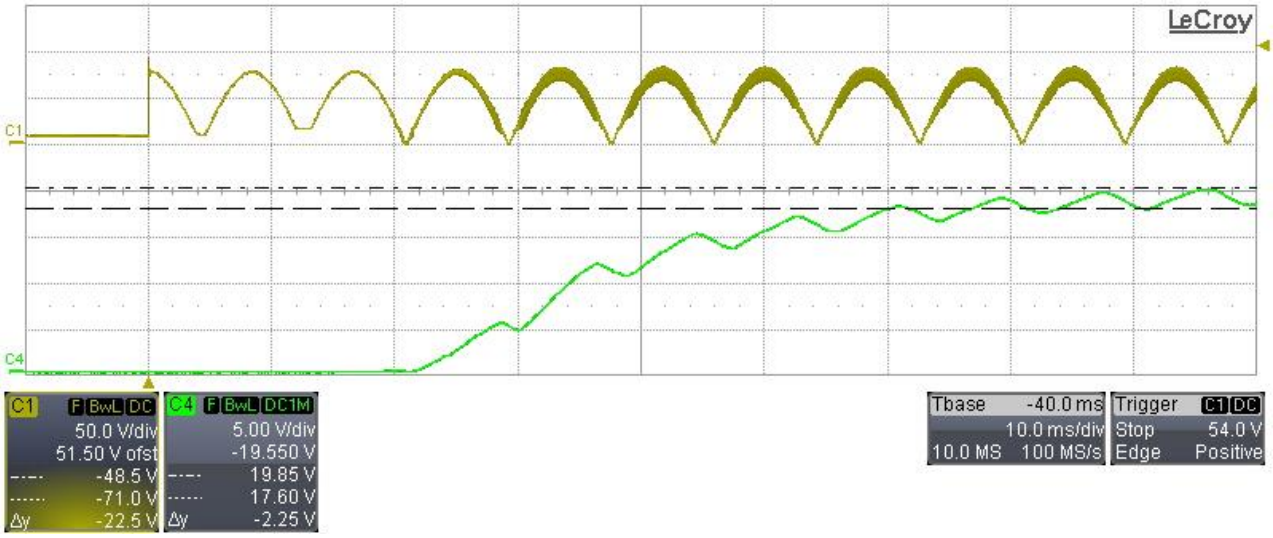
Ch.1: Input Voltage (20V/div, 20ms/div, 20MHz BWL)
Ch.4: Output Voltage (10V/div, 20MHz BWL)
Vin = 65Vdc



Ch.1: Input Voltage (100V/div, 20ms/div, 20MHz BWL)
Ch.4: Output Voltage (10V/div, 20MHz BWL)
Vin = 320Vdc

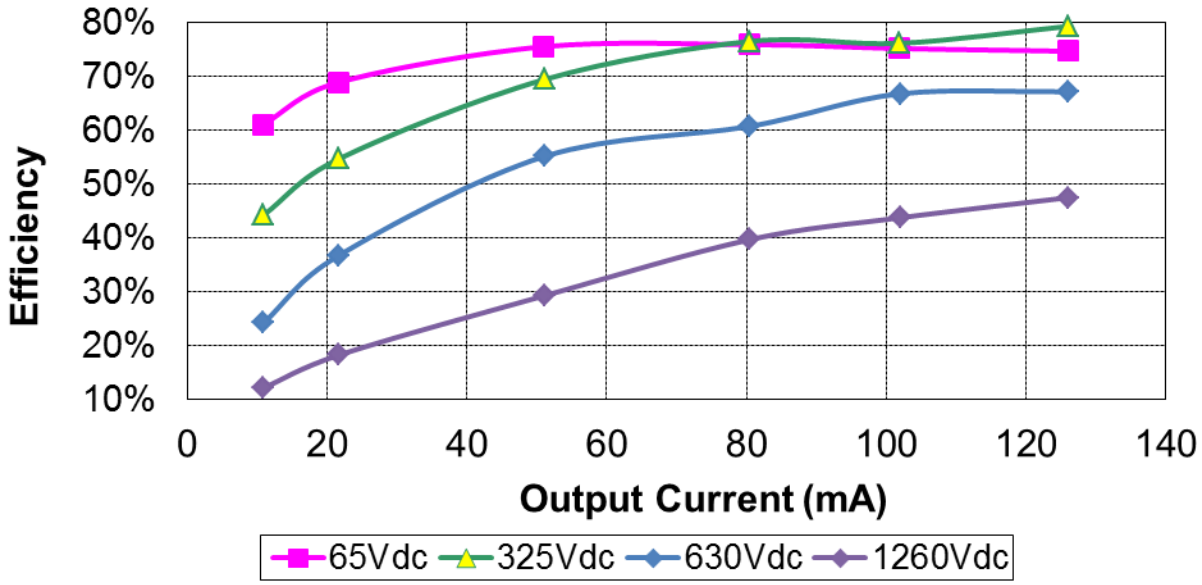


Ch.1: Input Voltage (50V/div, 10ms/div, 20MHz BWL)
Ch.4: Output Voltage (5V/div, 20MHz BWL)
Vin = 56Vac



3 Efficiency

The efficiency data are shown in the tables and graph below.
The input voltage has been set to DC peak value of 46Vac, 230Vac, 445Vac and 891Vac, respectively equivalent to 65Vdc, 325Vdc, 630Vdc and 1260Vdc. The output has been loaded from 0 to full load.



Vin (Vdc)	Iin (mA)	Vout (V)	Iout (mA)	Pout (W)	Pin (W)	Eff. (%)
65	2.06	25.86	0.0	0.00	0.13	0.0%
65	6.71	24.63	10.8	0.27	0.44	61.0%
65	11.69	24.23	21.6	0.52	0.76	68.9%
65	24.67	23.75	51.0	1.21	1.60	75.5%
65	38.34	23.50	80.5	1.89	2.49	75.9%
65	48.7	23.36	101.9	2.38	3.17	75.2%
65	60.3	23.23	126.0	2.93	3.92	74.7%

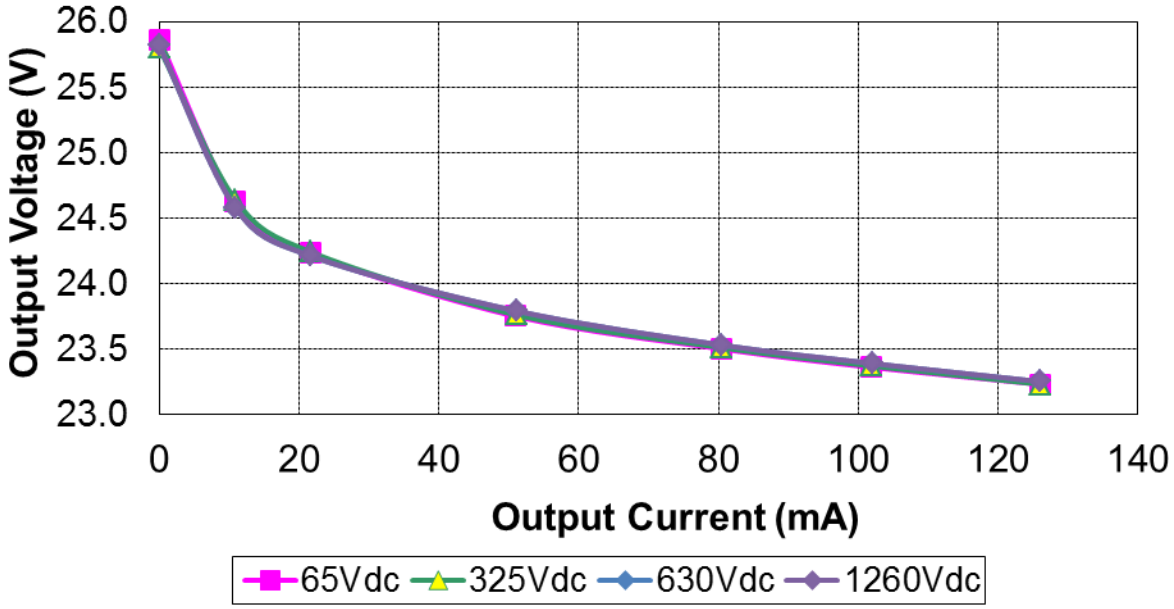
Vin (Vdc)	Iin (mA)	Vout (V)	Iout (mA)	Pout (W)	Pin (W)	Eff. (%)
325	1.08	25.80	0.0	0.00	0.35	0.0%
325	1.87	24.64	10.9	0.27	0.61	44.2%
325	2.96	24.24	21.7	0.53	0.96	54.7%
325	5.38	23.76	51.1	1.21	1.75	69.4%
325	7.61	23.51	80.5	1.89	2.47	76.5%
325	9.62	23.37	101.9	2.38	3.13	76.2%
325	11.36	23.23	126.1	2.93	3.69	79.3%

Vin (Vdc)	Iin (mA)	Vout (V)	Iout (mA)	Pout (W)	Pin (W)	Eff. (%)
630	1.09	25.82	0.0	0.00	0.69	0.0%
630	1.76	24.58	10.9	0.27	1.11	24.2%
630	2.27	24.21	21.7	0.53	1.43	36.7%
630	3.50	23.79	51.1	1.22	2.21	55.1%
630	4.95	23.53	80.5	1.89	3.12	60.7%
630	5.67	23.39	102.0	2.39	3.57	66.8%
630	6.93	23.25	126.1	2.93	4.37	67.2%

Vin (Vdc)	Iin (mA)	Vout (V)	Iout (mA)	Pout (W)	Pin (W)	Eff. (%)
1260	0.774	25.82	0.0	0.00	0.98	0.0%
1260	1.76	24.58	10.9	0.27	2.22	12.1%
1260	2.29	24.21	21.7	0.53	2.89	18.2%
1260	3.30	23.79	51.1	1.22	4.16	29.2%
1260	3.79	23.53	80.5	1.89	4.78	39.7%
1260	4.33	23.39	102.0	2.39	5.46	43.7%
1260	4.90	23.25	126.1	2.93	6.17	47.5%

4 Output Voltage Regulation

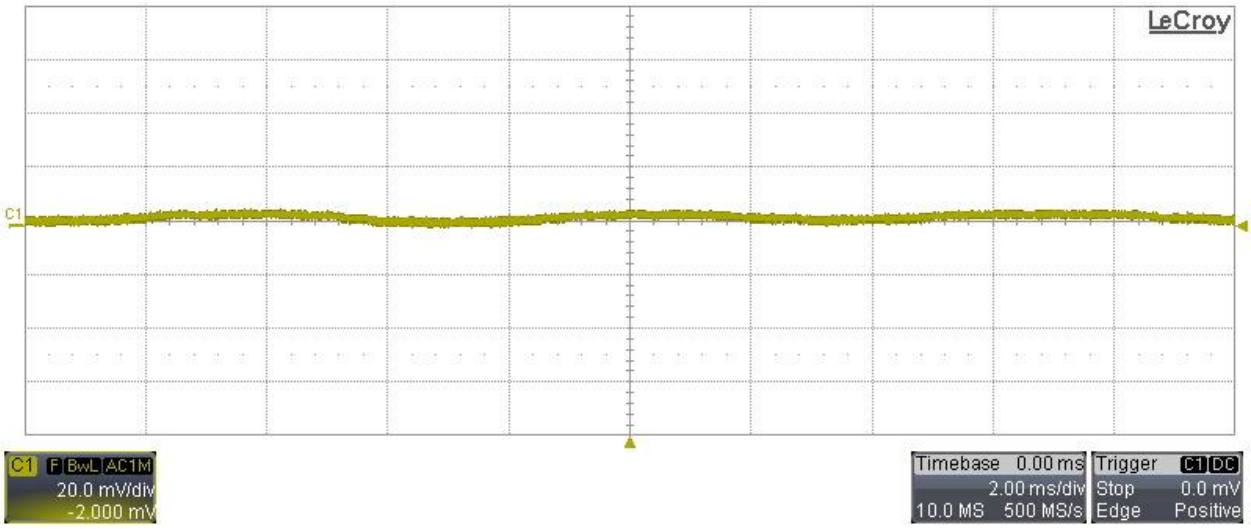
The output voltage variation versus load current is plotted below. The voltage variation was within +/-3% by connecting a minimum load of 10mA.



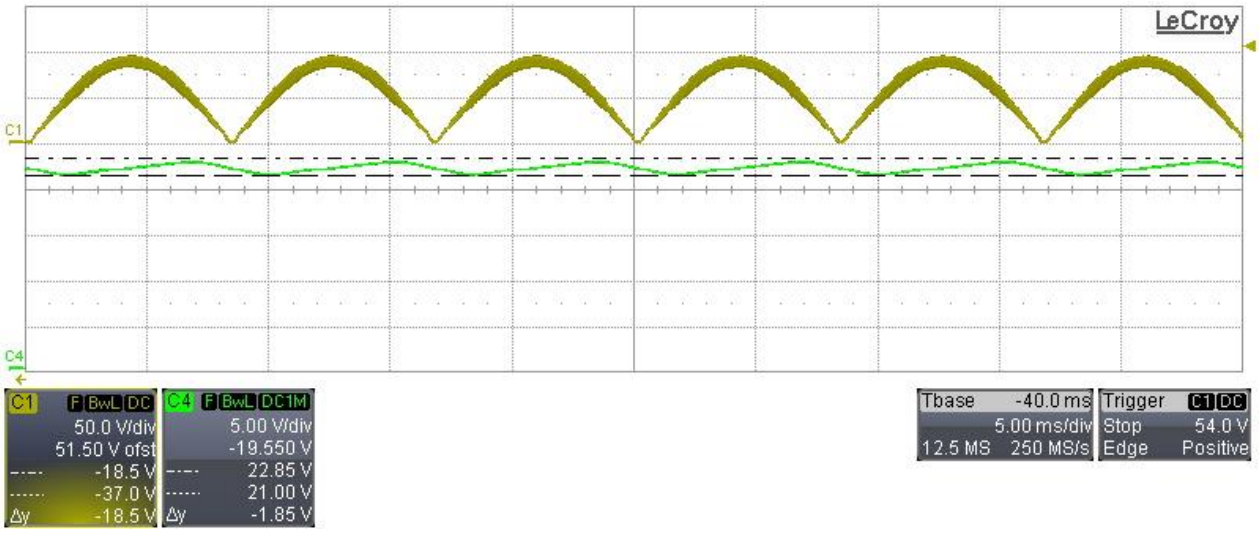
5 Output Ripple Voltage

The output ripple voltage has been measured by supplying the converter @ 325Vdc, 65Vac (60Hz) and 230Vac (50Hz) while the converter was fully loaded.

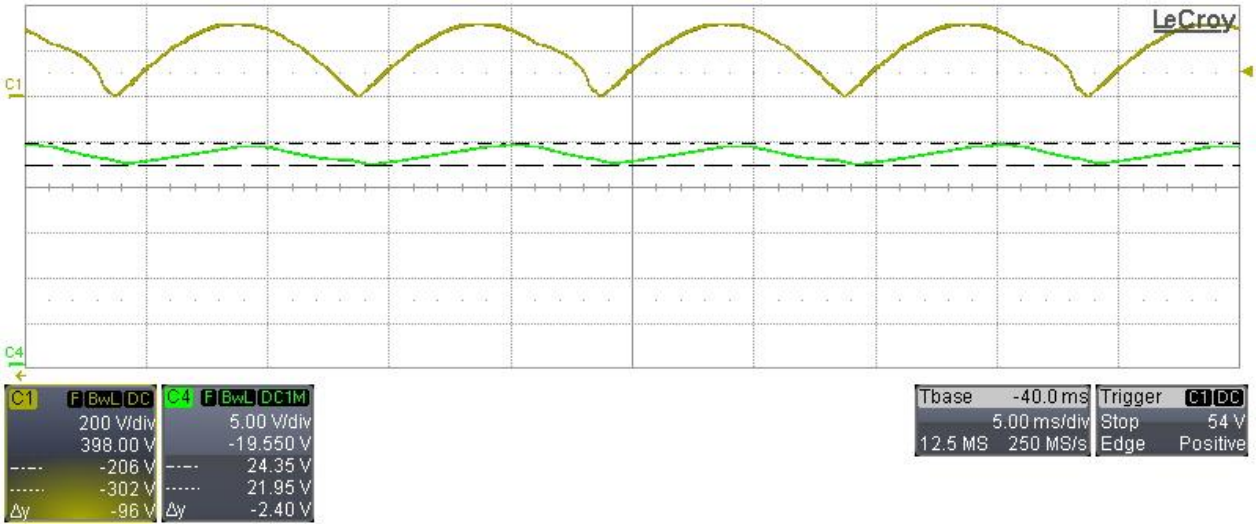
Ch.1: Output Voltage (20mV/div, 2ms/div., AC coupling), Vin = 325Vdc



Ch.1: Input Voltage (50V/div, 5ms/div., DC coupling), Vin = 65Vac, 60Hz
Ch.4: Output Voltage (5V/div, DC coupling)



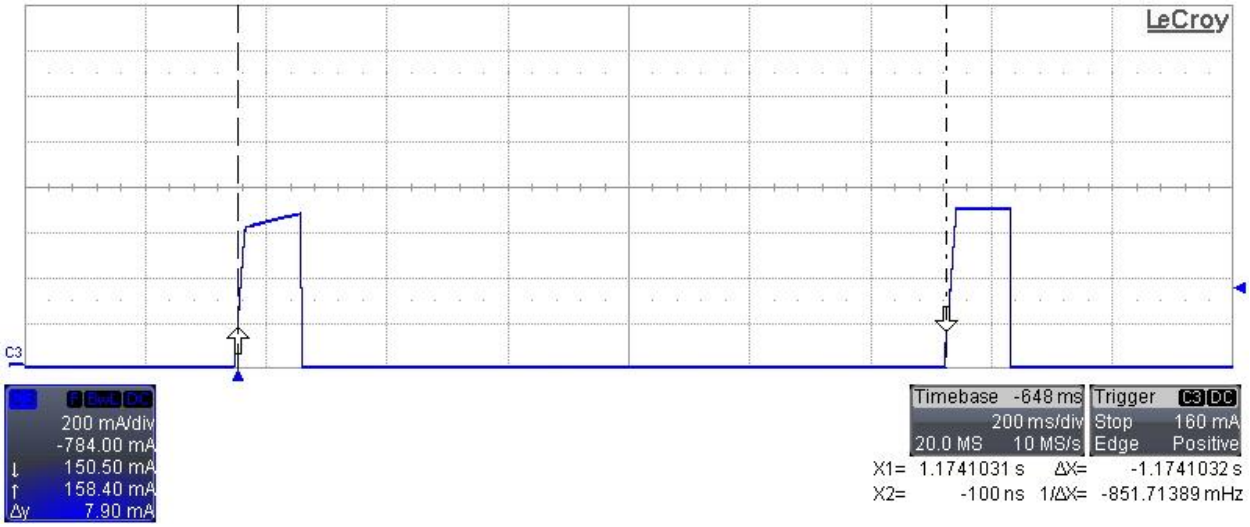
Ch.1: Input Voltage (200V/div, 5ms/div., DC coupling), Vin = 230Vac, 50Hz
Ch.4: Output Voltage (5V/div, DC coupling)



6 Short Circuit Test

The image below shows the output current behavior by applying a short circuit on output terminals; the input voltage was 135Vdc.

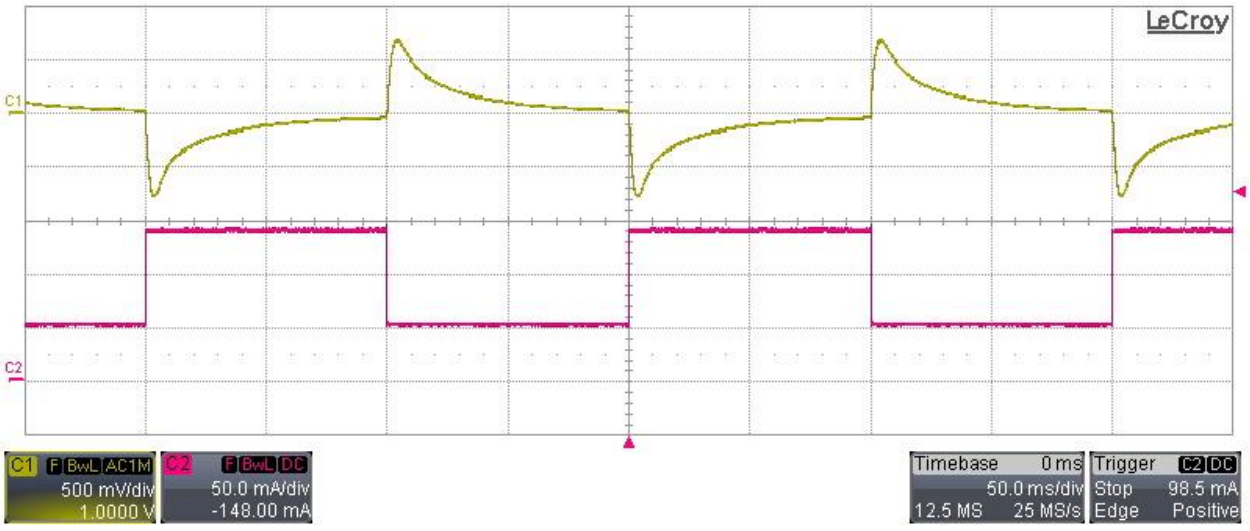
Ch.3: Output Current (200mA/div, 200ms/div. DC coupling, 20MHz BWL)



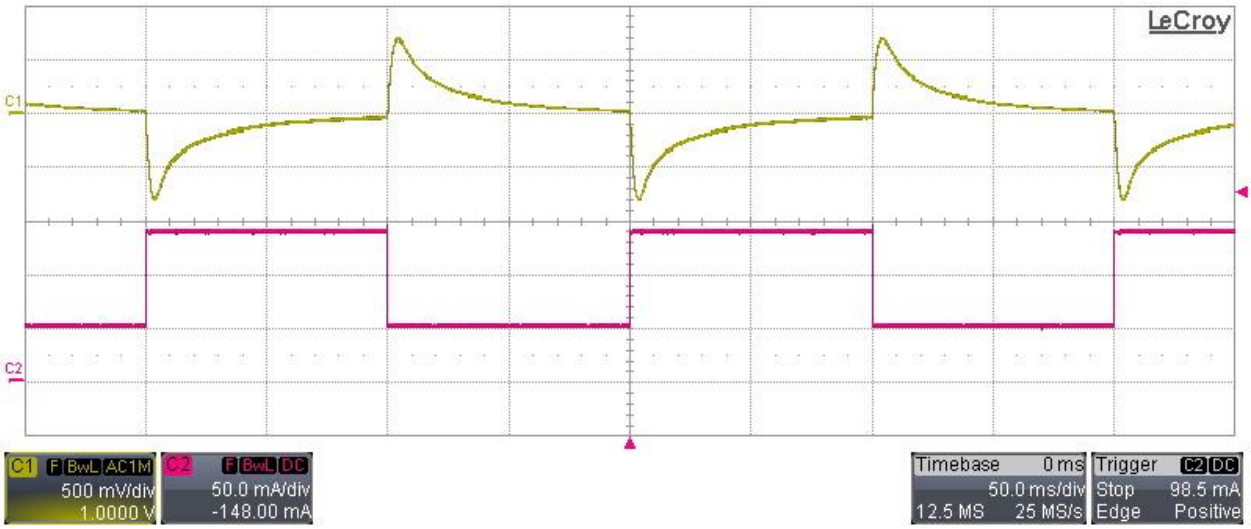
7 Transient Load Behavior

The converter has been supplied at 65Vdc and 325Vdc and the load switched between 50mA and 130mA. The images below show the voltage drop during the transients.

Ch.1: Output Voltage (500mV/div, 50ms/div., AC coupling, 20MHz BWL), Vin = 65Vdc
Ch.2: Output Current (50mA/div, DC coupling, 20MHz BWL)



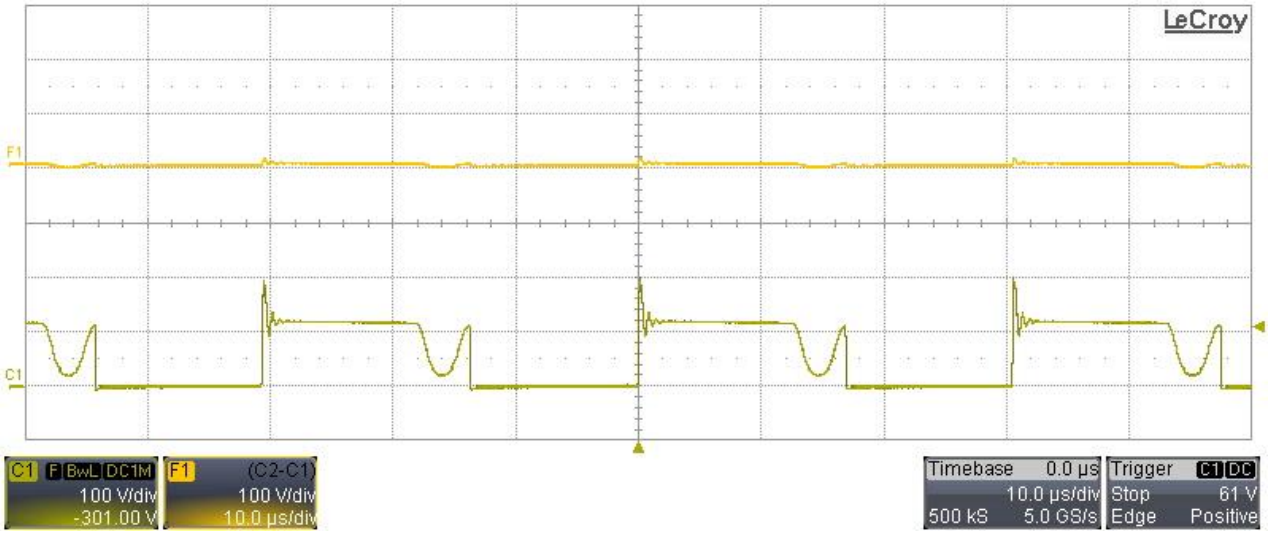
Ch.1: Output Voltage (500mV/div, 50ms/div., AC coupling, 20MHz BWL), Vin = 325Vdc
Ch.2: Output Current (50mA/div, DC coupling, 20MHz BWL)



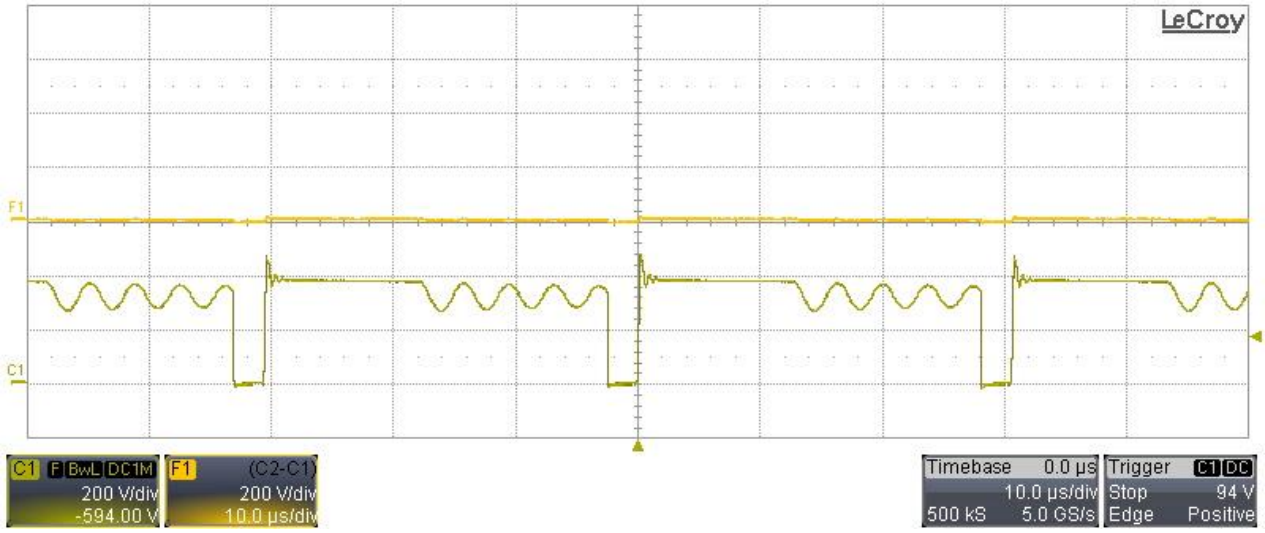
8 Switch node

The images below show the V_{DS} voltage of Q1 and Q2, taken respectively at 65Vdc, 325Vdc, 630Vdc and 1260Vdc while the output was fully loaded.

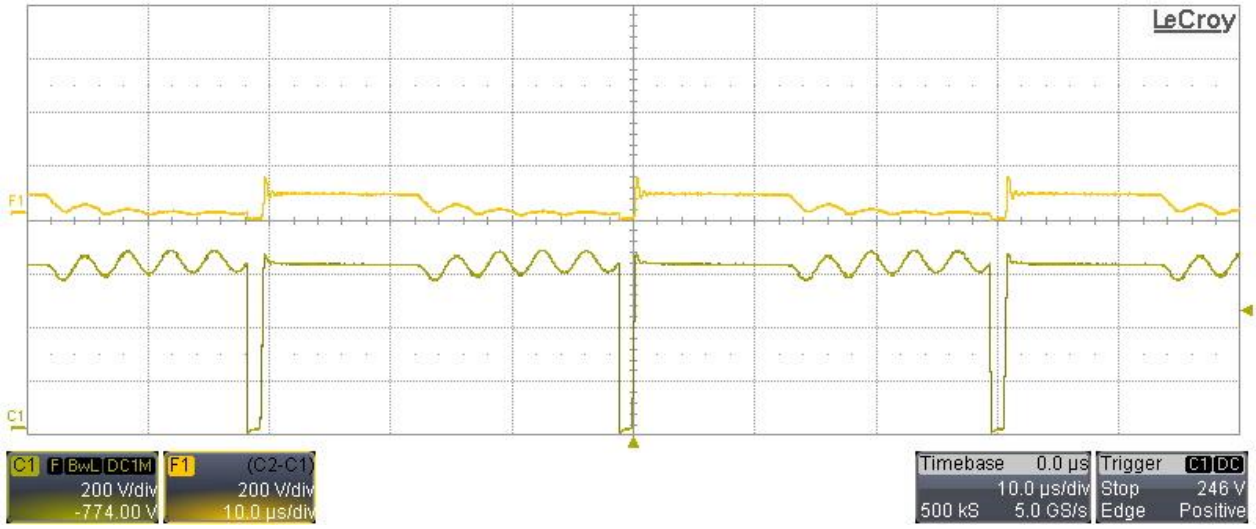
Ch.C1: V_{DS} Voltage of Q2 (100V/div, 10us/div, DC coupling, 200MHz BWL)
Ch.F1: V_{DS} Voltage of Q1 (100V/div, 10us/div, DC coupling, 200MHz BWL)
Vin = 65Vdc



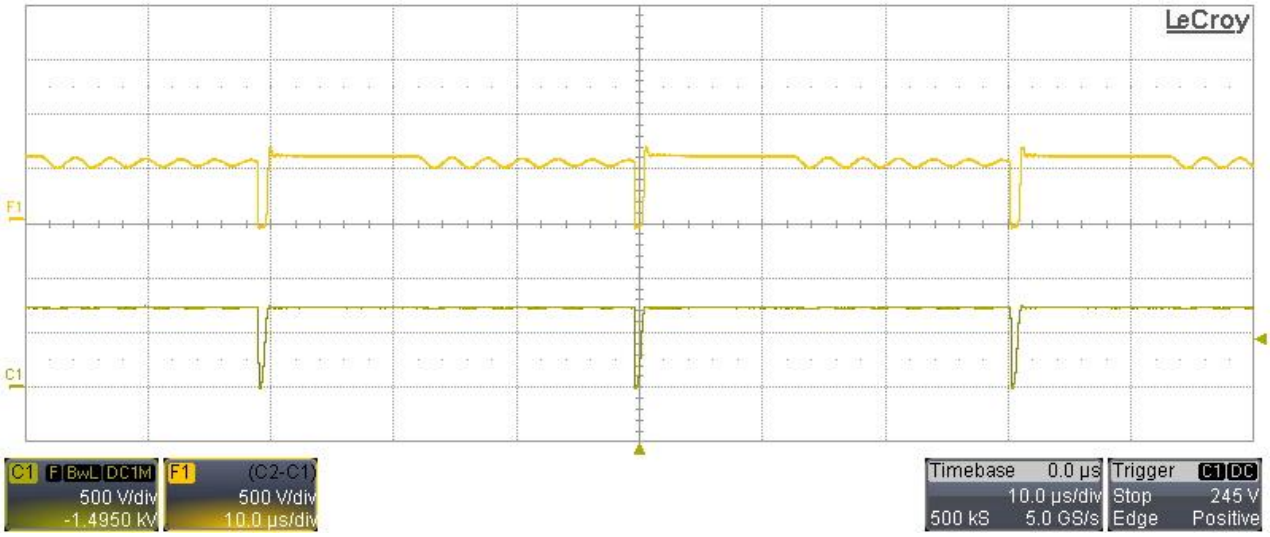
Ch.C1: V_{DS} Voltage of Q2 (200V/div, 10us/div, DC coupling, 200MHz BWL)
Ch.F1: V_{DS} Voltage of Q1 (200V/div, 10us/div, DC coupling, 200MHz BWL)
Vin = 325Vdc



Ch.C1: V_{DS} Voltage of Q2 (200V/div, 10us/div, DC coupling, 200MHz BWL)
Ch.F1: V_{DS} Voltage of Q1 (200V/div, 10us/div, DC coupling, 200MHz BWL)
Vin = 630Vdc

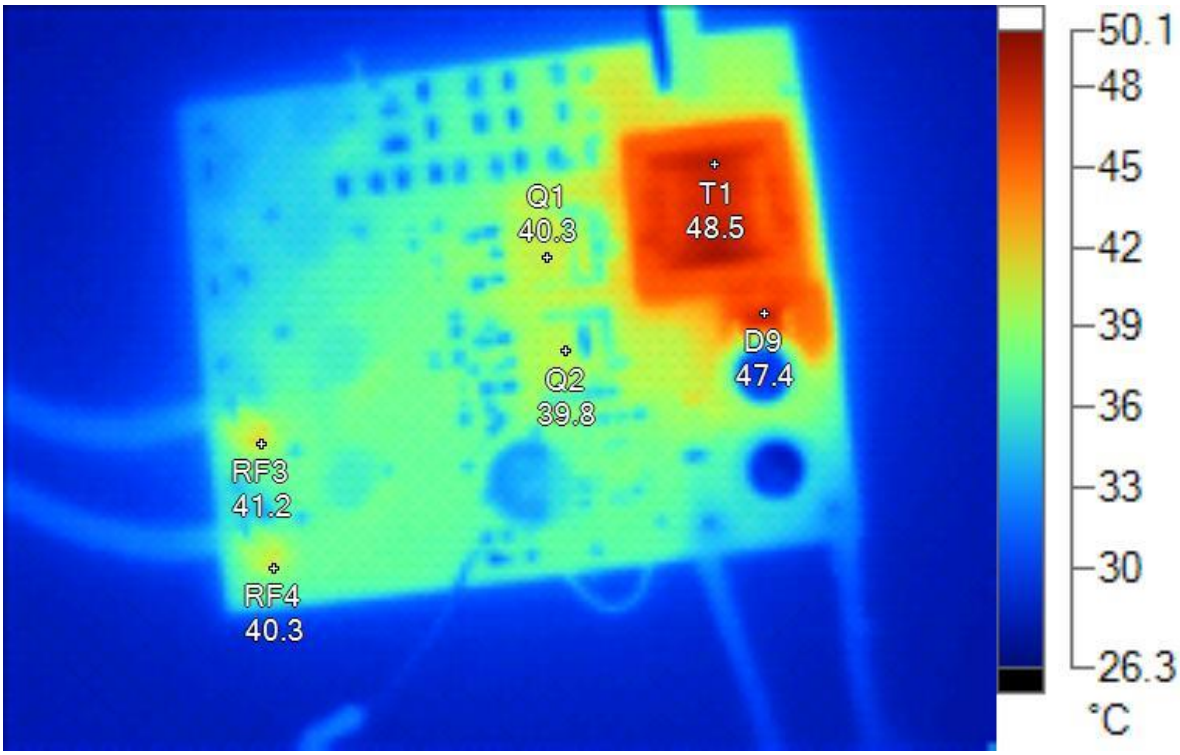


Ch.C1: V_{DS} Voltage of Q2 (500V/div, 10us/div, DC coupling, 200MHz BWL)
Ch.F1: V_{DS} Voltage of Q1 (500V/div, 10us/div, DC coupling, 200MHz BWL)
Vin = 1260Vdc



9 Thermal Report

The images below show thermal shots of the board, taken respectively at 65Vdc, 630Vdc and 1260Vdc input voltage while the load was 125mA. The board has been placed horizontally on the bench in still air conditions and the air temperature was 23º Celsius.



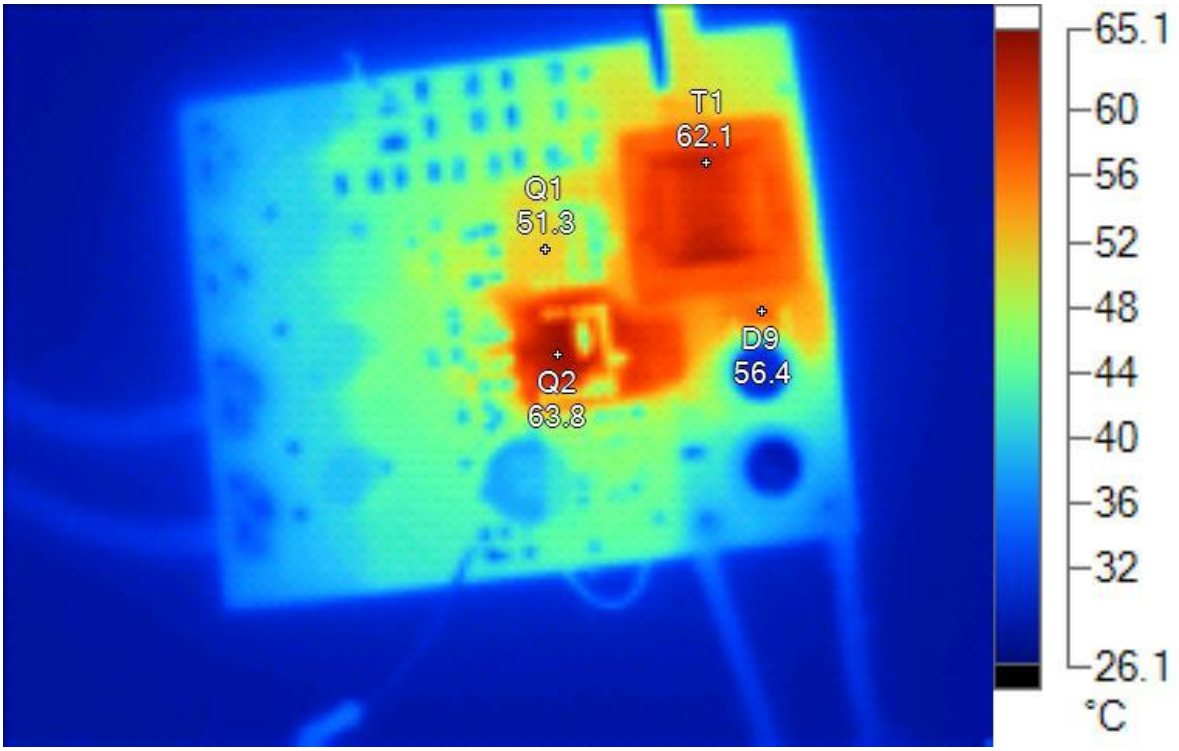
Vin = 65Vdc

Image Info

Background temperature	23°C
Average Temperature	32.9°C
Image Range	27.3°C to 49.1°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	10/19/2015 3:39:17 PM

Main Image Markers

Name	Temperature
T1	48.5°C
D9	47.4°C
Q2	39.8°C
Q1	40.3°C
RF3	41.2°C
RF4	40.3°C



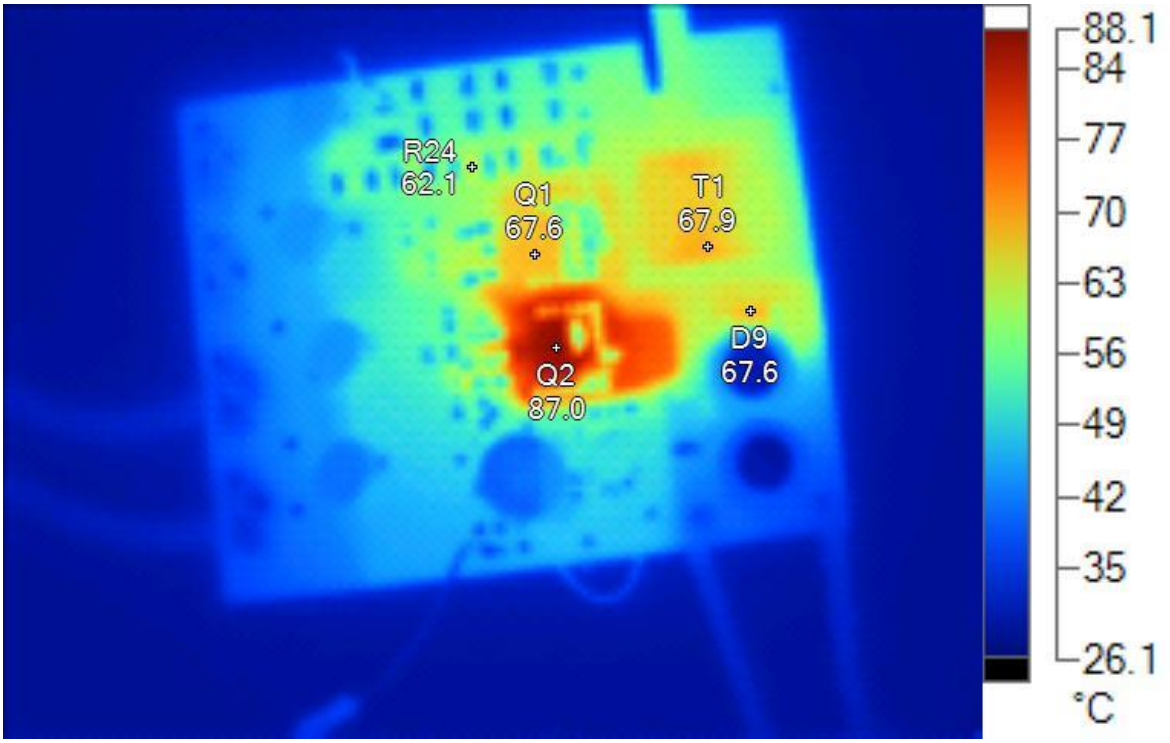
Vin = 630Vdc

Image Info

Background temperature	23°C
Average Temperature	36.1°C
Image Range	27.1°C to 64.0°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	10/19/2015 3:34:27 PM

Main Image Markers

Name	Temperature
T1	62.1°C
Q2	63.8°C
Q1	51.3°C
D9	56.4°C



Vin = 1260Vdc

Image Info

Background temperature	23°C
Average Temperature	38.7°C
Image Range	27.1°C to 87.3°C
Camera Model	Ti40FT
Camera Manufacturer	Fluke
Image Time	10/19/2015 3:31:53 PM

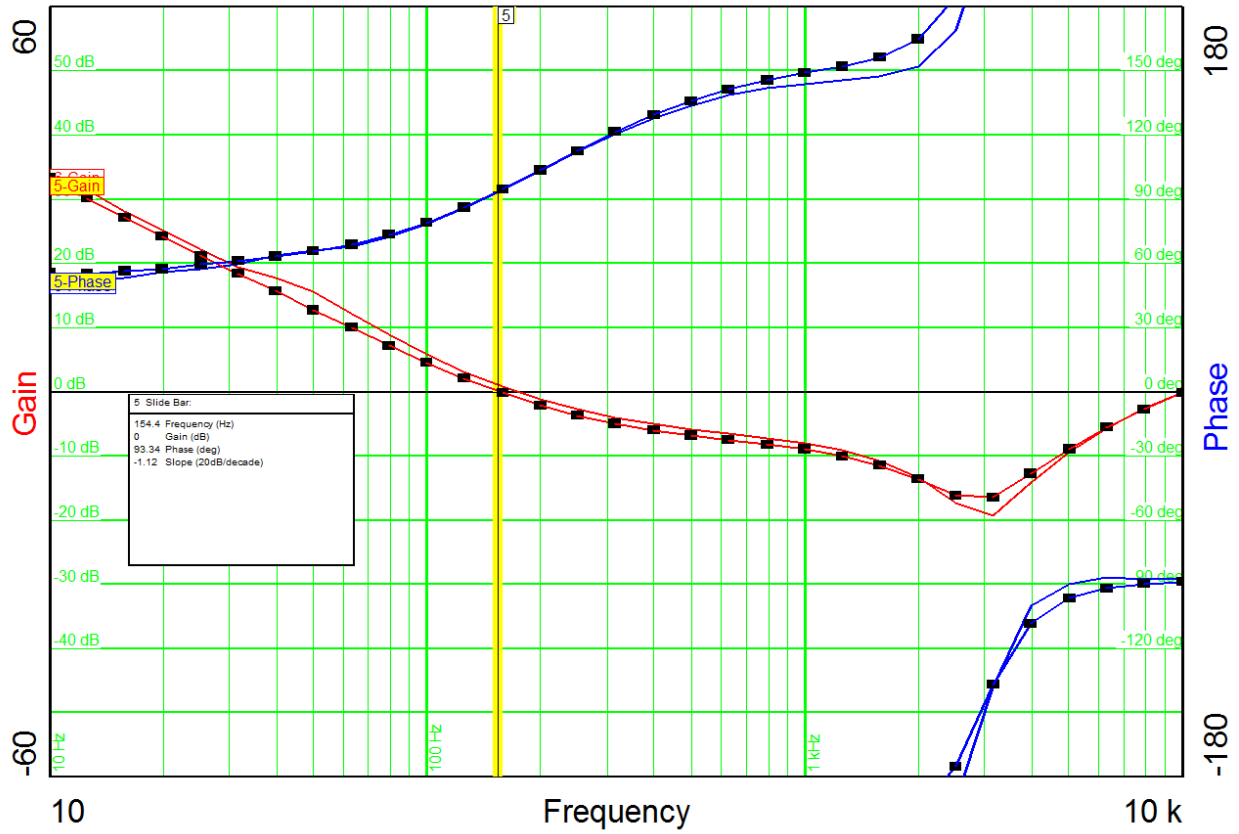
Main Image Markers

Name	Temperature
T1	67.9°C
Q2	87.0°C
Q1	67.6°C
R24	62.1°C
D9	67.6°C

10 Loop Analysis

The picture below shows the loop gain and phase of the power supply. A 50 Ohm resistor has been placed in series to R17 in order to measure the open loop transfer function. The input voltage has been set to 70Vdc and 320Vdc and the load was 125mA.

Worst case condition:
Vin: 70Vdc
Crossover frequency: 154.4 Hz
Phase margin: 93.34 deg.



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