TI Designs

Fluxgate Magnetic Current Sensing With High Linearity for Three-Phase Inverters Reference Design

Description

This TI Design provides a reference solution for accuracy, high linearity, and the galvanic isolation required for current measurement in three-phase inverters using closed-loop fluxgate magnetic current sensors. The sensor consists of a magnetic core with compensation winding interfaced to driver IC with a built-in fluxgate sensor. The design provides a pseudo-differential output with an option to connect to 3.3-V or 5-V analog-to-digital converters (ADCs). A hardware circuit for overcurrent and ground fault detection enables overcurrent protection of power switches.

Resources

TIDA-00905	Design Folder
DRV421	Product Folder
TLV1117-33	Product Folder
TLC372	Product Folder

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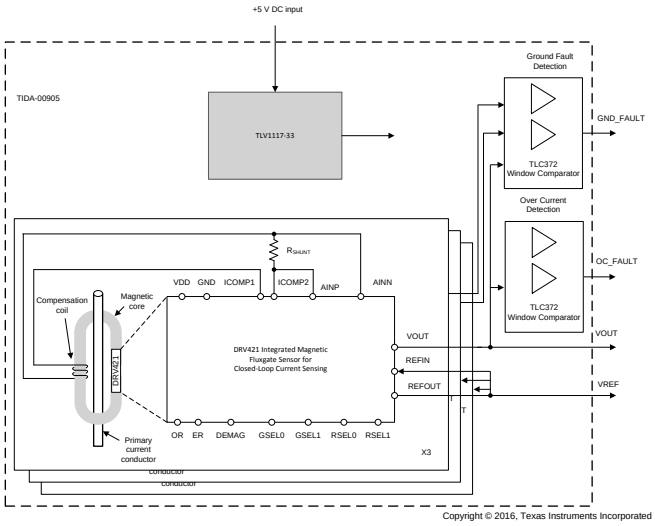
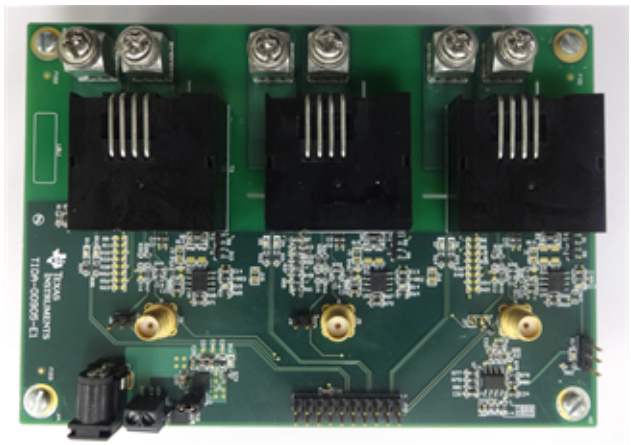
Features

- Accurately Measures Three-Phase Inverter Currents Up to 50 A_{RMS} (Nominal) and 150 A (Maximum)
- 200-kHz Bandwidth, Closed-loop Current Sensing Using Magnetic Module and Fluxgate Sensor (DRV421) to Enable Low Propagation Delay in Current Measurement
- Calibrated Current Measurement Accuracy of ±1% (Typical) Across Temperature Ranges from –25°C to +85°C
- Hardware Based Overload and Ground Fault Detection Enables Fast Response for Protection of Power Switches

Applications

- AC Inverter and VF Drives
- Three-Phase UPS
- Solar Inverters





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1 System Overview

1.1 System Description

Current measurement is an inherent part of any inverter-driven application. An important reason for measuring the motor current is to perform a control algorithm. Vector control and direct torque control require current sensing for control purposes. Information of motor parameters is also important for several control schemes. Stator current measurement is used to estimate motor parameters. Current measurement is also used for hardware overload and earth fault protection.

The output rating of the inverter must be derated while operating at a higher temperature. The higher temperature could be a result of increased ambient temperature, a faulty fan, or obstructions in the cooling path. In those scenarios, current measurement helps in derating the inverter current to keep the power devices within permissible operating temperatures.

The motor current can be measured at different locations in the inverter. Figure 1 shows the overview of usual measurement locations, considering a three-phase inverter for a motor control application. In Figure 1:

- A is the current measurement in the DC- and DC+ link.
- B is the current measurement in the bottom-side emitter path of each half bridge.
- C is the current measurement in the output phases.

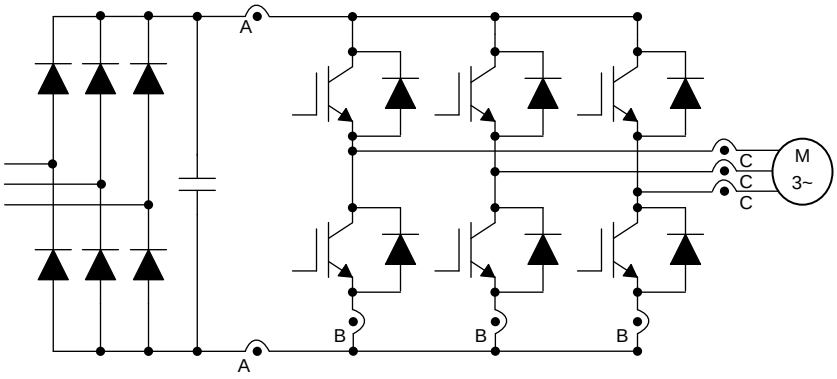

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Figure 1. Current Measuring Locations in Motor Drives

The cheapest variant of current measurement (A) is often used for applications in the lower power range. Typically, the current measurement is done on the DC- bus; this may be the reference potential of the microcontroller (MCU) and therefore is not necessary to isolate the signal. Another alternative location of current measurement (found in the low to medium power range) is variant B. Using variant B, the current is measured at the emitter of the bottom IGBT of each arm in a three-phase inverter.

It is possible to dispense with a third current measurement; this can be derived by calculation based on the two measured current signals. The advantage of this measurement method is similar to variant A; the negative section of the DC-bus can be taken as the common reference potential. However, the disadvantage is the increased stray inductance. In high dynamic drives and high-power applications, current is usually measured in the output phases of the inverter (variant C in Figure 1). The third current sensor is not necessary in this case either.

The objective of the TIDA-00905 design is to provide a reference solution for accurate current measurement (variant C) using closed-loop fluxgate magnetic current sensors. TIDA-00905 consists of a magnetic core with compensation winding interfaced to a driver IC with a built-in fluxgate sensor. This TI Design provides an analog output to interface with a 3.3-V or 5-V ADC and hardware circuit for fast detection of overcurrent and ground fault events in a three-phase inverter.

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1.2 Block Diagram

Figure 2 shows the TIDA-00905 block diagram. The design uses three devices from Texas Instruments.

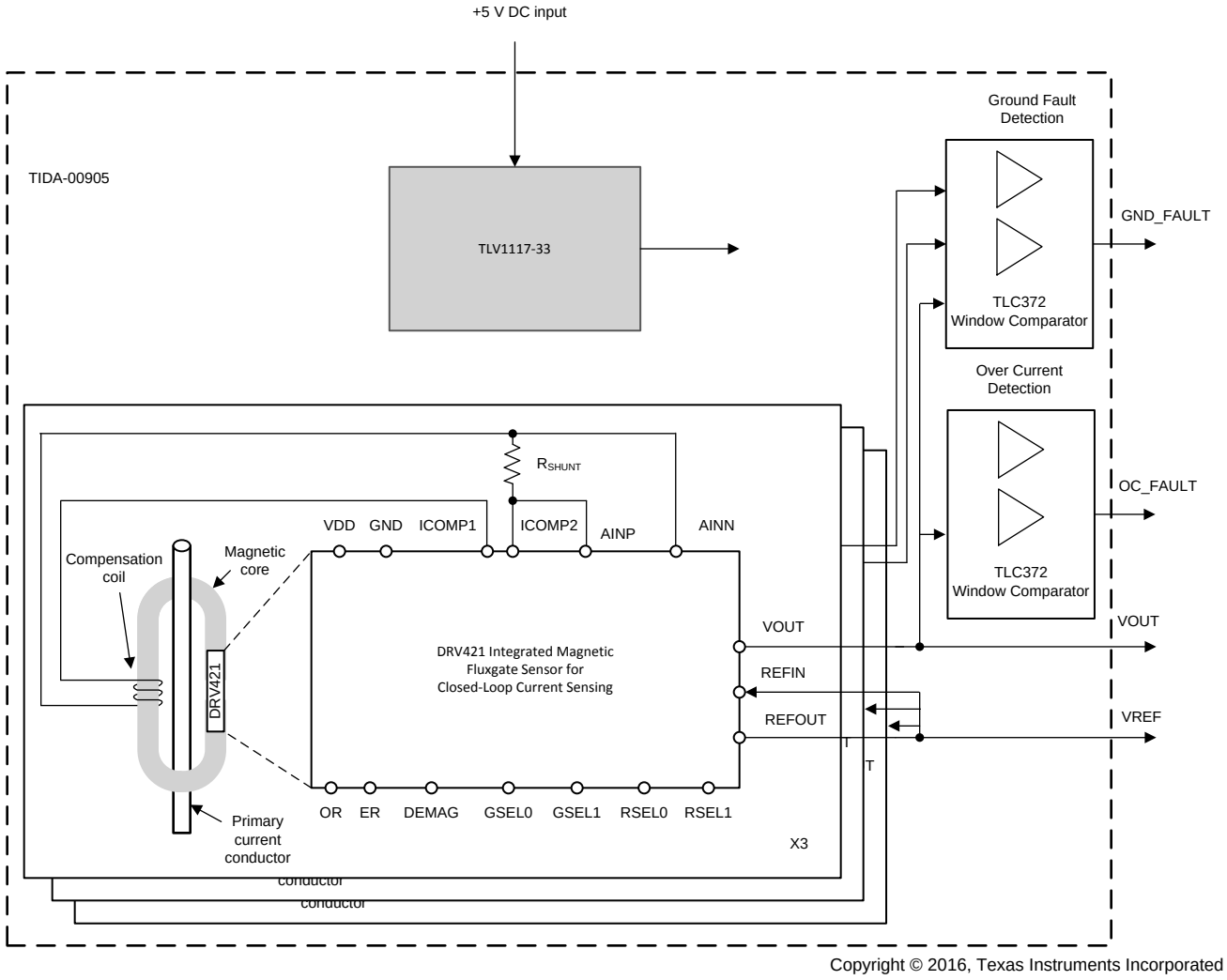

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Figure 2. TIDA-00905 Block Diagram

NOTE: Figure 2 shows only one of three channels.

At DC and in the low-frequency range, the DRV421 fluxgate senses the magnetic field induced by the primary current. The DRV421 filters the sensed signal and the internal H-bridge driver generates a proportional compensation current. The compensation current flows through the compensation coil and generates a magnetic field. The magnetic field drives the original magnetic flux in the core back to zero. The value of this magnetic field is increased by the number of compensation coil windings.

At higher frequencies, the magnetic field induced by the primary current directly couples into the compensation coil and generates a current. The low impedance of the H-bridge driver does not influence the value of this current. Also in this case, the value of the compensation current is the value of the primary current divided by the number of compensation coil windings. In either case, the compensation current passes through a shunt resistor (R_{SHUNT}). The voltage across R_{SHUNT} is tapped and given to the differential amplifier integrated inside of the DRV421. The output of the DRV421 is a pseudo-differential output where the current is proportional to the difference of VOUT and VREF.

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A low-dropout (LDO) voltage regulator (TLV1117-33) at the input-to-board is provided to power DRV421 with 3.3 V when interfacing with a 3.3-V MCU. This LDO can be bypassed by using a jumper setting when the LDO is not required.

The over current and ground fault protection feature is provide using window comparator using TLC372. The overcurrent thresholds can be set by a potential divider. The ground fault detection circuit is based on the principle that the sum of instantaneous three-phase currents should be zero in a balanced load or motor. The ground fault detection circuit averages the VOUT for the three measuring channels. The ground fault is signaled when the current becomes unbalanced beyond a certain threshold value.

1.3 Highlighted Products

This reference design features the following devices from Texas Instruments. For more information on each of these devices, see their respective product folders at www.ti.com or click on the links for the product folders on the first page of this reference design.

1.3.1 DRV421

The DRV421 is designed for magnetic closed-loop current sensing solutions, enabling isolated, precise dc- and ac-current measurements. This device provides a proprietary integrated fluxgate sensor and the required analog signal conditioning, minimizing the component count and cost. The low offset and drift of the fluxgate sensor, along with an optimized front-end circuit results in unrivaled measurement precision. The DRV421 provides all the necessary circuit blocks to drive the current-sensing feedback loop. The sensor front-end circuit is followed by a filter that can be configured to work with a wide range of magnetic cores. The integrated 250-mA H-Bridge drives the compensation coil and doubles the current measurement range (compared to conventional single-ended drive methods). The device also provides a precision voltage reference and shunt sense amplifier to generate and drive the analog output signal.

1.3.2 TLV1117-33

The TLV1117 device is a positive LDO voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5-, 1.8-, 2.5-, 3.3-, and 5-V, and adjustable-output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents.

1.3.3 TLC372

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2 V to 18 V. Each device features high input impedance (typically greater than 1012 Ω), allowing direct interfacing with high-impedance sources. The outputs are N-channel, open-drain configurations and can be connected to achieve positive-logic, wired-AND relationships.

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2 System Design Theory

2.1 Closed-Loop Sensing

2.1.1 Basic Theory of Closed-Loop Sensing

Closed-loop current transducers use a ferromagnetic core with a magnetic sensor inserted into a gap in the core. The core picks up the magnetic field created by the current that flows through the primary winding (I_{PRIM}). The magnetic field is measured by the magnetic sensor and passed on to a signal conditioning stage for filtering and amplification. The coil driver stage provides current to the compensation coil, I_{COMP}, which creates an opposing magnetic field that cancels the effect of the primary current. The compensation current passes through a shunt resistor R_{SHUNT} creating the differential voltage input for a precision sense amplifier. The amplifier gains the shunt voltage and drives the output stage of the transducer. The resulting voltage output, VOUT, is proportional to the current flowing through the primary winding.

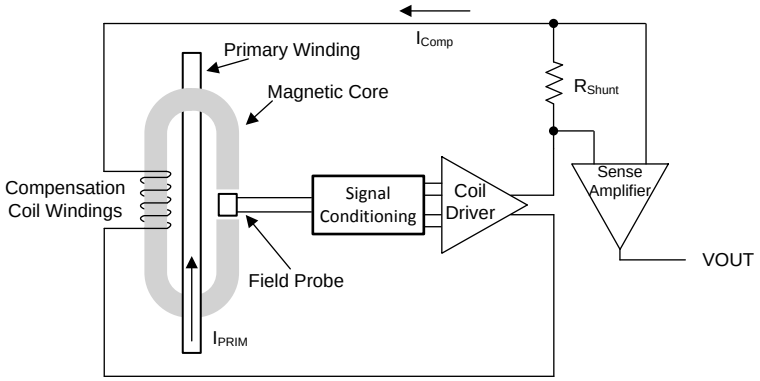

Figure 3. Closed-Loop Sensor Block Diagram

Although Figure 3 shows the primary current passing only once through the magnetic core, the most general case is a core with a primary winding that consists of N_P turns and a secondary winding that consists of N_S turns. The N_P and N_S turns affect the module output (see Equation 1).

$$V_{OUT} = I_{PRIM} \times \left(\frac{N_P}{N_S} \right) \times R_{SENSE} \times G_{SA} \quad (1)$$

where

- V_{OUT} is the transducer output
- I_{PRIM} is the primary current to be measured
- N_P is the number of turns in the primary winding
- N_S is the number of turns in the compensation-coil winding
- R_{SENSE} is the shunt resistor
- G_{SA} is the gain of the sense amplifier

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2.1.2 Integrated Fluxgate Sensor, Signal Conditioning, Coil Driver, and Sense Amplifier

The DRV421 was chosen to minimize the component count and error sources. This IC has an integrated fluxgate sensor, a compensation coil driver, and a precision differential amplifier for the output stage.

The H-bridge driver stage can provide up to 250 mA to the compensation coil, and the differential amplifier stage provides a gain of 4 V/V to the shunt resistor.

The fluxgate sensor offset voltage can be removed (along with the core magnetization) by using the demagnetization feature of the DRV421 (pin DEMAG). The demagnetization feature can be used at startup or during operation, but care must be taken to ensure the primary current is zero when the core is demagnetized. Please consult the DRV421 datasheet for further details. Because the DRV421 contains the fluxgate sensor, signal conditioning, coil driver, and the sense amplifier in a single package, the entire system shown in Figure 3 is simplified to that shown in Figure 4.

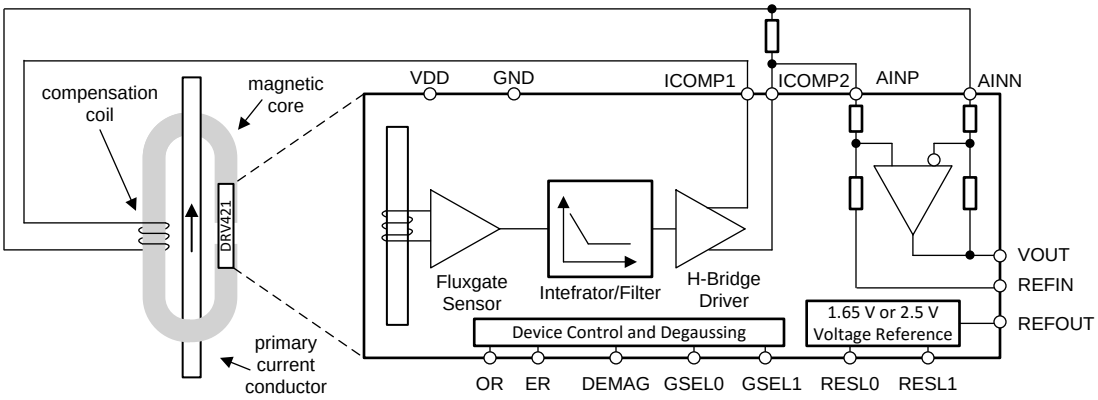

Figure 4. Closed Loop System Using DRV421 With Integrated Fluxgate Sensor

2.1.3 Magnetic Core Selection

The sensor module has a compensation coil and a primary coil. For this TI Design, the SC3113 module from Sumida was chosen. This module offers a magnetic core with magnetic gain of 500 μT/A, galvanic isolation tested up to 4.3 kV_{RMS} (50 Hz or 60 Hz for 1 minute), and consists of a 710-turn compensation coil and a set of four primary conductors. In this design, all four primary conductors are connected in parallel to yield a single turn for the primary winding (N_P) that is capable of carrying the maximum current from the design objectives.

The resulting secondary current (I_S) is 211.3 mA as (see Equation 2) for a primary current of 150 A (I_P).

$$I_S = \frac{I_P N_P}{N_S} = \frac{(150\ A) \times 1}{710} = 211.3\ mA \tag{2}$$

2.1.4 Shunt Resistor Selection

A shunt resistor placed in series with the compensation winding current path is required to provide a voltage to the output differential sense amplifier stage. Selecting an appropriate shunt resistor is dependent on the amount of current that flows through the secondary coil and the gain of the difference amplifier. The gain of the difference amplifier in the DRV421 is 4 V/V. The maximum voltage across the shunt must be less than ±625 mV for ±150 A of primary current. The value of $R_{shunt(max)}$ is calculated in Equation 3.

$$R_{shunt(max)} = \frac{V_{shunt(max)}}{I_{S(max)}} = \frac{625\ mV}{211\ mA} = 2.96\ \Omega \tag{3}$$

To provide a margin, select a value of 2.2 Ω.

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2.1.5 Sensing Current

Figure 5 shows the schematic of the sensing circuit.

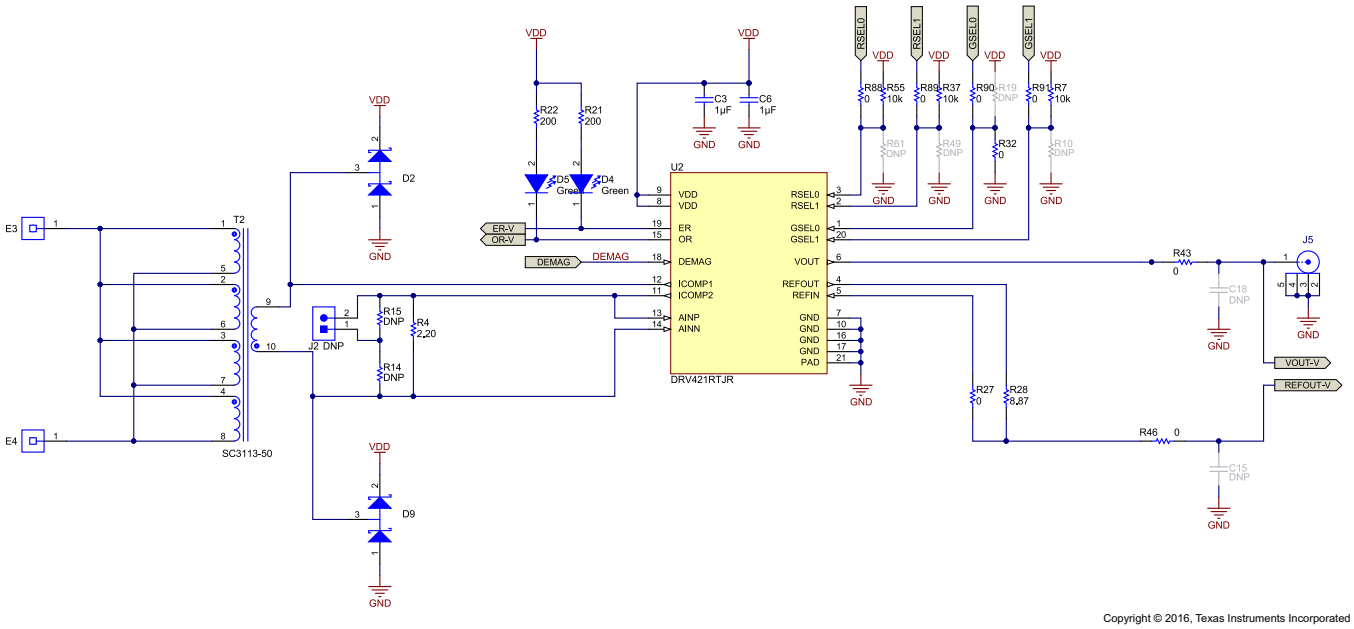

Figure 5. DRV421 and Sumida Magnetic Module SC3113-50

The SC3113-50 is a magnetic module from Sumida that has a primary nominal current (RMS) range of 50 A and measuring (peak) range of ±150 A. With this input current range, the recommended value of the sense resistor is 2.2 Ω. The primary windings are connected in parallel.

NOTE: The recommended value for the sense resistor (with the SC3113-50) is 2.2 Ω. With this shunt resistor value and 211.3 mA of compensation current (see Equation 2) the voltage developed across the shunt resistor is ±211.3 mA × 2.2 Ω = ±465 mV. The output must be measured between VOUT and REFOUT.

For more details about the gain and reference settings for the DRV421, refer to the datasheet of DRV421. In this TI Design, pins RSEL0 and RSEL1 are made high to make the REFOUT pin generate a reference voltage of $V_{DD}/2$. The high is selected for each of the three measurement channels. R55 and R37 are used to pull up the RSEL pins. The GSEL0 and GSEL1 pins are made low and high (respectively) by R32 and R7; this configures the internal AC open-loop gain of the internal integrator to 25.

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The REFOUT pin from one measuring channel is used and the three REFIN pins are tied together to this REFOUT pin. The pins are tied by populating resistors R87 and R86 (Figure 6). Tying the three REFIN prevents each channel from having a different reference drift with respect to temperature.

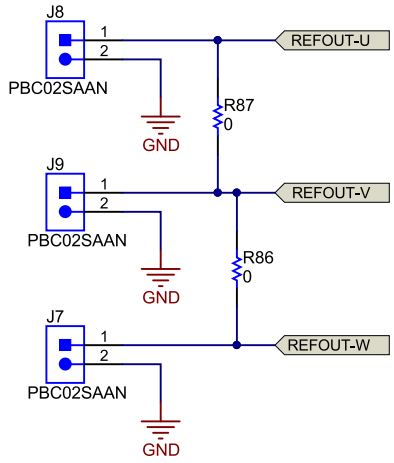

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Figure 6. Reference Configuration

2.1.6 Demagnetization Feature

An improper startup or a previous high-current situation could cause the magnetic core to become magnetized, resulting in an offset in the output. The DRV421 provides a feature to demagnetize the core by pulling up the DEMAG signal. In this TI Design, pulling up the DEMAG signal has be done by the push button shown in Figure 7. The DEMAG signal must be pulled up for a minimum of 25 µs when there is no current in the primary conductor. Alternatively, the signal may have been driven at startup by an MCU.

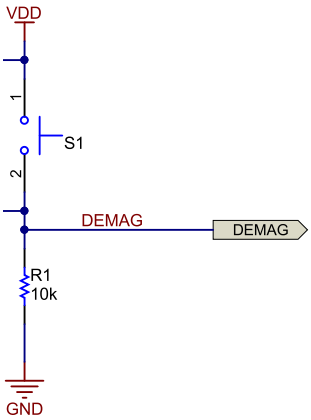

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Figure 7. DEMAG Circuit

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2.2 Scale Factor

The scale factor is used to calculate the input current from the output of the DRV421. The calculation is given below:

The full scale range of the magnetic module is 50 A_{RMS} and the turn ratio is 1:710. That is, the current in the secondary winding at full scale is 50 A / 710 = 0.0704 A_{RMS}.

The gain of the magnetic module is 0.0704 A / 50 A = 0.0014084 A/A. The Shunt value is 2.2 Ω. That is, the gain in terms of voltage per input current is 0.0014084 × 2.2 = 0.003098 V/A.

DRV421 shunt voltage scale factor: The scale factor to convert the measured voltage across the shunt to current in primary is 1 / 0.003098 = 322.72 A/V or 0.3227 A/mV.

Scale factor for output of DRV421: Considering the differential amplifier gives a gain of 4 V/V and the gain of input fluxgate stage is 0.003098 V/A; combining this, the overall gain is 4 × 0.003098 = 0.01239 V/A

Equation 4 shows the scale factor for the entire signal chain.

$$\frac{1}{0.01239} = 80.6818 \text{ A / V} \tag{4}$$

2.3 Overcurrent Detection

The overcurrent event is detected when the VOUT signal from DRV421 exceeds either the upper or lower threshold. The overcurrent circuit is shown in Figure 8, it comprises of TLC372 in a window comparator configuration. This circuit is present on all three phases.

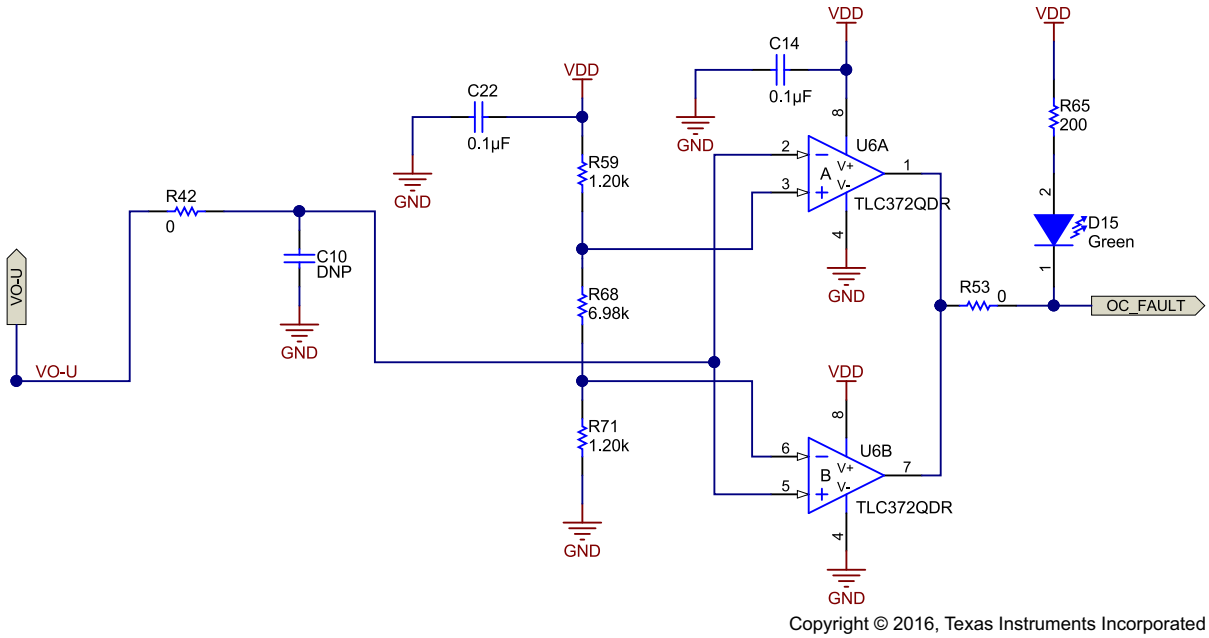

Figure 8. Overcurrent Detection Circuit

The thresholds need to be set at ±150 A. In Figure 8, the threshold is set by the potential divider consisting of resistor R59, R68, and R71. The resistor values were chosen using Equation 5 and Equation 6.

$$\text{Upper Threshold} = \frac{V_{DD}}{2} + \frac{\text{Current Threshold}}{\text{Scale Factor}} = 2.5 + \frac{150 \text{ A}}{80.6818} = 4.3591 \text{ V} \tag{5}$$

$$\text{Lower Threshold} = \frac{V_{DD}}{2} + \frac{\text{Current Threshold}}{\text{Scale Factor}} = 2.5 + \frac{150 \text{ A}}{80.6818} = 0.6408 \text{ V} \tag{6}$$

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The difference of the threshold values is ΔV_T = 4.3591 – 0.6408 = 3.7183 V. This voltage drop occurs across resistor R68. ΔV_T is given by Equation 7.

$$\Delta V_T = V_{DD}\left(\frac{R68}{R59 + R86 + R71}\right) \tag{7}$$

R59 is made equal to R71 to set the threshold equally from the value of V_{DD} / 2.

$$\Delta V_T = V_{DD}\left(\frac{R68}{2 \times R59 + R86}\right) \tag{8}$$

V_{CC} is 5 V, and if R68 is selected to be 6.98 KΩ, then R59 and R71 are approximately 1.2 KΩ.

2.4 Ground Fault Detection

In an inverter driving a motor load or a balanced three-phase load, the vector sum of the line currents should be zero. Any non-zero value indicates an imbalance and presence of some leakage current though the motor grounding. This fault condition is detected in hardware by averaging the V_{OUT} signal from the three measurement channels and detecting when it exceeds either a higher or lower threshold. Resistors R81, R79, and R77 add the VO-U, VO-V, and VO-W signals at the input of the window comparator (these signal are from the VOUT pin of each DRV421).

Consider the voltage across C31 to be V_A, then V_A = 1 / 3 × (VO-U + VO-V + VO-W). During normal conditions, the value of V_A would be near V_{DD} / 2. The V_{DD} is 5 V and V_{DD} / 2 is 2.5 V. The imbalance must be three times the threshold that is set by the potential divider. The desired current threshold is divided by three to calculate the corresponding voltage threshold on signal V_A; this is because the factor of 1 / 3 appears in the summing function of resistors R81, R79, and R77 (see Equation 9).

$$\Delta V_A = \frac{I_{Threshold}}{3 \times \text{Scale Factor}} = \frac{8.2}{3 \times 80.6818} = 0.0338 \text{ V} \tag{9}$$

The upper threshold is set to 2.5 V + 0.0338 V = 2.5338 V. The lower threshold is set to: 2.5 V – 0.0338 V = 2.4661 V.

The upper threshold is set by resistors R73 and R74 (see Equation 10).

$$R73 = R74\left(\frac{V_{DD} - V_{Upper\ Threshold}}{V_{Upper\ Threshold}}\right) \tag{10}$$

Selecting R74 = 11 kΩ gives R73 ≈ 10.7 kΩ.

The lower threshold is set by resistors R84 and R85 (see Equation 11).

$$R84 = R85\left(\frac{V_{DD} - V_{Lower\ Threshold}}{V_{Lower\ Threshold}}\right) \tag{11}$$

Select R85 = 10.7 kΩ gives R84 ≈ 11 kΩ.

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Figure 9 shows the ground fault detection circuit; it comprises of the TLC372 in a window comparator configuration.

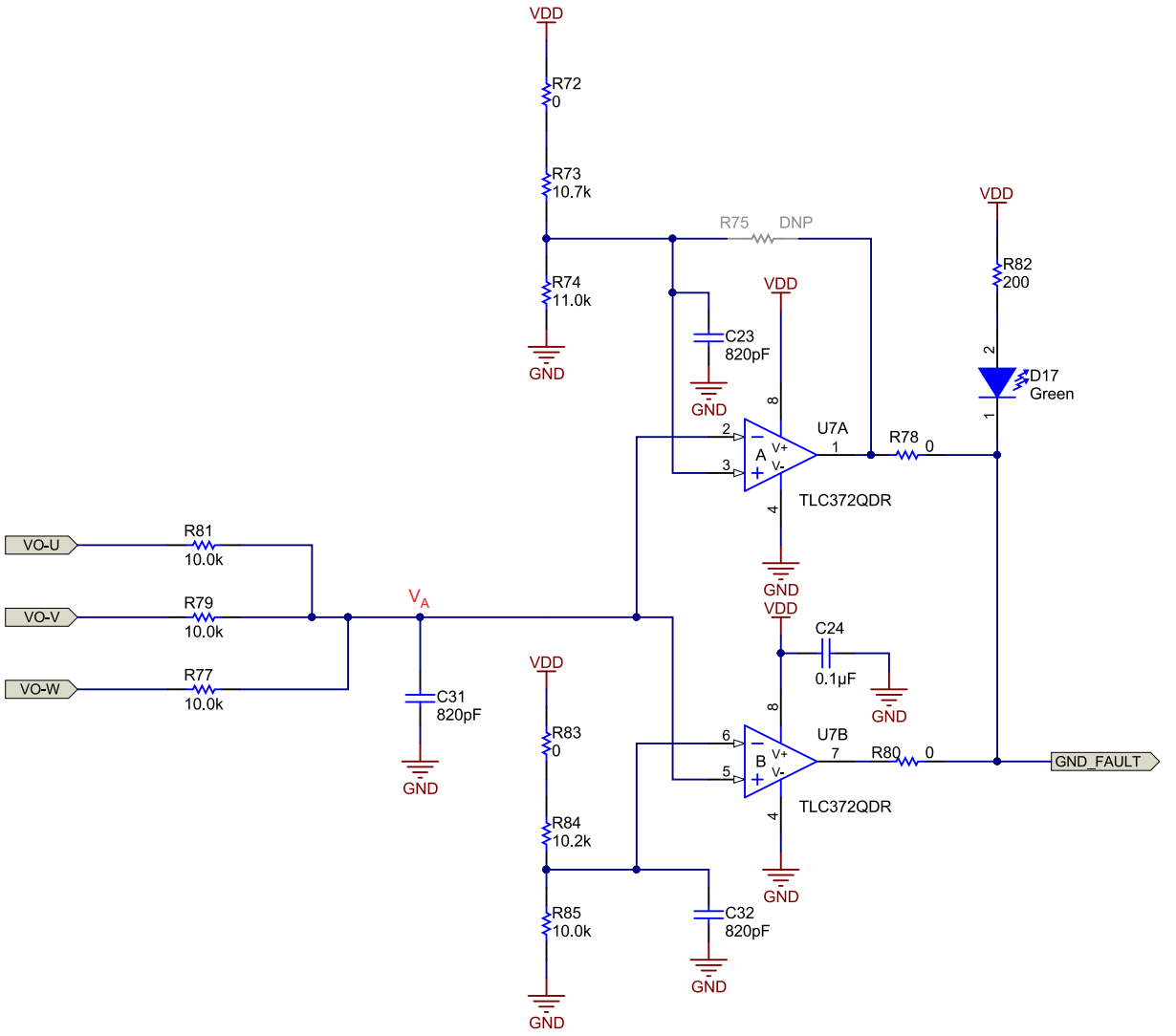

Figure 9. Ground Fault Detection Circuit

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2.5 5-V Input to 3.3-V Rail

Considering the design requirement to connect to 3.3 V MCU, it is necessary to provide 3.3 V supply to the DRV421. For converting 5 V to 3.3 V, an LDO is used. The TLV1117LV33 is selected for the following reasons:

- Input voltage range: 2 V to 5.5 V (6-V absolute maximum)
- Output current: up to 1 A
- Temperature range: –40°C to +125°C

It is important to check the thermal stress on the LDO. The total power it has to dissipate is calculated in Equation 12.

$$P_{LDO(max)} = \left(V_{LDO(IN)} - V_{LDO(OUT)}\right) \times i_{LDO(max)} = (5\,V - 3.3\,V) \times 300\,mA = 0.51\,W \quad (12)$$

For package selection, θ_{JA} is calculated (see Equation 13).

$$\theta_{JA(max)} = \frac{(T_J - T_A)}{P_{D(max)}} = \frac{(125°C - 85°C)}{0.51} = 78.43°C/W \quad (13)$$

The LDO should have a package where θ_{JA} is ≤ 78.43°C/W. Table 1 is from the TLV1117-33 data sheet, and a DRJ (SON8) package is suitable.

Table 1. Thermal Information for TLV1117-33

THERMAL METRIC		TLV1117							UNITS
		PowerFlex		DRJ (8 pins)	DCY (4 pins)	KVU (3 pins)	KCS, KCT (3 pins)	KTT (3 pins)	
		KTE (3 pins)	KTP (3 pins)						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.6	49.2	35.3	104.3	50.9	30.1	27.5	°C/W
$R_{\theta JC\_top}$	Junction-to-case (top) thermal resistance	34.7	60.6	36.5	53.7	57.9	44.6	43.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.2	3.1	60.5	5.7	34.8	1.2	17.3	
ΨJT	Junction-to-top characterization parameter	5.9	8.7	0.2	3.1	6	5	2.8	
ΨJB	Junction-to-board characterization parameter	3.1	3	12	5.5	23.7	1.2	9.3	
$R_{\theta JC\_bottom}$	Junction-to-case (bottom) thermal resistance	3	3	4.7	—	0.4	0.4	0.3	
$R_{\theta JP}$	Thermal resistance between the die junction and the bottom of the exposed pad	2.7	1.4	1.78	—	—	3	1.94	

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The schematic of the 5-V to 3.3-V conversion using an LDO (TLV1117-33) is shown in Figure 10. Diode D16 indicates the availability of the VDD rail. The board supply comes from an external source given at the J14 or J11 connector. The device is internally compensated to be stable with 0-Ω equivalent series resistance (ESR) capacitors. X5R and X7R type capacitors are best because they have minimal variation in value and ESR over the temperature range. Capacitor C29 is an input capacitor, and capacitors C27, C26, C25, and C28 are output capacitors.

Although an input capacitor is not required for the stability of the TLV1117LV33, C29 can impove the source impedance, noise, or PSRR for the LDO. In most LDOs, the band gap is the dominant noise source. Diode D18 is for reverse polarity protection. J12 is placed to bypass the LDO and give 5-V to the VDD rail.

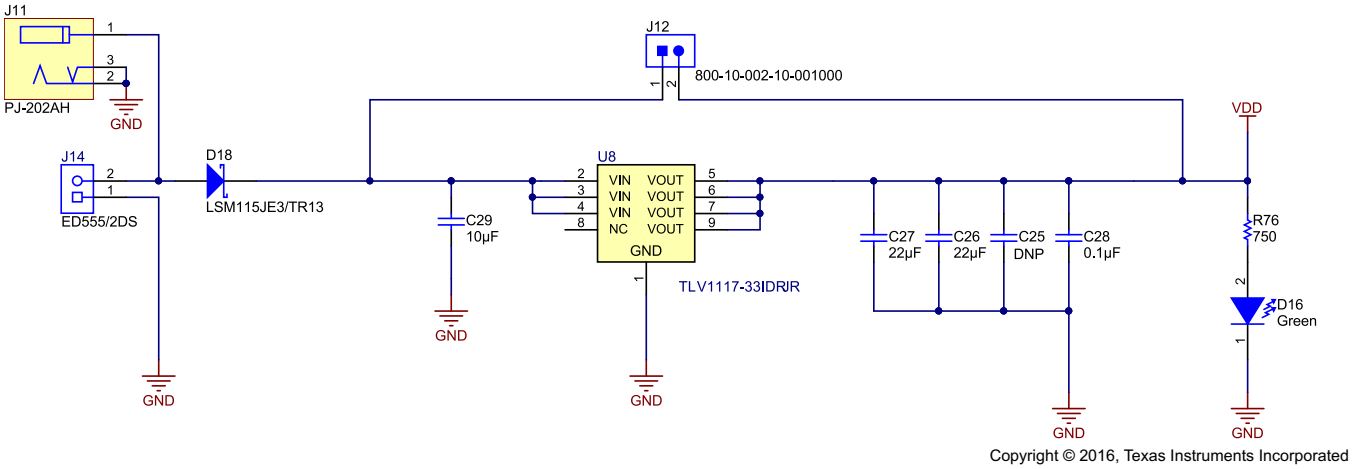

Figure 10. Schematic of 5-V to 3.3-V Converter Using TLC1117-33

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3 Getting Started Hardware

Figure 11 shows the TIDA-00905 board, with the power-supply input, jumper configuration and the signal position used for testing. The output is measured between VOUT and REFOUT for each phase.

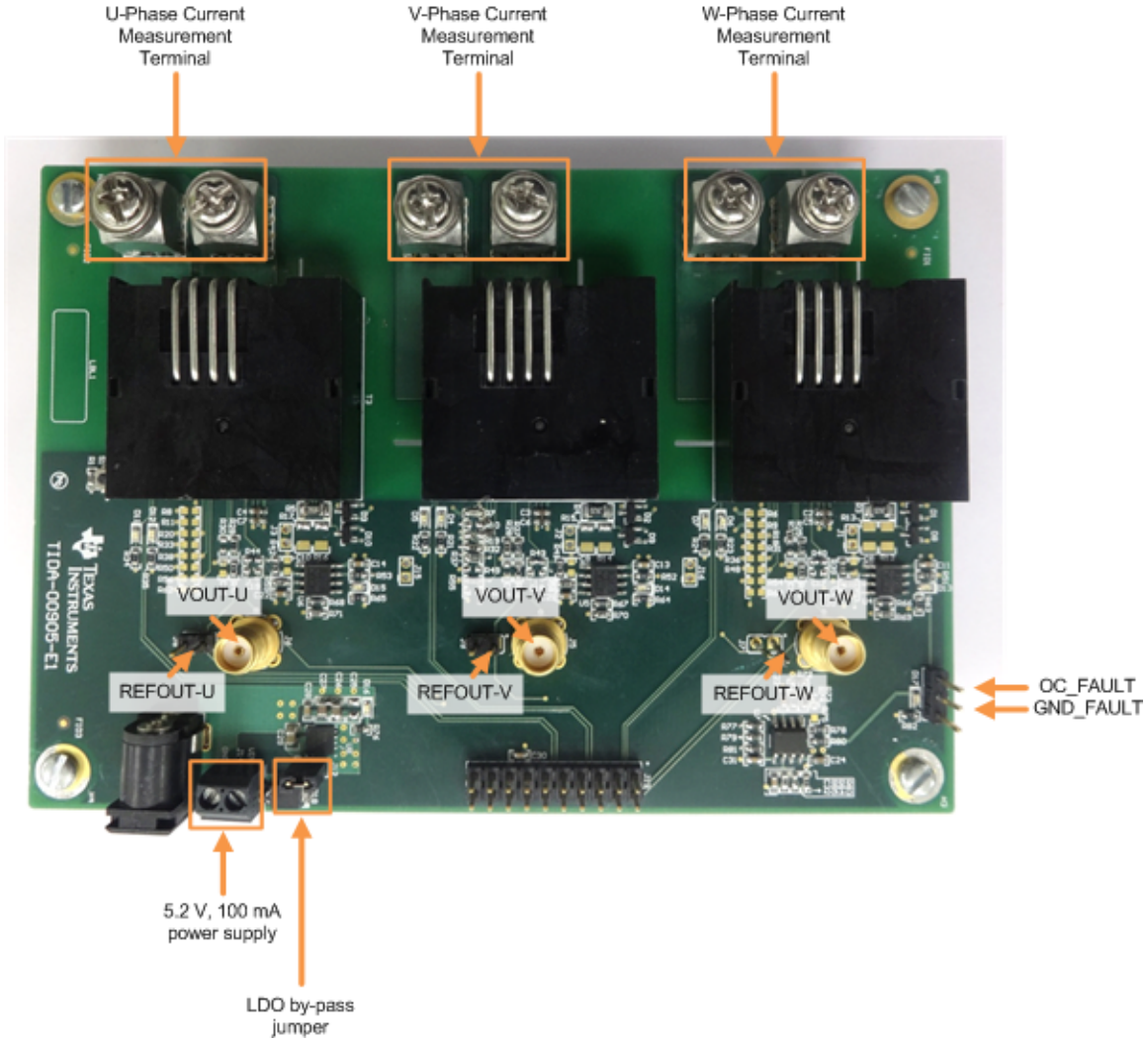

Figure 11. Getting Started With TIDA-00905 Board

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4 Testing and Results

The measurement performance is validated by AC and DC accuracy tests, step response and signal-to-noise ratio (SNR) measurements. A short-circuit test and ground fault is simulated to validate the performance of the overload selection and ground fault detection feature.

4.1 AC Accuracy and Temperature Drift

The AC accuracy test is done for a single measurement channel. The output is measured in RMS Voltage between the VOUT and REFOUT signals of the corresponding measurement channel using a 6½ digital multimeter (DMM). The accuracy test is done to obtain the error in measuring the motor current. The test uses a current standard to generate 0 A to 50 A_{RMS} sine waveform with a frequency of 50 Hz. The error in AC readings because of temperature drift is obtained by placing the TIDA-00905 board in a thermal chamber at –25˚C, +25˚C, and +85˚C.

Figure 12 shows the relative error versus the input current of the motor current. The uncalibrated current measurement at 25˚C is obtained by using the theoretical scale factor (refer to Section 2.2). The uncalibrated accuracy is within the tolerance of ±1.5%. The uncalibrated current measurement readings are calibrated with respect to input reference current by a best fit line; this gives the calibrated scale factor. The scale factor is used for the calibrated readings at 25˚C, –25˚C and 85˚C.

Figure 13 shows the plot of full scale error versus the input motor current, the error varies by ±1% from –25˚C to 85˚C.

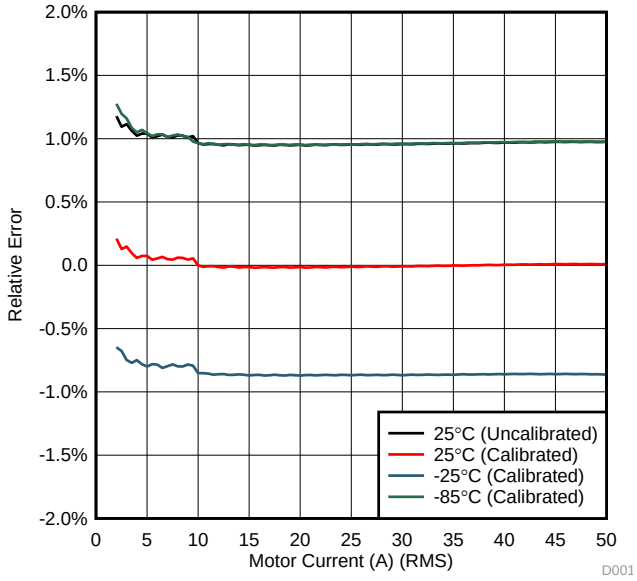

Figure 12. Relative Error versus Motor Current

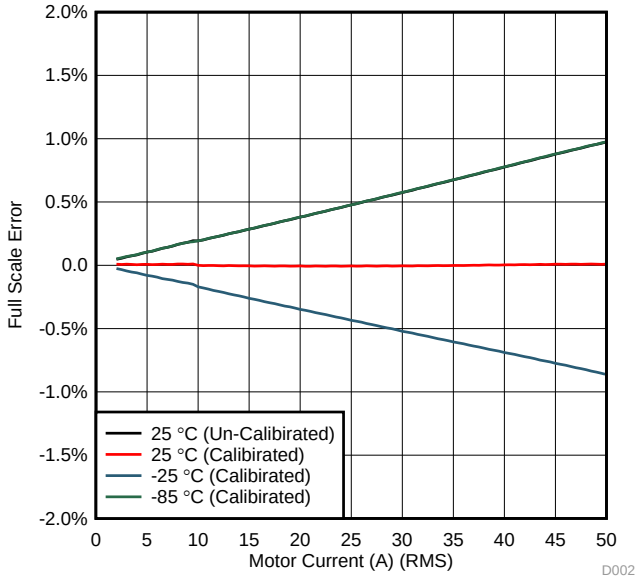

Figure 13. Full Scale Error versus Motor Current

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Figure 14 shows the output versus input transfer graph after calibration (no gain or offset errors). The errors remaining are only nonlinear errors. Figure 15 shows the nonlinear error in this transfer graph. The measurement is highly linear as the non-linearity errors are with in ±0.05%.

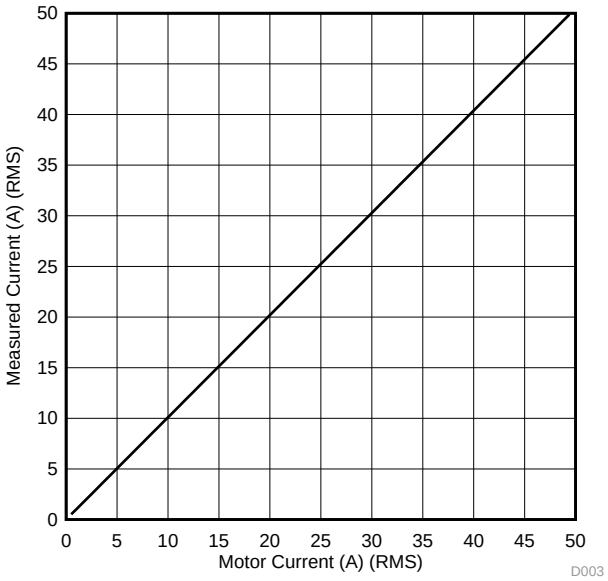

Figure 14. Output versus Input Transfer Graph

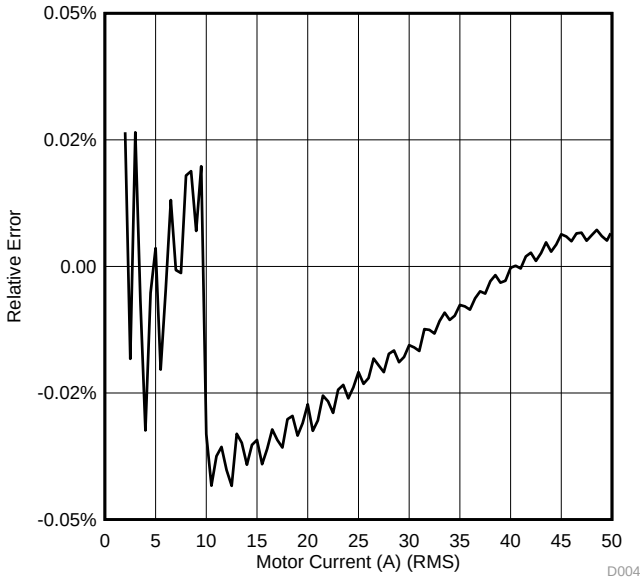

Figure 15. Relative Error versus Motor Current Calibrated at 25°C

4.2 DC Accuracy

The DC accuracy test is done for a single measurement channel. The output is measured in Voltage between VOUT and REFOUT signal of the corresponding measurement channel using a 6½ DMM.

Figure 16 shows the full scale error versus the input current of the motor current. The uncalibrated current measurement at 25˚C is obtained by using the full scale error versus the motor current, (refer to Section 2.2). The uncalibrated accuracy is within the tolerance of ±1.5% in the full scale measurement range. The uncalibrated current measurement readings are calibrated with respect to input reference current by a best fit line; this gives the calibrated scale factor. This scale factor is used for the calibrated readings at 25˚C.

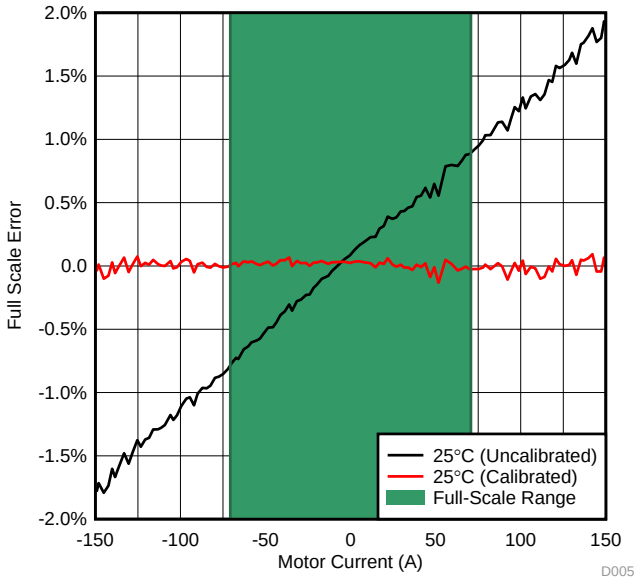

Figure 16. DC Accuracy

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4.3 Measuring the SNR

The SNR test is done by applying a 50 A, 50 Hz AC to a signal measurement channel. The board is interfaced to the ADS7253 EVM, which is a 12-bit pseudo-differential ADC. At a sampling rate of 1 MSPS, 13,000 samples are captured. Figure 17 shows the captured waveform data, the y-axis is the input to the ADC in volts. Figure 18 shows the frequency spectrum of the data. The amplitude has been normalized to the FSR of the ADC, but the applied signal does not cover the full scale range. Hence the measured SNR is adjusted by the amount the fundamental peak is below the 0 dB mark on the frequency spectrum. This is done to compare with the SNR value in datasheet of ADS7253 which is given for FSR. The total SNR is 63 dB + 8.98 dB = 71.98 dB. This SNR is close to the SNR for the 12 bit-ADS7253 ADC.

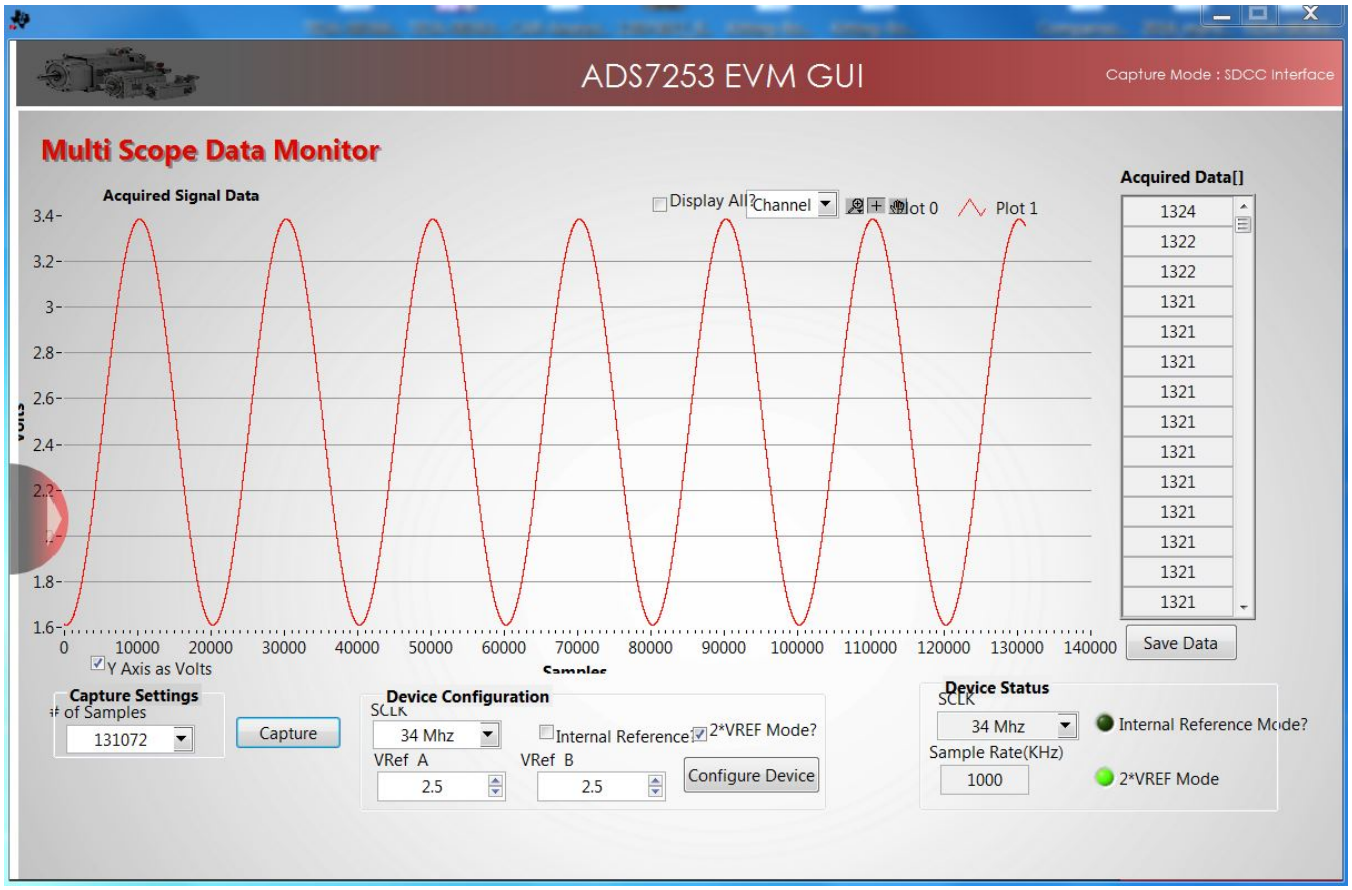

Figure 17. Plot of Captured Data

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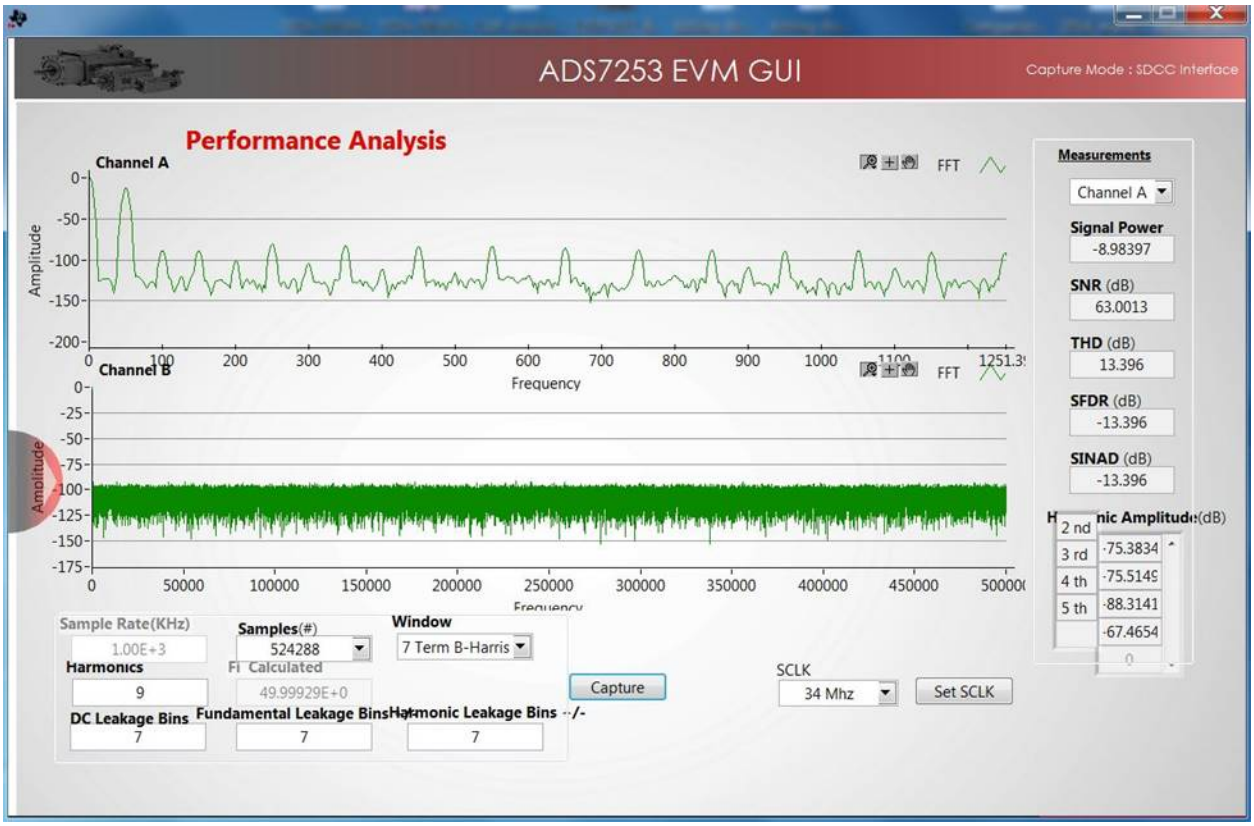

Figure 18. Spectrum of Captured Data Noise and Fundamental

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4.4 Step Response

The step response validates the propagation delay and the rise time of the current measurement circuit to a step change in the motor current. Figure 19 and Figure 20 show the VOUT to REFOUT signal during a step change in the primary conductor and measure the rise time and the propagation delay.

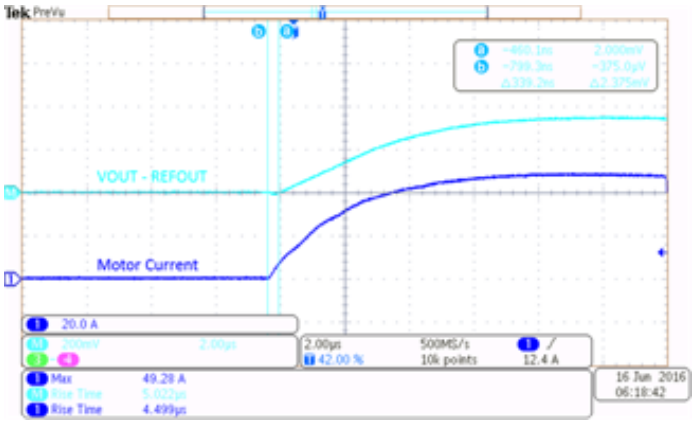

Figure 19. Step Response and Rise Time

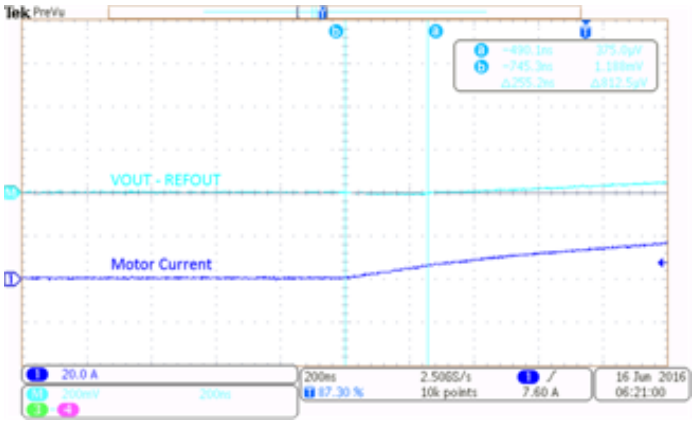

Figure 20. Step Response and Propagation Delay Time

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4.5 Overcurrent Detection Test

The overcurrent circuit detection test validates the response time for the OC_FAULT signal to activate when a high current occurs in the primary coil of the magnetic module. This test validates the time delay in magnetic module (DRV421 fluxgate sensor). Section 2.3 describes the thresholds set in the window comparator.

Figure 21 shows the test diagram; The MOSFET switch is turned on for duration of 12 µs to generate a step primary current in the magnetic module.

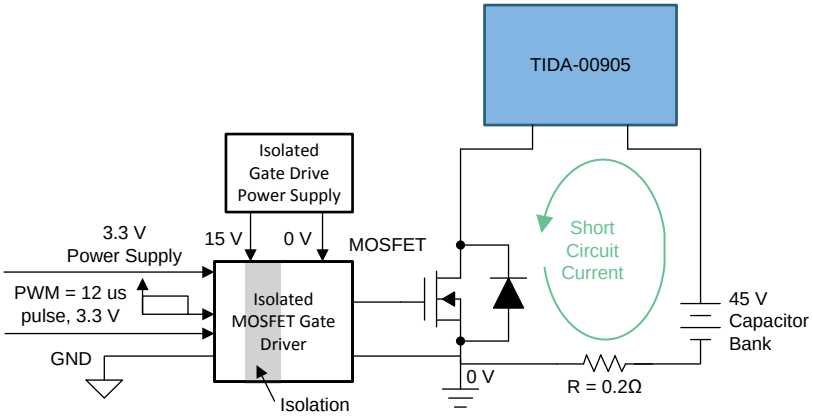

Figure 21. Short-Circuit Test Diagram

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The waveform for over current detection for a positive current is shown is Figure 22 and Figure 23. The time delay between the input current at the threshold of 150.1 A and OC_FAULT signal going low is 0.6 µs.

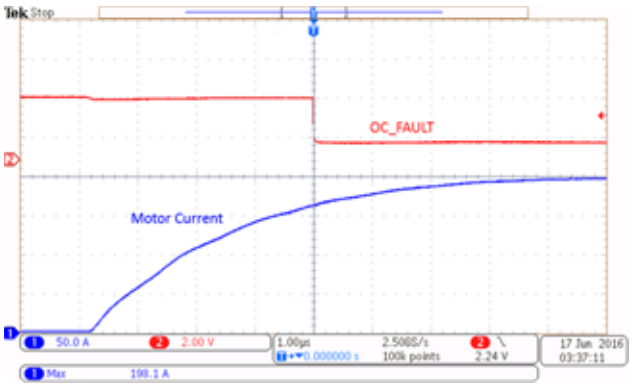

Figure 22. Overcurrent Detection for Positive Current

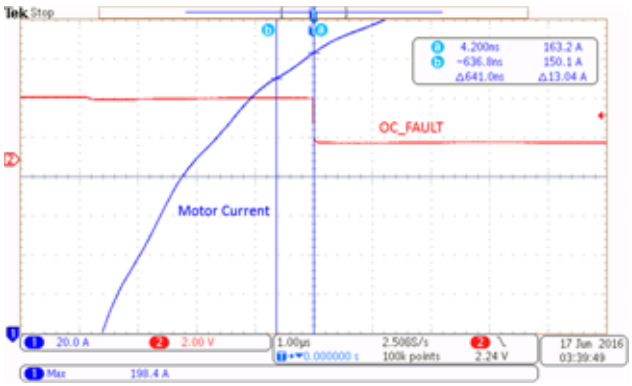

Figure 23. Zoomed-in View of Figure 22

Similarly, Figure 24 and Figure 25 show overcurrent detection for a negative current. The detection time for the negative current is 0.1 µs. The detection time delay is less than the 5 µs allowed for an IGBT overcurrent event. Hence, there is enough time from the activation of OC_FAULT to turn off typical IGBT modules before it becomes damaged.

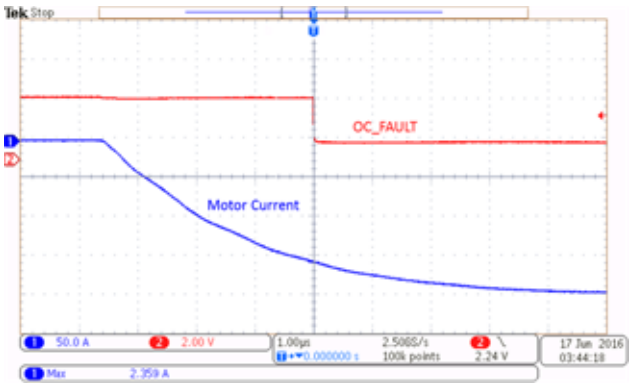

Figure 24. Overcurrent Detection for Negative Current

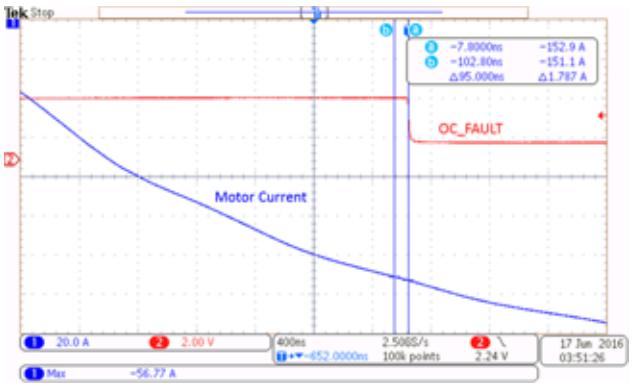

Figure 25. Zoomed-in View of Figure 24

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4.6 Ground Fault Detection

The ground fault circuit is tested by applying a step current to one measurement channel while the other two channels have zero current. The test setup to generate the step current is same as Figure 21. The circuit threshold setting is detailed in Section 2.4.

The ground fault detection waveform for a positive step current is shown in Figure 26 and Figure 27. The ground fault threshold is 8.2 A, the GND_FAULT signal is activated in 1.43 µs. Similarly, Figure 28 and Figure 29 show the ground fault detection to a negative step current. The response time to the threshold of 8.2 A is 1.23 µs. This fast detection time delay should provide enough time to turn of the system before a catastrophic failure in the system.

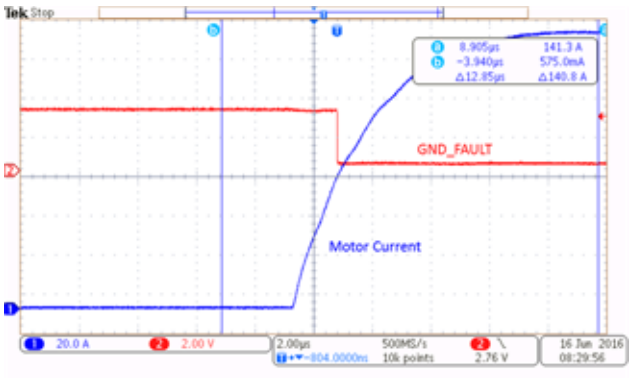

Figure 26. Ground Fault Detection for Positive Current

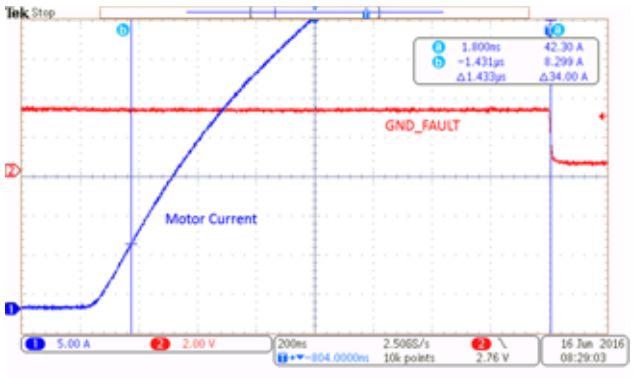

Figure 27. Zoomed-in View of Figure 26

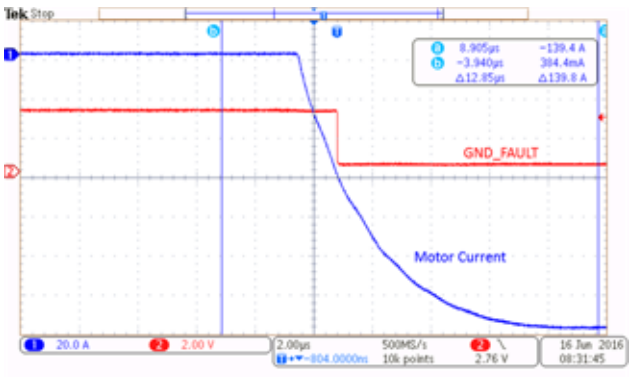

Figure 28. Ground Fault Detection for Negative Current

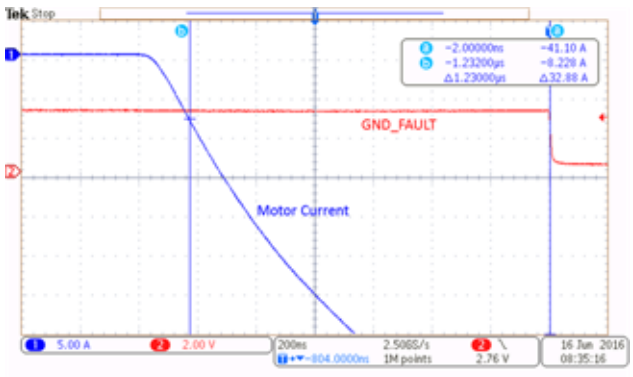

Figure 29. Zoomed-in View of Figure 28

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00905.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00905.

5.3 PCB Layout Recommendations

5.3.1 Layout Considerations for DRV421

Figure 30 shows the layout section for the Sumida module and DRV421 on TIDA-00905 board. The DRV421 has a high sensitivity to magnetic fields to enable design of a closed-loop current sensor with best-in-class precision and linearity.

It is important to observe proper PCB layout techniques because any current-conducting wire in the direct vicinity of the DRV421 generates a magnetic field that may distort measurements. As shown in Figure 30, the current conducting wires should be routed in pairs; that is, route a wire with an incoming supply current next to, or on top of the return current path. The opposite magnetic field polarity of these connections cancel each other. To facilitate this layout approach, the DRV421 positive and negative supply pins are located next to each other. The compensation coil connections are also placed close to each other as a pair to reduce coupling effects. Vertical current flow (for example, through via) generates a field in the fluxgate-sensitive direction; hence, is why the number of vias is minimized in the vicinity of the DRV421.

Also, it is important to note that all passive components (for example, decoupling capacitors and the shunt resistor) are placed outside of the portion of the PCB that is inserted into the magnetic core gap (common passive components and some PCB plating materials contain ferromagnetic materials that are magnetizable). Also, all GND pins are connected to a local ground plane.

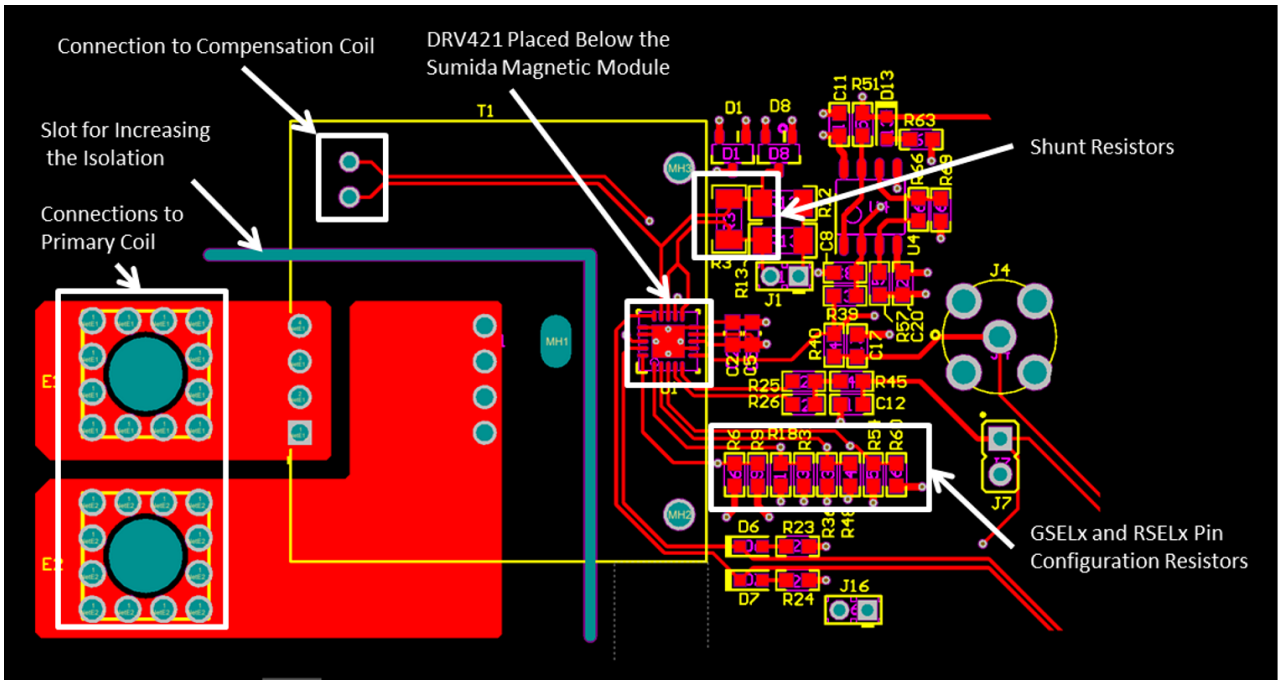

Figure 30. Layout Selection for Sumida Module and DRV421

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Figure 31 and Figure 32 show the power and ground layers (respectively) for the TIDA-00905 board.

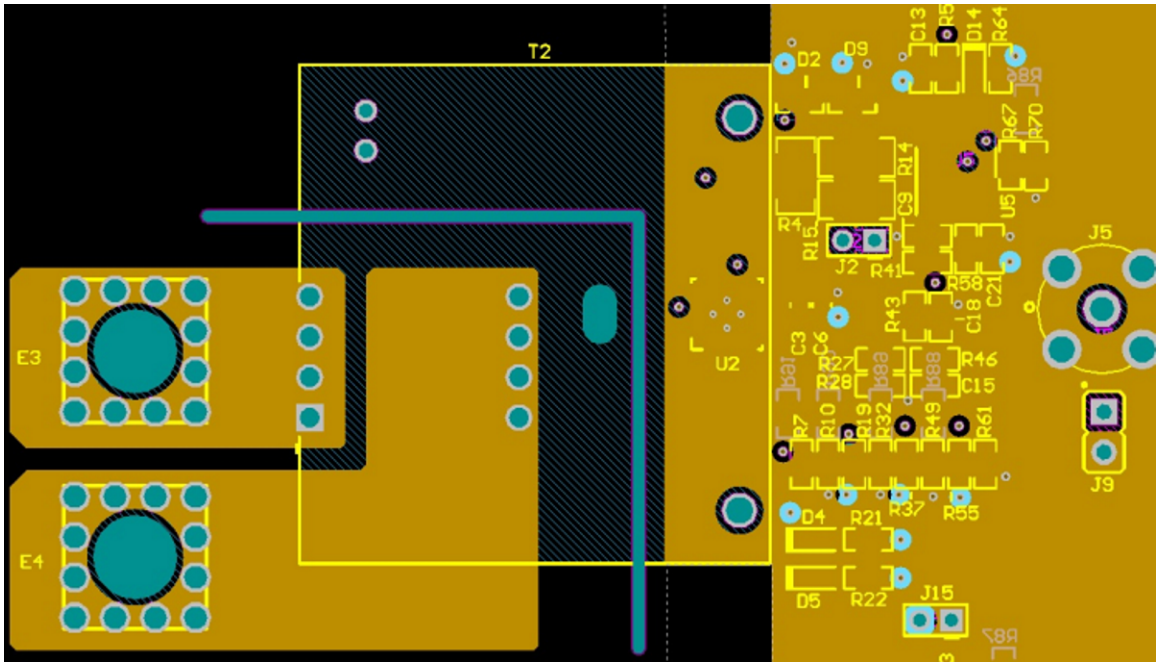

Figure 31. Power Layer for TIDA-00905

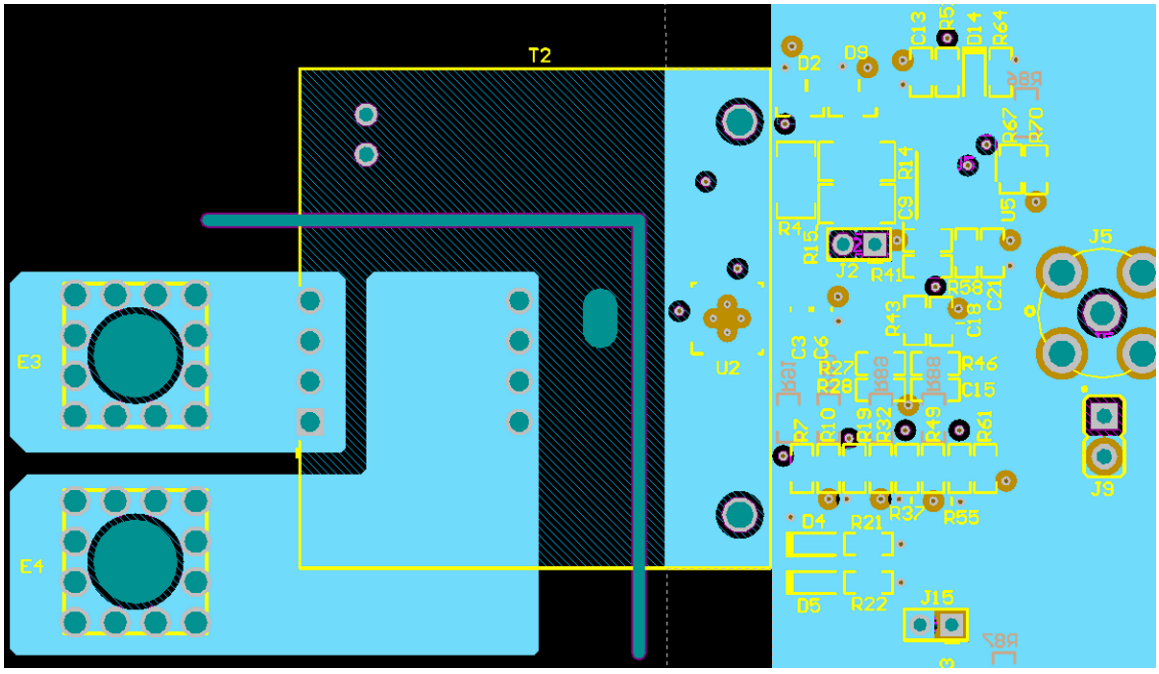

Figure 32. GND Layer for TIDA-00905

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5.3.2 Layout Prints

To download the layer plots, see the design files at TIDA-00905.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00905.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00905.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00905.

6 Software Files

To download the software files, see the design files at TIDA-00905.

7 Related Documentation

1. *±15A Current Sensor using Closed-Loop Compensated Fluxgate Sensor Reference Design*
2. *Designing with the DRV421: Closed Loop Current Sensor Specifications*
3. *Designing With the DRV421: Control Loop Stability*
4. *Designing with the DRV421: System Parameter Calculator*

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8 About the Author

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2016) to A Revision	Page
• Changed from preview draft	1

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