TI Designs: TIDA-01419

Four-Phase, 150-A Reference Design for Intel® Arria® 10 GX FPGAs Using TPS53647

Description

This reference design focuses on providing a compact, high-performance, multiphase solution suitable for powering Intel® Arria® 10 GX field-programmable gate arrays (FPGAs) with a specific focus on the 10AX115U145IVG variant. Integrated PMBus™ allows for easy output voltage setting and telemetry of key design parameters. The design enables programming, configuration, smart VID adjustment, and control of the power supply, while providing monitoring of input and output voltage, current, power, and temperature. TI's Fusion Digital Power™ Designer is used for programming, monitoring, validation, and characterization of the FPGA power design.

Resources

TIDA-01419	Design Folder
TPS53647	Product Folder
CSD95472Q5MC	Product Folder
Fusion Digital Power Designer	Product Folder

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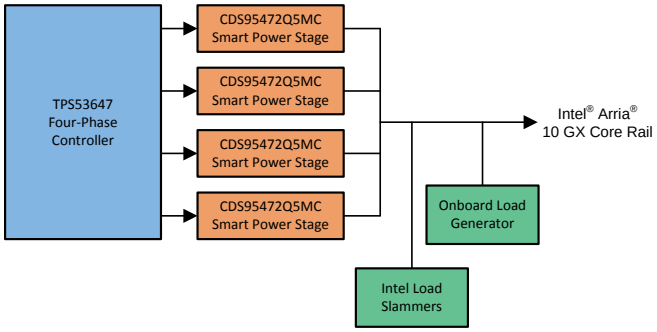
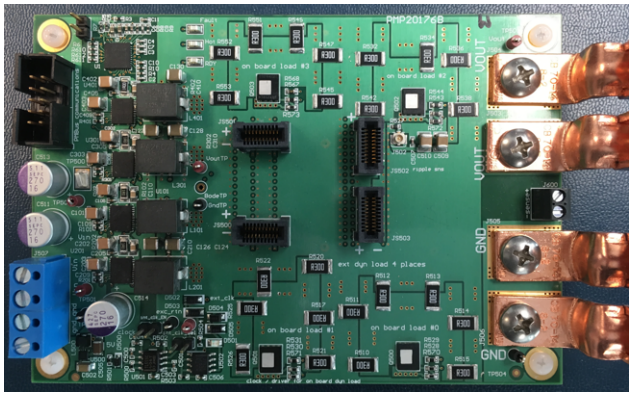
Features

- All Ceramic Output Capacitors
- D-CAP+™ Modulator for Superior Current-Sharing Capabilities and Transient Response
- Peak Efficiencies of 89% (V_{OUT} = 0.8 V) and 90% (V_{OUT} = 0.9 V) at 600 kHz
- Excellent Thermal Performance Under No Airflow Conditions
- Overvoltage, Overcurrent, and Overtemperature Protection
- PMBus Compatibility for Output Voltage Setting and Telemetry for V_{IN}, V_{OUT}, I_{OUT}, and Temperature
- PMBus and Pinstrapping Programming Options

Applications

- FPGA Core Rail Power
- Ethernet Switches
- Firewalls and Routers
- Telecom Base Band Units
- Test and Measurement





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1 System Description

The TIDA-01419 is a high-efficiency, power-dense design featuring a four-phase buck controller and TI's proprietary Smart Power Stages optimized for use in Intel® Arria® 10 GX FPGA core rail applications. These FPGAs are typically used in enterprise switching, telecom infrastructure, test and measurement, and cloud computing infrastructure environments with high utilization percentages that call for the high current and fast transient response that this design provides.

A 600-kHz switching frequency is used to minimize the size and number of output filter components while maintaining a thermal design current efficiency of 88.0%. The TPS53647 controller uses the D-CAP+™ multiphase modulator for fast transient response capabilities and tight regulation of the output voltage. The D-CAP+ modulator offers reliable current balancing between the four phases of the design that provides stability over a wide range of operating conditions and simple Type II compensation of the control loop. Additionally, the TPS53647 is compatible with TI's Smart Power Stages, like the CSD95472 used in this design, which offer optimized driver-FET solutions for high efficiency and integrated current-monitoring circuitry, that saves layout area and eliminates the requirement for external current sensing components.

Design modifications can be done in WEBENCH® Designer if a lower-power Altera 10 GX FPGA is used, or a different output capacitor mix is desired.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input supply	12 V ±5%
Nominal output voltage	0.9 V
DC regulation	<1.2%
DC ripple	2% max
AC ripple	±5%
Max output current	150 A
Typical output current	100 A
Max load step	75 A at 500 A/µs
Number of phases	4
Switching frequency	600 kHz

2 System Overview

2.1 Block Diagram

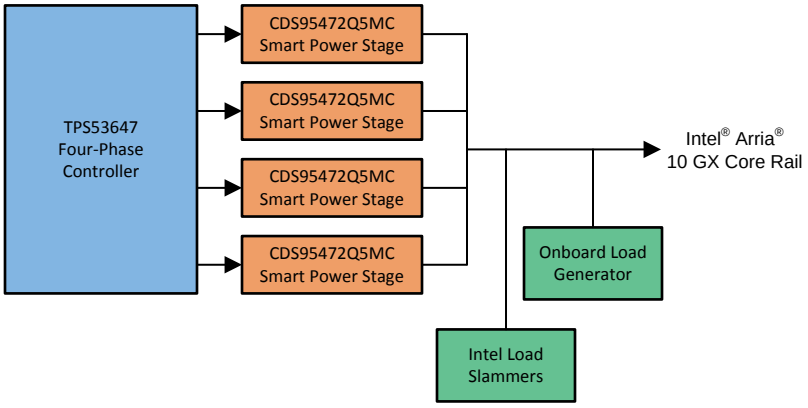

Figure 1. TIDA-01419 Block Diagram

2.2 Highlighted Products

2.2.1 TPS53647 – Four-Phase, D-CAP+™ Step-Down Buck Controller With NVM and PMBus™ Interface for ASIC Power and High-Current Point-of-Load

Features:

- 8-bit selectable boot voltage through pinstrap or non-volatile memory (NVM)
- One-, two-, three-, or four-phase operation
- 1.8-V or 3.3-V compatible PMBus™ system interface for fault monitoring and voltage, current, power, and temperature telemetry
- D-CAP+ modulator and eight independent levels of overshoot and undershoot reduction for excellent transient response
- Adjustable voltage positioning
- Dynamic phase shedding with programmable current threshold
- 6×6-mm, 40-pin, QFN PowerPAD™ integrated circuit package

2.2.2 CSD95472Q5MC – 60-A Synchronous Buck NexFET™ Smart Power Stage With DualCool™Package

Features:

- 60-A continuous current capability
- Low power loss of 2.3 W at 30 A
- High-frequency operation up to 1.25 MHz
- 3.3-V and 5-V pulse-width modulation (PWM) compatible
- Temperature-compensated bidirectional current sense
- Analog temperature output
- Integrated bootstrap diode and optimized deadtime
- 5-mm × 6-mm SON, low inductance, DualCool™ packaging

3 Hardware, Software, and Test Setup

3.1 Required Hardware and Software

3.1.1 Hardware

- +12-V supply capable of 20 A
- +5-V supply capable of 1 A
- Function generator capable of pulses with < 1-µs rise times (optional)
- Oscilloscope with differential and passive probes
- Digital multimeter
- Three 25-A Intel load mini slammers and associated control board[6] (optional)
- USB interface adapter EVM

The function generator must be used if the onboard clock generator is not used to drive the onboard load transient generator. Intel mini load slammers can be used in place of the entire onboard load circuitry if desired.

3.1.2 Software

This design uses TI's Digital Fusion Power Designer software.

3.2 Test Setup

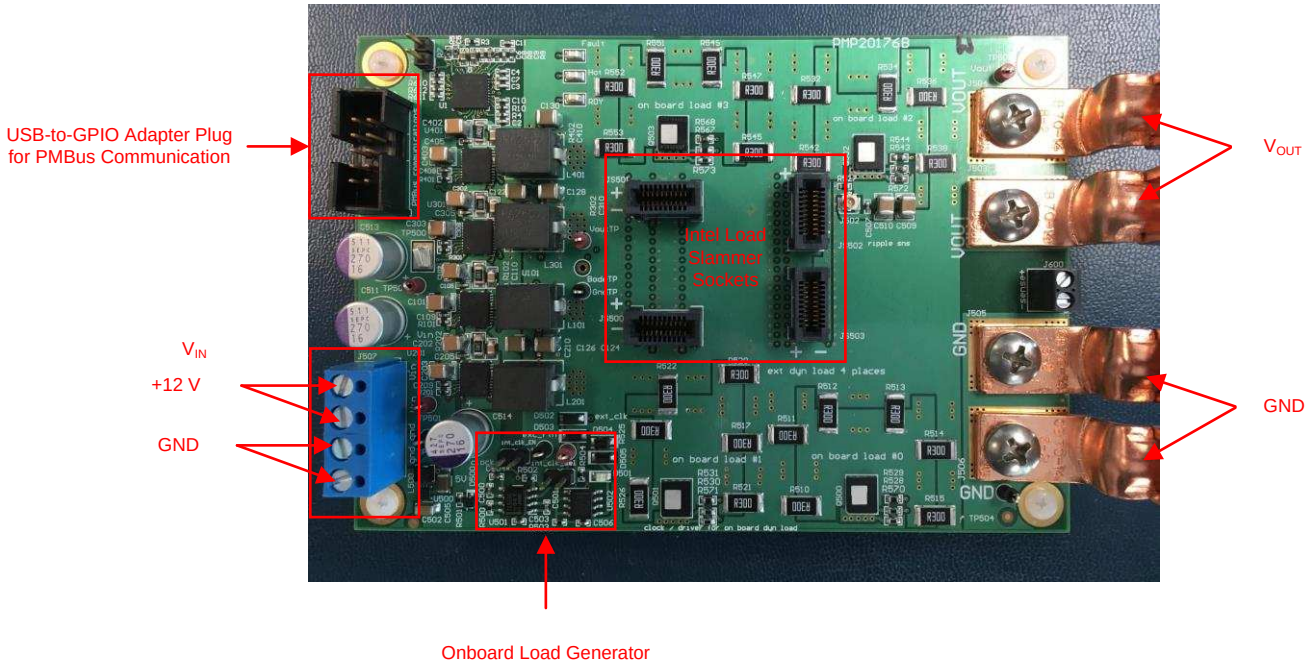

Figure 2. TIDA-01419 Test Setup

4 Test Results

4.1 Efficiency and Power Loss

Peak efficiencies of 89% (V_{OUT} = 0.8 V) and 90% (V_{OUT} = 0.9 V) were measured for this design. At the thermal design current (TDC) of 100 A, the efficiencies were 87% and 88% for 0.8 V and 0.9 V, respectively. When the load current was set to the maximum current of 150 A the efficiency was 83% for V_{OUT} = 0.8 V and 84% for V_{OUT} = 0.9 V. The curves also include the losses associated with the 5-V power stage VDD rail.

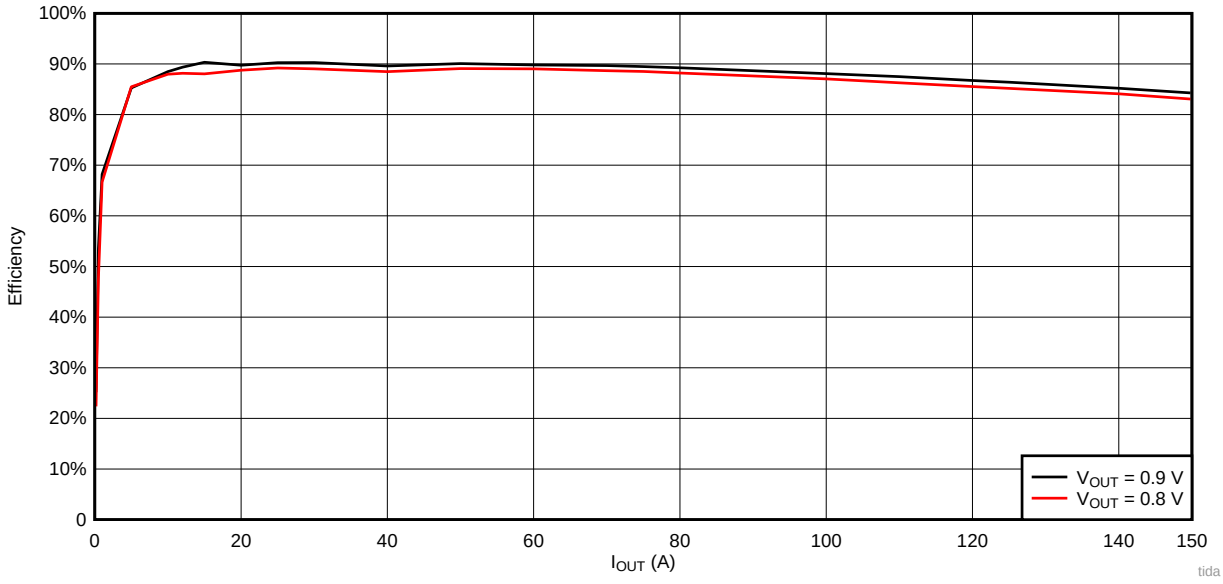

Figure 3. TIDA-01419 Efficiency Curves – V_{IN} = 12 V, 600 kHz

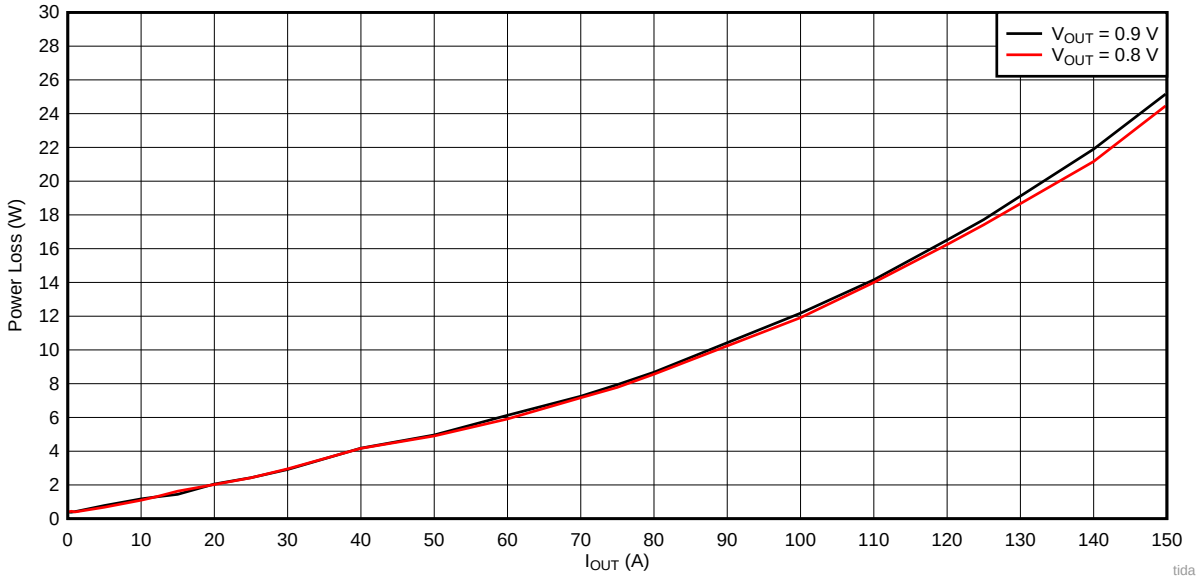

Figure 4. TIDA-01419 Power Loss Curves – V_{IN} = 12 V, 600 kHz

4.2 Steady-State Regulation

Steady-state stability, switching frequency, and DC ripple were tested at the 100-A TDC current for output voltages of 0.8 V and 0.9 V. No abnormalities were seen during testing. Care should be taken to ensure that the noise floor of the output voltage differential probe does not impact the results causing false failures in output ripple or stability. TI recommends to monitor a phase node as well to check against any possible questions regarding stability that may be attributed to a noisy differential probe. The design is likely stable if the switching frequency is consistent between phase pulses and varies within the TPS53647 datasheet limits.

Load regulation and the PMBus output voltage setting feature were also tested and found to comply with the specifications of the design. Note that the voltages steps in Figure 6 are exaggerated to be easily seen through the Fusion Digital Power™ graphical user interface (GUI) monitoring software. The actual application keeps the output voltage between 0.8 V and 0.9 V.

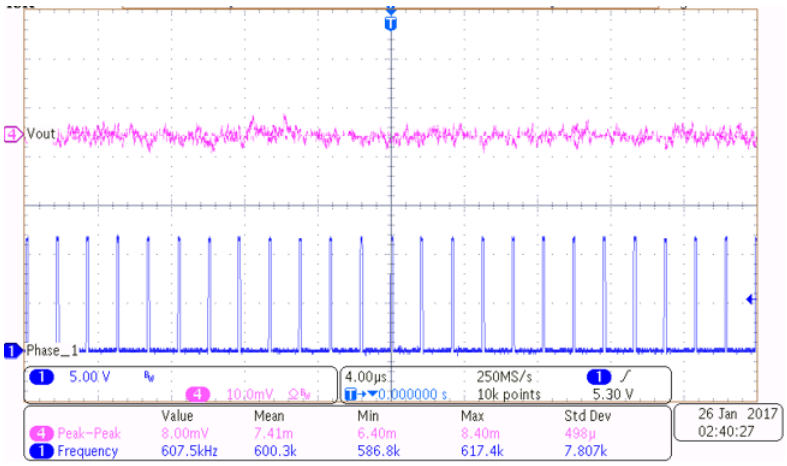

Figure 5. Steady State: 0.8 V, 100 A

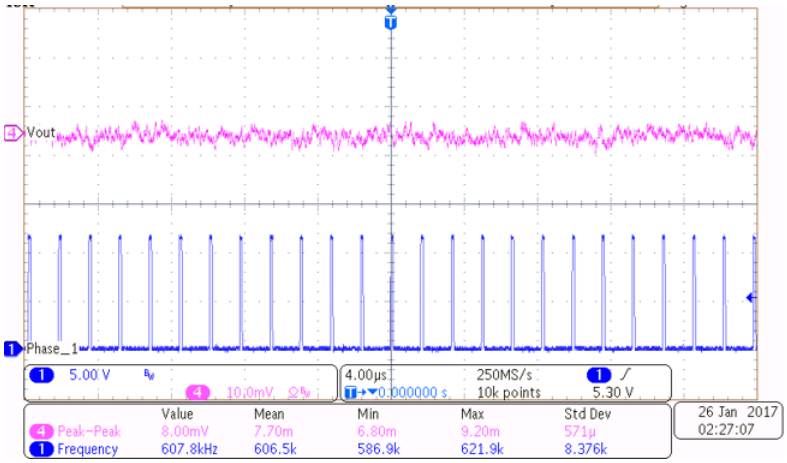

Figure 6. Steady State: 0.9 V, 100 A

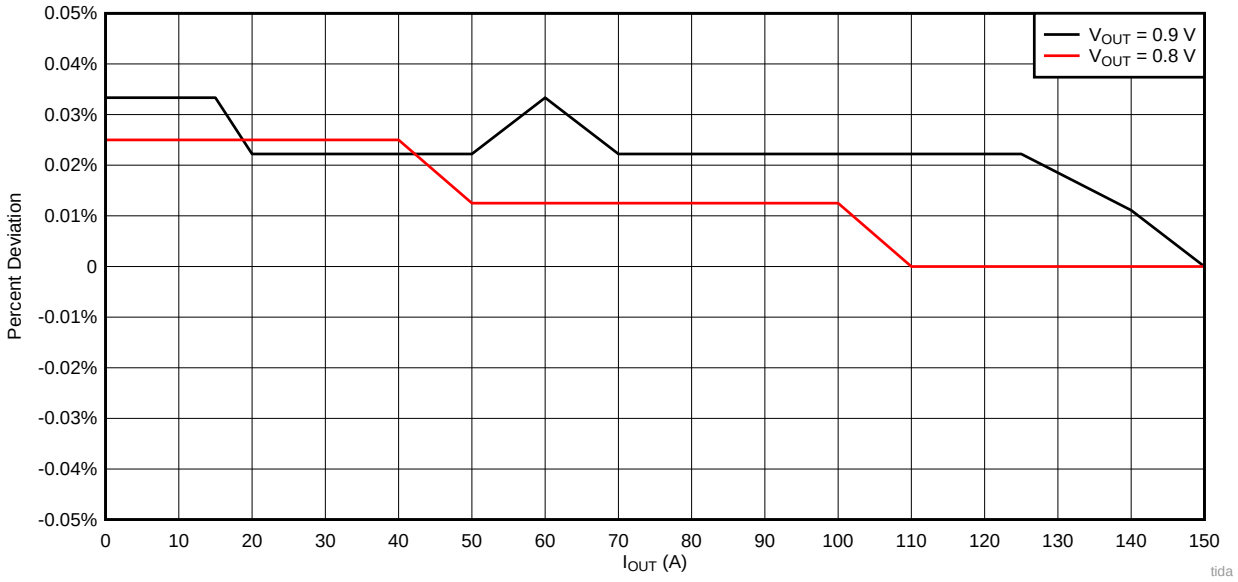

Figure 7. TPS53647 Load Regulation – V_{IN} = 12 V, 600 kHz

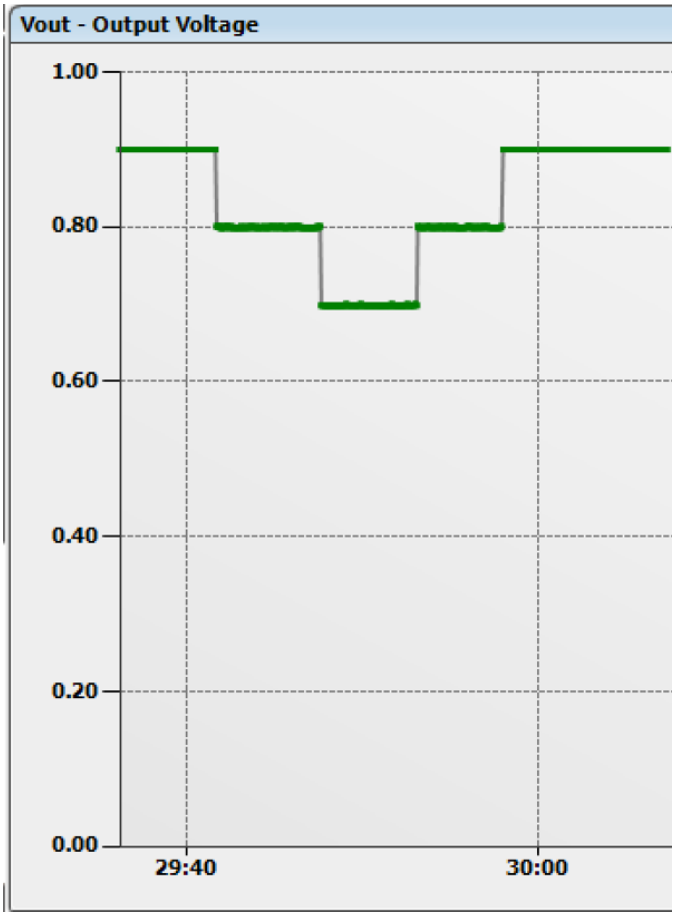

Figure 8. FPGA Core Smart VID Adjustment Using PMBus™ Commands

4.3 Thermal Performance

The design was placed under 25-A, 50-A, and 100-A loads at an output voltage of 0.9 V for five minutes before measurements were taken of the power stages and inductors using an infrared camera. During testing, the ambient temperature was 25ºC with no airflow across the board or heatsinks placed on the CSD95472 power stages.

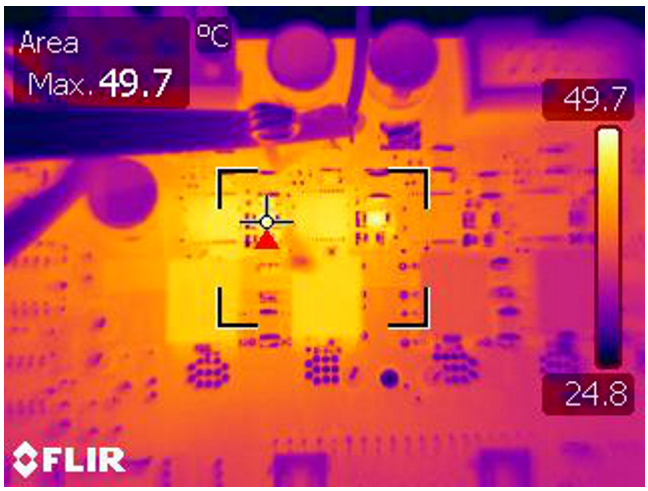

Figure 9. CSD95472 Temperature: 25-A Load

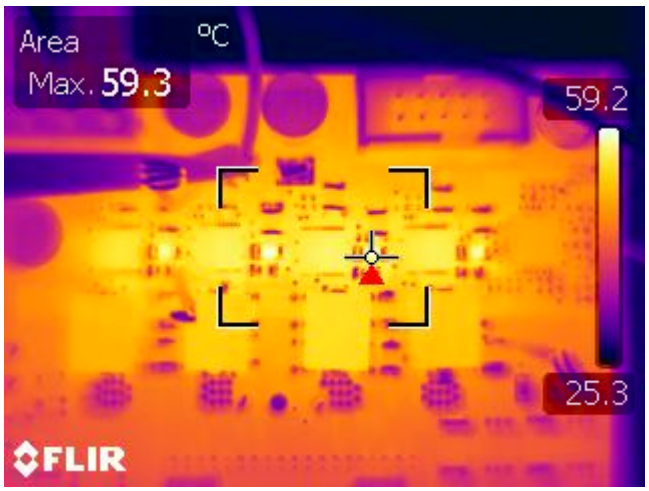

Figure 10. CSD95472 Temperature: 50-A Load

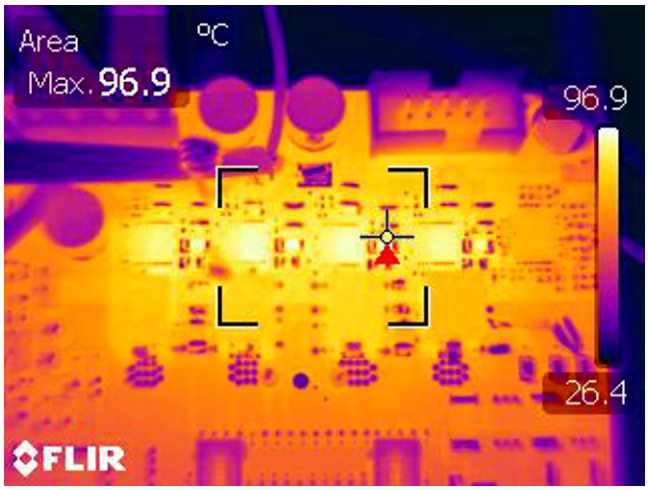

Figure 11. CSD95472 Temperature: 100-A Load

4.4 Transient Response

A load step of 75 A was applied to the TPS53647 regulator under two test conditions. The first test condition being from 50 A to 125 A and the second from 75 A to the maximum load of 150 A. Under both conditions the duty cycle was swept from 10% to 83% to check for stability under a wider range of operational corners. With no DC load line and an AC tolerance of ±5%, a peak-to-peak voltage swing of 90 mVpp is allowed at the nominal output voltage of 0.9 V. No stability issues were seen during testing and the output voltage remained within the regulation window.

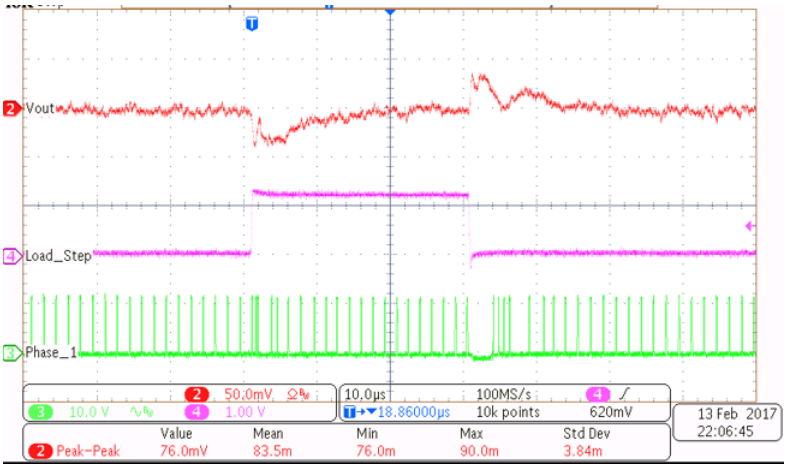

Figure 12. 50-A to 125-A Transient, 10% Duty Cycle

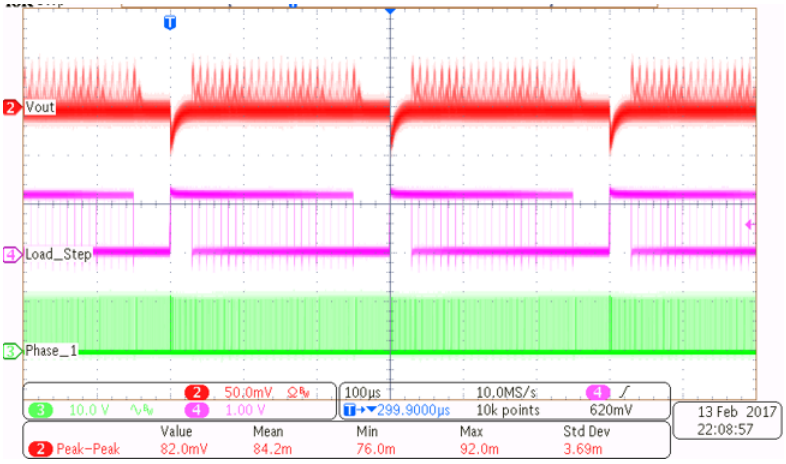

Figure 13. 50-A to 125-A Transient, 10% to 83% Duty Cycle Sweep

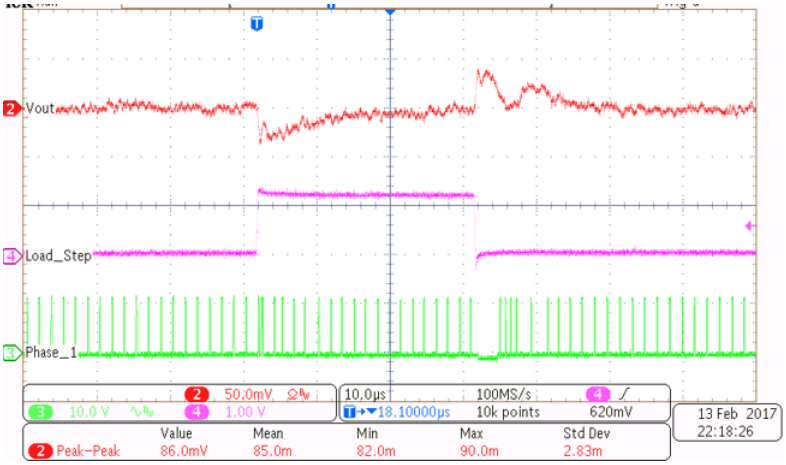

Figure 14. 75-A to 150-A Transient, 10% Duty Cycle

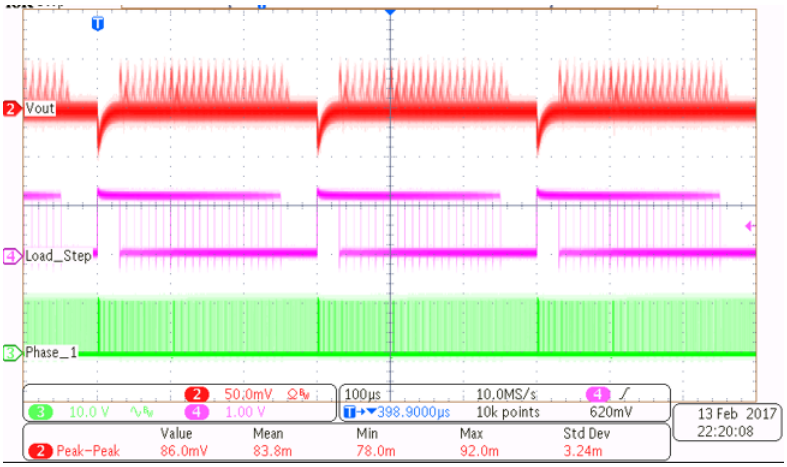

Figure 15. 75-A to 150-A Transient, 10% to 83% Duty Cycle Sweep

Table 2. Transient Response Validation Results

LOAD STEP	TRANSIENT SPECIFICATION AT NOMINAL OUTPUT VOLTAGE	VALIDATION RESULTS
75 A to 125 A	90 mVpp (±45 mV)	83.8 mVpp
100 A to 150 A	90 mVpp (±45 mV)	84.2 mVpp

4.5 Start-Up and Shutdown

Start-up and shutdown waveforms were taken at 10-A and 25-A loads while monitoring the enable, output voltage, and main phase node.

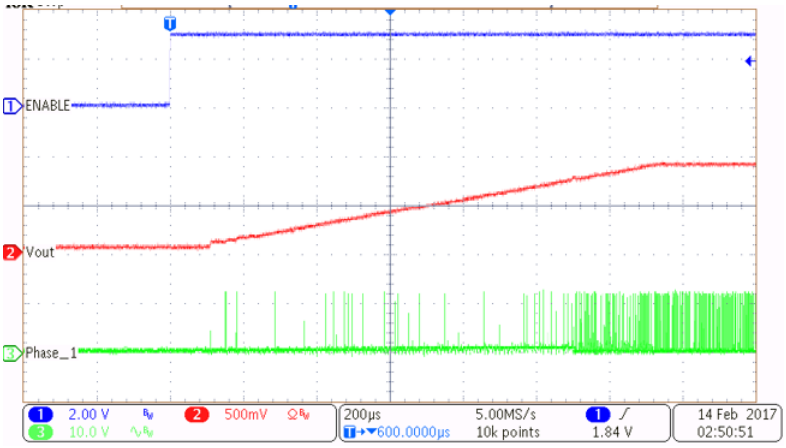

Figure 16. 10-A Start-Up

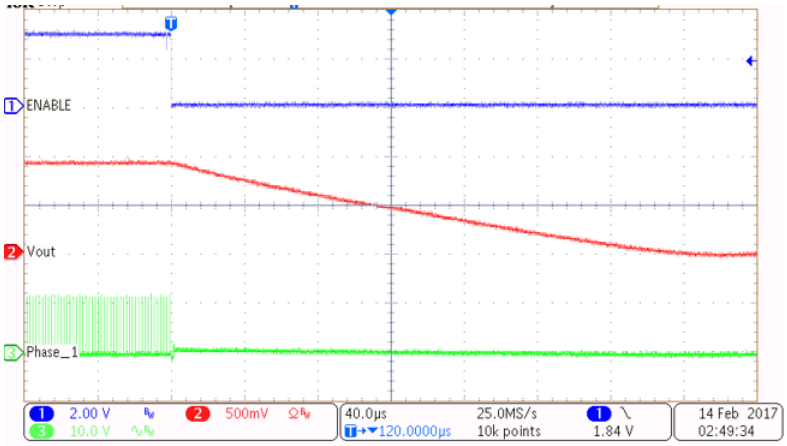

Figure 17. 10-A Shutdown

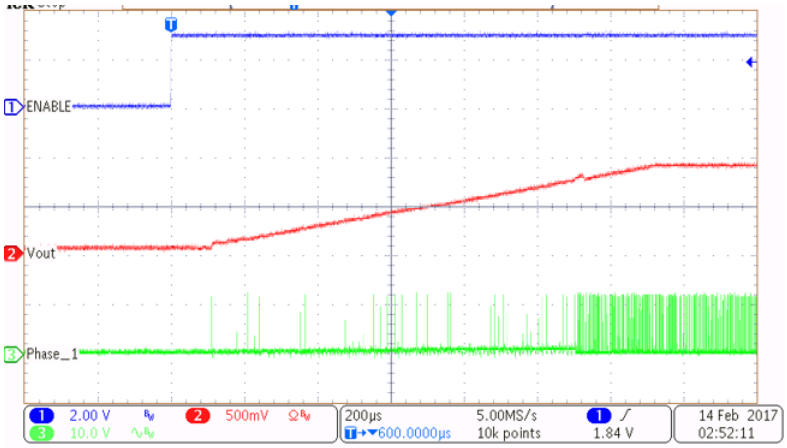

Figure 18. 25-A Start-Up

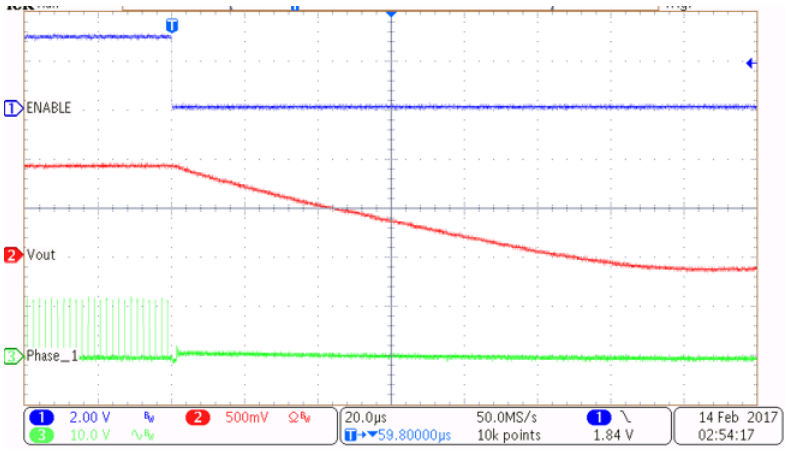

Figure 19. 25-A Shutdown

4.6 Protection Circuitry

When testing the protection circuit for this application, the TPS53647 device also performed admirably. The overcurrent and overtemperature protection features worked as intended when triggered, preventing the load and power field-effect transistors (FETs) from damage. Upon hitting the overcurrent limit, the controller went into hiccup mode and attempted to restart. Successful power-up only occurred after the high current was removed. After the overtemperature threshold was crossed, the phase node was tri-stated and the output voltage decayed to 0 V (according to the load current) until the part had cooled off.

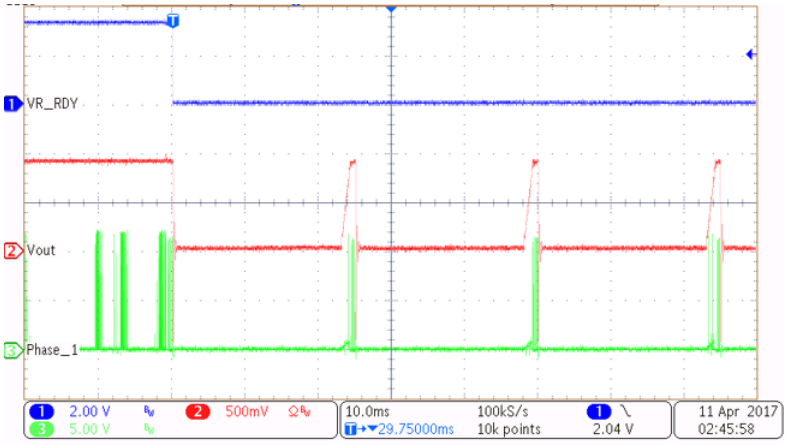

Figure 20. Overcurrent Shutdown Event With Hiccup Mode

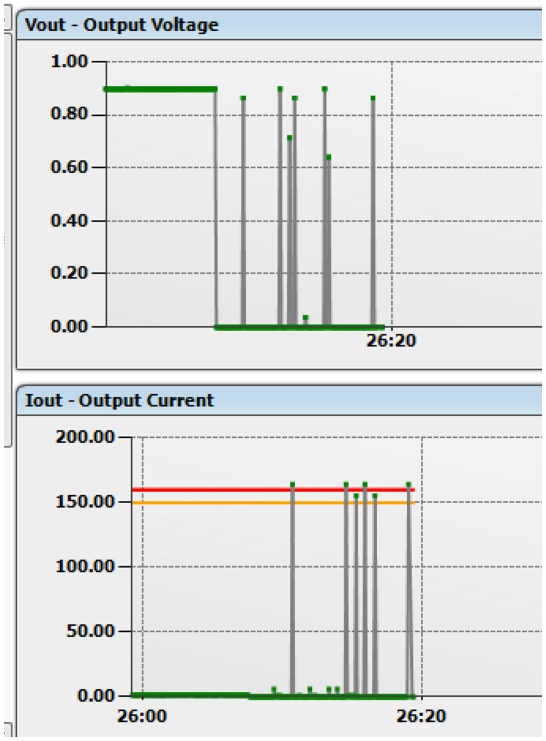

Figure 21. Overcurrent Event as Seen in Fusion GUI

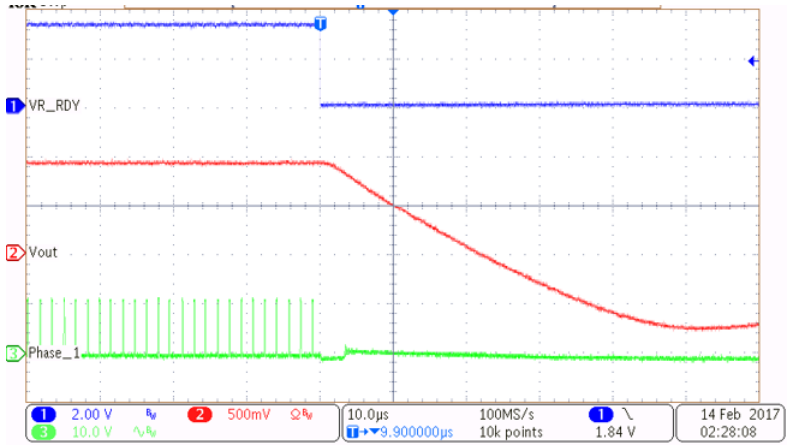

Figure 22. Overtemperature Shutdown Event

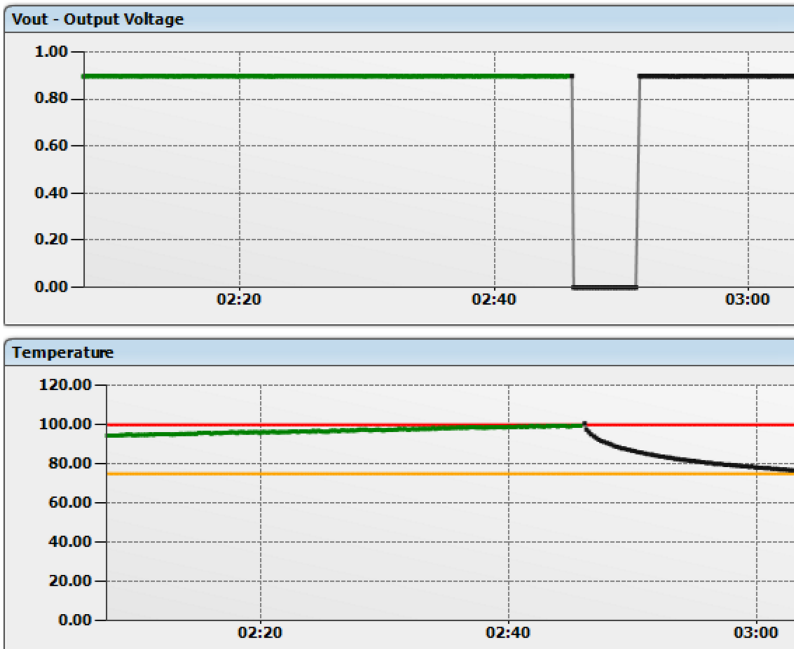

Figure 23. Overtemperature Event as Seen in Fusion GUI

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01419.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01419.

5.3 PCB Layout Recommendations

Follow all the layout instructions as specified in the respective datasheet for each part when laying out a design using the TPS53647 controller and CSD95472 Smart Power Stage. Some other guidelines to consider include:

- Keep the layout for all four phases identical to ensure optimal current balancing and thermal performance between phases.
- Route noisy traces such as PWM and the PMBus lines on a separate layer than the sensitive analog sense lines such as VSP, VSN, COMP, IMON, and so forth.
- Use quality capacitors for both the input and output decoupling to obtain the maximum performance possible with respect to DC ripple and transient response. Capacitors must be voltage rated to at least 16 V on V_{IN} and 2.5 V on V_{OUT} with a dielectric rating of X5R or better.
- Ensure that the VOUT and GND nodes are routed on multiple layers of copper and connected with enough vias to handle the current requirements for the best thermal performance. Following this guideline allows for a maximum amount of heat to flow out of the power stages and inductors into the board.

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01419.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01419.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01419.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01419.

6 Software Files

To download the Fusion Digital Power Designer software, see the following tool folder.

7 Related Documentation

1. Texas Instruments, *TPS53647 4-Phase, D-CAP+, Step-Down, Buck Controller with NVM and PMBus™ Interface for ASIC Power and High-Current Point-of-Load*, TPS53647 Datasheet (SLUSC39)
2. Texas Instruments, *CSD95472Q5MC Synchronous Buck NexFET™ Smart Power Stage* , CSD95472Q5MC Datasheet (SLPS599)
3. Intel, *Intel® Arria® 10 GX, GT, and SX Device Family Pin Connection Guidelines*, PCG-01017 (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/dp/arria-10/pcg-01017.pdf)
4. Intel, *Power Reduction Features in Arria 10 Devices*, AN-711 (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an711.pdf)
5. Intel, *SmartVID Controller IP Core User Guide*, UG-SVID (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug_smartvid.pdf)
6. Intel, *25A Mini Slammer*, Product Page (https://designintools.intel.com/25A_Mini_Slammer_p/q6uj9a00ms25.htm)

7.1 Trademarks

8 About the Author

CARMEN PARISI is a Senior Applications Engineer working in the Multiphase and Control Solutions (MCS) group at TI developing reference designs and application notes. He has six years of experience in power electronics working on mobile, desktop, and server V_{CORE} applications; battery chargers; and system PMICs. Carmen earned a combined BS/MS degree in electrical engineering from the Rochester Institute of Technology.

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