Design Guide: TIDA-010950

Damper and EEV Controller Reference Design with Power Regulation and Hall-Effect Position Sensing

Description

This reference design demonstrates a dual motor drive design for damper actuators and electronic expansion valves . The multiple motor drives include one bipolar stepper motor driver, one brushless DC motor driver, operating from a 15VDC source. The design shows accurate power limiting that helps for easy qualification as a low-power circuit, defined by IEC 60335-1. This reference design incorporates a 0-10V and 4-20mA control interface for controlling the position of the valve or damper, and a TMAG5273 which is used for accurate position sensing.

Resources

LMR38020	Product Folder
TPS62932	Product Folder
DRV8316C	Product Folder
DRV8428	Product Folder
TCAN334	Product Folder
ISO1212	Product Folder
MSPM0G3507	Product Folder
TLV9002	Product Folder
TMAG5273	Product Folder
TVS1401	Product Folder

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Features

- Operates at voltage ranging from 24V to 40V
- Brushless DC drive - 1.2 ARMS with two half bridges in parallel mode
- Bipolar stepper drive DRV8847 efficiency > 95 %
- Single MCU control with multi-device operation via I2C, SPI
- Power regulation with high accuracy to help easy low-power circuit qualification with IEC 60335-1
- 0-10V and 4-20mA control front-end

Applications

- HVAC Valve and Actuator Control
- HVAC Motor Control
- Air Conditioner Indoor Unit
- Air Conditioner Outdoor Unit
- HVAC Controller
- Heat Pump

Design Images

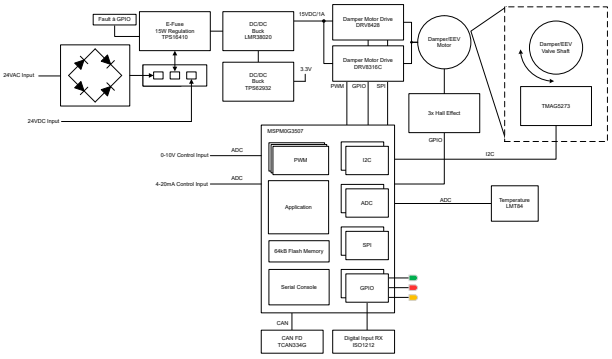

Figure 1-1. TIDA-010950 Block Diagram

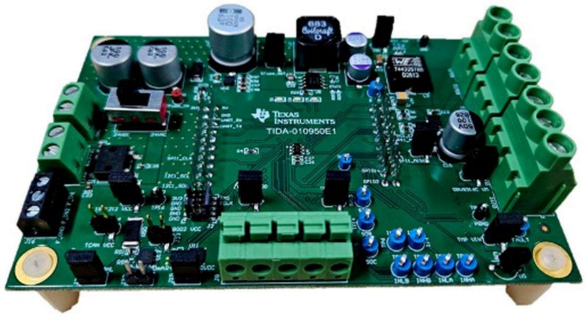

Figure 1-2. TIDA-010950 PCB

1 System Description

Many home appliances like HVAC zone dampers, electronic expansion devices, and water valves use multiple stepper motors, brushed DC motors, and many solenoid valves and actuators for operation. This reference design demonstrates a dual-motor drive design using a BLDC motor control IC and a stepper motor control IC. Both devices support a wide operating voltage range, and have features such as smart tune ripple and dynamic decay control and protection features including supply undervoltage lockout, overvoltage protection, charge pump undervoltage, overcurrent protection, over temperature warning and over-temperature shutdown

This design also considers industry recognized communication methods/protocols used to communicate with the motor control devices for dampers and electronic valves. A TCAN334 can transceiver is included in the design, paired with the dedicated CAN features of the MSPM0G3507 and the M0 SDK for quicker implementation. Both 0-10V control and 4-20mA control interfaces are also integrated for real-time control of the damper or expansion valve position from a host controller. The reliability and robustness of the system is further increased by surge protection provided by the TVS1401 at the control interface. In the case where only fully open or fully closed control is needed, this reference design incorporates an ISO1212 for field side fully open/fully closed control of the damper/valve.

Many household appliances have to be designed to meet specific UL (Underwriters Laboratories) or IEC (International Electrotechnical Commission) safety standards. For example, IEC 60335-1 and IEC 60730 are typically followed for household appliances. The standards define low-power circuit (LPC) in home appliances subsystems. A low-power point can be identified as the node where the maximum power delivered is less than 15W. The part of the circuit farther from the supply source than a low-power point is considered as a low-power circuit. A proven LPC can help to skip the glow wire test, needle flame test, and certain abnormal fault conditions as per the definition and requirements from the respective standards, leading to reduced qualification and design time, and money.

The use of an eFuse at the input of those sub-systems helps to achieve a precise power limit even during abnormal fault conditions. The design with the TPS16410 e-Fuse at the 24V-42V input can help the designer to qualify the circuit as a low-power circuit. The reference design shows <3% error in input power limit during testing which helps with qualification as a low-power circuit, defined by IEC 60335-1.

2 System Overview

2.1 Block Diagram

Table 2-1. TIDA-010950 Specifications

Parameter	Specification	
Input Voltage	24VDC	24VAC ± 20%
Overvoltage cutoff threshold	28VDC	41VDC
Input Power limit	13.65W	Up to 64W
Protection	OVP, UVP, OCP, Field Control Interface ESD	
15V buck efficiency	96% at 450mA	93% at 350mA - 900mA
3.3V buck efficiency	93% at 800mA – 850mA	
Communication interfaces	0-10V, 4-20mA, CAN, Isolated Field Interface, SPI, I2C	
PCB specifications	4 layer, 1-oz copper, 62mil	
Subsystem	**Bipolar Stepper**	**BLDC Motor**
Input Voltage	15V-24V	15V-24V
Total Phase Current	688.3mA Average	189.02 Average
Control Method	GPIO (STEP/DIR)	6x PWM

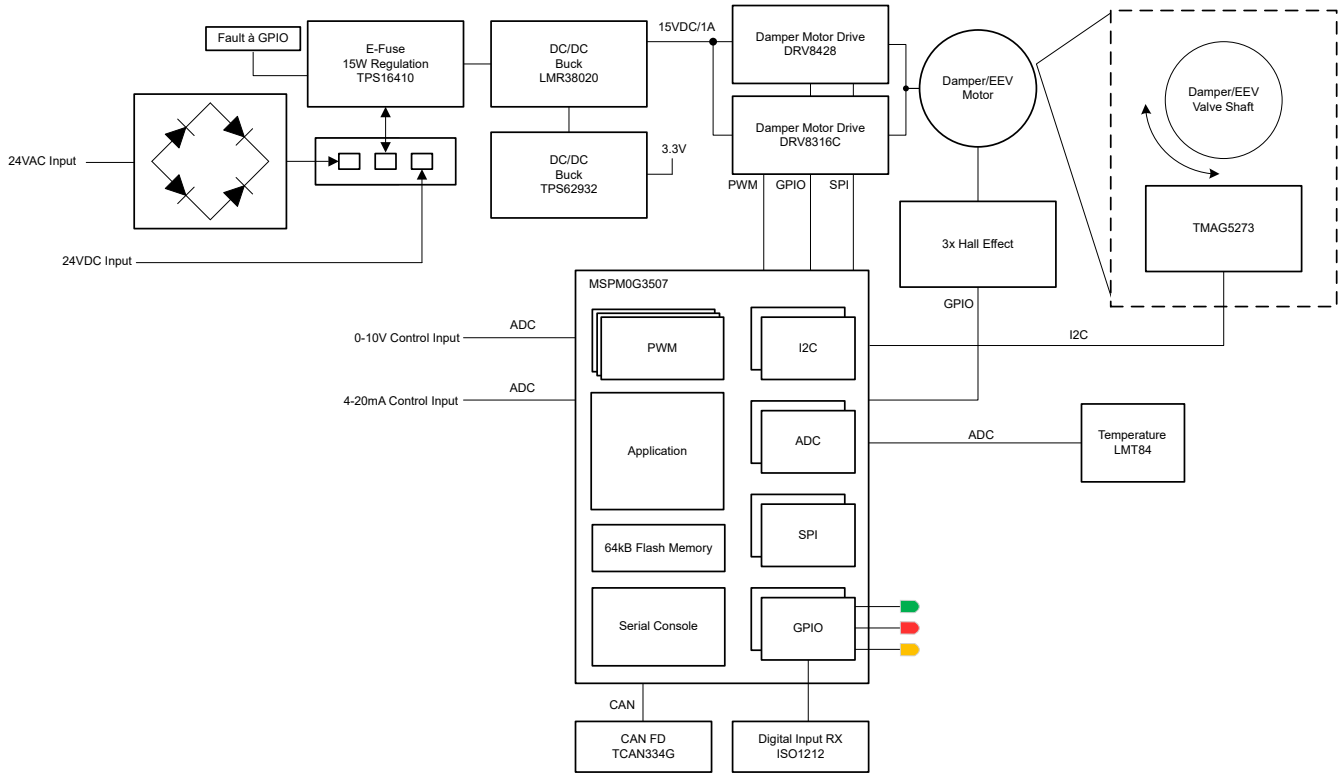

Figure 2-1. System Block Diagram

2.2 Design Considerations

The TIDA-010950 provides a single board design for BLDC motor control and electronic expansion valves control. This reference design allows the user to choose between BLDC motor control and stepper motor control.

This section outlines the theory and design considerations used to develop and design the TIDA-010950.

Selectable 24 VAC or 24 VDC Input

This reference designs allows for the user to select between either a 24VAC or a 24VDC input. Figure 2-2 shows the 24VAC and 24VDC inputs along with the switch to select between the two inputs. J18 is the 24VAC input connector. J19 is the 24VDC input connector, and S1 is the switch to select which input is being used.

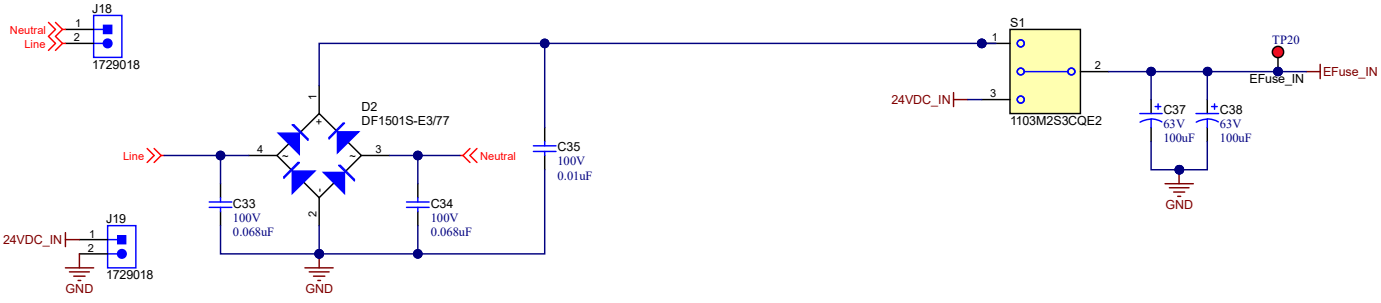

Figure 2-2. TIDA-010950 Input Power Source Select

24VAC Rectification

In this design when 24VAC input option is selected a full-bridge rectifier is used for DC rectification of the 24VAC input. The 120VAC to 24VAC voltage transformer has a leakage inductance and a parasitic capacitance. When the four diodes of the bridge rectifier are not conducting, the devices form a resonant circuit that oscillates at a

high frequency. One of the methods of reducing this oscillation is to use capacitors connected in parallel with the diodes, which helps to reduce the oscillation significantly.

Figure 2-3 below shows the simulation circuit and the resulting waveforms for the rectification stage leveraging a 100Ω resistor for the load.

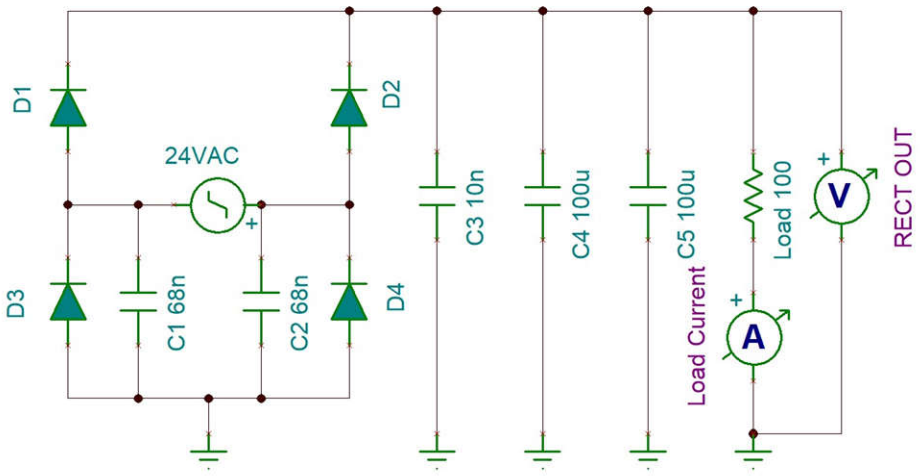

Figure 2-3. 24VAC Rectification TINA-TI Simulation Circuit

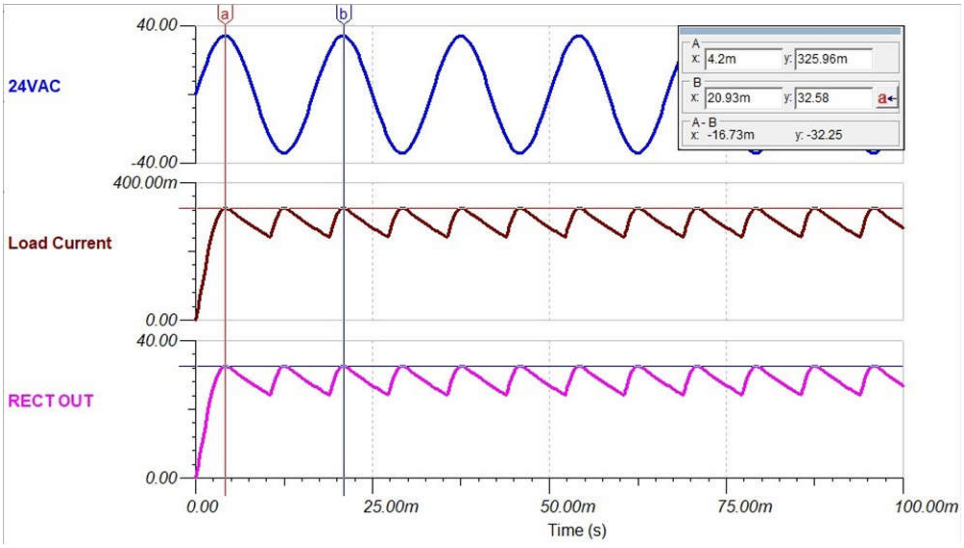

Figure 2-4. 24VAC Rectification TINA-TI Simulation Waveforms

eFuse Protection

The TIDA-010950 reference design leverages a TPS16410 eFuse to protect the ICs in the event of an overvoltage or overcurrent event. Figure 2-5 shows the implementation of the TPS16410 in this reference design. Depending on the input voltage applied, the TPS16410 can regulate the input power from 2W all the way up to 64W, based on the individual requirements of the implementation. For this design, the testing is done leveraging the 24VDC input, but the user can change the power regulation and protection thresholds as needed based on the following calculations.

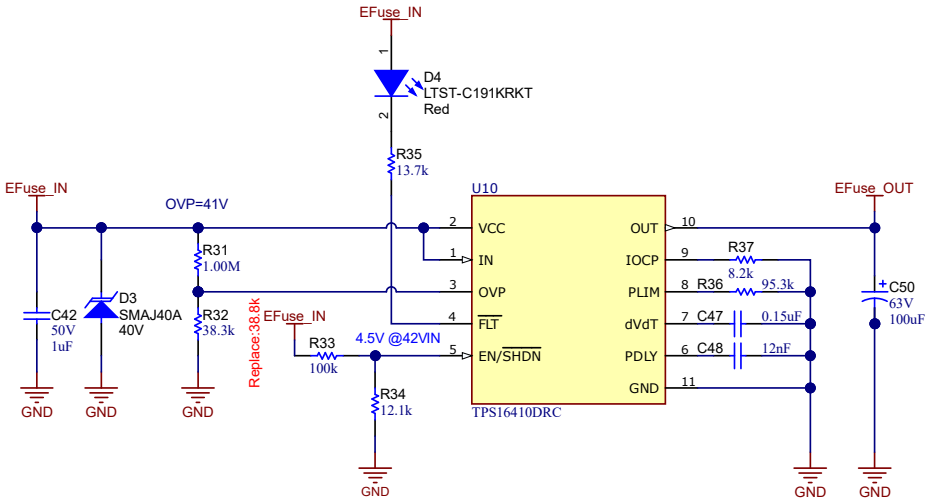

Figure 2-5. TPS16410 E-Fuse Circuit Implementation

To program the output power limit threshold of the TPS16410, use Equation 1 to calculate the required resistance of RPLIM (R36). To keep output power limit ≤ 15W, R36 was selected as 95.3kΩ.

$$P_{LIM} = \frac{13.82W}{95.3\ k\Omega} \times R_{PLIM} \quad (1)$$

Input overvoltage protection setpoints can be set by connecting resistors (R31, R32) from the IN pin to OVP pin. The value of R31 and R32 can be calculated using Equation 2 and Equation 3, where and from the device electrical specifications. To set the OVP rising setpoint to 41V, R31 = 1MΩ and R32 = 38.3kΩ were selected. For a OVP setpoint of 28V in the case where the input voltage is 24VDC, R32 can be changed to 59kΩ.

$$OVP\ Rising\ Setpoint = \frac{V_{OVPR} \times (R31 + R32)}{R32} \quad (2)$$

$$OVP\ Falling\ Setpoint = \frac{V_{OVPF} \times (R31 + R32)}{R32} \quad (3)$$

To set the output overcurrent setpoint, a resistor (R37) is required on the IOCP pin. To calculate the value of R37, use Equation 4. R37 was selected as to set IOCP to 1.5A, yielding a resistance to the nearest 1% value of 11kΩ.

$$I_{OCP} = \frac{2.25A}{R_{IOCP}} \times 7.32k\Omega \quad (4)$$

The TPS16410 also provides blanking time for overload or overcurrent events. This blanking time can be configured by connecting a capacitor on PDLY, and can be calculated using Equation 5. To set the blanking time to 6.5ms, C48 was selected to be 12nF.

$$Blanking\ Time\ (PDLY) = \frac{6.5\ ms}{12\ nF} \times C48 \quad (5)$$

For charging the large capacitors on output, the output slew rate can be controlled by using a capacitor on dV/dt pin. The value of inrush current can be estimated by Equation 6. To keep the inrush current below 75mA, C47 is selected as 150nF.

$$I_{INRUSH} = \frac{I_{dVdt} \times G_{dVdt} \times C_{OUT}}{C47} \quad (6)$$

TVS diode (D3) was added to protect the TPS16410 against voltage transients.

LMR38020 Voltage Rail

The LMR38020 is used to convert the 24V source to 15VDC for powering the motor drives and as an input to the 3.3V buck.

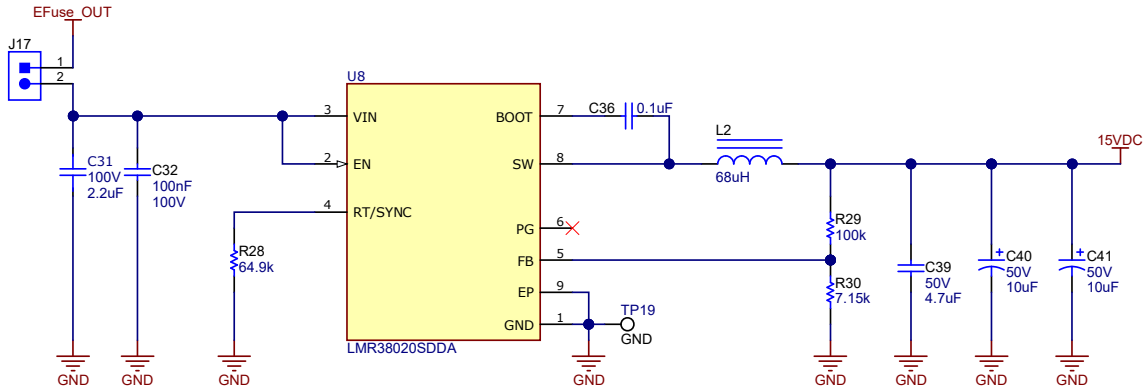

Figure 2-6. LMR38020 Circuit Implementation

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this design a switching frequency of 400kHz is used.

The output voltage of LMR38020 is externally adjustable using a resistor divider network. The range of recommended output voltage is found in the Recommended Operating Conditions of the data sheet. The divider network is comprised of R29 and R30, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, VREF. The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R29 is 100kΩ, this design follows the recommended value. After R29 is selected, Equation 7 is used to select the value of . VREF is nominally 1V.

$$R30 = \frac{R29}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \tag{7}$$

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the maximum device current. Equation 8 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this design, choose K = 0.175 and find an inductance of L = 60µH. Select the next standard value of L = 68µH for L2.

$$L2 = \frac{(V_{IN} - V_{OUT})}{f_{sw} \times K \times I_{OUTMAX}} \times \frac{V_{OUT}}{V_{IN}} \tag{8}$$

Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. The inductor saturation current must not be less than the device low-side current limit. To avoid sub-harmonic oscillation, the inductance value must not be less than that given in Equation 9:

$$L_{MIN} \geq M \times \frac{V_{OUT}}{f_{SW}} = 0.42 \times \frac{15V}{400\ kHz} = 15.75\ \mu H \tag{9}$$

Where

- L_{MIN} = minimum inductance (H)

- M = 0.42
- f_{SW} = switching frequency (Hz)

TPS62932 Voltage Rail

The TPS62932 is a highly integrated, synchronous, step-down, DC-DC converter. This device is used to convert the 15VDC output from the LMR38020 to a 3.3VDC rail to provide power to the MSPM0 and peripherals in this reference design.

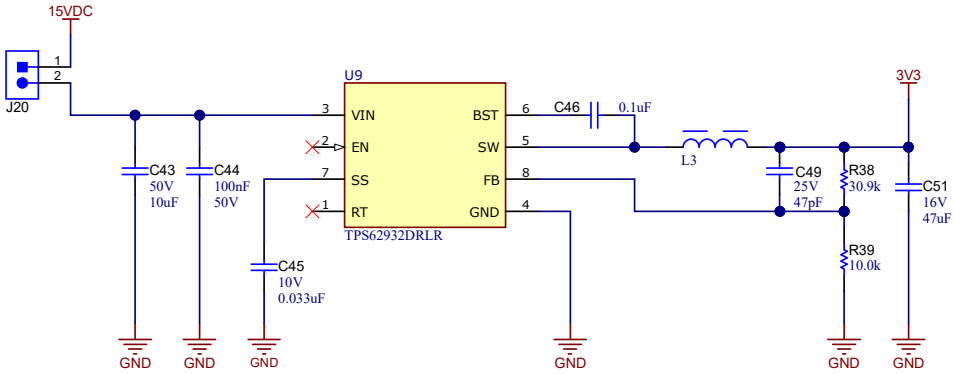

Figure 2-7. TPS62932 Circuit Implementation

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Referring to Figure 2-7, start with 10kΩ for R9 and use Equation 10 to calculate R38 = 30.9kΩ. To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the converter is more susceptible to noise and voltage errors from the FB input leakage current are noticeable.

$$R38 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R39 \tag{10}$$

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Higher switching frequency allows the use of smaller inductors and output capacitors, and hence, a more compact design. However, lower switching frequency implies reduced switching losses and usually results in higher system efficiency, so the 500kHz switching frequency was chosen for this reference design by leaving the RT pin floating.

The large CSS can reduce inrush current when driving large capacitive load. In this design 33nF is chosen for C45, which sets the soft-start time, tSS, to approximately 5ms.

A 0.1µF ceramic capacitor must be connected between the BST to SW pins for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor C46 must have a 16V or higher voltage rating.

The EN pin for the TPS62932 has an internal pullup current source, which allows the user to float the EN pin to enable the device. In this reference design the EN pin is left floating to enable to device.

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current, which can be calculated by Equation 11.

$$\Delta i_L = \frac{(V_{IN\_MAX} - V_{OUT})}{f_{sw} \times L} \times \frac{V_{OUT}}{V_{IN\_MAX}} \tag{11}$$

Usually, the K coefficient represents the amount of inductor ripple current relative to the maximum output current of the device, a reasonable value of K is 20% to 60%. For this reference design a value of 40% was chosen for K. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L. Use Equation 12 to calculate the minimum value of the output inductor to be 6.44. Given this minimum inductance value, L3 = 7.8 was selected for this design.

$$L3 = \frac{(V_{IN} - V_{OUT})}{f_{sw} \times K \times I_{OUTMAX}} \times \frac{V_{OUT}}{V_{IN}} \quad (12)$$

DRV8316C BLDC Motor Driver

For the TIDA-010950 the SPI variant was selected. The SPI variant supports a serial communication bus that allows the MSPM0 to send and receive data with DRV8316C. This allows the MSPM0 to configure device settings and read detailed fault information. The SPI is a four-wire interface using the SCLK, SDI, SDO, and nSCS pins.

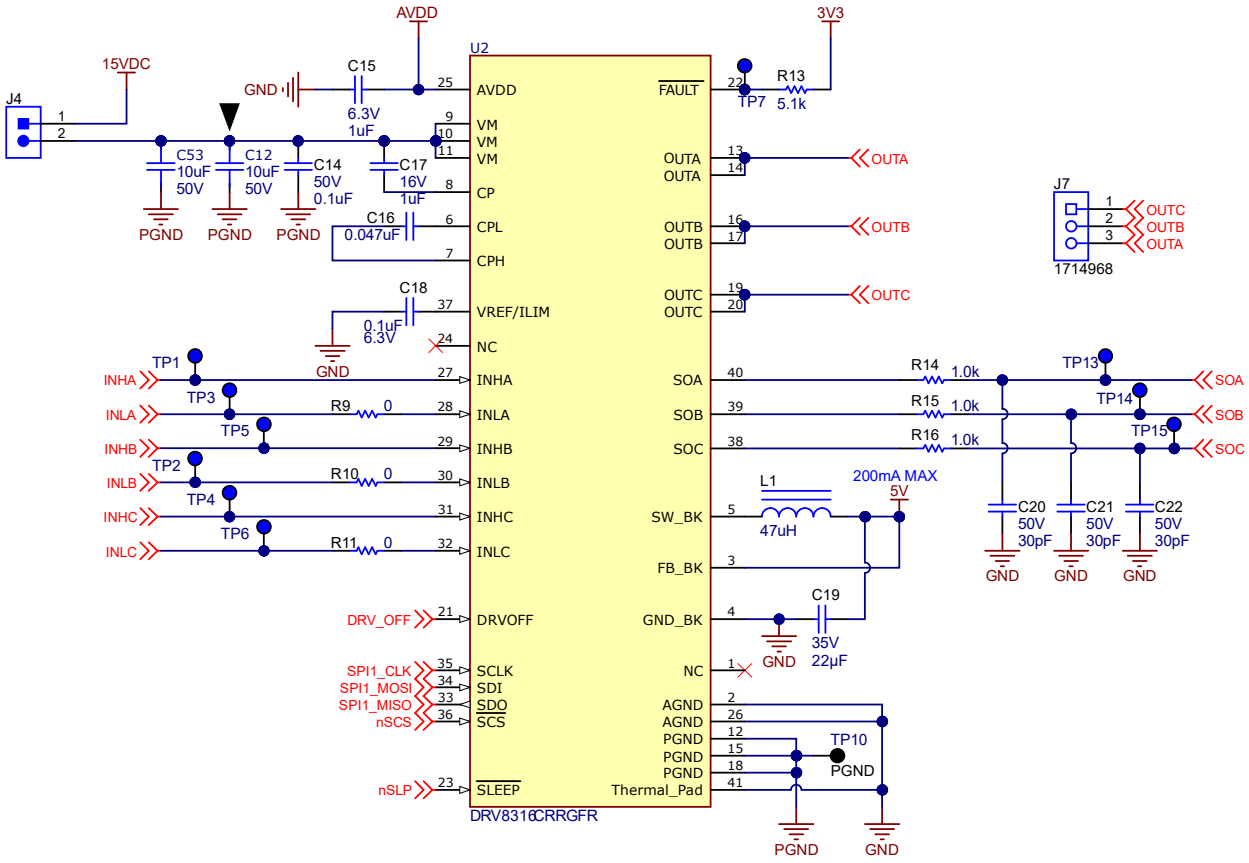

Figure 2-8. DRV8316C Circuit Implementation

The DRV8316C integrates three, high-performance low-side current sense amplifiers for current measurements using built-in current sensing. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless-DC commutation with an external controller. The three amplifiers can be used to sense the current in each of the half-bridge legs (when the low-side FET of the corresponding phase is conducting current). In the TIDA-010950 these current sense measurements are being read by the integrated ADC on the MSPM0.

The buck regulator in DRV8316C device is primarily designed to support low inductance of 47µH and 22µH inductors. In this reference design a 47µH inductor was selected for L1 which allows the buck regulator to operate up to 200mA load current support at 5V out. This reference design does not utilize this power source, but this can be leveraged to provide power to an MCU or other low voltage peripherals as needed.

DRV8428 Stepper Motor Driver

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring

the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM. Stepper motor drivers need to re-circulate the winding current by implementing several types of decay modes. The DRV8428 comes with smart tune decay modes. The smart tune is a decay mechanism that automatically adjusts for superb current regulation performance agnostic of voltage, motor speed, variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple current control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic fast decay percentage scheme to minimize distortion of the motor winding current while minimizing frequency content and significantly reducing design efforts. Along with this seamless, effortless automatic smart tune, DRV8428 also provides the traditional mixed decay mode.

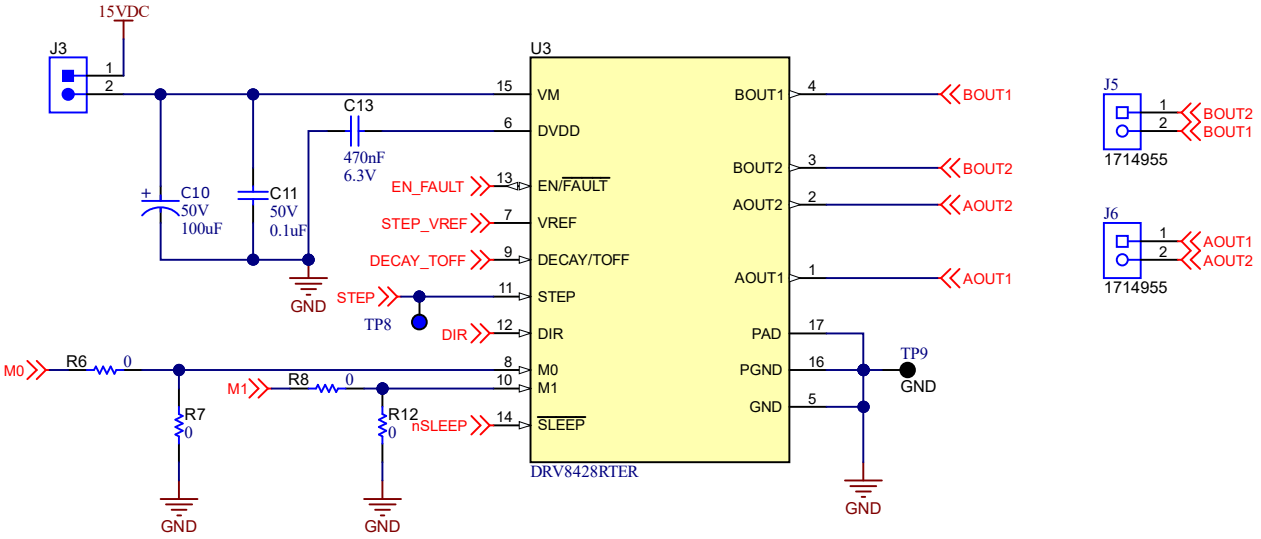

Figure 2-9. DRV8428 Circuit Implementation

This reference design uses the Decay set to 0 and HI-Z, enabling the smart tune ripple control or Smart Tune Dynamic Decay. This can also be set based on preference using the configurations shown below in Decay Mode Settings.

Table 2-2. Decay Mode Settings

DECAY/TOFF	DECAY MODE	OFF TIME
0	Smart tune Ripple Control	-
14.7kΩ to GND	Mixed 30% Decay	7µs
44.2kΩ to GND		16µs
100kΩ to GND		32µs
249kΩ to GND	Smart tune Dynamic Decay	7µs
Hi-Z		16µs
DVDD		32µs

The microstepping level is set by the M0 and M1 pins and can be any of the settings listed in Microstepping Settings. Higher microstepping results in a smoother motor motion and less audible noise, but requires a higher f_{step} to achieve the same motor speed. Through this reference design, the designer has the option of populating or depopulating R6, R7, R8, and R12 to set the desired step mode in Microstepping Settings. For the testing of this design M0 is set at 0 and M1 is connected through a 330kΩ resistor to ground.

Table 2-3. Microstepping Settings

M0	M1	STEP MODE
0	0	Full step (2-phase excitation) with 100% current
0	330kΩ to GND	Full step (2-phase excitation) with 71% current
1	0	Non-circular 1/2 step
Hi-Z	0	1/2 step
0	1	1/4 step
1	1	1/8 step
Hi-Z	1	1/16 step
0	Hi-Z	1/32 step
Hi-Z	330kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step
1	Hi-Z	1/256 step

DRV8428 External Components below shows the recommended discrete component values for the DRV8428 circuit, along with the connections for each pin.

Table 2-4. DRV8428 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	One X7R, 0.01µF, VM-rated ceramic capacitor
C_{VM2}	VM	PGND	Bulk, VM-rated capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47µF to 1µF, 6.3V ceramic capacitor
R_{REF1}	VREF	VCC	Resistor to limit chopping current. The value of parallel combination of R_{REF1} and R_{REF2} must be less than 50kΩ.
R_{REF2} (Optional)	VREF	GND	

Position Sensing

The TIDA-010950 leverages the TMAG5273 for position sensing of the damper/EEV. The TMAG5273 has an integrated angle calculation engine (CORDIC) that provides full 360° angular position information for both on-axis and off-axis angle measurement topologies. The angle calculation is performed using two user-selected magnetic axes. The device features magnetic gain and offset correction to mitigate the impact of system mechanical error sources.

This references design utilizes the angular output for the control loop feedback. More details are given in the software section of this guide.

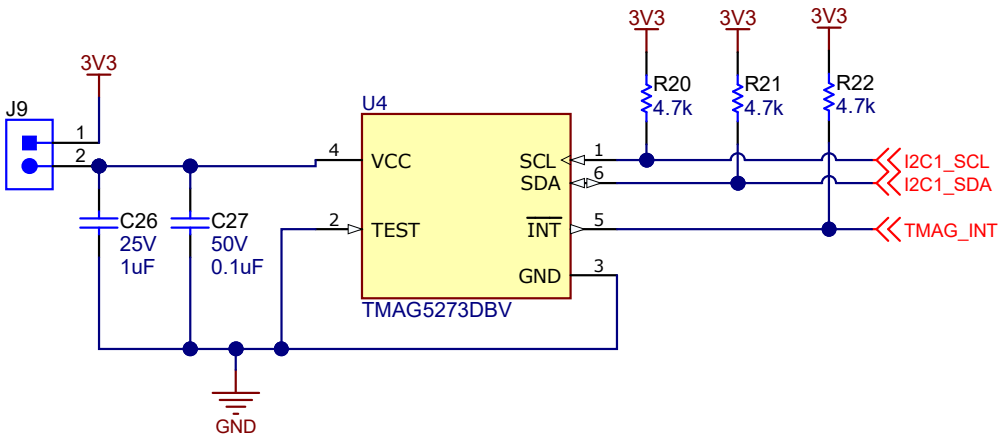

Figure 2-10. TMAG5273 Circuit Implementation

ISO1212

The ISO1212 is an isolated 24V to 60V digital input receiver, compliant to IEC 61131-2 Type 1, 2, and 3 characteristics. This device enables 9V to 300VDC and AC digital input modules in programmable logic controllers (PLCs), motor-control, and other industrial applications. Unlike traditional optocoupler designs with discrete, imprecise current limiting circuitry, the ISO121x devices provide a simple, low-power design with an accurate current limit to enable the design of compact and high-density I/O modules. These devices also do not require field-side power supply and are configurable as sourcing or sinking inputs.

For this reference design, the ISO1212 is used as an interface for a 24VDC open/closed controller signal. When the input on the SENSE 1 pin is high, the damper motor is engaged until the 90º (fully closed) damper position is reached. When SENSE 2 is high, the damper motor is also engaged according to the TMAG5273, moving the damper to the 0º position (fully open).

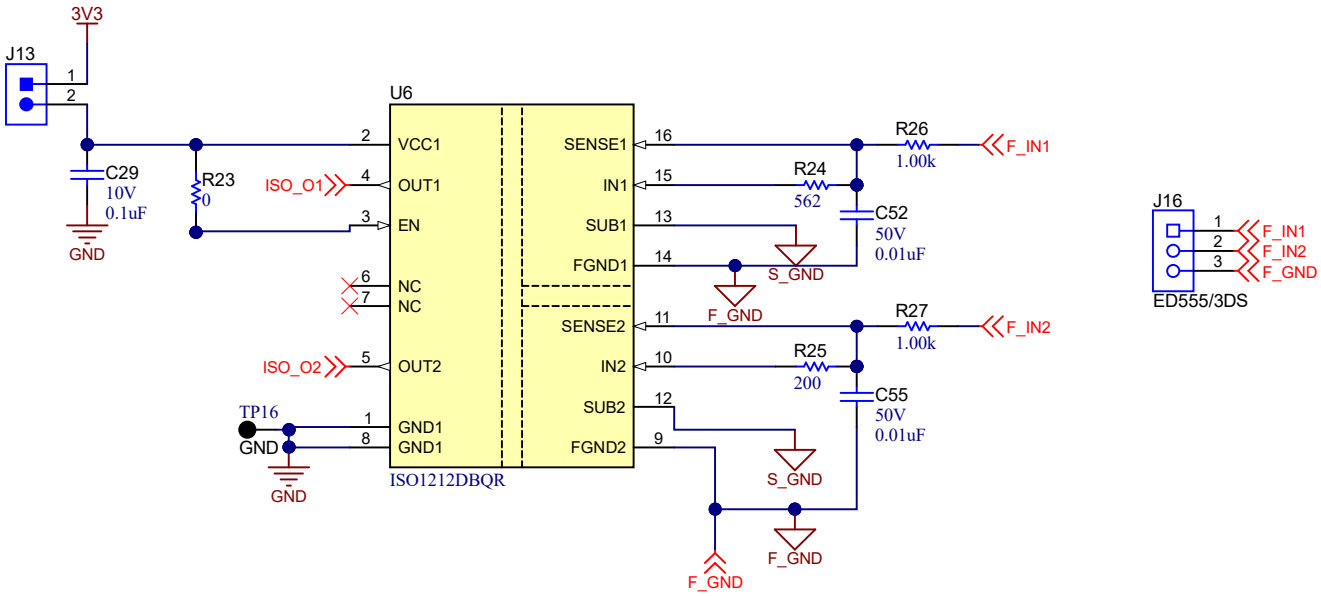

Figure 2-11. ISO1212 Circuit Implementation

The R_{SENSE} resistor (R24, R25) limits the current drawn from the field input. In each case, a (slightly) lower value of R_{SENSE} can be selected based on the need for a higher current limit or component availability. A 1% tolerance is recommended on R_{SENSE} but 5% resistors can also be used if higher variation in the current limit value is acceptable. The relationship between the R_{SENSE} resistor and the typical current limit (I_L) is given by Equation 13:

$$I_L = \frac{2.25mA \times 562\Omega}{R_{SENSE}} \quad (13)$$

The maximum voltage on the SENSE pins of the ISO121x device is 60V. However, because the R_{THR} resistor drops additional voltage, the maximum voltage supported at the module inputs is higher and given by Equation 14

$$V_{In}(\max) = 60V + R_{THR} \times \frac{2.1mA \times 562\Omega}{R_{Sense}} \quad (14)$$

The R_{THR} resistor sets the voltage thresholds (V_{IL} and V_{IH}) as well as limits the surge current. A value of 1kΩ is recommended for R_{THR} in Type 3 systems (maximum threshold voltage required is 11V). A value of 2.5kΩ is recommended for R_{THR} in Type 1 systems (maximum threshold voltage required is 15V) and a value of 330Ω is recommended for R_{THR} in Type 2 systems. More information on calculating the discrete component values can be found in the ISO1212 data sheet.

TCAN334

Termination is typically a 120Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination can be used. Split termination uses two 60Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Care must be taken in the power ratings of the termination resistors used. Typically, the worst-case condition is if the system power supply was shorted across the termination resistance to ground. In most cases the current flow through the resistor in this condition is much higher than the transceiver's current limit.

The designer has the option of utilizing the onboard TCAN interface if desired, and there is an additional external crystal oscillator provided on the board which is required by this interface, shown below. The MSPM0 SDK can be leveraged for implementation examples for CAN.

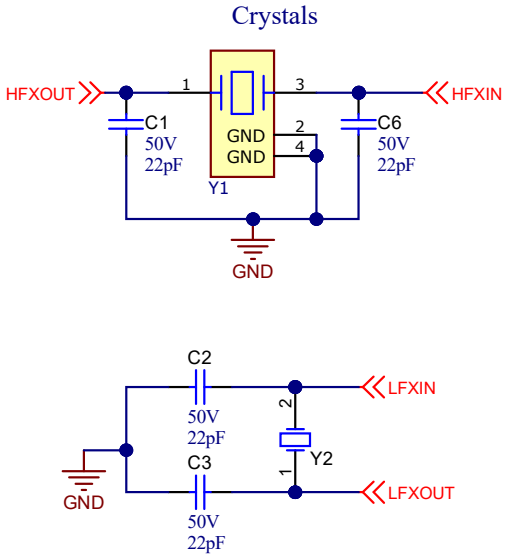

Figure 2-12. External Crystal Oscillators for TCAN Communication

4-20mA and 0-10V Circuitry

For this reference design, the damper and EEV position is adjusted based on the input signal received from either the 0-10V control interface or the 4-20mA control interface. The input front-end converts the industries typical signal input range to the ADCs input voltage range as well as setting the input impedance and providing required overvoltage and overcurrent protection. For both the 0-10V as well as the 4-20mA control interfaces, a single TLV9002 op-amp is used as a buffer before the control signal is sent to the M0 ADC. The TLV9002

The TLV9002 is a low-voltage (1.8V to 5.5V) operational amplifier with rail-to-rail input and output swing capabilities. This op amps provide a cost-effective design for space-constrained applications or applications where low-voltage operation and high capacitive load drive are required.

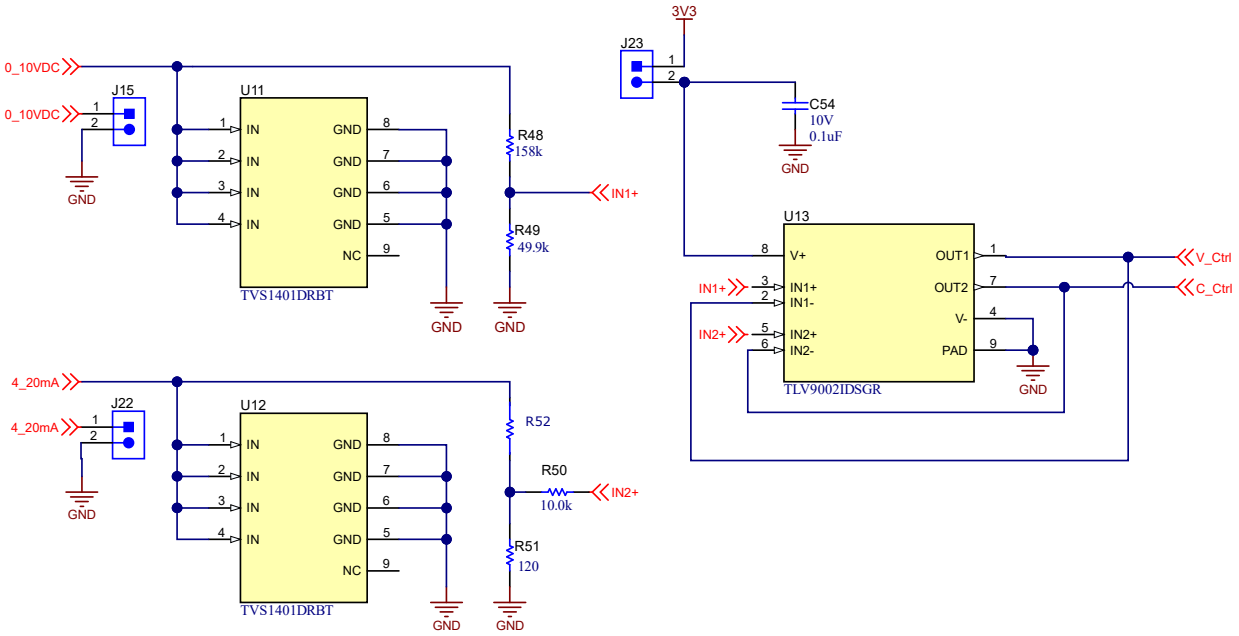

Figure 2-13. 0-10V and 4-20mA Control Interface Circuit Implementation

For the 0-10V input, a simple voltage divider is used to scale the voltage range to match that of the MSP M0 ADC. Leveraging the known input range and the V_{REF} of the M0 ADC (2.5V), along with Equation 15 below, the resistance values of R48 and R49 are calculated to be:

$$2.5 = 10 \times \frac{R_{49}}{R_{48} + R_{49}} \quad (15)$$

Choosing 49.9k for R49 yields a nearest 1% resistor value of 149.7k, but the gain factor of the input stages is chosen so that the 10V or 20mA input signals result in an input voltage to the ADC a bit lower than the full-scale of 2.5V to avoid saturation in consideration of offset, gain, and other errors, so a 158k resistance value is chosen for R48 . For the voltage input stage, a gain of 0.24V/V is used, that is, 2.4V corresponds to the 10V input. For the current input stage, a 20mA input current over the 120Ω shunt resistor results in 2.4V at the ADC input.

For the current input stage, a 20mA input current over the 120Ω shunt resistor results in 2.4V at the ADC input. The 4-20mA input front-end has an additional 24V PTC resistor (R52 = PRG18BB470MB1RB), which is used for protection. More information on the Input front-end can be found in *Reducing Cost for PLC Analog Input Modules Using the MSP430 MCU*.

Software

The software for TIDA-010950 relies on several of the MSPM0 peripherals including SPI, I2C, GPIO, and PWM. For both the damper BLDC motor control as well as the EEV stepper motor control use a very similar firmware loop, only differing in the motor control method respectively.

After initializing the communication channels, the ADC inputs are enabled which is primarily responsible for sensing the control voltage/current, as well as sensing the temperature from the LMT84 temperature sensor. The ADC V_{REF} is set to be internally referenced at 2.5V.

Next, in the case of the DRV8316, the SPI communication is established with the device, after which the motor control IC is enabled for operation. The direction of rotation as well as the end position is based on the current position of the damper (sensed by the TMAG5273) in relation to the control signal coming from the 0-10V or 4-20mA input front-end. Once the firmware computes the necessary changes, if any, the direction and PWM values are set, engaging the motor.

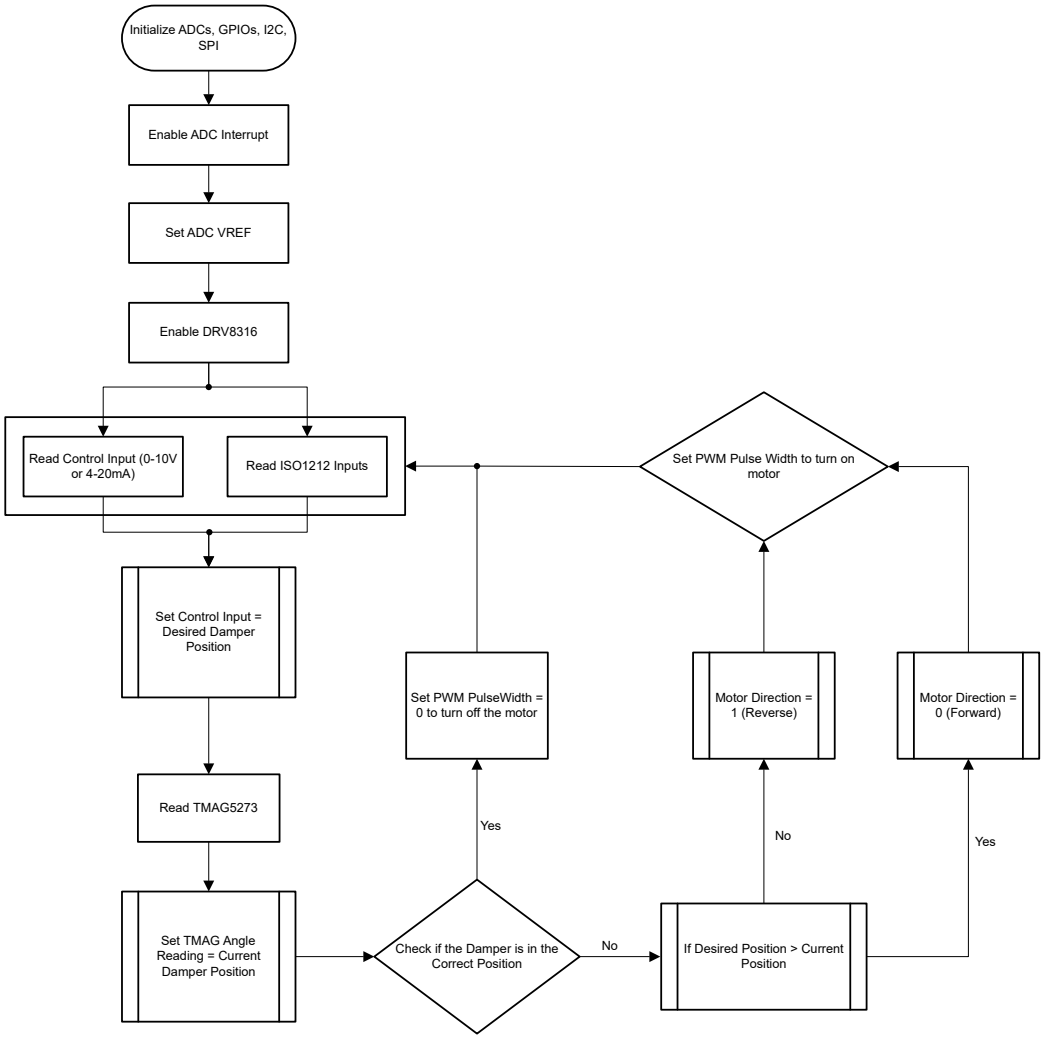

Figure 2-14. BLDC Motor Control Software Control Loop Diagram

Code Implementation Example:

```
while (1) {
    /* check 2 digital isolator pins for high */
    /* Read iso1 and iso2 states */
    iso1Status = HAL_readGPIOPin(iso1);
    iso2Status = HAL_readGPIOPin(iso2);

    if (iso1Status) {
        desiredDamperPosition = 90;
    }

    else if (iso2Status) {
        desiredDamperPosition = 0;
    }

    else {
        /* Read mV value of current control and control inputs */
        controlVoltage = (HAL_getmvFromADC(vControl) * 2500) / 2400; // scale to 0 - 2.4V input
        desiredDamperPosition = controlVoltage * 0.036;              // 0-2500mV = 0-90 degrees
    }
```

```
    do {
        /* Read in TMAG angle result and set to current damper
            position */
        tmagAngleResult();
        currentDamperPosition = tmagAngle;

        correctPosition = currentDamperPosition * 0.9 <= desiredDamperPosition &&
                          currentDamperPosition * 1.1 >= desiredDamperPosition;

        /* Set duty cycle to 0% when current position reaches the desired
        position */
        if (correctPosition) {
            firmVar.pulsewidth = 0x00;
            break;
        }

        /* Set motor direction */
        else if (currentDamperPosition < desiredDamperPosition) {
            firmVar.motorDirection = MOTOR_DIR_FORWARD;
        }

        else {
            firmVar.motorDirection = MOTOR_DIR_REVERSE;
        }

        /* Set PWM duty cycle */
        firmVar.pulseWidth = 0x64;

        /* Read mV value of current control and control inputs */
        controlVoltage = (HAL_getmvFromADC(vControl) * 2500) / 2400; // scale to 0 - 2.4V input
        desiredDamperPosition = controlVoltage * 0.036; // 0-2500mV = 0-90 degrees

       } while (!correctPosition);
    }
```

For the EEV stepper motor control, the user has the option to employ an additional component in the control loop, the temperature output from the LMT84 as shown below in Figure 2-15. This is used as an example implementation of a thermal feedback loop which can be used to modulate the EEV to allow more or less refrigerant to flow through the valve. for peripheral setup, the ADC is initialized in an identical manner to that of the DRV8316C firmware. There is no need for SPI communication for this firmware, this can be removed if the user so chooses.

The motor control interface is very simplistic, only requiring EN and nSLEEP pins controlled by the MCU. These pins enable and wake the device up when driven high and disable or put the device to sleep if driven low. For both examples below, a simple toggle of the STEP GPIO in the control loop is used to rotate the stepper motor. The user can adjust the pulse time in the firmware by increasing or decreasing the delay definition assigned value.

Once the device is set up and the peripherals are running, the temperature data is taken by the on-board LMT84. The user can also implement an offboard temp sensor if preferred through the boosterpack headers on the board. Based on the temperature reading, simulating the temperature at the suction line from the evaporator, the valve either rotates forward in the case of the suction line temperature being greater than the target temp, or vice-versa for suction line temperatures less than the target temp. In this example, the TMAG5273 is used only for rotation and position verification and does not play a part in the overall control loop.

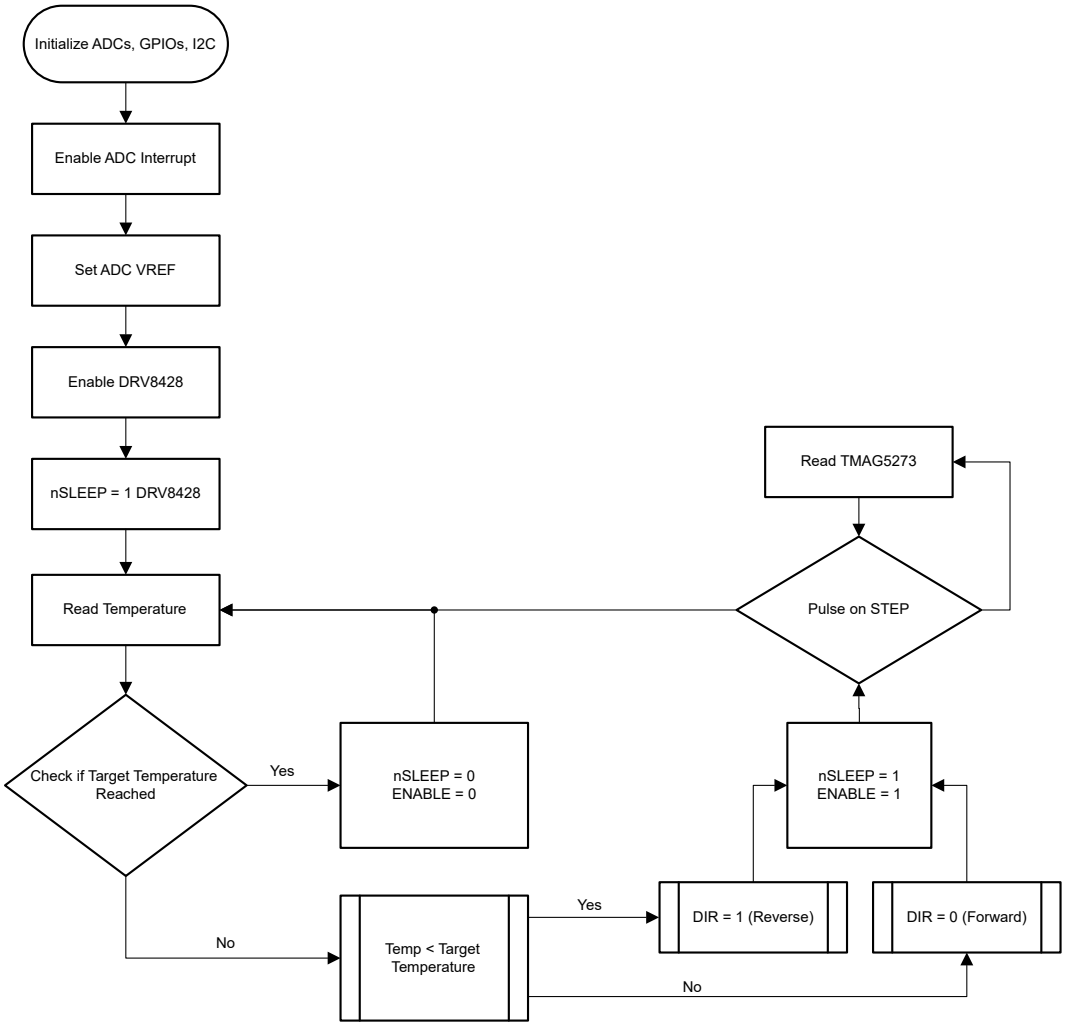

Figure 2-15. Stepper Motor Control Software Control Loop Diagram (Temperature Based)

```
#define ADC12_BIT_RESOLUTION (12)
#define ADC12_REF_VOLTAGE (2.5)
uint16_t gVolt = 0;

uint16_t getVolts() {

    uint16_t Voltage = 0;
    DL_ADC12_startConversion(VControl_ADC_INST);

    gAdcResult = DL_ADC12_getMemResult(VControl_ADC_INST, DL_ADC12_MEM_IDX_0);
    Voltage = (gAdcResult * ADC12_REF_VOLTAGE) / (1 << ADC12_BIT_RESOLUTION) * 3;
    DL_ADC12_enableConversions(VControl_ADC_INST);

    return (Voltage);
}
```

```
    while (1) {
        // Set the DRV8428 control pins to known values before entering loop
        gVolt = getVolts();
    If (gVolt != Target_TMP) { // now that we have a condition where desired and
                             // current position dont match, enable the device for
                             // the position change loop
        DL_GPIO_setPins (GPIO_LEDS_PORT,
                         (GPIO_LEDS_USER_LED_1_PIN); // Using this is a status pin
        DL_GPIO_setPins (GPIO_LEDS_PORT,
                          GPIO_LEDS_DRV8428_EN_PIN); // Logic high to enable outputs
        DL_GPIO_setPins (GPIO_LEDS_PORT,
                          GPIO_LEDS_DRV8428_SLP_PIN); // Logic high to enable device

    While (gVolt < Target_TMP) {
        DL_GPIO_setPins(
            GPIO_LEDS_PORT,
            GPIO_LEDS_DRV8428_DIR_PIN; // Set Direction pin for CW or CCW

        DL_GPIO_setPins(
            GPIO_LEDS_PORT,
            GPIO_LEDS_DRV8428_STEP_PIN; // Move motor ahead by one step

        DL_GPIO_SetPins(GPIO_LEDS_PORT,
                        GPIO_LEDS_USER_LED_1_PIN); // Using this as status pin

        delay_cycles(DELAY_MOTOR);

        DL_GPIO_clearPins(
            GPIO_LEDS_PORT,
            GPIO_LEDS_DRV8428_STEP_PIN); // Set Direction pin for CW or CCW

        DL_GPIO_ClearPins(GPIO_LEDS_PORT,
                          GPIO_LEDS_USER_LED_1_PIN); // Using this as status pin

        delay_cycles(DELAY_MOTOR);
    }
```

In the case where the modulation is not controlled by the temperature feedback loop as shown below in Figure 2-16, the 0-10V and 4-10mA control interfaces can be used to control the stepper direction and target end position. This example is almost identical to the previous example, but in this instance, the TMAG5273 is used in combination with the control front-end to provide current angular position relative to desired position and rotate the stepper motor accordingly.

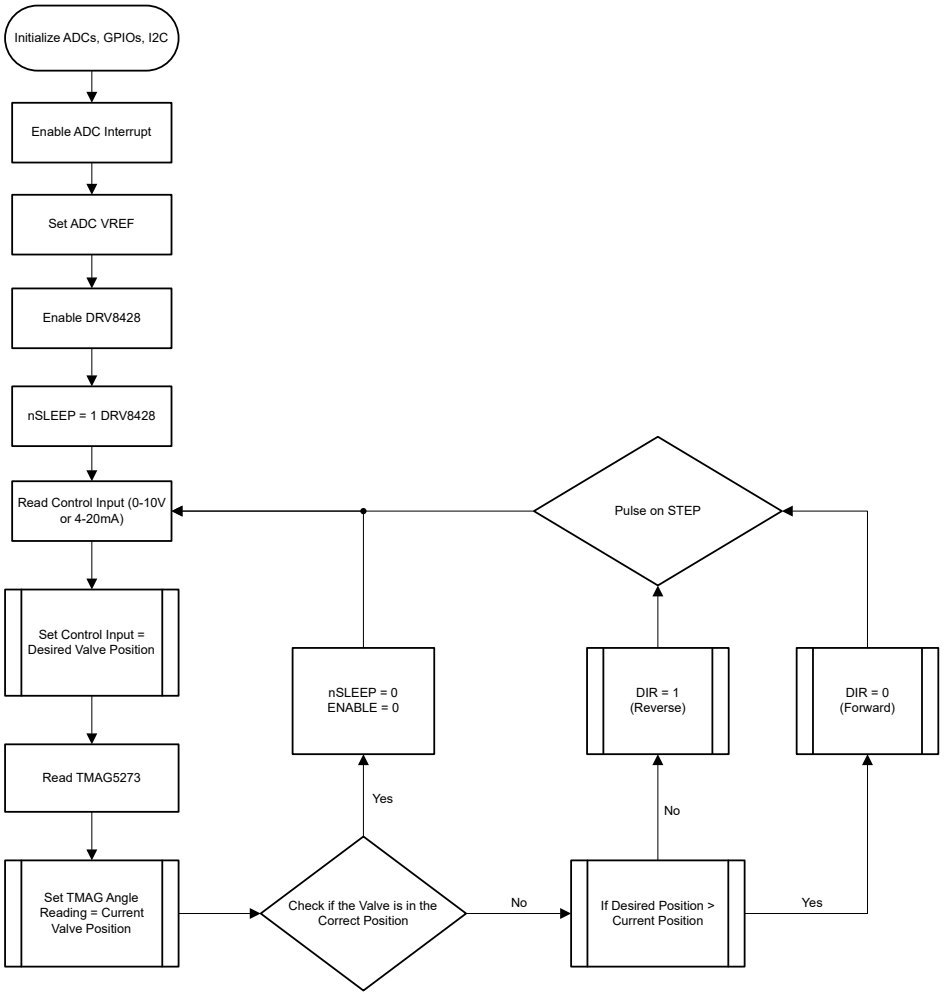

Figure 2-16. Stepper Motor Control Software Control Loop Diagram (Control Input Based)

In this specific example, a combination of the first 2 examples can be used to implement this in firmware, instead leveraging the GPIO control pins for the DRV8428 to control direction and rotation.

2.3 Highlighted Products

The TPS1641x is an integrated eFuse with accurate power limit or current limit. The device integrates an NFET with RON of 152mΩ. TPS16410, TPS16411, TPS16414 and TPS16415 provide power limiting whereas the TPS16412, TPS16413, TPS16416 and TPS16417 provide current limiting. The TPS16410, TPS16411, TPS16414 and TPS16415 can provide 15-W accurate power limiting for low power circuit (LPCs) as per IEC60335 and UL60730 standards. TPS16410, TPS16411, TPS16412 and TPS16413 also provide IN to OUT short detection and indication on FLT output. IN to OUT short detection eliminates the need of additional eFuse or power limiting circuit in case of IN to OUT short test for IEC60335, UL60730, and similar standards. FLT can be used as input for MCU or FLT can be used to drive an external PFET. TPS1641x devices also provide protection from adjacent pin short and pin short to GND faults. The TPS1641x device also provide configurable blanking time (IDLY or PDLY) and overcurrent protection (IOCP) for transient loads. Load such as motors need higher current for start-up. Blanking time is useful for providing higher current for start-up of loads such as motors. TPS1641x devices have overvoltage protection (OVP), overtemperature protection, and adjustable output slew rate control (dvdt). Vcc and FLT are rated up to 60V and can provide protection up to 60V with an external PFET.

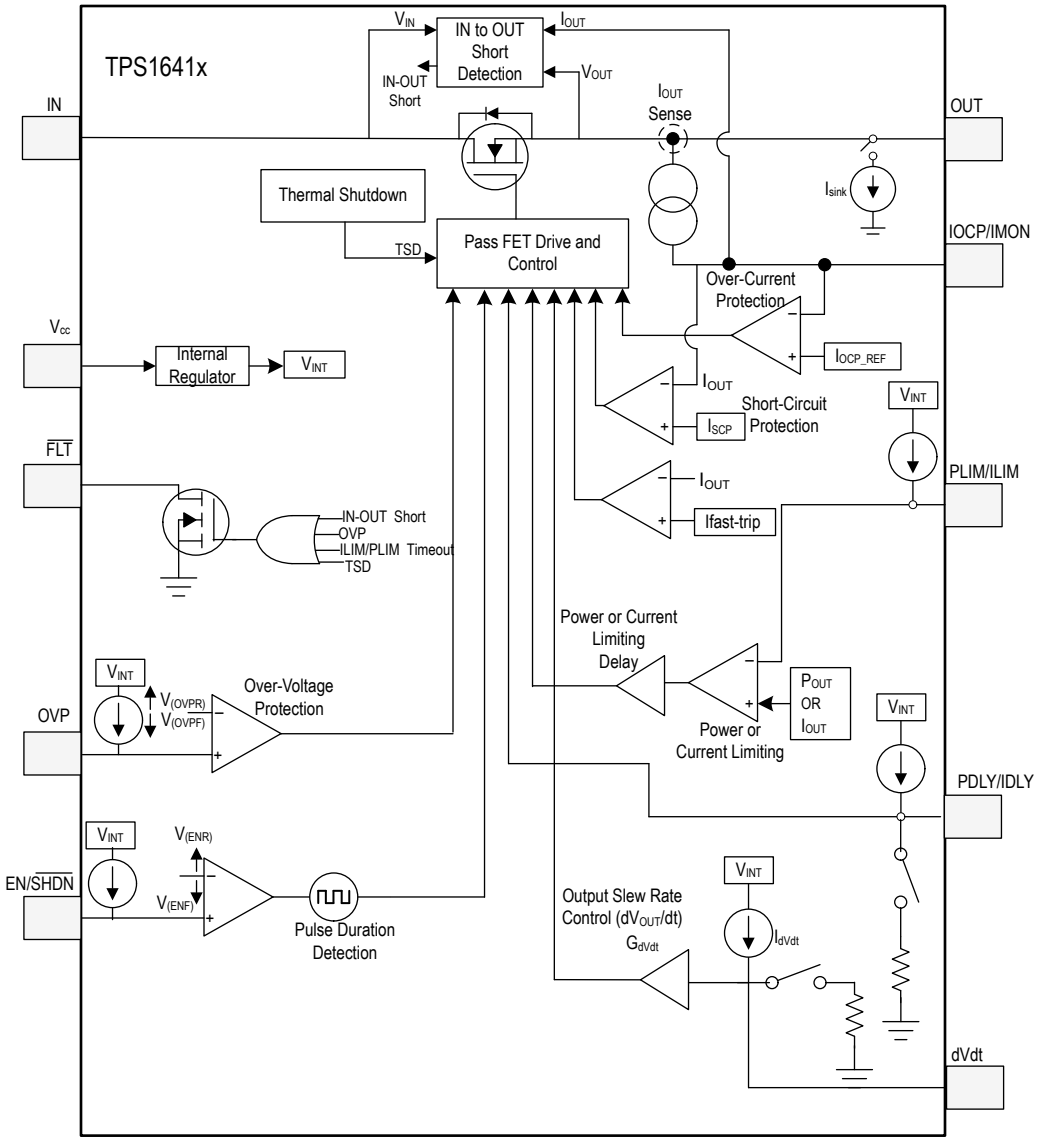

Figure 2-17. TPS16410

The LMR38020 converter is an easy-to-use synchronous step-down DC/DC converter that operates from a 4.2V to 80V supply voltage. The device is capable of delivering up to 2ADC load current in a small design size. The LMR38020 employs peak-current mode control. The device enters PFM mode at light load to achieve high efficiency for PFM version. A FPWM version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. The device is internally compensated, which reduces design time, and requires few external components. Additional features, such as precision enable and internal soft start, provide a flexible and easy-to-use design for a wide range of applications. Protection features include thermal shutdown, VIN undervoltage lockout, cycle-by-cycle current limit, and hiccup mode short-circuit protection. The family requires few external components and has a pinout designed for a simple PCB layout.

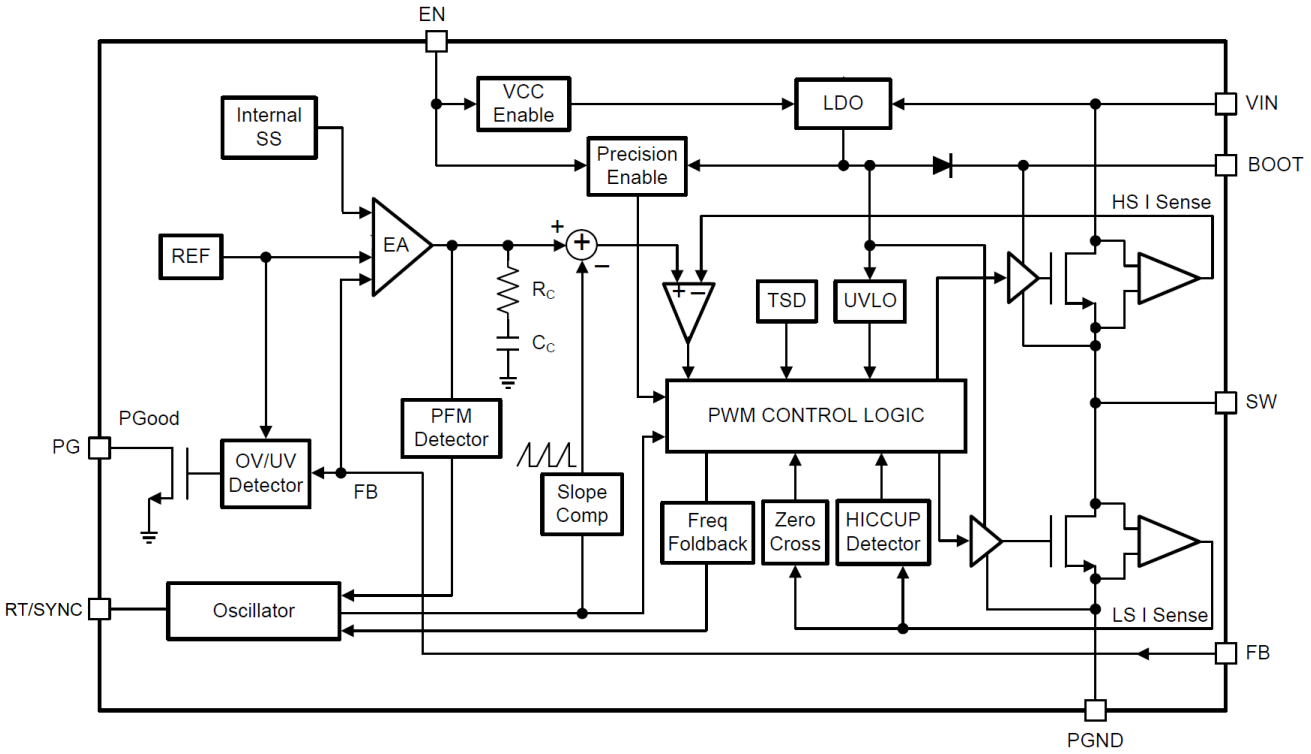

Figure 2-18. LMR38020

The TPS62932 and TPS62933x are 30V, 2A and 3A, synchronous buck (step-down) converters with two integrated n-channel MOSFETs. The TPS62932 and TPS62933x employ fixed-frequency peak current control mode for fast transient response and good line and load regulation. With the optimized internal loop compensation, the devices eliminate the external compensation components over a wide range of output voltage and switching frequency. The integrated 76mΩ and 32mΩ MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 2A (TPS62932) or 3A (TPS62933 and TPS62933x). The feedback reference voltage is designed at 0.8V. The output voltage can be stepped down from 0.8V to 22V. The devices are design for systems powered from 5V, 12V, 19V, and 24V power-bus rails. The TPS6293x has been designed for safe monotonic start-up into prebiased loads. The default start-up is at VIN equal to 3.8V. After the device is enabled, the output rises smoothly from 0V to the regulated voltage. The TPS6293x has low operating current when not switching under no load, especially the TPS62932, TPS62933, and TPS62933P whose operating current is 12µA (typical). When the TPS6293x is disabled, the supply current is approximately 2µA (typical). These features are extremely beneficial for long battery life time in low-power operation.

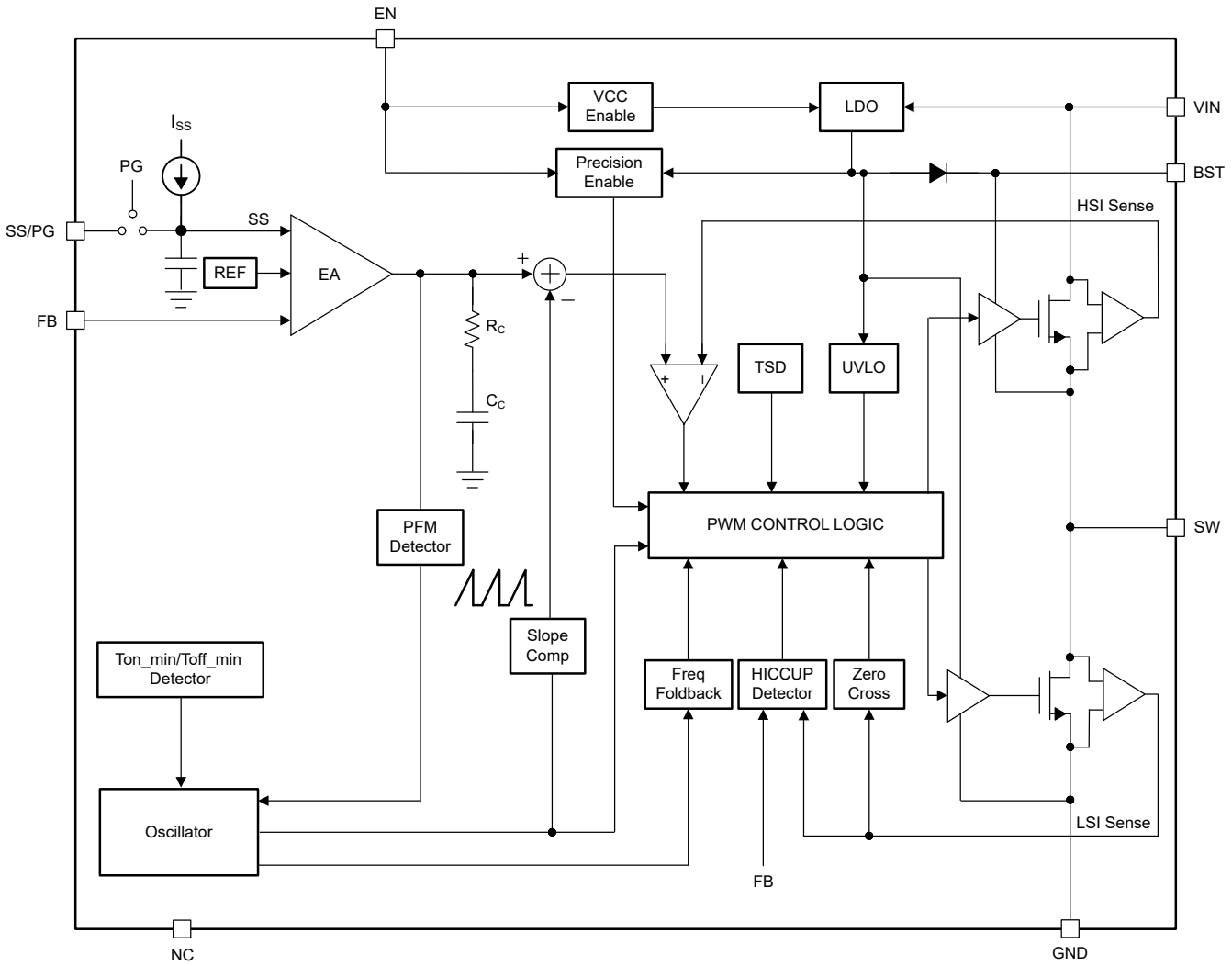

Figure 2-19. TPS62932

The DRV8316C device is an integrated 95mΩ (high-side + low-side MOSFETs on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, charge pump, current sense amplifiers, linear regulator and buck regulator for external loads. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external microcontroller. Alternatively, a hardware interface (pin) variant allows for configuring the most commonly used settings through fixed external resistors. The architecture uses an internal state machine to protect against short-circuit events and dv/dt parasitic turn-on of the internal power MOSFETs. The DRV8316C device integrates three, bidirectional current-sense amplifiers for monitoring the current level through each of the half-bridges using a built-in current sense. The gain setting of the amplifier can be adjusted through the SPI or hardware interface. In addition to the high level of device integration, DRV8316C provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD undervoltage lockout (AVDD_UV), buck regulator UVLO and overtemperature warning and shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI variant.

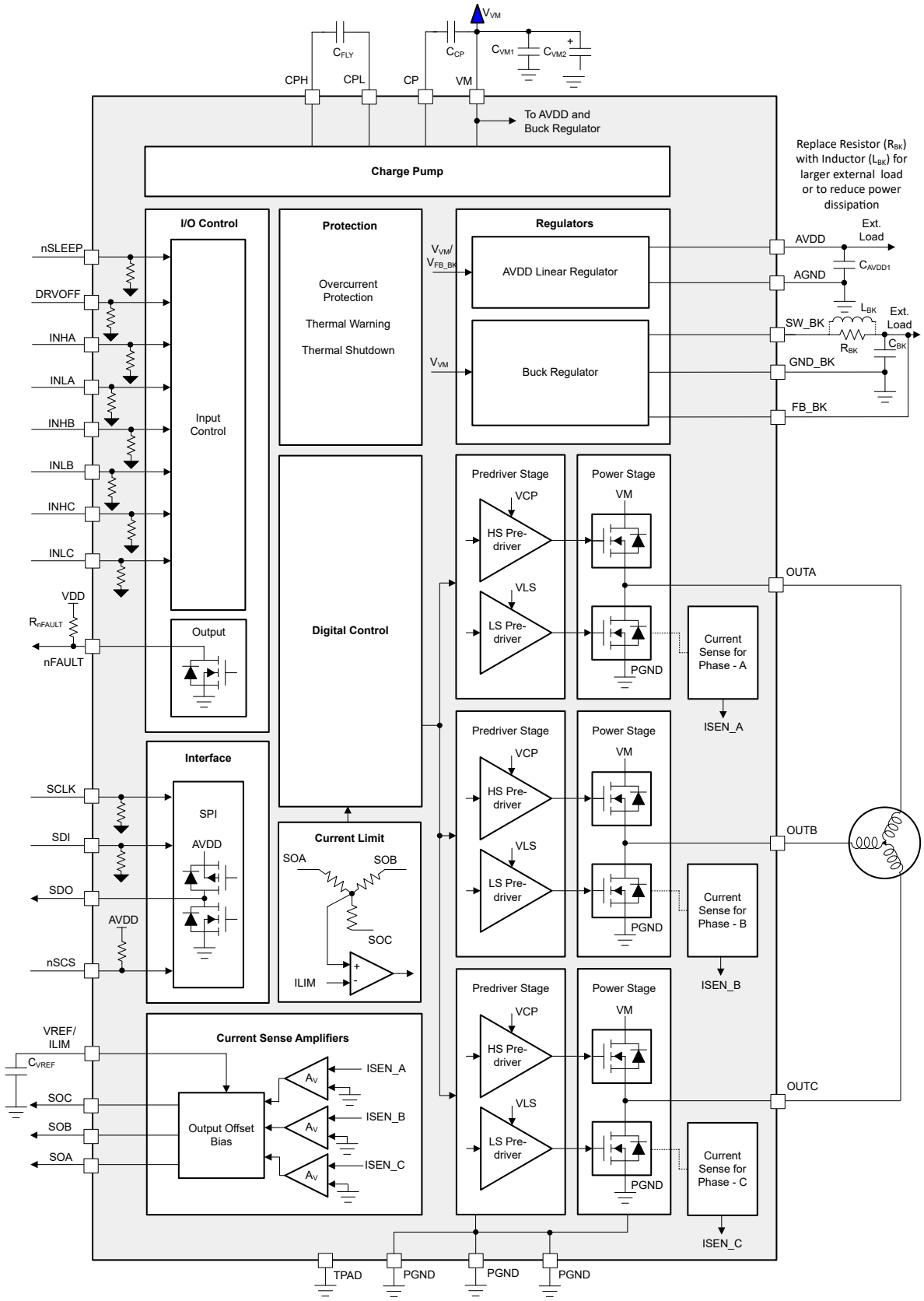

Figure 2-20. DRV8316C

The DRV8428 device is an integrated motor-driver design for bipolar stepper motors. The device provides the maximum integration by integrating two N-channel power MOSFET H-bridges, current sense resistors and regulation circuitry, and a microstepping indexer. The DRV8428 is capable of supporting wide supply voltage range of 4.2V to 33V. DRV8428 provides an output current up to 1.7A peak, 1A full-scale, or 0.7A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability. The DRV8428 uses an integrated current-sense architecture which eliminates the need for two external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREF pin. A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal microstepping indexer can execute high-accuracy micro-stepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping. High microstepping contributes to significant audible noise reduction and smooth motion. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM. Stepper motor drivers need to re-circulate the winding current by implementing several types of decay modes. The DRV8428 comes with smart tune decay modes. The smart tune is a remarkable decay mechanism that automatically adjusts for the best current regulation performance agnostic of voltage, motor speed, variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple current control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic fast decay percentage scheme to minimize distortion of the motor winding current while minimizing frequency content and significantly reducing design efforts. Along with this seamless, effortless automatic smart tune, DRV8428 also provides the traditional mixed decay mode. A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

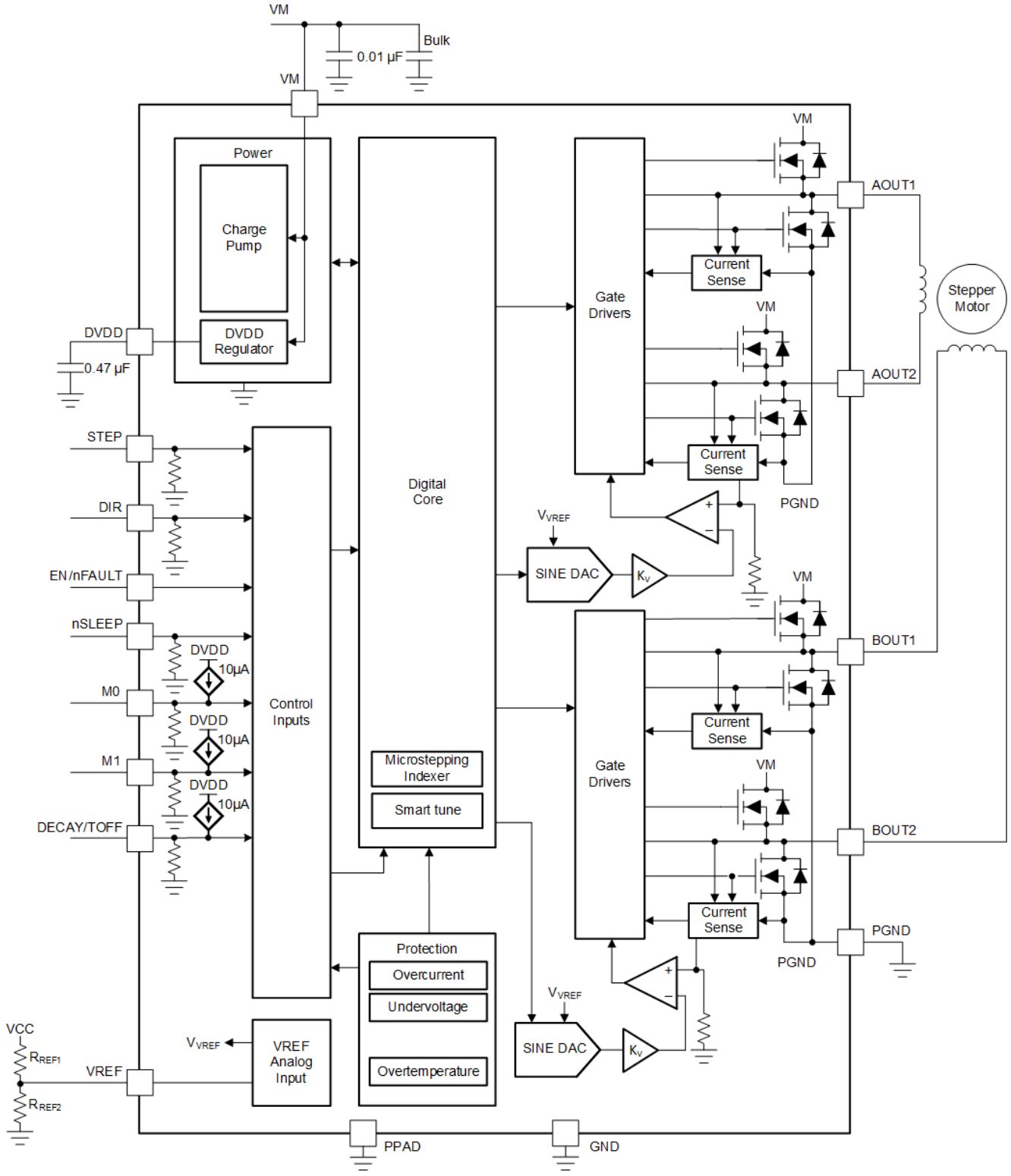

Figure 2-21. DRV8428

The ISO1211 and ISO1212 devices are fully-integrated, isolated digital-input receivers with IEC 61131-2 Type 1, 2, and 3 characteristics. The devices receive 24V to 60V digital-input signals and provide isolated digital outputs. No field-side power supply is required. An external resistor, RSENSE, on the input-signal path precisely sets the limit for the current drawn from the field input based on an internal feedback loop. The voltage transition thresholds are compliant with Type 1, 2, and 3 and can be increased further using an external resistor, RTHR.

For more information on selecting the RSENSE and RTHR resistor values, see the Detailed Design Procedure section. The ISO121x devices use an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The conceptual block diagram of the ISO121x device is shown in the Functional Block Diagram section.

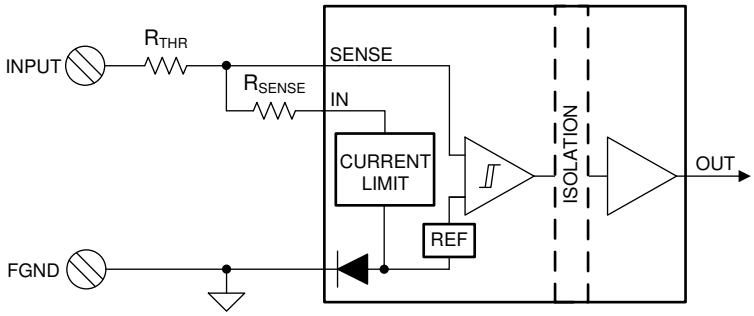

Figure 2-22. ISO1212

This family of CAN transceivers is compatible with the ISO11898-2 High-Speed CAN (controller area network) physical layer standard. The CAN transceivers are designed to interface between the differential bus lines in CAN and the CAN protocol controller.

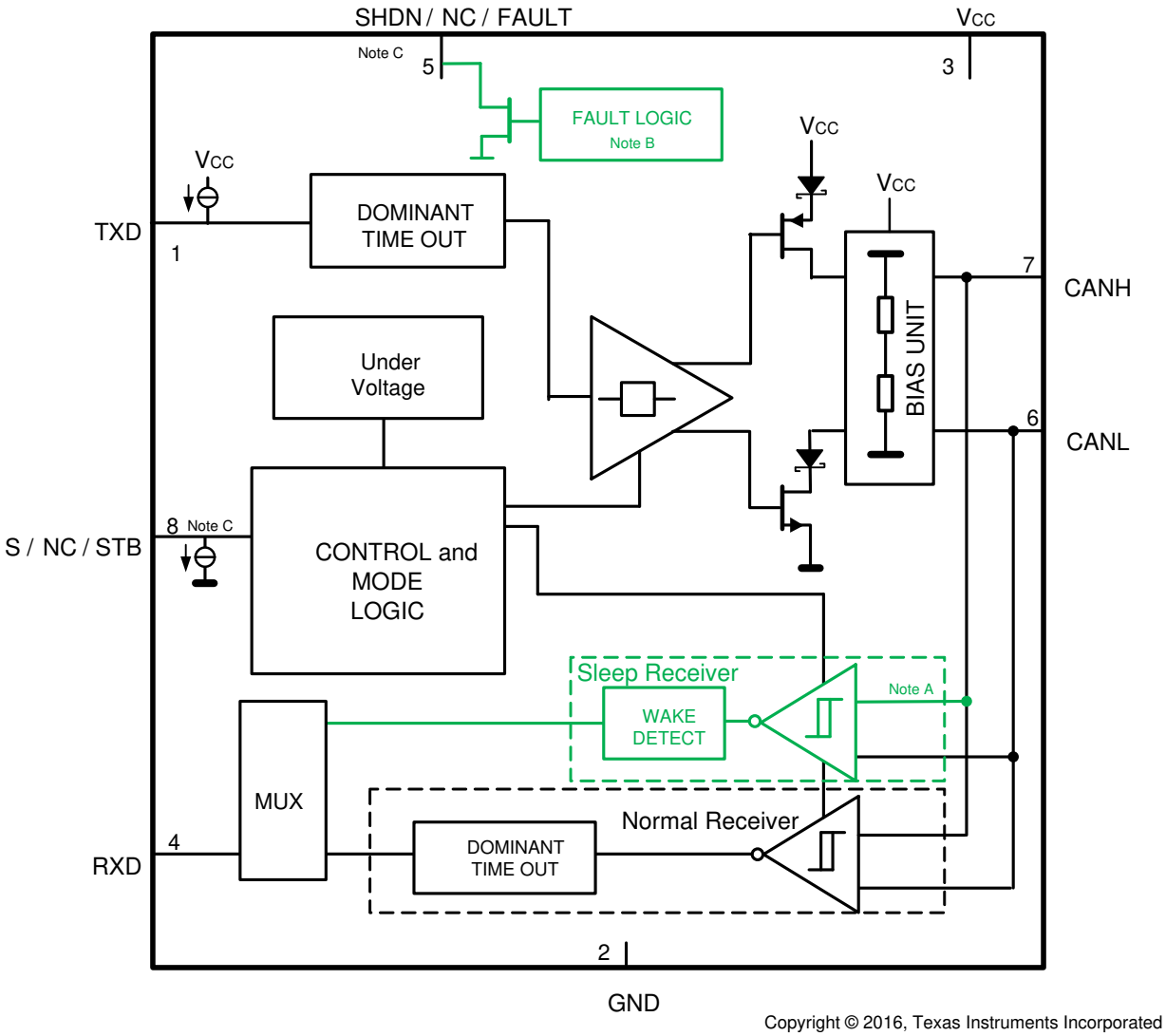

Figure 2-23. TCAN334

MSPM0G350x microcontrollers (MCUs) are part of the MSP highly integrated, ultra-low-power 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ 32-bit core platform operating at up to 80MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages ranging from 1.62V to 3.6V. The MSPM0G350x devices provide up to 128KB embedded flash program memory with built-in error correction code (ECC) and up to 32KB SRAM with hardware parity option. These MCUs also incorporate a memory protection unit, 7-channel DMA, math accelerator, and a variety of high-performance analog peripherals such as two 12-bit 4Msps ADCs, configurable internal shared voltage reference, one 12-bit 1Msps DAC, three high speed comparators with built-in reference DACs, two zero-drift zero-crossover op-amps with programmable gain, and one general-purpose amplifier. These devices also offer intelligent digital peripherals such as two 16-bit advanced control timers, five general-purpose timers (with one 16-bit general-purpose timer for QEI interface, two 16-bit general-purpose timers for STANDBY mode, and one 32-bit general-purpose timer), two windowed-watchdog timers, and one RTC with alarm and calendar modes. These devices provide data integrity and encryption peripherals (AES, CRC, TRNG) and enhanced communication interfaces (four UART, two I2C, two SPI, CAN 2.0/FD).

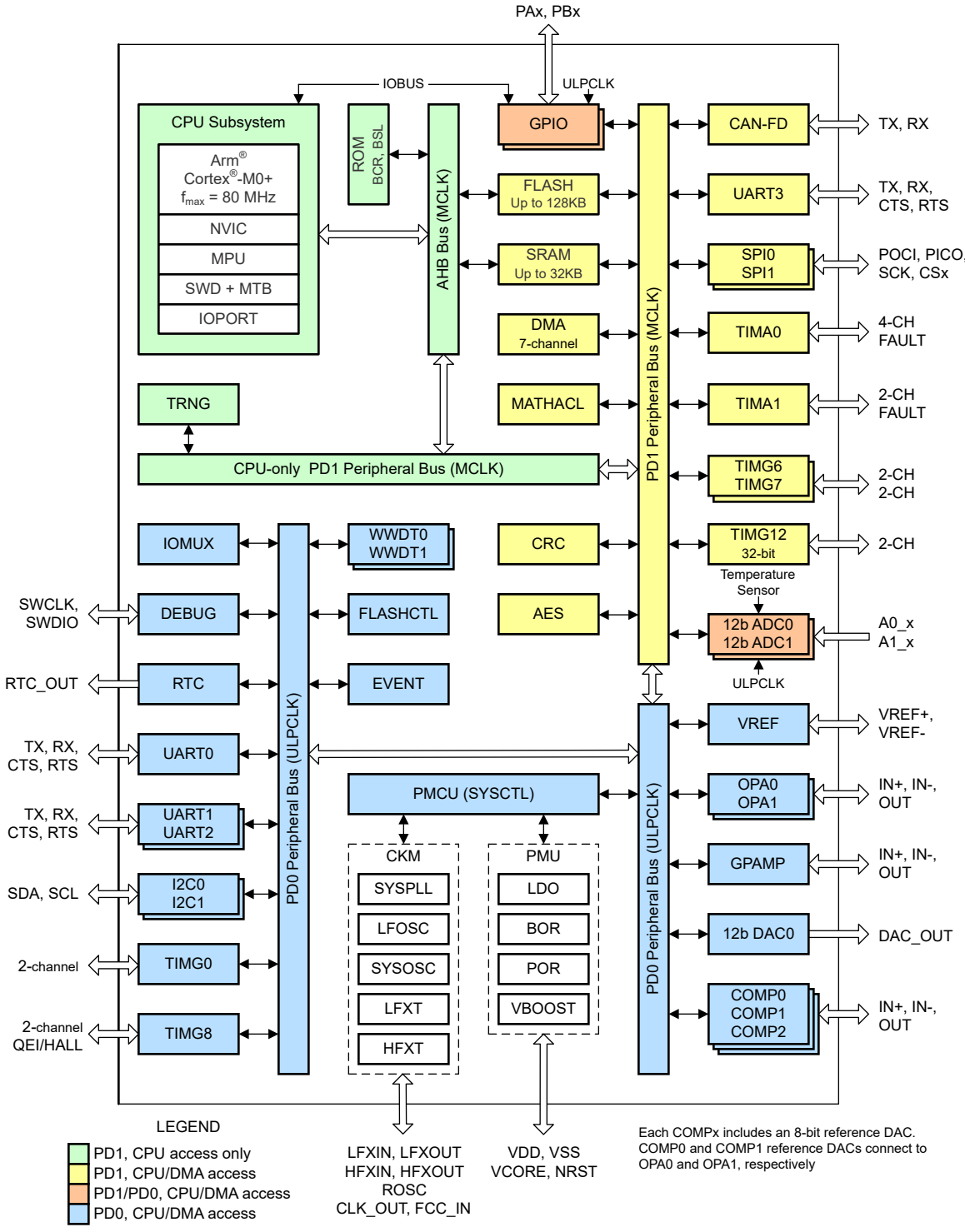

Figure 2-24. MSPM0G3507

The TMAG5273 IC is based on the Hall-effect technology and precision mixed signal circuitry from Texas Instruments. The output signals (raw X, Y, Z magnetic data and temperature data) are accessible through the I2C interface. The IC consists of the following functional and building blocks:

- The Power Management and Oscillator block contains a low-power oscillator, biasing circuitry, undervoltage detection circuitry, and a fast oscillator.

- The sensing and temperature measurement block contains the Hall biasing, Hall sensors with multiplexers, noise filters, integrator circuit, temperature sensor, and the ADC. The Hall-effect sensor data and temperature data are multiplexed through the same ADC.
- The Interface block contains the I2C control circuitry, ESD protection circuits, and all the I/O circuits. The TMAG5273 supports multiple I2C read frames along with integrated cyclic redundancy check (CRC).

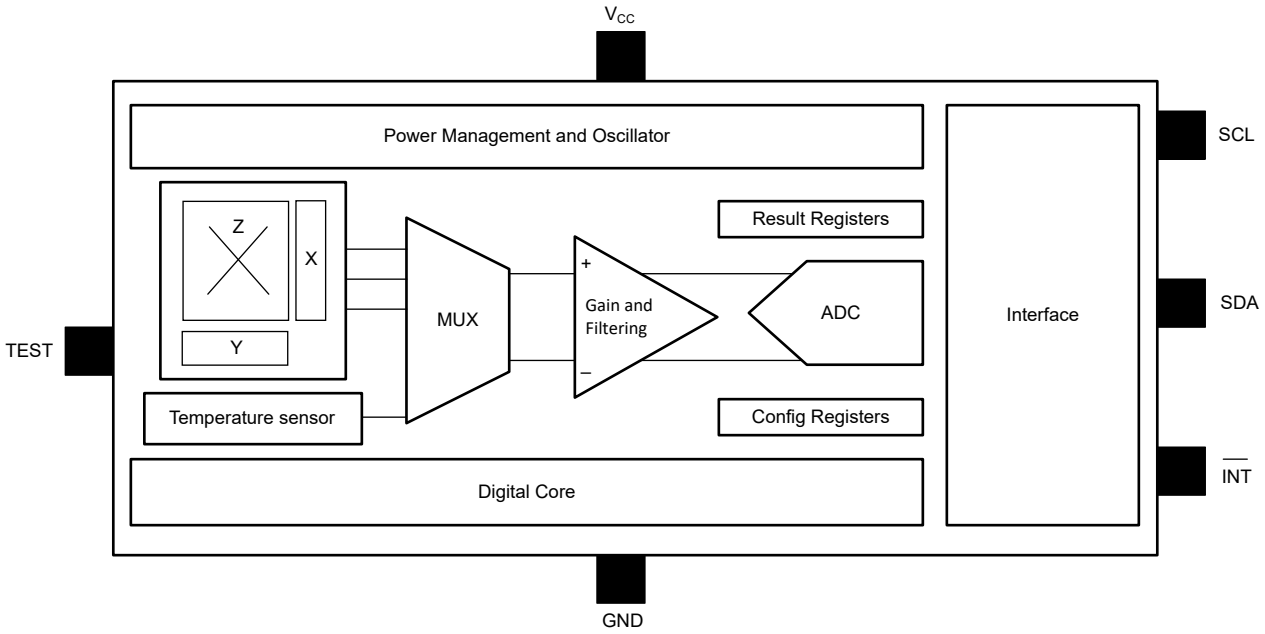

Figure 2-25. TMAG5273

The TLV900x is a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8V to 5.5V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV900x family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them an excellent choice for driving sampling analog-to-digital converters (ADCs).

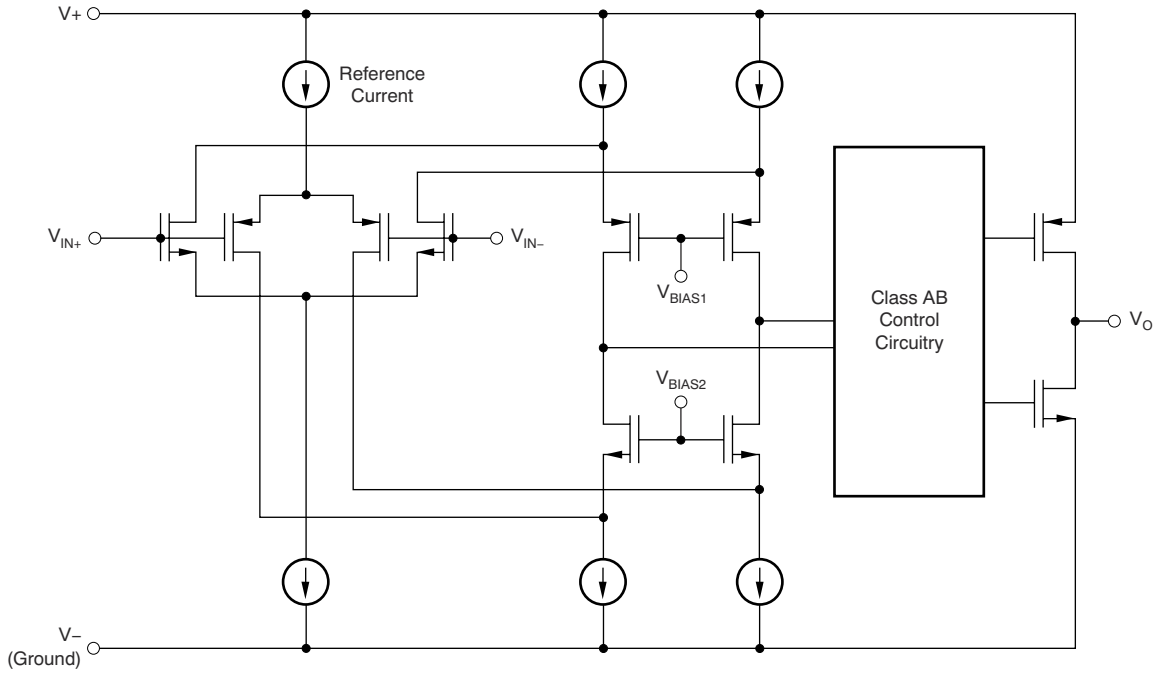

Figure 2-26. TLV9002

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

Figure 3-1 below shows the main interface connections for this reference design.

- The power can be switched from 24VAC to 24VDC or completely off based on the position of S1. This allows for flexibility with respect to the input power source while retaining the same functionality for devices down the line from the main power source. The 24VDC is connected via J19, and the 24VAC is connected via J18.
- J16 provides the connection for field inputs to the ISO1212 as well as the field ground.
- J21 is the connection point for the CAN interface.
- J22 is the connection point for the 4-10mA control input front-end. These pins must not be shorted with a jumper during evaluation.
- J15 is the connection point for the 0-10V control input front-end. These pins must not be shorted with a jumper during evaluation.
- J2 is the JTAG connector for deploying firmware to the embedded MSPM0.
- J8 provides the connection of the BLDC motor hall effect sensors to the MCU. A 3.3V connection and GND are also included in this connector for powering the Hall sensors.
- The J5, J6, and J7 srew terminal connectors are the output connections for the BLDC and stepper motor. J5 (B_{OUT}) and J6 (A_{OUT}) connect to the stepper motor, and J7 connects to the 3 phases of the BLDC motor.

There are also 4 LEDs on the board which indicate status:

- D4 – E-Fuse fault indication
- D1 – Damper position correct
- D5 – Error or motor drive fault
- D6 – Damper positional adjustment in progress

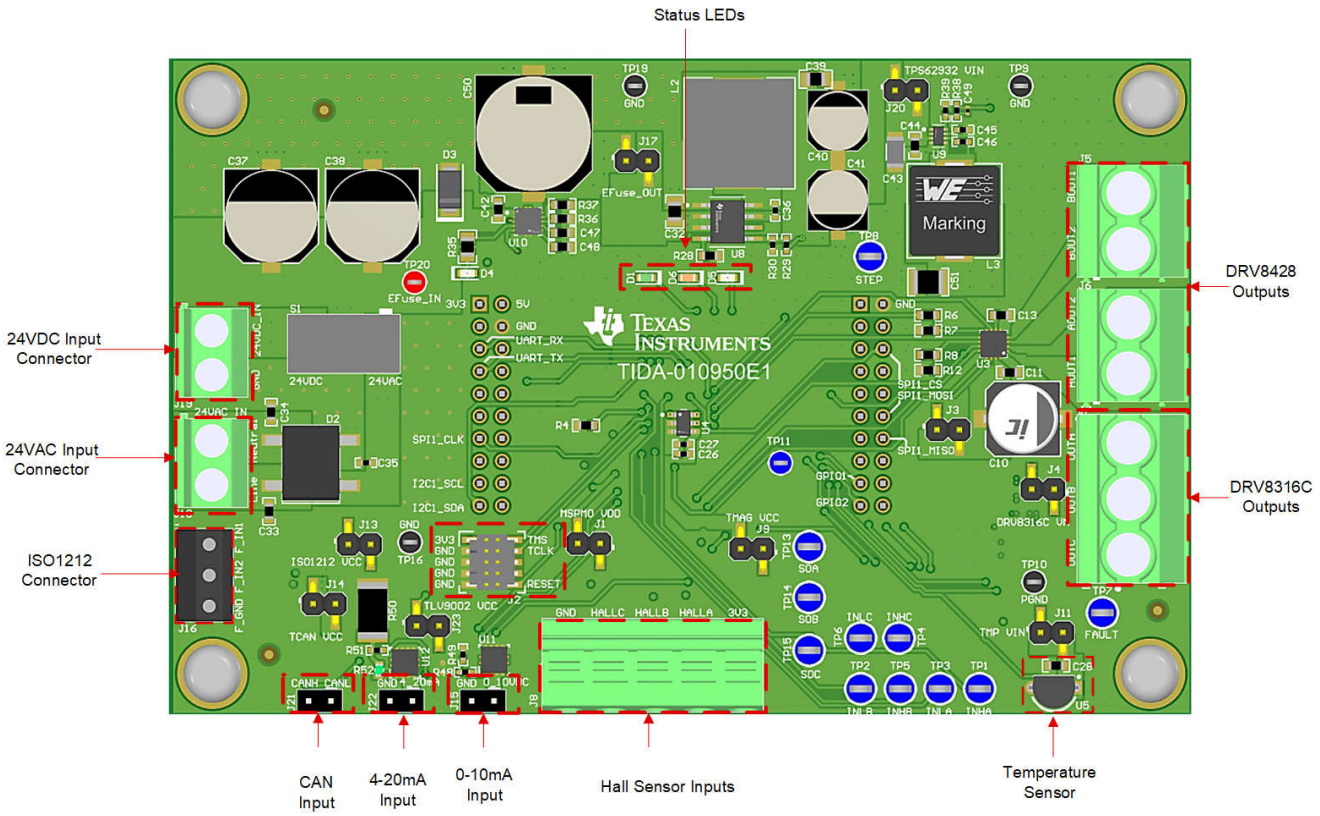

Figure 3-1. TIDA-010950 PCB Connections

3.2 Test Setup

Figure 3-2 and Figure 3-3 below show the lab test setup used to test the TIDA-010950 reference design. A DC power supply is used to provide the 24VDC rail to the input of the board, and a 120VAC-to-24VAC plug in transformer is used to provide power to the 24VAC input of the board.

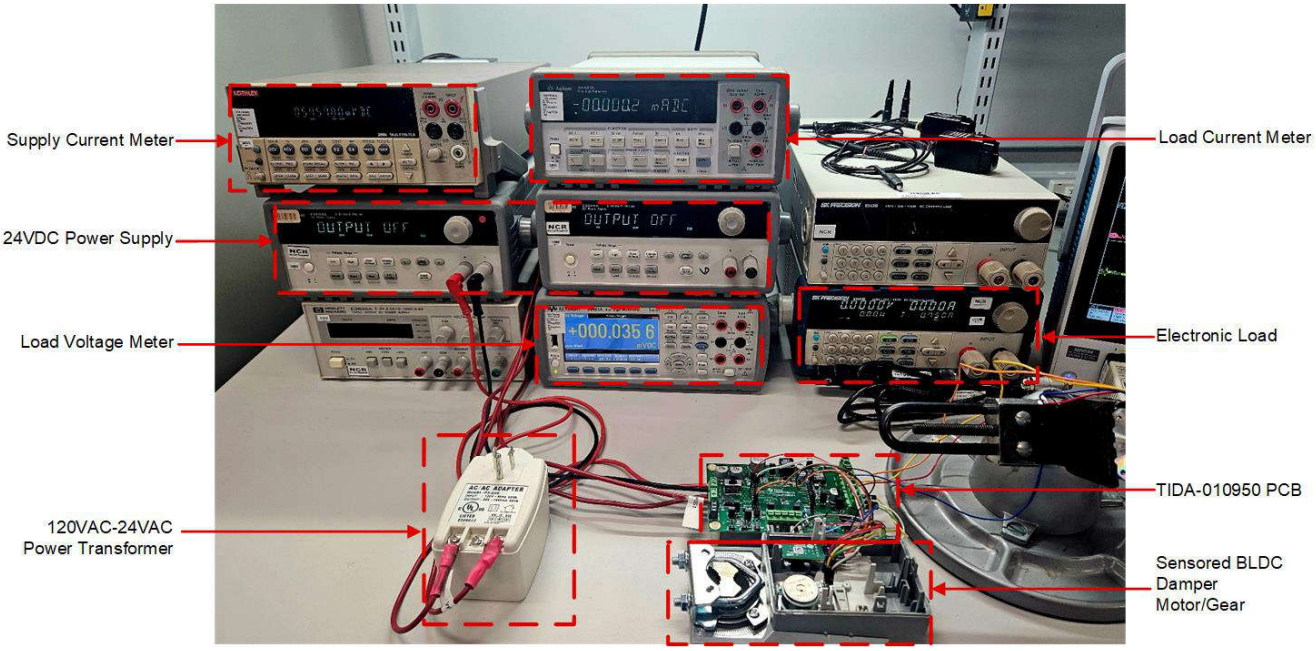

Figure 3-2. Lab Bench Test Setup I

For the BLDC testing, an end-user damper actuator platform is used. The control is handled by the reference design, but the BLDC motor, Hall sensors, and gear box of the existing product is used to replicate actual use in the field. For the EEV motor testing, an SS2421-5042 pancake bipolar stepper motor is used to replicate an EEV stepper motor.

Efficiency measurements are acquired leveraging an electronic load, in addition to several benchtop multi-meters for reading the input/output voltages and currents under each load step. The load for each buck is incrementally stepped from 100mA to 1A in 50mA step sizes.

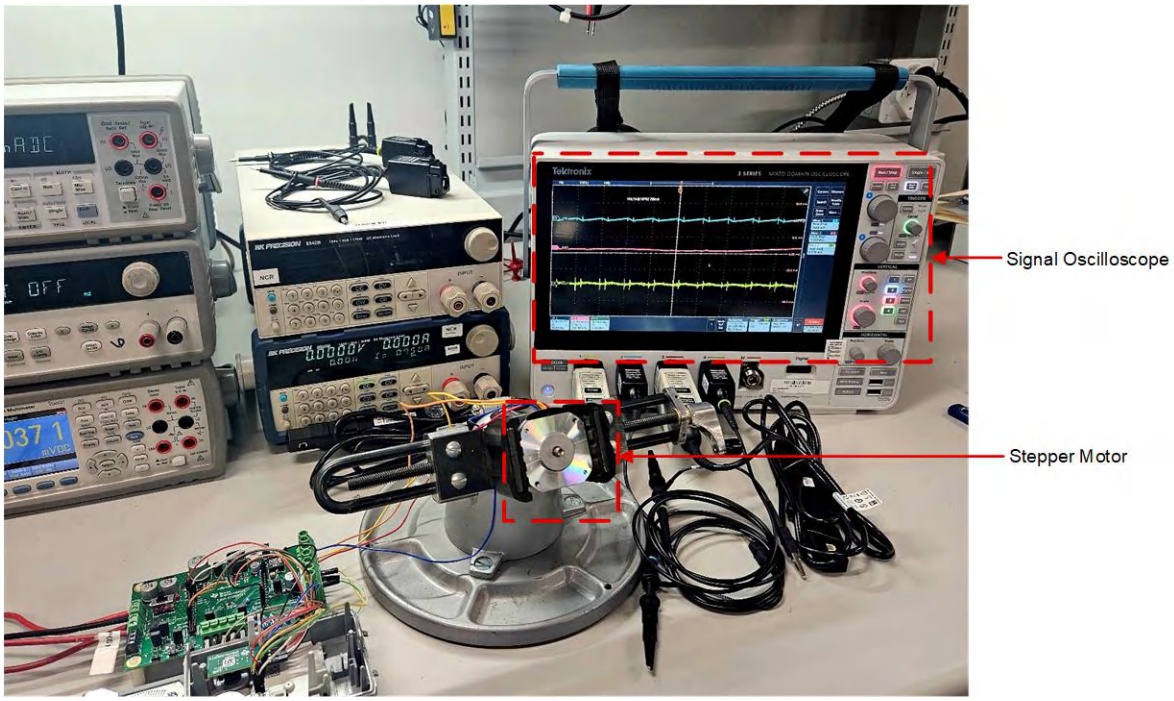

Figure 3-3. Lab Bench Test Setup II

The damper or EEV position is adjusted based on the input signal received from either the 0-10V control interface or the 4-20mA control interface. In addition, the EEV can be controlled by the temperature reading from the LMT84 as discussed in the software section.

3.3 Test Results

TPS16410 E-Fuse Test Results

To test the features of the TPS16410 e-fuse, an electronic load is used to draw the power from the supply. J17 in Figure 3-4 below shows the connection point for the E-load. The input power used for this test is a DC power supply operating at various voltages to capture the controlled start-up, the overvoltage and undervoltage protection response, in addition to the overcurrent protection and power limiting.

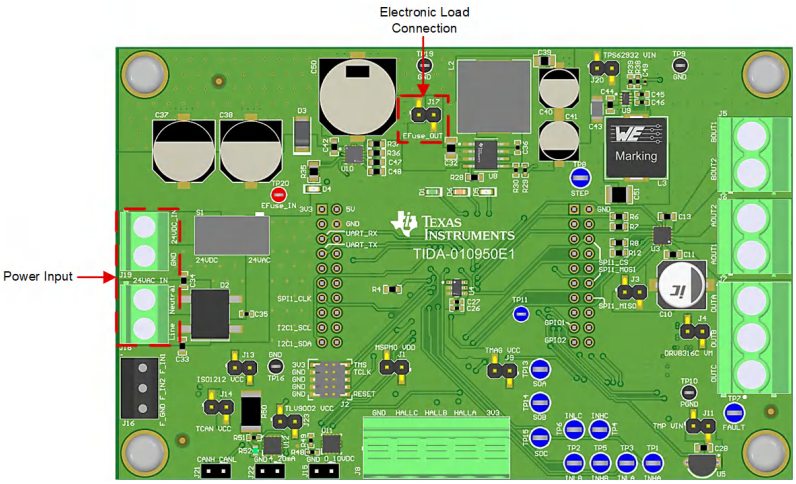

Figure 3-4. Board Connections Used to Test the TPS16410 E-Fuse

EFUSE startup, no load

Figure 3-5 below shows the start-up behavior of the TPS16410 when a voltage is applied to the input of the device and incrementally increased to just above the undervoltage threshold. Once the voltage reaches this point, the output voltage of the TPS16410 is enabled and there is a 1.98ms delay from the time the device is enabled to the time the input voltage is available on the output for downstream device power.

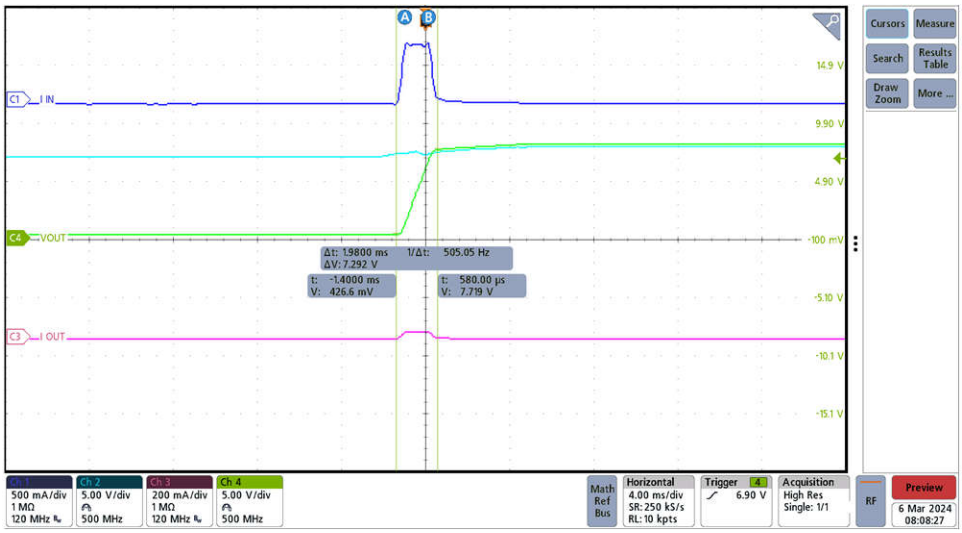

Figure 3-5. E-Fuse Start-up at No Load

Figure 3-6 below shows the response of the TPS16410 when power is turned on with a high load active. In this instance, the TPS16410 starts to regulate the power as expected but due to the inrush current associated with the already active load, the e-fuse eventually goes into a fault condition after approximately 200ms from the time the input voltage is turned on. The input power is limited to 14.30W for this test, yielding an error of approximately 3%.

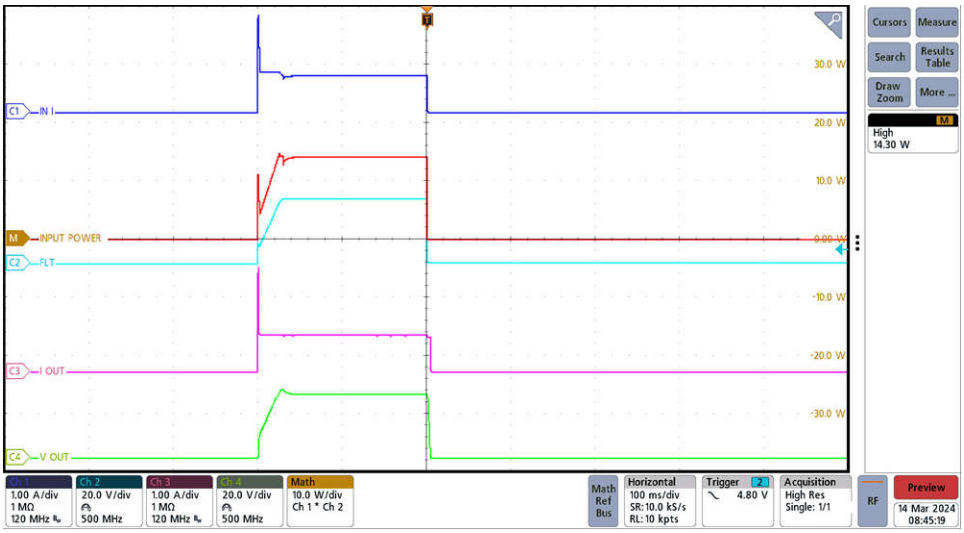

Figure 3-6. E-Fuse Regulation During Voltage Turn-On at High Load

Power Limiting

The TPS16410 circuit is designed to limit the power consumption to 13.65W for this design. For applications requiring a higher power limit (24VAC input), the equations in Section 2.2 can be used to adjust the power limit, or the device can be bypassed for evaluation.

If the device junction temperature reaches the thermal shutdown threshold (TSD), the internal FET is turned off. When the TPS16410 detects thermal overload, the device remains off until cooled down to T_{SDHYS}. Once the

TPS16410 has cooled down by T_{SDHYS}, the device remains off for an additional delay of $t_{TSD,RST}$ after which the device automatically retries to turn on if the device is still enabled. During thermal shutdown, the fault pin FLT pulls low to signal a fault condition.

Figure 3-7 below shows the power regulation of the device approaching the 13.7W threshold. The electronic load is set to constant power and gradually increased towards the power limit. As the load increases, the output voltage begins to droop to keep the power below the limit threshold. As the load is increased even more, the device disables the output. The TPS16410 has a power regulation accuracy of 99.5% for a P_{LIM} of 13.65W.

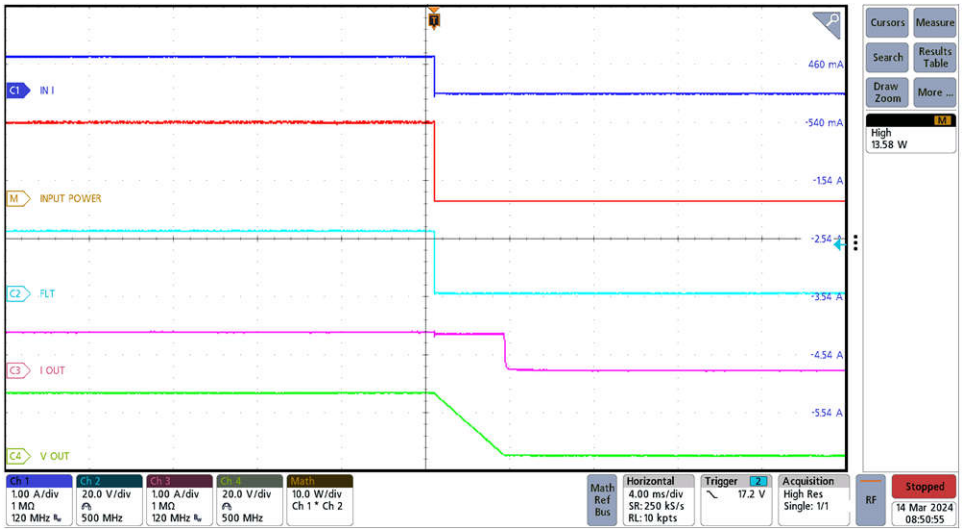

Figure 3-7. E-Fuse Power Limiting

Input Overvoltage protection

The TPS16410 device incorporates circuits to protect the system during overvoltage conditions. A voltage more than the V_{OVLO} threshold on the OVLO pin turns off the internal FET and protects the downstream load. The reference design is designed with overvoltage protection voltage of 28V with an input voltage of 24VDC and approximately 40V for a 24VAC input voltage. Figure 3-8 shows the overvoltage shut down at 28.13V, yielding an OVP accuracy of 99.5% for a 28V OVP threshold.

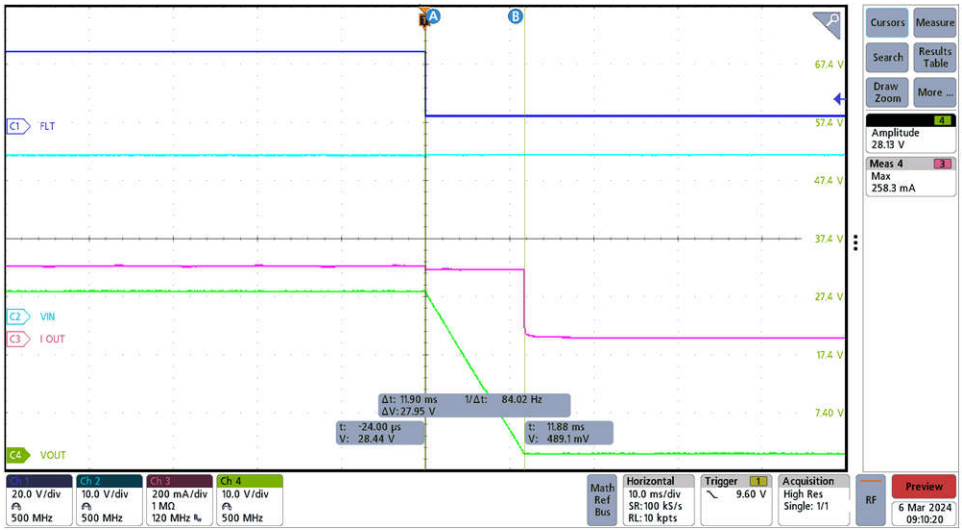

Figure 3-8. E-Fuse Input Overvoltage Protection Response

LMR38020 15V Power Rail Test Results

To test the efficiency of the LMR38020 across loads of 100mA to 1A, both 24VAC as well as 24VDC is provided to J18 and J19, respectively. An electronic load is used to create the specific load conditions for each test. The input voltage, the output voltage, and the output current ripple measurements are taken at the expected maximum allowable load while staying under the 15W total power limit.

Figure 3-9 below shows the voltage ripple of both input and output voltages in addition to the output current ripple for a 1A load on the LMR38020. At this load, the total consumption is right under the limit set by the E-fuse. The input voltage ripple at 1A load is approximately 592mV $_{pk-pk}$, while the output voltage ripple is approximately 186mV $_{pk-pk}$. The output current to the load shows a current ripple of approximately 9.3mA, or about 9.3% ripple $_{pk-pk}$.

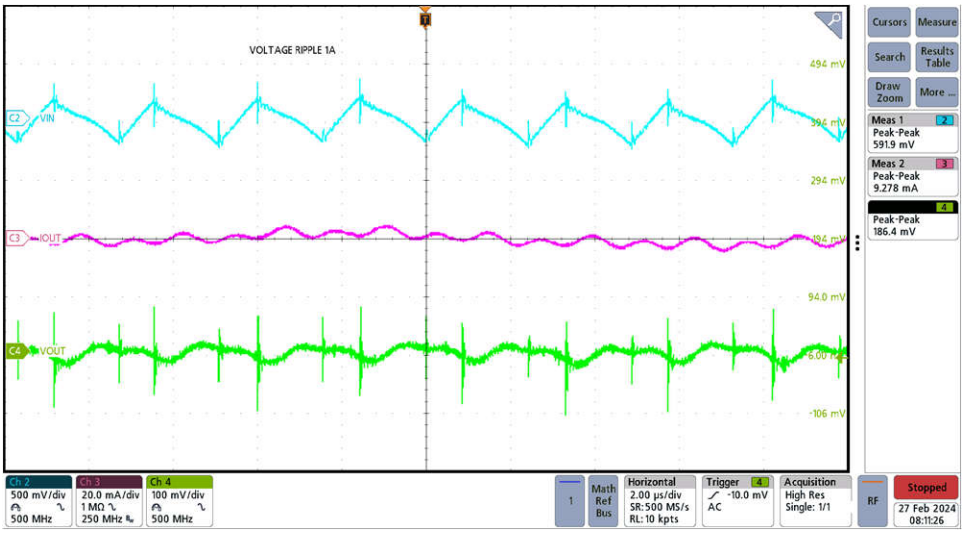

Figure 3-9. LMR38020 Output Voltage Ripple at 1A Load

Efficiency over load test results:

Table 3-1 below shows the test data for a 24VDC input to the LMR38020 with an electronic load on the output to the device. The load current range is increased from 100mA to 1A in 50mA steps.

Table 3-1. LMR38020 24VDC Input Efficiency Test Data

VIN (V)	IIN (mA)	VOUT (V)	IOUT (mA)	PIN (W)	POUT (W)	Efficiency
24	66.31	15.24	97.45	1.59	1.49	93.32
24	99.94	15.23	147.00	2.40	2.24	93.34
24	133.00	15.21	197.60	3.19	3.01	94.16
24	164.60	15.07	247.20	3.95	3.73	94.30
24	197.04	15.07	297.03	4.73	4.48	94.66
24	229.04	15.07	347.47	5.50	5.24	95.26
24	261.06	15.07	397.03	6.27	5.98	95.50
24	293.92	15.07	447.16	7.05	6.74	95.53
24	328.67	15.07	497.12	7.89	7.49	94.96
24	361.79	15.07	547.46	8.68	8.25	95.02
24	394.57	15.07	597.16	9.47	9.00	95.03
24	427.66	15.07	647.28	10.26	9.75	95.04
24	461.07	15.07	697.51	11.07	10.51	94.99
24	494.42	15.07	747.47	11.87	11.26	94.93
24	527.97	15.07	797.53	12.67	12.02	94.85
24	561.28	15.07	846.98	13.47	12.76	94.75
24	595.32	15.06	897.36	14.29	13.51	94.59
24	629.45	15.06	947.59	15.11	14.27	94.47
24	663.55	15.06	997.71	15.93	15.03	94.35

Figure 3-10 below shows the efficiency over load current. The efficiency across all load values is greater than 90%, peaking at 96% efficiency at a 450mA load current.

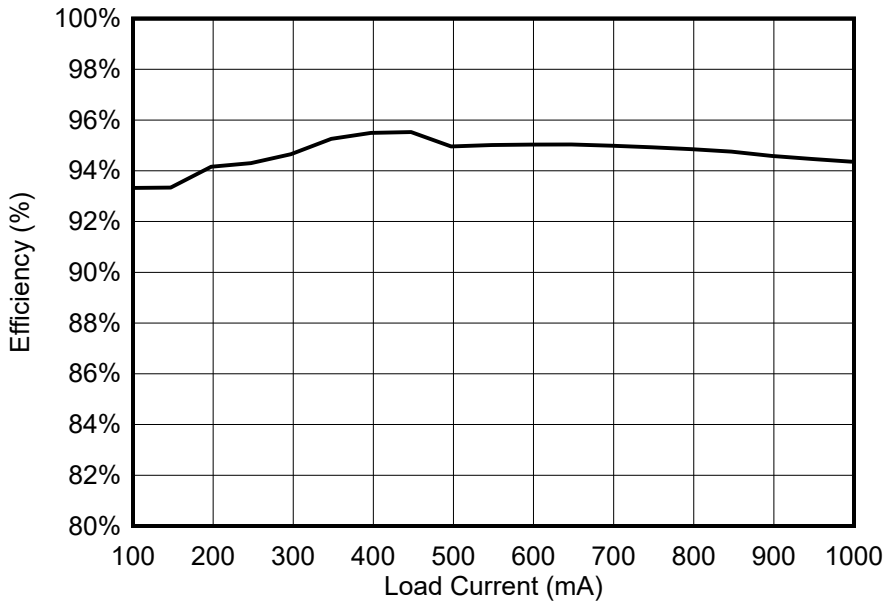

Figure 3-10. LMR38020 Efficiency Over Load With 24VDC Input

The same test is done for a 24VAC rectified input to the LMR38020, sweeping the load current again from 100mA to 1A in 50mA step sizes. This data is captured in Table 3-2 below.

Table 3-2. LMR38020 24VAC Input Efficiency Test Data

VIN (V)	IIN (mA)	VOUT (V)	IOUT (mA)	PIN (W)	POUT (W)	Efficiency
34.53	47.93	15.23	98	1.66	1.49	90%
34.22	72.91	15.22	147	2.49	2.24	90%
33.98	99.07	15.19	198	3.37	3.01	89%
33.78	120.37	15.06	248	4.07	3.73	92%
33.60	144.48	15.05	297	4.85	4.47	92%
33.39	168.70	15.04	348	5.63	5.23	93%
33.22	192.62	15.04	397	6.40	5.97	93%
33.01	218.14	15.03	447	7.20	6.72	93%
32.82	244.57	15.03	497	8.03	7.47	93%
32.61	270.47	15.03	548	8.82	8.24	93%
32.44	296.54	15.02	597	9.62	8.97	93%
32.23	323.26	15.02	648	10.42	9.73	93%
32.03	350.78	15.02	698	11.24	10.48	93%
31.82	378.61	15.01	748	12.05	11.23	93%
31.63	407.28	15.01	798	12.88	11.98	93%
31.42	435.92	15.00	847	13.70	12.71	93%
31.22	465.80	15.00	898	14.54	13.47	93%
31.00	496.66	15.00	948	15.40	14.22	92%
30.78	528.17	14.99	997	16.26	14.95	92%

Figure 3-11 below shows the efficiency versus load current for a rectified 24VAC input voltage to the LMR38020. The efficiency peaks at 93% and has a relatively flat efficiency curve from 350mA to 900mA load current.

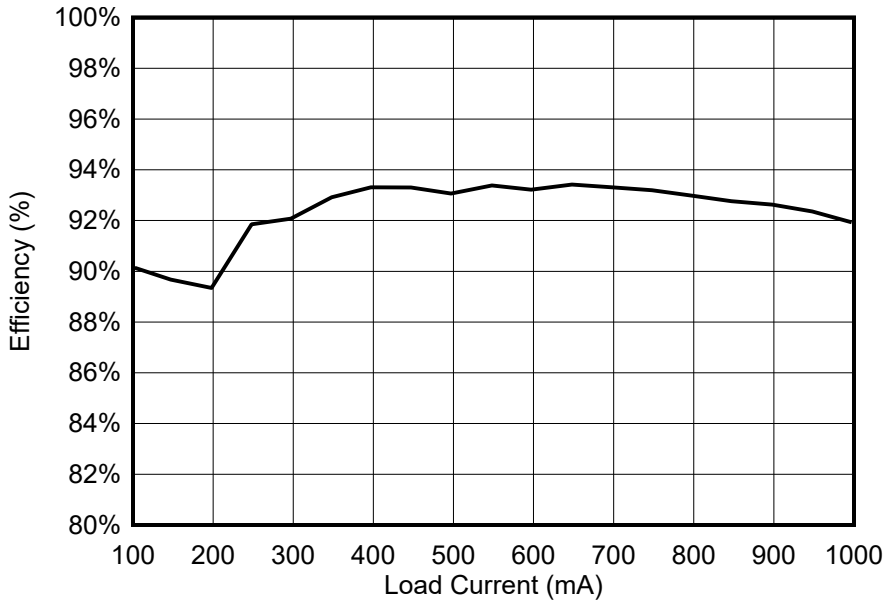

Figure 3-11. LMR38020 Efficiency Over Load With 24VAC Input

TPS62932 3.3V Power Rail Test Results

The test procedure for testing the efficiency of the TPS62932 under varying load conditions is identical to the test for the LMR38020 above. In this case, we are pulling 100mA to 1A from the 3.3VDC power rail while providing 15VDC to the input of the buck. This is done to isolate the performance of the 3.3VDC buck.

For the load on the 3.3V power rail, a worst-case scenario of 750mA is used as the load current to measure the input voltage ripple, output voltage ripple, and the output current ripple. Figure 3-12 below shows the ripple for each of the aforementioned parameters. The input voltage ripple **pk-pk** is 192mV, or approximately 1.3%. The output voltage ripple **pk-pk** is about 80.8mV, or about 2.4%. The output current ripple **pk-pk** is around 5.3mA or approximately 0.7%.

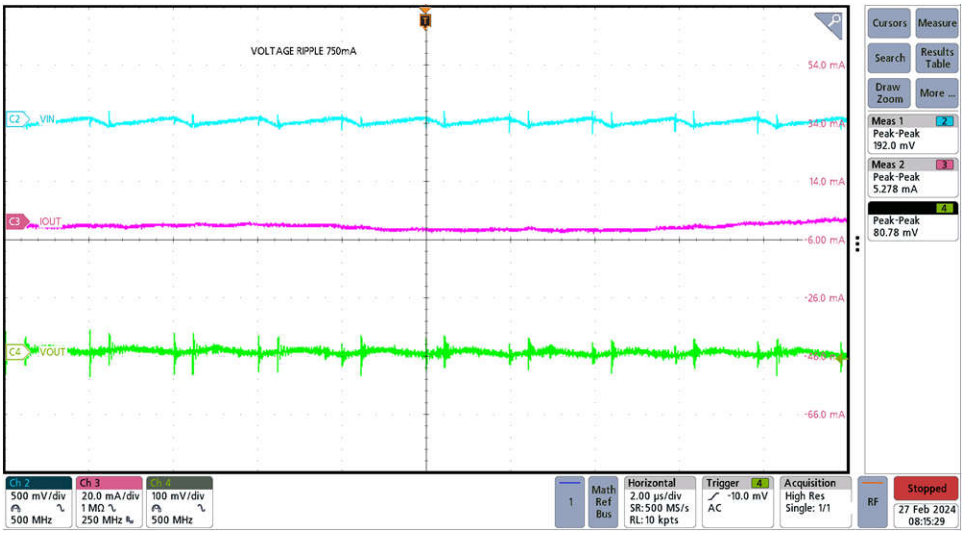

Figure 3-12. TPS62932 Ripple at 750mA Load

Efficiency Results:

Table 3-3 below shows the data captured for the efficiency test of the TPS62932. This test is identical to that of the LMR38020 for load current test values, although the 3.3V power rail total power consumption is much lower since the power rail is only used for the MCU and the board peripherals.

Table 3-3. TPS62932 Efficiency Test Data

VIN (V)	IIN (mA)	VOUT (V)	IOUT (mA)	PIN (W)	POUT (W)	Efficiency
15	25.56	3.28	97.75	0.38	0.32	83.63
15	39.02	3.27	147.26	0.59	0.48	82.27
15	51.06	3.27	197.82	0.77	0.65	84.46
15	62.96	3.27	247.44	0.94	0.81	85.68
15	74.90	3.2	297.26	1.12	0.97	86.52
15	86.85	3.27	347.68	1.30	1.14	87.27
15	98.91	3.27	397.25	1.48	1.30	87.55
15	110.56	3.26	447.34	1.66	1.46	87.94
15	120.11	3.26	497.31	1.80	1.62	89.99
15	131.23	3.26	547.69	1.97	1.79	90.70
15	142.08	3.26	597.36	2.13	1.95	91.38
15	152.94	3.26	647.48	2.29	2.11	92.01
15	164.29	3.26	697.71	2.46	2.27	92.30
15	175.78	3.26	747.67	2.64	2.44	92.44
15	187.34	3.26	797.72	2.81	2.60	92.54
15	198.81	3.26	847.20	2.98	2.76	92.61
15	210.50	3.25	897.58	3.16	2.92	92.39
15	222.17	3.25	947.63	3.33	3.08	92.42
15	233.76	3.25	997.25	3.51	3.24	92.43

Figure 3-13 below shows the efficiency of the TPS62932 versus load current. The efficiency peaks at 92.61% at an 850mA load, but since the total load on the 3.3V rail is much lower than this, the efficiency during operation has an average efficiency in the mid 80% range.

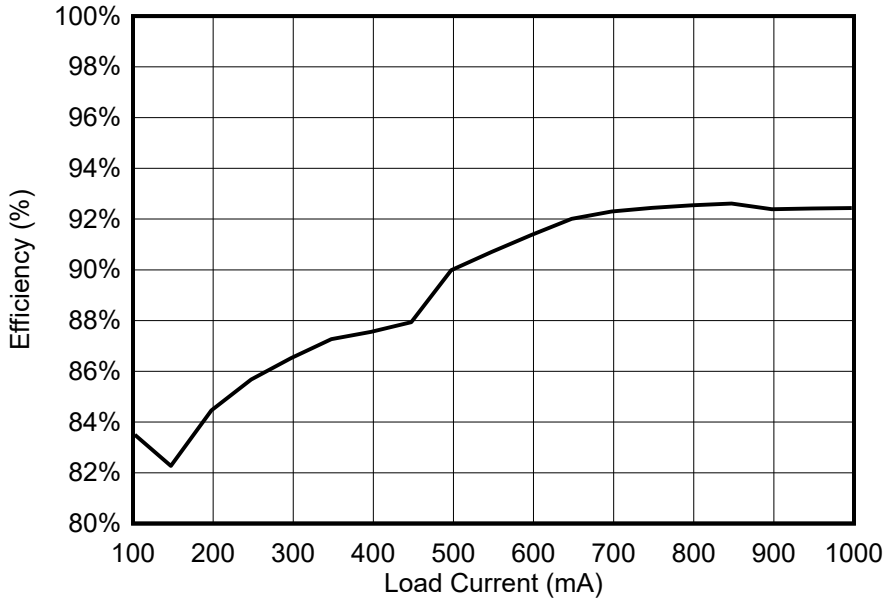

Figure 3-13. TPS62932 Efficiency Over Load

DRV8316 Test Results

To test the operational functionality of the DRV8316C, an actual end-user product is used to test performance of the TI device. The portions of the product used by this reference design are the Hall effect sensors, the BLDC damper motor, and the gears which effectively transfer the energy of the motor turning to the damper. The main test setup is shown below in Figure 3-14. As the motor rotates, a small portion of the gear network that is available is leveraged along with a magnet placed inside the gear cavity for rotation information. The TMAG5273 board is then mounted directly over the magnet/gear and sends angle data back to the main board during operation.

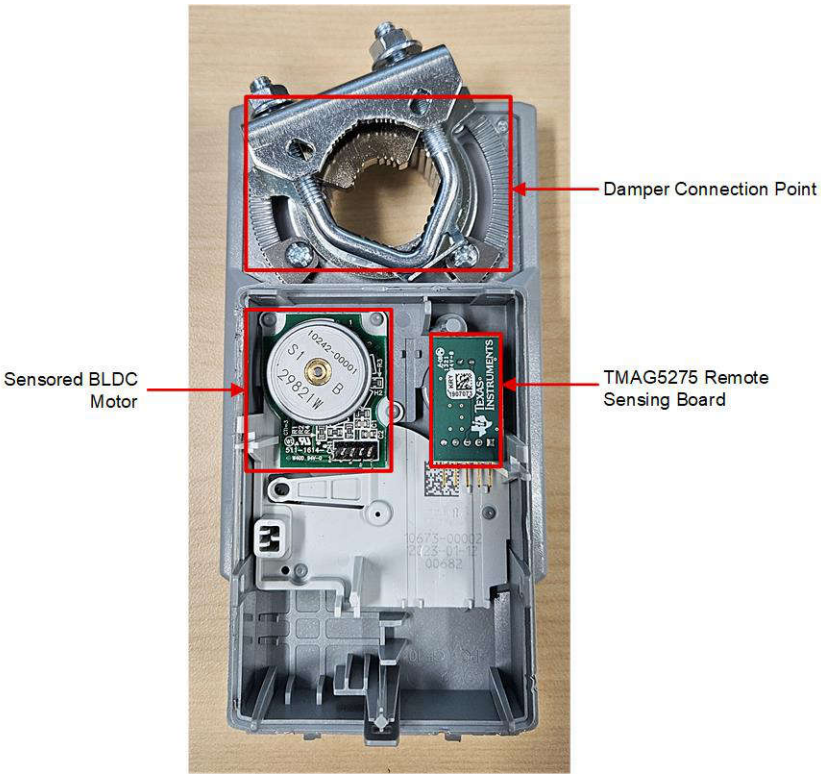

Figure 3-14. BLDC Damper Control Test Setup

One important note regarding the damper motor/gear is that the rotation to the left requires a higher current, while rotating to the right requires much less current. In this section, over to right (OTR) refers to the lower current rotation of the damper to the right while over to left represents the higher current rotation of the BLDC motor to the left.

A secondary TMAG5273 board is employed as a means of remotely detecting the damper position due to the size of the reference design and lack of mounting options for the board to the product. the TMAG5273 remote board is shown in Figure 3-15 below.

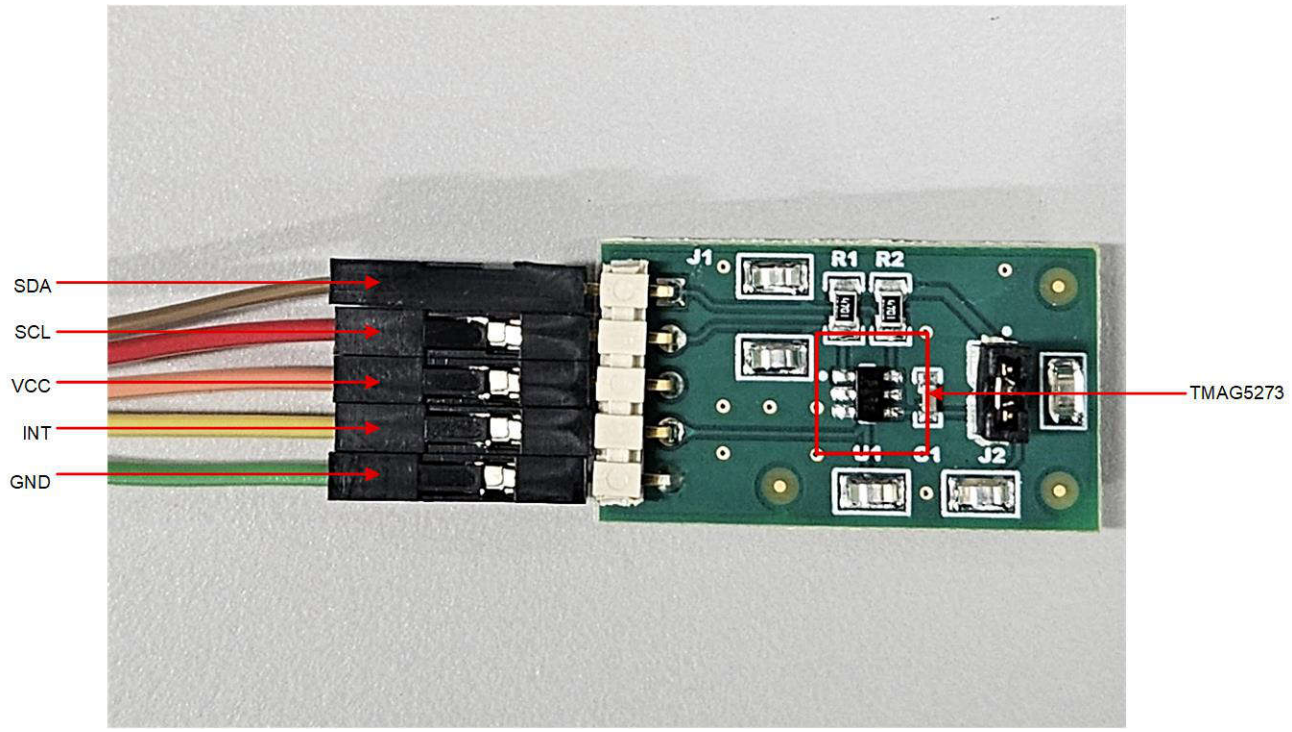

Figure 3-15. TMAG5273 Remote Sensing Board for BLDC Motor Position Sensing

Figure 3-16 below shows the motor voltage output on each of the 3 phases during OTL operation. The output to the BLDC motor is 120º between each phase and the output voltage to the BLDC motor is ranges from 15.38V to 15.73V for each output phase.

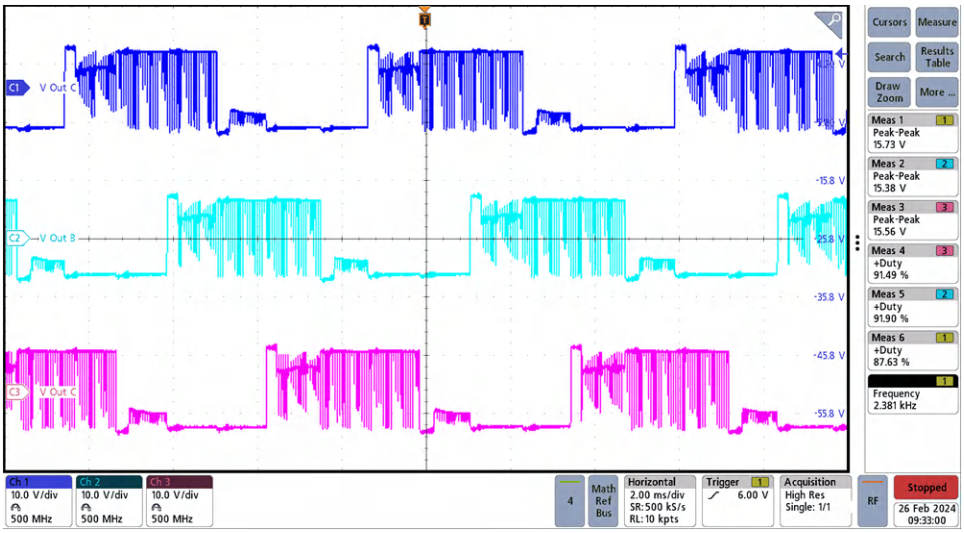

Figure 3-16. DRV8316C Voltage Output for Each Phase

DRV8316C phase current during operation: Figure 3-17 Below shows the output current for each phase of the BLDC motor during OTL operation. The phase current waveforms are 120 degrees between phase with a total RMS current of 474.6mA. The RMS current is captured during the high current rotation to the left.

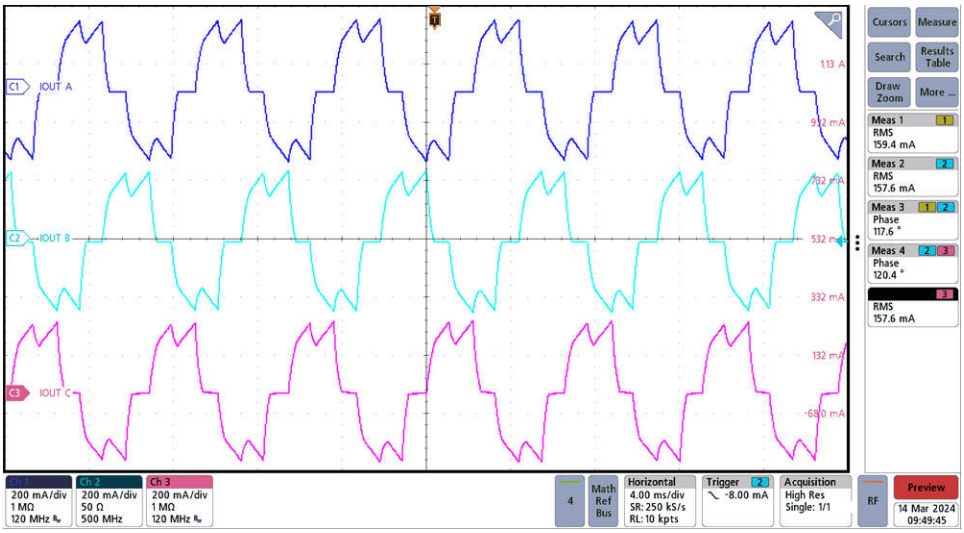

Figure 3-17. DRV8316C Output Current During Motor Operation

The waveform below in Figure 3-18 shows the current at the input to the DRV8316C during OTL operation of the BLDC motor. The current consumed by the DRV8316C peaks at approximately 187mA while driving the sensored BLDC motor apparatus with an RMS value of 190.1mA over the duration of movement. The Input voltage is AC coupled to extract the voltage ripple during operation. The voltage ripple is approximately 201mV during the high load rotation of the damper motor to the left.

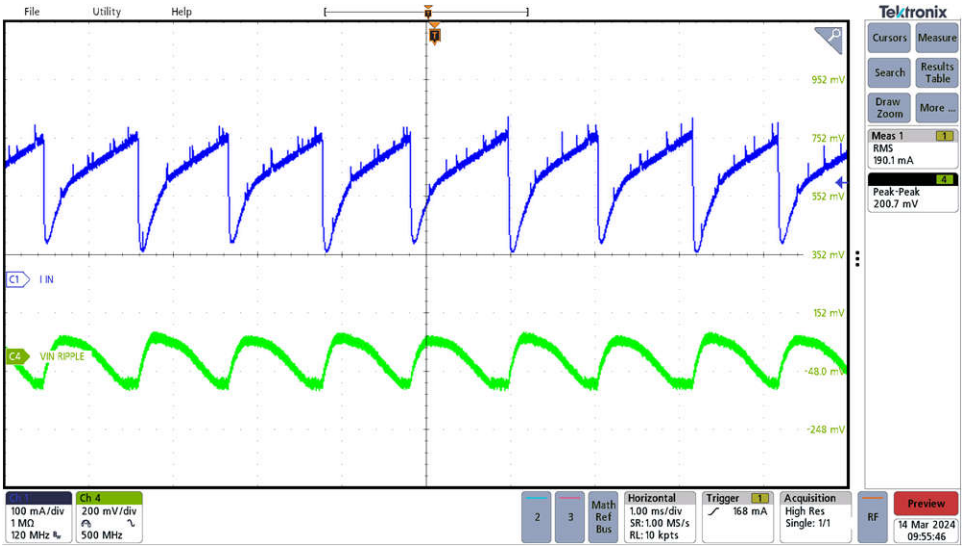

Figure 3-18. DRV8316C Input Current and Input Voltage Ripple During Operation

Figure 3-19 below shows the control signals from a single output phase of the MSPM0 (both INH and INL) as well as the current output from the SO pin during OTL operation.

The SOx pin on the DRV8316C outputs an analog voltage proportional to current flowing in the low side FETs multiplied by the gain setting (GCSA). The gain setting is adjustable between four different levels which can be set by the GAIN pin (in hardware device variant) or the GAIN bits (in SPI device variant). The current sense is implemented with the sense FET on each low-side FET of the DRV8316C device. This current information is fed to the internal I/V converter, which generates the CSA output voltage on the SOx pin based on the voltage on VREF pin and the Gain setting.

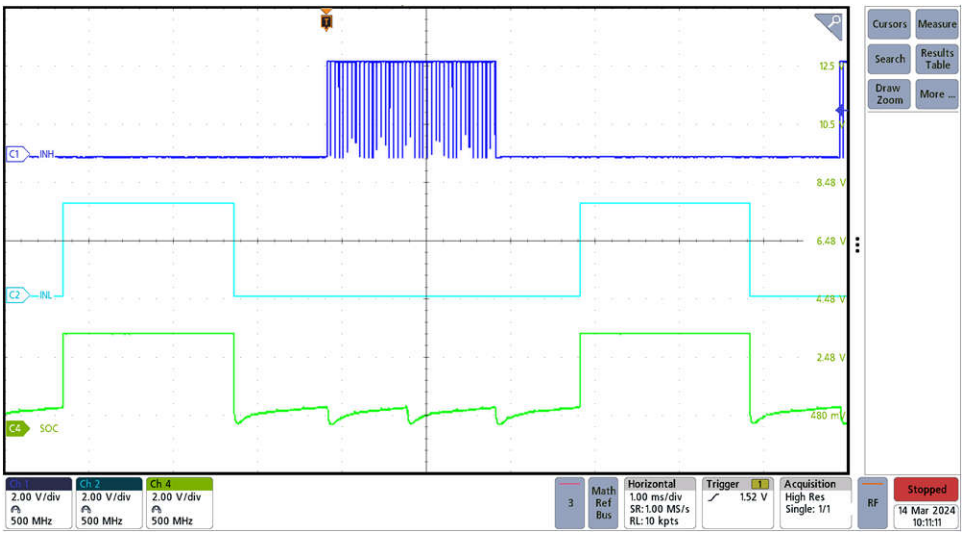

Figure 3-19. DRV8316C INH, INL, and SOx During Motor Operation (OTL)

Figure 3-20 shows the same outputs during the OTR operation. The INH and INL control signal along with the SOx are much shorter in duration with an increased frequency during the faster rotation of the damper motor in this scenario.

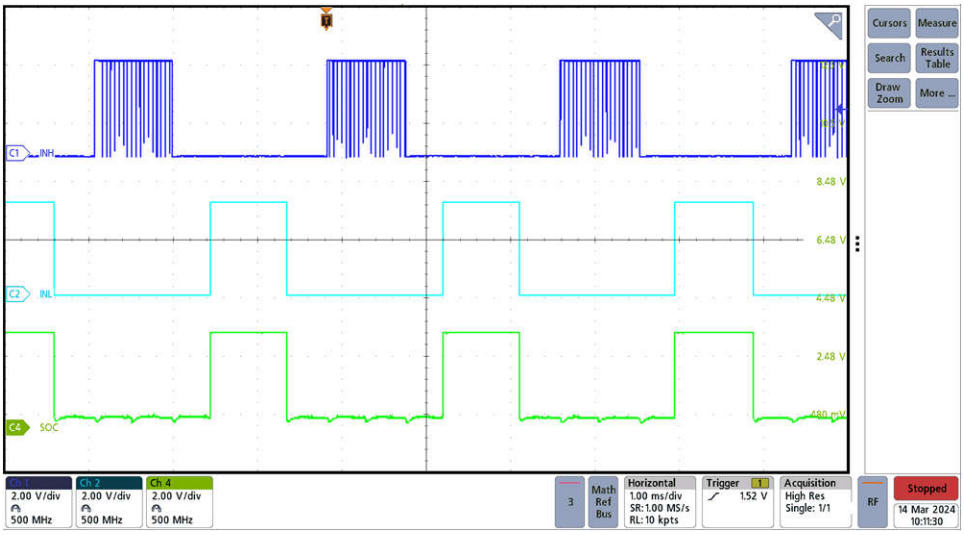

Figure 3-20. DRV8316C INH, INL, and SOx During Motor Operation (OTR)

DRV8428 Test Results

The DRV8428 testing is very similar to that of the BLDC damper motor, but instead leveraging a 24V**DC** bipolar stepper motor. A magnet is affixed to the back of the motor as shown below in Figure 3-21, and this is used for the position control loop in the case of 0V-10V or 4mA-20mA control, and simply as a position verification measure in the case the stepper motor is controlled by a temperature-based control loop.

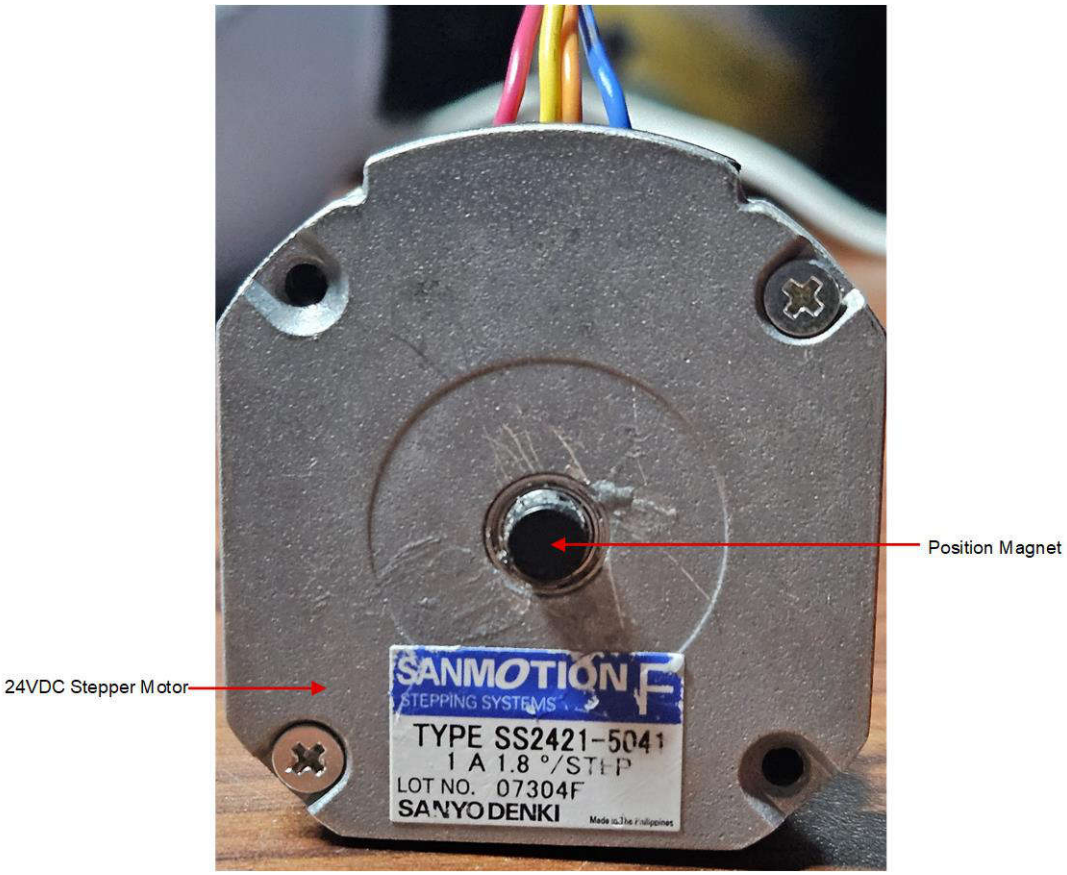

Figure 3-21. Stepper Motor Setup with Position Magnet

Figure 3-22 shows the load test results of the DRV8428 device driving a bipolar stepper motor in full stepping mode using a single-pin interface. In full-stepping mode, the full-bridge operates in either of two modes (forward or reverse mode) with a phase shift of 90° between the two windings. Figure 3-22 shows the STEP voltage, OUTA winding current, and OUT B winding.

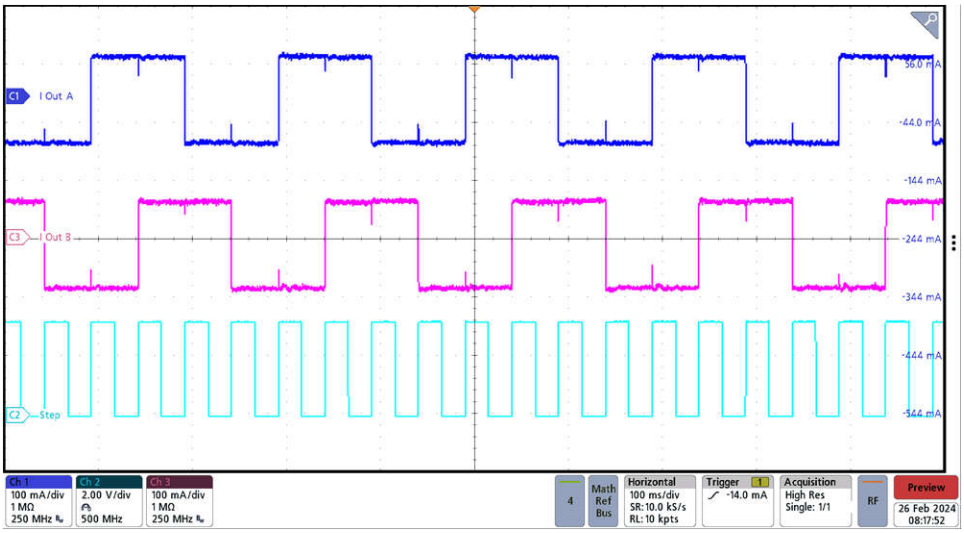

Figure 3-22. DRV8428 Phase Output and STEP Control Signal

DRV8428 Stepper Motor Drive efficiency:

To test the efficiency of the DRV8428, the input DC voltage to the device is swept from 15VDC to 24VDC while observing the current output of the power supply during operation. Current probes and voltage meters are used on each output from the DRV8316C during motor operation as well to acquire the RMS voltage and RMS current for each phase. The test is performed twice leveraging different decay mode settings to highlight the efficiency improvements that can be achieved.

Figure 3-23 below shows the current and voltage outputs for the DRV8428 during operation with the decay pin set to 0 through a GPIO from the MSPM0 (smart tune ripple control enabled). Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions. This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation. The V_{REF} pin is set to 1.5V from the MSPM0 DAC through firmware. The M0 pin of the DRV8428 is driven to 0, while the M1 pin is connected through a 330kΩ resistor to ground, setting the microstepping mode to full step (2-phase excitation) with 71% current.

The measured RMS voltage and current for AOUT 1 is 1.69V and 367.1mA RMS, and the BOUT 1 is 2.08V and 368.4mA respectively. The off-time for each phase is 9.86ms, and both outputs are 90 degrees phase shifted.

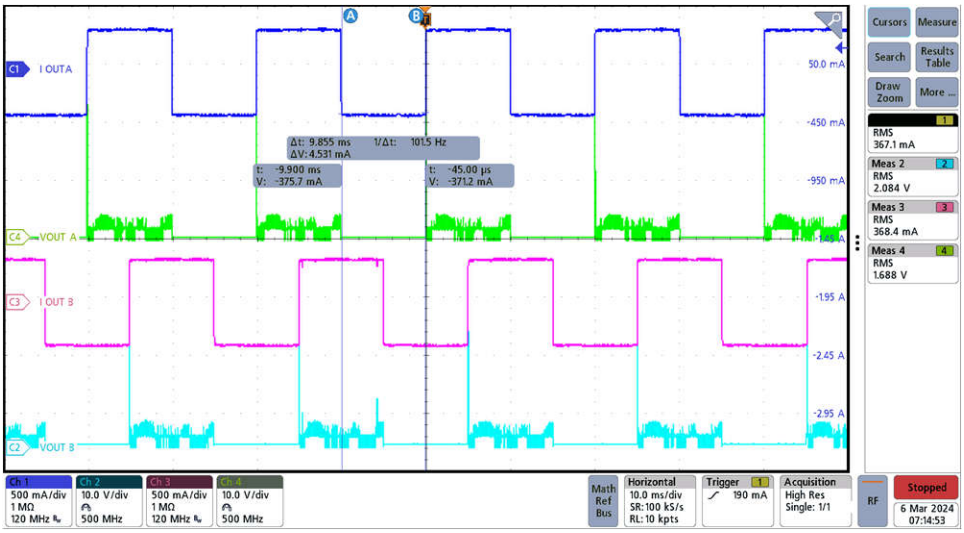

Figure 3-23. DRV8428 Output Current and Voltage with Smart Tune Ripple Control

Table 3-4 below shows the test results for the DRV8428 efficiency during operation with the decay mode set to smart tune ripple control. The input DC Power is gradually increased and the RMS output voltage/current is recorded to calculate the motor drive efficiency.

Table 3-4. Efficiency Over Input Power Data (Decay=0)

DC Input Power	Output RMS Current	Efficiency
1.85	721.10	71.93%
1.89	714.80	75.04%
1.93	715.00	74.39%
1.93	717.40	74.73%
2.01	717.30	72.98%
2.03	718.70	72.85%
2.05	719.90	72.98%
2.07	723.00	73.19%
2.10	725.10	73.61%

Table 3-4. Efficiency Over Input Power Data (Decay=0) (continued)

DC Input Power	Output RMS Current	Efficiency
2.11	726.20	74.78

Figure 3-24 below shows the resulting motor drive efficiency over the input DC power.

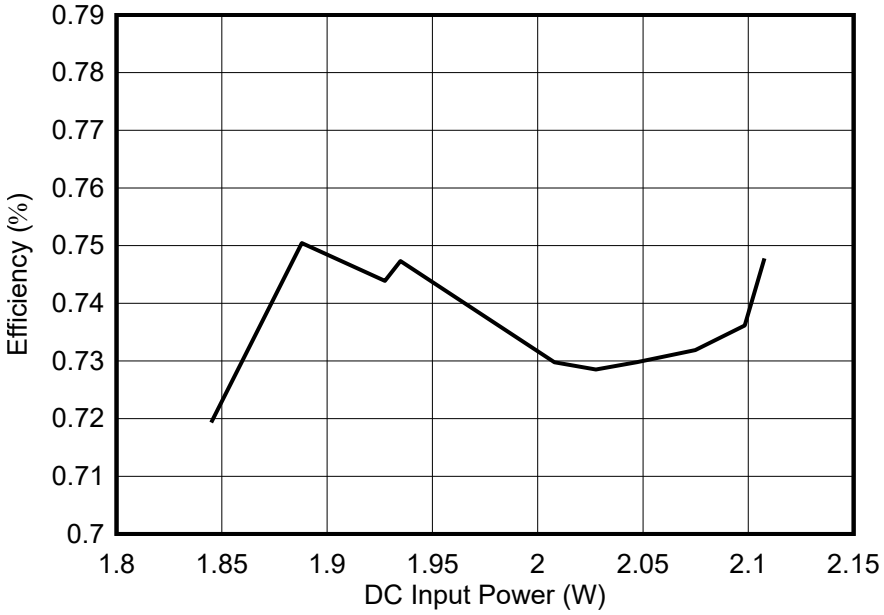

Figure 3-24. DRV8428 Efficiency Over Input Power

For the second test, the decay mode is set to HI-Z which leverages the smart tune dynamic decay mode. This decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly. The V_{REF} remains at 1.5V set with the MSPM0 DAC, utilizing full step 2 phase excitation with 71% current. Figure 3-25 below shows the output of both AOUT 1 and BOUT 1during motor operation. AOUT1 has an RMS voltage of 2.36V and an RMS current output of 317.4mA. For BOUT 1 the RMS voltage is 2.73V and RMS current is 320.1mA. The off-time in this mode is approximately 7.66ms.

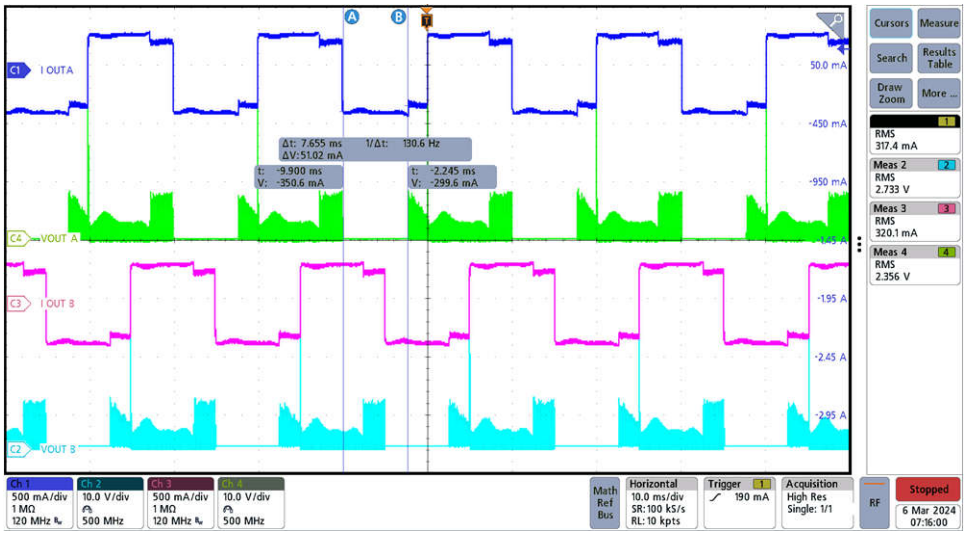

Figure 3-25. DRV8428 Output Current and Voltage With Smart Tune Dynamic Decay

Table 3-5 below shows the recorded data for each incremental input voltage value along with the calculated efficiency for each.

Table 3-5. Efficiency Over Input Power Data (Decay = HI-Z)

DC Input Power (W)	Total Output RMS Current (mA)	Efficiency (%)
1.54	671.80	77.05%
1.59	671.50	75.54%
1.59	667.30	79.74%
1.60	666.90	83.52%
1.61	660.20	84.14%
1.62	656.20	88.61%
1.62	650.40	91.88%
1.63	646.10	94.34%
1.65	639.90	95.42%
1.68	636.80	96.96%

Figure 3-26 below shows the efficiency and the total phase output current plots across the input power range for the DRV8428 with smart tune dynamic decay enabled. In this test, the efficiency numbers are considerably better and proportional to the input supply voltage, peaking at approximately 97% at 24VDC input voltage.

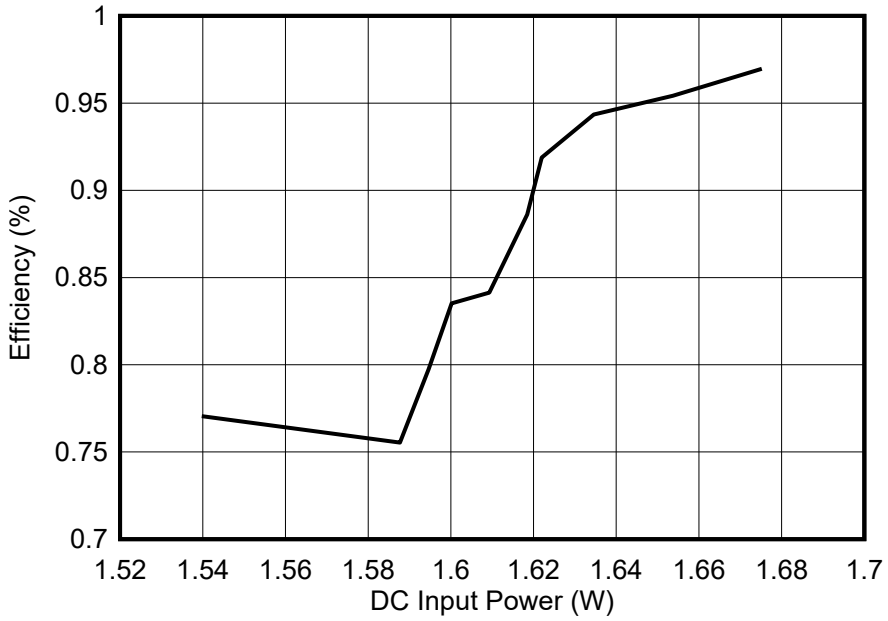

Figure 3-26. DRV8428 Efficiency over Input Power

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010950.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010950 .

4.2 Tools and Software

Tools

WEBENCH Power Designer	Creates customized power supply circuits based on your requirements. The environment gives you end-to-end power supply design capabilities that save you time during all phases of the design process.
TPS16410 Design Calculator	The design calculator allows customer to size the external peripheral components while designing with TPS1641 eFuse.

Software

MSPM0 Software Development	Accelerate time to market with optimized software drivers, hundreds of code examples, support for developer-friendly operating systems, and more.

4.3 Documentation Support

1. Texas Instruments, TPS1641 2.7-V to 40-V 152-mΩ 1.8-A eFuse with output power limiting data sheet
2. Texas Instruments, LMR38020 SIMPLE SWITCHER®power converter 4.2-V to 80-V, 2-A, synchronous buck with 40-µA IQ data sheet
3. Texas Instruments, TPS62932 3.8-V to 30-V input, 2-A, 200-kHz to 2.2-MHz, low-IQ synchronous buck converter in SOT-583 package data sheet
4. Texas Instruments, MSPM0G3507 80MHz Arm M0+ MCU, 128KB Flash, 32KB SRAM, 2×12bit 4Msps ADC, DAC, 3×COMP, 3×op-amp, CAN-FD, MATHACL data sheet
5. Texas Instruments, DRV8316C 40-V max 8-A peak 3-phase motor driver with integrated current sensing, FETs, and enhanced CSA specs data sheet
6. Texas Instruments, DRV8428 35-V, 1-A bipolar stepper motor driver with integrated current sensing & 1/256 microstepping data sheet
7. Texas Instruments, ISO1212 Dual-channel Isolated 24-V to 60-V digital input receiver for digital input modules data sheet
8. Texas Instruments, TMAG5273 Low-power linear 3D Hall-effect sensor with I²C interface data sheet
9. Texas Instruments, TCAN334 3.3-V CAN Transceivers data sheet
10. Texas Instruments, TLV9002 Dual, 5.5-V, 1-MHz, RRIO operational amplifier for cost-optimized applications data sheet

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

BRIAN DEMPSEY is a systems designer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Brian brings to this role his extensive experience in HVAC system electronics, along with his experience with mixed signal systems. Brian earned his bachelor of science in electrical engineering (BSEE) from Texas A&M University in College Station, TX.

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2024	*	Initial Release

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