Clock and Timing Applications

Texas Instruments

Wired Communications / Networking
Wireless Communications
Industrial
Automotive
Consumer
Computing

ti.com/clocks

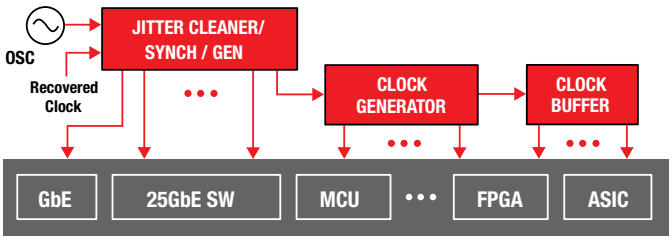
2016

Clock and Timing for Communications

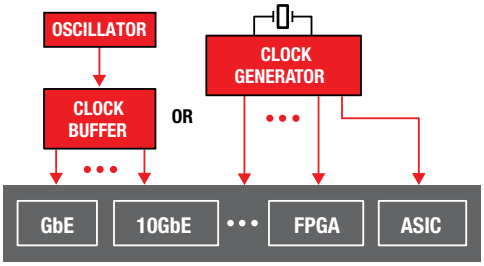
Wired and optical communications / networking / server and storage

TI's broad portfolio of low-jitter clock generators and buffers allows system designers to meet the most stringent data communication requirements while reducing complexity by eliminating the need for multiple low-jitter oscillators.

Wired/Optical Communications



Networking



Device	Description	Input: Output	Input Type	Output Type	Max Frequency (MHz)	Jitter	Programmability	Normalized PLL Phase Noise (dBc/Hz)
Featured Oscillators								
LMK61E2 ● ●	Ultra low jitter differential oscillator, Fully programmable,+/-50ppm,7mmx5mm	0:1	—	LVPECL, LVDS, HCSL	1000	0.1ps RMS**	I2C, EEPROM	—
LMK61E2156M25 ● ●	Ultra low jitter differential oscillator,+/-50ppm,7mmx5mm	0:1	—	LVPECL	156.25	0.1ps RMS**	Fixed freq	—
Featured Clock Generators								
LMK03328 ●	Ultra low jitter-dual high performance PLL based, with integrated EEPROM	2:8	Crystal, single ended, differential	CML, LVPECL, LVDS, HCSL, LVCMOS	1000	0.1ps RMS**	EEPROM, pin, I2C	–231
CDCM6208 ● ●	Any frequency, 2 inputs, 8 outputs with integer and fractional dividers	2:8	Crystal, single ended, differential	CML, LVPECL, LVDS, HCSL, LVCMOS	800	0.265 ps RMS***	SPI, I2C, pin	–224
LMK03806 ● ●	1 input, 14 outputs, ultra-low jitter with integer dividers	1:14	Crystal or external clock	LVDS, LVPECL, LVCMOS	1300	0.15 ps RMS**	µWire (SPI)	–227
CDCE62005 ● ●	3 inputs, 5 outputs with integrated dual VCOs	3:5	Crystal, single ended, differential	LVPECL, LVDS, LVCMOS	1500	0.35 ps RMS***	SPI, EEPROM	–218
Featured Clock Jitter Cleaners								
LMK0482x ●	Dual PLLs, lowest phase noise, JESD204B compliant, frequency holdover mode, programmable analog and digital delays	3:14	CLKin (PLL1): single ended, differential; OSCin (PLL2): can use pullable crystal	LVPECL, LVDS, HSDS, LCPECL	3100	88 fs	SPI	–227
LMK0480x ●	Dual PLLs, ultra-low phase noise, 2 selectable inputs, 14 outputs, frequency holdover mode, programmable analog and digital delays	2:14	CLKin (PLL1): single ended, differential; OSCin (PLL2): can use pullable crystal	LVPECL, LVDS, LVCMOS	3072	100 fs	SPI	–227
LMK04816 ● ●	Dual PLLs, ultra-low phase noise, 3 selectable inputs, 12 outputs, frequency holdover mode, programmable analog and digital delays	3:12	CLKin (PLL1): single ended, differential; OSCin (PLL2): can use pullable crystal	LVPECL, LVDS, LVCMOS	2600	100 fs	SPI	–227
LMK04906 ●	Dual PLLs, ultra-low phase noise, 3 selectable inputs, 6 outputs, frequency holdover mode, programmable analog and digital delays	3:6	CLKin (PLL1): single ended, differential; OSCin (PLL2): can use pullable crystal	LVPECL, LVDS, LVCMOS	2600	100 fs	SPI	–227
CDCM7005 ●	Low phase noise with frequency holdover	2:5	Single ended, differential	LVPECL, LVCMOS	1500	100 fs	SPI	–218

*** Typical Integrated RMS Jitter as measured from 12 kHz to 20 MHz *** Typical Integrated RMS Jitter as measured from 10 kHz to 20 MHz*

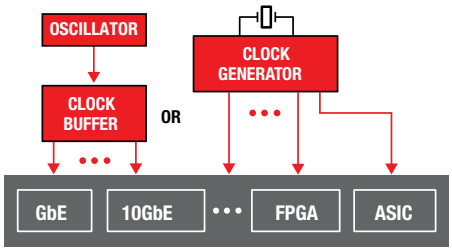
● *Wired* ● *Wireless*

Clock and Timing for Communications

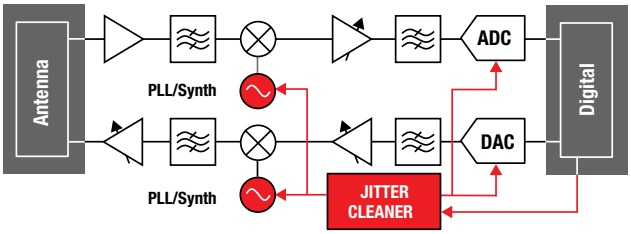
Wireless communications

With industry-leading performance, TI's clock jitter cleaners, clock generators, buffers and RF frequency synthesizers allow designers to maximize the quality and robustness of wireless links.

Wireless BBU



Wireless RRU



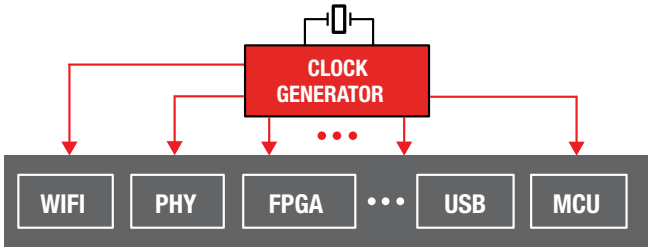
Device	Description	Input:Output	Input Type	Output Type	Max Frequency (MHz)	Jitter	Programmability	Normalized PLL Phase Noise (dBc/Hz)
Featured Clock Distributors / Fanout Buffers								
LMK0033x	Industry's lowest jitter PCIe 3.0 compliant 1-to-4/8 HSCL fanout buffers	1:4 (LMK00334) 1:8 (LMK00338)	LVPECL, LVDS, CML, SSTL, HSTL, HCSL or single ended	HSCL	400	30 fs, RMS additive	—	—
LMK0101	High performance clock buffer, divider, and distributor	2:10	LVPECL	LVPECL	1600	30 fs, RMS additive (100 Hz to 20 MHz)	SPI	—
LMK0030x	Ultra-low jitter, configurable differential buffer/level translators, crystal oscillator	3:4 (LMK00304) 3:6 (LMK00306) 3:8 (LMK00308) 3:10 (LMK00301)	Crystal, single ended, differential	LVPECL, LVDS, HCSL, 1 LVCMOS	3100	64 fs, RMS additive	Pin	—
CDCLVPxxxx	LVPECL buffers	from 1:2 to 2:16	Differential	LVPECL	2000 / 3500	68 fs, RMS additive	—	—
CDCLVDxxxx	LVDS buffers	from 2:4 to 2:16	Differential	LVDS	800 / 1100	300 fs, RMS additive	—	—
CDCLVCxxxx	LVCMOS buffers	from 1:2 to 1:12	LVCMOS	LVCMOS	250	100 fs, RMS additive	—	—
LMK0010x	Ultra-low jitter, configurable LVCMOS buffer/level translators, crystal oscillator	3:5 (LMK00105) 3:10 (LMK00101)	Crystal, single ended, differential	LVCMOS	200	30 fs, RMS additive	Pin	—
CDCM180x	Programmable dividers	1:2 (CDCM1802) 1:4 (CDCM1804)	Single ended, differential	LVPECL, LVCMOS	800 LVPECL 200 LVCMOS	150 fs, RMS additive	Pin	—
LMK01801	Dual clock divider buffers, programmable analog and digital delays	from 2:14 to 2:20	Single ended, differential	LVPECL, LVDS, LVCMOS	3100	50 fs, RMS additive	Pin, µWire (SPI)	—
Featured RF PLLs and Synthesizers								
LMX2531	Low power, low spur, frac-N synthesizer with integrated VCO	1:1	Single ended	Sinewave	553 to 3132	0.27 ps	SPI	–212
LMX2541	Low noise, excellent spurs, fractional-N, integrated VCO, optional external VCO	1:1	Single ended, differential	Sinewave	32 to 4000 (integrated VCO), 6000 (ext VCO)	0.12 ps	SPI	–225
LMX2581	Ultra-low noise, wideband, fractional-N synthesizer, integrated wideband VCOs	1:2	Single ended	Sinewave	50 to 3760	0.12 ps	SPI	–229
LMX248x	Ultra-low power, wideband, dual fractional-N PLLs, available auto grade versions	1:2	Single ended	Sinewave	50 to 7500	0.27 ps	SPI	–210

Wired *Wireless*

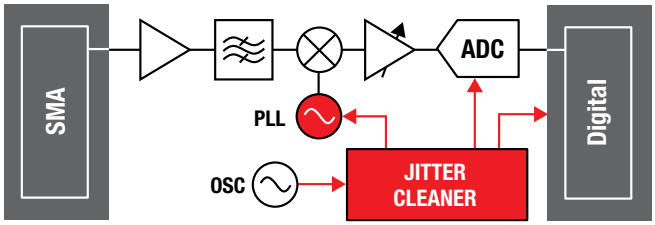
Clock and Timing for Industrial

TI's clock ICs can help improve the reliability of a system by consolidating multiple crystals and oscillators with a simple low-power clocking solution. In industrial applications, such as test and measurement and medical, where performance is critical, TI's low-jitter clocks and RF PLL and synthesizers let designers push the limits of performance to deliver differentiated solutions.

Industrial (General Purposes)



Test and Measurement/Medical Imaging



Device	Description	Input:Output	Input Type	Output Type	Max Frequency (MHz)	Jitter	Programmability
Featured Oscillators							
LMK61E2	Ultra low jitter differential oscillator, Fully programmable,+/-50ppm,7mmx5mm	0:1	—	LVPECL, LVDS, HCSL	1GHz	0.1ps RMS**	I²C,EEPROM
LMK61E2 156M25	Ultra low jitter differential oscillator,+/-50ppm,7mmx5mm	0:1	—	LVPECL	156.25	0.1ps RMS**	Fixed frequency
Featured Clock Generators							
LMK03328	Ultra low jitter,, dual high performance PLL based, with integrated EEPROM	2:8	Crystal, single ended, differential	CML, LVPECL, LVDS, HCSL, LVCMOS	1GHz	0.100ps RMS**	–231
CDCM6208	Any frequency, 2 inputs, 8 outputs with integer and fractional dividers	2:8	Crystal, single ended, differential	CML, LVPECL, LVDS, HCSL, LVCMOS	800	0.265 ps RMS***	SPI, I2C, pin
CDCM6100x	1 input, 1-4 outputs, crystal oscillator replacement	1:1 (CDCM61001) 1:2 (CDCM61002) 1:4 (CDCM61004)	Crystal, single ended	LVPECL, LVDS, LVCMOS	683.26	0.5 ps RMS***	Pin
CDCM9102	Low jitter, 2-channel, 100 MHz PCIe Gen-1/-2/-3	1:2	Crystal	LVPECL, LVDS, LVCMOS	100	0.5 ps RMS**	Pin
CDCE(L)913/ CDCE(L)949	1/4 PLL, integrated VCXO, spread spectrum clocking, 1.8/2.5/3.3V outputs	1:3* 1:9*	Crystal, single ended, option for on-chip VCXO	LVCMOS	230	60 ps peak-to-peak period	I2C, EEPROM, pin
CDCE706	3 PLLs, spread spectrum clocking, ultra flexible output switching matrix	1:6	Crystal, single ended, differential	LVCMOS	300	60 ps peak-to-peak period	SMBus, EEPROM
Featured Clock Jitter Cleaners							
LMK0480x	Dual PLLs, ultra-low phase noise, 2 selectable inputs, frequency holdover mode, programming delay	2:12+2	CLKin (PLL1): single ended, differential; OSCin (PLL2): can use crystal	LVPECL, LVDS, LVCMOS	3072	100	SPI
LMK0482x	Dual PLLs, lowest phase noise, JESD204B compliant, frequency holdover mode, programming delay	3:14+1	CLKin (PLL1): single ended, differential; OSCin (PLL2): can use crystal	LVPECL, LVDS, HSDS, LCPECL	3100	88	SPI

*** As measured from 12 kHz to 20 MHz **** As measured from 10 kHz to 20 MHz*

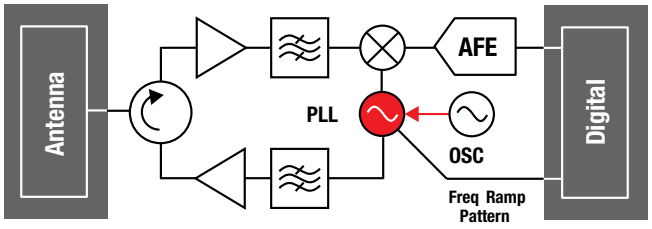
Clock and Timing for Industrial

Device	Description	Input:Output	Input Type	Output Type	Max Frequency (MHz)	Jitter	Programmability	Normalized PLL Phase Noise (dBc/Hz)
Featured Clock Distributors / Fanout Buffers								
LMK00725	Low jitter, low skew, 2:5, differential-to-3.3V LVPECL fanout buffer	2:5	LVPECL, LVDS, HCSL, SSTL, LVHSTL or single ended	LVPECL	650	43 fs typ at 312.5 MHz (10 k to 20 MHz)	—	–158 dBc/Hz at 312.5 MHz >1 MHz offset
LMK0030x	Ultra-low jitter, configurable differential buffer/level translators, crystal oscillator	3:4 (LMK00304) 3:6 (LMK00306) 3:8 (LMK00308) 3:10 (LMK00301)	Crystal, single ended, differential	LVPECL, LVDS, HCSL + 1 LVCMOS	3100	64 fs, RMS additive	Pin	—
CDCLVPxxxx	LVPECL buffers	from 1:2 to 2:16	Differential	LVPECL	2000 / 3500	68 fs, RMS additive	—	—
CDCLVDxxxx	LVDS buffers	from 2:4 to 2:16	Differential	LVDS	800 / 1100	300 fs, RMS additive	—	—
CDCLVCxxxx	LVCMOS buffers	from 1:2 to 1:12	LVCMOS	LVCMOS	250	100 fs, RMS additive	—	—
CDCM180x	Programmable dividers	1:2 (CDCM1802) 1:4 (CDCM1804)	Differential	LVPECL, LVCMOS	800 LVPECL 200 LVCMOS	150 fs, RMS additive	Pin	—
LMK01801	Dual clock divider buffers, programmable analog and digital delays	from 2:14 to 2:20	Single ended, Differential	LVPECL, LVDS, LVCMOS	3100	50 fs, RMS additive	Pin, µWire (SPI)	—
CDCVF2505	3.3V zero delay buffer	1:4	Single ended	LVCMOS	200	150 ps peak-to-peak cycle-to-cycle	—	—
CDCVF2510A	3.3V zero delay buffer	1:10	Single ended	LVCMOS	175	125 ps peak-to-peak cycle-to-cycle	—	—
CDCVF85x	2.5V zero delay buffers	1:4 (CDCVF855) 1:10 (CDCVF857)	Differential	Differential	220	30 ps peak-peak period	—	—
CDCU877x	1.8V zero delay buffers	1:10	Differential	Differential	340	30 ps peak-to-peak period	—	—
CDCUA877	1.8V zero delay buffer	1:10	Differential	Differential	410	30 ps peak-to-peak period	—	—
Featured RF PLLs and Synthesizers								
LMX2492	Low noise, fractional-N PLL with ramp generation	1:1	Single ended, differential	Sinewave	14000	0.15 ps	SPI	–227
LMX2522	Ultra-low power, dual RF synthesizer, integrated GPS/RF VCOs, IF PLL	1:1	Single ended	Sinewave	1619 to 1650, 1355 & 440	0.4 ps	SPI	–210
LMX2531	Low power, low spur, fractional-N synthesizer with integrated VCO	1:1	Single ended	Sinewave	553 to 3132	0.27 ps	SPI	–212
LMX2541	Low noise, excellent spurs, fractional-N, integrated VCO, optional external VCO	1:1	Single ended, differential	Sinewave	32 to 4000 (integrated VCO), 6000 (external VCO)	0.12 ps	SPI	–225
LMX2581	Ultra-low noise, wideband, fractional-N synthesizer, integrated wideband VCOs	1:2	Single ended	Sinewave	50 to 3760	0.12 ps	SPI	–229
LMX248x	Ultra-low power, wideband, dual fractional-N PLLs, available auto grade versions	1:2	Single ended	Sinewave	50 to 7500	0.27 ps	SPI	–216
LMX243x	Ultra-low power, low noise, dual integer PLLs	1:2	Single ended	Sinewave	250 to 5000	0.4 ps	SPI	–218

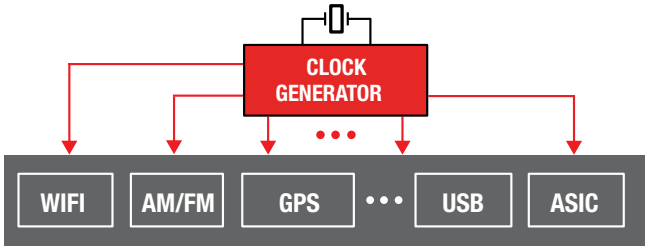
Clock and Timing for Automotive

With a range of automotive-grade clocks and RF PLLs, TI offers solutions for both infotainment and advanced driver assist systems (ADAS). In ADAS applications, TI's high-performance PLLs can significantly enhance the range and accuracy of radar systems while simplifying the design by integrating critical functions such as ramp generation. In infotainment applications, TI's clock generators and buffers help to consolidate multiple crystals and oscillators with a simple low-power clocking solution.

Automotive Radar



Automotive Infotainment



Device	Description	Input:Output	Input Type	Output Type	Max Frequency (MHz)	Jitter	Programmability
CDCE(L)913-Q1	1 PLL, integrated VCXO, spread spectrum clocking, 1.8/2.5/3.3V outputs	1:3*	Crystal, single ended, option for on-chip VCXO	LVCMOS	230	60 ps peak-to-peak period	I2C, EEPROM, pin
CDCE949-Q1	4 PLLs, integrated VCXO, spread spectrum clocking, 1.8/2.5/3.3V outputs	1:9	Crystal, single ended, option for on-chip VCXO	LVCMOS	230	70 ps peak-to-peak period	I2C, EEPROM, pin
CDCE(L)937-Q1	3 PLLs, integrated VCXO, spread spectrum clocking, 1.8/2.5/3.3V outputs	1:7	Crystal, single ended	LVCMOS	230	70 ps peak-to-peak period	I2C, EEPROM, pin
CDCS503-Q1	Spread spectrum clock generator	1:1	Crystal, single ended LVCMOS	LVCMOS	108	110 ps cycle-to-cycle	Pin
CDCVF2505-Q1	3.3V zero delay buffer with input clock detector and integrated series output resistors	1:4	Single ended	LVCMOS	200	150 ps cycle-to-cycle	—
LMX2485Q-Q1	Ultra-low power, wideband, dual fractional-N PLLs	1:2	Single ended	Sinewave	3100	0.27 ps	SPI
LMX2492-Q1	Low noise, fractional-N PLL with ramp generation	1:1	Single ended, differential	Sinewave	14000	0.15 ps	SPI

** 2 PLL / 5 output and 3 PLL / 7 output also available*
*** As measured from 12 kHz to 20 MHz*

Clock and Timing for Consumer and Computing

Consumer

Device	Description	Input:Output	Input Type	Output Type	Max Frequency (MHz)	Jitter	Programmability
Featured Clock Generators							
CDCM9102	Low jitter, 2 channel, 100 MHz PCIe Gen-1/-2/-3	1:2	Crystal	LVPECL, LVDS, LVCMOS	100	0.5 ps RMS**	Pin
CDCE(L)913	1 PLL, integrated VCXO, spread spectrum clocking, 1.8/2.5/3.3V outputs	1:3*	Crystal, single ended, option for on-chip VCXO	LVCMOS	230	60 ps peak-to-peak period	I2C, EEPROM, pin
CDCE(L)949	4 PLLs, integrated VCXO, spread spectrum clocking, 1.8/2.5/3.3V outputs	1:9*	Crystal, single ended, option for on-chip VCXO	LVCMOS	230	60 ps peak-to-peak period	I2C, EEPROM, pin
CDCE906	3 PLLs, spread spectrum clocking, ultra flexible output switching matrix	1:6	Crystal, single ended, differential	LVCMOS	167	90 ps peak-to-peak period	SMBus, EEPROM
CDCS50x	Spread spectrum clock generators	1:1	Crystal, single ended LVCMOS	LVCMOS	108	110 ps cycle-to-cycle	Pin
Featured Clock Distributors / Fanout Buffers							
CDCVF2505	3.3V zero delay buffer	1:4	Single ended	LVCMOS	200	150 ps peak-to-peak cycle-to-cycle	—
CDCVF2510A	3.3V zero delay buffer	1:10	Single ended	LVCMOS	175	125 ps peak-to-peak cycle-to-cycle	—
CDCVF85x	2.5V zero delay buffers	1:4 (CDCVF855) 1:10 (CDCVF857)	Differential	Differential	220	30 ps peak-to-peak period	—
CDCVF85x	1.8V zero delay buffers	1:10	Differential	Differential	340	30 ps peak-to-peak period	—
CDCUA877	1.8V zero delay buffer	1:10	Differential	Differential	410	30 ps peak-to-peak period	—

** 2 PLL / 5 output and 3 PLL / 7 output also available*
*** As measured from 12 kHz to 20 MHz*

Computing

Device	Description	Input:Output	Input Type	Output Type	Max Frequency (MHz)	Jitter	Memory Generation
CDCVF2505	3.3V zero delay buffer	1:4	Single ended	LVCMOS	200	150 ps peak-to-peak cycle-to-cycle	SDR
CDCVF2510A	3.3V zero delay buffer	1:10	Single ended	LVCMOS	175	125 ps peak-to-peak cycle-to-cycle	SDR
CDCVF85x	2.5V zero delay buffers	1:4 (CDCVF855) 1:10 (CDCVF857)	Differential	Differential	220	30 ps peak-to-peak period	DDR1
CDCU877x	1.8V zero delay buffers	1:10	Differential	Differential	340	30 ps peak-to-peak period	DDR2
CDCUA877	1.8V zero delay buffer	1:10	Differential	Differential	410	30 ps peak-to-peak period	DDR2

SN74SSTUB3286x	1.8V DDR2 registers	1:2 25-bit 1:2 28-bit	Single ended	SSTL	410	N/A	DDR2
SN74SSQEC32882	1.5V DDR3 register	1:2 28-bit	Single ended	SSTL	945	N/A	DDR3
CAB4A	1.2V DDR4 register	1:2 32-bit	Single ended	SSTL	1200	N/A	DDR4

Accelerate time-to-market with easy-to-use clock and timing solutions

Texas Instruments is the world's #1 supplier of analog semiconductor ICs, and offers a complete clock and timing IC portfolio – from clock oscillators, clock buffers and generators to jitter attenuators and RF PLLs/synthesizers – targeting a broad spectrum of end-equipments. TI's portfolio is supported by a number of innovative, robust online tools that ease design and reduce time-to-market.

Clock and timing solutions from TI offer:

- Flexible frequency planning
- Universal input and output formats
- Best-in-class jitter and phase noise performance
- Low power consumption
- In-system programming
- Sophisticated clock design tools that automate selection, configuration and simulation of TI clocking devices

Addressing broad applications:

- Wired communications / networking
- Wireless communications
- Industrial
- Automotive
- Consumer
- Computing

Design resources and references

WEBENCH® Design Center

WEBENCH® Clock Architect

The industry's only timing tool that recommends a system clock tree solution with device selection from an exhaustive database, with all the necessary features to enable system designers to quickly achieve a complete, optimized clock tree solution.

- PLL loop filter design capability
- Simulate phase noise of the output clocks
- Cascade noise from a device upstream in the clock tree solution to a downstream device
- Generate a configuration file for each of the devices in the recommended solution which can be used to program the individual device EVMs

ti.com/clockarchitect

CodeLoader

Software for device register programming
ti.com/codeloader

E2E Clock and Timing Forum

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TI E2E™ Community

Get more information on TI's entire family of clocking products at **ti.com/clocks.**

Texas Instruments

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