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Contents

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Introduction

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Reducing distortion from CMOS analog switches

By John Caldwell
Analog Applications Engineer

CMOS analog switches have become ubiquitous on the inputs and outputs of many electronic systems. They may be used to select between multiple input channels on data acquisition systems or to disable outputs during power-up or power-down events. In fact, analog switches have become so common that their operation is often taken for granted. But analog designers should be aware that semiconductor switches exhibit behavior quite unlike their mechanical cousins. For example, the resistance of a CMOS switch in the closed position, referred to as the on-resistance or R_{ON}, changes depending on the input voltage. This behavior is usually undesirable and can significantly distort the input signal in some applications.

To understand why CMOS switches behave in this manner, it is necessary to understand their basic construction and operation. A typical solid-state analog switch consists of two MOSFETs of opposite channel polarity and configured as a transmission gate as shown in Figure 1. The control voltages (C and $\overline{C}$) at the FET gates are dc voltages of opposite polarity. The switch is closed when the gate of the NMOS transistor is high and the gate of the PMOS transistor is low. Positive input voltages drive the V_{GS} of the PMOS more negative, decreasing the PMOS on-resistance. Therefore, the PMOS is the dominant current pathway for positive voltages. Conversely, negative voltages applied to the input terminal increase the gate-to-source voltage, V_{GS}, of the NMOS FET, decreasing its on-resistance and allowing current to flow through the NMOS pathway.

The basic switch architecture allows for both positive and negative voltages to be passed, but also causes the overall resistance of the switch to change with the input signal. Figure 2 is a plot of the on-resistance of the TS12A12511 switch versus the signal voltage range[1]. An R_{ON} "flatness" parameter may be included in the datasheet specification table to quantify the maximum deviation in the switch on-resistance over the signal range. For example, the R_{ON} flatness specification for the TS12A12511 is 1.6 Ω (typical).

A basic analog output circuit incorporating a CMOS switch is illustrated in Figure 3. Here the switch is used to disconnect the load from the output of an operational amplifier (op amp). Such applications of CMOS switches are very common in audio applications to suppress clicks and pops during the power-up or down of preceding circuitry.

Figure 1. CMOS transmission gate consisting of NMOS and PMOS transistors

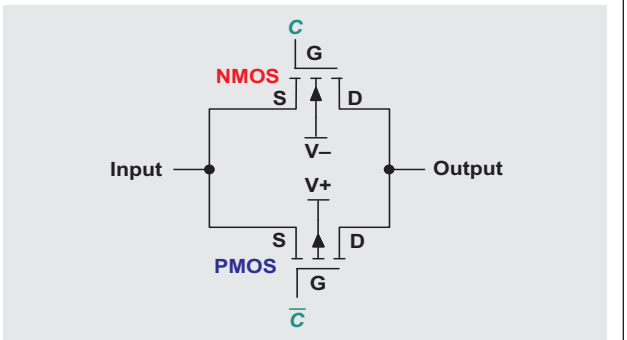


Figure 2. On-resistance variation of the TS12A12511 and example of R_{ON} flatness

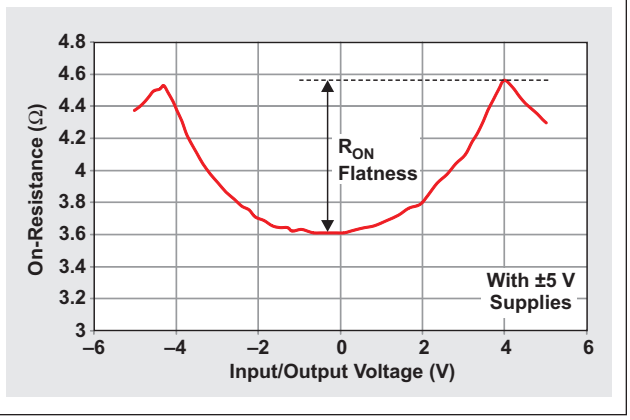
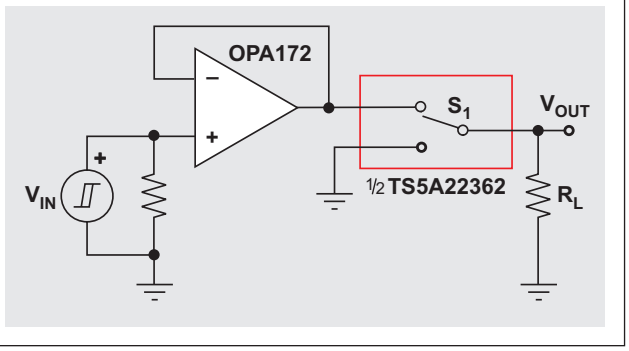


Figure 3. Signal distortion in a typical CMOS switch application



The switch on-resistance forms a voltage divider with the load resistance R_L and the output voltage is:

$$V_{OUT} = V_{IN}\frac{R_L}{R_{ON(S1)} + R_L} = \frac{V_{IN}}{\frac{R_{ON(S1)}}{R_L} + 1} \quad (1)$$

In reality, the value of $R_{ON(S1)}$ is not a constant, but is a function of V_{IN}. As an example, assume that $R_{ON(S1)}$ is a linear function of the input voltage:

$$R_{ON(S1)}(V_{IN}) = \Delta R \times V_{IN} + R_O \quad (2)$$

In Equation 2, ΔR represents the change in switch on-resistance with input voltage and R_O is the resistance for an input signal of 0 V. In reality, the relationship between R_{ON} and V_{IN} is more complex, but assuming a linear relationship simplifies the analysis while still revealing the distortion mechanism.

Inserting Equation 2 for on-resistance back into Equation 1 for output voltage gives a new equation:

$$V_{OUT} = \frac{V_{IN}}{\frac{\Delta R}{R_L}V_{IN} + \frac{R_O}{R_L} + 1} \quad (3)$$

For simplicity, a generic form of Equation 3 can be generated by substituting the constants A and B for terms in the above equation:

$$\text{Let } x = V_{IN},\ A = \frac{\Delta R}{R_L} \text{ and } B = \frac{R_0}{R_L} + 1,$$

$$\text{then } V_{OUT} = f(x) = \frac{x}{Ax + B} \quad (4)$$

To show the introduction of distortion, this more generic equation can be written instead as its equivalent Maclaurin series (shown here to 5 terms):

$$f(x) = \frac{1}{B}x - \frac{A}{B^2}x^2 + \frac{A^2}{B^3}x^3 - \frac{A^3}{B^4}x^4 + \frac{A^4}{B^5}x^5 \ldots \quad (5)$$

Now a sine wave is inserted as the input signal with $x = \sin(2\pi ft)$:

$$f[\sin(2\pi ft)] = \frac{\sin(2\pi ft)}{B} - \frac{A}{B^2}\sin(2\pi ft)^2 + \frac{A^2}{B^3}\sin(2\pi ft)^3 - \frac{A^3}{B^4}\sin(2\pi ft)^4 + \frac{A^4}{B^5}\sin(2\pi ft)^5 \ldots \quad (6)$$

Using the power reduction rules for trigonometric functions and simplifying the equation, the individual terms for each harmonic can be grouped together as shown in Table 1. The Maclaurin series was abbreviated to five terms so the amplitude for the harmonics are approximations.

Although the on-resistance of a CMOS switch is almost never linearly related to the input voltage, this example provides some useful rules for reducing the distortion from analog switches. Looking at the equations for the individual harmonics, a reduction in distortion requires that either the value of A must be very small, or B must be very large. The latter option is very un-attractive in most applications. Recalling the equation for B:

Table 1: Approximate amplitude of fundamental and distortion harmonics for the example calculation

Fundamental	$\left(\frac{1}{B} + \frac{3A^2}{4B^3} + \frac{5A^4}{8B^5}\right)\sin(2\pi ft)$
2nd Harmonic	$\left(\frac{A}{2B^2} + \frac{A^3}{2B^4}\right)\sin\left(4\pi f + \frac{\pi}{2}\right)$
3rd Harmonic	$\left(\frac{A^2}{4B^3} + \frac{5A^4}{16B^5}\right)\sin(6\pi f + \pi)$
4th Harmonic	$\left(\frac{A^3}{8B^4}\right)\sin\left(8\pi f + \frac{3\pi}{2}\right)$
5th Harmonic	$\frac{A^4}{16B^5}\sin(10\pi f)$

$$B = \frac{R_0}{R_L} + 1 \quad (7)$$

For B to be large, R_O must be much greater than R_L. Now the majority of the signal voltage is dropped across the switch, rather than the load resistor. The net effect is that the output signal is attenuated.

In most systems, it is more practical to reduce the value of A:

$$A = \frac{\Delta R}{R_L} \quad (8)$$

Examining the equation for A, it can be seen that if $\Delta R = 0$, the harmonic terms will be eliminated. Although this metric is constantly being improved in analog switches, the on-resistance is never completely independent of input voltage. An alternate, and more common solution, is to select a load resistance value that is much larger than the variations in the on-resistance. This solution is commonly used on analog inputs, where R_L is the input impedance of data acquisition circuitry and is typically very large.

Unfortunately, other applications that use analog switches do not have the luxury of specifying the load impedance. An example is switching the outputs to high-fidelity headphones. Furthermore, the distortion caused by even minute variations in switch on-resistance represents a surprising amount of distortion. The total harmonic distortion and noise (THD+N) of the circuit in Figure 3 was measured with a 2-V_{PP} signal and load resistances of 100 kΩ and 600 Ω. According to the TS5A22362 analog-switch datasheet, the on-resistance at 0 V (room temperature) is about 0.37 Ω. The on-resistance will vary approximately 0.115 Ω over the range of the 2-V_{PP} input signal.

The measured THD+N over frequency is given in Figure 4 for two load impedances. With the 100-kΩ load impedance, the THD+N is extremely low. In this case, the measurement is determined by the noise floor of the instrument, roughly 0.0005%. However, decreasing the load impedance to 600 Ω increases the distortion by an order of magnitude to 0.005%. This level of distortion may not be acceptable in many high-precision analog systems.

The distortion contribution from the switch is constant over frequency because the voltage-drop across the switch does not change over the measured bandwidth.

An FFT of the output signal at 1 kHz into a 600-Ω load (Figure 5) shows that the 2nd harmonic is dominant, but spurs are visible above the noise floor up to the 5th harmonic. The harmonics are due to the R_{ON} variations of the switch.

Conceivably, enclosing the switch inside the feedback loop of an amplifier allows for the additional distortion to be corrected, but this is not as simple as it may seem. The amplifier's feedback loop must still be closed when the switch is open, otherwise the amplifier output would saturate to one of the power supply rails. Closing the switch while the amplifier output is saturated could cause an undesirable transient voltage at the load.

One solution to this problem is shown in Figure 6. In this circuit topology, two switches are used. One switch, S_1, is the signal path for the load. The second switch, S_2, allows the op amp feedback loop to be closed around the first switch. S_2 contributes negligible additional distortion in the system because the op amp inverting input is a very high impedance.

With both switches configured as shown in Figure 6, resistor R_1 is in parallel with the pathway through S_1 and S_2. For minimal distortion, the dominant feedback pathway should be through the switches and not through R_1. Therefore, the on resistance of the switches should be much less than R_1:

$$R_1 \gg R_{ON(S1)} + R_{ON(S2)} \quad (9)$$

Considering the 0.37-Ω on-resistance of an analog switch such as the TS5A22362, this requirement is easily accomplished. But other switch parts, such as the extremely popular CD4066B, have typical on-resistances greater than 100 Ω.

When the switches are moved to their alternate position in order to disconnect the load from the amplifier output, R_1 closes the feedback loop of the op amp. Stability must always be considered when placing a resistor in the feedback path of an op amp. The feedback resistor interacts with the input capacitance to degrade the feedback-loop

Figure 4: THD+N measurement of the circuit in Figure 3

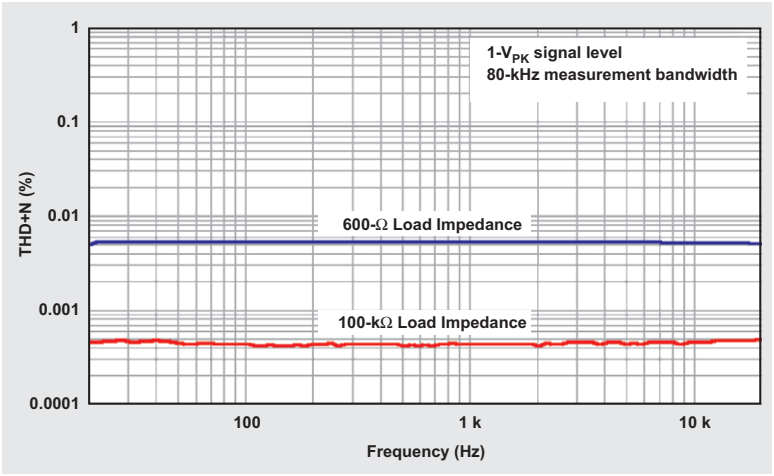


Figure 5. Spectrum of a 1-V_{PK}, 1-kHz sine wave at the output of the circuit in Figure 3

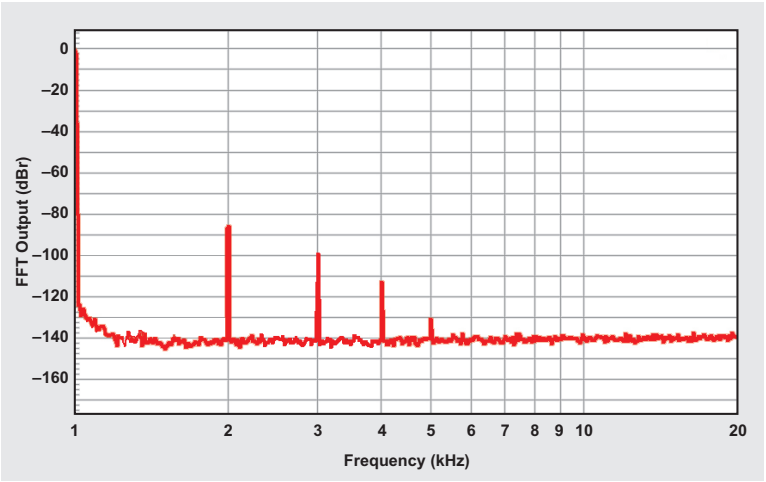
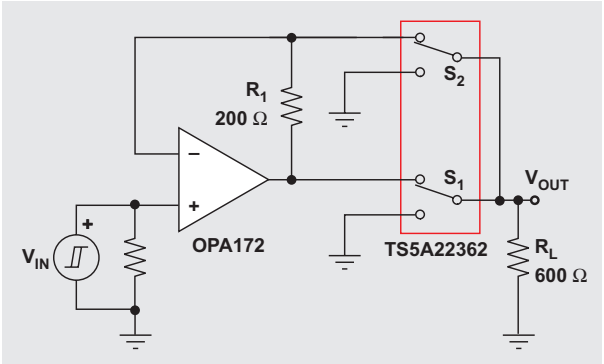


Figure 6: A dual-switch solution to close the amplifier feedback loop



phase margin. A conservative rule of thumb is given in Equation 10, the derivation of which is given in Reference 2.

$$\frac{1}{20\pi f_{GBW}(C_{CM} \parallel C_{DM})} \geq R_1 \quad (10)$$

Where f_{GBW} is the op amp gain-bandwidth product and C_{CM} and C_{DM} are the op amp common-mode and differential input capacitances, respectively. Inserting the appropriate values for the OPA172, a precision op amp, gives a maximum value for R_1 of 198.9 Ω. A 200-Ω resistor is reasonably close to the calculated value to avoid stability concerns.

$$\frac{1}{20\pi(10\ \text{MHz})(8\ \text{pF})} = 198.9 \geq R_1 \quad (11)$$

The circuit in Figure 6 was tested in the previously described manner and the results are given in Figures 7 and 8. By enclosing the switch inside the feedback loop of the op amp, the additional distortion from the R_{ON} variation has been effectively eliminated. The THD+N measurement over frequency for both load impedances (600 Ω and 100 kΩ) are identical, and at the noise floor of the measurement instrument.

Examining the FFT of the output signal (Figure 8) shows that the additional harmonics from the TS5A22362 are now below the noise floor of the measurement instrument.

For high-performance analog systems where harmonic distortion must be minimized, enclosing a CMOS analog switch inside the feedback loop of an op amp can greatly improve performance. The circuit topology shown in Figure 6 reduces harmonic distortion from the switch and also allows the amplifier output to be completely disconnected from the load. The feedback loop of the op amp is closed regardless of the switch configuration, preventing the amplifier output from saturating and causing unwanted voltage transients when the switch is closed. Furthermore, a CMOS analog switch with extremely low R_{ON} variation is no longer absolutely crucial, which can potentially reduce system costs.

Figure 7: THD+N measurement of the circuit in Figure 6

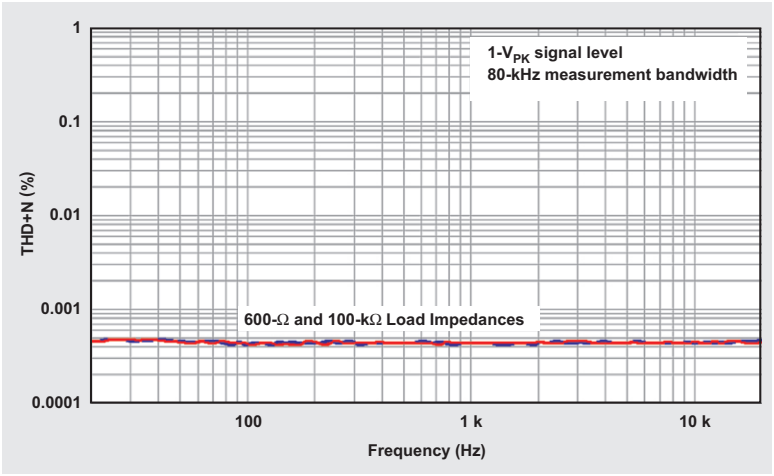
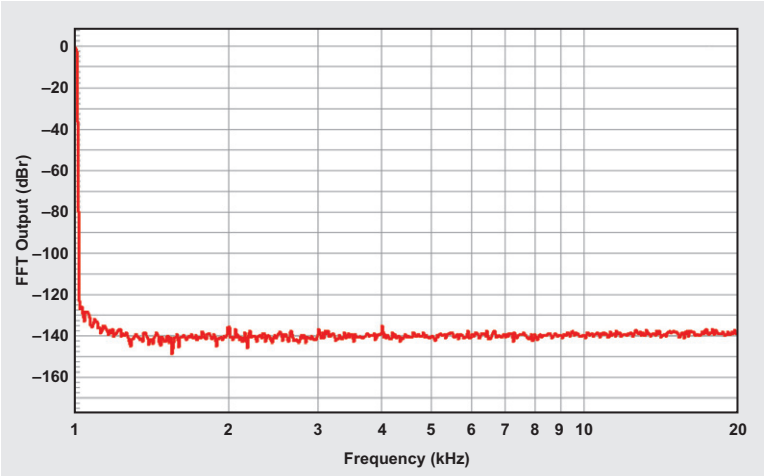


Figure 8: Spectrum of a 1-V_{PK}, 1-kHz sine wave at the output of the circuit in Figure 6



Acknowledgements

The author wishes to acknowledge John Xu, TI analog field applications engineer, whose idea was the initial inspiration for this work.

Reference

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Related Web sites

www.ti.com/1q15-TS5A22362

www.ti.com/1q15-CD4066B

www.ti.com/1q15-OPA172

Bandstop filters and the Bainter topology

By Bonnie C. Baker
Senior Applications Engineer

Many applications, such as tone-signaling, audio-signal, hearing-aid feedback, or mains rejection systems, require bandstop (notch) filters to eliminate undesirable signals. One can achieve these signal reductions by using active bandstop analog filters.

The bandstop filter circuit topologies considered in this article are Sallen-Key, multiple-feedback, and Bainter. Each circuit produces a second-order bandstop filter, with one pole and one zero in the transfer function

A starting point is to define the bandstop filter characteristics. In Figure 1, the bandstop filter disallows signals within a certain bandwidth (BW_P), while passing frequencies above and below the rejected frequency area.

This standard generic diagram highlights the key bandstop filter parameters; passband, stopband, f_0, BW_P, A_O, A_{SB}, BW_S, and R_P.

The three filter-response regions are the low-frequency passband, the stopband, and the high-frequency passband. In both of the passband frequency regions, signals pass freely from the input to the filter's output. In the stopband region, frequency signals are attenuated per the diagram in Figure 1. The notch filter's center frequency is f_0.

BW_P (passband bandwidth) defines the –3-dB bandwidth inside the bandstop filter. This bandwidth also defines the quality factor or Q (See Reference 1) of the filter, where $Q = (f_0 / BW_P)$. BW_S defines the stopband bandwidth. In the region below the BW_S point, the bandstop filter creates a notch, sometimes dipping –100 dB or more.

The stopband attenuation ranges from A_O to the A_{SB} (stopband magnitude). A_O (passband gain) and A_{SB} along with the specified stopband attenuation, defines the speed of the notch's attenuation. Finally, for Chebyshev approximations, the definition of the ripple magnitude is R_P.

The bandpass/notch filter requires pairs of poles and zeroes in the transfer function. The corner frequency of the poles and zeroes resides at or near f_0.

The transfer function of the bandstop/notch filter is:

$$H(s) = \frac{H_0\left(s^2 + w_z^{\,2}\right)}{s^2 + \frac{\omega_0}{Q}s + \omega_0^{\,2}} \qquad (1)$$

For comparison purposes, the following discussion includes the Sallen-Key, multiple-feedback, and Bainter filter topologies to realize a bandstop filter.

Figure 1. Frequency response of the bandstop filter

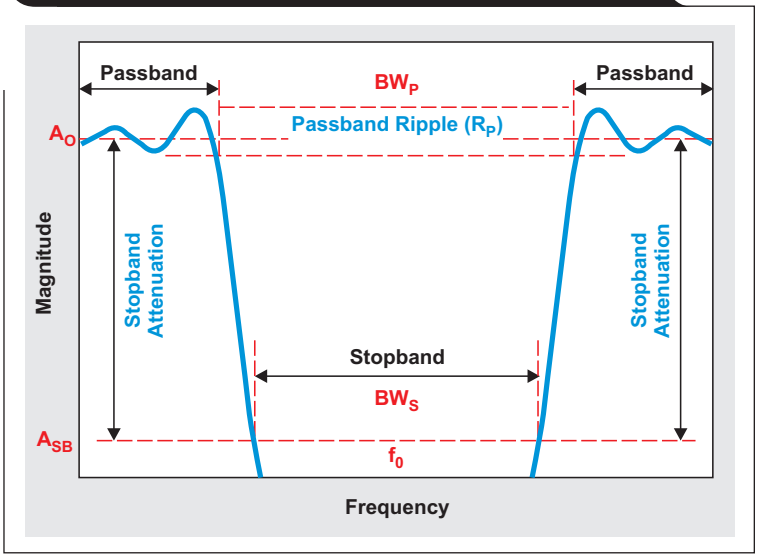
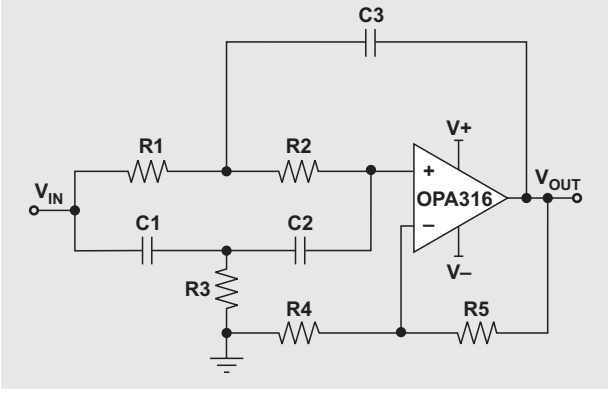


Figure 2. Second-order Sallen-Key bandstop or notch filter



Sallen-Key circuit topology

The Sallen-Key topology in Figure 2 implements a second-order bandstop filter. This particular circuit is valued for its simplicity, as it has one amplifier, five resistors, and three capacitors. One advantage of this circuit is that the ratio of the largest resistor to the smallest resistor is small, as well of the capacitor high and low values. This is beneficial to the manufacturability of the filter.

While the Sallen-Key filter is widely used in low-pass and high-pass filters, it has several serious drawbacks for bandstop filters. The Sallen-Key is not easily tuned because of the interaction of the component values on the center frequency (f_0) and Q. The open-loop output resistance

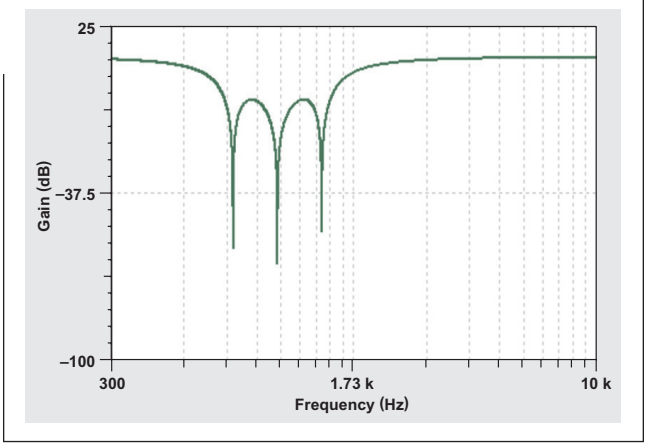
also interferes while attempting to produce the ideal notch-filter characteristics (Figure 3). Additionally, f_0 cannot be easily adjusted because of component interaction.

A sixth-order filter is implemented by cascading three second-order filters (Figure 2) in series. Figure 3 shows the sixth-order, closed-loop response of a Sallen-Key circuit. This figure shows the Sallen-Key's circuit closed-loop gain response of 4.58 V/V with a linear phase 0.5° approximation type and f_0 equal to 1 kHz.

The construct of this sixth-order filter uses ideal resistors (15), capacitors (9), and amplifiers (3). With ideal components and devices in the circuit, the closed-loop frequency response has three spurs going down and shows that there is only about –15 dB of attenuation within the notch.

As a consequence of these shortcomings, the Sallen-Key notch filter is not a recommended topology for bandstop filter construction.

Figure 3. Closed-loop frequency response of sixth-order Sallen-Key notch filter



Multiple-feedback circuit topology

The multiple-feedback (MFB) topology in Figure 4 implements a second-order bandstop. The MFB circuit is also valued for its simplicity, having one op amp, three resistors, and two capacitors in the first stage. In the final stage, there is one op amp and three resistors. The second stage of this filter provides a summing function to add high-pass and low-pass responses at the end of the circuit. If it were a sixth-order filter, the final stage of this filter is at the end of the signal line, while there are three proceeding first stages.

While the MFB filter topology is widely used in low-pass, high-pass, and bandpass filters, it has several serious drawbacks for bandstop filters. The dependence of the transfer function on the op amp parameters is greater than the Sallen-Key realization. It is also hard to generate high-Q, high-frequency sections because of the limited open-loop gain of the amplifier at high frequencies.

Figure 5 shows the sixth-order, closed-loop response of a MFB circuit. A sixth-order filter is implemented by cascading three second-order filters (Figure 4) in series. In Figure 5, the MFB's circuit closed-loop gain of 4.58 V/V with an approximation type of linear phase 0.5° and f_0 equal to 1 kHz.

The filter in Figure 5 uses ideal resistors (12), capacitors (6), and amplifiers (4). With ideal components and devices in the circuit, the closed-loop frequency response shows that there is approximately –36.6 dB of attenuation within the notch. However, on either side of the notch, the filter gain increases by an undesirable amount of about 1.4 dB. These two humps are a consequence of the challenge to match the high-pass and low-pass filter in this system with the final-stage summing function.

Figure 4. A second-order multiple-feedback bandstop or notch filter

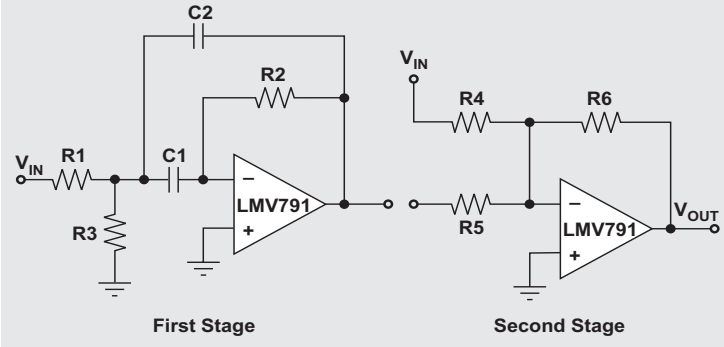
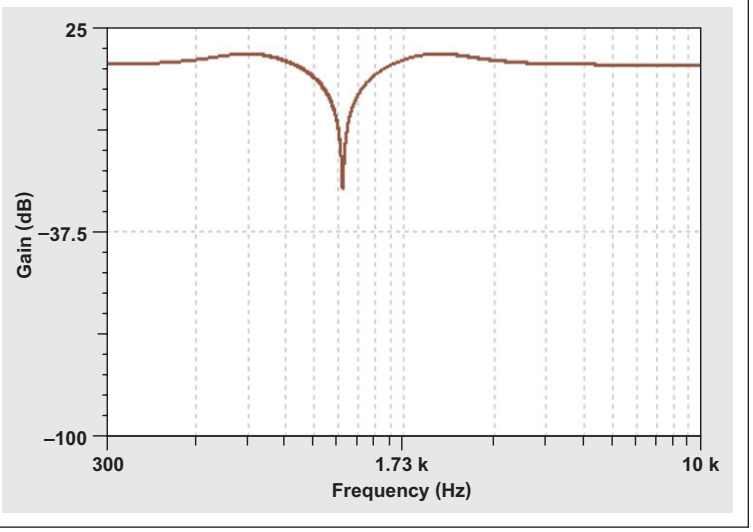


Figure 5. Closed-loop frequency response of sixth-order MFB notch filter



As a consequence of these shortcomings, the MFB notch filter is not a recommended topology for bandstop-filter construction.

Bainter circuit topology

As Figure 6 shows, the Bainter filter topology[2] has three simple amplifier circuit blocks with two feedback loops. The frequency response served at the output of A1 is a high-pass filter. The frequency response at the output of A2 is a low-pass filter, and A3 acts as a summer by providing the entire notch function at its output.

The circuit in Figure 6 has several fascinating properties. The Q of the notch is dependent on the gain of the amplifiers as opposed to component matching. Consequently, the notch depth is not sensitive to temperature drift or aging. The notch depth remains relatively constant even though the filter's frequency, f_0, may shift. Additionally, the component sensitivity of this filter is very low, about 0.5.

Figure 7 shows the sixth-order, closed-loop response of a Bainter circuit. A sixth-order filter is formed by cascading three second-order filters (Figure 6) in series. In Figure 7, the Bainter's circuit closed-loop gain is 4.58 V/V with an approximation type of linear phase 0.5° and f_0 equal to 1 kHz.

The construct of this filter uses ideal resistors (21), capacitors (6), and amplifiers (9). With ideal components and devices in the circuit, there is a less than –100 dB of attenuation for the closed-loop frequency response. Additionally, in contrast to the Sallen-Key and MFB filters, this is a very clean notch filter.

The Bainter notch filter is definitely a recommended topology for bandstop filter construction.

Figure 6. A second-order Bainter bandstop or notch filter

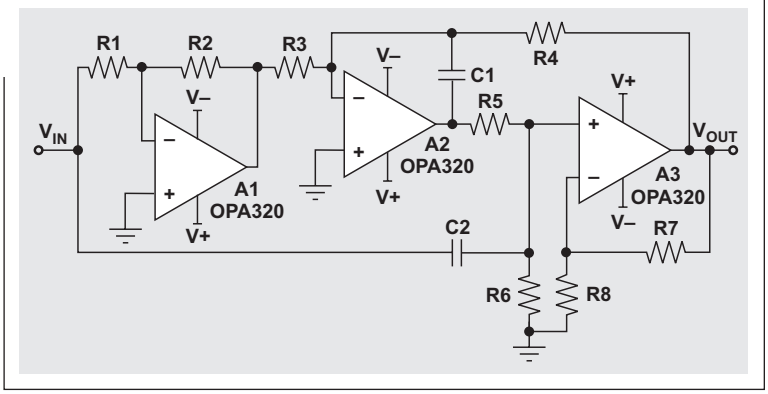
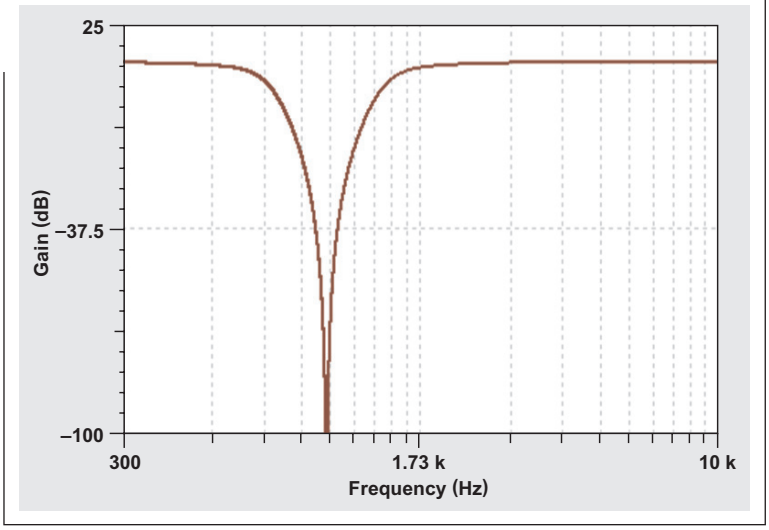


Figure 7. Closed-loop frequency response of sixth-order Bainter notch filter



Conclusion

When evaluating the correct topology for a bandstop filter, it is important to examine the closed-loop frequency response. Industry implementations of bandstop filters may use the Sallen-Key or MFB circuits. Both of these circuit topologies have their problems in the bandstop regions and in the passband regions with poor notch characteristics and unnecessary gain peaking in the passband region. The Bainter filter far surpasses the bandstop performance of these two filters by creating a clean notch filter.

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2. "Active filter has stable notch, and response can be regulated," Bainter, James, Electronics, October 2, 1975. Available: **www.google.com/**

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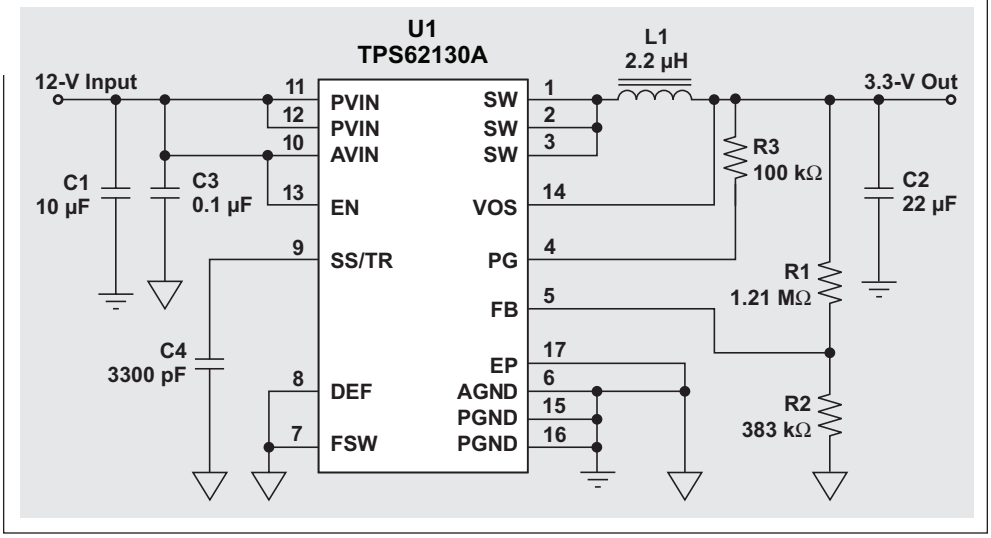
Five steps to a great PCB layout for a step-down converter

By Chris Glaser
Applications Engineer

Introduction

Especially for switch-mode power supplies (SMPSs), the printed circuit board (PCB) layout is a critical but often under appreciated step in achieving proper performance and reliability. Errors in the PCB layout cause a variety of misbehaviors including poor output voltage regulation, switching jitter, and even device failure. Issues like these should be avoided at all costs, since fixing them usually requires a PCB design modification. However, these pitfalls are easily circumvented if time and thought are spent during the PCB layout process before the first PCBs are ever ordered. This article presents five simple steps to ensure that your next step-down converter's PCB layout is robust and ready for prototyping.

Figure 1. TPS62130A circuit used to step-down 12-V to 3.3-V

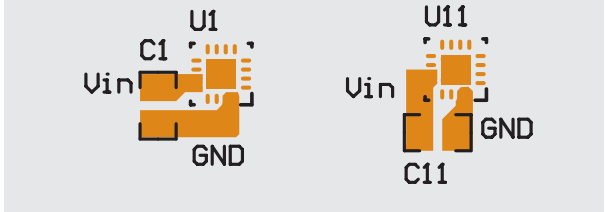


When designing a server, tablet, or electronic point-of-sale machine, a best-practice option with the least risk is to simply copy the PCB layout example found on the evaluation module (EVM) and shown in the datasheet. However, this may not always be possible for various reasons. This article was created for these cases and details a five-step procedure to design a good PCB layout for any TPS62xxx integrated-switch, step-down converter. The internal MOSFETs and integrated loop-compensation circuitry greatly simplify the PCB layout of these devices by reducing the difficulty and time required to do the PCB layout. The versatile TPS62130A is used as the example step-down converter, which can be used in each of the above applications. Figure 1 shows the completed schematic of a typical circuit.

Step #1. Place and route the input capacitor

The input capacitor is the single-most important component for reliable operation of any step-down converter. As such, it should be the first component placed in the layout after the IC. Route the capacitor to the IC immediately after it is placed, so that nothing else can be routed in its path. Extra parasitic inductance between the input capacitor's terminals, both power and ground, and the IC's PVIN and PGND terminals creates excessive voltage spikes due to the switching action from V = L × dI/dt. This can lead to IC failure.

Figure 2. Layout and routing of the IC and the input capacitor to reduce voltage spikes



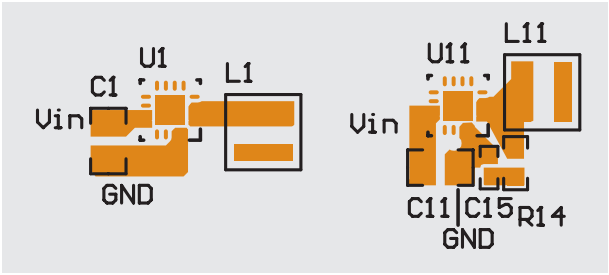
Place the input capacitor as close to the IC as allowed by manufacturing rules. Planes connect the input capacitor's terminals to the IC's. Making such a wide and short plane connection minimizes trace inductance. Add vias to connect to the system's input voltage and ground. These are added in Step #5 as they are less important. Figure 2 shows the correct placement and routing of the input capacitor and IC. Two circuits are shown due to two acceptable input-capacitor placements (C1 and C11) based on the TPS62130A's pinout (U1 and U11). Pin 1 of the IC is in the bottom right corner.

Step #2. Place and route the inductor and SW-node snubber

The second most important component to place and route is the inductor and SW-node snubber, if required. Snubber circuits are occasionally required to reduce the electromagnetic interference (EMI) of SMPSs by slowing down the rise and fall times of the SW node. Unfortunately, slowing down these timings reduces efficiency by increasing switching losses. Since the SW-node voltage swings from the input voltage to ground with very fast rise and fall times, it is the main generator of EMI in a SMPS. Modern SMPSs typically incorporate some EMI reduction techniques, which generally eliminate the need for a snubber. To be effective, add a resistor/capacitor (RC) snubber to the PCB layout at this step. This is where it has the shortest possible routing between the SW and PGND (GND) pins, minimizing its parasitic inductance.[1]

To reduce radiated EMI, place the inductor as close as possible to the IC with the area of the SW-node copper kept to a minimum. All copper connected to the SW node is one plate of a parasitic capacitor, whose other plate is each node in the circuit. This capacitor is a noise coupling path. By keeping the SW node small, the area of the capacitor plate is minimized and the coupling reduced. Rotate the inductor as needed in order to keep the SW node small and to make an easy connection to the output capacitor (Step #3). Figure 3 shows proper inductor placement (L1 and L11) with and without the RC snubber (R14 and C15) from SW to PGND (GND).

Figure 3. Layout and routing of the inductor and RC snubber to minimize EMI



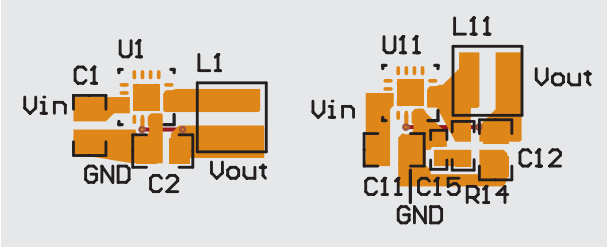
Step #3. Place and route the output capacitor and VOS pin

The output capacitor completes the routing of the power components (internal MOSFETs, input capacitor, output capacitor, inductor, and optional snubber). It is the final component connected to the power ground terminal in the system and is placed to minimize the distance from the inductor back to power ground. An improper output capacitor placement typically causes poor output voltage regulation.

Each power component is placed and routed to minimize the paths between them. Keeping these loop areas small enables the best operation of the SMPS. Finally, no vias should be used to route these components, because vias add significant inductance to the trace. In some specific cases, vias may be used on the SW-node connection. See the special considerations section at the end of this article.

The most critical small-signal connection is the VOS input pin. An improper or noisy VOS pin connection causes poor output voltage regulation, switching jitter, and in some cases, IC failure. Route the VOS pin now to ensure that it has priority over other signal routings. Make the VOS pin trace short and direct to the output capacitor. Due to the TPS62130A's pinout, route the VOS pin with two vias and a dedicated trace to the output capacitor. This gives priority to the power components in the circuit. To reduce noise pickup, isolate the two vias from all other connections except for the VOS pin and output voltage plane on the top layer. Do not route the TPS62130A's VOS pin directly on the top layer, as this breaks the PGND connection which is more important. Figure 4 shows proper placement and routing for C2 and C12 output capacitors and a good VOS-pin routing on the bottom layer.

Figure 4. PCB layout and routing of the output capacitor and the VOS pin for good regulation



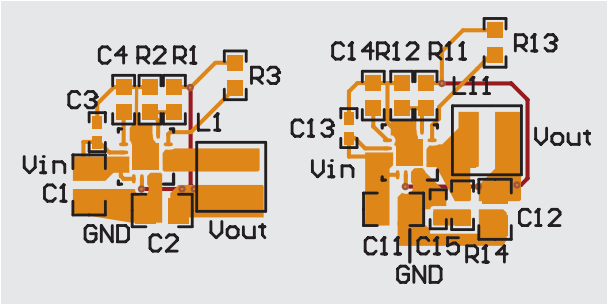
Step #4. Place and route the small-signal components

The small-signal components comprise all analog and digital components not directly related to the power conversion. These are components like the FB pin voltage divider, soft-start capacitor, and any small-value decoupling capacitors (0.1 µF for example). While the noisier power components and their nodes generate noise, the analog small-signal components are sensitive to noise. Place each of these components close to the IC with a short and direct routing to keep their noise sensitivity low. It is especially important to keep the FB node as small as possible to minimize noise pickup and provide good output voltage regulation. Use a common analog or quiet ground. Keep all components on a single side of the PCB for ease of routing. Common issues with poor placement and routing of small-signal components include poor output voltage regulation, erratic soft-start operation, and device operational problems.

Any digital signals, such as the EN and PG pin circuitry, are the least important to place and route, so do these last. Digital pins typically have a low impedance driving source. Any pull-up or pull-down resistors required

generally can be placed anywhere along the signal's path and do not need to be located close to the SMPS. Figure 5 shows proper placement and routing of the small-signal components: FB resistors (R1, R2 and R11, R12), SS/TR capacitor (C4 and C14), AVIN decoupling capacitor (C3 and C13), and PG pin pull-up resistor (R3 and R13).

Figure 5. Layout and routing of digital and small-signal components



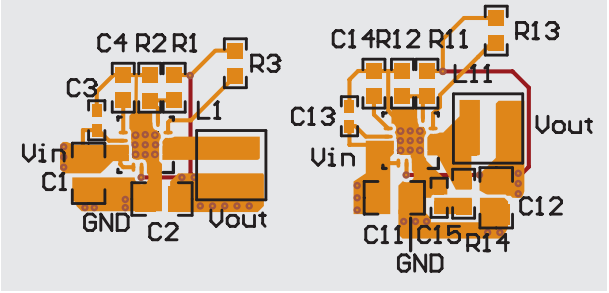
Step #5. Make a single-point ground and connect to the rest of the system

Always follow the datasheet's specific recommendations for grounding. Generally, this means keeping one ground for power components, which are noisy, and a separate ground for the small-signal components, which are quiet. By following the recommendations and steps given above, this is already done. Next, join these two grounds at a single point, typically the exposed thermal pad under the IC, which should also be connected to ground. Referring to Figure 5, the only edit needed to the grounds is to completely pour a copper plane between the PGND pins and the exposed thermal pad. The TPS62130A datasheet goes further to make this connection mandatory. Not making this connection might cause noise-related issues, such as poor output voltage regulation, or possibly improper logic levels for the digital input pins. This is due to voltage shifts between the grounds during operation. Properly connecting the grounds also provides the best thermal relief of the device.

With the grounding finished, it's time to connect this circuit to the rest of the system. This can be done with vias as the input voltage, output voltage, and ground are typically routed on planes on inner PCB layers to reach the various circuits. Starting with ground, vias are best placed directly under the IC so that the exposed thermal pad conducts its heat down into the PCB layers. This is required to achieve the IC's best thermal performance. Vias are also typically placed at the input- and output-capacitor's ground terminal. Placing vias into the system ground plane on the quiet grounded components is not generally recommended because this can couple noise from the ground plane into these nets. These grounds are best routed directly back to the AGND pin, where they make a single point connection to the exposed thermal pad.

Vias are also needed to connect the input and output voltages back into the system. It is best to place the vias outside the circuit, versus between the input capacitor and IC, for example, to not obstruct critical routings between components. A good rule of thumb for the number of vias necessary is to use one via per amp of current flowing. However, more is better if room allows. A finished layout is shown in Figure 6.

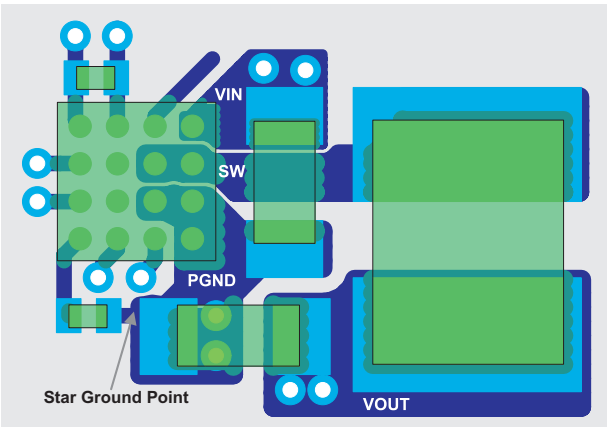
Figure 6. Finished PCB layout and routing with vias and single-point ground



Special considerations

Always consult the device's datasheet for specific layout recommendations and a recommended layout example. Directions and examples provided are sufficient for most devices' layouts. One type of layout that generates some confusion is commonly found on wafer chip-scale packages (WCSPs), such as the TPS62360. In many WCSP step-down converters, the IC's pinout places the SW pin between the VIN and PGND (GND) pins. If following Step #1, the input capacitor blocks access to the SW pin unless the SW pin is routed underneath the input capacitor. Some think this is undesirable because that trace must be rather thin to be routed between the terminals of a small component, such as the input capacitor. This then looks like Figure 7.

Figure 7. Recommended layout of the TPS62360 in a WCSP package[2]



The preferred PCB layout method is to route the SW pin underneath the input capacitor (Figure 7). While the SW trace is thin, it is also very short, which keeps the SW node small. This follows Step #2 to reduce EMI. If it is not possible to route such a trace, then use vias to connect the SW pin to the inductor. Vias in this connection merely create additional EMI by the longer routing. However, the added inductance of these vias is not critical as this parasitic inductance is in series with the inductor's inductance. Using vias in this path is a better choice than moving the input capacitor out of its ideal location.

Conclusion

When designing the PCB layout for a SMPS, always consult the device's datasheet and EVM for examples and specific recommendations. But for cases when it is not possible to exactly follow these, or in the rare case where these are not present, five simple steps allow for a good step-down converter layout:

1. Place and route the input capacitor.
2. Place and route the inductor and SW-node snubber.
3. Place and route the output capacitor and VOS pin.
4. Place and route the small-signal components.
5. Make a single-point ground and connect to the rest of the system.

Doing these steps will generate a robust design that gives good performance for servers, tablets, electronic point-of-sale machines, and any other system that uses step-down converters.

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Related Web sites

www.ti.com/1q15-TPS62130A

www.ti.com/1q15-TPS62360

Fly-Buck™ converter provides EMC and isolation in PLC applications

By Timothy Hegarty
Systems Engineer, Non-Isolated Power Solutions

How do you provide galvanically-isolated positive or negative voltage rails while keeping cost and complexity to a minimum? At the same time, how do you fend off a diversity of challenges tied to wide input voltage range, multiple outputs, small solution size, electromagnetic compatibility (EMC), and high reliability?

Consider factory automation and control end equipment segments such as programmable logic controllers (PLC), field transmitters, sensors and process instrumentation, industrial communication, data acquisition systems (DAS), human machine interface (HMI), and IGBT-based motor drives. There is an inescapable requirement in many of these applications for more functionality in less space. Solution footprint and height are critical, meaning system designers must explore all avenues to conserve valuable PCB real estate. For the power solution in particular, a key requirement is a robust design that provides one or more isolated voltage rails. This article focuses on PLCs in particular, examines EMC and safety isolation requirements, and describes a multi-output power converter solution.

PLC I/O module

An illustrative block diagram of a PLC I/O module is given in Figure 1. Used in modular rack-based PLC systems, an I/O module establishes the physical connection between the PLC and factory or field equipment. The rack can accept various types of I/O modules that effectively slide into slots in the rack to accomplish backplane connection.

The system in Figure 1 includes a microcontroller, data converters, isolators, input amplifiers, I/V output drivers, references, wired and/or wireless connectivity, and a multi-output DC/DC Fly-Buck™-based power solution[1,2]. Analog I/O signal ranges are usually selected from the voltage options of 0 to 5 V, 0 to 10 V, ±5 V, and ±10 V, or the current options of 0 to 20 mA and 4 to 20 mA.

Figure 1. Factory automation PLC I/O module

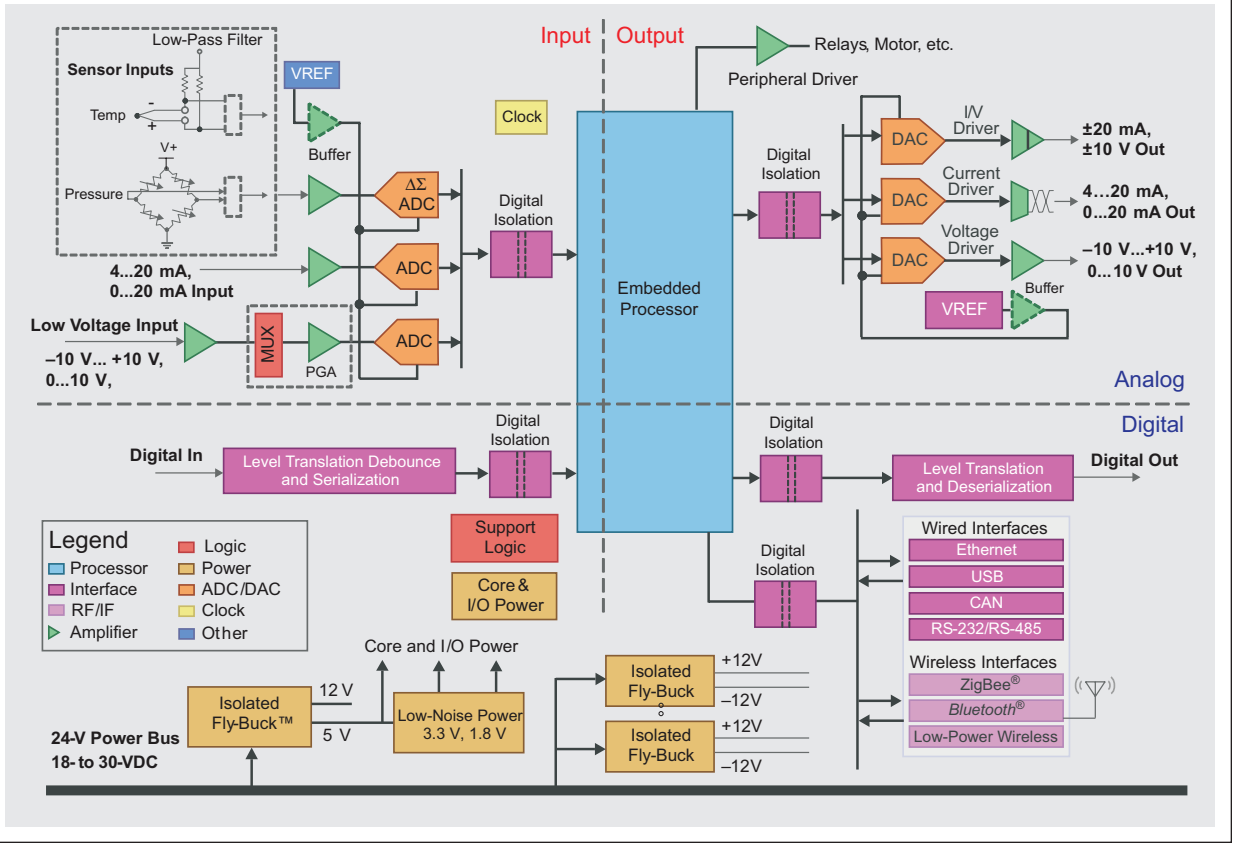


Table 1: Summary of popular harmonized standards for EMC and electrical safety

Standard	Applicability	Remarks
IEC/EN 61131-2	Listed in EMC Directive	PLC equipment specific requirements and tests
IEC/EN 61000-6-2/-4	Listed in EMC Directive	Generic immunity/emission standard for industrial environments
IEC/EN 61326-1/-2	Listed in EMC Directive	Electrical equipment for measurement, control and laboratory use
IEC/EN 61000-4-2	High-frequency disturbances	ESD immunity test
IEC/EN 61000-4-3		Radiated EM field immunity test
IEC/EN 61000-4-4		Switching transients (EFT/burst) immunity test
IEC/EN 61000-4-5		Surge impulse (lightning) immunity test
IEC/EN 61000-4-6		Conducted RF current immunity test
IEC/EN 61000-4-8	Low frequency disturbances	50/60-Hz magnetic field immunity test
IEC/EN 61000-4-11		Voltage dips and short interruptions immunity test
IEC/EN 61000-4-12		Damped oscillatory waves immunity test
IEC/EN 55011 (or CISPR 11)	Low- and high-frequency emissions	Conducted and radiated emissions for industrial, scientific, and medical (ISM) equipment
IEC/EN 60664-1	Listed in Low Voltage Directive	Insulation for equipment within low-voltage systems. Low voltage defined as 75 to 1500 VDC or 50 to 1000 VAC_{rms}
IEC/EN 61010-1	Safety	Safety requirements for electrical equipment for measurement, control and laboratory use
IEC/EN 60950-1	Safety	Safety of IT equipment

Emissions, immunity, and safety requirements for PLCs

Factory equipment placed into the European Union (EU) market should generally comply when fully installed with the EMC Directive (2014/30/EU) and low-voltage (LV) directive (2014/35/EU). These directives point to compliance of the main requirements using a list of harmonized standards based on several generic and product specific standards. Table 1 lists several European Norm (EN) standards[3-5] that apply to EMC and electrical safety. Many of these tests are performed at the system level, either at the enclosure power or data port(s). Note that the Low Voltage Directive applies if the applicable input or output voltage lies within 75 to 1500 VDC or 50 to 1000 VAC_{rms}.

EN 61131-2 specifies requirements and related tests specifically for PLCs and their associated peripherals. However, while this standard supersedes generic standards for immunity (EN 50082-2) and safety (EN 61010-3), generic standards are still used for emissions (EN 61000-6-2) and AC harmonics/fluctuations (EN 61000-3-2) for AC-powered equipment. Also, various tests referenced within the EN 61000-4 transient immunity specification cater to electrostatic discharge (ESD), electrical fast transient (EFT)/burst, lightning surge, and conducted/radiated RF immunity[6,7].

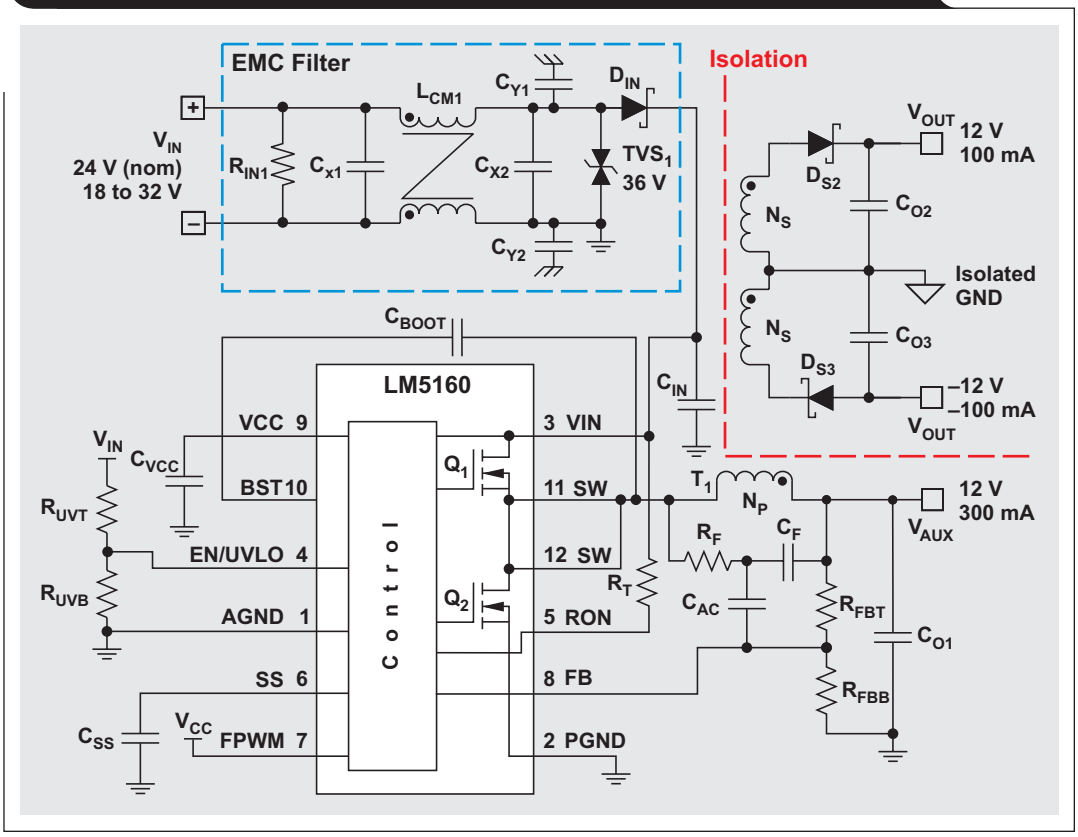
Choosing a power solution

Converter- or controller-based IC solutions are widely available, and the choice hinges initially on input voltage and output current specifications. However, solutions specifically with a large input voltage range (wide V_{IN}) offer outsized voltage rating and operating margin to deal with supply rail voltage transients described in EN 61000-4. For a given PLC application, the power solution must be chosen to provide sufficient power for the given I/O configuration and the number of base/option module slots to be powered. Multiple isolated-converter outputs are required, particularly if isolation is required on a per-channel basis to protect against transients and ground loops.

The wide-V_{IN} Fly-Buck circuit has gained prominence from a range of buck-based topologies. The concept is becoming a more mainstream solution for power system engineers. The most noteworthy feature of a Fly-Buck converter is what is missing. Built from the reliable synchronous buck regulator, the Fly-Buck has neither loop compensation nor feedback optocoupler components. A compensated error amplifier is not needed, and a constant on-time (COT) control approach gives nearly instantaneous response for excellent transient dynamics. Feedback regulation is from the primary side through a standard resistor divider. Switching frequency is kept steady with line feedforward and continuous conduction mode (CCM) operation.

For maximum flexibility, both isolated and non-isolated outputs are available. This makes the Fly-Buck ideal for auxiliary and bias rails, floating supplies for digital isolators (Figure 1), and bipolar supplies for powering high-precision amplifiers and data converters[2]. To customize for additional outputs, simply add a transformer secondary winding with requisite number of turns, a rectifier diode, and an output capacitor. For space-constrained designs, dual, triple, quad, or more outputs are easily obtained with a small-size magnetic component. As a multi-output converter, the Fly-Buck is an excellent fit for PLCs where a high level of integration is needed as PLC channel count and functional density increase while the enclosure gets smaller.

Figure 2: EMC-compliant Fly-Buck™ regulator supply for PLC applications



Fly-Buck™ circuit implementation

Based on the 65-V, LM5160 synchronous regulator, the schematic of Figure 2 details an EMC-compliant Fly-Buck converter that delivers ±12-V isolated rails from a center-tapped secondary winding. Output voltages are scaled commensurate with turns ratio N_P/N_S of transformer T_1, and a 12-V primary-side output, V_{AUX}, is also provided. The red dashed line shows the isolation boundary. The upper circuitry is the EMC filter with common-mode inductor, X and Y capacitors, damping resistor, bidirectional transient voltage suppressor (TVS) voltage clamp, and reverse-polarity protection diode.

Optimizing EMC and isolation

The Fly-Buck topology has broad versatility to meet EMC and isolation performance objectives[1, 8]. Generally, the goal of EMC-protected circuits is to shunt the external transients to ground with low impedance and protect the circuit from damage. A Fly-Buck regulator with wide-V_{IN} capability permits a higher voltage TVS diode with a lower power rating and a smaller footprint that still meets the input transient immunity specifications for the power stage. Selection of TVS voltage rating is based on the dynamic impedance of the TVS and the expected peak current. Y capacitors, denoted as C_{YI} and C_{Y2} in Figure 2, shunt transient energy from the input lines to the enclosure's chassis ground. This approach is supplemented by small ferrite beads to provide high impedance at particularly sensitive nodes in the signal chain where high attenuation is required[8].

Off-the-shelf transformers are readily available with slim form factor and isolation rating of up to 4.5 kV peak, based on the requisite creepage and clearance. Certainly, larger isolation ratings dictate increased winding spacing, which means higher leakage inductance. Fortunately, the Fly-Buck is more tolerant of leakage inductance than an equivalent flyback converter. The Fly-Buck has no primary-side voltage spike related to leakage inductance, which provides an increased operating voltage margin against input-voltage transients. Also helpful for EMC, the Fly-Buck has a primary-side current waveform with lower harmonic content compared to the flyback.

Note that the 24-V industrial bus is normally double or reinforced insulated. Thus, functional isolation to 500-VDC continuous is usually adequate for the downstream power stages. As an example, most sensors adopt a 4- to 20-mA loop to transmit the measured quantity without noise or line-length concerns. In this case, an isolated rail increases signal accuracy and avoids any ground noise current issues related to interconnection of other equipment. As an example for basic or reinforced isolation, when powering digital data isolators, select the magnetic component that meets the isolation grade requirement and design the PCB layout to meet the relevant creepage and clearance specification of the referencing standard.

Conclusion

PLCs for factory automation and control applications have unique power-stage design requirements. Testament to its ease-of-use, small size, safety isolation, EMC regulatory compliance, and low overall bill-of-materials cost, a wide-V_{IN} Fly-Buck solution meets these requirements. Looking forward, as more demanding isolated applications come to fruition, complying to regulatory specifications is clearly a benchmark of power solutions for industrial applications that is becoming more important.

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   - "PLC I/O Module Front-End Controller Using a Tiva™ C Series ARM® Cortex™ M4 MCU." Available: **www.ti.com/tool/TIDA-00123**

Related Web sites

www.ti.com/1q15-LM5160

Stacked-FET switches enable high-efficiency, high-density solutions

By Tiger Zhou
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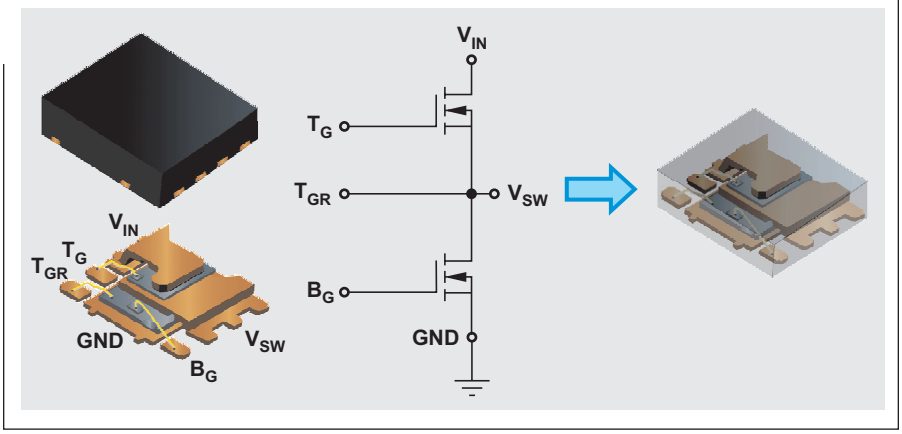
Introduction

High-efficiency, high-density power supplies have been a trend for communications equipment due to increasing power consumption and reduced board space. A stacked-FET switch enables high-efficiency and high-density solutions. Two real design examples are examined to illustrate this point. The first is a 30-A design where the benefits of a stacked-FET switch are evaluated relative to size reduction, efficiency gain and thermal budget savings. A second design implements the stacked-FET switch with an integrated driver to further increase system efficiency in a 60-A supply.

Figure 1. Stacked-FET switches in a SO8 package



As modern electronics equipment advances in speed and performance, the number of power rails keeps increasing in addition to an increase in power consumption. Conversely, the physical area for power supplies keeps shrinking because precious real estate is given to the core ASIC and processors. As such, a high-efficiency, high-density power supply is a challenge for every power designer.

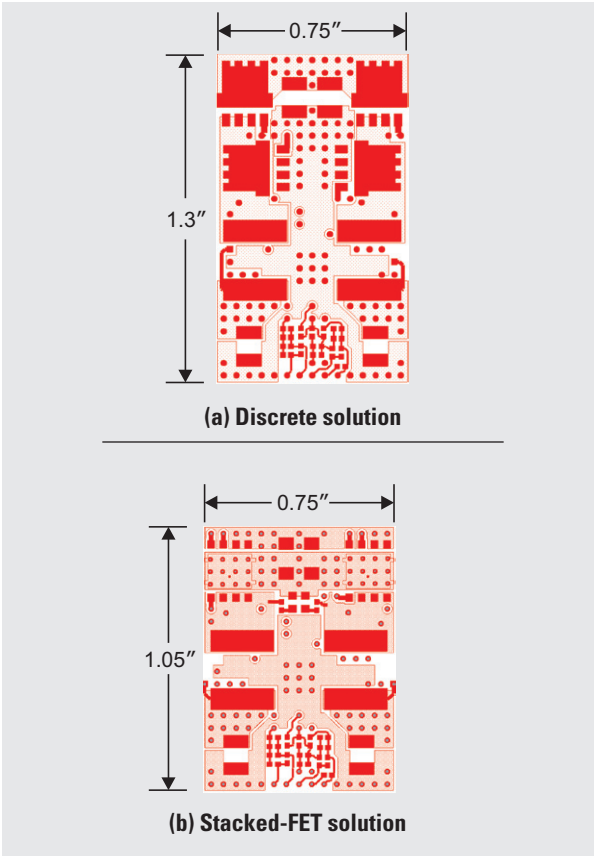
By combining the latest NexFET™ silicon and innovative packaging technologies, a dual FET (Figure 1) consists of two stacked FETs in a SO8 (5 mm x 6 mm) package. This configuration reduces the device footprint by half and doubles the output density.

Using a stacked-FET switch in point-of-load (PoL) applications has many benefits. this article presents a comparative study for a 1.8-V/30-A application using discrete FETs versus stacked FETs.

Reduced footprint

In the 30-A design example, a dual-phase synchronous buck controller was selected with optimum performance over ripple and transient responses. In the discrete solution layout, the FETs occupy nearly half the area. By replacing two discrete FETs with one stacked FET, the solution size shrinks by 20%. Figure 2 shows two layouts: (a) a discrete solution and (b) the stacked-FET solution. The discrete solution measures 0.75 by 1.3 inches, and the stacked-FET solution measures 0.75 by 1.05 inches.

Figure 2. A stacked-FET solution size is 20% smaller than a discrete-FET solution



Increased system efficiency

Compared to other state-of-the-art discrete FETs (Figure 3), the stacked-FET efficiency (red curve) is at least 2.2% higher. A stacked-FET switch, such as the CSD87350, has lower on-state resistance ($R_{DS(on)}$) and lower gate charge due to its unique device structure. Moreover, the stacked-FET packaging technique removes the parasitic inductance associated with traditional wire-bonded technology. Thus, it optimizes the switching speed and increases system efficiency. Both designs use the same inductor, input and output capacitors, and were tested under the same test conditions with a 10-V input, 1.8-V output and 300-kHz switching frequency.

Cooler operating temperatures

The power loss of stacked FETs is the sum of both the top and bottom FETs, but its thermal resistance is much less than that of discrete FETs. As illustrated in Figure 4, a stacked-FET switch runs 23° cooler than discrete FETs under the same test conditions (10 V_{IN}, 1.8-V/30-A output, 300 kHz). When the discrete FET reaches 108.7°C, the stacked-FET dies only reach 85.6°C because it is GND referenced.

The large area of the exposed pad connects to the ground plane of the PCB by 12 thermal vias, which utilizes multiple inner ground layers commonly available with a modern multi-layer PCB. For the discrete FET solution, the heat is concentrated in a small area, known as a switching plane, which prohibits multiple vias for signal integrity concerns.

It was demonstrated that stacked-FET technology enables high-efficiency and high-density solutions. One stacked FET replaces two discrete FETs, thus, reducing the overall solution size by 20%. Its increased efficiency and effective thermal conductivity allows it to run 23° cooler versus a discrete FET under same test conditions.

Figure 3. A stacked FET excels over other discrete FETs under the same test conditions

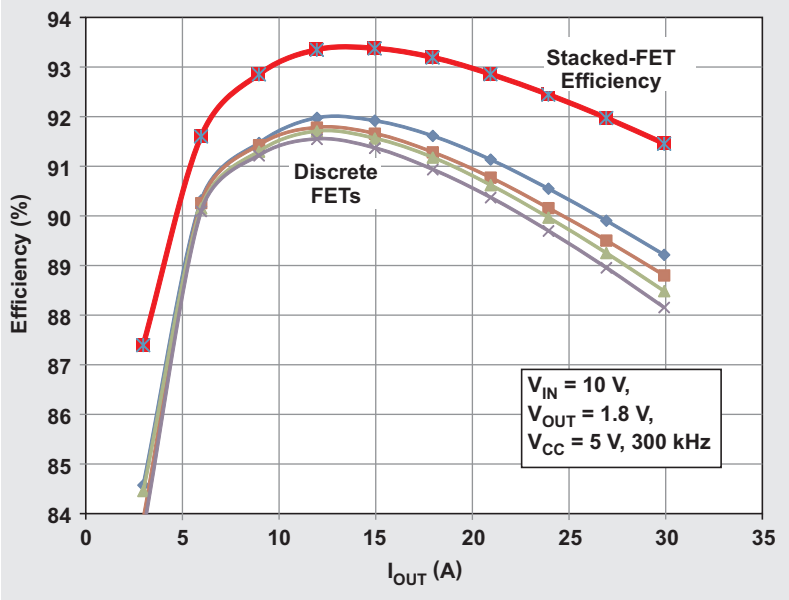
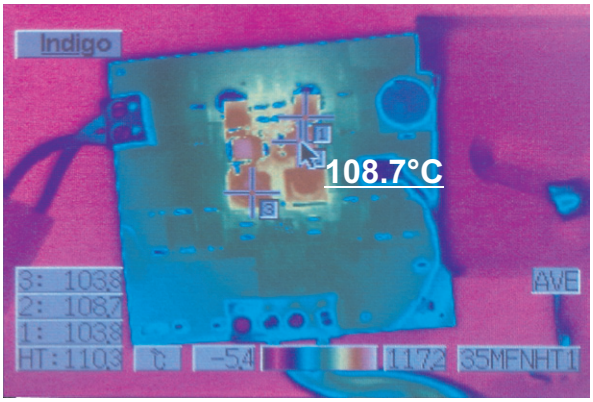
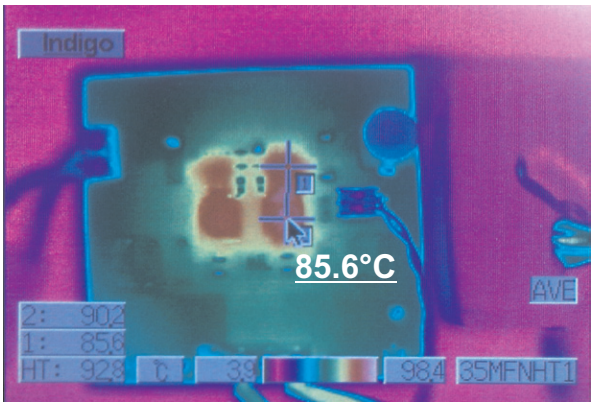


Figure 4. Operating temperatures of discrete and stacked FETs



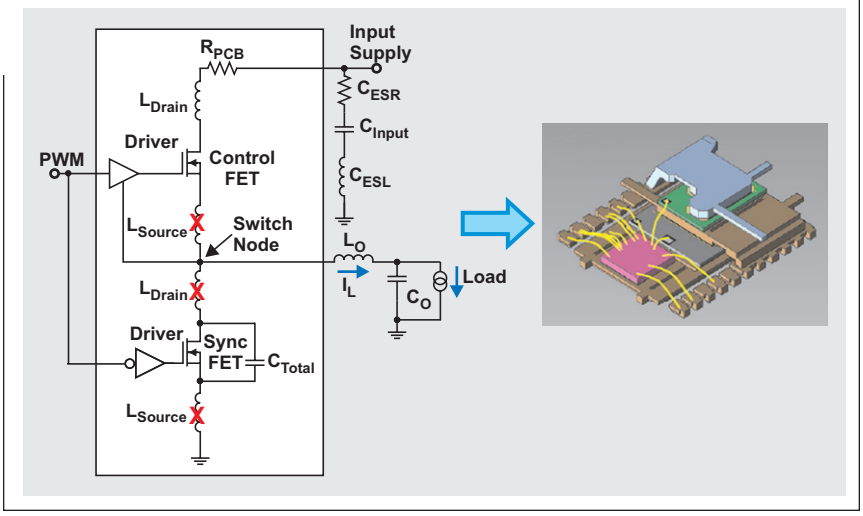
(a) Thermal image of a discrete FET



(b) Thermal image of a stacked FET

To further push the technology boundary, a new device, the CSD95372B in Figure 5, integrates a stacked-FET switch with an integrated driver. The package maintains the same size as a standard FET, which is SO8 (5 mm x 6 mm) package. By shortening the drive-to-FET distance, it fully optimizes the drive capability by minimizing the driver-related parasitic inductances. It has higher switching speeds, lower conduction loss and requires less PCB real estate. Therefore, it achieves even higher system efficiency.

Figure 5. A stacked FET with driver



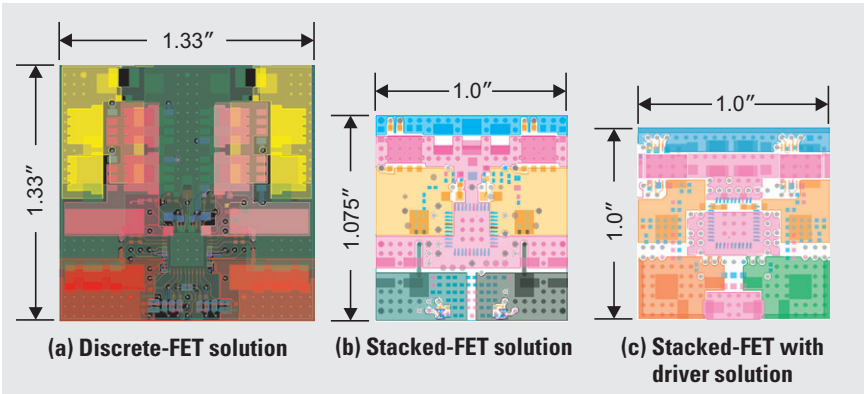
Advantages of stacked FET with integrated driver

A 1-V/60-A design solution was used to demonstrate the advantages of a stacked-FET switch with driver. This design was tested with a 12-V input, 1-V output and a 500-kHz switching frequency. The baseline solution used eight discrete FETs to supply the 60-A load current. As shown in Figure 6(a), the solution size is 1.33 by 1.33 inches.

In Figure 6(b), eight discrete FETs were replaced with two stacked FETs. The solution size now shrinks to 1 by 1.075 inches. This now results in a 40% size reduction from the discrete-FET solution.

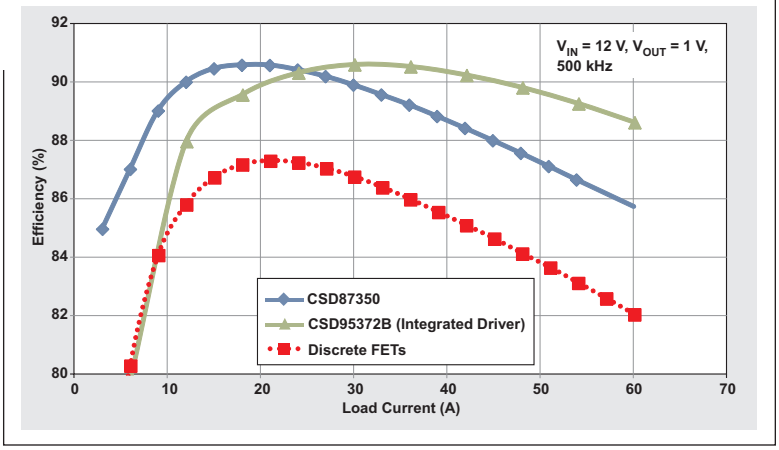
In Figure 6(c), two stacked-FET switches with driver also replaced eight discrete FETs. This solution size is 1 by 1 inch, or a 43% size reduction.

Figure 6. Three solutions for a 1-V/60-A supply



With the same test conditions applied to each design solution, the stacked-FET with driver solution achieves the highest efficiency of 88.6%. This is 6.6% higher than the discrete-FET efficiency and 2.9% higher at full load (60 A) than the stacked-FET solution without an integrated driver. Figure 7 shows the efficiency of the three different solutions. The green curve represents the stacked-FET with driver solution, the blue curve represents the stacked-FET solution, and the red curve represents a discrete-FET solution.

Figure 7. System efficiency is compared among three designs



Conclusion

The increasing efficiency and density requirements suggests that a high level of package integration is needed. Stacked-FET switches have silicon improvements and innovative packaging technologies that increase system efficiency. Likewise, by replacing a stacked-FET device with one that has an integrated driver, system efficiency further improves due to optimized driver and minimized parasitics.

Related Web sites

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Optimal operating point of an LED

By Donald Schelle
Analog Field Applications

Achieving optimal performance of an LED luminaire or LED backlight design requires numerous trade-offs. Understanding an LED's power transfer characteristics empowers intelligent choices regarding cost, power consumption, and weight. While most LED datasheets publish pertinent data that can be used to make these decisions, data may not be formatted in a way that is readily applicable to the chosen application. Optimal performance requires finding pertinent information from manufacturer's LED datasheets and utilizing methods to capture, reformat and analyze the data.

$$\#\mathrm{LED}_{min} > \underbrace{\frac{L_S^{\,2}}{K}\left(\frac{A_X \times A_Y}{A_X^{\,2} + A_Y^{\,2}}\right)}_{\text{Screen Area } (m^2)} \times \underbrace{M_{V(disp)}}_{\substack{\text{Max}\\ \text{Brightness}\\ \text{(nits)}}} \times \underbrace{\frac{1}{1 - V_{disp}}}_{\substack{\text{Lumped}\\ \text{Stackup}\\ \text{Losses}}} \times \underbrace{\frac{1}{\varphi_V}}_{\substack{\text{Lumen}\\ \text{Output of}\\ \text{Single LED}}} \quad (1)$$

Screen Size (inches) / Conversion Constant (inches² to m²); Aspect Ratio 16:9

A relevant case study involves a typical tablet LCD backlight application that drives a 10-inch display with a 16:9 aspect ratio. Driving the backlight, the LED chosen for our example is the Nichia NNSW208CT[1]. Typical displays in modern mobile devices emit approximately 650 nits of light when driven at maximum brightness. Most of the LED light produced is lost as it passes through the physical elements integrated into the display (light diffuser, polarizers, RGB color filter, touch-panel ITO, and so on). Modern display stack-ups loose approximately 95% of the light produced by the LED. This device in this case study emits 10.398 lumens when driven at the recommended continuous drive current of 25 mA. Calculate the minimum number of LEDs using Equation 1.

Using a conversion constant of K = 1550.0031 and the design requirements listed above, the calculated minimum number of LEDs is 35. While seven strings of five LEDs satisfies the design requirements, most LED driver ICs in this market are tailored to drive only six strings of LEDs. Adjusting the LED count to 36 enables an off-the-shelf LED driver. Assuming 100% driver efficiency, driving 36 LEDs at maximum brightness consumes 2.56 W of power.

LED efficacy, color shift, and thermal properties are key data metrics. Efficacy versus forward current is rarely provided in an LED datasheet. Tabulated efficacy data is also difficult to find in specifications. Calculating this key metric is relatively easy using available I_F versus V_F and luminosity versus I_F curves. Also required is a typical lumen output at a given I_F (8.4 lumens at I_F = 20 mA). All required data is readily available in the manufacturers' datasheets.

Start by importing/digitizing the datasheet graphs (Figure 1) into a spreadsheet using predefined increments of LED current. Free software tools speed the process and digitize Y data on pre-determined X increments[2], enabling the calculations required to derive efficacy.

Figure 1. Cornerstone plots used to derive the optimal LED operating point

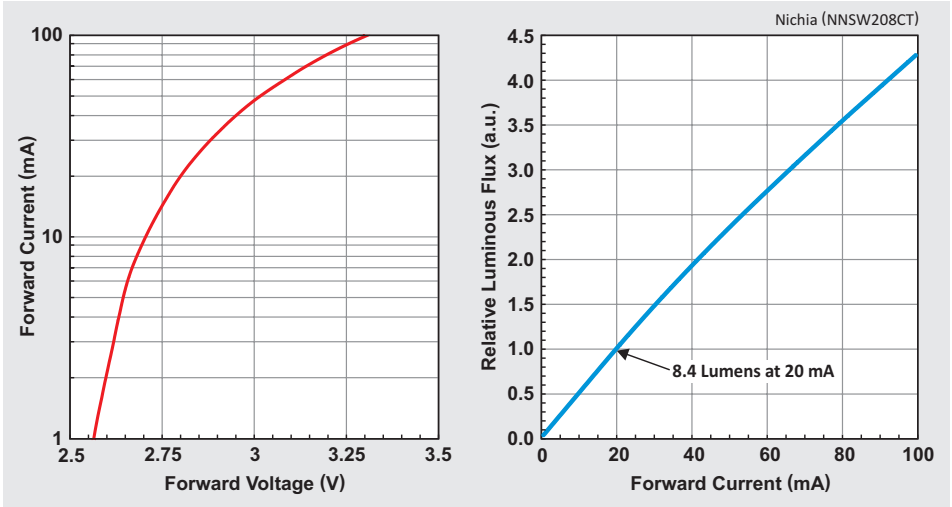
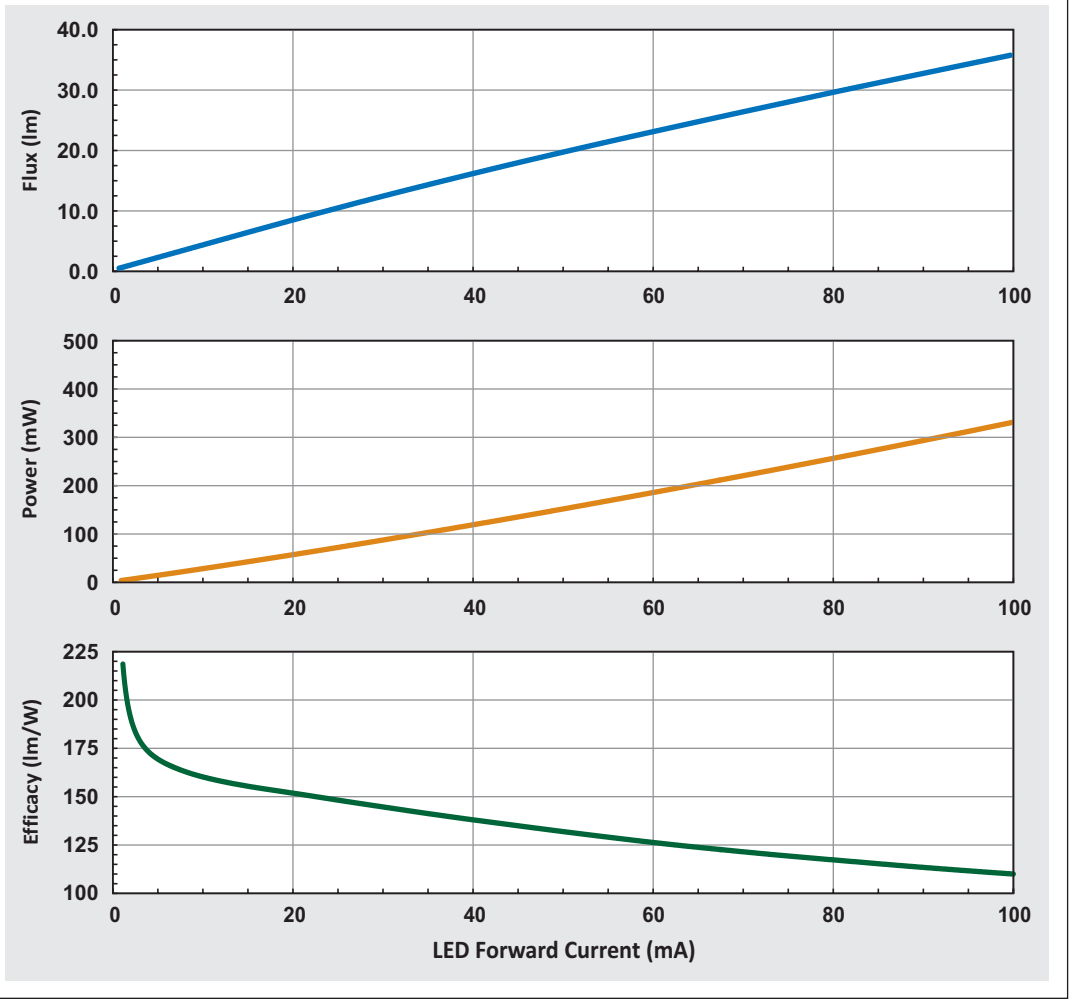


Figure 2. LED flux output, power consumption and efficacy can be calculated and plotted



Once digitized and tabulated, LED flux output (ΦV), LED power consumption (P_{LED}) and efficacy (η) are calculated versus LED forward current (I_F) (Figure 2). Peak efficacy is reached at a relatively low forward current and drops off steadily as forward current approaches the maximum rated amount.

Battery-powered applications greatly benefit by reducing these power requirements. Operating more LEDs at a lower forward current results in a net reduction of power for a given fixed-light output. Table 1 summarizes the original application requirements while comparing three alternative LED configurations.

Cost and mechanical volume requirements may limit the final configuration; however, doubling the number of LEDs yields a power savings of 160 mW. This equates to a 6.3% net power reduction. Additionally, the backlight can be operated at a much higher brightness (with increased power consumption) when ambient light conditions (outdoors/daylight) dictate a brighter image.

Table 1. A comparative backlight design study

Number of LEDs	LED Operating Point (mA)	Total Light Output (lm)	Total Power Consumption of LED Array (W)	Net Reduction in Operating Power (%)
Decreasing Number of LEDs				
24	32.6	373.2	2.65	–3.5
Control				
36	25	374.2	2.56	0
Increasing Number of LEDs				
42 (16%)	21.2	373.2	2.50	2.2
54 (50%)	16.4	374.1	2.45	4.1
72 (100%)	12.2	374.1	2.40	6.3

Figure 3 highlights the increasing power savings trend over a number of LED data points. Note that the LED knob turns both ways. Overdriving each LED decreases the total number required, yielding a less expensive display module; which is particularly beneficial when cost is crucial.

Operating the LEDs at a reduced brightness requires 100% duty cycle and a reduced current. Driving the LEDs using a traditional pulse-width modulation (PWM) architecture at maximum LED current yields no performance improvements.

White-point shift at lower currents is a perceived complication for backlight applications. Modern LEDs exhibit minimal to negligible color shift. Digitizing the LED's color-shift parametrics (Figure 4) and superimposing a MacAdam ellipse over the center of the operating range highlights this point. A one-step MacAdam ellipse encompasses all LED colors when operating between forward currents of 5 mA and 25 mA. Colors inside a one-step MacAdam ellipse are perceived as the same to the average observer.

Figure 3. LED power analysis shows lower power with greater number of LEDs

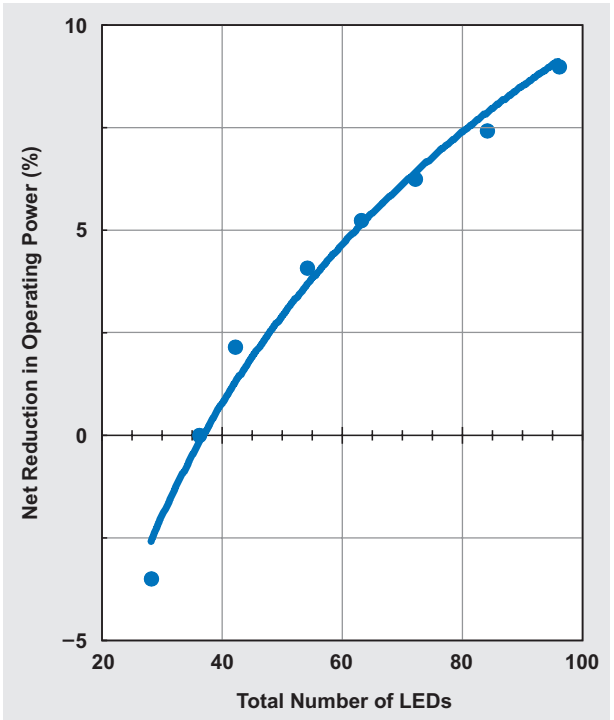


Figure 4. White point shift versus LED current

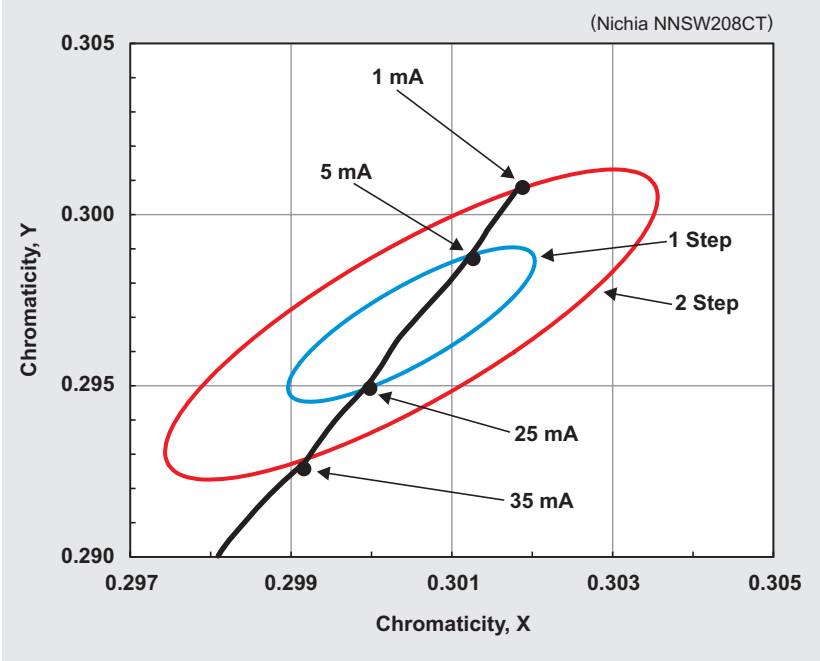
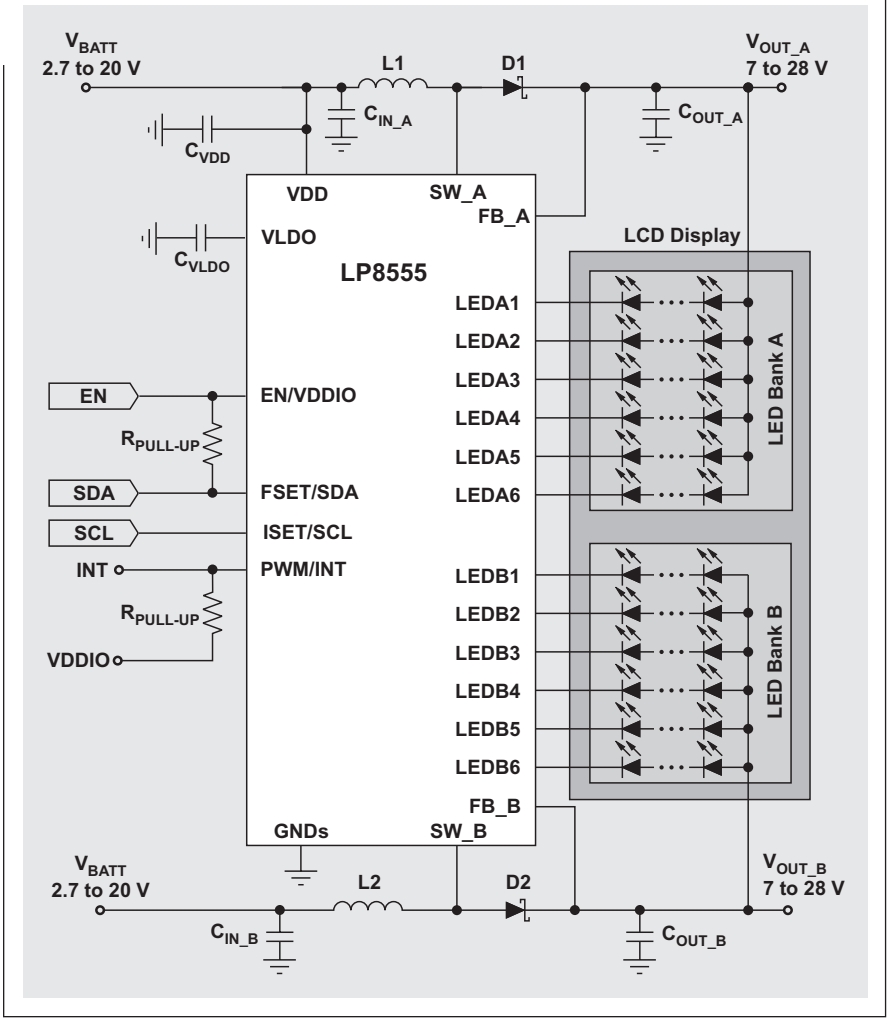


Figure 5. The LP8555 can power large matrices of LEDs



Powering a large array of LEDs is relatively easy using an LED driver such as the LP8555 (Figure 5). This device drives up to 96 LEDs, which is suitable for the largest of mobile displays and capable of driving all the configurations mentioned above. Two-percent string-to-string matching is a key metric to maintain a uniform image quality. A dual-boost architecture maximizes electrical efficiency while minimizing the physical height of the associated inductors. Additionally, this device features 12 current-sink inputs, enabling shorter series-LED strings. This allows the boost converters to power the LEDs at a more efficient electrical operating point. Key features such as adaptive dimming and content-adjustable backlight control (CABC) yield further electrical efficiency gains over all operating modes.

Conclusion

For maximum power savings, the key objective is to tailor the operating point of the LED to the most typical operating mode of the application. While LCD backlight applications have been the main focus, the concepts presented here can be easily applied to any LED lighting application that requires efficiency as a key performance metric.

References

1. Nichia NNSW208CT datasheet. Available : **www.nichia.co.jp/en/**
2. Donald Schelle, Mark Brouwer, "Digitize graphical data easily and accurately," *EDN*, March 2013. Available: **www.edn.com/**

Related Web sites

www.ti.com/1q15-LP8555

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