

## Routing the Middle Pins of the LP5562

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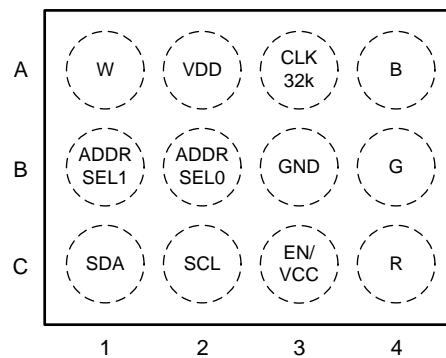


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Jussi Tikkanen

### ABSTRACT

The LP5562 is available in 12-bump DSBGA package with 0.4-mm pitch. This can be a limitation in cost sensitive applications as routing out the middle bumps separately requires HDI PCB technology which adds cost to the PCB manufacturing process.



**Figure 1. LP5562 Pinout Viewed From Top Side**

However, in most applications the middle pins can be routed via other pads thus avoiding use of microvias. This application report describes different configurations and example layouts.

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## 1 Overview of the LP5562 Pins used in this Report

### 1.1 ADDR0 and ADDR1

ADDR0 and ADDR1 pins are used to select the LP5562 I<sup>2</sup>C ID. [Table 1](#) lists ID combinations in 7-bit format, without R/W bit. ADDR pins must be connected to ground or positive supply (VDD or EN/VCC).

**Table 1. I<sup>2</sup>C ID**

ADDR0	ADDR1	I <sup>2</sup> C ID (7-bit)
0	0	30h
1	0	31h
0	1	32h
1	1	33h

### 1.2 CLK 32k

CLK\_32k is an external clock pin for supplying external 32-kHz clock to the LED engines. This can be used to synchronize multiple LP5562 devices or reduce standby mode power consumption. The LP5562 has also an internal 32-kHz oscillator which can be used but with increased typical power consumption of 0.24 mA. If this pin is not used, it must be connected to ground to avoid floating input.

### 1.3 LED Driver Pins W, R, G, and B

LED Driver pins W, R, G and B are internally connected to current sink (or low-side) type LED drivers. This allows connecting a driver pin to ground if it is not used.

### 1.4 VDD and GND

The VDD and GND pins are the positive power supply pin and ground pin of the device. These pins are always needed, and most of the routing examples in this report are based on different GND pin routing topologies. TI recommends using a decoupling capacitor to these pins.

## 2 Two-Layer Applications With an External Clock

Figure 2, Figure 3, Figure 4, and Figure 5 show different ways to do a two-layer layout in a system that uses external clock from the host. In Figure 3, Figure 4, and Figure 5, LED Driver pin G is used for routing the ground. This can be done if only three LED drivers are needed, for example if using an RGB LED.

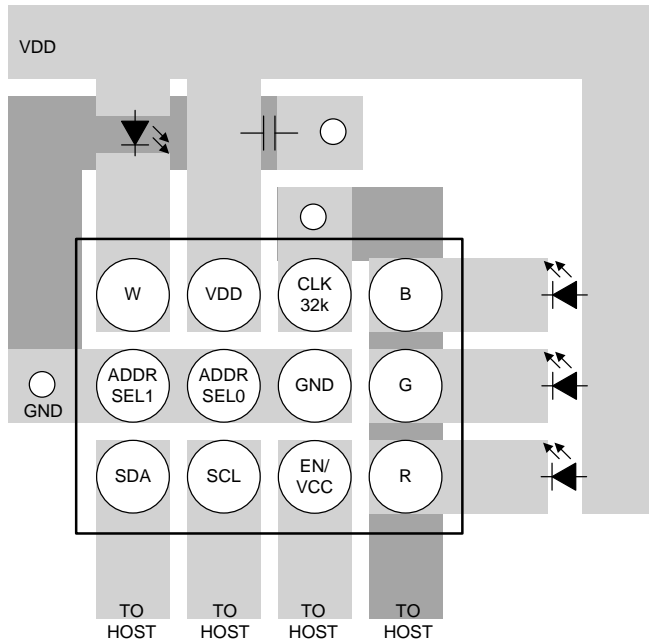


Figure 2. External Clock, I<sup>2</sup>C ID = 30h

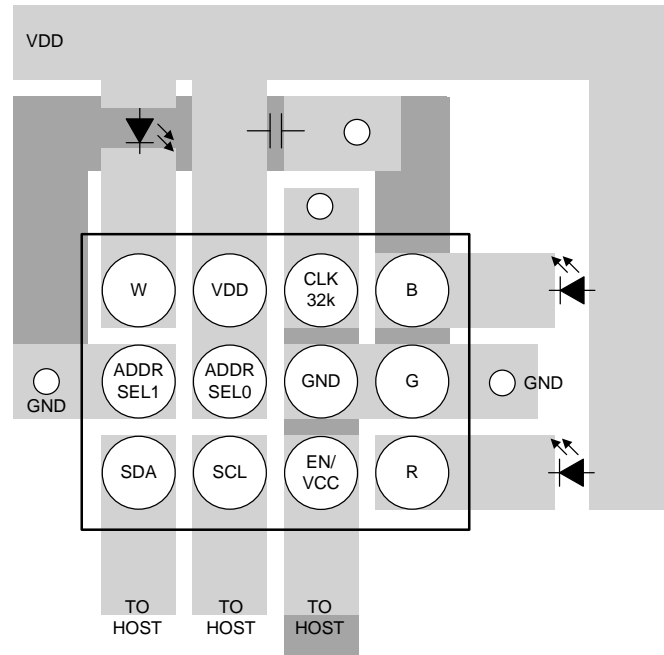


Figure 3. External Clock, I<sup>2</sup>C ID = 31h

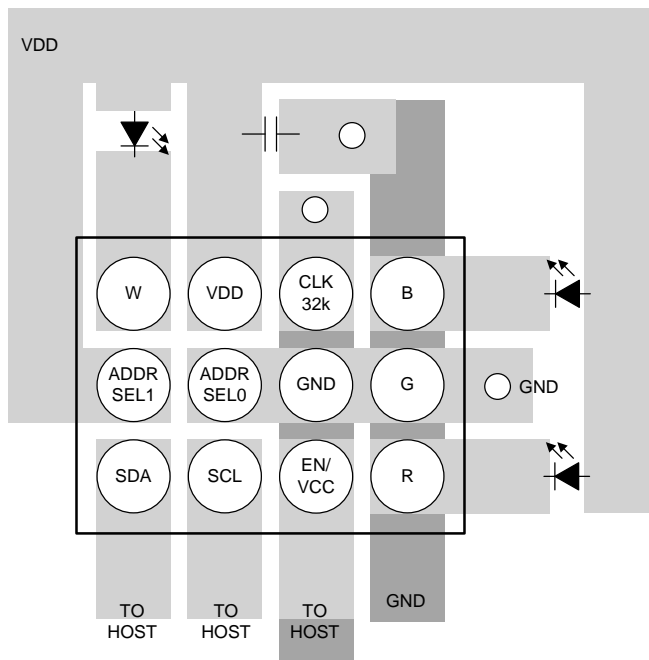


Figure 4. External Clock, I<sup>2</sup>C ID = 32h

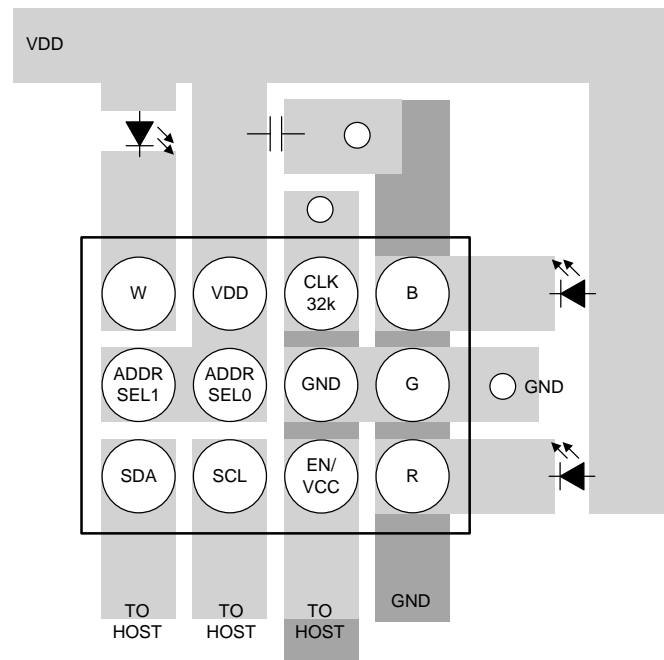


Figure 5. External Clock, I<sup>2</sup>C ID = 33h

### 3 Two-Layer Applications Without an External Clock

Grounding the external clock pin allows routing the ground via CLK\_32k pin in systems that don't use external clock feature. Figure 6, Figure 7, Figure 8, and Figure 9 show examples of how to route a two-layer board for the different I2C IDs.

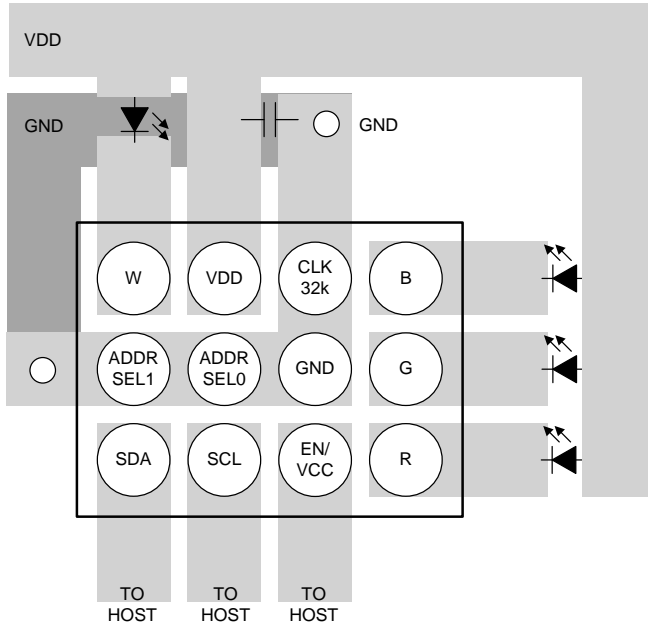


Figure 6. No External Clock, I<sup>2</sup>C ID = 30h

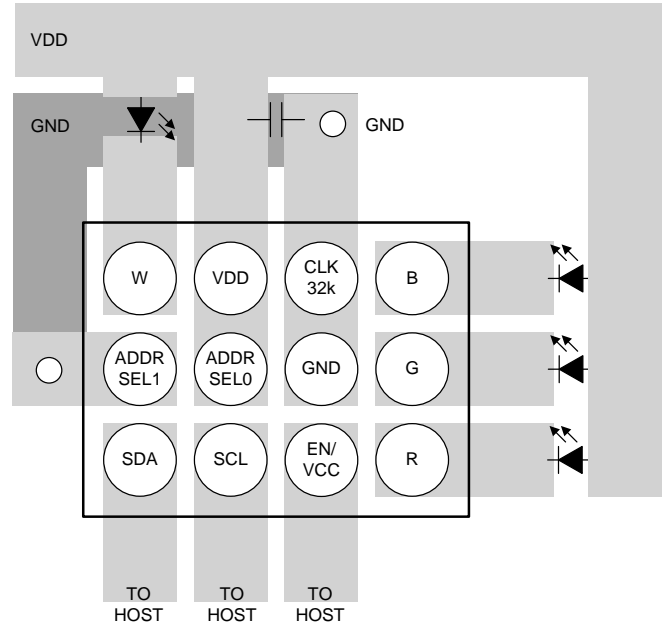


Figure 7. No External Clock, I<sup>2</sup>C ID = 31h

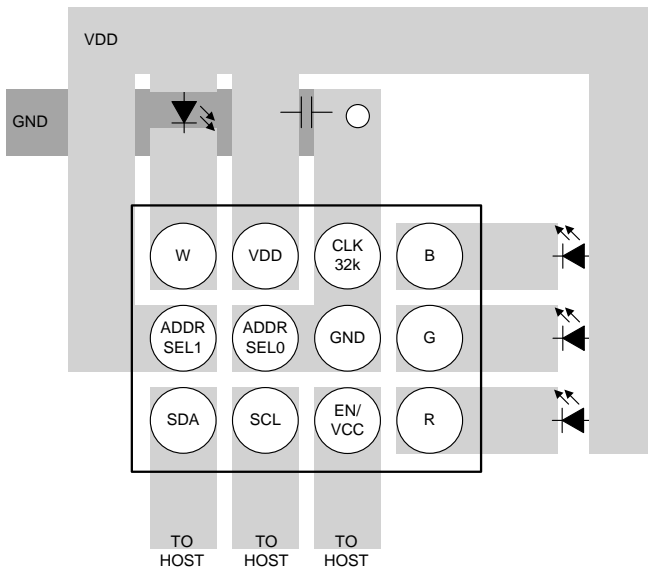


Figure 8. No External Clock, I<sup>2</sup>C ID = 32h

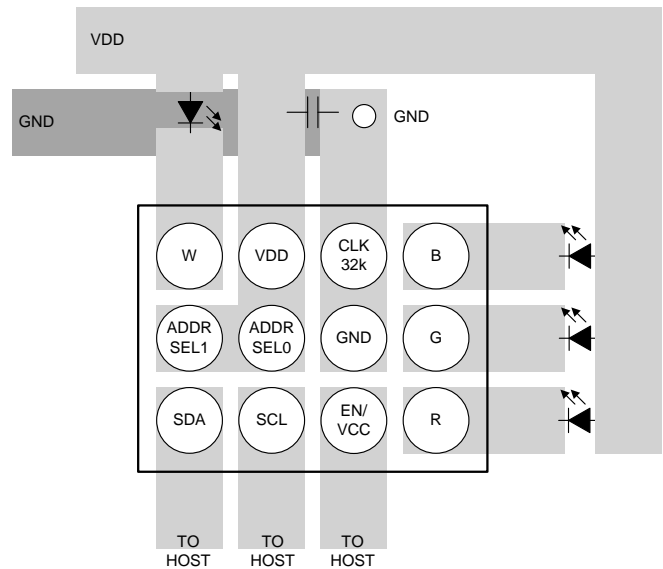


Figure 9. No External Clock, I<sup>2</sup>C ID = 33h

#### 4 Single-Layer Applications Without an External Clock

In some applications number of routing layer is limited to only a single PCB layer. [Figure 10](#), [Figure 11](#), [Figure 12](#), and [Figure 13](#) show examples of how to route ADDR pins by using only one layer. These all are based on previous examples without external clock, as it allows routing the ground through CLK 32k pin.

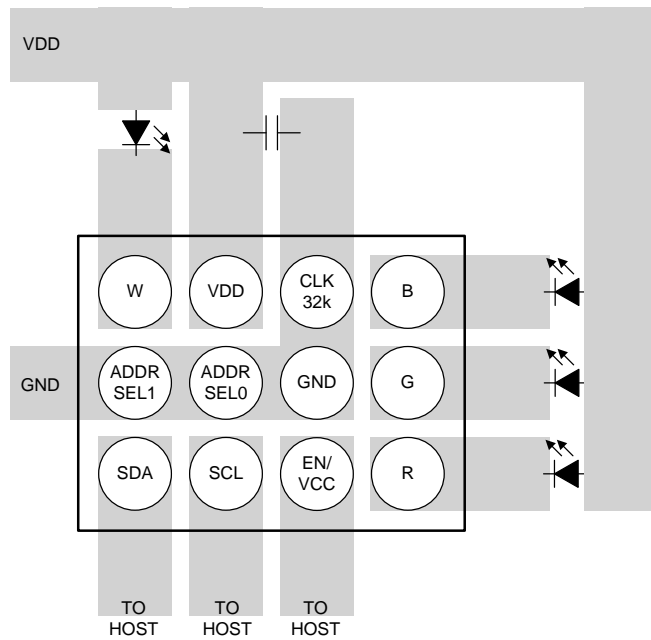


Figure 10. Single Layer, I<sup>2</sup>C ID = 30h

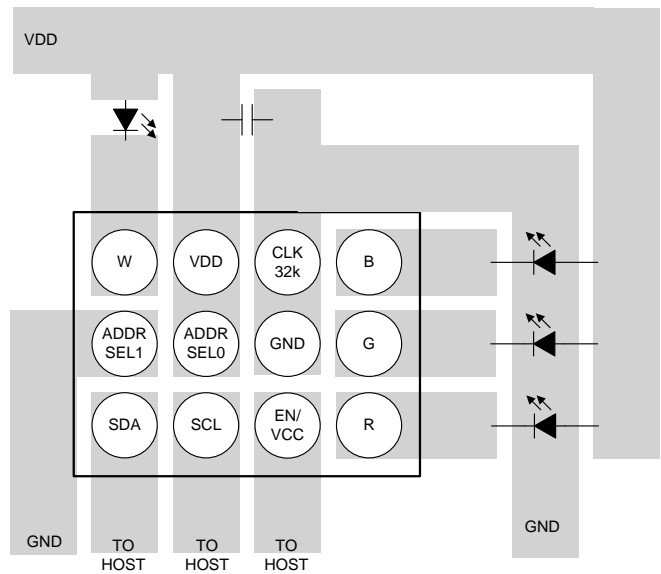


Figure 11. Single Layer, I<sup>2</sup>C ID = 31h

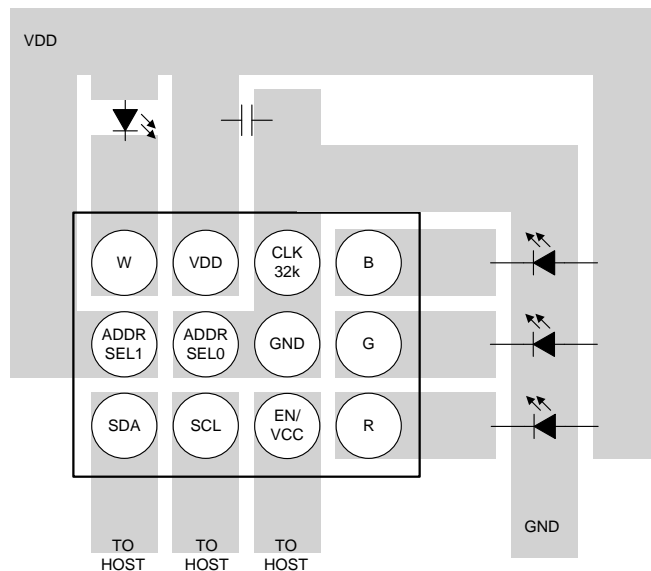


Figure 12. Single Layer, I<sup>2</sup>C ID = 32h

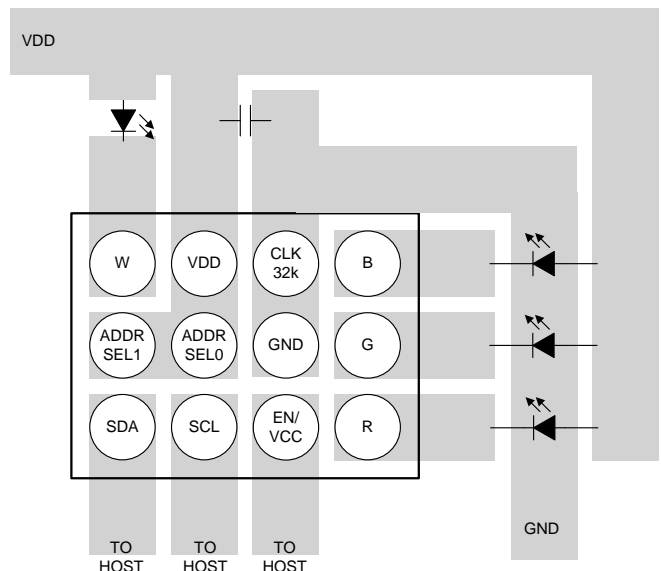


Figure 13. Single Layer, I<sup>2</sup>C ID = 33h

## 5 Summary

The LP5562 with 12-bump DSBGA package is also suitable for low-cost boards with only small limitations to pin usage in applications. Without an external clock it is also possible to use a single layer for routing the LP5562.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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