

# PV Inverter Design Using Solar Explorer Kit

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### ABSTRACT

This application report goes over the solar explorer kit hardware and explains control design of Photo Voltaic (PV) inverter using the kit.

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# 1 Introduction

The solar explorer kit, TMDSSOLAR(P/C)EXPKIT, (see Figure 1) provides a flexible and low voltage platform to evaluate the C2000<sup>™</sup> microcontroller family of devices for a variety of PV and solar power applications. The kit is available through the TI e-store (<u>http://www.ti.com/tool/tmdssolarpexpkit</u>).



Figure 1. TMDSSOLAR(P/C)EXPKIT

# WARNING

This EVM is meant to be operated in a lab environment only and is not considered by TI to be a finished end-product fit for general consumer use.

This EVM must be used only by qualified engineers and technicians familiar with risks associated with handling high voltage electrical and mechanical components, systems and subsystems.

This equipment operates at voltages and currents that can result in electrical shock, fire hazard and personal injury if not properly handled or applied. Equipment must be used with necessary caution and safeguards employed to avoid personal injury or property damage. appropriate

It is your responsibility to confirm that the voltages and isolation requirements are identified and understood, prior to energizing the board and or simulation. When energized, the EVM or components connected to the EVM should not be touched.

# 2 Getting Familiar With the Kit

# 2.1 Kit Contents

The kit follows the controlCARD concept and any device from the C2000 family with the DIMM100 controlCARD can be used with the kit. The kit is available with two part numbers: TMDSSOLARPEXPKIT and TMDSSOLARCEXPKIT. The TMDSSOLARPEXPKIT ships with the F28035 MCU controlCARD, which is part of the Piccolo<sup>™</sup> family in the C2000 MCU product line and TMDSSOLARCEXPKIT ships with the F28M35x controlCARD, which is part of the Concerto<sup>™</sup> family. Concerto devices are heterogeneous dual core devices, where one, C28x Core, handles the control of the power stage and the other core (ARM core) handles the communication such as USB, Ethernet.

The kit consists of:

- F28M3H52C controlCARD (TMDSSOLARCEXPKIT)
- F28035 controlCARD (TMDSSOLARPEXPKIT)
- Solar Explorer Baseboard
- 20 V 2 Amps Power Supply
- Banana Plug Cords (installed on the board)
- 50W 24Vac Light Bulb
- USB-B to A Cable
- USB mini to A Cable

The controlCARDs are pre-flashed to run with the respective graphical user interface (GUI) for a quick demo. All of the software projects are available for the kit through <u>controlSUITE</u>.

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### 2.2 Kit Overview

The solar panel or PhotoVoltaic (PV) panel, as it is more commonly called, is a DC source with a nonlinear V vs I characteristics.

A variety of power topologies are used to condition power from the PV source so that it can be used in variety of applications such as to feed power into the grid (PV inverter) and charge batteries. The Texas Instruments C2000 microcontroller family, with its enhanced peripheral set and optimized CPU core for control tasks, is ideal for these power conversion applications.

The solar explorer kit shown in Figure 2 has different power stages that can enable the kit to be used in a variety of these solar power applications. The input to the solar explorer kit is a 20 V DC power supply that powers the controller and the supporting circuitry. A 50W solar panel can be connected to the board (typical values Vmpp 17V, Pmax 50W). However, for quick demonstration of the power processing from the solar panel, a PV emulator power stage is integrated on the board along with other stages that are needed to process power from the panel. Using a Piccolo-A device integrated on the board lessens the burden of the controller used to control the solar power conditioning circuit control of the PV panel.

Thus, the board uses two C2000 controllers, a dedicated Piccolo-A device is present on the baseboard and used to control the PV emulator stage. The device on the DIMM100 controlCARD is used to control the DC-DC Boost, DC-AC and DC-DC Sepic stage.

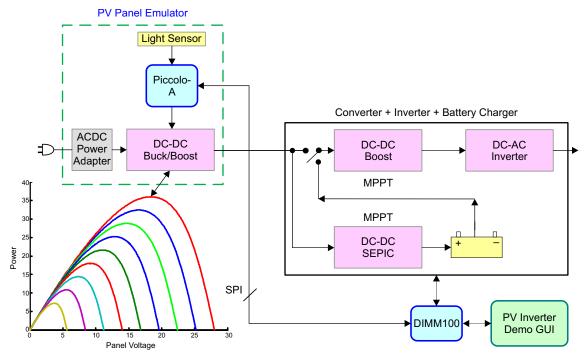


Figure 2. Solar Explorer Kit Overview

As PV is a light dependent source, a light sensor is integrated on the board, which can be used to change behavior of the panel with varying light conditions.



# 3 Power Stages on the Kit

To enable easy debug individual power stages have their input and output available as terminal blocks or banana jacks. With help of this macro-based approach in hardware, it is possible to realize different PV systems using the solar explorer kit.

### 3.1 Macros Location and Nomenclature

Figure 3 shows the location of the different power stage blocks and macros present on the board.

- TMDSSOLAREXPL Kit Main Board [Main] Consists of controlCARD socket, light sensor, relay, communications, instrumentation (DAC's) and routing of signals in between the macros and to the controlCARD.
- Boost DC-DC Single Phase with MPPT [M1] DC-DC macro accepts DC input that can be from the PV panel or a battery output (depending on system configuration), and boosts it. This block has the necessary input sensing to implement MPPT.
- Inverter Single Phase [M2] DC-AC macro accepts a DC voltage and uses a full bridge single phase inverter to generate a sine wave. The output filter, filters high frequencies, therefore, generating a smooth sine wave at the output.
- Sepic DC-DC with MPPT Battery Charging [M3] DC-DC macro accepts DC input from the PV panel and is used to charge a battery. The sepic stage provides both buck and boost capabilities that are necessary while charging the battery.
- Sync Buck Boost DC-DC Panel EMU [M4] DC-DC macro accepts DC input from the DC power entry macro (20 V typical) and uses it to generate the PV panel emulator output. The module senses the output voltage and current that makes emulation of the panel's V vs I characteristics possible.
- **Pic-A USB-mini EMU [M5]** This is a macro with the TMS320F28027 microcontroller and the JTAG emulator present to control and debug the M4 stage.
- DC-PwrEntry VinSw 12V 5V 3V3 [M6] DC power entry, used to generate the 12 V, 5 V and 3.3 V for the board from 20 V DC power supply supplied with the kit. This macro also supplies power for the onboard panel emulator, M4.
- ISO USB to JTAG [M7] JTAG connection to the main board.

Nomenclature: Components are referenced with the macro number in brackets, followed by the component label designator. For example, [M3]-J1 would refer to the jumper J1 located in the macro M3. Likewise, [Main]-J1 would refer to the jumper J1 located on the main board outside of any defined macro blocks.



Power Stages on the Kit

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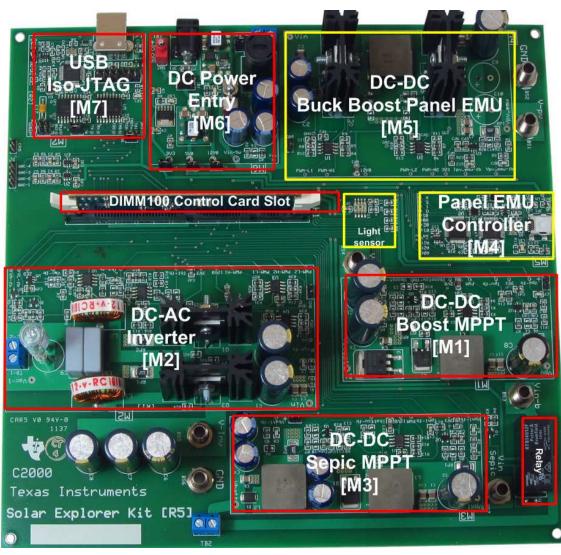


Figure 3. Macro Block on Solar Explorer Kit

The following section goes through the individual macros and the control scheme.



# 3.2 Boost DC-DC Single Phase With MPPT

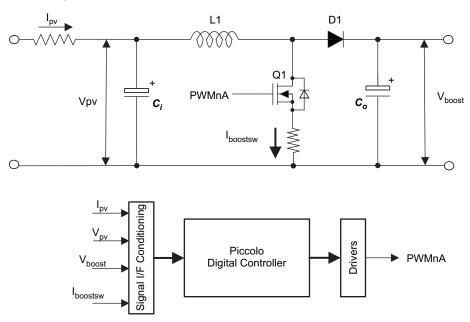


Figure 4. Boost DC-DC Single Phase With MPPT Power Stage

# 3.2.1 Power Stage Parameters

Input Voltage : 0 -30 V (Panel Input) Input Current : 0- 3.5 Amps (Panel Input) Output Voltage : 30 V DC Nominal Output Current: 0-2 Amps Power Rating: 50W fsw = 100 Khz

# 3.2.2 Control Description

The single phase boost stage is used to boost the voltage from the panel and track the MPP. The input current  $I_{pv}$  is sensed before the input capacitance  $C_i$  along with the panel voltage  $V_{pv}$ . These two values are then used by the MPPT algorithm, which calculates the reference point the panel input needs to be maintained at to be at MPP.

The MPPT is realized using an outer voltage loop and an inner current loop, as shown in Figure 5. Increasing the current reference of the boost (current drawn through the boost loads, the panel and resulting in the panel output voltage drop). Therefore, the sign for the outer voltage compensator reference and feedback are reversed. It is noted that the output of the boost is not regulated. To prevent the output voltage from rising higher than the rating of the components, the voltage feedback is mapped to the internal comparators, which can do a cycle-by-cycle trip of the PWM in case of over voltage.



### Power Stages on the Kit

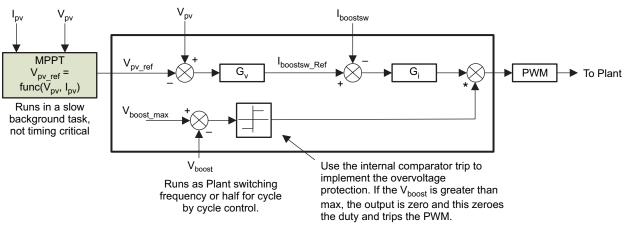
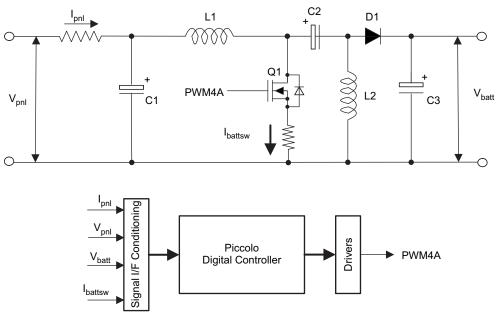


Figure 5. Boost With MPPT Control Diagram

# 3.3 DC-DC Battery Charging, Sepic





### 3.3.1 Power Stage Parameters

Input Voltage : 0 -30 V (Panel Input) Input Current : 0- 3.5 Amps (Panel Input) Output Voltage : 10V-16V DC max Output Current: 0-3.5 Amps Power Rating: 50W Max fsw = 200 Khz



### 3.3.2 Control Description

This stage is responsible for charging a typical 12 V battery from the solar panel and, therefore, has panel current  $I_{pv}$  and panel voltage  $V_{pv}$  sensing to track MPP. A sepic stage was chosen to realize this function, as both buck and boost operation are possible using the sepic stage. A typical lead acid battery charging can be divided into four stages, stage determination and transition is done as:

- Trickle Charging State: When the battery voltage is below a discharge threshold V<sub>chgenb</sub>, the battery has been deeply discharged or has shorted cells. In this case, the charging begins with a very low trickle current I<sub>tc</sub>. If the battery cells are shorted, then the battery voltage would remain below the V<sub>chgenb</sub>, preventing the charging state from going to the bulk charging stage. Otherwise, the battery voltage would slowly build up and would come within a nominal range (above V<sub>chgenb</sub>). At this stage, the state would move to bulk charging. While in trickle charging mode, MPPT may not be needed.
- Bulk Charging State: In this stage, the charger acts like a current source for the battery providing a constant current I<sub>bulk</sub>. As the PV may not be able to supply the ideal I<sub>bulk</sub> to charge the battery, however, it tries its best by operating at MPP. As the battery voltage exceeds 0.95 V<sub>oc</sub>, the charger enters the over charger mode.
- Over Charging State: The role of this state is to restore the full capacity in minimum amount of time at the same time avoiding over charging. All the battery voltage and current loop are enabled while MPPT is disabled. V<sub>Batt Ref</sub> now equals V<sub>oc</sub>. Initially, overcharge current equals bulk charge current, but as overcharge voltage is approached, the charge current diminishes. I<sub>Bref</sub> is determined by the voltage loop.
- Float Charge State: During this state, the battery voltage is maintained at V<sub>float</sub> to maintain battery capacity against self discharge. The charger would deliver as much current is needed for sustaining the float voltage. The battery would remain in the float state until the battery voltage drops below 90% of the float voltage due to discharging, at which point operation is reverted to bulk charging.

Typical values for 12V battery are:

Overcharge Voltage, V<sub>oc</sub> =15V

Floating Voltage, V<sub>float</sub> = 13.5V

Discharge Threshold,  $V_{chaenb} = 10.5V$ 

Load disconnect voltage, V<sub>Idv</sub> = 11.4

Load disconnect voltage, V<sub>Idv</sub> = 11.4

Figure 7 illustrates the control proposed for this stage when doing MPPT. The control when doing MPPT is similar to the boost stage; however, when the battery is not in the bulk charging stage, the MPP cannot be maintained as the battery cannot absorb the max power from the panel.

Hence, the control of the stage changes from the input voltage of the stage or output of the panel regulation to the output voltage of the stage regulation. The instance when the control is switched is dependent on the battery type and charging algorithm.



Power Stages on the Kit

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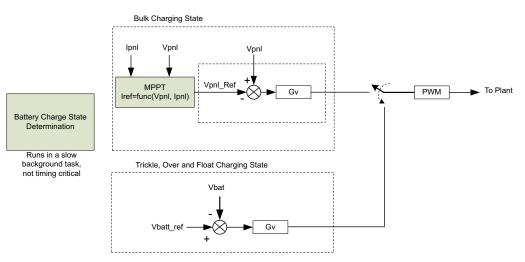
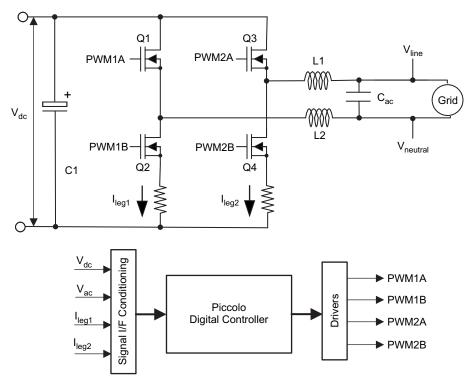


Figure 7. Battery Charging With MPPT Control Diagram

# 3.4 Single Phase Inverter





TEXAS INSTRUMENTS

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### 3.4.1 Power Stage Parameters

Input Voltage : 30 V DC Nominal

Input Current : 0- 2 Amps

Output Voltage : 20-24Vrms Max

Output Current: 0-2 Amps

Power Rating: 50W

fsw = 10 Khz-20 Khz

### 3.4.2 Control Structure

To appreciate the control of a full bridge inverter, first the mechanism of how the high frequency full bridge inverter feeds current into the grid and line needs to be understood. For this, an understanding of the PWM modulation scheme is necessary. The following derivations uses the unipolar modulation scheme to analyze the current fed from the converter.

In a unipolar modulation scheme, alternate legs are switched depending on which half of the sine of the AC signal is being generated.

- · Positive Half: SW1 and SW2 are modulated and SW4 is always ON, SW3 is always OFF
- Negative Half: SW3 and SW4 are modulated and SW2 is always ON, SW1 is always OFF

This modulation scheme is highlighted in Figure 9.



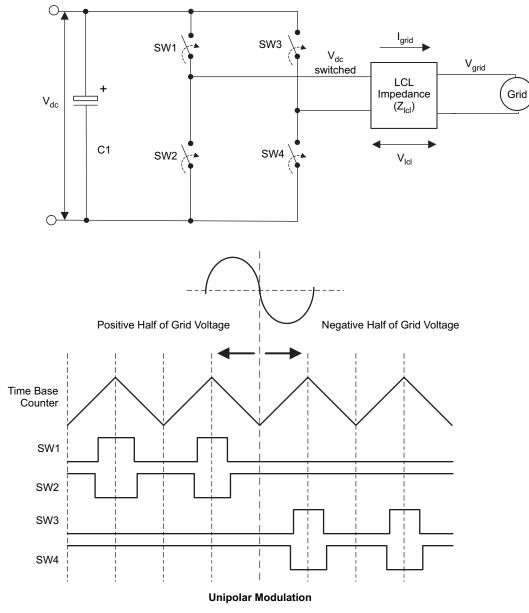


Figure 9. Modulation Scheme

The LCL filter at the output of the inverter filters this waveform. Now the voltage across the LCL filter can be written as:

- $V_{LCL,on} = V_{dc} V_{grid}$ , when SW1 and SW4 are conducting
- $V_{LCL,on} = -V_{dc} V_{grid}$ , when SW3 and SW4 are conducting
- $V_{LCL,off} = -V_{grid}$ , when SW2 and SW4 are conducting

Therefore, the change in grid current per switching cycle is computed shown in Equation 1:

$$\Delta i_{grid} = \frac{\left(V_{dc} - v_{grid}\right)D}{Z_{LCL}\left(F_{SW}\right)} + \frac{\left(0 - v_{grid}\right)\left(1 - D\right)}{Z_{LCL}\left(F_{SW}\right)} = \frac{V_{dc} * D - v_{grid}}{Z_{LCL}\left(F_{SW}\right)}$$

(1)

It is noted from Equation 1 that the current can be controlled by varying the duty cycle. Typically, a current transformer is used to measure the gird current. However, on the explorer kit, shunt current measurement is used as this is a learning platform.

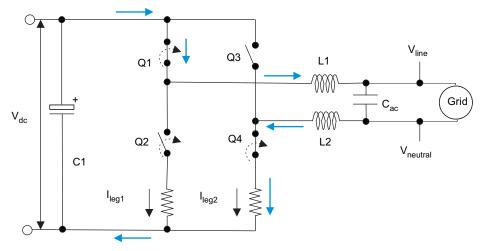


(2)

Two shunt current measurement resistors are placed, the grid current (that is, the current fed into the grid from the inverter) is estimated by subtracting the two leg currents.

$$\Delta i_{grid} = i_{leg2} - i_{leg1}$$

Assume the positive half of the sine wave feeds current into the grid.





Primary current fed into the grid during the positive half is  $i_{leg2}$ ,  $i_{leg1}$  and measures zero. However, when the current reference for the inverter is very low (Q1 is open most of the times), this can result in shorting the grid across SW2 and SW4. When shorted, a high current flows through both Leg1 and Leg2. This is why the Leg1 current is subtracted from the Leg1 current at all times to get the change in the grid current.

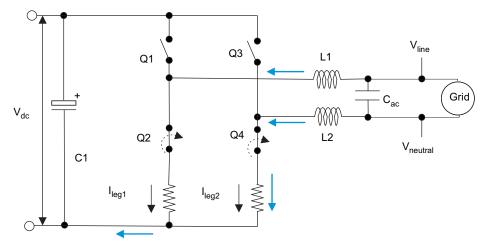


Figure 11. Shorting the Grid

Shorting the grid under low modulation case, then the negative current is not sensed.



Power Stages on the Kit

### 3.5 PV Emulator

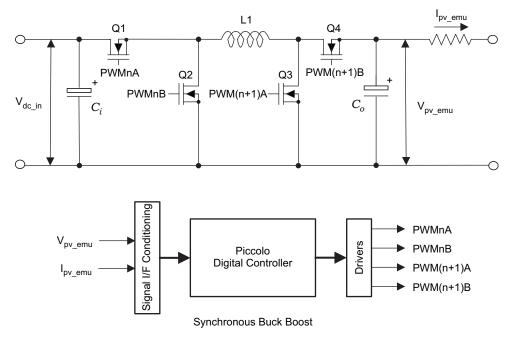


Figure 12. Synchronous Buck Boost

### 3.5.1 Power Stage Parameters

Input Voltage : 24 V, DC Power Supply

Input Current : 2.5 Amps Max , DC Power Supply

Output Voltage : 0-30 V DC Max

Output Current: 0-2.5 Amps

Power Rating: 50 W

fsw = 200 Khz

Note that the ratings mentioned above are maximum ratings, depending on the panel emulator characteristics the maximum ratings would be different.

### 3.5.2 Control Description

A synchronous buck boost stage is used to realize the PV array. The power stage comprises of buck side switches Q1 and Q2, boost side switches Q3 and Q4, an inductor L1 and input and output capacitor Ci and Co. The ideal DC gain of the stage is given by Equation 3:

$$G = \frac{V_0}{V_i} = \frac{D_{bu}}{1 - D_{b0}}$$

Where,  $D_{bu}$  is the duty of the buck stage and  $D_{bo}$  is the duty of the boost stage.

(3)



If the power stage is switched such that the buck and the boost duty are the same (that is,  $D_{bu}$  -  $D_{bo}$ ) the gain curve is as shown in Figure 13.

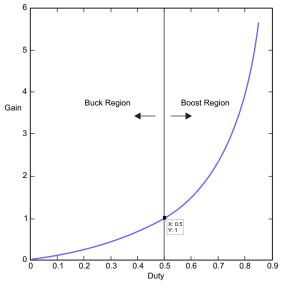
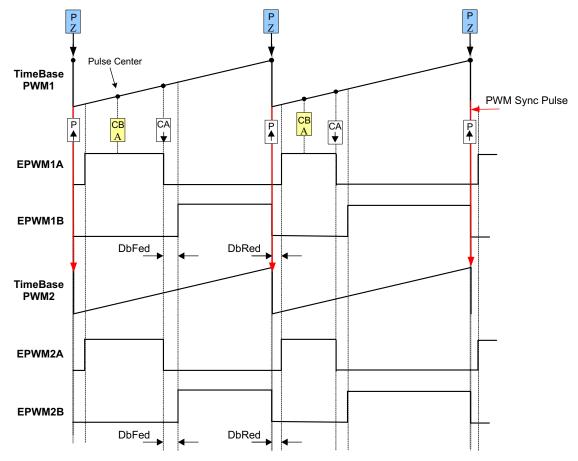


Figure 13. Gain Curve

Therefore, it can be concluded for duty less than 50% the stage behaves as a buck and 50% and above as a boost. The detailed switching diagram using C2000 PWM module is depicted in Figure 14.







Power Stages on the Kit

This stage is controlled using Piccolo-A (F28027), which is present on the EVM baseboard. This controller is separate from the controller that does the DC-DC boost, battery charging and the DC-AC conversion present on the board.

The input voltage to the buck boost stage is from the DC Power entry block. This voltage is 20 V, as the power adapter shipped with the kit is 20 V. However, you can use another voltage input by connecting it to the terminal block present on the board.

To emulate the panel characteristics, the stage needs to operate as a current controlled voltage source (depending on the load current demand, the output voltage will change). This is achieved by changing the voltage reference of the stage based on the look-up table value.

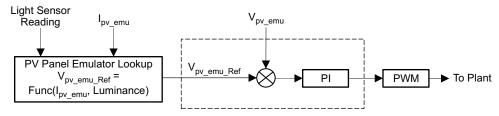


Figure 15. Light Sensor Panel

The current being drawn by the panel  $I_{pv}$  is used as the index for the look-up table that is stored on the controller. The look-up table is then used to provide the voltage reference  $V_{pv_ref}$  for the panel corresponding to the  $I_{pv}$ . A light sensor is placed on the board to control the irradiance level and produce a corresponding V-I curve. For getting curves between different luminance levels, the values from the stored curve are interpolated using Equation 4.

$$pv_ref_G2 = \frac{G2}{G1} * V_{pv_ref}$$

(4)

Where, G2 is the new luminance value and G1 is the old luminance value.

**NOTE:** This is just an approximation of the PV characteristics, the real panel characteristics may differ.

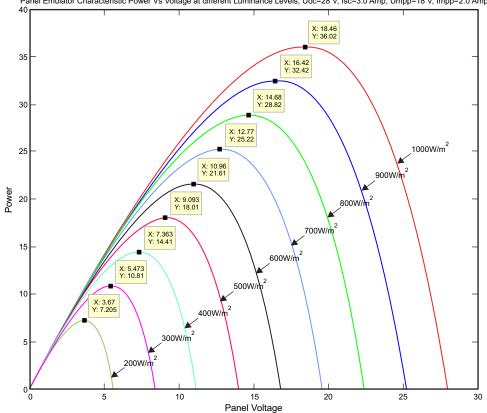
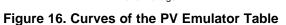


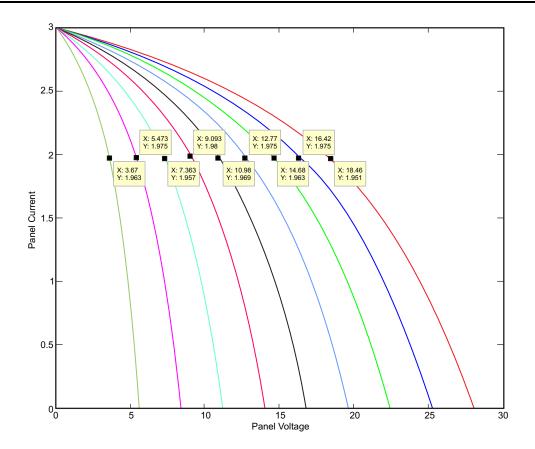
Figure 16 shows the curves of the PV emulator table that are stored for the PV emulation on the controller.



Т	able	1.	ΡV	Emulator	Table
-					

Luminance Ratio (w.r.t 1000W/m^2)	Pmpp =(Pmax * Luminance Ratio) Watts	Vmpp (Volts)
1.0 = 1000 W/m^2	36.02	18.46
0.9 = 900W/m^2	32.42	16.42
0.8 = 800W/m^2	28.82	14.68
0.7 = 700W/m^2	25.22	12.77
0.6= 600W/m^2	21.61	10.98
0.5=500W/^2	18.01	9.093
0.4=400W/m^2	14.41	7.363
0.3=300W/m^2	10.81	5.473
0.2=200W/m^2	7.205	3.67







### 3.6 DC Link Capacitor Requirement

In a PV inverter system, the DC-DC boost stage feeds the input to the inverter stage as the inverter provides an AC load that causes a 100-120Hz ripple (depending on the frequency of the AC load) on the DC bus of the inverter. A DC link capacitor is typically used to compensate for this power ripple. Figure 17 shows the relationship between this DC link capacitor and ripple on the DC Bus.

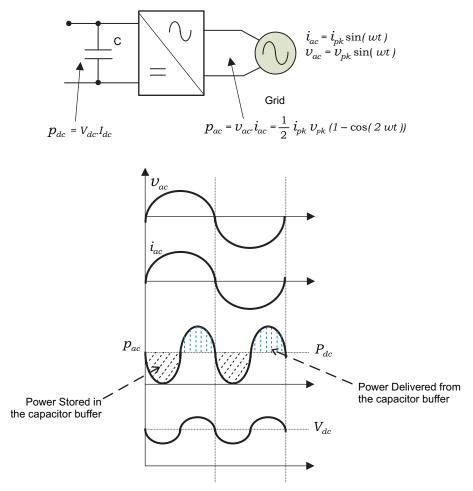


Figure 17. DC Link Capacitor and Ripple on the DC Bus

Let the AC current being fed to the grid or load and the AC voltage be:

•  $i_{ac} = I_{pk} sin(wt)$ 

which implies the power supplied by the inverter is:

$$p_{ac} = v_{ac} * i_{ac} = \frac{1}{2} V_{pk} I_{pk} \left[ 1 - \cos(2wt) \right]$$

(5)

In Equation 5, the power injected into a single-phase grid follows a sinusoidal waveform with twice the frequency of the grid. The PV module cannot be operated at the MPP if this alternating power is not decoupled by means of an energy buffer. Therefore, a capacitor bank is typically used for buffering this energy.

To estimate the amount of capacitance needed to buffer this energy, let the magnitude of the ripple induced on the DC bus due to the alternating nature of the power being drawn be  $\Delta V$ . Now Looking at a quarter of the sinusoidal power waveform, the equation for the power being drawn for 1/8th of the grid cycle can be written as follows:



PV Systems Using Solar Explorer Kit

$$\rho_{ac} = \frac{\Delta E}{\frac{1}{7}/8} = \frac{\frac{1}{2}CV^2 - \frac{1}{2}C(V - \Delta V)^2}{\frac{1}{(8*f_{ac})}} = 4*f_{ac}*C\left(V^2 - (V - \Delta V)^2\right)$$

(6)

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As is clear from Equation 6, the minimum capacitance required is a function of the value of voltage this energy buffer is kept at and the AC power delivered.

# 4 PV Systems Using Solar Explorer Kit

PV energy can be utilized in a wide variety of fashion, from powering street lights, feeding current into the grid, powering remote base stations, and so forth. The solar explorer kit can be used to experiment with a variety of these applications.

# 4.1 PV DC-DC Systems

PV powered street lighting, parking stations and thin clients are all part of DC-DC applications for which PV can be used. Figure 18 depicts a PV powered street light configuration that can be experimented with the solar explorer kit.

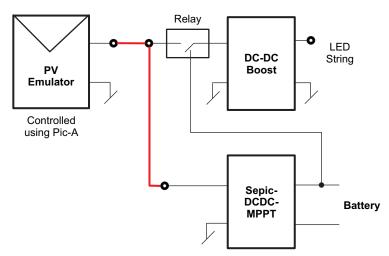


Figure 18. DC-DC PV Street Lighting

**NOTE:** The idea is not to illustrate the most optimal power stage, but to illustrate the control of such a system using C2000 MCU's.

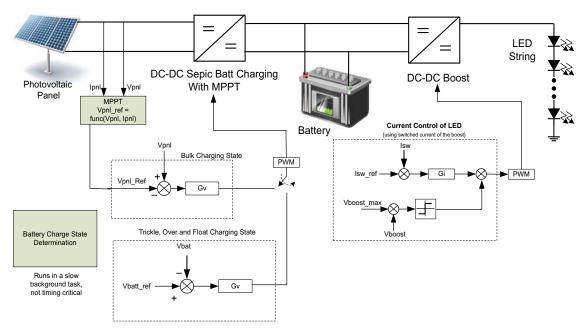


Figure 19. Control of PV Street Light With Battery Charging

# 4.2 PV Grid Tied Inverter

PV energy can be fed into the grid using a current control inverter. A typical PV grid tied inverter uses a boost stage to boost the voltage from the PV panel such that the inverter can feed current into the grid. The DC bus of the inverter needs to be higher than the maximum grid voltage. Figure 20 illustrates a typical grid tied PV inverter using the macros present on the solar explorer kit.

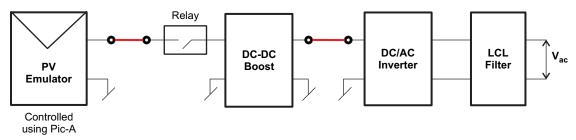


Figure 20. PV Grid Tied Inverter

The DC-DC stage is responsible to maintain MPPT of the panel and the inverter is responsible for the synchronization with the grid and feeding current into the grid. Figure 21 shows the control of a PV inverter stage.



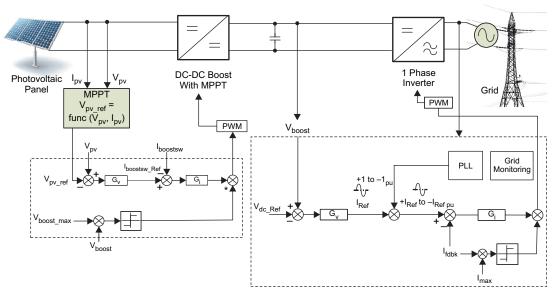


Figure 21. Control of PV Grid Tied Inverter

# 4.3 PV Off Grid Inverter

PV energy is not a steady source of energy. In daytime, the PV generates power, whereas, at night, it does not generate any power. A power storage element is needed for PV to supply power to a standalone installation. This is done with the help of a battery charging stage. Such a system can be realized using the solar explorer kit as shown in the Figure 22.

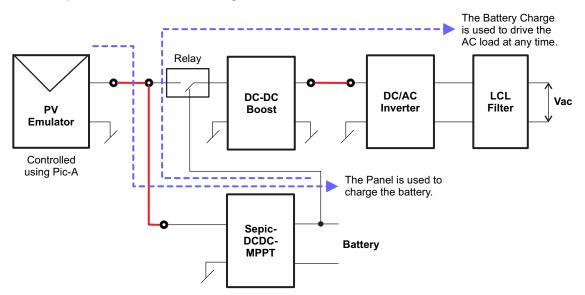


Figure 22. PV Off Grid Inverter System



# 5 Hardware Details

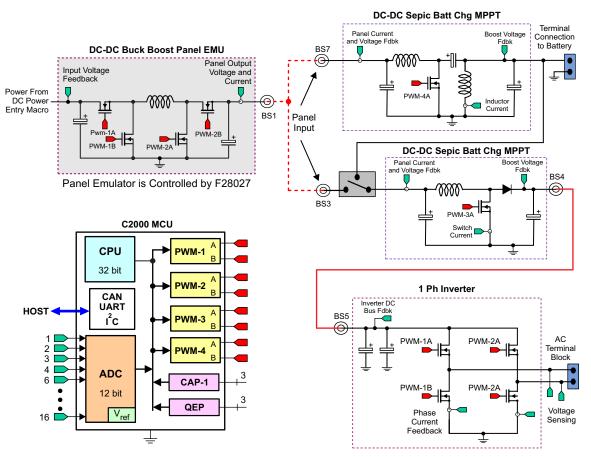
### 5.1 Resource Allocation

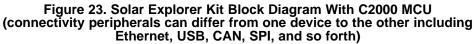
Figure 23 shows the various stages of the board in a block diagram format and illustrates the major connections and feedback values that are being mapped to the C2000 MCU. Table 2 lists these resources; however, it only lists the resources used for power stages that convert power from the panel and that are mapped to the DIMM100 connector on the board, and not of the panel emulation stage.

Macro Name	Signal Name	PWM Channel/ADC Channel No/Resource Mapping F2803x	PWM Channel/ADC Channel No/ Resource Mapping F28M35x	Function
Single Phase Inverter	PWM-1L	PWM-1A	PWM-1A	Inverter drive PWM
	PWM-1H	PWM-1B	PWM-1B	Inverter drive PWM
	PWM-2L	PWM-2A	PWM-2A	Inverter drive PWM
	PWM-2H	PWM-2B	PWM-2B	Inverter drive PWM
	lleg1-fb	ADC-A4	ADC1-A4	Leg1 Current
	lleg2-fb	ADC-A6	ADC1-A6	Leg2 Current
	VL-fb	ADC-B1	ADC2-B0	Line Voltage Feedback
	VN-fb	ADC-A5	ADC1-B4	Neutral Voltage Feedback
	Vac-fb	ADC-A7	ADC1-A7	AC Voltage Feedback
	VdcBus-fb	ADC-A3	ADC1-A3	DC Bus Voltage Feedback
	ZCD	ECAP1	ECAP1	ZCD Capture
DC-DC Single Phase Boost With MPPT	PWM	PWM-3A	PWM-3A	Boost PWM
	Vpv-fb	ADC-A1	ADC1-B0	Panel Voltage Feedback
	lpv-fb	ADC-A0	ADC1-A0	Panel Current Feedback
	Iboostsw-fb	ADC-B6	ADC2-A6	Boost Switched Current
	Vboost-fb	ADC-A2	ADC1-A2	Boost Voltage Feedback
DC-DC Sepic With MPPT	PWM	PWM-4A	PWM-4A	Sepic PWM
	Vpnl-fb	ADC-B2	ADC2-A2	Panel Voltage Feedback
	Ipnl-fb	ADC-B3	ADC2-A3	Panel Current Feedback
	Ibattsw-fb	ADC-B7	ADC2-A7	Battery Switched Current
	Vbatt-fb	ADC-B4	ADC2-A4	Battery Voltage
Main-Board	RLY-en	GPIO-12	GPIO-12	Relay Switch
	Light-fb	ADC-B0	ADC2-A0	Light Sensor Feedback
	PWM	PWM-5A	PWM-5A	DAC-1
	PWM	PWM-6A	PWM-6A	DAC-2
	PWM	PWM-7A	Not Available	DAC-3
	PWM	PWM-7B	Not Available	DAC-4
	SPISOMI-B	SPISOMI-B	SSI	Comm. to PV Emu
	SPISIMO-B	SPISIMO-B	SSI	Comm. to PV Emu
	SPISTE-B	SPISTE-B	SSI	Comm. to PV Emu
	SPICLK-B	SPICLK-B	SSI	Comm. to PV Emu
	Tx-slave	SCITX-A	Not used	Comm. to SCI GUI
	Rx-slave	SCIRX-A	Not used	Comm. to SCI GUI

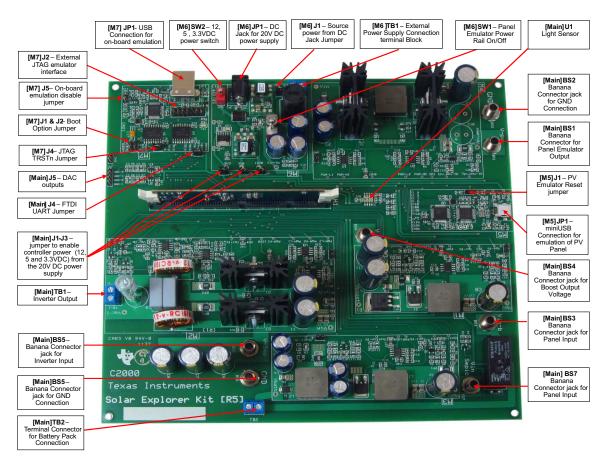
Table 2. Resource Mapping: PWM, ADC, GPIO, Comms













### 5.2 Jumpers and Connectors

Table 3 shows the various connections available on the board, and is split up by the macro each connection is included in. Figure 24 illustrates the location of these connections on the board with help of a board image.

[Main]-BS1	Banana jack for panel emulator output connection		
[Main]-BS2, BS6	Banana jack for GND connection		
[Main]-BS3, BS7	Banana jack for panel input connection		
[Main]-BS4	Banana jack for boost voltage connection		
[Main]-BS5	Banana jack for connecting the input to the DC-AC inverter, typically this is the boost output an input voltage		
[Main]-H1	DIMM100 connector, used to insert the C2000 MCU controlCARD		
[Main]-TB2	Terminal block for output of Sepic stage[M3], used to connect to battery pack		
[M2]-TB1	Inverter output voltage connection terminal block		
[M6]-JP1	DC power jack, input connection from the DC power supply		
[M6]-SW1	Switch to enable or disable power to the PV emulator stage. When in the ON position, 20 V from the DC power entry macro goes to the panel emulator stage.		
[M6]-SW2	Switch to enable or disable power to the board. When in the On position, the input voltage is used to generate 12 V, 3.3 V and 5 V rail on the board. Also, if the [M6]-J1 jumper is populated, the power from the DC jack is also used for the power rail of the panel emulator stage.		

Table 3. Jumpers and Connectors	on Solar Explorer Board
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Software

Table 5. bumpers and bonneetors on bolar Explorer Board (continued)			
[M6]-J1	When the jumper is populated, the power for the PV emulator stage is the input of the DC power jack [M6]-JP1. When unpopulated, a separate external power supply can be connected to [M6]-TB1 to source power for the panel emulator stage.		
[M6]-TB1	External power supply connection for the PV emulator. The PV emulator can source power from the 20 V power supply that feeds into [M6]-JP1; however, if it is desired, an external power supply can be connected to [M6]-TB1 that will separate the DC Link from the controller power. When using external power supply, [M6]-J1 needs to be depopulated.		
[M7]-JP1	USB connection for on-board emulation		

### Table 3. Jumpers and Connectors on Solar Explorer Board (continued)

# 5.3 GUI Connection

The FTDI chip present on the board can be used as an isolated SCI for communicating with a HOST (that is, PC). The following jumper settings must be done to enable this connection.

As the GUI software with SCI is provided for F28035 controlCARD only, F28035 settings are discussed below:

- 1. Populate the jumper [M7]-J4
- 2. Remove the jumper [Main]-J4, this disables the JTAG connection.
- 3. Put SW3, on the F28035 controlCARD, to the OFF position.
- 4. Connect a USB cable from [M7]-JP1 to the host PC.

### 6 Software

This section describes the details of the PV inverter control and software for the solar explorer kit.

### 6.1 Project Framework

As shown earlier, the PV inverter control requires two real-time ISR's: one is for the closed loop control of the DC-DC stage and the other for the closed loop control of the DC-AC stage. The C2000 Solar Explorer Kit project makes use of the "C-background/C-ISR/ASM-ISR" framework. The fast ISR (100 kHz), controlling the DC-DC Boost stage, runs in assembly environment using the digital power library and slower ISR (20 kHz), controlling the DC-AC inverter, is run from the C environment. This DC-AC ISR is made interruptible by the DC-DC ISR. The project uses C-code as the main supporting program for the application and is responsible for all system management tasks, decision making, intelligence, and host interaction.

**NOTE:** If you are going to boot from Flash and connect using the GUI, you would need to use the Boot from Flash settings as described in the Table Boot Options.



Figure 25 shows the structure of the PV inverter software, with the main background loop, the DC-DC ISR and the DC-AC ISR.

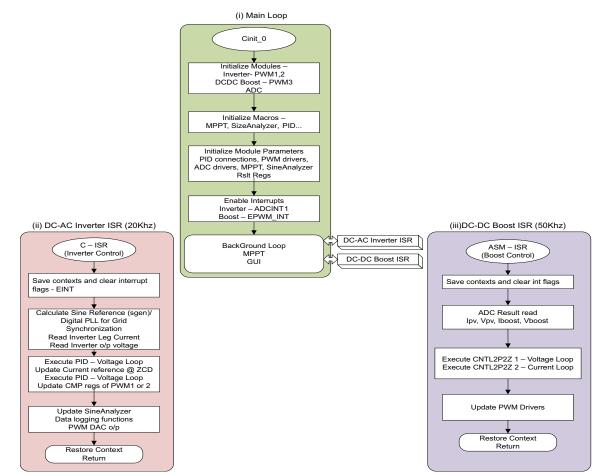


Figure 25. PV Inverter Software Structure (i) Main Loop (ii) Inverter Stage ISR (iii) DCDC Boost Stage ISR

# 6.2 DC-DC Boost With MPPT Control Software

To get the most energy out of the solar panel, the panel needs to operate at its maximum power point. However, the maximum power point is not fixed due to the non linear nature of the PV cell and changes with temperature, light intensity, and so forth. Thus, different techniques are used to track the maximum power point of the panel, like Perturb and Observe, incremental conductance algorithms. These techniques try to track the maximum power point of the panel under given operating conditions and are referred to as Maximum Power Point Tracking (MPPT) techniques and algorithms. The Solar Explorer kit has a front-end boost converter to boost the input voltage from the solar panel to a suitable level for the inverter and track the MPP.

The control of the stage to track the MPP was discussed earlier; for which the input voltage  $(V_{pv})$  and input current  $(I_{pv})$  are sensed. The boost converter is a traditional single phase converter with a single switching MOSFET Q1. The duty cycle of the PWM output driving the Q1 MOSFET switch determines the amount of boost imparted and is the controlled parameter. The MPPT is realized using nested control loops, an outer voltage loop that regulates input DC voltage  $(V_{pv})$  and an inner current loop that controls the current of the boost stage. Increasing the current reference of the boost, that is, current drawn through the boost loads the panel and hence results in the panel output voltage drop. Therefore, the sign for the outer voltage compensator reference and feedback are reversed. The current and voltage controllers are executed at a rate of 50 kHz (half of the PWM switching frequency) while the MPPT controller is executed at a much



slower rate ~ 10Hz. It is noted from Figure 5 that the boost stage output voltage is not being controlled through software. Boost output voltage however is regulated by the DC-AC inverter, which modulates the current drawn by the inverter to keep this voltage regulated. However, for protection, the output of the boost is connected to the ADC pin with the internal comparator that can be used to trip the PWM to the DC-DC stage in case of over-voltage.

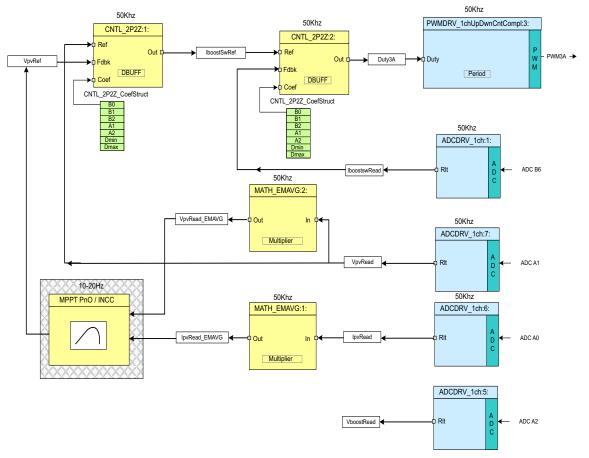


Figure 26. DC-DC 1ph Boost With MPPT Software Diagram

As the switching rate of the DC-DC stage is fairly high, 100 Khz, the control ISR for the DC-DC is implemented in an optimized assembly ISR (ASM – ISR) that uses components from the digital power library. In the PV inverter project, the DC-DC ISR is invoked every alternate switching cycle; this is done because the PV panel output does not change very fast. Figure 26 shows the software diagram for the DC-DC stage using the optimized blocks from the digital power library.

The ADC result registers are read by the ADCDRV\_1ch block and converted to normalized values, and stored in variables I<sub>pvRead</sub>, V<sub>pvread</sub>, I<sub>boostswread</sub> and V<sub>boostread</sub>. Two 2-pole 2-zero controllers (CNTL\_2P2Z) are used to close the inner DC-DC boost current loop and the outer input voltage loop. The MPPT algorithm provides reference input voltage to the boost stage to enable panel operation at maximum power point. The sensed input voltage is compared with the voltage command (V<sub>pvref</sub>) generated by the MPPT controller in the voltage control loop. The voltage controller output is then compared with the output current (I<sub>boostswread</sub>) feedback in the current controller. The current loop controller's output decides the amount of duty to be imparted to the PWM so as to regulate the input voltage indirectly. The PWMDRV\_1ch\_UpDwnCntCompl block is used to drive the DC-DC stage. The panel current and voltage are filtered using the MATH\_EMAVG block; this is done to remove any noise on the panel current and voltage sensing that may confuse the MPPT algorithm.



Notice the color coding for the software blocks. The blocks in 'dark blue' represent the hardware modules on the C2000 controller. The blocks in 'blue' are the software drivers for these modules. The blocks in 'yellow' are the controller blocks for the control loop. Although a 2-pole 2-zero controller is used here, the controller could very well be a PI/PID, a 3-pole 3-zero or any other controller that can be suitably implemented for this application. Similarly for MPP tracking, you can choose to use a different algorithm.

# 6.3 DC-AC Single Phase Inverter Control Software

The inverter stage gets input from the DC-DC boost stage and the inverter converts DC into AC. For a full bridge inverter, it can be noted that when using unipolar modulation the current fed is given by Equation 7:

$$\Delta i_{grid} = \frac{(V_{dc} - v_{grid}).D}{Z_{LCL}(F_{sw})} + \frac{(0 - v_{grid})(1 - D)}{Z_{LCL}(F_{sw})} = \frac{V_{dc} * D - v_{grid}}{Z_{LCL}(F_{sw})}$$

(7)

Where, D is the duty cycle.

It is clear from Equation 7 that for the inverter to be able to feed current into the grid, the Vdc must always be greater than the max grid voltage. Also, it is known from the PV inverter control scheme that the DC bus is not regulated by the DC-DC boost stage. Therefore, the inverter stage software uses nested control loops: an outer voltage loop and an inner current loop. The voltage loop generates the reference command for the current loop, as increasing the current command will load the stage and hence cause a drop in the DC bus voltage the sign for reference and the feedback are reversed. The current command is then multiplied by the AC angle to get the instantaneous current reference. In the case of "off-grid" configuration, sine reference is generated using the SGEN library function, which provides the angle value, whereas, for the grid connected software PLL provides the grid angle. The instantaneous current reference is then used by the current compensator along with the feedback current to provide duty cycle for the full bridge inverter. The outer voltage loop is only run at ZCD of the AC to prevent any distortion in the current.

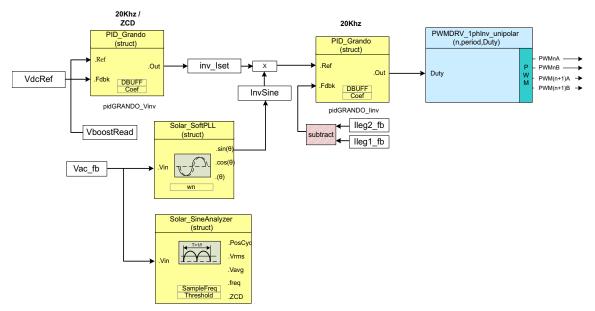


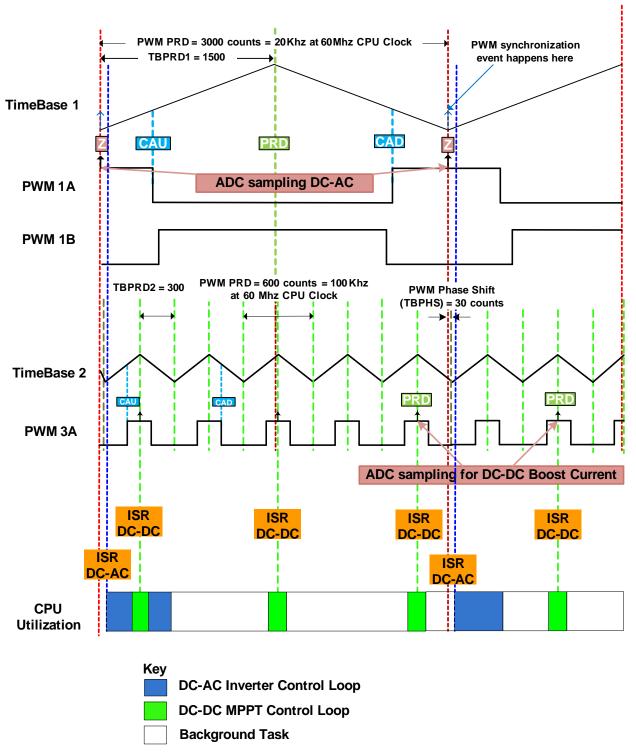
Figure 27. Closed Loop Current Control for DC-AC With Grid Connection



### 6.4 DC-DC and DC-AC Integration

As shown in Figure 25, the PV inverter control requires two real-time ISR's: one is for the closed loop control of the DC-DC stage (100 Khz) and the other for the closed loop control of the DC-AC stage (20 Khz). The peripheral, that is, ADC and PWM's on the C2000 device family have been designed to integrate multi frequency control loops and ensure sampling at correct instances of the PWM waveform. However, as only one ADC present (two sample and holds) it needs to be ensured that the multi-rate ISRs do not conflict for the ADC resource at any instance. For this, the phase shift mechanism of the PWM's on the ePWM peripheral is employed. Figure 28 illustrates the timing diagram for configuring the EPWM for the inverter and the boost stage and the synchronization mechanism used to avoid ADC conflicts.





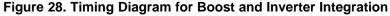


Figure 28 illustrates the PWM waveform generation on a 60 MHz device for 20 KHz DC-AC inverter and a 50 KHz control loop rate of the DC-DC boost with MPPT stage (note the switching rate is 100 KHz). The PWM peripheral offers the flexibility to trigger the start of conversions (SOC's) for the ADC every switching cycle or alternate, avoiding any unnecessary load on the ADC.



Software

In addition to this, a phase shift is implemented to avoid any conflict on the ADC resource. A phase shift of 30 clock cycles is chosen to account for a 7 cycle sampling window and a 15 cycle first conversion delay.

### 6.5 Incremental Build Level System

The software project for the Solar Explorer kit in <u>controlSUITE</u> is divided into simplified incremental builds to run smaller subsystems of increasing complexity. This makes it easier to learn and get familiar with the board and software, and enables easy debugging and testing boards. The three incremental builds are:

Build 1: Illustrates closed current loop control of the inverter stage. This level is used to verify PWM switching, ADC sampling and protection circuitry.

Build 2: Illustrates MPPT and DC bus regulation along with closed current loop control of the inverter stage with a Bulb Load at the output of the inverter, and locally generated sine reference.

Build 3: Illustrates the grid connection of the PV inverter along with MPPT, DC Bus regulation and closed loop current control of the inverter, a resistive load must be used (not shipped with the kit) for this build.

Figure 29 illustrates the full control scheme for the PV inverter using solar explorer kit. For source code, download <u>controlSUITE</u> and choose solar explorer kit at the time of installation.



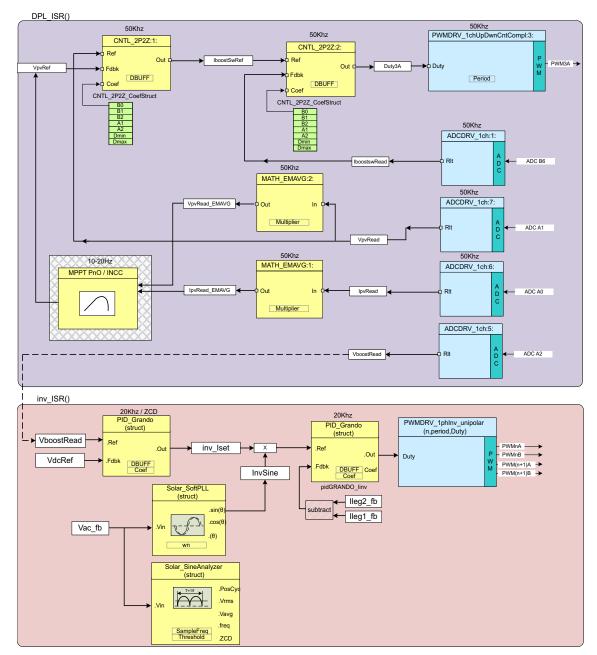


Figure 29. Full Control Scheme for the PV Inverter



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