Application Report
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Grid-Connected Micro Solar Inverter Implement Using a C2000 MCU

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ABSTRACT

The current boom in the development of renewable energy use will trigger a fourth industrial revolution. Photovoltaic power generation is a vital part of the overall renewable energy scheme. In all solar inverters, the micro solar inverters are critical components.

This paper describes how to use a TMS320F2802x to design a micro solar inverter with low cost and high performance. Also discussed is the use of the interleaved active-clamp flyback, plus an SCR full-bridge, to realize a micro solar inverter with a 220-W output, and also provide the entire system firmware architecture and control strategy. Finally, the waveforms in lab are provided.

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1 Overview

1.1 Introduction for Solar Inverter

Material, energy, and information are the three important elements for human survival and development. Each new discovery for energy use transformed and greatly promoted the development of modern civilization:

- The invention of the steam engine brought us into the machine age.
- The invention and use of electricity brought us into the electrical age.
- The invention of the semiconductor transistor brought into the information age.

The present renewable energy development and use will trigger a fourth industrial revolution; of all the renewable energy use methods, photovoltaic power generation is a critical part of overall renewable energy development. According to the world energy organization predictions, as the traditional energy sources (such as coal, oil, and so forth) gradually dry up, renewable energy power generation will become a major energy method. Figure 1 shows the development trend of world energy.

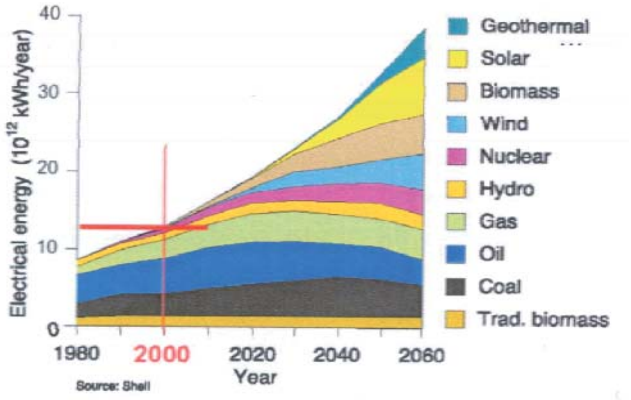


Figure 1. Development Trend of World Energy

Governments are greatly concerned about the development of renewable energy. In 2007, the Chinese government issued a "renewable can meet the long-term development planning", and in 2008 issued a renewable energy development plan for the eleventh 5-year. According to the requirements of the plan, China photovoltaic power generation installed capacity in 2010 is 250 billion watts; it is estimated that by 2020 this capacity will reach 5000 billion watts, which, combined with the grid-tie photovoltaic power generation, accounts for 75 percent of the total.

The main advantages of solar photovoltaic power generation include:

- Solar energy is abundant and inexhaustible.
- The material to product PV panels is widely distributed and abundant reserves.
- Simple system structure, high conversion efficiency
- No pollution and can be recycle used
- Long life of photovoltaic battery, low maintenance costs

Shortcomings of solar photovoltaic power generation include:

- Low power density, larger cover area

- Generation limited by natural conditions, no sun and no power
- High unit generating cost

1.2 Classification of the Photovoltaic Power Generation System

According to the application of the scene, photovoltaic generation system can be divided into the off-grid solar inverter system and the grid-tied solar inverter system.

The off-grid solar inverter system is mainly used in composition-independent photovoltaic power generation system, applied in the family, the countryside, island, and remote areas of the power supply, and urban lighting, communications, testing and application of the system of power supply. Figure 2 is a system block diagram that shows the main components of the solar panels components, solar inverter units, energy storage unit, and electricity load and so on.

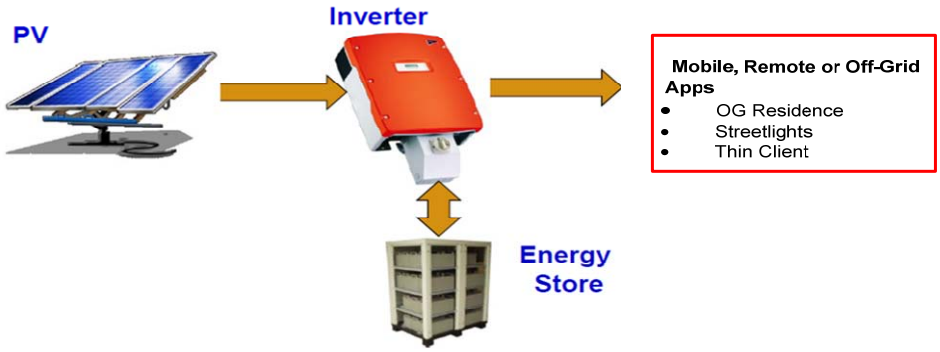


Figure 2. Off-Grid Solar Inverter System

While the grid-tie solar inverter system is mainly used in parallel with the traditional utility grid, the solar inverter converts the energy from the PV panel to the traditional utility grid, the main components of the solar panels components, solar inverter units, smart bidirectional metering, the house's consumer load and traditional utility grid, and so forth (see Figure 3).

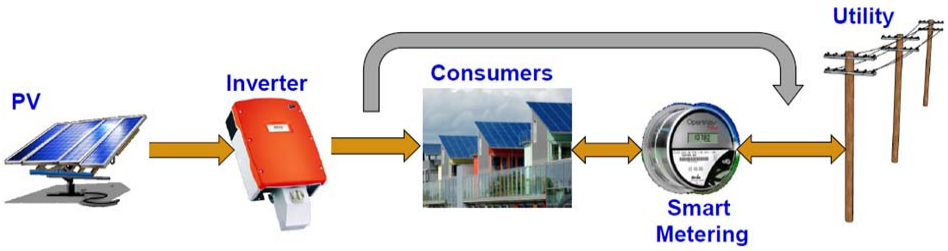


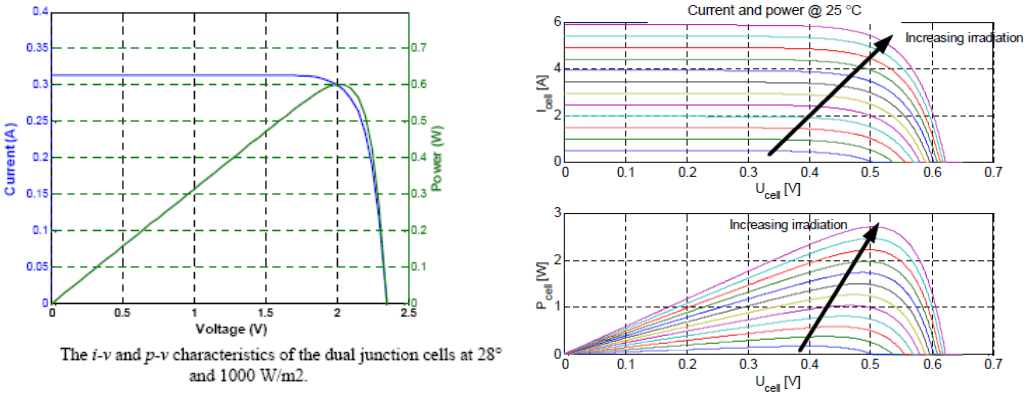
Figure 3. Grid-Tie Solar Inverter System

1.3 PV Panel Electrical Characteristics

Solar inverter power output varies almost directly with sunlight, but current drops off much faster until you reach very low light levels. PV panels typically will generate 16V under very low light conditions, but at very little current.

In addition, as the PV panel temperature increases, voltage output decreases and vice versa. Curve moves with lighting condition, temperature, and so forth, just like Figure 4.

Solar inverters must operate at the MPP to capture maximum energy from the PV panel. This is accomplished by the maximum power point control loop known as the maximum power point tracker (MPPT).



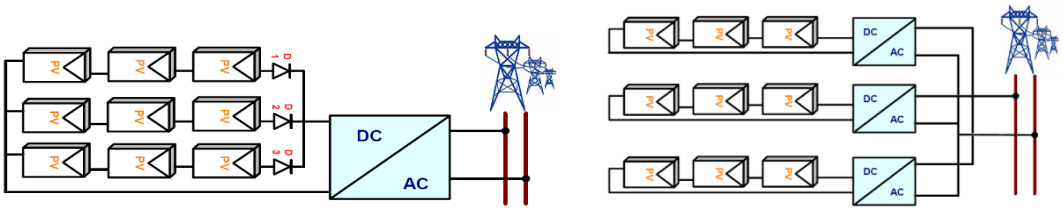
The *i-v* and *p-v* characteristics of the dual junction cells at 28° and 1000 W/m2.

Figure 4. PV Panel Electrical Characteristics

1.4 Solar Inverter Topology Shifts

Because the output voltage of one PV cell is from 20 to 45 volts with the change of illumination, if a higher output voltage is needed to suit for grid-tied application, usually consider putting a PV cell in parallel and in series to obtain high input voltage, and use one inverter to realize electric energy conversion. This type of topology is called “central inverters” just like Figure 5(a); its main feature is:

- 10 to 250 kw, 3-phase and several strings in parallel
- High converter efficiency, low cost and low reliability
- Not optimal MPPT
- Usually used for power plants



(a) (b)

Figure 5. Central and String Topology

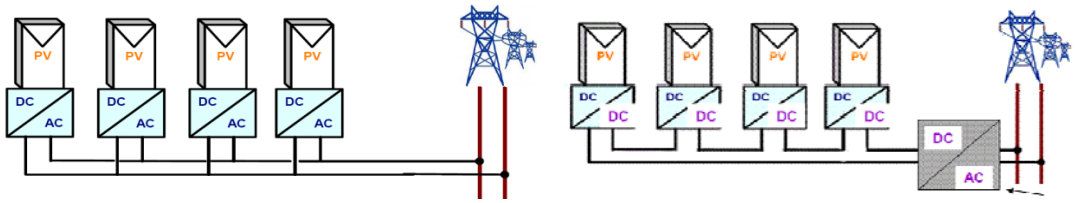
Another application is putting a PV cell in series to make the energy conversion, in every series branch. There is one MPPT module to capture maximum energy from the PV panel. This type of topology is called “string inverters” just like Figure 5(b); its main feature is:

- 1 to 10 kw, typical residential application
- Each string branch has its own inverter enabling better MPPT.
- The strings can have different orientations.
- Three-phase inverters for output power above 5 kw

Although the string inverter can gain more efficiency in energy capture, when one of the series PV cell is kept out by shadow, this string branch for energy capture decreases with it just like Figure 6(a). If a MPPT module is placed to capture every PV panel, it will be solved. This type of topology is called “micro inverters” just like Figure 7.

(a) (b)

Figure 6. Energy Harvest Influence by Shadow



(a) (b)

Figure 7. Micro Inverters Topology

Obviously, for micro inverters, this is a “distributed MPPT” architecture that adds cost per PV panel; however, efficiency is increased by 5 to 25 percent by recovering the following efficiency losses:

- PV panel mismatch losses (3 to 5 percent)
- Partial shading losses (5 to 25 percent)
- Simpler system design and alleviated fault tolerance (0 to 15 percent)
- Suboptimal MPPT losses (3 to 10 percent)
- Also, increases safety and square footage (roof) use

So if we choose the micro inverters topology, it sacrifices the converter efficiency but make the energy capture more efficient.

2 Hardware Design

2.1 System Block Diagram

In our solution for solar inverter, we choose the topology that is interleaved flyback plus SCR full-bridge for industrial frequency inverting. All of the control is only one MCU (2802×) to realize, there is also an interface by RS485 or PLC for communication. Figure 8 shows a block diagram of the micro solar inverter. For detail specifications, see Appendix A.

This topology has the following features:

- Simple system structure

- High efficiency and low cost
- Complete isolation and high reliability
- Unable to realize the reactive power compensation

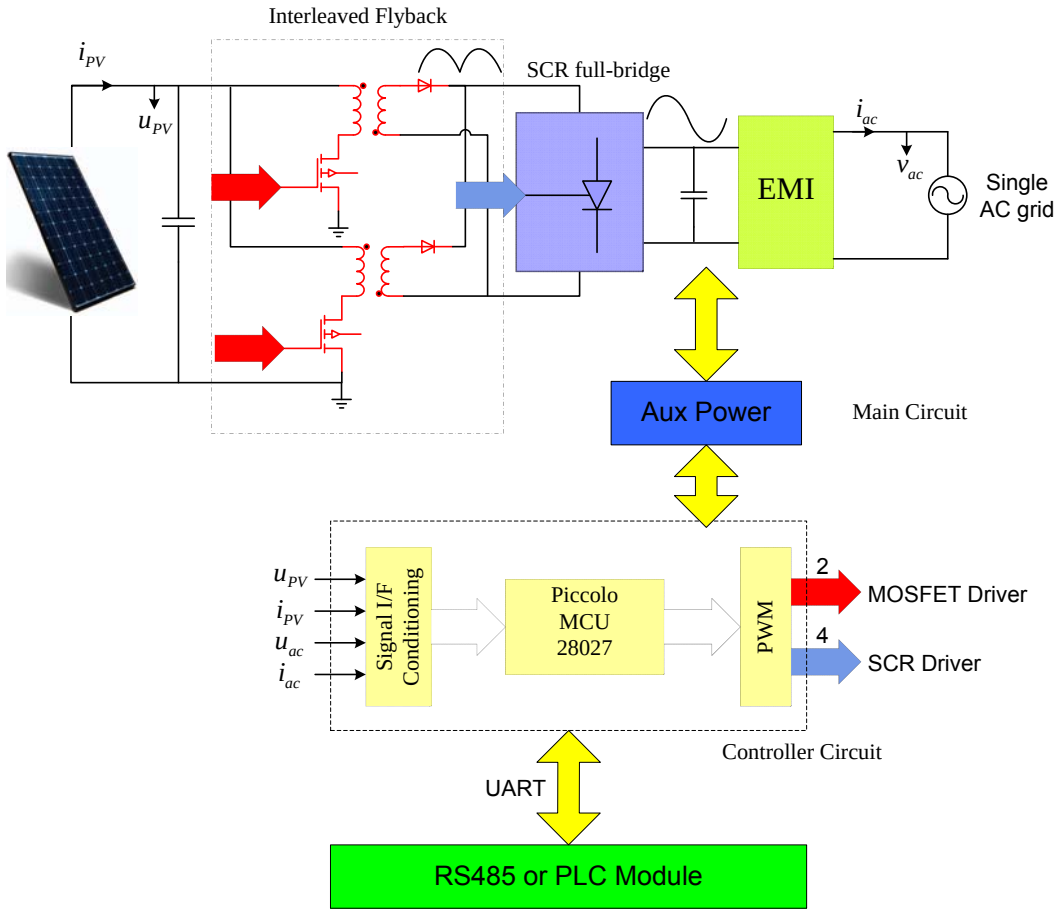


Figure 8. System Block Diagram of Micro Solar Inverter

2.2 Auxiliary Power Supply Design

In a micro solar inverter, we need auxiliary power that can output multiple voltages to A/D sample circuits, drive circuits, MCU controller, and so forth. On the other hand, the auxiliary power must be completely isolated from primary side to secondary side.

So the LM34927 chip is selected; this chip has many features as follows:

- Wide input range from 9 to 100V
- Low cost, integrated 100 V, high- and low-side switches
- The constant-on-time (COT) control scheme requires no loop compensation and provides excellent transient response.
- Full protected functions including adjustable UVLO.

Figure 9 shows the typical application schematic of LM34927. From the schematic, it is determined that the primary side of LM34927 is a buck circuit and the secondary side is a flyback topology to realize the isolation.

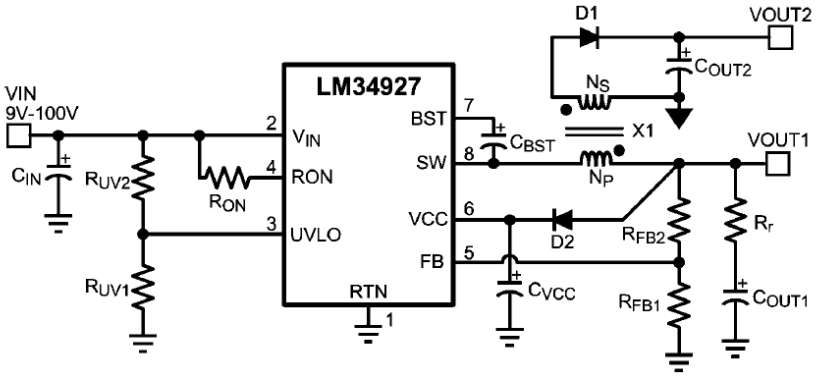


Figure 9. Typical Application Schematic of LM34927

2.3 Active-Clamp Flyback as an Isolated Front-End Converter Design

2.3.1 Active-Clamp Flyback Converter Overview

Figure 10 shows the incorporation of an active-clamp circuit into the basic flyback topology. In the figure, the flyback transformer is replaced with an equivalent circuit model showing the magnetizing and leakage inductances (L_r represents the total transformer leakage inductance reflected to the primary in addition to any external inductance).

Switches Q1 and Q2 are shown with their associated body diodes. C_r represents the parallel combination of the parasitic capacitance of the two switches. This device capacitance resonating with L_r enables zero-voltage switching (ZVS) for Q1.

With the active-clamp circuit, the transistor turn-off voltage spike is clamped, the transformer leakage energy is recycled, and ZVS for both primary (Q1) and auxiliary (Q2) switches becomes possible.

These advantages come at the expense of additional power stage components and increasing control circuit complexity (two switches as opposed to the usual one switch).

For this description of circuit operation, the following assumptions are made:

- Ideal switching components
- The magnetizing current is always nonzero and positive.
- L_r (includes the transformer leakage inductance) is much less than the transformer magnetizing inductance L_m (typically 5 to 10 percent of L_m).
- Sufficient energy is stored in L_r to completely discharge C_r and turn on the body diode of Q1.

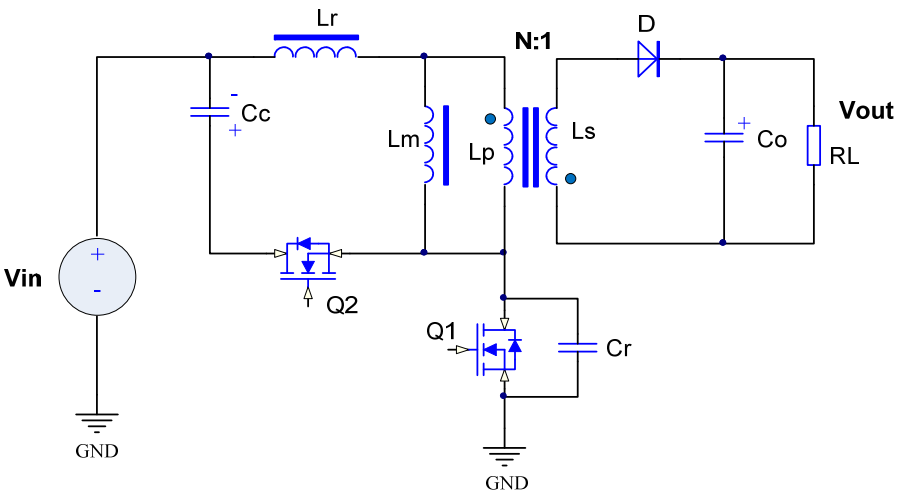


Figure 10. Simplified Schematic of the Active-Clamp Flyback Converter

2.3.2 Zero-voltage switching for active-clamp Flyback Design Considerations

To achieve ZVS for Q1, Q2 must be turned on during the decline interval of the resonant inductor current. If not, the resonant inductor current reverses (becoming positive again), recharging C_r, and ZVS is lost (or at least partially lost). Therefore, the delay time between Q2 turning off and Q1 turning on is critical to ZVS operation. The optimum value of this delay is one-quarter of the resonant period formed by L_r and C_r:

$$T_{delay} = \frac{\pi}{2} \times \sqrt{Lr \times Cr}$$

So it is best to put the dead time between the Q1 closed and Q2 open to less than T_{delay} to get partial condition of the ZVS.

Even if insufficient energy is stored in L_r to completely discharge the switch capacitance C_r, to minimize possible voltage stress on Q1 and Q2 (and get higher converter efficiency), we must cautiously design parameters of resonant inductor L_r, resonant capacitance C_r, and clamp capacitance C_c.

2.3.2.1 Design of Resonant Inductor L_r

After the value of L_m is fixed, the resonant inductor can be designed. As mentioned previously, it is assumed its value will be a small fraction of L_m (typically 5 to 10 percent of L_m).

For a given converter operating point and the value of C_r, to achieve ZVS the size of L_r must be sufficient to completely discharge the switch capacitance.

Designing L_r is difficult because the resonant capacitor voltage (Vc_r) is a function of the value of L_r as shown in the following equation:

$$I_{Q_1\_pk} = I_{Lm\_pk} = I_{Lr\_pk} \geq Vc_r \times \sqrt{\frac{C_r}{L_r}}$$

However, in a practical design situation, the resonant inductor voltage is relatively small (compared to $V_{in} + NV_o$) and can be solved for an approximate minimum value of L_r necessary to achieve ZVS conditions:

$$L_r \geq \frac{C_r \times (V_{in} + NV_o)^2}{I^2_{Q1\_pk}}$$

In this application requiring high-output voltage, it may be more desirable to specifically tailor the soft-switching characteristics of the output rectifier than to necessarily realize ZVS of the primary switch.

2.3.2.2 Design of Clamp Capacitor C_c

Choosing the value of clamp capacitance is done based on the design of L_r. The resonant frequency formed by the clamp capacitor and the resonant inductor should be sufficiently low so that excessive resonant ringing does not occur across the power switch when the switch is turned off. However, using a value of clamp capacitance that is too large yields no improvement in clamping performance at the expense of a larger (more costly) capacitor. A good compromise for design purposes is to select the capacitor value so that one-half of the resonant period formed by the clamp capacitor and resonant inductance exceeds the maximum off time of Q1. Therefore:

$$C_{clamp} \rangle\rangle \frac{\left(1 - D^{HL}\right)^2}{\pi^2 \times L_r \times f_s^{\,2}}$$

Where D^{HL} denotes operation at the maximum input voltage, f_s is the operation switch frequency of Q1 and Q2.

The capacitor voltage rating must exceed NV_o by the amount of voltage dropped across L_r:

$$V_{clamp\_\max} \approx NV_o + \frac{2 \times L_r \times f_s \times P_{o\_\max}}{\eta \times V_{in\_HL} \times (1 - D^{HL})}$$

The resonant period of the clamp capacitor and resonant inductance can be calculated by the following equation:

$$T_{resonant} = 2\pi \times \sqrt{L_r \times C_r}$$

2.3.3 Open-Loop Simulation of the Active-Clamp Flyback

Figure 11 is the open-loop simulation model of the active-clamp flyback. The following values apply to this simulation: input voltage V_{in} = 36 volt, switch frequency of primary MOSFET $f_s = 65kHz$, resonant inductance L_r =0.5 μH, resonance capacitance C_r = 1 nF, clamping capacitance C_c =10 μF, the maximum duty cycle for primary main switch MOSFET D = 0.6, and load R_{Load} = 100 Ω.

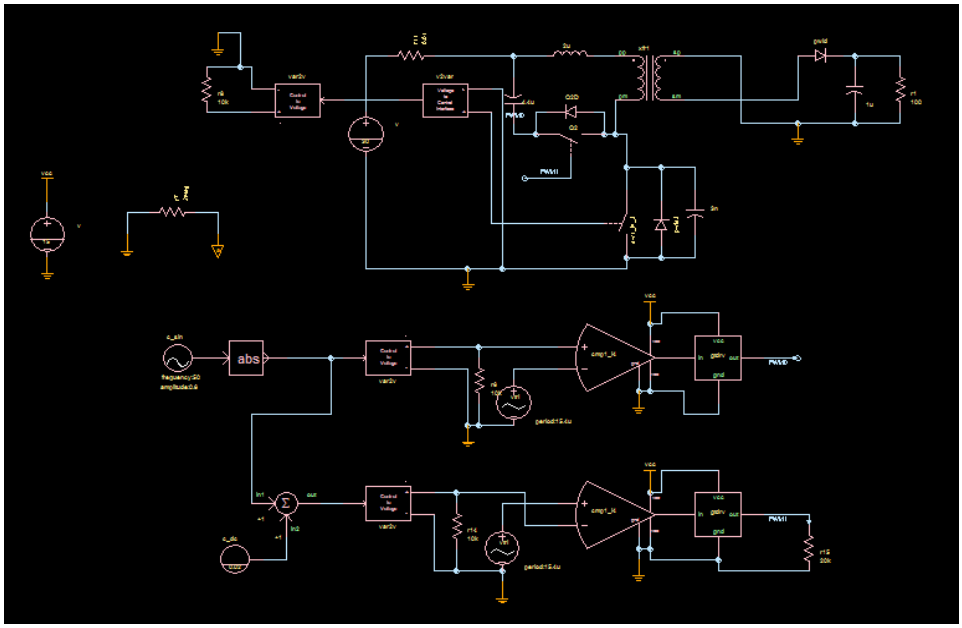
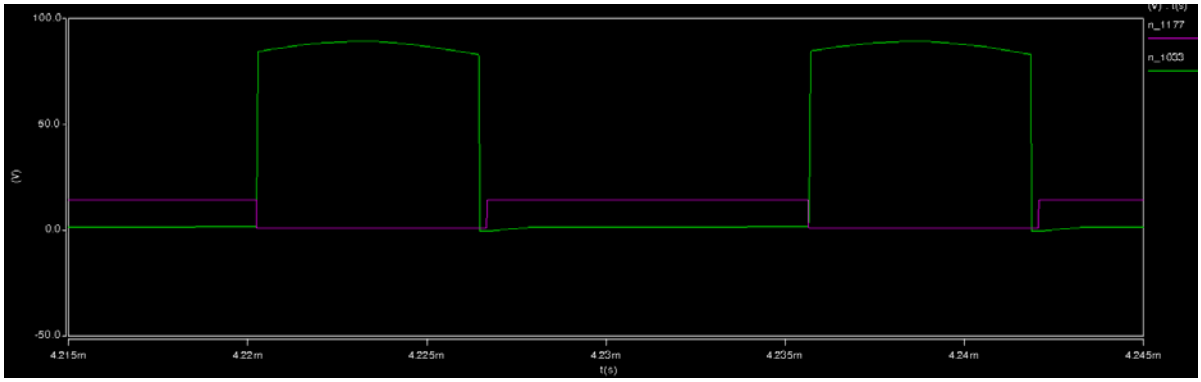


Figure 11. Open-Loop Simulation Model of Active-Clamp Flyback



(Red waveform is V_{GS}, green waveform is V_{DS})

Figure 12. Simulated Waveform of V_{DS} and V_{GS} on Q1

Figure 12 indicates the voltage rise of gate drive after the voltage of drain to source drops to zero, so it can be confirmed that Q1 realized ZVS. Also, the voltage spike of V_{DS} is clamped to $V_{in} + NV_{out}$, meaning that the primary side realized active-clamp.

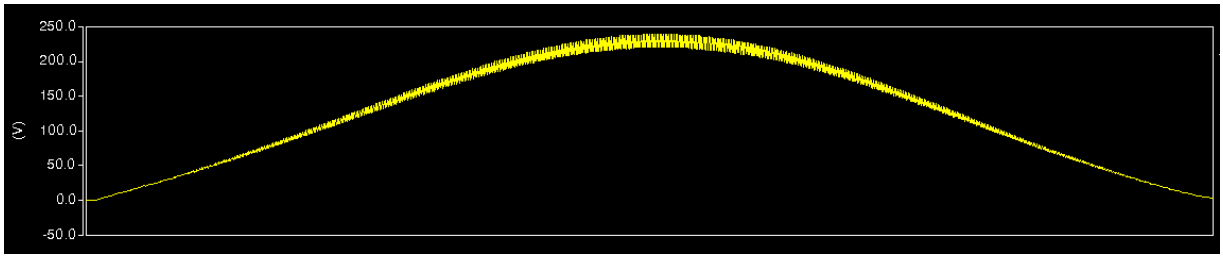


Figure 13. Simulated Output Voltage Waveform

2.4 Isolated MOSFET Bridge Drive Circuit Design

To achieve complete isolation from primary side to secondary side, A/D sampling and drive circuit isolation is required, in addition to auxiliary power isolation.

Because the MCU is placed in the secondary side while the main switch MOSFET is at the primary side, we must turn the control signal of secondary side transfer to the primary side to control MOSFET.

To transfer the control signal from secondary side to primary side, select the chip of the high-speed digital isolators plus the high- and low-side driver. Figure 14 shows a schematic diagram of the isolated MOSFET high- and low-side driver.

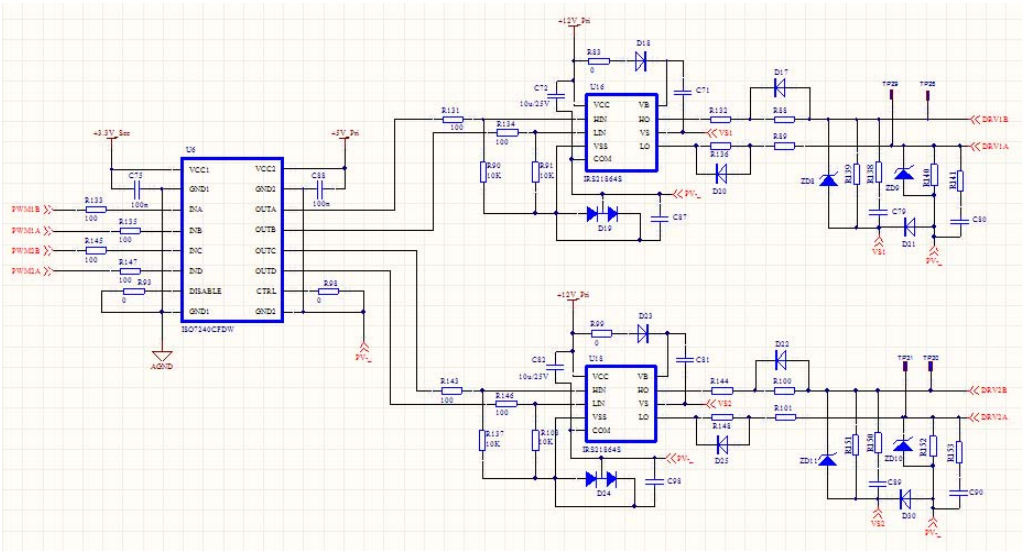


Figure 14. Schematic Diagram of Isolated MOSFET High- and Low-Side Driver

In this application, the isolated MOSFET has many features, including:

- Simple structure, easy implementation
- Fully operational to +600 V

- 4-kV ESD protection
- Bootstrap operation

In addition, pay special attention to the initial state of the high-speed digital isolators; otherwise, it can damage the main switch MOSFET.

Table 1. High-Speed Digital Isolators Function Table

Vcc1	Vcc2	Date Input (IN)	Disable Input (DISABLE)	Fail Safe Control Input (CTRL)	Data Output (OUTPUT)
PU	PU	H	L or Open	×	H
PU	PU	L	L or Open	×	L
×	PU	×	H	H or Open	H
×	PU	×	H	L	L
PD	PU	×	×	H or Open	H
PD	PU	×	×	L	L

(PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level)

3 Firmware Design

3.1 Firmware Specification

3.1.1 Function Specification

The firmware of the system includes the following functions:

1. Turn On/Off. The user can turn on or turn off the system by pressing the turn on/off button. The software setting must enable this function.
2. Auto Turn On/Off. If the turn on condition is satisfied, the system can turn on itself automatically. When the condition is not fit to feed the energy to the grid, the system stays in the standby mode, and observes the condition changes. If the system is already turned on, the system turns off automatically when the condition is not fit to feed energy.
3. Soft start turning on. When the system must turn on, it starts from the zero current feeding, and the PWM turns on at the zero-crossing point to reduce the rush current to the grid.
4. LED Control. The system has one status LED. When the system is in standby mode, the corresponding LED flashes every 1.2 seconds. When the system is turned on, the LED flashes every 2.4 seconds. When there is a fault, the LED is lighted continuously.
5. User Key Control. The inverter has a user key. The user key can turn on or turn off the inverter, and it can also clear the fault. When the system stays in standby mode, if the key is pressed on for more than 1 second, the system turns on if the condition is satisfied. If the system is already turned on, when the key is pressed on for more than 1 second, the system turns off. When there is a fault and the system stays in fault mode, the fault can be cleared and go into standby mode again by pressing the user key for more than 1 second.

3.1.2 Measurements

To control and monitor the system status, the following measurements are calculated:

- Grid voltage RMS
- Grid frequency
- Output active power of the inverter
- Input power
- Input PV voltage
- Temperature

3.1.3 Protection

The system has some basic protection functions.

1. Primary side rush current protection. When a rush current caused by the short circuit or the saturation of the primary inductor occurs, the PWM works in CBC mode first; however, when the CBC is more than three times, the system turns off and goes into fault mode.
2. Secondary side overvoltage. When the SCR is not turn on normally, a very high voltage in the secondary side occurs. The system turns off and goes into the fault mode.
3. Output overcurrent. When the amplitude of the output current exceeds the threshold, an output overcurrent fault occurs. The system turns off and goes into fault mode.
4. Grid voltage/frequency over/under. If the system is already turned on, when the grid voltage/frequency is out of the normal range, the system turns off in five grid cycles.
5. Anti-islanding. If the islanding condition is satisfied, the system turns off in 4 seconds. If the condition is recovered to normal, the system can restart in 1 second.
6. Over temperature

3.1.4 Grid-tie Converter Controller

To feed the energy to the grid, the following controller algorithm must be realized in this system:

1. Phase-locked loop (PLL) controller. The PLL controller is used to synchronize with the grid voltage, which can provide a reference phase to the current controller.
2. Grid-tie current controller. The current controller can ensure the output current is a sine wave and trace the current reference to balance the input power and the output power.
3. Maximum power point tracking (MPPT). The MPPT is used to put the panel into a maximum power output stage.

3.2 Firmware Structure

3.2.1 Background and Task

The whole firmware system is a forward-background system. Figure 15 shows the background structure.

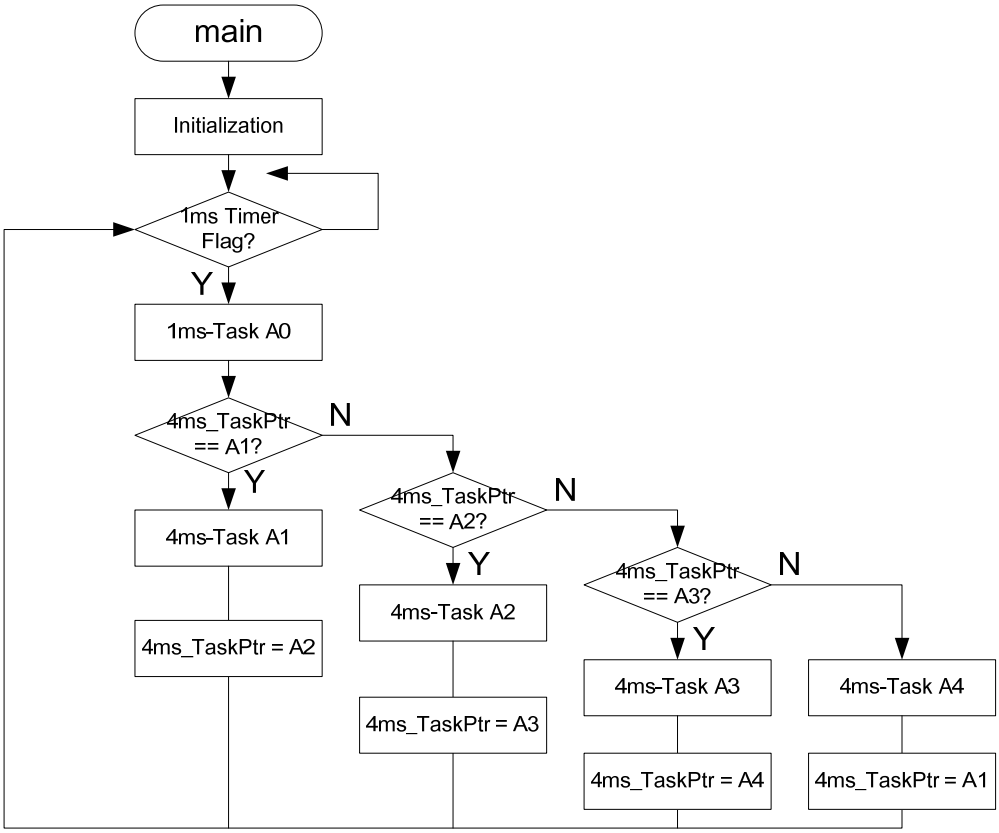


Figure 15. Background Structure

There are one 1-ms task and four 4-ms tasks in this system.

1. 1ms-Task A0. The 1-ms periodical task. In this task, the LED control executes. Besides, the PLL controller is also located in this task.
2. 4ms-Task A1. The A1 4-ms periodical task. The status machine processor.
3. 4ms-Task A2. The A2 4-ms periodical task. All the measurements are calculated in this task.
4. 4ms-Task A3. The A3 4-ms periodical task. The user key detection is here, and the over/under range of the running conditions are detected here as well, and the fault command is sent out.
5. 4ms-Task A4. The A4 4-ms periodical task. MPPT controller and the debug support.

3.2.2 The Status Machine of the System

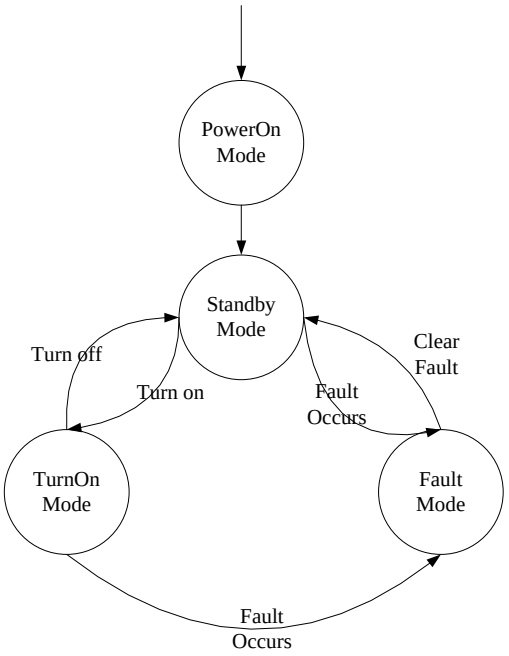


Figure 16. The Status Machine

Figure 16 shows the status machine processed in task A1. Different status represents different running mode.

There are four status modes in this system:

- Power on
- Standby
- Turn-on
- Fault

Power on mode is a transition mode when the system power is on. In this mode, the system does some initializations, after which the system gets into the standby mode automatically.

Standby mode is the mode in which the system waits for the command to turn on. All the PWM and the SCR control signal are off. In this mode, all the measurements are valid. The system detects the outside conditions and checks if the system can be turned on.

When the system is turn on successfully from standby mode, the system gets into turn-on mode. All the PWM and the SCR control signal are on in this mode. The system starts to feed the energy to the grid.

If a fault occurs, the system goes into fault mode, all the PWM and the SCR control signal is off. If the fault is cleared, the system can go back to standby mode automatically.

3.2.3 Interrupt Sevice Routine

The interrupt service routine (ISR) in this system has the following functions:

- Read the ADC result and a part of the measurement calculation.
- Grid-tie current controller
- SCR on/off control
- Emergency protection. The primary-side rush current, the secondary-side overvoltage and the output current amplitude over protection.
- Debug support. Record the debug data to the buffer.

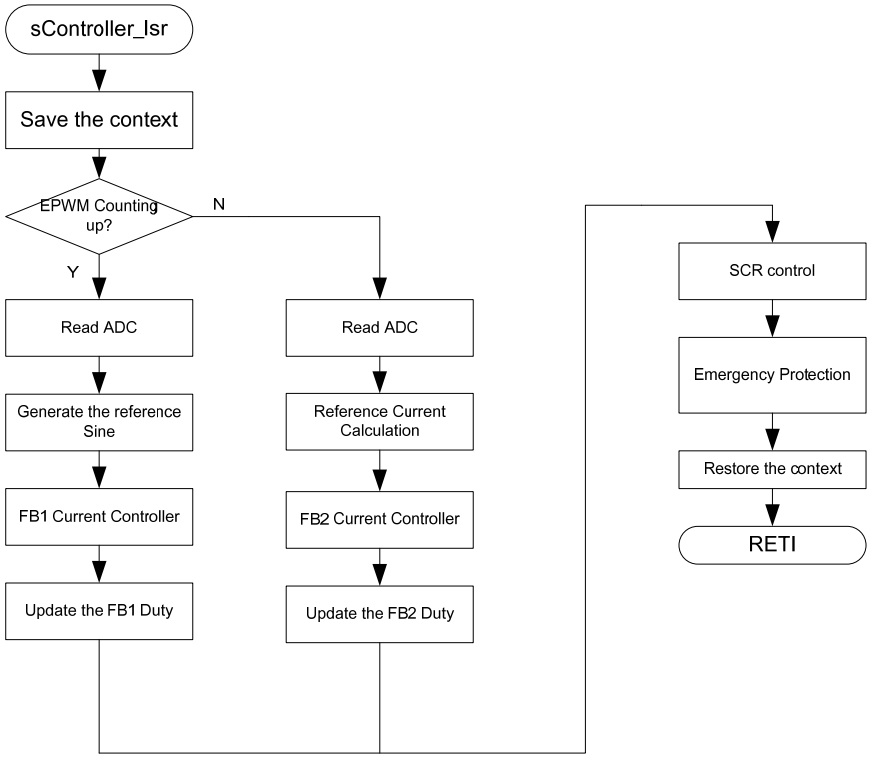


Figure 17. The ISR Flow Chart

3.3 Grid-Tie Converter Controller

Figure 18 shows the whole grid-tie converter structure.

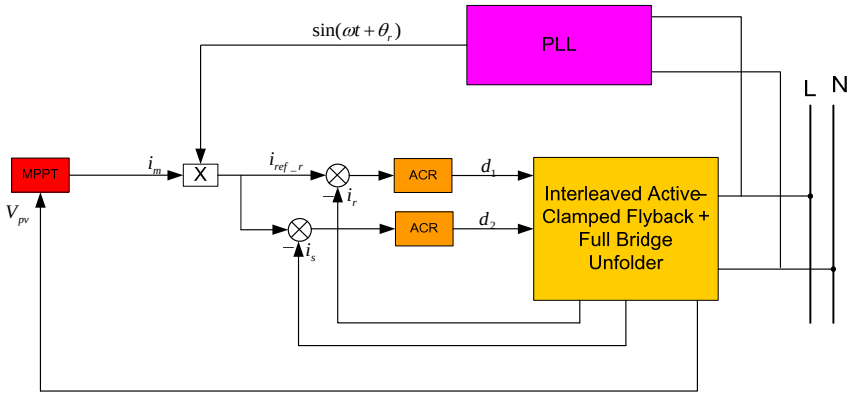


Figure 18. The Controller Structure

3.3.1 PLL Controller

Figure 19 shows the PLL control system.

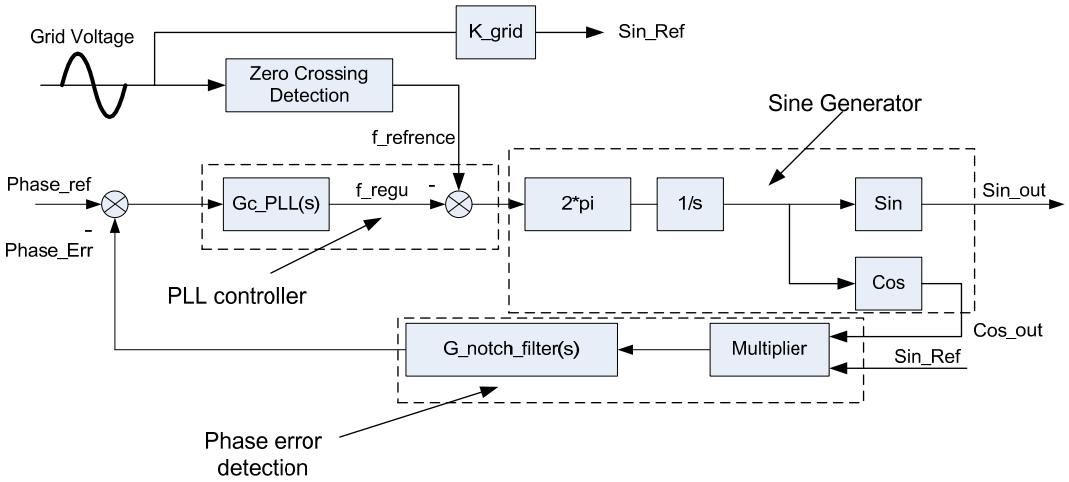


Figure 19. The PLL Control System Diagram

The PLL system is made up of the following parts:

- The phase error detection. Detect the phase error between the reference and the sine wave out. This detection is done in 1-ms task A0.
- The PLL controller. Close loop controller, the controller is executed in 1-ms task A0.
- The Sine generator. Generate the sine wave according to the frequency and sample time; this is done in the ISR.

3.3.2 Current Controller

To design the current loop, the object model must be built first. The small signal model can be used here.

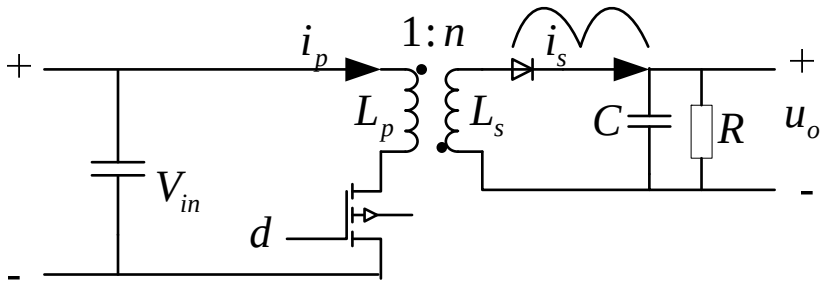


Figure 20. The Flyback Circuit

Assume a flyback circuit shown in Figure 6; also, assume it works in continuous mode.

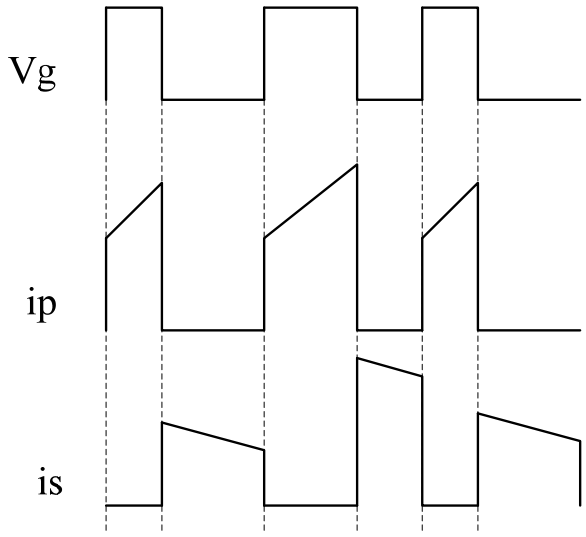


Figure 21. The Continuous Mode Current of the Flyback

If the MOS in the primary side is turned on, the current of the primary side increases, the L_p is charged, and the energy is stored in it. In the secondary side, the D1 turns off; the C is discharged to take the load. So the following equations can be obtained:

$$\begin{cases} L_p \dfrac{di_p}{dt} = V_{in} \\ C \dfrac{du_o}{dt} = -\dfrac{u_o}{R} \end{cases} \quad (1)$$

If the Q1 is turned off, the energy transfers to the secondary side immediately, the i_p degrades to zero soon. In the secondary side, the diode turns on, the secondary inductor takes the load and charges to the C. Equation (2) can be obtained.

$$\begin{cases} L_s \dfrac{di_s}{dt} = -u_o \\ i_s = C\dfrac{du_o}{dt} + \dfrac{u_o}{R} \end{cases} \tag{2}$$

The primary inductance L_p and the secondary inductance L_s have the following relationship:

$$L_s = n^2 L_p \tag{3}$$

Put Equation (3) to Equation (2):

$$\begin{cases} n^2 L_p \dfrac{d\frac{i_p}{n}}{dt} = -u_o \\ \dfrac{i_p}{n} = C\dfrac{du_o}{dt} + \dfrac{u_o}{R} \end{cases} \rightarrow \begin{cases} L_p \dfrac{di_p}{dt} = -\dfrac{u_o}{n} \\ C\dfrac{du_o}{dt} = \dfrac{i_p}{n} - \dfrac{u_o}{R} \end{cases} \tag{4}$$

Use the average state space method, if the duty is d, then we can get the following equation:

$$\begin{cases} L_p \dfrac{di_p}{dt} = d \bullet V_{in} - (1-d)\dfrac{u_o}{n} \\ C\dfrac{du_o}{dt} = -\dfrac{u_o}{R} + (1-d)\dfrac{i_p}{n} \end{cases} \tag{5}$$

Add the small disturbance to Equation (5):

$$\begin{cases} L_p \dfrac{d(i_p + \hat{i}_p)}{dt} = (d + \hat{d}) \bullet V_{in} - (1-d-\hat{d})\dfrac{(u_o + \hat{u}_o)}{n} \\ C\dfrac{d(u_o + \hat{u}_o)}{dt} = -\dfrac{u_o + \hat{u}_o}{R} + (1-d-\hat{d})\dfrac{i_p + \hat{i}_p}{n} \end{cases} \tag{6}$$

Remove the high-order infinitesimal element:

$$\begin{cases} L_p \dfrac{d\hat{i}_p}{dt} = \hat{d}(V_{in} + \dfrac{u_o}{n}) - \dfrac{1-d}{n}\hat{u}_o \\ C\dfrac{d\hat{u}_o}{dt} = -\dfrac{\hat{u}_o}{R} + (1-d)\dfrac{\hat{i}_p}{n} - \hat{d}\dfrac{i_p}{n} \end{cases} \tag{7}$$

So the relation between $\hat{d}(s)$ and $\hat{i}_p(s)$ is:

$$G_{id}(s) = \frac{\hat{i}_p(s)}{\hat{d}(s)} = \frac{V_{in} + \frac{u_o}{n}}{L_p} \tag{8}$$

The stable state of the d is:

$$D = \frac{u_o}{nV_{in} + u_o} \tag{9}$$

The controller loop is:

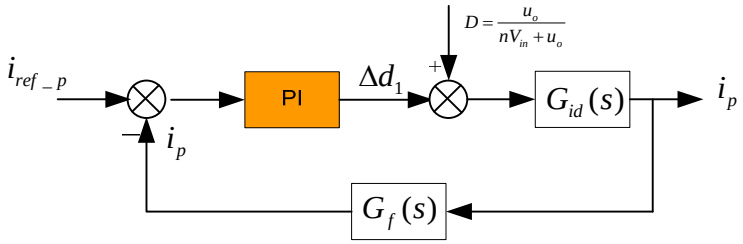


Figure 22. The Current Controller Loop

Using the PI controller, the controller calculation frequency is 22 kHz. The open loop bandwidth must be set to 1 to 2 kHz.

Figure 8 indicates that the feedback of the close loop must be the primary side current i_p, but in the real system it is the middle point current when Q1 is turned on in the real system. If the converter is working in continuous mode, the relationship between the primary feedback and the secondary average current is:

$$ni_s = (1-d)i_p \tag{10}$$

To get a sine wave output current, the secondary average current must be a sine wave; therefore, it is necessary to modify the feedback current to the following model:

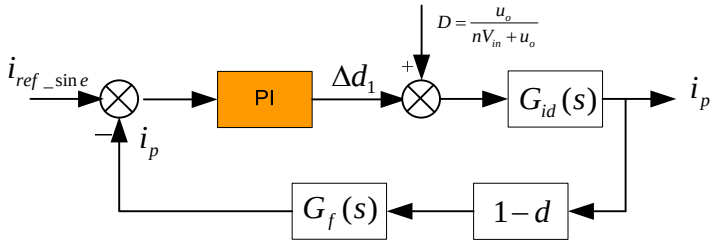
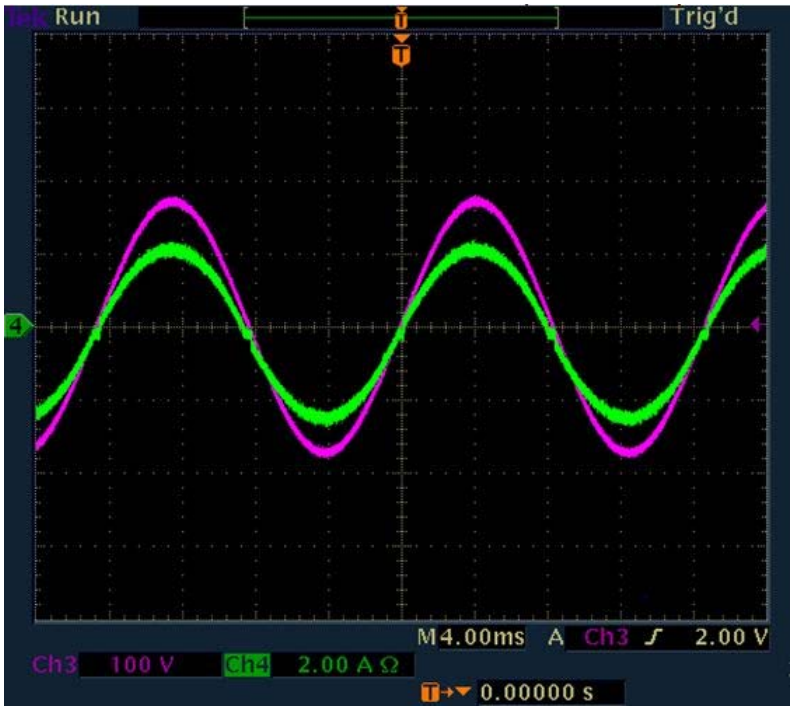


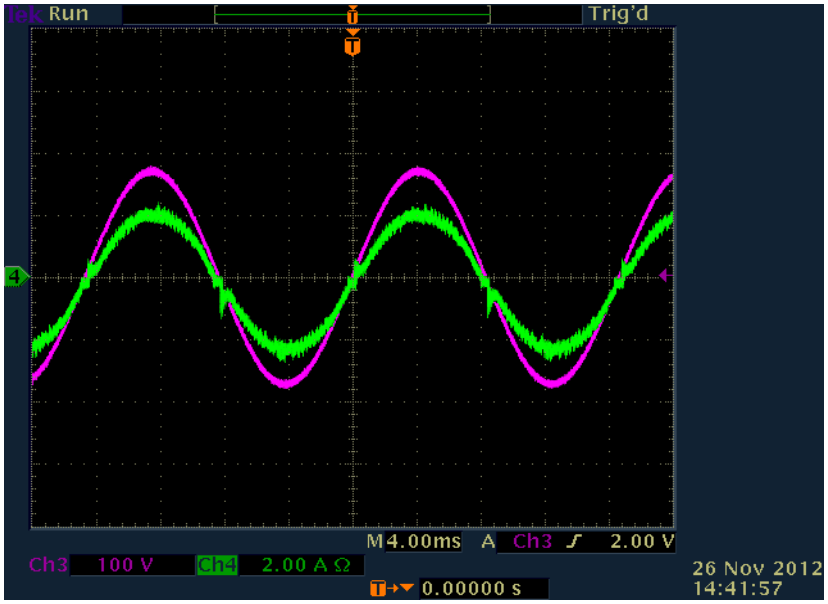
Figure 23. The Modified Current Loop

4 Test Waveforms in Lab



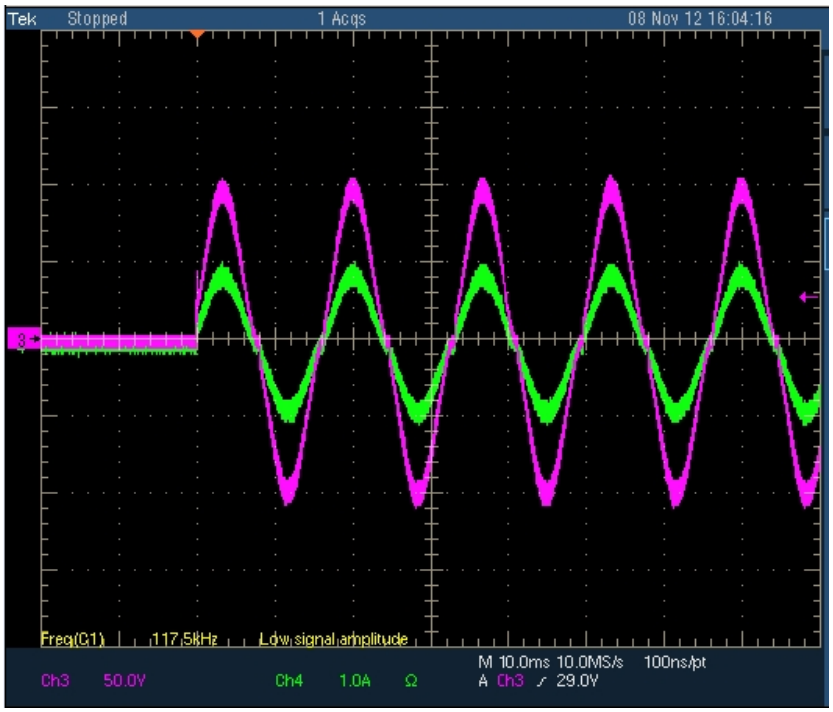
(CH3 Close-loop output Voltage, CH4 Close-loop output current)

Figure 24. Close-Loop Output Current and Voltage



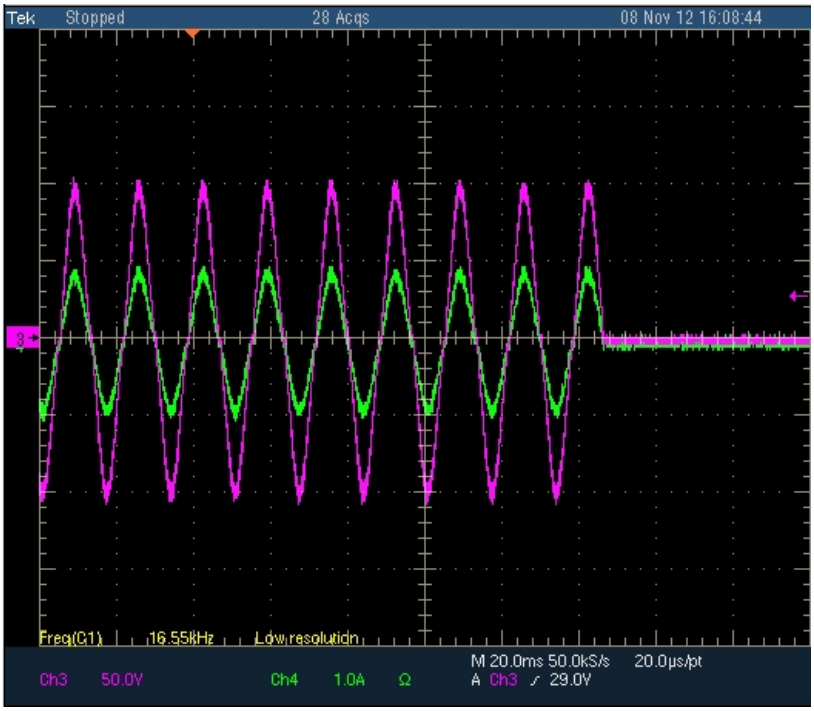
(CH3 Grid-tie Voltage, CH4 Grid-tie current)

Figure 25. Grid-Tie Current and Grid-Tie Voltage



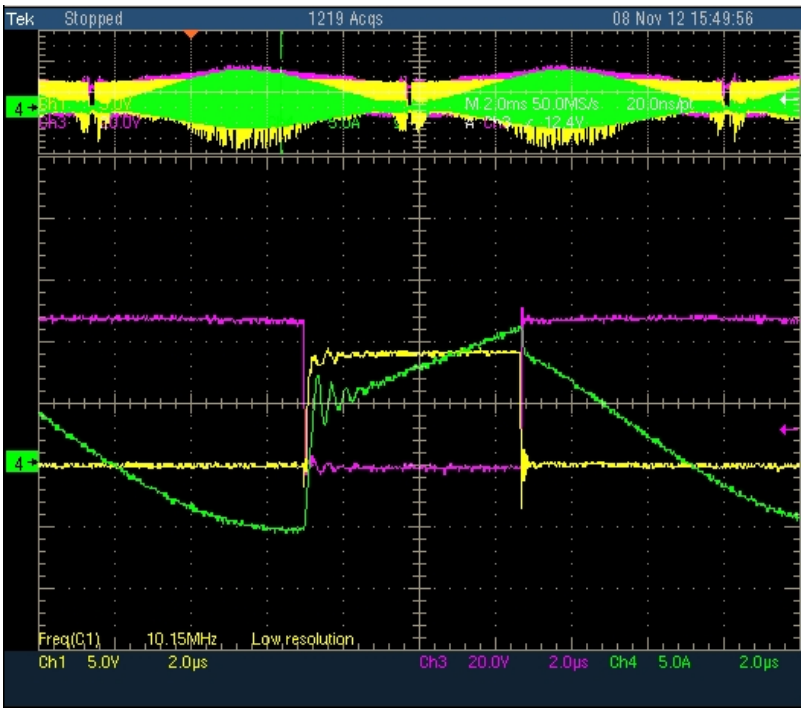
(CH2 Grid-tie Voltage, CH4 Grid-tie current)

Figure 26. Voltage and Current Waveform When System Turning On



(CH2 Grid-tie Voltage, CH4 Grid-tie current)

Figure 27. Voltage and Current Waveform When System Turning Off

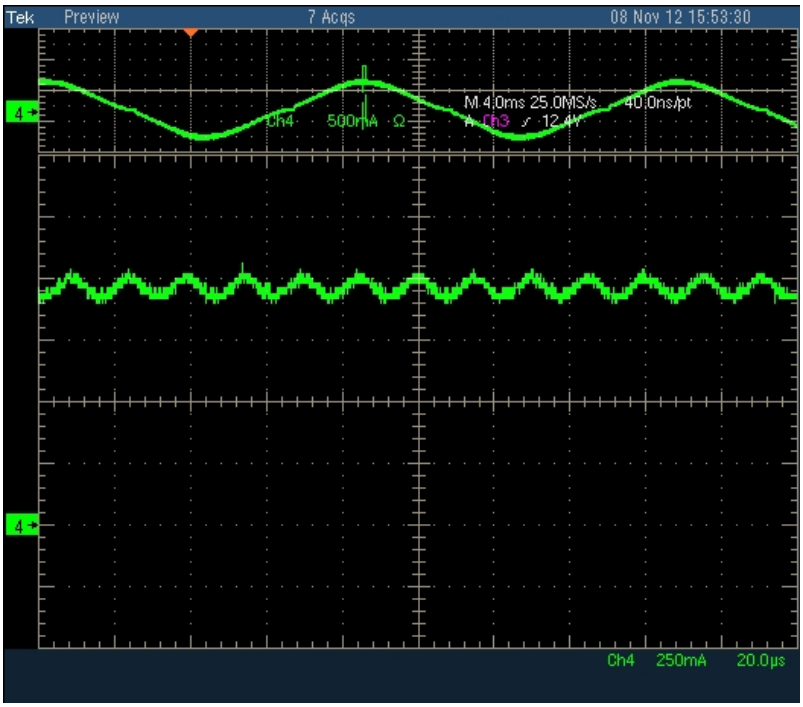


(CH1 V_{GS} of main switch MOSFET,

CH3 V_{DS} of main switch MOSFET,

CH4 resonance current on L_r)

Figure 28. ZVS Waveform of Main Switch MOSFET and Resonance Current on L_r



(CH4 Grid-tie current ripple)

Figure 29. Grid-Tie Current Ripple

5 Others

For schematics, see Appendix B.

6 References

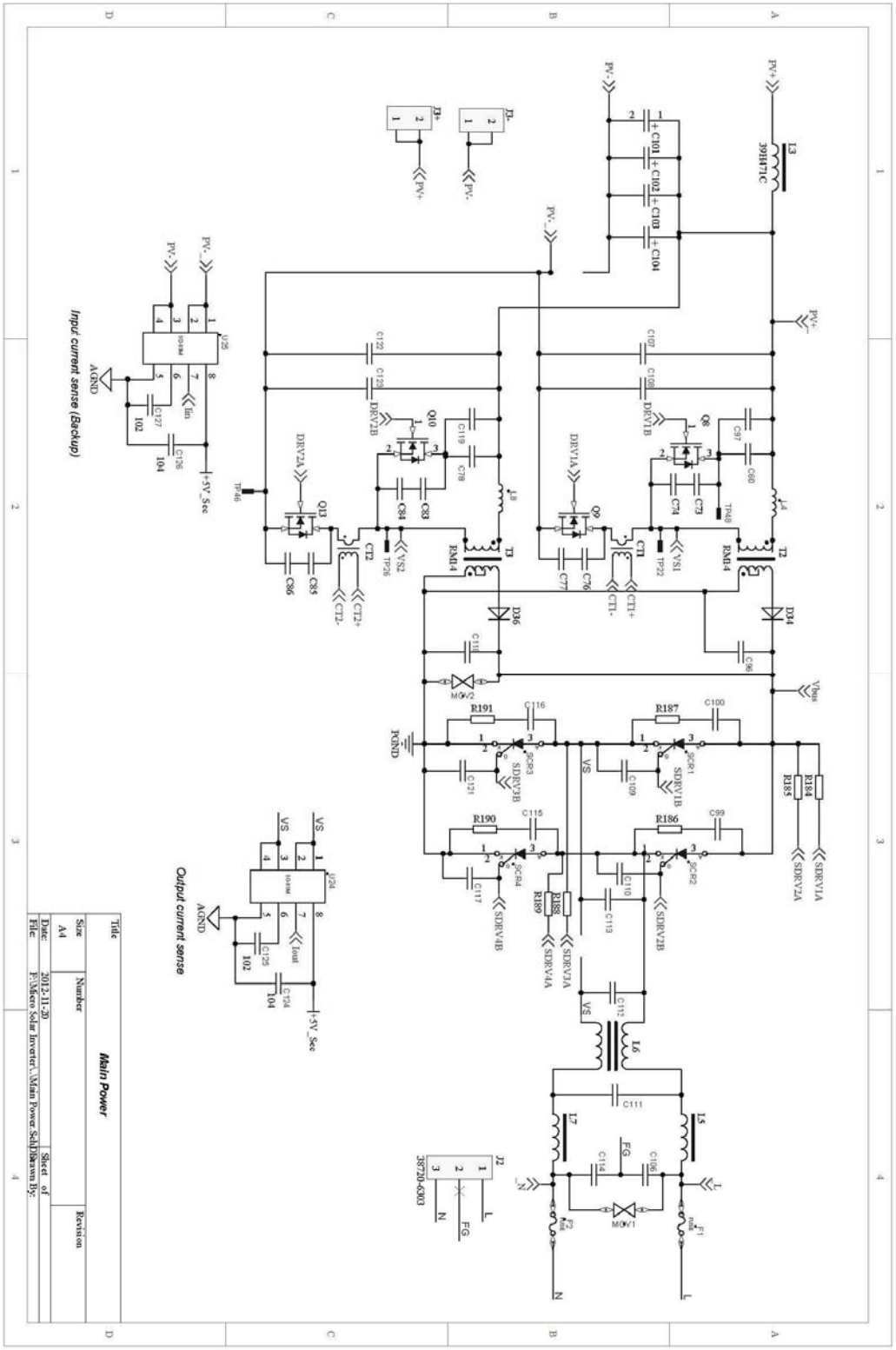
1. TMS320F2802x Datasheet, SPRS523G

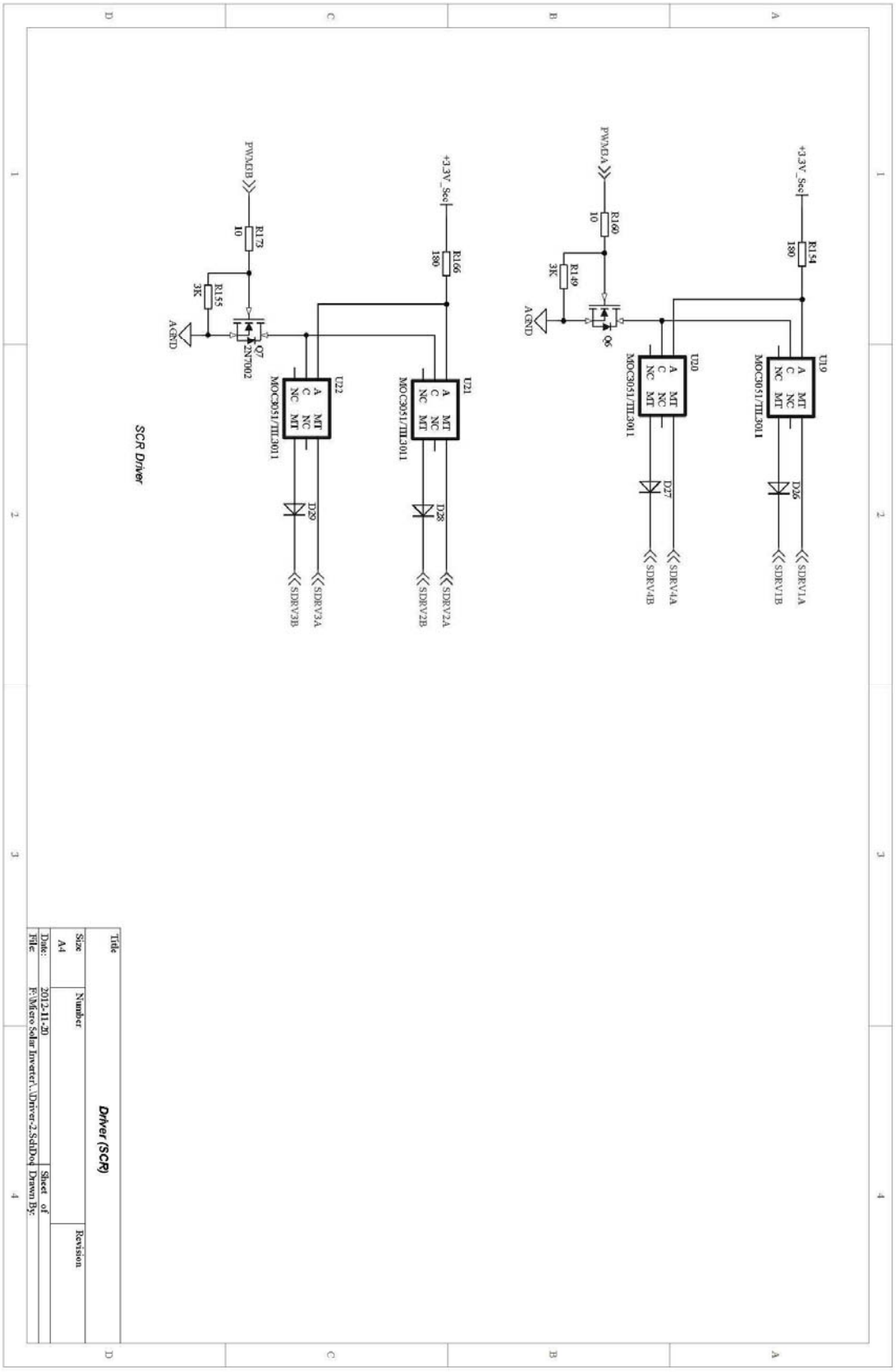
Appendix A. Electrical Specifications

DC Parameters				
Items	**Unit**	**Min**	**Typ.**	**Max**
MPPT voltage range	V	22		40
Operating range	V	20		45
Maximum DC input voltage	V			50
Minimum start voltage	V	18		
Maximum DC input short circuit current	A			15
Maximum DC input current	A			10
AC Parameters				
Items	**Unit**	**Min**	**Typ.**	**Max**
Rated AC output power	W		220	
Output power factor (PF)		0.95	0.99	1
Nominal AC output voltage range	Vrms	90	110	135
Nominal AC output current	A		2.1	
Nominal AC output frequency range	Hz		60	
Miscellaneous Parameters				
Items	**Unit**	**Min**	**Typ.**	**Max**
Peak inverter efficiency	%			95
Static MPPT efficiency	%		99	
Total harmonic distortion current	%	3	5	
Ambient temperature range	°C	-25		50
Night tare loss	W		1	

Software Functions	
Communication	PLC or RS485 (optional)
Protection	Islanding/Over Range/Short Circuit
Status LED display	Aux power LED, running LED, fault LED
Turn On/Off	Manual start, soft start (optional)
Debug support	RS485 interface
GUI	RS485
Dimensions (W × H × D)	
Cooling	Natural convection

Appendix B. Schematics

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Size
A4
Number
Revision
Date:
2012-11-20
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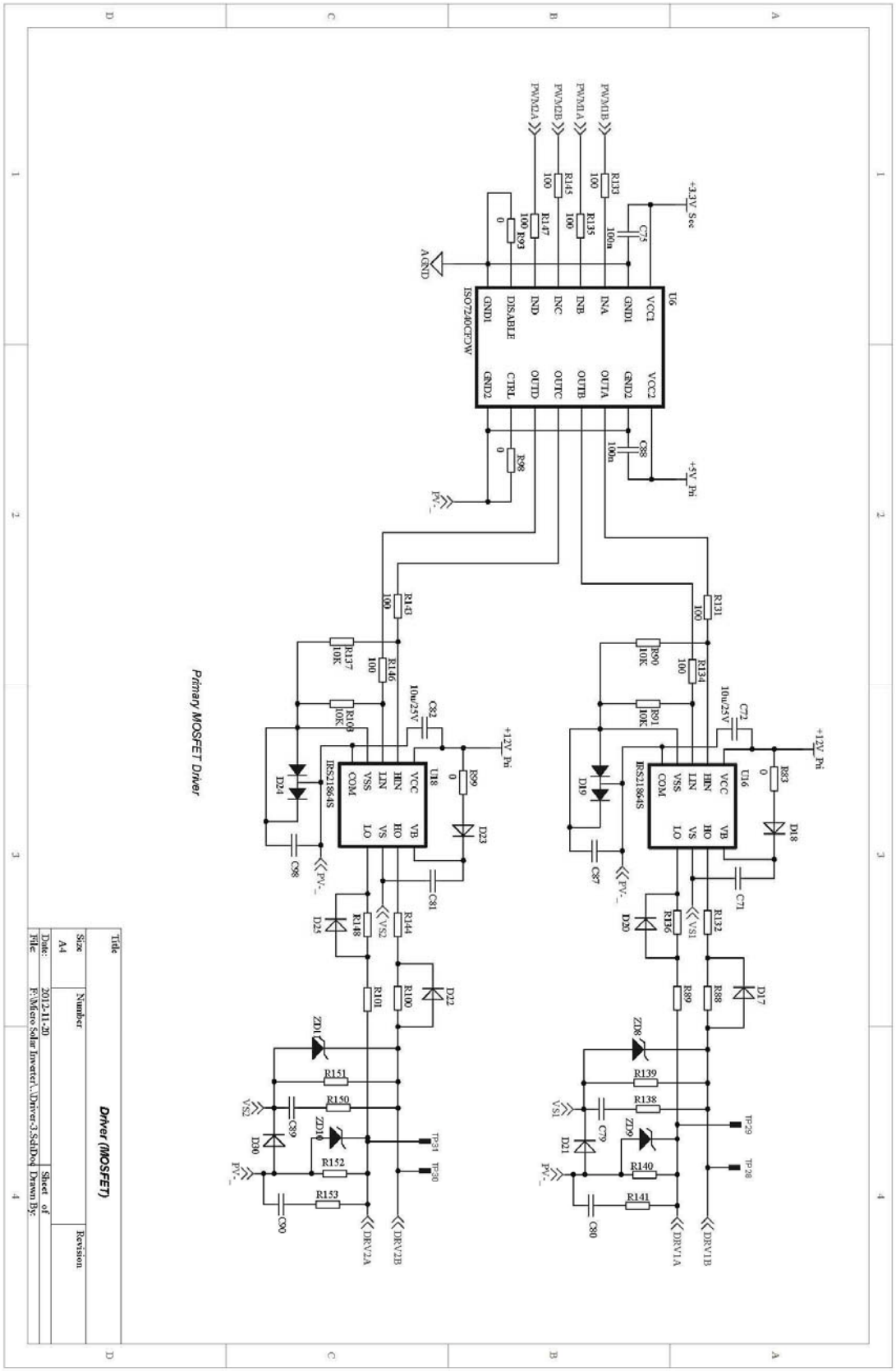
Drawn By:
+3.3V_Soc
PWMDA
PWMDB
R154
180
R160
10
R149
3K
R166
180
R173
10
R155
3K
AGND
Q6
Q7
2N7002
U19
U20
U21
U22
MOC3051/TIL3011
D26
D27
D28
D29
SDEV1A
SDEV1B
SDEV4A
SDEV4B
SDEV2A
SDEV2B
SDEV3A
SDEV3B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Driver (MOSFET)
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Size
A4
Number
Revision
Date:
2012-11-20
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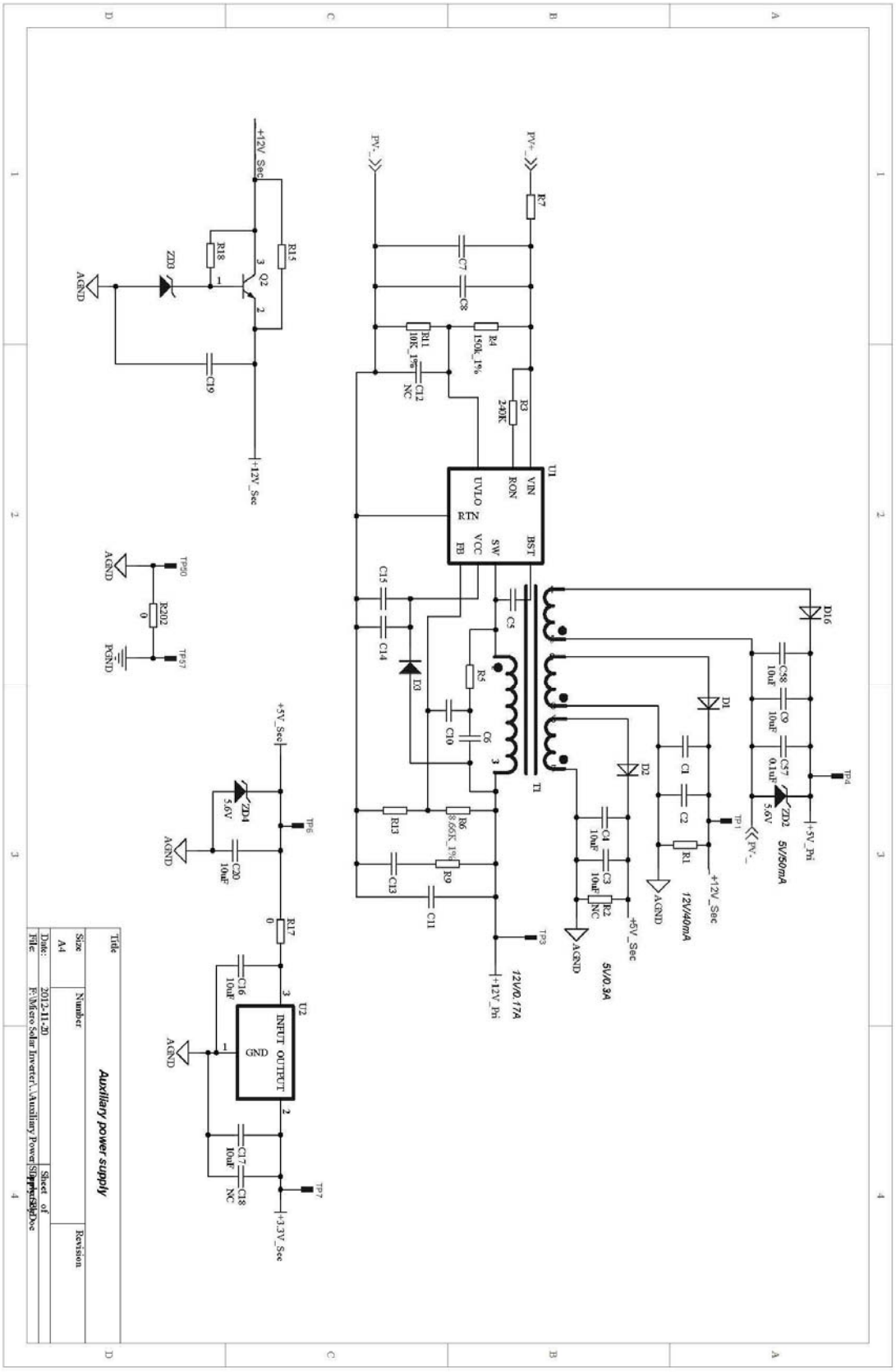
Sheet of
Drawn By:
U6
ISO7240CFDW
U18
U16
IRS21864S
+3.3V Sec
+12V_Pri
+5V_Pri
AGND
PWMGA
PWMGB
PWMIA
PWMIB
DRV2A
DRV2B
DRV1A
DRV1B
VS2
VS1
TP31
TP30
TP29
TP28


Auxiliary power supply
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Size
A4
Number
Revision
Date:
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+12V Sec
PV+
PV-
AGND
PGND
+5V_Sec
+3.3V_Sec
+12V_Pri
+5V_Pri
5V/50mA
12V/40mA
5V/0.3A
12V/0.17A
U1
VIN
RON
UVLO
RTN
VCC
FB
SW
BST
U2
INPUT
OUTPUT
GND
T1
ZD1
ZD2
ZD3
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D1
D2
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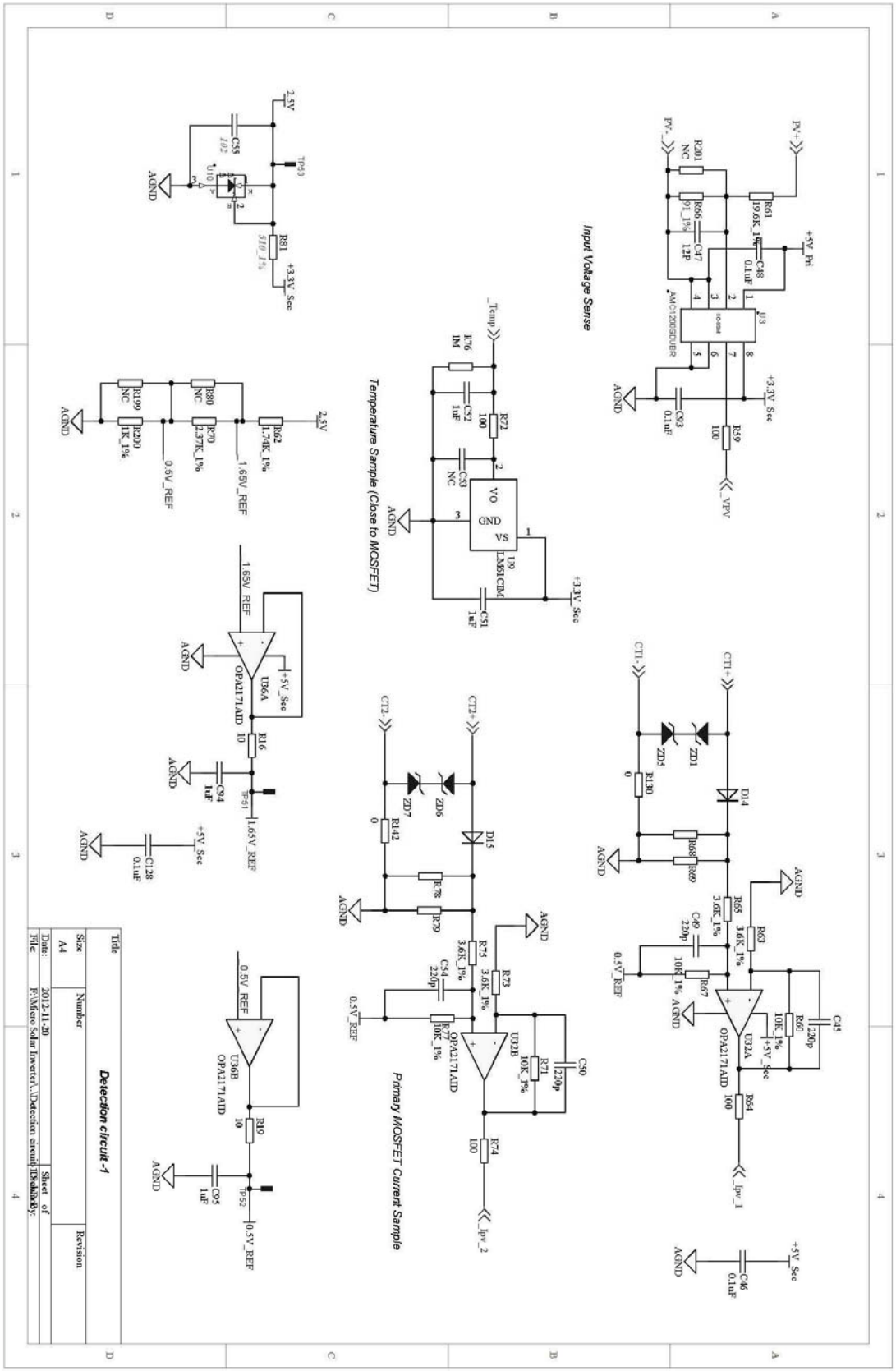
TP6
TP7


Input Voltage Sense
Temperature Sample (Close to MOSFET)
Primary MOSFET Current Sample
Detection circuit -1
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Size
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Number
Revision
Date:
2012-11-20
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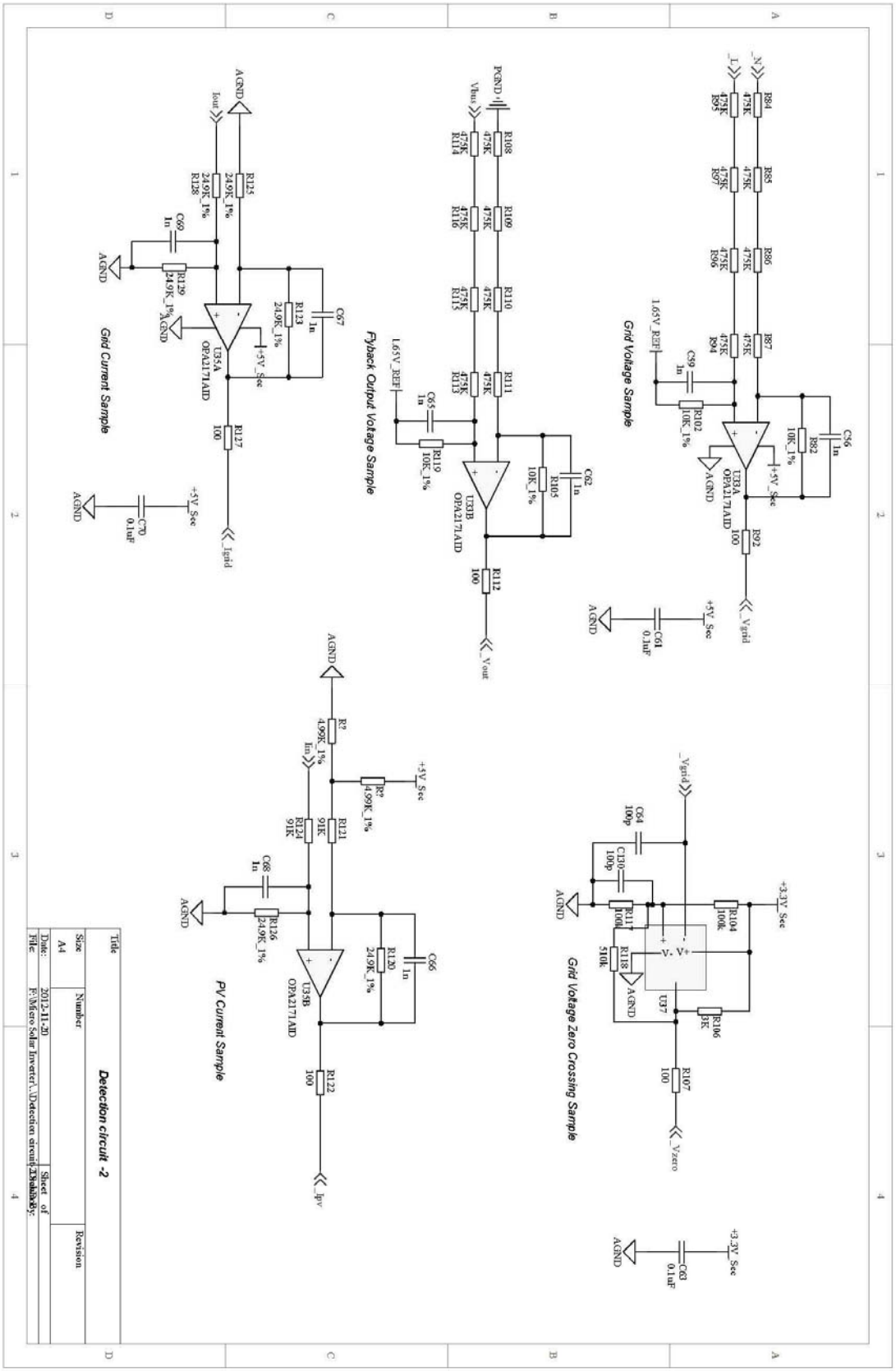
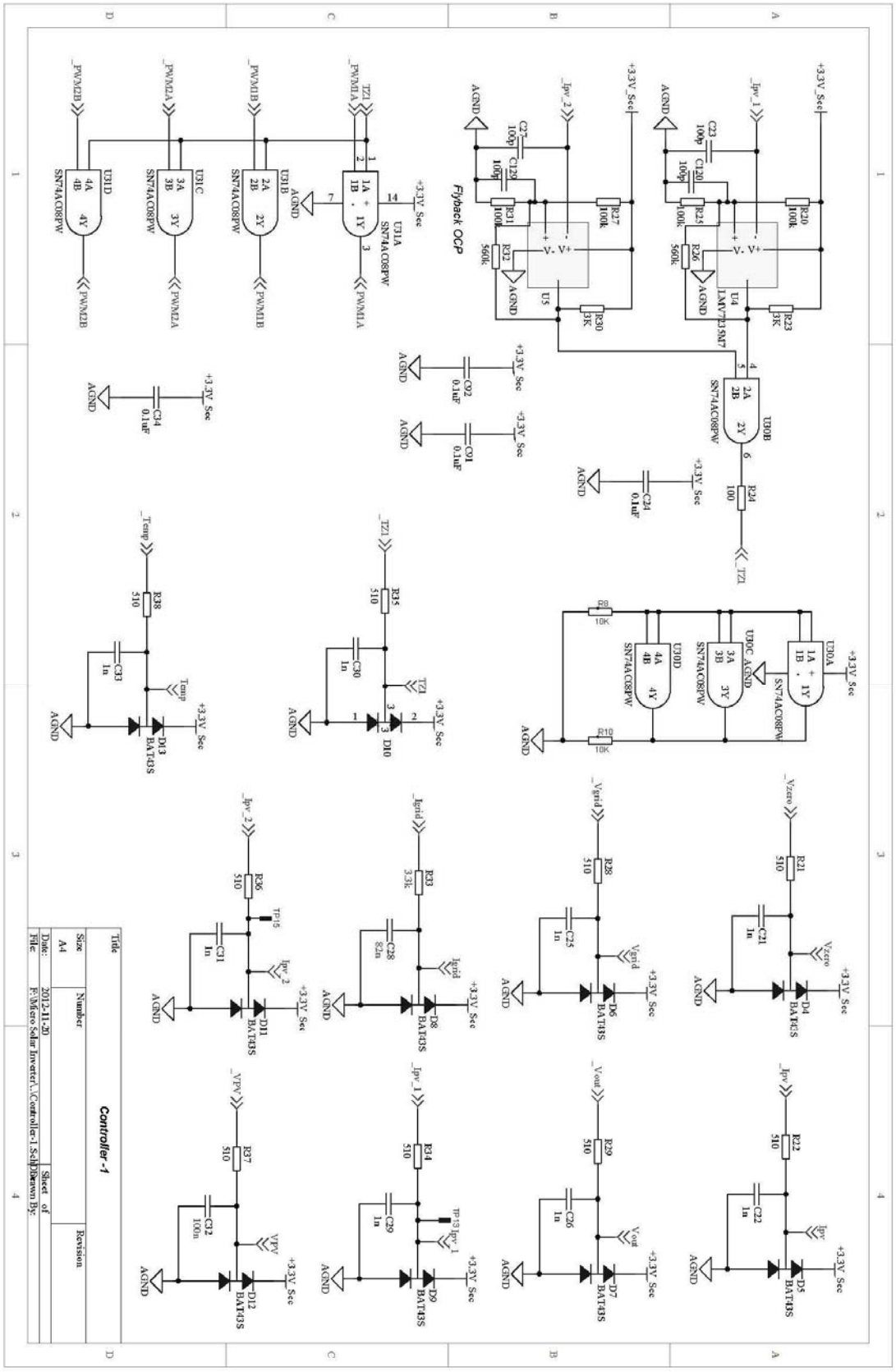
Drawn By:


Grid Voltage Sample
Flyback Output Voltage Sample
Grid Current Sample
PV Current Sample
Grid Voltage Zero Crossing Sample
Detection circuit -2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Number
Revision
Date:
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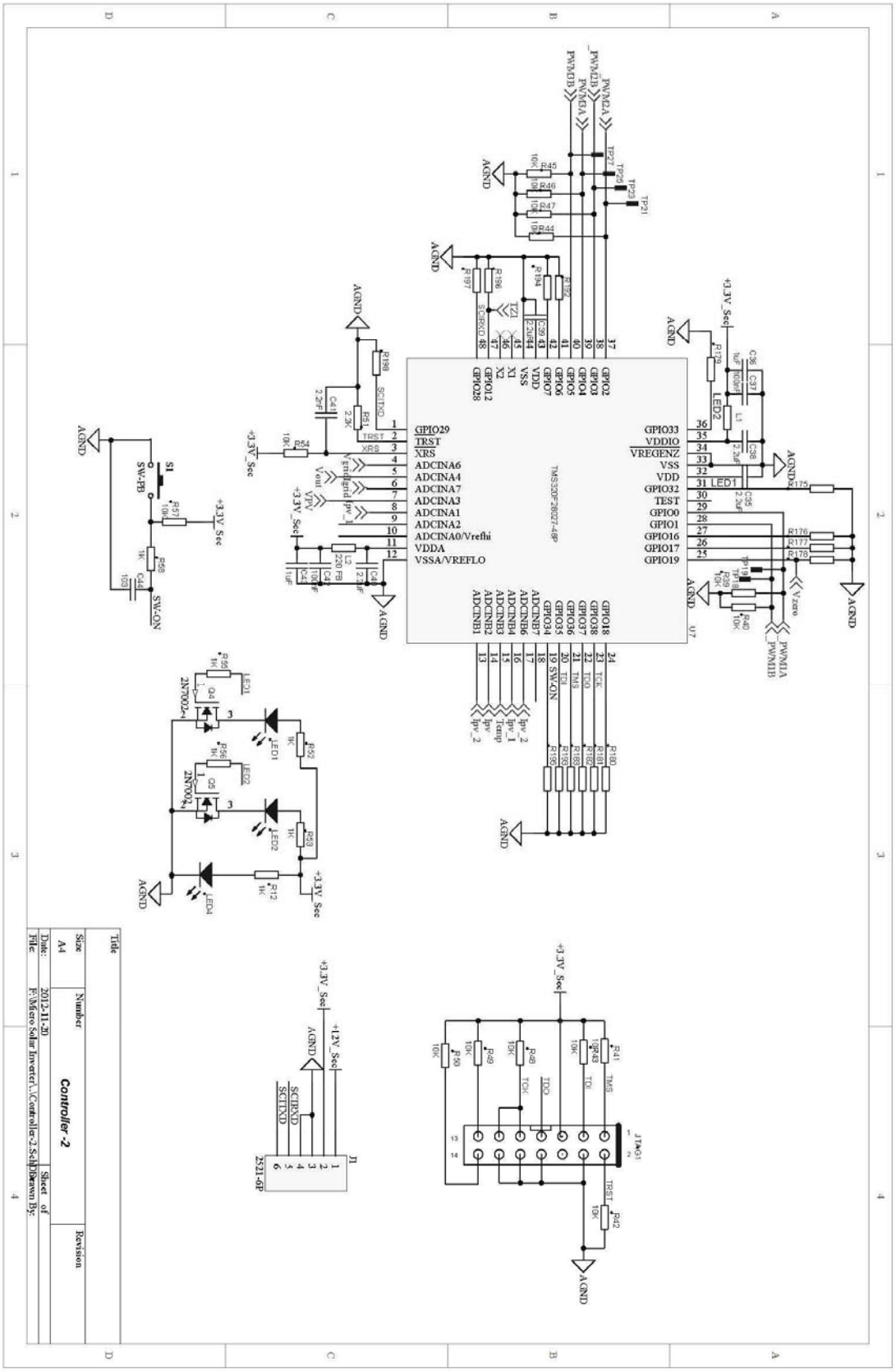
Drawn By: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Revision
Date:
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Drawn By:
TMS320F28027-48P
GPIO29
TRST
XRS
ADCINA6
ADCINA4
ADCINA7
ADCINA3
ADCINA1
ADCINA2
ADCINA0/Vrefhi
VDDA
VSSA/VREFLO
GPIO33
VDDIO
VREGENZ
VSS
VDD
GPIO32
TEST
GPIO0
GPIO1
GPIO16
GPIO17
GPIO19
GPIO18
GPIO28
GPIO37
GPIO36
GPIO35
GPIO34
SW-ON
TCK
TDO
TMS
TDI
Ipv_2
Ipv_1
Temp
Ipv
Vout
Vpv
Vgridgnd
SCITXD
SCIRXD
TZ1
X1
X2
AGND
+3.3V_Sec
+12V_Sec
S1
SW-PB
SW-ON
LED1
LED2
LED3
LED4
2N7002
JTAG1
J1
2521-6P

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Interface	interface.ti.com	Medical	www.ti.com/medical
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