DLPC2607 Software

Programmer's Guide

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DLPC2607 Software Programmer's Guide

This programmer's guide specifies the command and control interface to the DLPC2607 – pico projector chip set. It defines all applicable communication protocols, initialization, default settings, and timing and control register bit definitions.

1 Applicable Documents

This programmer's guide references the following TI document: DLPC2607 ASIC data sheet, TI literature number DLPS030.

The following non-TI documents are for reference only:

- I²C Bus Specification – Philips Semiconductor 1994 Desktop Video Data Handbook
- Appropriate SPI serial flash data sheets

2 Interface Protocol

2.1 Interface Standards

There are two interfaces that can be used for communication with the DLPC2607:

- I²C interface
- SPI, serial flash interface

The I²C interface supports full read and write access to the DLPC2607 ASIC configuration register and mailbox space as well as full read and write access to the SPI serial flash. The flash interfaces do not support flash access. Register and mailbox access is limited to write-only access.

Commands received via the I²C interface are limited to standard, low-level, DLP® defined register and mailbox access commands.

Flash interface write access to the DLPC2607 configuration register and mailbox space is in response to a direct memory access (DMA) request. Such requests are supported from the I²C interface. This DMA feature can be used to upload flash contents to be read via the I²C, to automatically load an embedded DLPC2607 mailbox, or to automatically load a set of DLPC2607 configuration registers. Access to flash memory itself has slightly different restrictions. The I²C interface is the only interface that provides full flash read or write access.

The DLPC2607 provides an auto-initialization engine, which uploads application-specific, configuration data from flash at power-up. Upon the completion of the auto-initialization routine, the DLPC2607 is ready to accept image data in the desired format and over the desired interface with no required additional configuration on the part of the host processor. For details on how to configure auto-initialization, see Section 2.3.2.1.

2.2 I²C Interface

The I²C interface is intended for DLPC2607 projector control. This includes initializing ASIC configuration parameters and loading internal memories. These memories include the initialization and command processor (ICP) memory, white point correction (WPC) memory, DMD reset controller (DRC) memory, DLP® PWM sequence (SEQ) memory, contour mitigation look-up table (CMT) memory, blue noise mask (BNM) memory, sharpness look-up table (SCL) memory, and a splash screen when needed. The I²C interface can download these memories directly or indirectly by initiating a DMA from the external flash.

The I²C protocol used in communicating information to the DLPC2607 consists of a serial data bus conforming to the Philips I²C specification and is rated up to a speed of 400 kHz. There are three sets of I²C commands. One set of commands is for projector control. The second set is for programming the flash in the system. The third set is compound I²C commands, which are serviced by embedded software in DLPC2607. The device ID and status can be read though the I²C interface as well.

2.2.1 Projector Control I²C Commands

The I²C addresses for projector control are 8 bits, followed by an 8-bit sub-address. The address or sub-address, or both, are followed by either writing or reading 32 bits of data. The protocols for I²C projector control read and write are listed in the following:

Write Command:

Address	Sub-Address	Data	
(8-bit)	(8-bit)	(32-bit)	
0x36	0xAA	0xdddddddd	(0xAA = Register address, 0xdddddddd = Write data)

Read Command:

(8-bit)	(8-bit)	(8-bit)	
0x36	0x15	0xAA (register address)	Read part 1 (write address of requested register)
(8-bit)		(32-bit)	
0x37		0xdddddddd	Read part 2 (read data of requested register)

The splash screen, CMT LUT, SCL LUT, BNM LUT, DRC LUT, WPC program code, ICP program code, and sequence LUTs can be configured through the I²C or flash and all but the splash screen can be read back via the I²C. The LUT accesses are grouped according to the clock domain their functional logic is based on.

To access the SCL, CMT, BNM, and splash screen configuration space, the commands are:

Write Command:

To access the address register:

Address	Sub-Address	Data	
(8-bit)	(8-bit)	(32-bit)	
0x36	0xFA	0xdddddddd	(0xdddddddd = LUT address)

To access the configuration register (mailbox select):

Address	Sub-Address	Data	
(8-bit)	(8-bit)	(32-bit)	
0x36	0xFB	0xdddddddd	(0xdddddddd = LUT mailbox select)

To access the data register:

Address	Sub-Address	Data	
(8-bit)	(8-bit)	(32-bit)	
0x36	0xFC	0xdddddddd	(0xdddddddd = LUT write data)

Read Command:

(8-bit)	(8-bit)	(8-bit)	
0x36	0x15	0xFA (register address)	Read part 1 (write address of requested register)
(8-bit)		(32-bit)	
0x37		0xdddddddd	Read part 2 (read data of requested register)

To access the WPC, sequences, and DRC LUT configuration space, the commands are:

Write Command:

To access the address register:

Address (8-bit)	Sub-Address (8-bit)	Data (32-bit)	
0x36	0xFD	0xddddddddd	(0xddddddddd = LUT address)

To access the configuration register (Mailbox select):

Address (8-bit)	Sub-Address (8-bit)	Data (32-bit)	
0x36	0xFE	0xddddddddd	(0xddddddddd = LUT mailbox select)

To access the data register:

Address (8-bit)	Sub-Address (8-bit)	Data (32-bit)	
0x36	0xFF	0xddddddddd	(0xddddddddd = LUT write data)

Read Command:

(8-bit)	(8-bit)	(8-bit)	
0x36	0x15	0xFD (register address)	Read Part 1 (write address of requested register)
(8-bit)		(32-bit)	
0x37		0xddddddddd	Read Part 2 (read data of requested register)

To access the auto init (ICP) configuration space, the commands are:

Write Command:

To access the address register

Address (8-bit)	Sub-Address (8-bit)	Data (32-bit)	
0x36	0xF7	0xddddddddd	(0xddddddddd = LUT address)

To access the configuration register (mailbox select)

Address (8-bit)	Sub-Address (8-bit)	Data (32-bit)	
0x36	0xF8	0xddddddddd	(0xddddddddd = LUT mailbox select)

To access the data register

Address (8-bit)	Sub-Address (8-bit)	Data (32-bit)	
0x36	0xF9	0xddddddddd	(0xddddddddd = LUT write data)

Read Command:

(8-bit)	(8-bit)	(8-bit)	
0x36	0x15	0xF7 (register address)	Read part 1 (write address of requested register)
(8-bit)		(32-bit)	
0x37		0xddddddddd	Read part 2 (read data of requested register)

2.2.1.1 Slave Receive Mode (Write)

When the DLPC2607 is operating in the slave-receiver configuration, the first byte following the start condition is the DLPC2607 device write address (for example 36h). The interface consists of a number of sub-address registers each capable of accepting multiple bytes of data. Each command or sub-address expects a certain number of data bytes, typically four. The number of data bytes for each command or sub-address is described in Section 2.4.1.

2.2.1.2 Slave Receive Mode (Read)

When the DLPC2607 operates in the slave-transmitter mode, the first byte following the start condition is the DLPC2607 device read address (37h). The selected register to read must be specified with a write previously.

2.2.1.3 Reserved Areas

When writing to valid registers, all unused or reserved bits should be set to 0, unless otherwise specified. Reserved registers should never be written to or read from. When reading valid registers, all unused or reserved bits should be ignored.

2.2.2 I²C Control Commands

There are two sets of I²C commands. The first (36h, 37h) are for control of the projector with an option to re-map to 3Ah/3Bh. Control commands, register sub-addresses, and corresponding control bits are specified in the following. Control commands shall be accepted in any order, except when special sequencing is required (for example setting up the flash). Each control command is validated for sub-address and parameter errors as they are received. Commands that fail validation are ignored. On power-up, it is necessary to wait for the DLPC2607 device to complete initialization before sending the device any I²C transactions. The best way to do this is to wait for the GPIO4_INTF to signal that initialization is complete (see Figure 1).

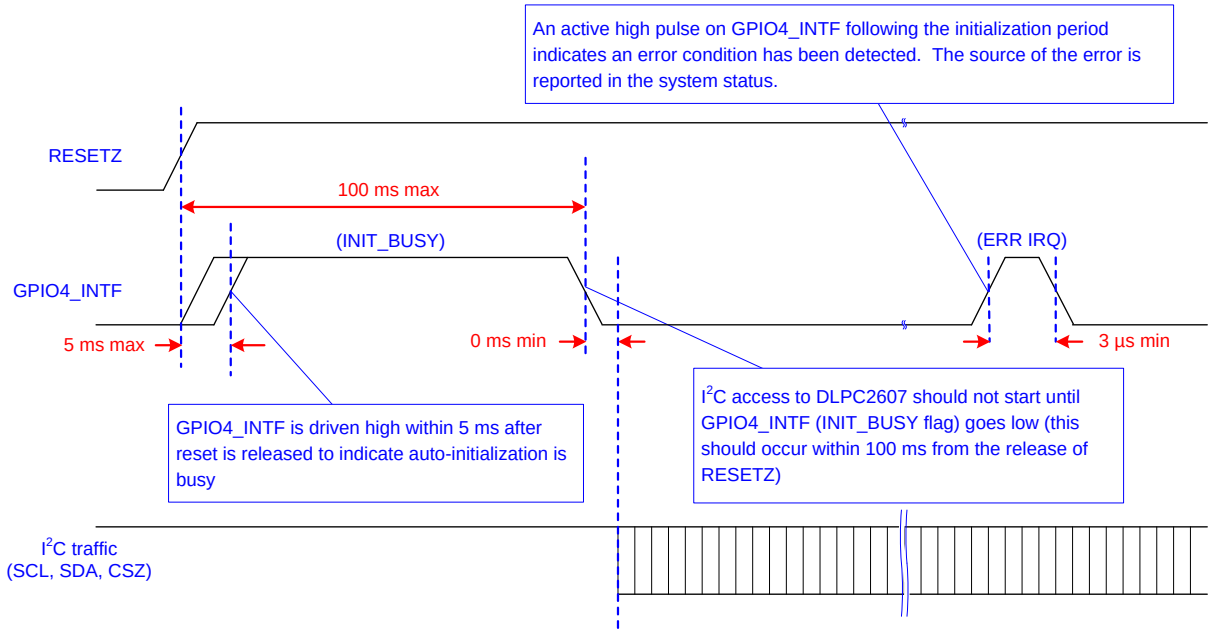


Figure 1.

The I2C_ADDR_SEL pin provides the ability to select the alternate set of I²C device addresses. If I2C_ADDR_SEL pin is low, then 36h/37h are enabled. If I2C_ADDR_SEL pin is high, then 3Ah/3Bh are enabled.

Some commands may cause brief visual artifacts in the display image. Most command data values can be read. Those that cannot be written are marked as read-only.

2.2.3 Using the I²C on the DLPC2607 Reference Design

The DLPC2607 reference design provides several options for supporting I²C communication. For initial system debugging, the recommended method is to use the DLPC2607 GUI tool installed on a standard PC with a USB connection from the PC to a USB-to-I²C board that converts the USB instructions to I²C. For more information, see the DLPC2607 GUI User's Guide, TI literature number DLPU015.

2.3 Flash Interface

The flash interface provides the mechanism through which the DLPC2607 can interface with a variety of external, SPI-based serial flash components. At the hardware level, the serial flash interface is a 5-bit interface composed of a 1-bit input data pin, a 1-bit output data pin, a 1-bit output clock pin, and 2 chip selects. It should be noted that the flash device used for initialization must be connected to chip select 0. At the software level, these flash components can be accessed by a number of different methods.

2.3.1 I²C High-Level Flash Interface

For the I²C interface, a set of new high-level compound I²C commands are available that hide most of the low-level flash controller and mailbox register transactions from the user. For more details, see Section 2.4.1.22.

2.3.2 I²C Low-Level Flash Interface

The low-level flash accesses the flash at the hardware level, making use of register level peak and poke commands. This approach is more tedious and is only recommended when a more abstract equivalent command is not available. The rest of this section describes this low-level interface.

Specific user data, like CMT look-up tables, PWM sequences, DMD reset control look-up table, scalar coefficient data, auto initialization data, and splash screen data are loaded into DLPC2607 from the serial flash. The flash interface can perform nearly any command available to an SPI serial memory device.

The serial flash interface supports the following standard serial flash memory instructions via the I²C:

- Write disable or write enable
- Read status register or write status register
- Fast read
- Sector erase or chip erase
- Page program
- Power-down, release-power-down, device ID
- Fast read parameter page
- Program parameter page or erase parameter page
- Manufacture ID, device ID, JEDEC ID

The only standard flash command not supported by the DLPC2607 is a normal read command. A fast read command must be used in place of a normal read command.

The flash controller also includes a direct memory access (DMA) controller that can be used to write to the same DLPC2607 configuration registers accessible via the I²C interface. The serial flash device can be programmed via the I²C bus through the DLPC2607. The flash contents can also be read via the I²C.

In addition to supporting those external interfaces, the flash interface provides an auto-initialization engine, which uploads application specific, configuration data from flash at power-up. Upon the completion of the auto-initialization routine, the DLPC2607 is ready to accept image data in the desired format and over the desired interface with no required additional configuration on the part of the host processor.

2.3.2.1 Flash Memory Controller Power-Up Initialization

As mentioned earlier, the flash controller automatically performs a DMA read operation to upload auto-initialization code to initialization and command processor (ICP) program memory. The flash start address of the auto-init program is stored at address 0 to 3 (4 bytes) in the flash. The size of the auto-init program (in bytes) is assumed to be stored at address 4 to 7 (4 bytes) in the flash. While the flash controller is performing the initialization operation, no commands from an external host are accepted by the DLPC2607.

Upon release of the external reset signal, the flash memory controller within the DLPC2607 set bit 10 in the main status register (I^2C: 0x03) signifying the start of auto-initialization, and then fetch 8 bytes of size and location data stored at flash addresses 0 through 7. The flash controller then uploads the code defined by these pointers to the auto initialization program memory within the ASIC. After the upload is completed, the flash memory controller clears set bit 10 in the main status register and release the ICP processor to begin auto-initialization program execution. The ICP sets bit 11 in the main status register once initialization is complete. Note that GPIO4_INTF is typically configured as an output Interrupt signal that outputs an active high pulse when auto-initialization is in progress, or when an error condition exists. Auto-initialization and error stats can be read from the interrupt status register.

2.3.2.2 Flash Interface Modes of Operation

To use the flash interface, it is first necessary to set-up the flash interface in its desired mode of operation via I^2C command. The flash interface supports the following modes of operation:

1. Flash DMA to LUT memories (PWM sequences, DMD reset control RAM, WPC LUT CMT tables, BNM threshold table, splash data, scaler (SCL) sharpness coefficient LUTs, and ICP program memory)

   (a) SEQ RAM; 1, 32-bit sequence instruction is mapped to each 32-bit flash word.

Bit 31 Bit 0

SEQ LUT Data 1(31:0)			
Byte 3	Byte 2	Byte 1	Byte 0

   (b) WPC LUT; 1, 32-bit WPC instruction is mapped to each 32-bit flash word.

Bit 31 Bit 0

WPC LUT Data 1(31:0)			
Byte 3	Byte 2	Byte 1	Byte 0

   (c) DMD reset control RAM; 1, 13-bit reset control instruction is mapped to each 32-bit flash word. Bytes 2, 3, and part of byte 1 are zero padded.

Bit 31 Bit 0

Unused		DRC LUT Word 1(12:0)	
X"0000"		b"000" and DRC_Data0(12:0)	
Byte 3	Byte 2	Byte 1	Byte 0

   (d) CMT RAM (gamma or STM dither pattern); 2, 16-bit CMT words are packed in each 32-bit flash word. This table must be configured to match the number of bit splits in the sequence.

Bit 31 Bit 0

CMT Word 1(15:0)		CMT Word 0(15:0)	
Byte 3	Byte 2	Byte 1	Byte 0

   (e) ICP program memory LUT; 1, 32-bit ICP instruction is mapped to each 32-bit flash word.

Bit 31			Bit 0
WPC LUT Data 1(31:0)			
Byte 3	Byte 2	Byte 1	Byte 0

(f) Splash data; 2, 16-bit pixel data are mapped to each 32-bit flash word. Data is assumed to be serially concatenated in GRB order. The pixel stored in the lower word precedes the pixel stored in the upper word in the raster scan order. If the splash pixels per line is not an even number, then the last word for every splash line should be 0 padded.

Bit 31	Bit 16	Bit 15	Bit 0
Splash Pixel 2(15:0)		**Splash Pixel 1(15:0)**	
G1(5:0):R1(4:0):B1(4:0)		G0(5:0):R0(4:0):B0(4:0)	
Byte 3	Byte 2	Byte 1	Byte 0

(g) SCL sharpness coefficient LUTs (separate tables of different sizes, but same format for horizontal and vertical coefficients); 4, 8-bit coefficients are mapped to each 32-bit flash word.

Bit 31			Bit 0
SCL LUT Data 1(31:0)			
SCL Coefficient 4(7:0)	**SCL Coefficient 3(7:0)**	**SCL Coefficient 2(7:0)**	**SCL Coefficient 1(7:0)**
Byte 3	Byte 2	Byte 1	Byte 0

(h) BNM threshold coefficient LUT; 4, 8-bit coefficients are mapped to each 32-bit flash word.

Bit 31			Bit 0
SCL LUT Data 1(31:0)			
BNM Coefficient 4(7:0)	**BNM Coefficient 3(7:0)**	**BNM Coefficient 2(7:0)**	**BNM Coefficient 1(7:0)**
Byte 3	Byte 2	Byte 1	Byte 0

(i) Auto-init RAM; 1, 32-bit instruction is mapped to each 32-bit flash word.

Bit 31			Bit 0
Auto Init LUT Data 1(31:0)			
Byte 3	Byte 2	Byte 1	Byte 0

2. Flash DMA to configuration registers (supports batch file like programming from flash)

(a) The contents shall consist of a linked list of address and data pairs

(i) A single 9-bit configuration address shall be mapped to each 32-bit flash address word. The address defines the configuration register address to which the paired data is written.

(ii) A single N-bit configuration register data word shall be mapped to each 32-bit flash data word.

For example, if a data of FEAD is to be written to the configuration address 9 and data DEADBEEF is to be written to address 1A0, the data should be written to the flash as in this example:

Bit 31			Bit 0
Flash Word 1			
Address Byte 3	Address Byte 2	Address Byte 1	Address Byte 0
x00	x00	x00	x09
Flash Word 2			
Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0
x00	x00	xFE	xAD
Flash Word 3			
Address Byte 3	Address Byte 2	Address Byte 1	Address Byte 0
x00	x00	x01	xA0
Flash Word 4			
Data Byte 3	Data Byte 2	Data Byte 1	Data Byte 0
xDE	xAD	xBE	xEF

3. Flash content reads via I^2C – This can be used on power-up to read the flash ID and status.
4. Flash re-programming via I^2C – This is a multiple-step operation, which involves erasing the desired sector, setting up the write enable to the flash, reading the flash status to see if the flash is write protected, writing to the flash to clear the write protection bit, and finally programming the flash with the desired data.
5. Flash single command operations – This is used to perform operations like WRITE ENABLE or WRITE DISABLE.

2.3.2.3 Flash Interface Set-Up Protocol

To configure the flash in one of the previously mentioned modes of operation, the external host must perform a series of I^2C transactions to the following configuration registers:

1. Flash start address register to identify from where to start the DMA operation in flash
2. Serial flash specific configuration parameters such as opcode, dummy bytes
3. DMA length register to identify how many bytes to transfer from or to the flash for the DMA

The last transaction from the host, before it relinquishes control of the configuration space to the flash interface, must be to configure the flash in one of the modes mentioned in Section 2.4.1.18.1. After configuration control is transferred to the flash controller, the host should poll the flash DMA busy status bit to know if the desired flash operation is complete. If control is transferred back to the host interface before the DMA busy bit is set, then the previous flash transaction is aborted. The user must check if the DMA status bit is cleared before using the flash interface for any further transactions.

2.3.2.3.1 Command Sequence for DMA from Flash to Configuration Register Mailbox

- I^2C write to configuration registers: “flash start address (address 0x79)”, flash ADDR BYTES (address: 0x74), “flash opcode (address 0x78)”, “flash dummy bytes (address 0x75)”, “flash read data byte quantity (address 0x77)”, “flash write data byte quantity (address 0x76)”
- I^2C write to “mailbox sub-address (address 0xFA or 0xFD)” to set LUT sub-address to zero I^2C write to “mailbox control (address 0xFB or 0xFE)” to select the desired mailbox LUT to be loaded
- I^2C write to “mailbox control (address 0xFB or 0xFE)” to select the desired mailbox LUT to be loaded
- I^2C write to “flash mode control (address 0x08)” to select flash DMA to mailbox mode (data = 1) and give control of configuration space to the flash interface
- I^2C read to poll “main status (address 0x03)” to see if DMA is done
  - Repeat at a regular interval until DMA is complete
  - No other configuration access shall be performed via I^2C until the DMA completes, or it aborts
- I^2C write to “flash mode control (address 0x08)” to place the flash controller back in idle mode (data = 0)

2.3.2.3.2 Command Sequence for DMA from Flash to Configuration Register Space

- I^2C write to configuration registers: “flash start address (address 0x79)”, flash ADDR BYTES (address: 0x74), “flash opcode (address 0x78)”, “flash dummy bytes (address 0x75)”, “flash read data byte

quantity (address 0x77)", "flash write data byte quantity (address 0x76)"

- I²C write to "flash mode control (address 0x08)" to select flash DMA to configuration space (data = 2) and give control of configuration space to the flash interface
- I²C read to poll "main status (address 0x03)" (I²C register) to see if DMA is done
  - Repeat at a regular interval until DMA is complete
  - No other configuration access shall be performed via I²C until the DMA completes, or it aborts
- I²C write to "flash mode control (address 0x08)" to place the flash controller back in idle mode (data = 0)

2.3.2.3.3 Flash Read Command Sequence

- I²C write to configuration registers: "flash start address (address 0x79)", flash ADDR BYTES (address: 0x74), "flash opcode (address 0x78)", "flash dummy bytes (address 0x75)", "flash read data byte quantity (address 0x77)", "flash write data byte quantity (address 0x76)"
- I²C write to "flash mode control (address 0x08)" to select to select flash read mode (data = 3) and give control of configuration space to the flash interface
- I²C read of the flash read data register (address 0x07) (I²C read returns contents of 32 bits flash data per address)
- Repeat I²C reads until the pre-defined byte count is reached. If more I²C reads were performed than defined in the DMA length, then the last data is repeated
- I²C poll of main status register (address 0x03) to check if the flash transactions is complete
  - No other configuration access shall be performed via I²C until the DMA completes, or it aborts
- I²C write to "flash mode control (address 0x08)" to place the flash controller back in idle mode (data = 0)

2.3.2.3.4 Flash Write Command Sequence (Erasing or Programming the Flash)

- **Read flash status register to check if the flash is write protected:**
  - I²C write to configuration registers: "flash start address (address 0x79)", flash ADDR BYTES (Address: 0x74), "flash opcode (address 0x78)", "flash dummy bytes (address 0x75)", "flash read data byte quantity (address 0x77)", "flash write data byte quantity (address 0x76)"
  - Set flash opcode (address 0x78) to READ_STATUS (refer flash spec for value) to check whether the flash is write protected and "read data byte quantity (address 0x77)" = 1
  - I²C write to "flash mode control (address 0x08)" to select flash read mode (data = 3) and give control of configuration space to the flash interface
  - I²C poll of main status register (address 0x03) to check if the flash transaction is complete
    - No other configuration access shall be performed via I²C until the DMA completes, or it aborts
  - I²C write to "flash mode control (address 0x08)" to place the flash controller back in idle mode (data = 0)
- **Clear flash write protection if flash is write protected:**
  - I²C write to configuration registers: "flash start address (address 0x79)", flash ADDR BYTES (address: 0x74), "flash opcode (address 0x78)", "flash dummy bytes (address 0x75)", "flash read data byte quantity (address 0x77)", "flash write data byte quantity (address 0x76)"
  - I²C write to flash opcode (address 0x78) to WRITE_ENABLE (refer to flash spec for value)
  - I²C write to "flash mode control (address 0x08)" to select flash command mode (data = 5) and give control of configuration space to the flash interface
  - I²C poll of main status register (address 0x03) to check if the flash transaction is complete
    - No other configuration access shall be performed via I²C until the DMA completes, or it aborts
  - I²C write to "flash mode control (address 0x08)" to place the flash controller back in Idle mode (data = 0)
  - I²C write to the flash opcode (address 0x78) register set it up to clear the write protection (refer to flash spec for value)

- I²C write of 1 to the “write data byte quantity (address 0x76)”
- I²C write to configuration registers: “flash start address (address 0x79)”, “flash dummy bytes (address 0x75)”
- I²C write to “flash mode control (address 0x08)” to select flash write mode (data = 4) and give control of configuration space to the flash interface
- I²C poll of main status register (address 0x03) to check if the flash transaction is complete
  - No other configuration access shall be performed via I²C until the DMA completes, or it aborts
- I²C write to “flash mode control (address 0x08)” to place the flash controller back in idle mode (data = 0)

- **If flash write protection is not set, erase the desired sector or block flash:**
  - I²C write to configuration registers: “flash start address (address 0x79)”, flash ADDR BYTES (address: 0x74), “flash opcode (address 0x78)”, “flash dummy bytes (address 0x75)”, “flash read data byte quantity (address 0x77)”, “flash write data byte quantity (address 0x76)”
  - I²C write to flash opcode (address 0x78) to WRITE_ENABLE (refer to flash spec for value)
  - I²C write to “flash mode control (address 0x08)” to select flash command mode (data = 5) and give control of configuration space to the flash interface
  - I²C poll of status register (address 0x03) to check if the flash transaction is complete
    - No other configuration access shall be performed via I²C until the DMA completes, or it aborts
  - I²C write to “flash mode control (address 0x08)” to place the flash controller back in Idle mode (data = 0)
  - I²C write to configuration registers: “flash start address (address 0x79)”, “flash opcode (address 0xD8 – for block erase or 0x20 for sector erase)”, “flash dummy bytes (address 0x75)”, “flash write data byte quantity (address 0x76)”
  - I²C write to “flash mode control (address 0x08)” to select flash command mode (data = 5) and give control of configuration space to the flash interface
  - I²C poll of status register (address 0x03) to check if the flash transaction is complete
    - No other configuration access shall be performed via I²C until the DMA completes, or it aborts
  - I²C write to “flash mode control (address 0x08)” to place the flash controller back in idle mode (data = 0)
- **Read flash status register to check if flash has finished erasing**:
  - I²C write to configuration registers: “flash start address (address 0x79)”, flash ADDR BYTES (address: 0x74), “flash dummy bytes (address 0x75)”, “flash write data byte quantity (address 0x76)”
  - Set flash opcode (address 0x78) to READ_STATUS (refer to flash spec for value) to check whether the erase or write in progress flag and “read data byte quantity (address 0x77)” = 1
  - I²C write to “flash mode control (address 0x08)” to select flash read mode (data = 3) and give control of configuration space to the flash interface
  - I²C poll of status register (address 0x03) to check if the erase or write in progress flag is ‘0’
  - I²C write to “flash mode control (address 0x08)” to place the flash controller back in idle mode (data = 0)
  - This entire sequence should be repeated until the erase or write in progress flag is ‘0’
- **After erasing the flash program it (256 bytes at a time for page program)**:
  - I²C write to configuration registers: “flash start address (address 0x79)”, flash ADDR BYTES (address: 0x74), “flash opcode (address 0x78)”, “flash dummy bytes (address 0x75)”, “flash read data byte quantity (address 0x77)”, “flash write data byte quantity (address 0x76)”
  - I²C write to “flash mode control (address 0x08)” to select flash write mode (data = 4) and give control of configuration space to the flash interface
  - Write flash data 4 bytes at a time through the I²C interface (data should be written to register 0x7B) until the bytes specified in “write data byte” quantity has been reached.
  - I²C poll of status register (address 0x03) to check if the flash transaction is complete

- No other configuration access shall be performed via I²C until the DMA completes, or it aborts

– I²C write to “flash mode control (address 0x08)” to place the flash controller back in idle mode (data = 0)

- **Read flash status register to check if flash has finished programming**:
  – I²C write to configuration registers: “flash start address (address 0x79)”, flash ADDR BYTES (address: 0x74), “flash dummy bytes (address 0x75)”, “flash write data byte quantity (address 0x76)”. Note that the flash device is limited to page programming thus the data byte quantity must be limited by the distance from the start address to the end of the 256 byte page containing the start address. Hence, this process must be repeated for every page until the desired address space is programmed.
  – Set FLASH opcode (address 0x78) to READ_STATUS (refer to flash spec for value) to check whether the erase or write in progress flag and “read data byte quantity (address 0x77)” = 1
  – I²C write to “flash mode control (address 0x08)” to select flash read mode (data = 3) and give control of configuration space to the flash interface
  – I²C poll of status register (address 0x03) to check if the erase or write in progress flag is ‘0’
  – I²C write to “flash mode control (address 0x08)” to place the flash controller back in idle mode (data = 0)
  – This entire sequence should be repeated until the erase or write in progress flag is ‘0’

2.4 I²C, Flash Access Projector Control Commands

2.4.1 Configuration Register Projector Control Commands

The following sections define all DLPC2607 supported configuration registers and associated control parameters. Some registers are further broken down into fields. Note that flash accessibility is defined in the subsection title and I²C access is always supported. Associate addressing for each access interface is also provided in the subsection title.

The type column in the following tables defines the supported access type. A type ‘wr’ field indicates that the field is both write and read accessible. A type ‘r’ field indicates that the field is read-only. Writes to these fields have no effect. A type ‘s’ field indicates a latched STATUS bit. Reading a ‘1’ in this field type means that the signal has gone high since it was last cleared. Writing a ‘1’ to this field clears the status bit.

The reset column in the following tables defines the default value of the command register immediately after power-up due to the power-up reset internal operation of the DLPC2607.

When writing to valid registers, all unused or reserved bits should be set to 0 unless specified otherwise. All undefined register addresses should be assumed to be reserved. Reserved registers should never be written to because some locations are for DLP® use only.

2.4.1.1 Interrupt Status Register Set 1 (I²C: 0x00/0x01, Not Accessible via Flash)

Note: The interrupt status register is mapped to two addresses: x000 and x001. Reading either returns the same value.
When being written: 0 = No effect. 1 = Sets or clears the interrupt.
When being read (interrupt status): 0 = Interrupt is not active. 1 = Interrupt is active.

Bits	Description	Reset	Type
0	Sequencer Abort Status Flag 0 = No abort 1 = Sequencer abort has occurred	b0	r
1	DMD Reset Waveform Controller Overrun Error Flag 0 = No error has occurred 1 = Reset waveform controller overrun has occurred	b0	r
2	DMD Reset Controller Reset Block Error Flag 0 = No error has occurred 1 = Multiple overlapping bias/ reset operations are accessing the same DMD block	b0	r

Bits	Description	Reset	Type
3	DMD Reset Controller I/F Overrun Error Flag 0 = No error has occurred 1 = Overlapping DMD reset requests have been detected and can not be supported across the serial interface	b0	r
4	Formatter Read Buffer Overflow 0 = No error has occurred 1 = Formatter read buffer has overflowed	b0	r
5	Formatter (CMB) Starvation Error 0 = No error has occurred 1 = Formatter (CMB) starvation error has occurred	b0	r
6	Reserved	b0	r
7	Flash Memory Controller FIFO Error 0 = No error has occurred 1 = Flash memory controller FIFO errors occurred	b0	r
8	Flash Memory Controller DMA abort 0 = No error has occurred 1 = Flash memory controller DMA abort has occurred	b0	r
9	Formatter (CMB) Multiple Errors 0 = No error has occurred 1 = Formatter (CMB) multiple error occurred	b0	r
10	Formatter (CMB) Command Error 0 = No error has occurred 1 = Formatter (CMB) command error occurred	b0	r
11	Formatter (CMB) Queue Warning 0 = No error has occurred 1 = Formatter (CMB) queue warning occurred	b0	r
12	mDDR Memory Controller BP-Write FIFO Overflow 0 = No error has occurred 1 = mDDR memory controller BP-write FIFO overflowed	b0	r
13	mDDR Memory Controller FB-Write FIFO Overflow No Data 0 = No error has occurred 1 = mDDR memory controller FB-write FIFO overflowed	b0	r
14	Scaler Line Count Error 0 = No error has occurred 1 = The number of lines in a frame was less than expected occurred	b0	r
15	Scaler Pixel Count Error 0 = No error has occurred 1 = The number of pixels in a line was less than expected occurred	b0	r
16	Reserved	b0	r
17	Reserved	b0	r
18	LED Timeout Error 0 = No error has occurred 1 = LED timeout error occurred (that is a given color was continuously enabled for > 18 ms)	b0	r

2.4.1.2 Main Status Register (I^2C: 0x03, Not Accessible via Flash)

The main status register provides non-latched DLPC2607 status information.

Table 1. (1)

Bits	Description	Reset	Type
2:0	Contains the device ID, the state of the flash DMA operation Bit 7:0 Indicates device ID DLPC2607 ID = x8A Bit 8(1) Indicates DMA STATUS 1 = Busy 0 = Current operation is complete Bit 9 Reserved		s

(1) Bit 8 should be polled following the initiation of a flash memory controller DMA operation to determine when it is complete because no other flash memory controller operation can be requested during a DMA transaction or the DMA is aborted.

Table 1. (1) (continued)

Bits	Description	Reset	Type
	Value is a don't care Bit 10(2) Indicates the flash controller is performing initialization. 0 = Initialization complete 1 = Flash controller performing initialization Bit 11(2) Indicates when auto-initialization is complete. 0 = Auto initialization is in progress 1 = Auto initialization is complete (or was bypassed) Bit 12 Indicates LED timeout status 0 = No time has occurred 1 = LED timeout error occurred (that is, a given color was continuously enabled for > 18 ms)		

(2) Bits 10 and 11 can be polled following the release of reset, for I²C applications only, to determine when auto-initialization is complete. When bit 10 = 0 and bit 11 = 1, then initialization is complete. Alternatively, GPIO4_INTF can be monitored for an active high pulse.

2.4.1.3 Input Source Selection: (I²C: 0x0B, Flash :0x0000000B)

Bits	Description	Reset	Type
2:0	Select the input source and interface mode: 0 - Parallel I/F 1 - Internal test pattern 2 - Splash screen 3 - Reserved 4 - BT.656 I/F Other - RESERVED	x2	wr

Further clarification on the previous five options:

0: The parallel interface supports both RGB and YCrCb data formats. Frames are assumed to be periodic in nature.

1: Internal test pattern generation provides a set of predefined images that are sent to the display on a periodic basis. Command 0x11 is used to select the test pattern type. However, supported test pattern source resolution is a function of DMD display resolution (as defined in Section 2.4.1.10).

2: Splash screens are single-frame, still images stored in flash that are uploaded upon command. However, supported splash screen resolution is a function of DMD resolution (as defined in Section 2.4.1.6). TI recommends QWVGA resolution for all WVGA and nHD applications to minimize flash storage requirements. TI recommends QVGA resolution for all VGA applications. Note that splash images can also be sent to the DLPC2607 directly via the I²C, but this can be very slow.

3: BT.656 – Embedded syncs are assumed (non-external syncs are accepted). Supports only NTSC and PAL input resolutions. (Note that the PDM_CVS_TE sideband signal masks BT.656 data if not appropriately tied off). BT.656 support is only available for DLPC2607. YCrCb to RGB color space conversion and 4:2:2 to 4:4:4 chroma interpolation (both controlled via I²C: 0xC3) must be enabled when BT.656 is selected.

NOTE: The pixel format command (0x0D) must use one of the allowed pixel formats for the interface mode being selected via the input source and interface mode command.

2.4.1.4 YCrCb Source Control

2.4.1.4.1 Source Color Space and Sampling Control (I²C: 0xC3, Flash :0x000000C3)

This register must be configured to match the color space and sampling attributes on the source.

Bits	Description	Reset	Type
0	Reserved Set to 0	b0	wr
1	YCrCb 4:2:2 to 4:4:4 Chroma Interpolation Function Enable (See (1) (2)) 0 = Function disabled 1 = Function enabled	b0	wr
2	YCrCb to RGB Color Space Conversion Function Enable (See (3) (4)) 0 = Function disabled 1 = Function enabled	b0	wr
5:03	Reserved Must be set to 0	b000	wr

(1) 4:2:2 to 4:4:4 chroma interpolation is only valid for YCrCb source.
(2) The partial image horizontal start address must be *even* for YCrCb 4:2:2 source data.
(3) When enabled, YCrCb to RGB control register (I^2C: 0xA4) and the YCrCb 4:2:2 to 4:4:4 chroma interpolation parameter (I^2C: 0xC3 above) must be set appropriately.
(4) Both the YCrCb 4:2:2 to 4:4:4 chroma interpolation parameter and the YCrCb to RGB color space conversion parameter must be set for BT.656 operation.

2.4.1.4.2 YCrCb To RGB Control (I^2C: 0xA4, Flash :0x000000A4)

This register must be configured to match the attributes on a YCrCb source. This register only applies when YCrCb to RGB color space conversion (I^2C: 0xC3) is enabled.

Bits	Description	Reset	Type
0	YCrCb to RGB Color Space Select 0= BT.601 color space 1= BT.709 color space	b0	wr
1	YCrCb to RGB Dynamic Range Select 0= YCrCb source with 0 to 255 dynamic range on all three components 1= YCrCb source with 16 to 240 Y and –112 to +112 CrCb	b1	wr
2	YCrCb to RGB Input Luma Offset Select 0= YCrCb input luma offset = '0' 1= YCrCb input luma offset = '–16'	b1	wr
3	YCrCb to RGB Input Chroma Offset Binary Select 0= YCrCb chroma is input as a 'signed' value (set input chroma offset to '0') 1= YCrCb chroma is input as an 'offset binary value (set input chroma offset to '–128')	b1	wr

2.4.1.4.3 Chroma Channel Swap (I^2C: 0x33, Flash :0x00000033)

This register applies to both 4:2:2 and 4:4:4 YCrCb data sources. It allows the Cr and Cb chroma data received from the source to be swapped. The reference Cb/Cr order for a YCrCb 4:2:2 input is assumed to be Cb/Cr. Thus, setting this changes the order to Cr/Cb. For YCrCb 4:4:4 this bit also swaps the input channels.

Bits	Description	Reset	Type
0	Chroma Channel Cr/Cb Swap 0 = Chroma channel swap disabled (for YCrCb 4:2:2 input = Cb/Cr) 1 = Chroma channel swap enabled (for YCrCb 4:2:2 input = Cr/Cb)	b0	wr

2.4.1.5 Pixel Data Format Select: (I^2C: 0x0D, Flash :0x0000000D)

Bits	Description				Type	Notes
3:0	Select the pixel format				wr	
		Parallel	Test Pattern	Splash	BT.656	See (1)
	0 - RGB565 transferred on a 16-bit bus	Y	no	Y	no	

(1) This parameter is actually ignored for test pattern and splash applications. internal test patterns are assumed to be RGB888 regardless of this pixel format setting. Splash is assumed to be RGB565 regardless of this pixel format setting.

Bits	Description				Type	Notes
	1 - RGB666 or 4:4:4 YCrCb666 transferred on an 18-bit bus	Y	no	no	no	See (2)
	2 - RGB888 or 4:4:4 YCrCb888 on a 24-bit bus, or 4:2:2 YCrCb880 on a 24-bit bus	Y	Y	no	Y	See (2)(3)
	3 - RGB565 transferred on an 8-bit bus	no	no	no	no	See (4)
	4 - RGB888 or 4:4:4 YCrCb888 transferred on an 8-bit bus (1 pixel over 3 clocks)	no	no	no	no	See (4)(2)
	5 - RGB888 or 4:4:4 YCrCb888 transferred on a 16-bit bus (2 pixel over 3 clocks)	no	no	no	no	See (4)(2)
	6 - RGB666 transferred on an 8-bit bus (1 pixel over 3 clocks)	no	no	no	no	See (4)
	7 - RGB666 transferred on a 16-bit bus (2 pixel over 3 clocks)	no	no	no	no	See (4)
	8 - 4:2:2 YCr/Cb transferred on a 16-bit bus (8-bit Y and 8-bits Cr/Cb)	no	no	no	no	See (4)(2)
	9 - 4:2:2 YCr/Cb transferred on an 8-bit bus (8-bit Y and 8-bits Cr/Cb) (1 pixel over 2 clocks)	no	no	no	no	See (4)(2)
	Other - Reserved	N/A	N/A	N/A	N/A	

(2) RGB vs YCrCb source selection is made via I^2C address 0xC3

(3) Although the BT.656 source selection is option 2, YCrCb888 on a 24-bit bus, data is actually only input on the 8 LSBs of the 24-bit PDATA bus.

(4) The horizontal width must be even when using data formats 3 to 9. Thus, the 427 × 240 and 853 × 480 source resolutions are not supported for these data formats.

2.4.1.6 Input Resolution Select: (I^2C: 0x0C, Flash :0x0000000C)

Yellow highlighting (with a table note) indicates the displayed image does not fill the entire DMD. All input resolutions and orientations listed in the following table apply to both parallel buses.

Table 2. Supported Input and Output Resolutions for the 0.3 WVGA DMD

Bits	Description					Reset	Type	Notes
4:0	Select the input resolution:					d1	wr	See (1)
	Input Resolution Options (decimal)	**Source Resolution**		**Display Non-Rotated**		**Display Rotated**		
		H	**V**	**H**	**V**	**H**	**V**	See (2)
	0 – QVGA portrait	240	320	360(3)	480	640(3)	480	See (4)
	1 – QVGA landscape	320	240	640(3)	480			See (4)
	2 – QWVGA portrait	240	427	270	480	853	480	See (4) (5)
	3 – QWVGA landscape	427	240	853	480			See (6)
	4 – 2:3 VGA portrait	430	640	322(3)	480	714(3)	480	See (4)
	5 – 3:2 VGA landscape	640	430	716(3)	480			See (4)
	6 – VGA portrait	480	640	360(3)	480	640	480	See (4)
	7 – VGA landscape	640	480	640(3)	480			See (4)
	8 – WVGA-720 portrait	480	720	320(3)	480	720(3)	480	See (4)
	9 – WVGA-720 landscape	720	480	720(3)	480			See (4)
	10 – WVGA-752 portrait	480	752	306(3)	480	752(3)	480	See (4)
	11 – WVGA-752 landscape	752	480	752(3)	480			See (4)
	12 – WVGA-800 portrait	480	800	288(3)	480	800(3)	480	See (4)
	13 – WVGA-800 landscape	800	480	800(3)	480			See (4)
	14 – WVGA-852 portrait	480	852	270(3)	480	853	480	See (4)
	15 – WVGA-852 landscape	852	480	853	480			
	16 – WVGA-853 portrait	480	853	270(3)	480	853	480	See (4)
	17 – WVGA-853 landscape	853	480	853	480			See (6)

(1) See Section 2.4.1.3 for input sources resolution restrictions

(2) Unless otherwise noted, all display resolutions are the Manhattan equivalent (dia = diamond)

(3) The displayed image does not fill the entire DMD

(4) Horizontal display resolutions less than 853 are centered with black borders

(5) Non-rotated portrait QWVGA is not supported for WXGA DMD due to a known hardware bug

(6) The DLPC2607 does not support an odd number of active, full-image, pixels per line in partial buffer mode. Thus, 427 × 480 and 853 × 480 resolutions are not supported for partial buffer mode.

Table 2. Supported Input and Output Resolutions for the 0.3 WVGA DMD (continued)

Bits	Description					Reset	Type	Notes
	18 – WVGA-854 portrait	480	853	270[3]	480	853	480	See [4]
	19 – WVGA-854 landscape	854	480	853	480			
	20 – WVGA-864 portrait	480	854	270[3]	480	853	480	See [4]
	21 – WVGA-864 landscape	864	480	853	480			
	22 – Reserved							
	23 – NTSC landscape	720	240	640[3]	480			See [4] [7]
	24 – Reserved							
	25 – PAL landscape	720	288	640[3]	480			See [4] [7]
	26 – nHD portrait	360	640	270	480	853	480	See [4]
	27 – nHD landscape	640	360	853	480			
	28 – Reserved							
	29 - WVGA-854 landscape input or VGA output	854	480	640[3]	480			See [4]
	30 to 34 – Reserved							
	35 – WVGA DMD optical test landscape	608 Dia	684 Dia	608 Dia	684 Dia			See [8]
	Others – Reserved							

[7] BT.656 source port only; interlaced

[8] All WVGA DMD optical test images are assumed to map 1:1 to the diamond WVGA DMD device. For proper processing, these images must be remapped to a 608h × 684v orthogonal resolution. To do this, the optical test image file must be compacted horizontally. To compact horizontally, the half-pixel shift between *vertical rows* is simply removed. Prior to horizontal compacting, it is assumed that the diamond image has the same phase as the DMD. Specifically, the top line (along with all other odd lines) of the diamond image are assumed to be shifted a half pixel to the right relative to the second line (and all other even lines) of the diamond image. This diamond phase orientation also requires that the image flip long-axis parameter (I^2C: 0x0F) and image flip short-axis parameter (I^2C: 0x10) to be set to the same value.

Yellow highlighting (with a table note) indicates the displayed image does not fill the entire DMD. All input resolutions and orientations listed in the following table apply to both parallel buses.

Table 3. Supported Input and Output Resolutions for the 0.24 VGA DMD

Bits	Description					Reset	Type	Notes
4:0	Select the input resolution:					d1	wr	See [1]
	Input Resolution Options (decimal)	**Source Resolution**		**Display Non-Rotated**		**Display Rotated**		
		H	**V**	**H**	**V**	**H**	**V**	See [2]
	0 - QVGA portrait	240	320	360[3]	480	640	480	See [4]
	1 – QVGA landscape	320	240	640	480			See [4]
	2 – QWVGA portrait	240	427					See [4] [5]
	3 – QWVGA landscape	427	240					See [6]
	4 – 2:3 VGA portrait	430	640					See [4]
	5 – 3:2 VGA landscape	640	430					See [4]
	6 – VGA portrait	480	640	360[3]	480	640	480	See [4]
	7 – VGA landscape	640	480	640	480			See [4]
	8 – WVGA-720 portrait	480	720					See [4]
	9 – WVGA-720 landscape	720	480					See [4]
	10 – WVGA-752 portrait	480	752					See [4]
	11 – WVGA-752 landscape	752	480					See [4]
	12 – WVGA-800 portrait	480	800					See [4]
	13 – WVGA-800 landscape	800	480					See [4]
	14 – WVGA-852 portrait	480	852					See [4]

[1] See Section 2.4.1.3 for input sources resolution restrictions

[2] Unless otherwise noted, all display resolutions are the Manhattan equivalent (dia = diamond)

[3] The displayed image does not fill the entire DMD

[4] Horizontal display resolutions less than 853 are centered with black borders

[5] Non-rotated portrait QWVGA is not supported for WXGA DMD due to a known hardware bug

[6] The DLPC2607 does not support an odd number of active, full-image, pixels per line in partial buffer mode. Thus, 427 × 480 and 853 × 480 resolutions are not supported for partial buffer mode.

Table 3. Supported Input and Output Resolutions for the 0.24 VGA DMD (continued)

Bits	Description					Reset	Type	Notes
	15 – WVGA-852 landscape	852	480					
	16 – WVGA-853 portrait	480	853					See (4)
	17 – WVGA-853 landscape	853	480					See (6)
	18 – WVGA-854 portrait	480	853					See (4)
	19 – WVGA-854 landscape	854	480					
	20 – WVGA-864 portrait	480	854					See (4)
	21 – WVGA-864 landscape	864	480					
	22 –Reserved							
	23 – NTSC landscape	720	240	640	480			See (4) (7)
	24 – Reserved							
	25 – PAL landscape	720	288	640	480			See (4) (7)
	26 – nHD portrait	360	640					See (4)
	27 – nHD landscape	640	360					
	28 – Reserved							
	29 – WVGA-854 landscape input or VGA output	854	480	640	480			See (4)
	30 to 34 – Reserved							
	35- VGA DMD optical test landscape. (Note that a WVGA pattern is input but only the center 456 × 684 VGA region is displayed)	608 Dia	684 Dia	608 Dia	684 Dia			See (8)
	Others – Reserved							

(7) BT.656 source port only; interlaced

(8) All WVGA DMD optical test images are assumed to map 1:1 to the diamond WVGA DMD device. For proper processing, these images must be remapped to a 608h × 684v orthogonal resolution. To do this, the optical test image file must be compacted horizontally. To compact horizontally, the half-pixel shift between *vertical rows* is simply removed. Prior to horizontal compacting, it is assumed that the diamond image has the same phase as the DMD. Specifically, the top line (along with all other odd lines) of the diamond image are assumed to be shifted a half pixel to the right relative to the second line (and all other even lines) of the diamond image. This diamond phase orientation also requires that the image flip long-axis parameter (I^2C: 0x0F) and image flip short-axis parameter (I^2C: 0x10) to be set to the same value.

Note that in general, the VGA DMD application can be used the same as a WVGA DMD with the understanding that any display image widths wider than 640 pixels are centered and cropped to 640 when displayed on the VGA DMD.

Yellow highlighting (with a table note) indicates the displayed image does not fill the entire DMD. All input resolutions and orientations listed in the following table apply to both parallel buses.

Table 4. Supported Input and Output Resolutions for the 0.2 nHD DMD

Bits	Description					Reset	Type	Notes
4:0	Select the input resolution:					d1	wr	See (1)
	Input Resolution Options (decimal)	**Source Resolution**		**Display Non-Rotated**		**Display Rotated**		
		H	**V**	**H**	**V**	**H**	**V**	See (2)
	0 - QVGA portrait	240	320	270 (3)	360	480 (3)	360	See (4)
	1 – QVGA landscape	320	240	480 (3)	360			See (4)
	2 – QWVGA portrait	240	427	202 (3)	360	640	360	See (4)
	3 – QWVGA landscape	427	240	640	360			See (5)
	4 – 2:3 VGA portrait	430	640	242 (3)	360	536 (3)	360	See (4)
	5 – 3:2 VGA landscape	640	430	536 (3)	360			See (4)
	6 – VGA portrait	480	640	270 (3)	360	480 (3)	360	See (4)
	7 – VGA landscape	640	480	480 (3)	360			See (4)
	8 – WVGA-720 portrait	480	720	240 (3)	360	540 (3)	360	See (4)

(1) See Section 2.4.1.3 for input sources resolution restrictions

(2) Unless otherwise noted, all display resolutions are the Manhattan equivalent (dia = diamond)

(3) The displayed image does not fill the entire DMD

(4) Horizontal display resolutions less than 640 are centered with black borders

(5) The DLPC2607 does not support an odd number of active, full-image, pixels per line in partial buffer mode. Thus, 427 × 480 and 853 × 480 resolutions are not supported for partial buffer mode.

Table 4. Supported Input and Output Resolutions for the 0.2 nHD DMD (continued)

Bits	Description					Reset	Type	Notes
	9 – WVGA-720 landscape	720	480	540[3]	360			See [4]
	10 – WVGA-752 portrait	480	752	230[3]	360	564	360	See [4]
	11 – WVGA-752 landscape	752	480	564[3]	360			See [4]
	12 – WVGA-800 portrait	480	800	216[3]	360	600[3]	360	See [4]
	13 – WVGA-800 landscape	800	480	600[3]	360			See [4]
	14 – WVGA-852 portrait	480	852	202[3]	360	640	360	See [4]
	15 – WVGA-852 landscape	852	480	640	360			
	16 – WVGA-853 portrait	480	853	202[3]	360	640	360	See [4]
	17 – WVGA-853 landscape	853	480	640	360			See [5]
	18 – WVGA-854 portrait	480	853	202[3]	360	640	360	See [4]
	19 – WVGA-854 landscape	854	480	640	360			
	20 – WVGA-864 portrait	480	864	202[3]	360	640	360	See [4]
	21 – WVGA-864 landscape	864	480	640	360			
	22 – Reserved							
	23 – NTSC landscape	720	240	480[3]	360			See [4] [6]
	24 – Reserved							
	25 – PAL landscape	720	288	480[3]	360			See [4] [6]
	26 – nHD portrait	360	640	270[3]	360	480	360	See [4]
	27 – nHD landscape	640	360	640	360			
	28 – Reserved							
	29 – nHD landscape input or VGA output	640	360	480[7]	360			See [8]
	30 to 35 – Reserved							
	Others – Reserved							

(6) BT.656 source port only; interlaced
(7) The displayed image does not fill the entire DMD
(8) Horizontal display resolutions less than 640 are centered with black borders

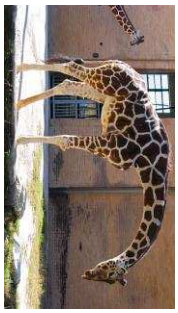
2.4.1.7 *Image Rotation Control: (I^2C: 0x0E, Flash :0x0000000E)*

When this command is received by the projector, the data defines whether the input image is to be rotated by 90° or not on the DMD. This command is used when the portrait image is to be displayed as landscape. It is not applicable for landscape source images.

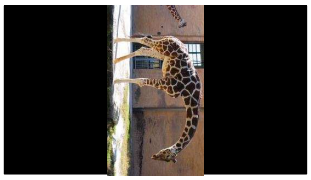
Bits	Description	Reset	Type
0	Image rotation (only used if input is portrait, should be set to 0 if input is landscape) 0 – No rotation (center image on DMD and pad with black bars) 1 – Portrait input image is scaled and rotated on DMD WVGA DMD: Applies –90° image rotation nHD DMD: Applies +90° image rotation	d0	wr

Note: If this parameter is changed when the input source is a still image, the input still image should be sent again. If the image is not sent again, the output image might be slightly corrupted. Note also that rotation direction can be reversed by also applying both long-side and short-side image flip.

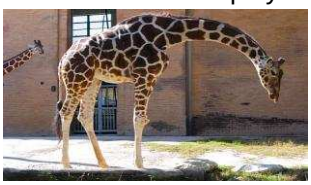
Portrait Source



Non-Rotated Display



-90° Rotated Display



2.4.1.8 Long-Side Image Flip: (I^2C: 0x0F, Flash: 0x0000000F)

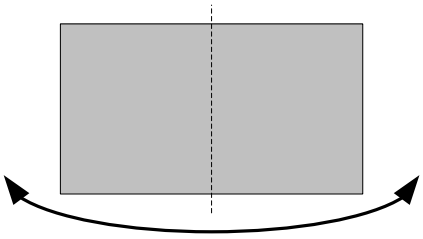
When this command is received by the projector, the data defines whether or not the input image is flipped about the axis that bisects the long side of the DMD.

Bits	Description	Reset	Type
0	Flips image along the long side of the DMD: 0 – Disable flip 1 – Enable flip	d0	wr

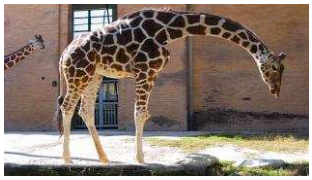
Note: If this parameter is changed when the input source is a still image, the input still image should be sent again. If the image is not sent again, the output image might be slightly corrupted.

Long-side flip means this:

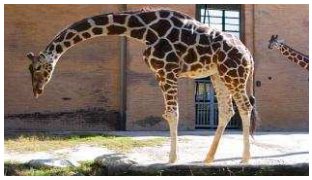
DMD



Flip Disabled



Flip Enabled



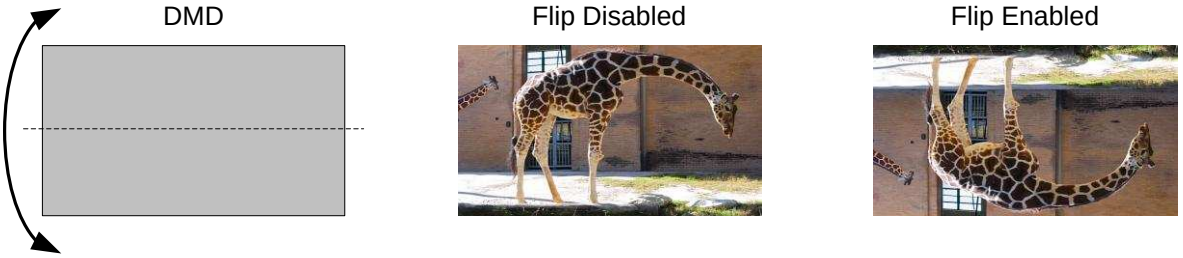
2.4.1.9 Short-Side Image Flip: (I^2C: 0x10, Flash: 0x00000010)

When this command is received by the projector, the data defines whether or not the input image is flipped about the axis that bisects the short side of the DMD.

Bits	Description	Reset	Type
0	Flips image along the short side of the DMD: 0 – Disable flip 1 – Enable flip	d0	wr

Note: If this parameter is changed when the input source is a still image, the input still image should be sent again. If the image is not sent again, the output image might be slightly corrupted.

Short-side flip means this:



2.4.1.10 Internal Test Patterns Select: (I^2C: 0x11, Flash: 0x00000011)

Table 5. (1)(2)

Bits	Description				Reset	Type
3:0	Internal test pattern select:				xD	wr
		Required Source Resolution				
	Options	**WVGA DMD**	**VGA DMD**(3)	**nHD DMD**		
	0x0 – Fine Checkerboard (WVGA DMD - 14 × 8 checkerboard) (VGA DMD – 14 × 8 checkerboard) (nHD DMD – 16 × 9 checkerboard)	854 × 480	854 × 480	640 × 360		
	0x1 – Solid black	854 × 480	854 × 480	640 × 360		
	0x2 – Solid white	854 × 480	854 × 480	640 × 360		
	0x3 – Solid green	854 × 480	854 × 480	640 × 360		
	0x4 – Solid blue	854 × 480	854 × 480	640 × 360		
	0x5 – Solid red	854 × 480	854 × 480	640 × 360		
	0x6 – Vertical lines (1 white, 7 black)	854 × 480	854 × 480	640 × 360		
	0x7 – Horizontal lines (1 white, 7 black)	854 × 480	854 × 480	640 × 360		
	0x8 – Vertical lines (1 white, 1 black)	854 × 480	854 × 480	640 × 360		
	0x9 – Horizontal lines (1 white, 1 black)	854 × 480	854 × 480	640 × 360		
	0xA – Diagonal lines	854 × 480	854 × 480	640 × 360		
	0xB – Vertical gray ramps	854 × 480	854 × 480	640 × 360		
	0xC – Horizontal gray ramps	854 × 480	854 × 480	640 × 360		
	0xD – ANSI 4 × 4 checkerboard	852 × 480	852 × 480	640 × 360		

(1) These test patterns are internally generated and injected into the beginning of the DLPC2607 image processing path. Therefore, all image processing is performed on the test images. All command registers should be set up as if the test images are input from an RGB 8:8:8 external source and the input resolution should be set to the value listed in this table for the corresponding DMD. No other input resolutions are supported.

(2) For a typical WVGA DMD test pattern usage, use the following command settings:
Input source and interface mode: (I^2C: 0x0B, flash: 0x0000000B
- 0x1 – Internal test patterns

Input resolution: (I^2C: 0x0C, flash: 0x0000000C)
- 0x19 – WVGA landscape (854h*480v)

Pixel format: (I^2C: 0x0D, flash: 0x0000000D)
- 0x2 – RGB888

(3) WVGA patterns must be used as test patterns on the VGA DMD. Note that only the center 640 × 480 VGA region is displayed (which corresponds to the center 456 × 684 on the diamond array).

2.4.1.11 LED Driver Control

LED driver operation is a function of the LED_ENABLE input, individual red, green, and blue LED enable software control parameters, individual red, green and blue LED current software control parameters, and the WPC function. The recommended order for initializing LED drivers is to:

1. Assert the LED_ENABLE input HIGH.
2. Program the individual red, green, and blue LED driver currents.
3. Turn on the DLP® display sequence.
4. Simultaneously turn on the red, green, and blue LED enables.
5. Turn on WPC (as desired).

The LED current software control parameters define PWM values that drive corresponding LED current. The WPC function, when enabled, continually monitors LED intensity, via an external senor, and automatically adjusts these PWM values to maintain a constant white point. Due to LED manufacturing variations, TI recommends a pico projector manufacturing calibration step to set the initial WPC of each unit. When the WPC function is not enabled, the control bus accessible red, green, and blue LED driver current parameters, listed in Section 2.4.1.11.1, must be used to set the drive for each LED.

2.4.1.11.1 RGB LED Driver Enable (I²C: 0x16, Flash: 0x00000016)

Bits	Description	Reset	Type
0	Enable Red LED: 0 – Disable red LED 1 – Enabled red LED	d0	wr
1	Enable Green LED: 0 – Disable green LED 1 – Enable green LED	b0	wr
2	Enable Blue LED: 0 – Disable blue LED 1 – Enable blue LED	b0	wr

2.4.1.11.2 Red LED Driver Current (I²C: 0x12, Flash: 0x00000012)

This parameter defines a PWM duty cycle that controls the red LED current. The resolution is 11 bits and corresponds to a percentage of the LED current. The PWM value can be set from 0% to 100% in 1/1024 steps. The max PWM value of 0x400 gives the minimum current setting.

Bits	Description	Reset	Type
10:0	Red LED Current PWM Value(1) Valid range is 0x000 (0% duty cycle → LEDs are 100% on) to 0x400 (100% duty cycle → LEDs are 0% on) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus *varies by OEM*. The equation for LED driver defined in the TI reference design schematics is: **I(LED_TI_REF) in ma = 1.04 × (1024 – PWM) + 20** Where “PWM” in the equation is the decimal equivalent of this register	d1023	wr

(1) The LED current PWM registers are not applicable when the WPC function is enabled.

2.4.1.11.3 Green LED Driver Current (I²C: 0x13, Flash: 0x00000013)

This parameter defines a PWM duty cycle that controls the green LED current. The resolution is 11 bits and corresponds to a percentage of the LED current. The PWM value can be set from 0% to 100% in 1/1024 steps. The max PWM value of 0x400 gives the minimum current setting.

Bits	Description	Reset	Type
10:0	Green LED Current PWM Value(1) Valid range is 0x000 (0% duty cycle → LEDs are 100% ON) to 0x400 (100% duty cycle → LEDs are 0% ON) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus *varies by OEM*. The equation for LED driver defined in the TI reference design schematics is: **I(LED_TI_REF) in ma = 1.04 × (1024 – PWM) + 20** Where “PWM” in the equation is the decimal equivalent of this register	d1023	wr

(1) The LED current PWM registers are not applicable when the WPC function is enabled.

2.4.1.11.4 Blue LED Driver Current (I^2C: 0x14, Flash: 0x00000014)

This parameter defines a PWM duty cycle that controls the blue LED current. The resolution is 11 bits and corresponds to a percentage of the LED current. The PWM value can be set from 0% to 100% in 1/1024 steps. The max PWM value of 0x400 gives the minimum current setting.

Bits	Description	Reset	Type
10:0	Blue LED Current PWM Value(1) Valid range is 0x000 (0% duty cycle → LEDs are 100% ON) to 0x400 (100% duty cycle → LEDs are 0% ON) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus *varies by OEM*. The equation for LED driver defined in the TI reference design schematics is: **I(LED_TI_REF) in ma = 1.04 × (1024 – PWM) + 20** Where “PWM” in the equation is the decimal equivalent of this register	d1023	wr

(1) The LED current PWM registers are not applicable when the WPC function is enabled.

2.4.1.11.5 WPC Golden Ratio (I^2C: 0xB4, Flash :0x000000B4)

This parameter defines the golden color ratios that WPC uses for typical operation. These values are typically determined as part of factory calibration and programmed by the host upon initialization.

Bits	Description	Reset	Type
10:0	Green or Blue WPC Golden Ratio Valid range is 0x000 to 0x7FF Given an LSB decimal weight of 0.005, the decimal range is 0 to 10.24	x000	wr
15:11	Spare		
26:16	Green or Red WPC Golden Ratio Valid range is 0x000 to 0x7FF Given an LSB decimal weight of 0.005, the decimal range is 0 to 10.24	x000	wr

2.4.1.11.6 WPC Control (I^2C: 0xB5, Flash :0x000000B5)

This register contains several WPC configuration control parameters as described in the following:

Bits	Description		Reset	Type
0	WPC Function Enable 0 = WPC disabled 1 = WPC enabled		b0	wr
1	WPC (Wcor) Enable 0 = Wcor disabled 1 = Wcor enabled	or WPC Processing Enable or 0 = WPC processing disabled or 1 = WPC processing enabled	b0	wr
2	LED Power Correction (Pcor) Enable 0 = Pcor disabled 1 = Pcor enabled	or WPC Processing Enable or 0 = Power correction processing disabled or 1 = Power correction processing enabled	b0	wr
3	Wcor Fast Convergence Mode Enable 0 = Wcor slow convergence mode 1 = Wcor fast convergence mode	or WFAST Enable or 0 = WFAST disabled or 1 = WFAST enabled	b0	wr
4	Pcor Fast Convergence Mode Enable 0 = Wcor slow convergence mode 1 = Wcor fast convergence mode	or PFAST Enable or 0 = PFAST disabled or 1 = PFAST enabled	b0	wr

2.4.1.12 Parallel Bus Specific Commands

The following commands are unique to operating the parallel bus interface.

2.4.1.12.1 Parallel Bus Polarity Control (I^2C: 0XAF, Flash: 0x000000AF)

These parameters apply only to parallel bus operation and must be configured to match the attributes of the source feeding the DLPC2607.

Bits	Description	Reset	Type
0	Reserved Must be set = 0	b0	wr
1	Defines the polarity of the incoming HSYNC signal: 0 – Active low pulse 1 – Active high pulse	b0	wr
2	Defines the polarity of the incoming VSYNC signal: 0 – Active low pulse 1 – Active high pulse	b0	wr
3	Pixel Clock Polarity 0 – Data sample on rising edge 1 – Data sample on falling edge	b0	wr
4	DATEN Polarity 0 – Active low 1 – Active high	b1	wr

2.4.1.12.2 Parallel Bus Data Mask Polarity (I^2C: 0XB2, Flash: 0x000000B2)

Bits	Description	Reset	Type
0	Parallel Bus Data Mask (PDM) Polarity Select 0 = PDM is active low (that is PDATA and DATEN are masked and ignored when PDM = 0) 1 = PDM is active high (that is PDATA and DATEN are masked and ignored when PDM = 1)	x1	wr

2.4.1.12.3 Parallel Bus Data Mask Enable (I^2C: 0XB3, Flash: 0x000000B3)

Bits	Description	Reset	Type
0	Parallel Bus Data Mask (PDM) Enable 0 = PDM is disabled 1 = PDM is enabled	X0	wr

2.4.1.12.4 Vertical Sync Line Delay (I^2C: 0x23, Flash: 0x00000023)

When this command is received by the projector, an adjustable delay on VSYNC can be added internal to the DLPC2607. This delay is sometimes needed if the vertical front porch is too short. This VSYNC delay command is only applicable to the parallel interface and BT.656 interface.

Bits	Description	Reset	Type
4:0	Vertical Sync Line Delay (VSLD) Range is 0 to 15 lines, and it should be set such that: 6 – VFP (min 0) ≤ VSLD ≤ VBP-2 (max 15) Where VFP = Vertical front porch (in lines) and VBP = Vertical back porch (in lines)	x05	wr

2.4.1.12.5 Auto Framing Function

Auto framing supports the automatic generation of a data valid (DATEN) signal for sources that do not provide a data valid. It requires vertical and horizontal back porch timing to be consistent from frame to frame (that is zero variation). Horizontal and vertical back porch framing parameters (register 0xB0-0xB1) should be defined before enabling the function (register 0xAE). This feature should not be used for still image operation if HSYNCs and VSYNCs continue to be sent in the absence of data (that is, otherwise auto framing would continue to frame the "data" even though there is not any). Note that for auto framing to be a valid option, video timing must be consistent from frame to frame such that vertical and horizontal back porch counts have zero variation.

2.4.1.12.5.1 Auto Framing Function Enable (I^2C: 0XAE, Flash: 0x000000AE)

Table 6. (1)

Bits	Description	Reset	Type
0	Auto Framing Function Enable 0 = Auto-generation of the DATEN signal is disabled 1 = Auto-generation of the DATEN signal is enabled (default = 0 disabled)	b0	wr

(1) Applies to parallel bus sources only

2.4.1.12.5.2 Auto Framing Horizontal Back Porch (I^2C: 0XB0, Flash: 0x000000B)

Table 7. (1)

Bits	Description	Reset	Type
11:0	Expected input horizontal back porch blanking. "One-based" value that defines the number of clocks between input HSYNC active edge and first clock of active data. Only applicable when “auto framing function enable” = 1.	x000	wr

(1) Applies to parallel bus sources only

2.4.1.12.5.3 Auto Framing Vertical Back Porch (I^2C: 0XB1, Flash: 0x000000B1)

Table 8. (1)

Bits	Description	Reset	Type
11:0	Expected input vertical back porch blanking. "One-based" (1 based value; 1 = 1) value that defines the index of the first non-blanking (active data) line. Applicable when auto framing function enable = 1 (to feed image framing) or BT.656 source is selected.	x000	wr

(1) Applies to BT656 or parallel bus sources only

2.4.1.12.6 Custom Framing Commands

Custom framing is applicable to parallel bus applications only. It provides the option to define a subset of active frame data using pixel and line counts relative to the source data enable signal (DATEN). This feature allows the source image to be cropped as the first step in the processing chain.

2.4.1.12.6.1 First Active Line in the Frame (I^2C: 0x29, Flash: 0x00000029)

Bits	Description	Reset	Type
10:0	First Active Line In Frame (Relative to Active lines) Image Crop Control 0 based (0 = first line, 1= second line, and so forth), default = 0 (no left cropping)	x000	wr

2.4.1.12.6.2 Last Active Line in the Frame (I²C: 0x2A, Flash: 0x0000002A)

Table 9. (1)

Bits	Description	Reset	Type
10:0	Last Active Line In Frame (Relative to Active lines) Image Crop Control 1 based (N = N except 0 = line 1024), Default = 0 (no right cropping)	x000	wr

(1) Last active line in frame (VCROP_LALIF) is relative to the un-cropped source (that is first active line in frame does not affect this parameter).

2.4.1.12.6.3 First Active Pixel in the Line (I²C: 0x2B, Flash: 0x0000002B)

Bits	Description	Reset	Type
10:0	First Active Pixel In Line (Relative to Active Pixels) Image Crop Control 0 based (0 = first line, 1 = second line, etc), Default = 0 (no top cropping)	x000	wr

2.4.1.12.6.4 Last Active Pixel in the Line (I²C: 0x2C, Flash: 0x0000002C)

Table 10. (1)

Bits	Description	Reset	Type
10:0	Last Active Pixel In Line (Relative to Active Pixels) Image Crop Control 1 based (N = N except 0 = line 1024), Default = 0 (no bottom cropping)	x000	wr

(1) Last active pixel in line (relative to active pixels) is relative to the un-cropped source (that is, the first active pixel in line does not affect this parameter).

2.4.1.13 Display Frame Rate Control

The display frame rate must always be periodic. It is driven by the frame rate attribute of the selected DLP® display sequence. For the best motion video performance, the display frame rate and the DLP® display sequence, should be chosen to match an integer multiple of the source frame rate and the sequence sync mode parameter (0x1E) should be set to “lock-to-VSYNC” mode. This is most useful for BT.656 and parallel bus applications as these sources are assumed to always possess a periodic source frame rate.

When the source frame rate is aperiodic, the display frame rate cannot be synchronized to source, and thus the sequence sync mode parameter (0x1E) should be set to free-run mode. Free-run mode can also be used for periodic sources, but the lack of synchronization may result in visible motion judder. Note that the DLP® display sequence must always be greater than or equal to the display frame rate or additional artifacts result. Free-run mode should be used for splash and test pattern generation applications.

2.4.1.13.1 Video Frame Rate Control (I²C: 0x19, Flash: 0x00000019)

The video frame rate parameter defines the periodic frame rate of the source. BT.656 and parallel bus applications are assumed to always possess a periodic source frame rate. Splash and test pattern generation applications should be assumed to always possess a non-periodic source frame rate.

Table 11. (1)

Bits	Description	Reset	Type
11:0	Defines the free-run sequence rate. Range is 30 to 72 Hz (default = x0859, 60 Hz) Value (decimal) = (1000000 / Freq(Hz)) / 7.8 Example; F = 60 Hz, Value = (1000000 / 60) / 7.8 = 2137 (decimal) = x0859 (hex)	x000	wr

(1) The video frame rate parameter is automatically set when the compound I²C command to change sequences is applied. Manual configuration of this register is only needed for free run, when the sequence selection compound I²C command is not used.

2.4.1.14 DLP® Display Sequence Control

DLP® display sequence control consists of several parameters which dictate the operation of the uploaded DLP® PWM sequence.

2.4.1.14.1 Sequence Vector Set-up: (I^2C: 0x83, Flash: 0x00000083)

Bits	Description	Reset	Type
7:0	Sequence Vector Select Selects the desired sequence to run from on-chip memory. Given only one sequence is loaded into local sequence memory from flash, the value should be set to 0 to select the first sequence (reset value = 0).	x00	wr
15:8	Number of Sequence Sub-Vectors 0 = A value of 0 is illegal 1 = 1× 2 = 2× 3 = 3× And so forth	x02	wr
	The “number of SEQ sub-vectors” parameter defines how many times the sequence is to be repeated for each input VSYNC. This allows the display frame rate to be an integer multiple of the source frame rate and thus minimize artifacts associated with low frame rates.		

2.4.1.14.2 Sequence Sync Mode (I^2C: 0x1E, Flash: 0x0000001E)

The sequence sync mode defines whether or not the DLP® display frame rate needs to be independent of the source frame or synchronized with the source frame rate.

When the source frame rate is non-periodic, such as when a still image updates in response to a user’s control, the DLP® display frame rate needs to be independent from the source such that the display can be refreshed at a regular rate. To do this, the sequence sync mode must be set to free-run mode. In this mode, the DLP® display frame rate is defined directly by the frame rate attribute of the selected DLP® display sequence.

When the source frame rate is periodic, such as from a motion video or graphics source, the DLP® display frame rate needs to be synchronized to the source such that motion artifacts are minimized. To do this, the sequence sync mode must be set to lock-to-VSYNC mode where VSYNC is the applicable vertical sync signal. For BT.656 applications, the VSYNC signal is encoded into the data stream. For parallel bus applications, the VSYNC input pin drives source synchronization.

The DLPC2607 provides the ability to synchronize the DLP® display frame rate to an integer multiple of the source frame rate over a range of 1× to 12×. A multiple that is greater than one provides the option to increase the display frame rate when the source frame rate is slow and would result in an undesirably low display refresh rate. As in all modes, the DLP® display frame rate is defined by the frame rate attribute of the selected DLP® display sequence; however, the source frame rate is assumed to be DLP® display frame rate divided by N (where N is a programmable integer multiplier).

Bits	Description	Reset	Type
0	Sequence Sync Mode 0 – Free-run (the display is asynchronous with respect to the source) 1 – Lock-to-VSYNC (the display is synchronous with the source)	d0	wr

The *only* valid image inputs for using “lock-to-VSYNC” mode are:

1. Parallel I/F input frames that are periodic and equal to the available DLP® sequence frame rates
2. NTSC inputs from the TVP5151 video decoder (periodic at 60 Hz)
3. PAL or SECAM inputs from the TVP5151 video decoder (periodic at 50 Hz)

“Free-run” mode must be selected in these cases:

1. Parallel I/F for frame rates that are < 5 Hz or non-sub-multiples of the available DLP® display sequence frame rates
2. Parallel I/F for frame rates that are not periodic

3. Splash screens
4. Internal test patterns (this allows it to work with any DLP® display sequence)

2.4.1.15 Image Processing Parameter Definitions

2.4.1.15.1 Temporal Dither Control: (I^2C: 0x7E, Flash: 0x0000007E)

When this command is received by the projector, temporal dithering is turned on or off. Temporal dither should be disabled for any non-periodic source or any periodic source with a frame rate slower than 50 Hz. Otherwise, temporal dither should be enabled to improve image quality.

Table 12. (1)

Bits	Description	Reset	Type
1:0	Temporal Dither Control 0 – Enable temporal dithering 1 – Reserved 2 – Disable temporal dithering 3 – Reserved	b10	wr

(1) A special CMT table is required in order to disable spatial dithering. This parameter only controls temporal dithering.

2.4.1.15.2 Automatic Gain Control Function

The auto gain control function helps to maintain maximum perceived display brightness. The following parameters control AGC operation. These parameters are source frame rate dependent and must be updated accordingly.

2.4.1.15.2.1 Auto Gain Control Function Enable (I^2C: 0x50, Flash: 0x00000050)

Auto gain control is intended for use with motion video sources.

Bits	Description	Reset	Type
2:0	AGC Function Enable 0 to 5 – Reserved 6 – AGC disabled 7 – AGC enabled	b110	wr

2.4.1.15.2.2 AGC Step Size Increment (I^2C: 0x52, Flash: 0x00000052)

Bits	Description	Reset	Type
11:0	Step size for gain increase for brightness decreases Recommended value = 60 / source frame rate Default: b1 (60 Hz recommended value)	d1	wr

2.4.1.15.2.3 AGC Step Size Decrement (I^2C: 0x53, Flash: 0x00000053)

Bits	Description	Reset	Type
2:0	Step size for gain decrease for brightness decreases Recommended value = 60 / source frame rate Default: d1 (60 Hz recommended value)	d1	wr

2.4.1.15.2.4 AGC Leap Size Decrement (I²C: 0x54, Flash: 0x00000054)

Bits	Description	Reset	Type
11:0	Largest gain decrement amount for drastic brightness increases Recommended value = 20 + (1200 / source frame rate) Default: d40 (60 Hz recommended value)	d40	wr

2.4.1.15.3 Color Coordinate Adjustment (CCA) Function

When enabled, the color coordinate adjustment (CCA) function modifies the color coordinates of the incoming image. This allows the color coordinates and color gain to be adjusted for R, G, B, and W (Y, C, and M) are not programmable. Default coefficients due to a hardware power-up reset, and when the CCA function is disabled, are a unity matrix.

NOTE: The format for all coefficients is u1.8 for all coefficients.

2.4.1.15.3.1 CCA Function Enable (I²C: 0x5E, Flash :0x0000005E)

Bits	Description	Reset	Type
0	CCA Function Enable 0 - CCA disabled 1 - CCA enabled	d1	wr

2.4.1.15.3.2 CCA C1R1 Coefficient (I²C: 0x5F, Flash :0x0000005F)

Bits	Description	Reset	Type
8:0	Column 1 row 1 coefficient (red)	x100	wr

2.4.1.15.3.3 CCA C1R2 Coefficient (I²C: 0x60, Flash :0x00000060)

Bits	Description	Reset	Type
8:0	Column 1 row 2 coefficient (red)	x000	wr

2.4.1.15.3.4 CCA C1R3 Coefficient (I²C: 0x61, Flash :0x00000061)

Bits	Description	Reset	Type
8:0	Column 1 row 3 coefficient (red)	x000	wr

2.4.1.15.3.5 CCA C2R1 Coefficient (I²C: 0x62, Flash :0x00000062)

Bits	Description	Reset	Type
8:0	Column 2 row 1 coefficient (green)	x000	wr

2.4.1.15.3.6 CCA C2R2 Coefficient (I²C: 0x63, Flash :0x00000063)

Bits	Description	Reset	Type
8:0	Column 2 row 2 coefficient (green)	x100	wr

2.4.1.15.3.7 CCA C2R3 Coefficient (I^2C: 0x64, Flash :0x00000064)

Bits	Description	Reset	Type
8:0	Column 2 row 3 coefficient (green)	x000	wr

2.4.1.15.3.8 CCA C3R1 Coefficient (I^2C: 0x65, Flash :0x00000065)

Bits	Description	Reset	Type
8:0	Column 3 row 1 coefficient (blue)	x000	wr

2.4.1.15.3.9 CCA C3R2 Coefficient (I^2C: 0x66, Flash :0x00000066)

Bits	Description	Reset	Type
8:0	Column 3 row 2 coefficient (blue)	x000	wr

2.4.1.15.3.10 CCA C3R3 Coefficient (I^2C: 0x67, Flash :0x00000067)

Bits	Description	Reset	Type
8:0	Column 3 row 3 coefficient (blue)	x100	wr

2.4.1.15.3.11 CCA C4R1 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 4 row 1 coefficient (yellow)	x000	wr

2.4.1.15.3.12 CCA C4R2 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 4 row 2 coefficient (yellow)	x100	wr

2.4.1.15.3.13 CCA C4R3 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 4 row 3 coefficient (yellow)	x100	wr

2.4.1.15.3.14 CCA C5R1 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 5 row 1 coefficient (cyan)	x100	wr

2.4.1.15.3.15 CCA C5R2 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 5 row 2 coefficient (cyan)	x000	wr

2.4.1.15.3.16 CCA C5R3 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 5 row 3 coefficient (cyan)	x100	wr

2.4.1.15.3.17 CCA C6R1 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 6 row 1 coefficient (magenta)	x100	wr

2.4.1.15.3.18 CCA C6R2 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 6 row 2 coefficient (magenta)	x100	wr

2.4.1.15.3.19 CCA C6R3 Coefficient (Hard Coded – Not Programmable)

Bits	Description	Reset	Type
8:0	Column 6 row 3 coefficient (magenta)	x000	wr

2.4.1.15.3.20 CCA C7R1 Coefficient (I^2C: 0x71, Flash :0x00000071)

Bits	Description	Reset	Type
8:0	Column 7 row 1 coefficient (white)	x100	wr

2.4.1.15.3.21 CCA C7R2 Coefficient (I^2C: 0x72, Flash :0x00000072)

Bits	Description	Reset	Type
8:0	Column 7 row 2 coefficient (white)	x100	wr

2.4.1.15.3.22 CCA C7R3 Coefficient (I^2C: 0x73, Flash :0x00000073)

Bits	Description	Reset	Type
8:0	Column 7 row 3 coefficient (white)	x100	wr

2.4.1.16 Memory Control Parameter Definitions

2.4.1.16.1 Display Buffer Swap Freeze (I^2C: 0xA3, Flash: 0x000000A3)

Bits	Description	Reset	Type
0	Display Buffer Swap Freeze (also called Memory Buffer Swap Disable) 0 = Enable buffer swapping (default) 1 = Disable buffer swapping (freeze) TI recommends to use freeze when changing source or operating modes to block temporary corruption caused by reconfiguration from reaching the display. When frozen, the last display image continues to be displayed.	b0	wr

2.4.1.16.2 mDDR Memory BIST Status Register (I^2C: 0x9B)

This register provides mDDR memory built-in-self-test (BIST) status information.

Bits	Description	Reset	Type
0	Memory Controller BIST ERROR 1 = An error has been detected during mDDR memory BIST execution 0 = No BIST errors have been detected	b0	r
1	Memory Controller BIST DONE 0 = BIST is in progress (if enabled) 1 = BIST is complete	b0	r

2.4.1.17 DMD Interface Parameter Definitions

2.4.1.17.1 Display Curtain Control (I^2C: 0xA6, Flash: 0x000000A6)

This register provides image curtain control. When enabled, the image curtain displays a solid field on the entire DMD display regardless of other ASIC source configurations. However, it does require that the sequence is running. This provides an alternate method of masking temporary source corruption, caused by reconfiguration, from reaching the display. It is also useful for an optical test and debug support.

Bits	Description	Reset	Type
3:0	Display Curtain Enable (all undefined values are reserved) x0 = Curtain disabled x1 = Curtain enabled	x0	wr
7:4	Display Curtain Color Select (all undefined values are reserved) X0 = Black x3 = Yellow (Red + Green) x1 = Red x5 = Magenta (Red + Blue) x2 = Green x6 = Cyan (Green + Blue) x4 = Blue x7 = White	x0	wr

2.4.1.17.2 DMD Bus Swap Control (I^2C: 0xA7, Flash: 0x000000A7)

DMD bus swap control provides the ODM to reverse the bit-ordering of the DMD data bits output by the DLPC2607 to potentially facilitate simpler PCB routing.

Bits	Description	Reset	Type
0	DMD Bus Swap Control 0 = Swap disabled 1 = Swap enabled (output DMD data bus bit-order is reversed)	b0	wr

2.4.1.17.3 DMD PARK (I^2C: 0x2D, Flash: 0x0000002D)

The DMD PARK command provides a software programmable alternative to using the PWRGOOD signal. If PWRGOOD is tied high, the DMD PARK command can be used to warn the DLPC2607 is impending DMD power loss such that it can PARK the DMD mirrors and avoid reliability degradation.

Table 13. (1)

Bits	Description	Reset	Type
0	DMD Park Control 0 = Unpark the DMD (default) 1 = Park the DMD	b0	wr

(1) This park operation does not de-assert the DMD_PWR_EN output thus DMD power remains on.

2.4.1.18 Serial FLASH Control

2.4.1.18.1 FLASH Controller Mode of Operation (I^2C: 0x08, Flash :0x00000008)

This register defines the desired flash memory controller (FMC) mode of operation. A transition from “000” to any other valid mode initiates the corresponding FMC operation. A transition from any valid mode to “000” aborts and terminates any active FMC operation.

Table 14. (1) (2)

Bits	Description	Reset	Type
2:0	Flash Memory Controller Mode of Operation (2:0): 000 – Idle mode (all FMC operations are disabled) 001 – Flash to (CMIS) mailbox DMA operation 010 – Flash to configuration register DMA operation 011 – Flash read data operation 100 – Flash write data operation 101 – Flash command operation 110 and 111 – Reserved	0	wr

(1) The flash memory controller starts its direct memory access (DMA) data transfer operation when it detects a change in this register from “000” to “001” to “010”.

(2) No other flash memory controller operation can be requested during a DMA transaction or the active DMA is aborted.

2.4.1.18.2 FLASH READ Register (I^2C 0x07; Not Accessible via Flash)

Bits	Description	Reset	Type
31:0	This register is used to read the contents of the flash 32 bits at a time after the flash has been set up to do the READ-FLASH operation	b0	wr

2.4.1.18.3 Flash DMA Read Stall Register (Flash: 0x00000009, Not Accessible via I^2C Interface)

Bits	Description	Reset	Type
0	This register is used when the flash memory controller mode of operation register (refer to Section 2.4.1.18.1) is set up to perform a “flash to configuration register DMA” operation. When the flash controller encounters a value of 1 in this register it stops further DMA reads until the mDDR memory controller has issued a buffer swap signal. 0 = “Flash to configuration register DMA” operation continues as normal 1 = “Flash to configuration register DMA” operation is stopped until the mDDR memory controller issues a buffer swap. The value is cleared upon the buffer swap operation.	0	wr

2.4.1.18.4 Flash ADDR BYTES (I^2C: 0x74, Flash: 0x00000074)

Table 15. (1)

Bits	Description	Reset	Type
2:0	ADDR_BYTE_QTY – Number of address bytes to be issued during a flash operation. 000 = 0 address bytes 001 = 1 address byte (that is UCA_ADDRESS(8:0)*) 010 = 2 address bytes (that is UCA_ADDRESS(15:0)) 011 = 3 address bytes (that is UCA_ADDRESS(23:0)) (Default) 1xx = 4 address bytes (that is UCA_ADDRESS(31:0))	x3	wr

(1) Refer to the data sheet for the external flash device used to program this register. All typical flash use the default setting.

2.4.1.18.5 Flash Dummy Bytes (I²C: 0x75, Flash: 0x00000075)

Table 16. (1)

Bits	Description	Reset	Type
5:0	**DUMMY_BYTE_QTY** – Number of don't care (dummy) bytes to be issued (following address bytes) during a flash command access. 0 = 0 dummy bytes 1 = 1 dummy byte 2 = 2 dummy bytes … 63 = 63 dummy bytes	x1	wr

(1) Refer to the data sheet for the external flash device used to program this register.

2.4.1.18.6 Flash WDATA BYTES (I²C: 0x76, Flash: 0x00000076)

Table 17. (1)

Bits	Description	Reset	Type
24:0	WDATA_BYTE_QTY – Number of write data bytes that is transmitted to serial memory during flash command write access. 0x0000000 = 0 write data bytes 0x0000001 = 1 write data byte 0x0000002 = 2 write data bytes … 0x0FFFFFF = (16M – 1) write data bytes 0x1000000 – 0x1FFFFFF = 16M write data bytes	x0	wr

(1) Refer to the data sheet for the external flash device used to program this register.

2.4.1.18.7 Flash RDATA BYTES (I²C: 0x77, Flash: 0x00000077)

Table 18. (1)

Bits	Description	Reset	Type
24:0	RDATA_BYTE_QTY – Number of read data bytes that are to be received from serial memory during a read flash access. 0x0000000 = 0 read data bytes 0x0000001 = 1 read data byte 0x0000002 = 2 read data bytes … 0x0FFFFFF = (16M – 1) read data bytes 0x1000000 – 0x1FFFFFF = 16M read data bytes	x0	wr

(1) Refer to the data sheet for the external flash device used to program this register.

2.4.1.18.8 Flash OPCODE (I²C: 0x78, Flash: 0x00000078)

Table 19. (1)

Bits	Description	Reset	Type
7:0	OPCODE – Instruction opcode value to be issued during a flash access	x0	wr

(1) Refer to the data sheet for the external flash device used to program this register

2.4.1.18.9 Flash Address (I²C: 0x79, Flash: 0x00000079)

Table 20. (1)

Bits	Description	Reset	Type
31:0	ADDRESS(31:0) – Address value to be issued during a flash operation. The number of valid addresses bit is a function of the flash device. For example, only 24-bit address bits per chip select are used to support the 16 MB (128 Mb) target device size.	x0	wr

(1) ADDR_BYTE_QTY must be adjusted according to how many address bytes are expected by the flash device. Refer to the flash memory map recommended in Appendix C.

2.4.1.18.10 Flash Write DATA (I²C: 0x7B, Flash: 0x0000007B)

Bits	Description	Reset	Type
31:0	Flash Write DATA – Data written to this register are written into the flash	x0	wr

2.4.1.18.11 Flash Write Byte Enable (I²C: 0x7C, Flash: 0x0000007C)

Table 21. (1)

Bits	Description	Reset	Type
3:0	TXDATA_BYTE = Transmit data byte indicates the number of bytes written to the flash 0xF – Indicates 4 bytes to be written 0x7 – Indicates 3 bytes to be written 0x3 – Indicates 2 bytes to be written 0x1 – Indicates 1 bytes to be written	0xF	wr

(1) Refer to the data sheet for the external flash device used to program this register.

2.4.1.19 SCL, CMT, BNM, and Splash Screen LUT Control

To access SCL, CMT, BNM, and splash screen LUTs, configure the start address of the LUT, set up the auto-increment feature, and select the LUT to be accessed. Then, the LUT is programmed by writing to data register.

2.4.1.19.1 SCL, CMT, BNM, and Splash Start Sub-Address (I²C: 0XFA, Flash: 0x000000FA)

Bits	Description	Reset	Type
10:0	Start address of the selected SCL, CMT, BNM, and splash memory to be accessed (typically set to 0)	x000	wr

2.4.1.19.2 SCL, CMT, BNM, and Splash Memory Configuration Select (I²C: 0XFB, Flash: 0x000000FB)

Bits	Description	Reset	Type
3:0	This register is used to select the specific LUT to be programmed. (See Table 22 for selection options.)	x0	wr

Table 22.

Selection Value	Depth	Width	Delay	Function and Target Memory Description
x0	N/A	N/A	N/A	Disable all memory access(1)
x1	128	32	short	CMT green LUT(2)
x2	128	32	short	CMT red LUT(2)

(1) All memory accesses must be disabled (this register set to 0) before an image can be properly displayed
(2) SCL, Splash, BNM, and CMT tables are *not* accessible when I/F SLEEP mode is enabled.

Table 22. (continued)

Selection Value	Depth	Width	Delay	Function and Target Memory Description
x3	128	32	short	CMT LUT blue[2]
x4	384	32	short	CMT all LUTs[2][3]
x5	2048	32	short	Splash LUT [2][4]
x6	256	32	short	BNM threshold LUT[2]
x7	80	32	short	SCL horizontal sharpness coefficient LUT[2]
x8	48	32	short	SCL vertical sharpness coefficient LUT[2]

(3) Writing a value of 4 to this register supports programming all three CMT LUTs in a single file transfer, with LUT data written consecutively in the GRB order.

(4) To download a splash image from flash or I^2C, this register must be set to a value of 5. This must be done each time a splash image is needed.

2.4.1.19.3 SCL, CMT, BNM, and Splash Data Access Register (I^2C: 0XFC, Flash: 0x000000FC)

Bits	Description	Reset	Type
31:0	Data written to this register is programmed into the selected LUT. The format to be written is shown in the following tables.	X0000 0000	wr

CMT LUT Data

Bit 31 Bit 16 Bit 15 Bit 0

CMT Word 1(15:0)		CMT Word 0(15:0)	
Byte 3	Byte 2	Byte 1	Byte 0

Splash Data

Bit 31 Bit 16 Bit 15 Bit 0

Splash Pixel 2(15:0)		Splash Pixel 1(15:0)	
G1(5:0):R1(4:0):B1(4:0)		G0(5:0):R0(4:0):B0(4:0)	
Byte 3	Byte 2	Byte 1	Byte 0

Note: If the splash pixels per line is not an even number; then the last word for every splash line should be zero padded to fill the entire 32-bits.

BNM LUT Data

Bit 31 Bit 0

SCL LUT Data (31:0)			
BNM Coefficient 4(7:0)	**BNM Coefficient 3(7:0)**	**BNM Coefficient 2(7:0)**	**BNM Coefficient 1(7:0)**
Byte 3	Byte 2	Byte 1	Byte 0

SCL LUT Data

Bit 31 Bit 0

SCL LUT Data (31:0)			
SCL Coefficient 4(7:0)	**SCL Coefficient 3(7:0)**	**SCL Coefficient 2(7:0)**	**SCL Coefficient 1(7:0)**
Byte 3	Byte 2	Byte 1	Byte 0

2.4.1.20 WPC, DLP® Display Sequence and DMD Reset LUT Control

To access the WPC, DLP® display sequence (SEQ), and DMD reset control (DRC) LUTs, the user must configure the start address of the LUT, set up the auto-increment feature, and select the LUT to be accessed. Then, the LUT is programmed by writing to the DATA register.

2.4.1.20.1 WPC, SEQ, and DRC Start Sub-Address (I^2C: 0XFD, Flash: 0x000000FD)

Bits	Description	Reset	Type
10:0	Start address of the selected WPC, SEQ, or DRC memory to be accessed (typically set to 0)	X000	wr

2.4.1.20.2 WPC, SEQ, and DRC Memory Configuration Select (I^2C: 0XFE, Flash: 0x000000FE)

Bits	Description	Reset	Type
3:0	This register is used to select the specific LUT to be programmed. (See the following table for selection options.)	X0	wr

Selection Value	Depth	Width	Delay	Function / Target Memory Description
x0	N/A	N/A	N/A	Disable all memory access(1)
x1	64	32	short	DMD reset control LUT 0
x2	64	32	short	DMD reset control LUT 1
x3	64	32	short	DMD reset control LUT 2
x4	64	32	short	DMD reset control LUT 3
x5	2048	32	short	SEQ memory
x6	64	32	short	DMD reset control LUT all(2)
x7	2048	32	short	WPC LUT

(1) All memory accesses must be disabled (this register set to 0) before an image can be properly displayed.
(2) Writing a value of 6 to this register programs all the DRC (DMD reset control) LUT with the same data (written to register FC).

2.4.1.20.3 WPC, SEQ, and DRC LUT Data Access Register (I^2C: 0XFF, Flash: 0x000000FF)

Bits	Description	S/P	Type
31:0	Data written to this register is programmed into the selected LUT. The format to be written is shown in the following.	P	wr

DMD Reset Control (DRC) LUT Data

Bit 31 Bit 16 Bit 15 Bit 0

Unused		DRC LUT Word 1(12:0)	
X"0000"		b"000" DRC_Data0(12:0)	
Byte 3	Byte 2	Byte 1	Byte 0

Sequence (SEQ) LUT Data

Bit 31 Bit 0

SEQ LUT Data 1(31:0)			
Byte 3	Byte 2	Byte 1	Byte 0

WPC LUT Data

Bit 31 Bit 0

WPC LUT Data (31:0)			
Byte 3	Byte 2	Byte 1	Byte 0

2.4.1.21 Initialization and Command Processor (ICP) Program Memory Control

To access the ICP program memory, the user must configure the start address of the LUT, set up the auto-increment feature, and select the memory to be accessed. Then, the LUT is programmed by writing to DATA register.

2.4.1.21.1 ICP Program Memory Start Sub-Address (I^2C 0XF7, Flash: 0x000000F7)

Bits	Description	Reset	Type
10:0	Start address of the memory to be accessed (typically set to 0)	X000	wr

2.4.1.21.2 ICP Program Memory Configuration Select (I^2C: 0XF8, Flash: 0x000000F8)

Bits	Description	Reset	Type
3:0	This register is used to select the memory to be programmed (see the following table for selection options)	X0	wr

Selection Value	Depth	Width	Delay	Function or Target Memory Description
x0	N/A	N/A	N/A	Disable all memory access[(1)]
x1	2048	32	short	ICP Program memory

(1) All memory accesses must be disabled (this register set to 0) before an image can be properly displayed.

2.4.1.21.3 ICP Program Memory Data Access Register (I^2C: 0XF9, Flash: 0x000000F9)

Bits	Description	S/P	Type
31:0	Data written to this register is programmed into the selected LUT. The format to be written is shown in the following.	P	wr

ICP LUT Data

Bit 31 Bit 0

ICP LUT Data 1(31:0)			
Byte 3	Byte 2	Byte 1	Byte 0

2.4.1.22 Compound I^2C Command Processing

The ICP supports processing of a few 8-bit, compound I^2C commands. Compound I^2C commands are abstractions of several basic DLPC2607 operations including splash, sequence, and CMT table selection and WPC calibration. This means instead of having to know where in flash these tables reside, and then perform a flash DMA operation to individually upload them, the ICP does the process for the user. The supported compound I^2C commands are defined in Section 2.4.1.22.4.

To use a compound command, the ICP data register (I^2C: 0x39) and the ICP handshake register (I^2C: 0x3A) must first be written with the desired command parameter value and busy status prior to writing the corresponding command to the ICP command register (I^2C: 0x38). To avoid potential corruption, no other I^2C transactions, except to the ICP data and ICP handshake registers as described in the following, should be sent to the DLPC2607 until prior compound I^2C command processing is complete; because, these compound commands typically take much longer to complete. To determine when current compound I^2C command processing is complete the host must poll the “ICP command handshake” register and wait for the ICP command busy flag to be cleared.

Note that a flash erase command is considered complete by the ICP when the command is forwarded to the flash device. Unlike processing for all other commands, the ICP does *not* hold the ICP command busy flag and wait for all processing associated with the command (that is the flash erase) to complete. However, the host is still required to wait for the erase operation to complete before issuing any additional flash-related commands following a flash erase command. The host does this by successively issuing a flash status command until the ERASE COMPLETE bit is cleared to 0. (The ICP sets this flag when it receives the flash erase command). To help ensure the proper protocol is followed, the ICP verifies that the flash device is not busy performing an erase operation every time it receives a flash-related command. If the flash is busy with an erase operation when a new flash command is received, then the ICP ignores this incoming command and sets both the flash error flag in the system status word and the flash busy error flag in the flash status word.

2.4.1.22.1 ICP Command (Compound I²C Command) Register (I²C: 0x38, Flash : N/A)

The compound I²C command (also called ICP command) register accepts a set of commands processed by the ICP. These commands are 8-bit commands received via the I²C bus (only), which do more than simple register read and write operations. Most commands must also be accompanied by compound I²C command data (I²C register 0x39). For commands that require a compound I²C command-data value, this value must be written prior to writing the compound I²C command to apply the value.

Bits	Description	Reset	Type
7:0	ICP command or compound I²C command	d0	wr

2.4.1.22.2 ICP Data (Compound I²C Command-Data) Register (I²C: 0x39, Flash : N/A)

The compound I²C command-data (also called ICP data) register accepts a parameter associated with the compound I²C command. The need for this parameter and the range of the parameter is compound I²C command dependent and captured in the compound I²C command definition table (see Section 2.4.1.22.4).

Bits	Description	Reset	Type
31:0	(Optional) compound I²C command – data	d0	wr

2.4.1.22.3 ICP Command Handshake (I²C: 0x3A, Flash : N/A)

The “ICP command handshake” register provides a single “ICP command busy flag” that can be polled to help manage ICP command processing. The intent of this flag is to ensure a new command is not sent until processing of the prior command has been completed and that any associated data is properly transferred.

The “ICP command busy flag” is to be set by the host before it writes any new command to the ICP command register. This flag remains set until the ICP is done processing the command, and thus is used to inform the host that the ICP has not yet complete command processing. When the ICP has completed all processing associated with the command it clears the “ICP command busy flag” to inform the host it is ready to accept another command. The host is expected to poll the “ICP command handshake” register and must not send a new command until “ICP command busy flag” is cleared by the ICP. If the ICP receives a new command before processing of the prior command is complete, it aborts the prior command, sets a corresponding error in the ICP command error status register, and then processes the new command. This avoids the ICP getting hung.

When a single word, write command is received, the ICP clears the busy flag only after it reads the data from the ICP data register and writes it to the appropriate destination. When a multi-word write command is received, the ICP does the same for each 32-bit data word within the command, and then waits for the host to again set the flag to 1 to indicate that the next word is available in the ICP data register. (The host must only issue an ICP command register write before the first word on a multi-word write command).

Note, that if the host word count exceeds the word count expected by the ICP, the ICP is no longer polling the busy flag and its possible that the host can hang. Thus, the host should have a timeout. If the opposite condition occurs and the host falls short of the word count expected by the ICP, the ICP continues to poll until a new ICP command is received, at which time it aborts the multi-word write command and proceeds with the new command. The ICP flags this condition in the system status register.

If a read command is received, the ICP clears the busy flag only after it has fetched the requested data and written it to the ICP data register. The host is expected to wait for this busy flag to be cleared before sending the next command, or next word of the current command.

Bits	Description	Reset	Type
0	ICP Command Busy Flag (To be set by the host before it writes any new command to the ICP command register. To be cleared by the ICP when it completes command processing. The host is expected to wait for this busy flag to be cleared before sending the next command, or next word of the current command.) 0 = ICP command processing is idle and the ICP is ready to accept new data in a multi-word write command or otherwise a completely new command. 1 = An ICP command has been issued and is being processed (indicates that command processing is *not* complete and any command received during this time aborts processing of the prior command in order to process the new command).	b0	wr

2.4.1.22.4 Compound I²C Command Definitions

Table 23 provides a list of supported compound I²C command and their corresponding op-codes, options, and operation. Unless otherwise noted, these commands are supported by ICP program code version 1.3.1 or later.

Table 23.

Compound I2C Command			Notes
ICP Command Register (I²C: 0x38)		ICP Data Register (I²C: 0x39)	See [1]
x02	Read ICP SW Version	**ICP Software Version Read Response** Byte(0) – Patch LSByte revision Byte(1) – Patch MSByte revision Byte(2) – Minor revision Byte(3) – Major revision	See [5]
x03	Read WPC SW Version	**WPC Software Version Read Response** Byte(0) – Patch LSByte revision Byte(1) – Patch MSByte revision Byte(2) – Minor revision Byte(3) – Major revision	See [5]
x04	Read ICP AOM Template Version	**ICP AOM Template Version Read Response** Byte(0) – Patch LSByte revision Byte(1) – Patch MSByte revision Byte(2) – Minor revision Byte(3) – Major revision	See [5] [15]
x05	Read WPC AOM Template Version	**WPC AOM Template Version Read Response** Byte(0) – Patch LSByte revision Byte(1) – Patch MSByte revision Byte(2) – Minor revision Byte(3) – Major revision	See [5] [15]
x26	Gamma Set (selects and uploads new CMT table based on the desired gamma curve)	**Valid Gamma Set Selection Values:** x0000: Gamma curve 0 (OEM defined) x0001: Gamma curve 1 (OEM defined) x0002: Gamma curve 2 (OEM defined) x0003: Gamma curve 3 (OEM defined) x0004: Gamma curve 4 (OEM defined) x0005: Gamma curve 5 (OEM defined) x0006: Gamma curve 6 (OEM defined) Else: Undefined	See [4] [7] [8]

Table 23. (continued)

Compound I2C Command			Notes
xBA	Execute Register Batch File (uploads and executes the selected register batch file stored in flash)	**Valid Register Batch File Selection Values:** x0000: Register batch file 0 x0001: Register batch file 1 x0002: Register batch file 2 x0003: Register batch file 3 x0004: Register batch file 4 x0005: Register batch file 5 x0006: Register batch file 6 x0007: Register batch file 7 Else: Undefined	See [7] [8]
xBD	Write Splash Screen Select (selects, uploads, and displays the selected splash stored in flash)	K = 0 to x0003 and x0009, where K is the splash screen image number stored in the flash as mapped in ICP application data and a value of x0009 corresponds to the optical test image	See [7] [8]
xC1	Write Sequence Select (selects and uploads a new DLP® display sequence)	N = 0 to x000F, where N is the number of sequences that have been stored in the flash and mapped in the ICP application data	See [2] [3] [7] [8]
xC4	Read System Status	No command data / ICP data register is used to return system status flags	See [5] [13]
		Byte 0 (General System Status): b(0) – System Initialization 0 = No error 1 = Error b(1) – Flash Error (See Flash Status) 0 = No error 1 = Error b(2) – Overtemperature Warning 0 = No warning 1 = Warning b(3) – PAD1000 Present 0 = Not present 1 = Present b(4) – Reserved b(5) – LED Calibration Test Complete 0 = Complete 1 = Not complete b(6) – mDDR BIST Complete 0 = Complete 1 = Not complete b(7) – Reserved	See [5]
xC4	Read System Status (continued)	**Byte 1 (Communication Status):** b(0) – Invalid Command Error (Invalid CMD OpCode) 0 = No error 1 = Error b(1) – Partial Command Error (Invalid Number of Parameters) 0 = No error 1 = Error b(2) – Memory Read Continue Error (Not Applicable to I^2C Operation) b(3) – Command Parameter Error (Undefined or Illegal Parameter) 0 = No error 1 = Error b(4) – Command Abort Error (A New CMD Received While the ICP was Busy) 0 = No error 1 = Error b(7-5) – Reserved 0 = N/A 1 = N/A	See [5]

Table 23. (continued)

Compound I2C Command			Notes
xC4	Read System Status (end)	**Byte 2 (Unused Status):** b(7:0) – Reserved 0 = N/A 1 = N/A	See [5]
		Byte 3 (MISC Status): b(0) – Display Sequence Abort Error 0 = No error 1 = Error b(1) – Flash Controller DMA Abort Error 0 = No error 1 = Error b(2) – Reserved b(3) – Reserved b(4) – Reserved b(5) – Source Line Count Error 0 = No error 1 = Error b(6) – Source Pixel Count Error 0 = No error 1 = Error b(7) – DLPC2607 Hardware Error [14] 0 = No error 1 = Error	
xC5	Read Temperature Value	No command data or the ICP data register is used to return the measured temperature value (MTV) in sign-magnitude format MTV(11) = MTV sign MTV(10:0) = 10 times the MTV magnitude value in binary The host must divide the MTV value by 10 after converting to decimal to get the temperature value in °C Example 1: MTV(11:0) = 000110101010b = +426d Measured Temperature = +42.6°C Example 2: MTV(11:0) = 100110101010b = –426d Measured Temperature = –42.6°C Note that the returned value may be stale as it provides the last periodic measurement (the period of which is defined in WPC AOM) when using the “run automatically at fixed intervals” mode.	See [5]
xCA	Focus Motor Lens Movement (ABS or REL mode)	**Bytes 1 and 0:** b(9:0) – Lens Position (ABS) / Number of Steps (REL) -- is an unsigned integer If mode = ABS, then b(9:0) = ABS position relative to the default position (10 bits) If mode = REL, then b(9:0) = Number of steps to be taken (10 bits) b(15:10) = Reserved	
		Byte 2: b(16) – Lens Movement Direction (ABS/ REL) -- gives sign of value defined by bytes 2 thru 0 0 = Negative direction (4-wire sequence = HLLH, LHLH, LHHL, HLHL, HLLH, …) 1 = Positive direction (4-wire sequence = HLHL, LHHL, LHLH, HLLH, HLHL, …) b(23:17) – Reserved	

Table 23. (continued)

Compound I2C Command			Notes
xCA	Focus Motor Lens Movement (ABS or REL mode) (continued)	**Byte 3:** b(26:24) – Execute Lens Movement 000 = No action 001 = If mode is **ABS**: Go to ABS default position If mode is **REL**: No action 010 = If mode equals **ABS**: Go to selected lens position defined by bytes 2 through 0 If mode is: Move the motor the number of steps defined by bytes 2 through 0 011 = If mode is ABS: Go to reference stop or sensor transition (whichever method is selected) If mode is **REL**: no action 100 = If mode is **ABS**: re-start focus lens control function If mode is REL: no action 101= If mode is **ABS** or **REL**: Force power-down of focus lens control hardware b(31:27) – Reserved	
xCB	Focus Motor Wire State (DIR mode)	**Byte 0:** b(0) – Motor Driver 0 = Disabled 1 = Enabled b(7:1) – Reserved	
		Byte 1: b(3:0) – 4-Wire State b(7:4) – Reserved	
xCC	Focus Motor Status Register (ABS)	No Command Data / ICP Data register is used to return Focus Status Flags **Byte 0:** b(0) – Position Sensor State (0 or 1 as read from sensor) b(1) – Position Sensor Transition Detected at Start-Up 0 = > Not detected 1 = > Detected b(2) – Lens Movement command aborted 0 = Never aborted 1 = Aborted at least once b(3) = At Default Position 0 = Not at default 1 = At default b(4) = At Selected Position 0 = Not at selected position 1 = At selected position b(5) = Negative Out of Range Attempted 0 = Never attempted 1 = Attempted at least once b(6) = Positive Out of Range Attempted 0 = Never attempted 1 = Attempted at least once b(7) – Reserved	See [5]
xCD	Focus Motor Driver Control (ABS, REL, and DIR modes)	**Byte 0:** b(0) – Motor Driver Control 0 = Motor driver automatically turns on (PS = 1) when needed then shuts off (PS=0) 1 = Force motor driver always on (PS = 1) if focus lens control function is enabled	
xD0	Write PAD1000 Register Address	b(31:00) – PAD1000 address	
xD1	Read PAD1000 Register	No command data / ICP data register is used to return PAD1000 read data from the address specified by xD0 b(31:00) – PAD1000 read data value	See [5]
xD2	Write PAD1000 Register	b(31:00) – PAD1000 write data value to be the written to the address specified by xD0	
xD3	Propagate LED Currents to PAD1000	A write to this parameter (with any command data value) initiates a transfer of the 3 R, B, and G LED current values held in DLPC2607 registers x12, x13, and x14 over to the PAD1000	See [11] [12]

Table 23. (continued)

Compound I2C Command			Notes
xE9	Run LED Calibration (the results must be extracted via the read LED sensor data commands upon completion of the calibration process) **(Command not yet supported)**	A write to this parameter with any command data value triggers LED calibration	See [9] [10] [16]
xEA	Read Red LED Sensor Data (determined by LED calibration) **(Command not yet supported)**	No command data or ICP data register is used to return LED sensor data Bits 15:0 - Red LED Sensor Data	See [5] [6]
xEB	Read Green LED Sensor Data (determined by LED calibration) **(Command not yet supported)**	No command data or ICP data register is used to return LED sensor data Bits 15:0 - Green LED Sensor Data	See [5] [6]
xEC	Read Blue LED Sensor Data (determined by LED calibration) **(Command not yet supported)**	No command data or ICP data register is used to return LED sensor data Bits 15:0 - Blue LED Sensor Data	See [5] [6]
Other	Reserved	N/A	

(1) The “ICP data” parameter value must be written before the “ICP command” is written because the data value is captured upon receipt of an “ICP command” (assuming it requires data).

(2) The ICP application data file defined when building the flash determines the specific sequence that is selected.

(3) The write sequence select command automatically changes the “video frame rate (I^2C: 0x19)” parameter to match the frame rate of the selected sequence, changes the CMT table to one that matches the selected sequence and is consistent with the currently select gamma curve, and informs the WPC processor of the duty cycles associated with the selected sequence, so it can adjust accordingly. The write sequence select command should also automatically change AGC parameters that are frame rate dependent (I^2C: 0x52, 0x53, and 0x54).

(4) The gamma curve value corresponds to the CMT number associated with each sequence. Thus, CMT tables with the same CMT number, but belonging to different sequence sets, must have the same gamma curve. The gamma curve characteristics are however completely ODM defined.

(5) Before reading the ICP data register for a compound I^2C command that returns data, the host must first wait for ICP command busy flag to be cleared to 0.

(6) RGB sensor data is updated upon execution of the run LED calibration command. This data must be processed offline by the OEM, and then subsequently programmed in the WPC unit configuration data section of the flash to complete the LED calibration process.

(7) The listed max value is that which is supported by ICP software. The actual max value is further limited by what is programmed in flash and mapped in ICP application data.

(8) Any undefined parameter sent with this command is ignored, and the current table selection is not changed.

(9) This command allows the OEM to iterate the LED calibration process until a final LED golden ratio data is determined. Once this data is finalized, it should be written into the WPC unit calibration block of flash.

(10) When the DLPC2607 ICP powers up, it accesses the desired LED golden ratio data from the WPC unit calibration block of flash. A starting value must be programmed in the flash prior to calibration from which a final value can be derived through calibration and the value updated in the flash.

(11) The 0xD3 command (transfer LED current values to the PAD1000) only applies when the WPC function (Wcor) is disabled (and the PAD1000 is utilized). When Wcor is enabled (and the PAD1000 is utilized), the DLPC2607 calculates new values and transfers them automatically.

(12) To change the LED currents for PAD1000 application when the WPC function (Wcor) is disabled, the host must first write to the standard I^2C registers for R, G, and B LED currents (that is x12, x13, and x14). Note that for PAD1000 operation, these are only intermediate registers within the DLPC2607. These values must then to be transferred to PAD1000 current registers. To transfer the current values from the DLPC2607 to the PAD1000, the host must subsequently send the “propagate LED currents to PAD1000” I^2C compound command.

(13) Appropriate communication error status bits are set upon detection and then remain set until the system status register is read. The act of reading the system status register clears all error flags. Thus, status reflects errors for all commands received since the last time the register was read.

(14) DLPC2607 hardware error shall be set to a 1 if any bit, other than bits 0, 6, 8, 14 ,15, 16, or 17, is set in the DLPC2607 interrupt status register set 1 (I^2C 0x00).

(15) The ICP AOM template version is the version of the “DLPC2607_asic_cfg.h” header file and the WPC AOM template version is the version of the “wpc_cfg.h” header file, both of which are used by the DLPC2607 embedded software to access ICP application data that is stored in the flash.

(16) When the DLPC2607 ICP powers up, it accesses initial current driver PWM duty cycle value for each LED from the WPC unit calibration block of flash. A starting value must be programmed in the flash prior to calibration, so that a final value can be derived through calibration and then the value updated in the flash.

2.4.1.23 Miscellaneous Parameters

2.4.1.23.1 Software Reset (I^2C: 0x1F, Flash: 0x0000001F)

When this command is received by the projector, the data defines if a software reset occurs for the DLPC2607. When written with any value, a software reset occurs. This command has no specific intended application. It is provided simply as a back-up recovery mechanism.

Table 24. (1)

Bits	Description	Reset	Type
0	Software Reset: 0 – Software reset is recognized (bit value is don't care) 1 – Software reset is recognized (bit value is don't care)	d0	wr

(1) Prior to issuing a software reset command, TI recommends that a DMD PARK (I^2C: 0x2D) command be applied first, followed by a 500-µs wait interval before issuing the reset.

2.4.1.23.2 Front End Reset (I^2C: 0x21, Flash: 0x00000021)

When this command is received by the projector, a front end reset occurs in the DLPC2607. A front end reset, resets all logic that operates on the external pixel clock. This command has no required application but rather provides a back-up recovery mechanism in the event of the source clock falls outside specs and causes the logic state of the DLPC2607 to be upset. The value that is written is don't care, but 0 is recommended.

Bits	Description	Reset	Type
0	Front End Reset: 0 – Front end reset is recognized (bit value is don't care) 1 – Front end reset is recognized (bit value is don't care)	b0	wr

2.4.1.23.3 MSP430 Firmware Revision (I^2C: 0x30, Flash: 0x00000030)

This is a general purpose read or write storage register. The value written has no affect on DLPC2607 operation. It is provided for use in accessory projector applications to store MSP430 firmware revision information making it more easily accessible from an external host; because, there is no way to read this information directly from the MSP430. This register can be used for other reasons if the MSP430 is not present in the system.

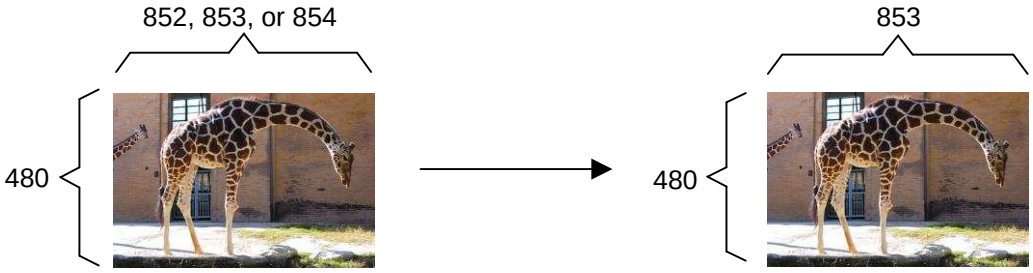
Bits	Description	Reset	Type
5:0	6-bit general purpose R/W register	x00	wr

2.4.2 Sample Display Options for Various Input Image Resolutions and Orientations

The following sections provide a sample of the display option for various input image resolutions and orientations. This includes only a subset of available source options.

2.4.2.1 Landscape WVGA (852 × 480, 853 × 480, or 854 × 480) Source to WVGA (853 × 480)

Scale Factor: Uniform

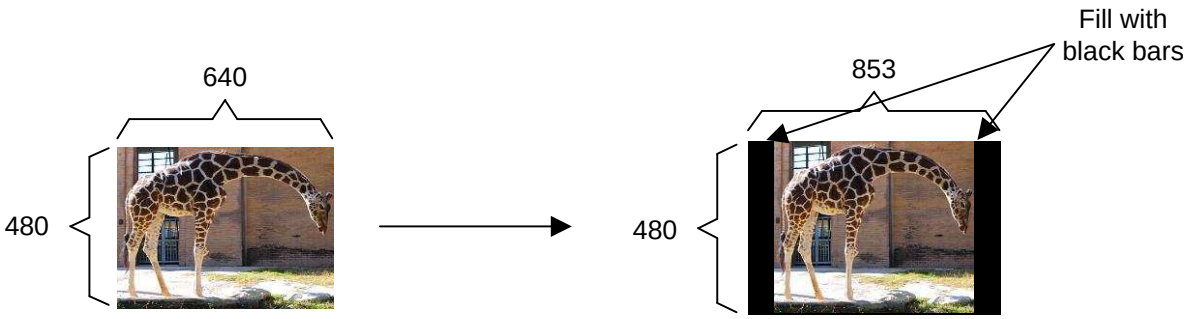


Commands:	Image Resolution:	WVGA landscape	(Addr x0C=xF,x11,x13)
	Image Rotation:	No rotation	(Addr x0E=x0)

2.4.2.2 Landscape VGA Source to WVGA

Scale Factor: Uniform

Note that other WVGA resolutions such as 720 × 480, 752 × 480, and 800 × 480 are uniformly scaled and displayed with vertical black bars similar to a VGA source (as shown in the following image.)

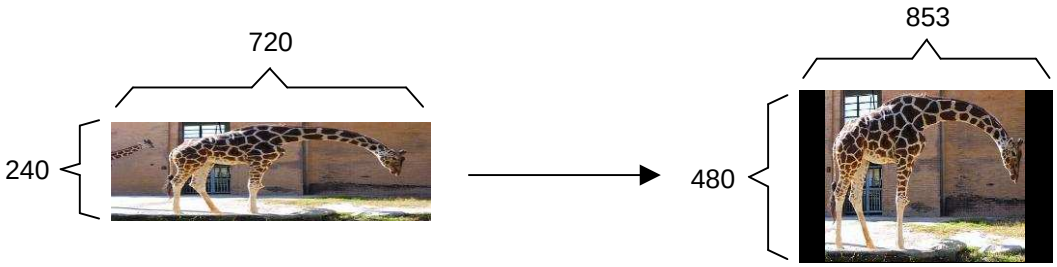


Commands:	Image Resolution:	VGA landscape	(Addr x0C=x7)
	Image Rotation:	No rotation	(Addr x0E=x0)

2.4.2.3 Landscape NTSC Source to WVGA

Scale Factor: Non-Uniform

The image size is 720 × 240 output by the TVP5151 video decoder for each 60-Hz NTSC field. The image is only 240 lines tall because every other line is missing due to interlacing. The DLPC2607 scales the field to create a full frame of data to display on the DMD at a 60-Hz frame rate. The scaling operation achieves a low-cost method of de-interlacing.

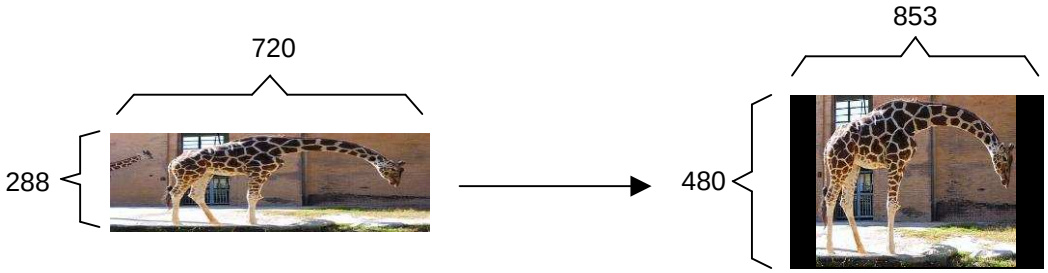


Commands:	Image Resolution:	NTSC landscape	(Addr x0C=x17)
	Image Rotation:	No rotation	(Addr x0E=x0)

2.4.2.4 Landscape PAL or SECAM Source to WVGA

Scale Factor: Non-Uniform

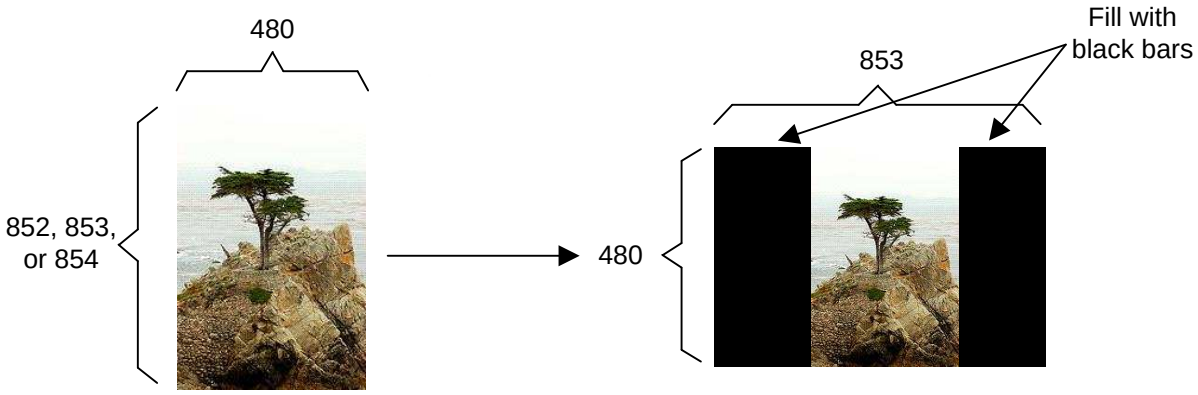
The image size is 720 × 288 output by the TVP5151 video decoder for each 60-Hz PAL or SECAM field. The image is only 288 lines tall because every other line is missing due to interlacing. The DLPC2607 scales the field to create a full frame of data to display on the DMD at a 50-Hz frame rate. The scaling operation achieves a low-cost method of de-interlacing.



Commands:	Image Resolution:	PAL or SECAM landscape	(Addr x0C=x19)
	Image Rotation:	No rotation	(Addr x0E=x0)

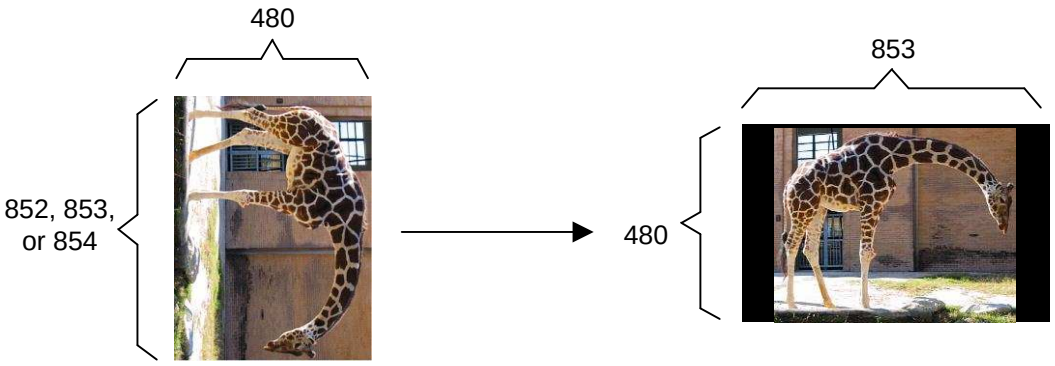
2.4.2.5 Portrait WVGA (852x480, 853x480 or 854x480) Source to WVGA (853x480)

For Normal Image
Scale Factor: Uniform



Commands:	Image Resolution:	WVGA portrait	(Addr x0C=xE,x10,x12)
	Image Rotation:	No rotation	(Addr x0E=x0)

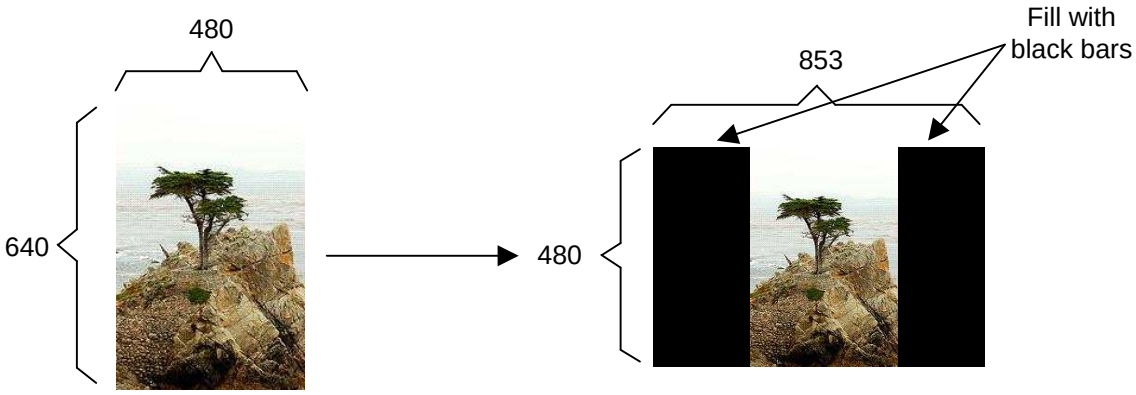
For Rotated Image:
Scale Factor: Uniform



Commands:	Image Resolution:	WVGA portrait	(Addr x0C= xE,x10,x12)
	Image Rotation:	Rotation (–90°)	(Addr x0E=x1)

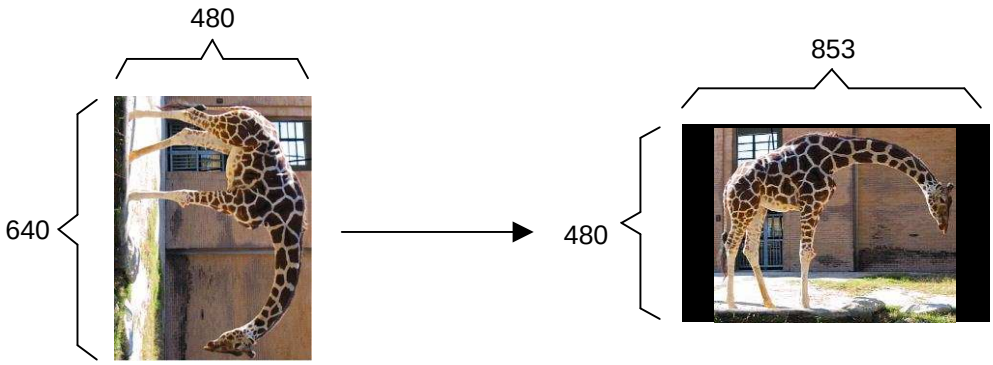
2.4.2.6 Portrait VGA source to WVGA

For Normal Image:
Scale Factor: Uniform



Commands:	Image Resolution:	VGA portrait	(Addr x0C=x6)
	Image Rotation:	No rotation	(Addr x0E=x0)

For Rotated Image:
Scale Factor: Uniform



Commands:	Image Resolution:	VGA portrait	(Addr x0C=x6)
	Image Rotation:	No rotation (–90°)	(Addr x0E=x1)

3 Power-Up, Power-Down, and Initialization Considerations

3.1 Power-Up

The DLPC2607 electronics and I^2C command processor interface inside the DLPC2607 are initialized and ready to process commands 0.1 s after the signal RESETZ goes high. Detailed power-up timing is given in the DLPC2607 data sheet, DLPS030.

3.2 Power-Down

No commands are required at the power-down of the DLPC2607. The DC power supplies must be turned off and PWRGOOD must be set low, according to the timing in the DLPC2607 data sheet.

3.3 Power-Up Auto-Initialization

Upon release of system reset, the DLPC2607 execute an auto-initialization routine, which is automatically uploaded from flash. This initialization process consists of setting ODM specific register configurations, uploading ODM specific configuration tables (such as sequence, CMT, and so forth), running mDDR memory BIST, displaying an ODM defined splash screen for a fixed amount of time and then running an ODM generated configuration batch file to program the DLPC2607 for the desired mode of operation. The goal of the auto-initialization process is to allow the DLPC2607 to fully configure itself for default operation with no external I^2C control.

An “auto-initialization” status flag, GPIO4_INTF, is held high to indicate that auto initialization is in progress. It is set low when “auto-initialization” is complete. Subsequently, GPIO4_INTF is typically configured as an output interrupt signal that outputs an active high pulse when an error condition exists (see Section 2.2).

4 Mode Transition and System Reconfiguration Requirements

Re-configuring the system is a process that could result in artifacts or corrupted data being displayed, if not properly handled. Re-configuration generally includes such operations as source selection changes, operational mode changes, and feature selection changes. In general, if a change could potentially cause some form of undesirable artifact, proper transition procedures must be followed to minimize the artifact. These procedures apply to source attributes changes (channel, resolution, and format) and display attributes changes (rotation and flip). Although DLP® display sequence changes, sequence synchronization mode (free-run to lock-to-VSYNC or vice versa) changes and CMT table changes also result in display artifacts, if not managed properly, the DLPC2607 ICP processor manage these transitions internally.

In general, the process is to either turn off the LEDs (resulting in the display turned off), blank the screen (also called, put up a curtain), or freeze the last displayed image to hide the visible effects resulting from data-path re-configuration from the viewer.

The following is the generalized procedure that should be followed for LUT changes, source attribute changes (channel, resolution, and format), and display attributes changes (rotation and flip). In general, this can be done by freezing the image in the Formatter Buffer. By freezing the formatter buffer before making any changes it ensures that if a frame boundary passes, that the formatter buffer does not swap and expose intermediate parameter changes to the viewer.

1. Freeze the formatter display buffer by setting freeze or buffer swap disable bit to 1 (I^2C address 0xA3)
   (a) The formatter continues to display the last image.
   (b) In general, wait for at least one frame (20 ms) before freezing the formatter to allow the last frame to propagate to the display.
   (c) To display a black screen instead of the last displayed image, set the curtain enable bit to 1 (I^2C address 0xA6). Note that this is the recommended operation for a long-side flip.
2. Do the necessary system reconfiguration:
   (a) For mode changes, set the interface bit as desired (I^2C address 0x18)
   (b) Load the new CMT tables either through I^2C or flash DMA
   (c) Make source attribute changes as desired:

(i) Channel – I^2C address 0x0B
(ii) Resolution – I^2C address 0x0C
(iii) Format – I^2C address 0x0D

(d) Make display attributes changes as desired:
(i) Rotation – I^2C address 0x0E
(ii) Flip – I^2C address 0x0F and 0x10

3. If the last displayed image was a still image, then the still image must be re-sent before unfreezing.
4. Wait for at least 20 ms (1 to 50-Hz frame timing) before unfreezing the display buffer to allow a completely new image to propagate to the formatter input buffer.
5. Unfreeze the display buffer by setting the freeze or buffer swap disable bit to 0 (I^2C address 0xA3).
(a) The unfreeze operation is synchronized to the vertical sync to avoid tearing.

Appendix A Command Quick Reference

The following table provides a quick reference summary of all available projector commands. The default values shown are the DLPC2607 hardware power-up reset values. This value may be subsequently modified by auto-initialization based on auto-configuration data stored in flash. All register addresses not listed in Section A.1 are reserved or allocated solely to auto-configuration. To avoid the risk of corrupting ASIC operation, do not access an unlisted register.

A.1 Register Quick Reference

I^2C Address	Flash Address	Description	Type[1][2]	Reset Value[3]	Default Action	Section Number
0x00	N/A	Interrupt clear register	I	N/A		Section 2.4.1.1
0x01	N/A	Interrupt set register	I	N/A		Section 2.4.1.1
0x03	N/A	Main status registers	RO	0x 88		Section 2.4.1.2
0x07	N/A	Flash read register	RO			
0x08	N/A	Flash memory controller mode of operation	RW	0x 0	Reset	Section 2.4.1.18.1
N/A	0x00000009	DMA read stall	RW	0x 0	N/A	
0x0B	0x0000000B	Input source selection	RW	0x 2	Splash	Section 2.4.1.3
0x0C	0x0000000C	Input resolution selection	RW	0x 1	QVGA landscape	Section 2.4.1.6
0x0D	0x0000000D	Pixel data format select	RW	0x 2	RGB888	Section 2.4.1.5
0x0E	0x0000000E	Image rotation control	RW	0x 0	No rotate	Section 2.4.1.7
0x0F	0x0000000F	Long-side image flip control	RW	0x 0	Disabled	Section 2.4.1.8
0x10	0x00000010	Short-side image flip control	RW	0x 0	Disabled	Section 2.4.1.9
0x11	0x00000011	Internal test pattern select	RW	0x D	Checkerboard	Section 2.4.1.10
0x12	0x00000012	Red LED driver current	RW	0x03FF	Min current	Section 2.4.1.11.2
0x13	0x00000013	Green LED driver current	RW	0x03FF	Min current	Section 2.4.1.11.3
0x14	0x00000014	Blue LED driver current	RW	0x03FF	Min current	Section 2.4.1.11.4
0x15	N/A	Reserved for I^2C read				
0x16	0x00000016	RGB LED driver enables	RW	0x 0	Disabled	Section 2.4.1.11.1
0x19	0x00000019	Video frame rate	RW	0x0859	60 Hz	Section 2.4.1.13.1
0x1E	0x0000001E	Sequence sync mode	RW	0x 0	Free-run	Section 2.4.1.14.2
0x1F	0x0000001F	Software reset	RW	0x 0	Not in reset	Section 2.4.1.23.1
0x21	0x00000021	Front end reset	RW	0x 0	Not in reset	Section 2.4.1.23.2
0x23	0x00000023	Vertical sync line delay	RW	0x 5	Delay = 5 lines	Section 2.4.1.12.4
0x29	0x00000029	Auto framing – first active line in a frame	RW	0x 0	N/A	Section 2.4.1.12.6.1
0x2A	0x0000002A	Auto framing – last active line in a frame	RW	0x 0	N/A	Section 2.4.1.12.6.2
0x2B	0x0000002B	Auto framing – first active pixel in a line	RW	0x 0	N/A	Section 2.4.1.12.6.3
0x2C	0x0000002C	Auto framing – last active pixel in a line	RW	0x 0	N/A	Section 2.4.1.12.6.3
0x2D	0x0000002D	DMD park control	RW	0x 0	Disabled	Section 2.4.1.17.3
0x30	N/A	MSP430 firmware revision	RW	0x 0		Section 2.4.1.22.4
0x33	0x00000032	Chroma channel swap	RW	0x 0		Section 2.4.1.4.3

(1) 'RW' type is writeable and data is also readable.
(2) 'RO' type is read-only. Writes to these fields have no effect.
(3) Note that the "reset value" listed in the table is the hardware reset value, which for some registers, is overwritten by auto-initialization software.

I²C Address	Flash Address	Description	Type[1][2]	Reset Value[3]	Default Action	Section Number
0x38	N/A	ICP Command **— Compound I²C CMDs —** 0x02: Read ICP SW version 0x03: Read WPC SW version 0x04: Read ICP AOM version 0x05: Read WPC AOM version 0x26: Gamma set 0xBA: Run register batch file 0xBD: Write splash select 0xC1: Write sequence select 0xC4: Read system status 0xC5: Read temperature value 0xCA: Focus motor lens control 0xCB: Focus motor write state 0xCC: Focus motor status 0xCD: Focus motor driver control 0xE9: Run LED calibration 0xEA: Read red LED sensor 0xEB: Read green LED sensor 0xEC: Read blue LED sensor	RW	0x 0		Section 2.4.1.22.1
0x39	0x00000039	ICP data	RW	0x 0		Section 2.4.1.22.2
0x3A	0x0000003A	ICP command handshake	RW	0x 0		Section 2.4.1.22.3
0x3B	0x0000003B	Reserved	RW	0x 0		
0x50	0x00000050	AGC control	RW	0x 6	AGC disabled	Section 2.4.1.15.2.1
0x52	0x00000052	AGC step-size increment	RW	0x 1		Section 2.4.1.15.2.2
0x53	0x00000053	AGC step-size decrement	RW	0x 1		Section 2.4.1.15.2.3
0x54	0x00000054	AGC leap-size decrement	RW	0x 28		Section 2.4.1.15.2.4
0x5E	0x0000005E	CCA control	RW	0x 1		Section 2.4.1.15.3
0x5F	0x0000005F	CCA parameter – red 1	RW	0x 100		Section 2.4.1.15.3.2
0x60	0x00000060	CCA parameter – red 2	RW	0x 0		Section 2.4.1.15.3.3
0x61	0x00000061	CCA parameter – red 3	RW	0x 0		Section 2.4.1.15.3.4
0x62	0x00000062	CCA parameter – green 1	RW	0x 0		Section 2.4.1.15.3.5
0x63	0x00000063	CCA parameter – green 2	RW	0x 100		Section 2.4.1.15.3.6
0x64	0x00000064	CCA parameter – green 3	RW	0x 0		Section 2.4.1.15.3.7
0x65	0x00000065	CCA parameter – blue 1	RW	0x 0		Section 2.4.1.15.3.8
0x66	0x00000066	CCA parameter – blue 2	RW	0x 0		Section 2.4.1.15.3.9
0x67	0x00000067	CCA parameter – blue 3	RW	0x 100		Section 2.4.1.15.3.10
0x71	0x00000071	CCA parameter – white 1	RW	0x 100		Section 2.4.1.15.3.20
0x72	0x00000072	CCA parameter – white 2	RW	0x 100		Section 2.4.1.15.3.21
0x73	0x00000073	CCA parameter – white 3	RW	0x 100		Section 2.4.1.15.3.22
0x74	0x00000074	Flash ADDR BYTES	RW	0x 3		Section 2.4.1.18.4
0x75	0x00000075	Flash dummy BYTES	RW	0x1		Section 2.4.1.18.5
0x76	0x00000076	Flash WDATA BYTES	RW	0x 0		Section 2.4.1.18.6
0x77	0x00000077	Flash RDATA BYTES	RW	0x 0		Section 2.4.1.18.7
0x78	0x00000078	Flash OPCODE	RW	0x 0		Section 2.4.1.18.8
0x79	0x00000079	Flash ADDRESS	RW	0x 0		Section 2.4.1.18.9
0x7B	0x0000007B	Flash write DATA	RW	0x 0		Section 2.4.1.18.10
0x7C	0x0000007C	Flash write BYTE enable	RW	0x F		Section 2.4.1.18.11
0x7E	0x0000007E	Temporal dither control	RW	0x 2	Dither disabled	Section 2.4.1.15.1
0x83	0x00000083	Sequence vector set-up	RW	0x 0	SEQ VECT = 0, Two sub-vectors per SEQ	Section 2.4.1.14.1
0x9B	N/A	mDDR memory BIST status	RO	0x 0		Section 2.4.1.16.2
0xA3	0x000000A3	Display buffer swap freeze	RW	0x 0	Unfrozen	Section 2.4.1.16.1
0xA4	0x000000A4	YCrCb to RGB control	RW	0x E	BT.601	Section 2.4.1.4.2
0xA6	0x000000A6	Display image curtain control	RW	0x 0	Curtain disabled	Section 2.4.1.17.1
0xA7	0x000000A7	DMD bus swap enable	RW	0x 0	Disabled	Section 2.4.1.17.2
0xAE	0x000000AE	Auto-framing function enable	RW	0x 0	Disabled	Section 2.4.1.12.5.1
0xAF	0x000000AF	Parallel bus polarity control	RW	0x 10		Section 2.4.1.12.1

I²C Address	Flash Address	Description	Type[1][2]	Reset Value[3]	Default Action	Section Number
0xB0	0x000000B0	Auto framing - horizontal back porch select	RW	0x 0		Section 2.4.1.12.5.2
0xB1	0x000000B1	Auto framing - vertical back porch select	RW	0x 17		Section 2.4.1.12.5.3
0xB2	0x000000B2	Parallel bus data mask polarity	RW	0x 1	Active high	Section 2.4.1.12.2
0xB3	0x000000B3	Parallel bus data mask enable	RW	0x 0	Disabled	Section 2.4.1.12.3
0xB4	0x000000B4	Golden ratio	RW	0x 0		Section 2.4.1.11.5
0xB5	0x000000B5	WPC control	RW	0x 0	Disabled	Section 2.4.1.11.6
0xC3	0x000000C3	Source color space and sampling control	RW	0x 0	RGB, 4:4:4	Section 2.4.1.4.1
0xCF	0x000000CF	Reserved (AT)	RW	0x 0	Disabled	
0xD0	0x000000D0	Reserved (AT)	RW	0x 0		
0xD1	0x000000D1	Reserved (AT)	RW	0x 0		
0xD2	0x000000D2	Reserved (AT)	RW	0x 0		
0xD3	0x000000D3	Reserved (AT)	RW	0x 0		
0xD4	0x000000D4	Reserved (AT)	RW	0x 0		
0xF7	0x000000F7	ICP program memory sub-address	RW	0x 0		Section 2.4.1.21.1
0xF8	0x000000F8	ICP program memory configuration	RW	0x 0	No memories selected	Section 2.4.1.21.2
0xF9	0x000000F9	ICP program memory data access port	RW	0x 0		Section 2.4.1.21.3
0xFA	0x000000FA	SCL, CMT, BNM, or splash sub-address	RW	0x 0		Section 2.4.1.19.1
0xFB	0x000000FB	SCL, CMT, BNM, or splash memory configuration	RW	0x 0	No memories selected	Section 2.4.1.19.2
0xFC	0x000000FC	SCL, CMT, BNM, or splash memory data access port	RW	0x 0		Section 2.4.1.19.3
0xFD	0x000000FD	WPC, SEQ, or DRC LUT sub-address	RW	0x 0		Section 2.4.1.20.1
0xFE	0x000000FE	WPC, SEQ, or DRC memory configuration	RW	0x 0	No memories selected	Section 2.4.1.20.2
0xFF	0x000000FF	WPC, SEQ, or DRC memory data access port	RW	0x 0		Section 2.4.1.20.3

A.2 Mailbox Quick Reference

Parameter	I²C Transaction	CMT	Splash	Sequence	DRC	WPC	ICP	SCL Sharpness
LUT Start Address	I²C sub-address	0xFA	0xFA	0xFD	0xFD	0xFD	0xF7	0xFA
	Data value	0	0	0	0	0	0	0
LUT Configuration Select	I²C sub-address	0xFB	0xFB	0xFE	0xFE	0xFE	0xF8	0xFB
	Data value	x6	x5	x5	x6	x7	x1	H-SCL: x7
								V-SCL: x8
LUT Data Mailbox	I²C sub-address	0xFC	0xFC	0xFF	0xFF	0xFF	0xF9	0xFC
	Data value	As defined by TI Tools[1]	As desired[1]	As defined by TI Tools[1]	As defined by TI	As defined by TI	As defined by TI	As defined by TI
	Data packing	2-Bytes per entry	2-Bytes per entry	4-Bytes per entry	4-Bytes per entry	4-Bytes per entry	4-Bytes per entry	4-Bytes per entry
	Data length in number of entries (reference only)	768 entries[2]	Varies based on image size[3]	Varies based on sequence (max entries = 2048)	64 entries	Varies based on program (max entries = 2048)	Varies based on program (max entries = 2048)	H-SCL: 80 entries V-SCL: 48 entries
	Data length in bytes	3072	2045, 960 (QWVGA)	Varies	256	Varies	Varies	H-SCL: 320 V-SCL: 192

(1) Sequential data beginning at address 0 and progressing until all data is sent

(2) For CMT green, red and blue tables are concatenated in this order

(3) Typical size of splash for WVGA and nHD applications is QWVGA consisting of 102480 entries. Typical size of splash for VGA applications is QVGA consisting of 76800 entries (only optical splash should be full resolution)

Appendix B Example Batch Files

The following is an example of selected batch files.

B.1 Sequence Instruction Set Memory Upload from Flash via DMA

Note that this process is obsolete when using compound I^2C commands (see Section 2.4.1.22.4) as individual register accesses, demonstrated in the following example, are simplified into a more abstract command.

```
# Load SEQ memory via FLASH DMA from splash
# Set up DMA start address (assume the starting Sequence location = x0004A000)
w 0x36 0x79 0x00 0x04 0xA0 0x00
# Set up DMA size (Read Byte quantity is 4KBytes or x00001000)
w 0x36 0x77 0x00 0x00 0x10 0x00
# Set up Flash Read Opcode
w 0x36 0x78 0x00 0x00 0x00 0x0B
# Set up Flash Read dummy bytes
w 0x36 0x75 0x00 0x00 0x00 0x01
# Set up Flash address bytes
w 0x36 0x74 0x00 0x00 0x00 0x03
# Set up CMIS1 Memory select (Open the SEQ Memory)
w 0x36 0xFE 0x00 0x00 0x00 0x05
# Set up CMIS1 address (Set the starting address in the SEQ Memory to zero)
w 0x36 0xFD 0x00 0x00 0x00 0x00
# Transfer control to flash read (Note FMC automatically infers CMIS1 Data
Register)
w 0x36 0x08 0x00 0x00 0x00 0x01
# Wait some time to allow DMA to complete before testing DMA status
delay 2 usec
# Read DMA Busy status to see that DMA is in fact done
w 0x36 0x15 0x03
r 0x37 0x04
# # Transfer control from flash read back to I2C
w 0x36 0x08 0x00 0x00 0x00 0x00
# Close CMIS1 mailbox(Close the SEQ Memory)
w 0x36 0xFE 0x00 0x00 0x00 0x00
```

B.2 CMT Table Memory Upload from Flash via DMA

Note that this process is obsolete when using compound I²C commands (see Section 2.4.1.22.4) as individual register accesses, as demonstrated in the following example, are simplified into a more abstract command.

```
# Set up DMA start flash address (starting CMT table 1 location = x0004B800)
w 0x36 0x79 0x00 0x04 0xB8 0x00

# Set up DMA size (Read Byte quantity is 1.5KBytes or x00000600)
w 0x36 0x77 0x00 0x00 0x06 0x00

# Set up Flash Read Opcode
w 0x36 0x78 0x00 0x00 0x00 0x0B

# Set up Flash Read dummy bytes
w 0x36 0x75 0x00 0x00 0x00 0x01

# Set up Flash address bytes
w 0x36 0x74 0x00 0x00 0x00 0x03

# Set up CMIS0 (Splash-CMT) Memory select (Open the CMT "ALL" LUT Memory)
w 0x36 0xFB 0x00 0x00 0x00 0x04

# Set up CMIS0 address (Set the starting address in the CMT Memory to zero)
w 0x36 0xFA 0x00 0x00 0x00 0x00

# Transfer control to flash read (Note FMC automatically infers CMIS0 Data
Register)
w 0x36 0x08 0x00 0x00 0x00 0x01

# Wait some time to allow DMA to complete before testing DMA status
delay 2 usec

# Read DMA Busy status to see that DMA is in fact done
w 0x36 0x15 0x03
r 0x37 0x04

# # Transfer control from flash read back to I2C
w 0x36 0x08 0x00 0x00 0x00 0x00

# Close CMIS0 mailbox(Close the CMT Memory)
w 0x36 0xFB 0x00 0x00 0x00 0x00
```

B.3 Auto-Configuration Data, Batch File Upload from Flash via DMA

The following example shows how to use an auto-configuration batch file that is stored in flash and subsequently uploaded upon command. An optical engine manufacturer or design house can take any I^2C-based batch file and convert it to flash storage format. After storing in flash, a few simple commands allow the user to execute the stored batch file.

B.3.1 Loading an Auto Configuration Batch File Stored in Flash via DMA

The following example shows how to upload an auto-configuration batch file that is stored in flash. This example assumes the batch file created in the prior section stored at starting flash memory location x00043000).

```
# Set up DMA start flash address (XYZ batch file start location= x00043000)
w 0x36 0x79  0x00 0x04 0x30 0x00

# Set up DMA size (The batch file in this example is 128 Bytes or x00000080)
w 0x36 0x77 0x00 0x00 0x00 0x80

# Set up Flash Read Opcode
w 0x36 0x78 0x00 0x00 0x00 0x0B

# Set up Flash Read dummy bytes
w 0x36 0x75 0x00 0x00 0x00 0x01

# Set up Flash address bytes
w 0x36 0x74 0x00 0x00 0x00 0x03

# Transfer control to "Flash to Configuration Register DMA operation" (also
called Auto Init upload)
w 0x36 0x08 0x00 0x00 0x00 0x02

# Wait some time to allow DMA to complete before testing DMA status
delay 0.5 usec

# Read DMA Busy status to see that DMA is in fact done
w 0x36 0x15 0x03
r 0x37 0x04

# "If" DMA is still busy then Wait some more time to allow DMA to complete
before
#  again testing DMA status (that is Poll the busy flag)
    delay 0.5 usec
    w 0x36 0x15 0x03
    r 0x37 0x04

# Transfer control from flash read back to I2C
w 0x36 0x08 0x00 0x00 0x00 0x00
```

B.3.2 Flash Write Enable

```
#set up DLPC2607 to do a write enable command opcode
#Flash addr bytes
w 0x36 0x74 0x00 0x00 0x00 0x00
#Flash dummy bytes
w 0x36 0x75 0x00 0x00 0x00 0x00
#Flash write data bytes
w 0x36 0x76 0x00 0x00 0x00 0x00
#Flash read data bytes
w 0x36 0x77 0x00 0x00 0x00 0x00
#Write enable opcode
w 0x36 0x78 0x00 0x00 0x00 0x06
#Switch I2P mux to Flash command
w 0x36 0x08 0x00 0x00 0x00 0x05
delay 10usec
#Switch I2P mux to I2C command
w 0x36 0x08 0x00 0x00 0x00 0x00
```

B.3.3 Sector Erase

```
#Sector erase
#First set up DLPC2607 to do a write enable command opcode

#Switch I2P mux to I2C
w 0x36 0x08 0x00 0x00 0x00 0x00

# Set up DMA start address (the starting Flash erase location to x00042000)
w 0x36 0x79  0x00 0x04 0x20 0x00

#Flash write data bytes (0 since erasing we are not writing thro I2C)
w 0x36 0x76 0x00 0x00 0x00 0x00

#Flash addr bytes
w 0x36 0x74 0x00 0x00 0x00 0x03

#Flash dummy bytes
w 0x36 0x75 0x00 0x00 0x00 0x00

#sector erase opcode
w 0x36 0x78 0x00 0x00 0x00 0x20

#Write TX byte enable
w 0x36 0x7C 0x00 0x00 0x00 0x0F

#Switch I2P mux to Flash command
w 0x36 0x08 0x00 0x00 0x00 0x05

#Switch I2P mux to I2C
w 0x36 0x08 0x00 0x00 0x00 0x00
```

Appendix C Example Flash Memory Map

The following is a list of the elements that are typically contained in a standard flash build.

Element	Description	Required	Variable	QTY	Size Per (KBytes)
ICP Firmware	Initialization and command processing firmware. Required ASIC firmware. This firmware should only change for a TI product update.	Yes	No	1	8.0
WPC Firmware	LED WPC, LED power control, and thermistor monitor firmware with optional ASIC features. This firmware should only change for a TI product update. Although a maximum of 7.5KB, it must be aligned to the *end* of a 4KB sector such that is can be contiguous with WPC series calibration data.	No	No	0-1 (1)	7.5
WPC Product Series Calibration Data	WPC product series calibration data contains a voltage or current curve corresponding to the LED type used in the product series. This data block must immediately follow the WPC program code and must be on a sector boundary to facilitate the erase and re-programming of this data without affecting other flash content. This requires an actual allocation of 1 full sector.	No	No	0-1 (1)	0.5 (4.0 allocation)
WPC Unit Calibration Data	WPC unit calibration data contains a LED golden ratio data for the specific unit. This data block must be on a sector boundary to facilitate the erase and re-programming of this data without affecting other flash content. Thus, this requires an actual allocation of one full sector.	No	No	0-1 (1)	0.25 (4.0 allocation)
DRC	DMD reset control waveform look-up table. This firmware should never change.	Yes	No	1	0.25
Vertical Sharpness	Scaler vertical sharpness coefficient look-up table. This firmware should rarely change.	Yes	No	1-M	1.25
Horizontal Sharpness	Scaler horizontal sharpness coefficient look-up table. This firmware should rarely change.	Yes	No	1-M	0.75
BNM Thresholds	Contour mitigation blue noise mask (BNM) threshold data. This firmware is unique for the nHD versus VGA versus WVGA DMD, but should rarely change for a given ASIC type.	Yes	Yes	1	1.0
CMT LUT Set	Contour mitigation look-up table consists of gamma correction and dithering data. A set consists of one red, one green, and one blue table concatenated together. Only one CMT table set can be used at a given time but multiple table options are typically desired for a given product. The selected CMT table must be matched with the sequence instruction set.	Yes	Yes	1-N	1.5
Sequence Instruction Set	The sequence instruction set defines the order and length of time each bit plane is displayed on the DMD. Only one instruction set can be used at a given time but multiple options are typically desired for a given product. The instruction set varies based on frame rate and desired color duty cycle.	Yes	Yes	1-N	5.0 (2)
Optical Test Splash Screen	Full WVGA splash screen that maps pixel for pixel to the 0.3, diamond WVGA DMD.	No	Yes	0-N	812.25
	Full WVGA splash screen that maps pixel for pixel to the 0.24, diamond VGA DMD.				812.25
	Full nHD splash screen that maps pixel for pixel to the 0.2, Manhattan nHD DMD.				450.0
Standard Splash Screen	QWVGA (427 × 240) splash screen for WVGA and nHD applications	No	Yes	0-N	200.625
	QVGA (320 × 240) splash screen for VGA applications				150
ICP Application Data	ICP application data consists of a set of system initialization parameters along with an address pointer table to various other data stored in the flash.	No	Yes	1	4

(1) If no WPC firmware is included, then the host processor must set LED currents through DLPC2607 programmable LED PWM registers.
(2) Sequence size is variable but should be less than the 5.0K byte size listed above.

Element	Description	Required	Variable	QTY	Size Per (KBytes)
Register Batch File	Register batch files define a series of configuration register writes to the DLPC2607 register space (address x00 to xFF). These files consist of a simple set of address or data pairs. An optical engine manufacturer or design house can take any I^2C-based batch file and convert it to flash storage format for use as a register batch file. Once stored in flash, a few simple commands allow the user to execute the stored batch file. Two such batch files are also called as part of auto initialization providing the option to customize ASIC register settings as part of initialization.	Yes	Yes	1-N	0.5
User Configuration Data	A sector in flash reserved for use by the host processor. For example, calibration data may be programmed here at the time of manufacturing test to be read by the host processor upon initialization. Must be a full sector size and sector aligned to support erase and reprogramming.	No	Yes	0-N	4
Thermistor LUT	Temperature response curve for the thermistor used for overtemperature sensing.	No	Yes	1	3.5

The following example shows a flash memory map. It is the exact map that is used in the DLPC2607 reference design. Note that the reference design utilizes a 16Mbit flash but the memory map is designed to support 4Mbit, 8Mbit, and 16Mbit flash devices with a graduated level of content support. The specific content supported is captured in the following.

Flash Density (Mbit)	Quantity of Features that are Supported				
	Optical Test Splash Screens	Standard Splash Screens	User Data Sector	PWM Sequences	CMT Tables per SEQ
4M-bit	0	1	1	9	7
8M-bit	0	3	1	16	2
16M-bit	1	4	1	16	7

The following is the DLPC2607 reference design flash memory map:

Table 25. 4M-bit Address Map [1] [7]

Starting Address	Data located at this address	Size (Bytes)	Required	Notes
x0000,0000	ICP application data	4K	Yes, unless auto-init is disabled	See [2]
x0000,1000	ICP Program Code	8K	Yes, unless Auto-Init is disabled	
x0000,3000	Reserved	0.50K		
x0000,3200	WPC program code	7.50K		See [3]
x0000,5000	WPC product series data	0.50K		See [4]
x0000,5200	Thermistor LUT	3.50K		See [11]
x0000,6000	WPC unit calibration data	4K		See [5]
x0000,7000	Register batch file number 0	0.50K		
x0000,7200	Register batch file number 1	0.50K		
x0000,7400	Register batch file number 2	0.50K		
x0000,7600	Register batch file number 3	0.50K		
x0000,7800	Register batch file number 4	0.50K		
x0000,7A00	Register batch file number 5	0.50K		
x0000,7C00	Register batch file number 6	0.50K		
x0000,7E00	Register batch file number 7	0.50K		
x0000,8000	BNM thresholds	1K	Yes – always	See [10]
x0000,8400	DRC	0.25K	Yes – always	
x0000,8500	Reserved	0.75K		
x0000,8800	Reserved	0.50K		

Table 25. 4M-bit Address Map [1] [7] (continued)

Starting Address	Data located at this address	Size (Bytes)	Required	Notes
x0000,8A00	Reserved (spare)	1.50K		
x0000,9000	Vertical sharpness number 0	0.75K	Yes – always	
x0000,9300	Horizontal sharpness number 0	1.25K	Yes – always	
x0000,9800	Vertical sharpness number 1	0.75K		
x0000,9B00	Horizontal sharpness number 1	1.25K		
x0000,A000	Sequence set number 0 – sequence	5K	Yes – always	See [8]
x0000,B400	Sequence set number 0 – CMT set number 0	1.5K	Yes – always	
x0000,BA00	Sequence set number 0 – CMT set number 1	1.5K		
x0000,C000	Sequence set number 0 – CMT set number 2	1.5K		
x0000,C600	Sequence set number 0 – CMT set number 3	1.5K		
x0000,CC00	Sequence set number 0 – CMT set number 4	1.5K		
x0000,D200	Sequence set number 0 – CMT set number 5	1.5K		
x0000,D800	Sequence set number 0 – CMT set number 6	1.5K		
x0000,DE00	Reserved (unavailable)	0.50K		Unavailable
x0000,E000	Sequence set number 1 – sequence	5K		See [8]
x0000,F400	Sequence set number 1 – CMT set number 0	1.5K		
x0000,FA00	Sequence set number 1 – CMT set number 1	1.5K		
x0001,0000	Sequence set number 1 – CMT set number 2	1.5K		
x0001,0600	Sequence set number 1 – CMT set number 3	1.5K		
x0001,0C00	Sequence set number 1 – CMT set number 4	1.5K		
x0001,1200	Sequence set number 1 – CMT set number 5	1.5K		
x0001,1800	Sequence set number 1 – CMT set number 6	1.5K		
x0001,1E00	Reserved (unavailable)	0.50K		Unavailable
x0001,2000	Sequence set number 2 – sequence	5K		See [8]
x0001,3400	Sequence set number 2 – CMT set number 0	1.5K		
x0001,3A00	Sequence set number 2 – CMT set number 1	1.5K		
x0001,4000	Sequence set number 2 – CMT set number 2	1.5K		
x0001,4600	Sequence set number 2 – CMT set number 3	1.5K		
x0001,4C00	Sequence set number 2 – CMT set number 4	1.5K		
x0001,5200	Sequence set number 2 – CMT set number 5	1.5K		
x0001,5800	Sequence set number 2 – CMT set number 6	1.5K		
x0001,5E00	Reserved (unavailable)	0.50K		Unavailable
x0001,6000	Sequence set number 3 – sequence	5K		See [8]
x0001,7400	Sequence set number 3 – CMT set number 0	1.5K		
x0001,7A00	Sequence set number 3 – CMT set number 1	1.5K		
x0001,8000	Sequence set number 3 – CMT set number 2	1.5K		
x0001,8600	Sequence set number 3 – CMT set number 3	1.5K		
x0001,8C00	Sequence set number 3 – CMT set number 4	1.5K		
x0001,9200	Sequence set number 3 – CMT set number 5	1.5K		
x0001,9800	Sequence set number 3 – CMT set number 6	1.5K		
x0001,9E00	Reserved (unavailable)	.50K		Unavailable

Table 25. 4M-bit Address Map [1] [7] (continued)

Starting Address	Data located at this address	Size (Bytes)	Required	Notes
x0001,A000	Sequence set number 4 – sequence	5K		See [8]
x0001,B400	Sequence set number 4 – CMT set number 0	1.5K		
x0001,BA00	Sequence set number 4 – CMT set number 1	1.5K		
x0001,C000	Sequence set number 4 – CMT set number 2	1.5K		
x0001,C600	Sequence set number 4 – CMT set number 3	1.5K		
x0001,CC00	Sequence set number 4 – CMT set number 4	1.5K		
x0001,D200	Sequence set number 4 – CMT set number 5	1.5K		
x0001,D800	Sequence set number 4 – CMT set number 6	1.5K		
x0001,DE00	Reserved (unavailable)	.50K		Unavailable
x0001,E000	Sequence set number 5 – sequence	5K		See [8]
x0001,F400	Sequence set number 5 – CMT set number 0	1.5K		
x0001,FA00	Sequence set number 5 – CMT set number 1	1.5K		
x0002,0000	Sequence set number 5 – CMT set number 2	1.5K		
x0002,0600	Sequence set number 5 – CMT set number 3	1.5K		
x0002,0C00	Sequence set number 5 – CMT set number 4	1.5K		
x0002,1200	Sequence set number 5 – CMT set number 5	1.5K		
x0002,1800	Sequence set number 5 – CMT set number 6	1.5K		
x0002,1E00	Reserved (unavailable)	.50K		Unavailable
x0002,2000	Sequence set number 6 – sequence	5K		See [8]
x0002,3400	Sequence set number 6 – CMT set number 0	1.5K		
x0002,3A00	Sequence set number 6 – CMT set number 1	1.5K		
x0002,4000	Sequence set number 6 – CMT set number 2	1.5K		
x0002,4600	Sequence set number 6 – CMT set number 3	1.5K		
x0002,4C00	Sequence set number 6 – CMT set number 4	1.5K		
x0002,5200	Sequence set number 6 – CMT set number 5	1.5K		
x0002,5800	Sequence set number 6 – CMT set number 6	1.5K		
x0002,5E00	Reserved (unavailable)	.50K		Unavailable
x0002,6000	Sequence set number 7 – sequence	5K		See [8]
x0002,7400	Sequence set number 7 – CMT set number 0	1.5K		
x0002,7A00	Sequence set number 7 – CMT set number 1	1.5K		
x0002,8000	Sequence set number 7 – CMT set number 2	1.5K		
x0002,8600	Sequence set number 7 – CMT set number 3	1.5K		
x0002,8C00	Sequence set number 7 – CMT set number 4	1.5K		
x0002,9200	Sequence set number 7 – CMT set number 5	1.5K		
x0002,9800	Sequence set number 7 – CMT set number 6	1.5K		
x0002,9E00	Reserved (unavailable)	.50K		Unavailable
x0002,A000	Sequence set number 8 – sequence	5K		See [8]
x0002,B400	Sequence set number 8 – CMT set number 0	1.5K		
x0002,BA00	Sequence set number 8 – CMT set number 1	1.5K		
x0002,C000	Sequence set number 8 – CMT set number 2	1.5K		
x0002,C600	Sequence set number 8 – CMT set number 3	1.5K		
x0002,CC00	Sequence set number 8 – CMT set number 4	1.5K		
x0002,D200	Sequence set number 8 – CMT set number 5	1.5K		
x0002,D800	Sequence set number 8 – CMT set number 6	1.5K		
x0002,DE00	Reserved (unavailable)	.50K		Unavailable

Table 25. 4M-bit Address Map [1] [7] (continued)

Starting Address	Data located at this address	Size (Bytes)	Required	Notes
x0002,E000	Sequence set number 9 – sequence	5K		See [8]
x0002,F400	Sequence set number 9 – CMT set number 0	1.5K		
x0002,FA00	Sequence set number 9 – CMT set number 1	1.5K		
x0003,0000	Sequence set number 9 – CMT set number 2	1.5K		
x0003,0600	Sequence set number 9 – CMT set number 3	1.5K		
x0003,0C00	Sequence set number 9 – CMT set number 4	1.5K		
x0003,1200	Sequence set number 9 – CMT set number 5	1.5K		
x0003,1800	Sequence set number 9 – CMT set number 6	1.5K		
x0003,1E00	Reserved (unavailable)	0.50K		Unavailable
x0003,2000	Sequence set number 10 – sequence	5K		See [8]
x0003,3400	Sequence set number 10 – CMT set number 0	1.5K		
x0003,3A00	Sequence set number 10 – CMT set number 1	1.5K		
x0003,4000	Sequence set number 10 – CMT set number 2	1.5K		
x0003,4600	Sequence set number 10 – CMT set number 3	1.5K		
x0003,4C00	Sequence set number 10 – CMT set number 4	1.5K		
x0003,5200	Sequence set number 10 – CMT set number 5	1.5K		
x0003,5800	Sequence set number 10 – CMT set number 6	1.5K		
x0003,5E00	Reserved (unavailable)	0.50K		Unavailable
x0003,6000	Sequence set number 11 – sequence	5K		See [8]
x0003,7400	Sequence set number 11 – CMT set number 0	1.5K		
x0003,7A00	Sequence set number 11 – CMT set number 1	1.5K		
x0003,8000	Sequence set number 11 – CMT set number 2	1.5K		
x0003,8600	Sequence set number 11 – CMT set number 3	1.5K		
x0003,8C00	Sequence set number 11 – CMT set number 4	1.5K		
x0003,9200	Sequence set number 11 – CMT set number 5	1.5K		
x0003,9800	Sequence set number 11 – CMT set number 6	1.5K		
x0003,9E00	Reserved (unavailable)	0.50K		Unavailable
x0003,A000	Sequence set number 12 – sequence	5K		See [8]
x0003,B400	Sequence set number 12 – CMT set number 0	1.5K		
x0003,BA00	Sequence set number 12 – CMT set number 1	1.5K		
x0003,C000	Sequence set number 12 – CMT set number 2	1.5K		
x0003,C600	Sequence set number 12 – CMT set number 3	1.5K		
x0003,CC00	Sequence set number 12 – CMT set number 4	1.5K		
x0003,D200	Sequence set number 12 – CMT set number 5	1.5K		
x0003,D800	Sequence set number 12 – CMT set number 6	1.5K		
x0003,DE00	Reserved (unavailable)	0.50K		Unavailable
x0003,E000	Sequence set number 13 – sequence	5K		See [8]
x0003,F400	Sequence set number 13 – CMT set number 0	1.5K		
x0003,FA00	Sequence set number 13 – CMT set number 1	1.5K		
x0004,0000	Sequence set number 13 – CMT set number 2	1.5K		
x0004,0600	Sequence set number 13 – CMT set number 3	1.5K		
x0004,0C00	Sequence set number 13 – CMT set number 4	1.5K		
x0004,1200	Sequence set number 13 – CMT set number 5	1.5K		
x0004,1800	Sequence set number 13 – CMT set number 6	1.5K		
x0004,1E00	Reserved (unavailable)	0.50K		Unavailable

Table 25. 4M-bit Address Map [1] [7] (continued)

Starting Address	Data located at this address	Size (Bytes)	Required	Notes
x0004,2000	Sequence set number 14 – sequence	5K		See [8]
x0004,3400	Sequence set number 14 – CMT set number 0	1.5K		
x0004,3A00	Sequence set number 14 – CMT set number 1	1.5K		
x0004,4000	Sequence set number 14 – CMT set number 2	1.5K		
x0004,4600	Sequence set number 14 – CMT set number 3	1.5K		
x0004,4C00	Sequence set number 14 – CMT set number 4	1.5K		
x0004,5200	Sequence set number 14 – CMT set number 5	1.5K		
x0004,5800	Sequence set number 14 – CMT set number 6	1.5K		
x0004,5E00	Reserved (unavailable)	0.50K		Unavailable
x0004,6000	Sequence set number 15 – sequence	5K		See [8]
x0004,7400	Sequence set number 15 – CMT set number 0	1.5K		
x0004,7A00	Sequence set number 15 – CMT set number 1	1.5K		
x0004,8000	Sequence set number 15 – CMT set number 2	1.5K		
x0004,8600	Sequence set number 15 – CMT set number 3	1.5K		
x0004,8C00	Sequence set number 15 – CMT set number 4	1.5K		
x0004,9200	Sequence set number 15 – CMT set number 5	1.5K		
x0004,9800	Sequence set number 15 – CMT set number 6	1.5K		
x0004,9E00	Reserved (unavailable)	0.50K		Unavailable
x0004,A000	Reserved (spare)	8K		Spare
x0004,C000	General OEM data	4K		
x0004,D000	Splash screen number 0	204K	Yes, unless power-up splash is disabled	See [6]

Table 26. 8M-bit Address Map (0-4Mbit is the same as the 4Mbit Map) [1] [7]

Starting Address	Data Located at this Address	Size (Bytes)	Required	Notes
x0008,0000	Splash screen number 1	204K		See [6]
x000B,3000	Splash screen number 2	204K		See [6]
x000E,6000	Reserved (spare)	104K		Spare

Table 27. 16M-bit Address Map (0-8Mbit is the same as the 8Mbit Map) [1] [7]

Starting Address	Data Located at this Address	Size (Bytes)	Required	Notes
x0010,0000	Splash screen number 3	204K		See [6]
x0013,3000	Optical test splash screen	816K		See [6] [9]
x001F,F000	Reserved (spare)	4K		Spare

(1) This address map was created with the assumption that the flash sector size is 4KBytes.

(2) ICP application data defines product and ODM-specific default configuration. It includes pointers to all flash content as well as associated auto-initialization default values. ICP application data is defined by the optical engine manufacturer or design house. This data must be located at address 0 in the flash.

(3) WPC program code is limited to 7.50KB and must be aligned to the END of the two 4KB sectors that are allocated to it.

(4) The WPC product series data block must be aligned to the sector boundary immediately after the WPC program code sectors, and must equal one sector. The WPC program code expects this information to immediately the program code and must be on a sector boundary to facilitate the erase and re-programming of this data without affecting the WPC program code. The data in this block includes: the V/I curve data for the product series LEDs, followed by product series default values for the LED golden ratio data.

(5) The WPC unit calibration data block must be aligned to a sector boundary and must equal one sector. This is to allow for fast factory programming of unit specific LED golden ratio data into this block, and if necessary, to facilitate the erase and re-programming of this data on a “unit-by-unit” basis without effecting any other block. The data for this block is the “final” LED golden ratio data after the completion of the LED calibration process. In addition to the actual data, the first four bytes of the block provide a software cue to indicate whether these values have been programmed or not. If not programmed, WPC

software uses default LED golden ratio data.

(6) Additional size is reserved to make alignment simpler.

(7) The white and gray shading in the table is used to keep information lined up in flash block increments.

(8) A sequence set is defined to be the DLP® display sequence plus all associated CMT tables compatible with the sequence. Each CMT table essentially represents a different gamma curve for the corresponding sequence. Each sequence set must be generated with the same number of valid CMT table options and each CMT option, as identified by number, must correspond to the same gamma curve attributes. This default flash table supports up to 7 valid CMT tables per sequence; however, 7 CMT tables are not necessarily populated. The number of populated CMT table options is defined in the ICP APPLICATION DATA region. All parts of a sequence set must be contained in sequence unique sectors to allow for updating of individual sequence sets.

(9) Four splash screens (example: 4 through 7 – each located on a 204 KByte boundary) or an optical test splash screen can be stored in this space.

(10) Note that the BNM table is DMD-dependent, and thus, the appropriate table must be loaded.

(11) Thermistor LUT data is thermistor-device dependent.

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