

User's Guide SBVU024–October 2014

TLV73312PDQN-643 Evaluation Module



This user's guide describes the operational use of the TLV73312PDQN-643 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the <u>TLV73312PDQN</u>, an ultra-small, low-quiescent current, low-dropout regulator (LDO). Included in this user's guide are setup instructions, a schematic diagram, printed circuit board (PCB) layout drawings, and a bill of materials for the EVM.

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Introduction

1 Introduction

The Texas Instruments TLV73312PDQN-643 EVM helps design engineers evaluate the operation and performance of the TLV733 series of LDOs for possible use in their own circuit applications. This particular EVM configuration contains the TLV73312PDQN LDO configured with a single 1-µF input capacitor and no output capacitor. The TLV733 series are ultra-small, low quiescent current LDOs capable of operating capacitor-free with good load and line transient performance in a 4-pin DQN (X2SON) package. This document describes the configuration and setup of the TLV73312PDQN-643 EVM board.

2 Hardware

This section describes the connectors on the EVM, as well as how to properly connect, set up, and use the TLV73312PDQN-643.

2.1 Input and Output Connectors

2.1.1 J1—ON, EN, OFF

J1 allows a jumper to connect the enable pin (pin 2 of J1) to VIN (pin 3 of J1) or to GND (pin 1 of J1). The board is shipped with the jumper connecting the EN pin to GND, and must be moved to connect the enable pin to VIN for normal regulation.

2.1.2 J2—VIN

Connect the input power supply (1.4 V to 5.5 V) positive terminal to J2. Two pins are provided to allow space for multiple connections.

2.1.3 J3—VOUT

Connect the output load positive terminal to J3. Two pins are provided to allow space for multiple connections.

2.1.4 J4—GND

Connect the output load negative terminal to J4. Two pins are provided to allow space for multiple connections.

2.1.5 J5—GND

Connect the input supply negative terminal to J5. Two pins are provided to allow space for multiple connections.

2.1.6 VIN_S

VIN_S allows for a Kelvin measurement directly to the IN pin of the TLV73312PDQN. Use this test post for voltage measurements to a high-impedance digital voltmeter (DVM).

2.1.7 VOUT_S

VOUT_S allows for a Kelvin measurement directly to the OUT pin of the TLV73312PDQN. Use this test post for voltage measurements to a high-impedance DVM.

2.1.8 GND_S

GND_S allows for a Kelvin measurement directly to the GND pin of the TLV73312PDQN. Use this test post for the negative connection of the VIN_S and VOUT_S DVM measurements.

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2.2 Components

2.2.1 C1

C1 is the input capacitor for the TLV73312PDQN but is not necessary for stability. However, C1 can help the device output transient response when the impedance between the input supply and the LDO is inductive. An input capacitor of 1 μ F is recommended for applications where the input impedance is unknown.

2.2.2 C2

C2 is the output capacitor and is not populated on this board. If improved transient response is required, a ceramic capacitor of any value less than or equal to 100 μ F can be populated for C2. A 1- μ F capacitor is a good choice for a balance of size and cost versus transient performance.

2.2.3 R1

R1 allows for a resistor to connect the EN pin to the VIN voltage. The EN pin must be pulled above 0.9 V to enable the device. If a resistive connection to VIN is necessary (in the case that an external open-drain enable signal is used), R1 can be populated with an appropriate pull-up resistor. If a direct short to VIN is desired, the jumper provided on J1 can be used to short EN to VIN.

3 Setup and Test

- Set the input power-supply voltage to 0 V. Connect the positive voltage lead from the power supply to J2 (VIN). Connect the ground lead from the power supply to J5 (GND).
- Short EN to VIN by connecting the jumper on J1 to the header pins marked ON and EN.
- Connect a voltmeter across VOUT_S and GND_S.
- Add the required load from J3 (VOUT) to J4 (GND).
- Vary the input power-supply voltage as necessary for test purposes.

4 Operation

The TLV73312PDQN is a fixed 1.2-V LDO. The device is designed to operate with 1.4 V \leq VIN \leq 5.5 V, and 0 \leq IOUT \leq 300 mA.

TEXAS INSTRUMENTS

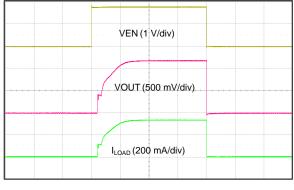
Test Results

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5 Test Results

5.1 Startup Performance

Figure 1 shows the startup performance of the TLV73312PDQN-643 EVM.

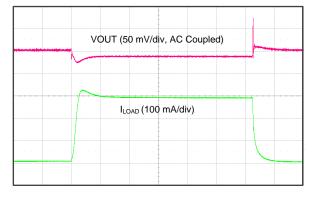


Time (200 µs/div)

Figure 1. Startup Performance with a 3.7- Ω Load Resistor, VIN = 1.8 V

5.2 Load Transient Performance

Figure 2 shows the load transient performance of the TLV73312PDQN-643 EVM.



Time (100 µs/div)

Figure 2. Load Transient Response, 0 mA to 300 mA, VIN = 1.8 V, VEN = VIN



6 Thermal Guidelines and Layout Recommendations

Thermal management is a key design component of any power converter and is especially important when the power dissipation in the LDO is high. Use Equation 1 to approximate the maximum power dissipation for the particular ambient temperature:

 $T_{_J} = T_{_A} + P_{_D} \times \theta_{_{JA}}$

where

- T_J is the junction temperature,
- T_A is the ambient temperature,
- P_D is the power dissipation in the device (Watts),
- and θ_{JA} is the thermal resistance from junction to ambient.
- All temperatures are in degrees Celsius.

(1)

The maximum operating junction temperature, T_J , must not to exceed 125°C. The layout must use copper traces and planes as thermal sinks in order to keep T_J below the maximum operating temperature during worst-case conditions.

Table 1 includes information from the Dissipation Ratings Table of the <u>TLV733 series data sheet</u> for comparison with the thermal resistance, θ_{JA} , for High-K JEDEC standard boards. The maximum input voltage can be calculated for full load at different ambient temperatures. The input voltage must be less than these values in order to maintain a safe junction temperature.

Table 1. Thermal Resistance, θ_{JA} , and Maximum Power Dissipation

IC	Board	Package	θ _{JA}	Max VIN at 300 mA $(T_A = 25^{\circ}C)$	Max VIN at 300 mA (T _A = 70°C)
TLV73312	High-K	DQN	218.6°C/W	2.724 V	2.03 V

7 Board Layout

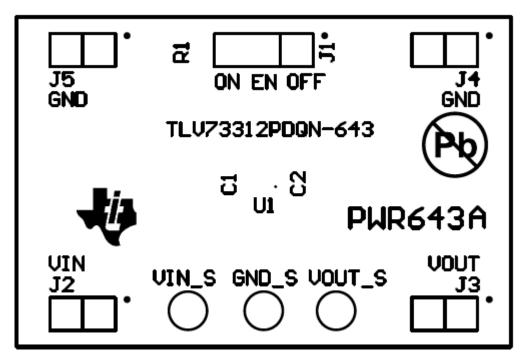


Figure 3. Top Silk Screen

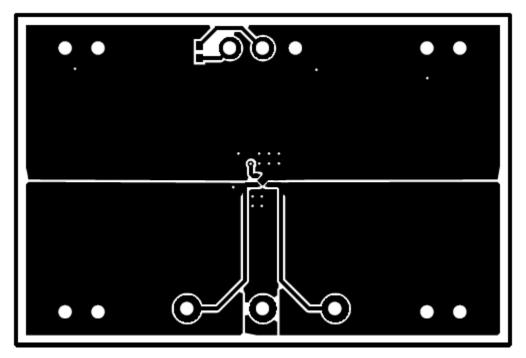


Figure 4. Top Layer Routing



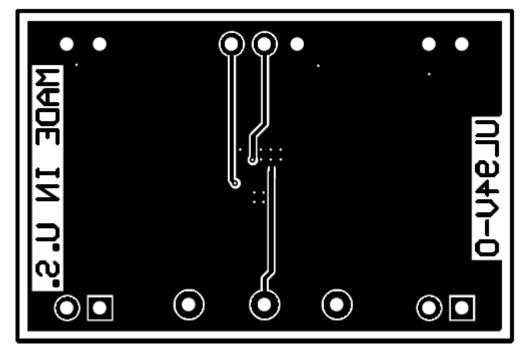


Figure 5. Bottom Layer Routing

8 Schematic

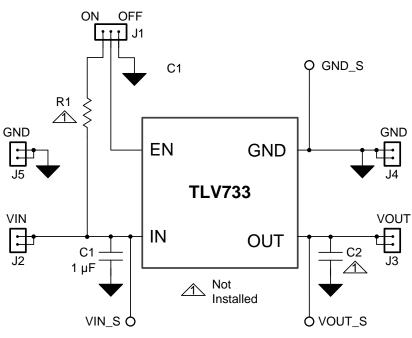


Figure 6. TLV73312PDQN-643 Schematic



Bill of Materials

9 Bill of Materials

Qty	Designator	Value	Description	Size	Part Number	Manufacturer
1	C1	1 uF	CAP, CERM, 1uF, 6.3V, +/-20%, X5R, 0402	0402	SC1005X5R0J105M	ток
0	C2	1 uF	CAP, CERM, 1uF, 6.3V, +/-20%, X5R, 0402	0402	SC1005X5R0J105M	ток
0	R1	10 kΩ	RES, 10.0k ohm, 1%, 0.063W, 0402	0402	CRCW040210K0FKED	Vishay-Dale
1	J1	3 x 1	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	100 mil.	TSW-103-07-G-S	Samtec
4	J2, J3, J4, J5	2 x 1	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	100 mil.	TSW-102-07-G-S	Samtec
1	SH-J1	1 x 2	Shunt, 100mil, Gold plated, Black	Shunt	SPC02SYAN	Sullins
1	U1 ⁽⁴⁾	_	IC, Capacitor-Free, 300-mA, Low- Dropout Regulator with Foldback Current Limit for Portable Devices	1x1 SON	TLV73312PDQN	ті
1	_	_	PCB, 1.0 in x 1.5 in x 0.062 in	1.00 in x 1.50 in x 0.062 in	PWR643	Any

Table 2. TLV73312PDQN-643 Bill of Materials⁽¹⁾⁽²⁾⁽³⁾

⁽¹⁾ These assemblies are electrostatic-discharge (ESD) sensitive; observe ESD precautions.

⁽²⁾ These assemblies must be clean and free from flux and all contaminants. Do not use no-clean flux.

⁽³⁾ These assemblies must comply with workmanship standards IPC-A-610 Class 2.

⁽⁴⁾ Cannot be substituted. All other components can be substituted with equivalent manufacturer components.

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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
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