The Texas Instruments TSW308x evaluation module (EVM) provides a basic platform to evaluate the DAC348x in a complete RF transmit signal chain. Along with the DAC348x, the EVM includes a LMK04806B clock jitter cleaner and generator source, which provides the clocks required for the DAC and the external pattern generator. The EVM also includes on-board TRF3705 I/Q modulators, which provide IF-to-RF upconversion for basic transmitter evaluation. This EVM is ideally suited for mating with the Texas Instruments TSW1400 pattern generation board for evaluating WCDMA, LTE, or other high-performance modulation schemes.
1 Introduction

1.1 Overview

The TSW308x evaluation module (EVM) is a family of circuit boards that allow designers to evaluate the performance of the Texas Instruments DAC348x digital-to-analog converters (DAC). The DAC348x family consists of DAC3482, DAC3484, and DAC34H84. The 16-bit, 1.25 GSPS, DAC348x has integrated 2x/4x/8x/16x interpolation filters, 32-bit NCO, on-chip PLL, and exceptional linearity at high IFs. The EVM provides a flexible environment to test the DAC348x under a variety of clock, data input, and RF output conditions. For ease of use as a complete RF transmit solution, the TSW308x EVM includes the LMK04806B low-noise, clock generator/jitter cleaner for clocking the DAC348x. Besides providing a high-quality, low jitter DAC sampling clock to the DAC348x, the LMK04806B also provides FPGA clocks to the TSW1400EVM (or TSW3100EVM) as FPGA reference clocks.

The TSW3085 (populated with DAC3482) has one pair of I/Q channel and is designed as a single RF channel transmit solution, while the TSW3084 (populated with DAC3484) and TSW30H84 (populated with DAC34H84) have two pairs of I/Q channel and are designed for dual RF channels transmit solution. Both the TSW3085 and TSW30H84 can accept up to 625MSPS of input data rate for each I or Q channel. The TSW3084 can be considered as a lower bus width alternative for the dual RF channel while accepting up to 312.5MSPS of input data rate.

Each transmit channel of the TSW308x has the TRF3705 quadrature modulator, which follows immediately after the DAC348x as part of the signal chain. Its output ranging from 300 MHz to 4 GHz, to up-convert the I/Q outputs from the DAC to RF. The default RF signal paths is the direct TRF3705 I/Q modulator output. To add flexibility to the RF evaluation, the modulator outputs can also connect to the optional RF amplifier and programmable attenuator path to meet additional test conditions and requirements.

The EVM can be used along with TSW1400 or TSW3100 to perform a wide varieties of test and measurement. This board is also compatible with Altera® and Xilinx® FPGA development platforms for rapid evaluation and prototyping. The on-board HSMC connector input allows direct connection to the HSMC compatible Altera development platforms, and the externally attached FMC-DAC-Adapter board available from TI enables the connection of the EVM to the Xilinx development platforms with FMC headers.

Other DAC348x families can be evaluated on different EVM platforms. For details of the DAC348x family and the corresponding EVM part number, see Table 1.

Table 1. DAC348x Family

<table>
<thead>
<tr>
<th>DAC Part No.</th>
<th>DAC3484</th>
<th>DAC3482</th>
<th>DAC34H84</th>
<th>DAC34SH84</th>
</tr>
</thead>
<tbody>
<tr>
<td>EVM Part No.</td>
<td>TSW3084EVM</td>
<td>TSW3085EVM</td>
<td>TSW30H84EVM</td>
<td>TSW30SH84EVM</td>
</tr>
<tr>
<td>Output Channels</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Maximum DAC Rate</td>
<td>1.25 GSPS</td>
<td>1.25 GSPS</td>
<td>1.25 GSPS</td>
<td>1.5 GSPS</td>
</tr>
<tr>
<td>Digital Interface</td>
<td>16-Bit LVDS Interface</td>
<td>16-Bit LVDS Interface</td>
<td>32-Bit LVDS Interface</td>
<td>32-Bit LVDS Interface</td>
</tr>
<tr>
<td>Maximum Data Rate per Channel</td>
<td>312.5 MSPS</td>
<td>625 MSPS</td>
<td>625 MSPS</td>
<td>750 MSPS</td>
</tr>
<tr>
<td>Maximum LVDS Bus Toggle Rate</td>
<td>1.25 GSPS</td>
<td>1.25 GSPS</td>
<td>1.25 GSPS</td>
<td>1.5 GSPS</td>
</tr>
<tr>
<td>Pattern Generator Support</td>
<td>TSW1400/TSW3100</td>
<td>TSW1400/TSW3100</td>
<td>TSW1400/TSW3100</td>
<td>TSW1400/TSW3100 with limited data rate support</td>
</tr>
</tbody>
</table>

See the DAC348x EVM web folders at:
http://www.ti.com/tool/dac3482evm
http://www.ti.com/tool/dac3484evm
http://www.ti.com/tool/dac34h84evm
http://www.ti.com/tool/dac34sh84evm

For evaluation of the DAC348x family with transformer coupled IF output, see the DAC348xEVM user’s guide (SLAU432).

For evaluation of the TSW30SH84 with the on-board DAC34SH84, see the TSW30SH84EVM user’s guide (SLAU433).
### 1.2 EVM Block Diagram

Figure 1 shows the TSW3084EVM block diagram, Figure 2 shows the TSW3085EVM block diagram, and Figure 3 shows the TSW30H84EVM block diagram.
**Figure 2. TSW3085EVM Block Diagram**
Figure 3. TSW30H84EVM Block Diagram
2 Software Control

2.1 Installation Instructions

Perform the following steps to install the software.

1. Open the folder named TSW308x_Installer_vxpx (xpx represents the latest version).
2. Run Setup.exe.
3. Follow the onscreen instructions.
4. Once installed, launch the program by clicking on the TSW308x program in Start>Programs>Texas Instruments DACs>TSW308x. For Windows XP system, the installation directory is located at C:\Program Files\Texas Instruments\TSW308x. For Windows 7 system, it is located at C:\Program Files (x86)\Texas Instruments\TSW308x
5. When plugging in the USB cable for the first time, you are prompted to install the USB drivers.
   (a) When a pop-up screen opens, select Continue Downloading.
   (b) Follow the onscreen instructions to install the USB drivers.
   (c) If needed, the drivers can be accessed directly in the install directory.

2.2 Software Operation

The software allows programming control of the DAC, the LMK, and the attenuator devices. The front panel provides a tab for full programming of each device. The GUI tabs provide a more convenient and simplified interface to the most used registers of each device.

Each device has its own custom control interface. At the top level of the GUI are five control tabs. The first four are used to configure the DAC348x and the last for the LMK04800. The attenuator control window on the right side of the GUI is used to program the attenuator.
2.2.1 Input Tab Control Options

Figure 4. Input Tab Control Options – DAC348x

- FIFO: allows the configuration of the FIFO and FIFO synchronization (sync) sources.
- LVDS delay: provides internal delay of either the LVDS DATA or LVDS DATACLK to help meet the input setup/hold time.
- Data Routing: provides flexible routing of the A, B, C, and D sample input data to the appropriate digital path. Note: the DAC3482 does not support this mode.
- SIF Control: provides control of the Serial Interface (3-wire or 4-wire) and Serial Interface Sync (SIF Sync).
- Input Format: provides control of the input data format (that is, 2’s complement or offset binary).
- Parity: provides configuration of the parity input.
- PLL Settings: provides configuration of the on-chip PLL circuitry.
- Temperature Sensor: provides temperature monitoring of DAC348x die temperature.

2.2.1.1 FIFO Settings

The DAC348x has 8-samples deep FIFO to relax the timing requirement of a typical transmitter system. The FIFO has an input pointer and an output pointer, and both pointers can accept various input sources as reset triggers of input and output pointer position. One important application for input and output pointer control is the ability to synchronize multiple DACs in the system. For additional information, see the relevant DAC348x data sheet.

- FIFO Offset: The default position of FIFO output pointer after reset by the synchronization source. This setting can be used to change the latency of the DAC348x.
- Data Formatter Sync (DAC3482 and DAC3484): Synchronization source for FIFO data formatter. Select between LVDS FRAME or LVDS SYNC signals.
• FIFO Sync Select (DAC34H84 and DAC34SH84): Select the internal digital routing of LVDS ISTR or LVDS SYNC to the FIFO ISTR path
• FIFO Input Sync: Synchronization source for FIFO input pointer. Select among the LVDS FRAME (ISTR), LVDS SYNC, and/or SPI register SIF-SYNC to reset the FIFO input pointer position.
• FIFO Output Sync: Synchronization source for FIFO output pointer. Select among the LVDS FRAME (ISTR), LVDS SYNC, SPI register SIF-SYNC, and/or OSTR signal to reset the FIFO output pointer position.
  – For single device application without the need for precise latency control, Single Sync Source Mode may be used. The FIFO output pointer position can be reset with LVDS FRAME (ISTR), LVDS SYNC, and/or SPI register SIF-SYNC. See the Single Sync Source Mode in the relevant DAC348x data sheet for details.
  – For multiple device synchronization, select the OSTR signal as the FIFO output synchronization source. If the DAC is configured to accept external DAC Clock input, then the OSTR signal is the external LVPECL signal to the OSTRP/N pins. If the DAC is configured to accept the internal on-chip PLL clock, then the OSTR signal is the internally generated PFD frequency. See the Dual Sync Sources Mode in the relevant DAC348x data sheet for details.

2.2.1.2 LVDS Delay Settings

Depending on the signal source implementation (that is, TSW1400, TSW3100, or FGPA system), the following options can be implemented to meet the minimum setup and hold time of DAC348x data latching:
• Set the on-chip LVDS DATACLK delay: The DAC348x includes on-chip LVDS DATA or DATACLK delay. The delay ranges from 0 ps to 280 ps with an approximate 40-ps step. This LVDS DATACLK delay does not account for additional PCB trace-to-trace delay variation, only the internal DATACLK delay. The TSW1400 and TSW3100 pattern generators send out LVDS DATA and DATACLK as edge-aligned signal. Typical setting of 160 ps or more help meet the timing requirement for most of the pattern generator and DAC348x EVM setup.
• Modify the external LVDS DATACLK PCB trace delay: Additional trace length can be added to the DATACLK P&N PCB trace length.
  – At the top side of the TSW3084, set SJP9, SJP10, SJP11, and SJP12 to the 2-3 position for approximately 2 inches (320 ps) of trace delay.
  – At the top side of the TSW3085, set SJP1, SJP6, SJP7, and SJP8 to the 2-3 position for approximately 2 inches (320 ps) of trace delay.
  – At the top side of the TSW30H84, set SJP9, SJP10, SJP11, and SJP12 to the 2-3 position for approximately 1 inches (160 ps) of trace delay.

2.2.1.3 PLL Settings

![ PLL Settings Diagram ]

Figure 5. PLL Configuration
Perform the following steps to configure the PLL.

1. Enable PLL.
2. Uncheck PLL reset and PLL sleep.
3. Set \( M \) and \( N \) ratio such that \( F_{DAC} = \frac{M}{N} \times F_{ref} \).
4. For the DAC3482, DAC3484, and DAC34H84, set the prescaler such that the \( F_{DAC} \times \) prescaler is within 3.3 GHz and 4 GHz.
5. For the DAC34SH84, set the prescaler such that the \( F_{DAC} \times \) prescaler is within 2.7 GHz and 3.3 GHz.
6. Set VCO Bias Tune to 1.
7. Charge Pump setting
   a. If stability \((P \times M)\) is less than 120, then set to Single.
   b. If stability \((P \times M)\) is greater than 120, then set to Double or install external loop filter.
8. Adjust the Freq. Tune (Coarse) accordingly. For additional information, see the relevant DAC348x data sheet.

2.2.2 Digital Tab Control Options

- Interpolation: allows control of the data rate versus DAC sampling rate ratio (that is, data rate \( \times \) interpolation = DAC sampling rate).
- Digital Mixer: allows control of the coarse mixer function.
  Note: If fine mixer (NCO) is used, the Enable Mixer button must be checked, and the coarse mixer must be bypassed. See the following NCO bullet for detail.
- Inverse sinx/x filter: allows compensation of the sinx/x attenuation of the DAC output.
  **Note:** If inverse sinx/x filter is used, the input data digital full-scale must be backed off accordingly to avoid digital saturation.
- Clock Receiver Sleep: allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- Clock Divider Sync: allows the synchronization of the internal divided-down clocks using either Frame, Sync, or OSTR signal. Enables the divider sync as part of the initialization procedure or resynchronization procedure.
- Group Delay: allows adjustment of group delay for each I/Q channel. This is useful for wideband sideband suppression. **Note:** This feature is not available for the DAC34SH84.
- Offset Adjustment: allows adjustment of dc offset to minimize the LO feedthrough of the modulator output. This section requires synchronization for proper operation. The synchronization options follow:
  - **REGWR:** auto-sync from SIF register write. If this option is chosen, the GUI automatically synchronizes the offset adjustment with each value update by writing to 0x08 (Offset A) or 0x0A (Offset C) registers last.
  - **OSTR:** sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source.
  - **SYNC:** sync from the external LVDS SYNC signal.
  - **SIF SYNC:** sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.
- QMC Adjustment: allows adjustment of the gain and phase of the I/Q channel to minimize sideband power of the modulator output.
  - **REGWR:** auto-sync from SIF register write. If this option is chosen, the GUI automatically synchronizes the offset adjustment with each value update by writing to 0x10 (QMC PhaseAB) or 0x11 (QMC PhaseCD) registers last.
  - **OSTR:** sync from the external LVPECL OSTR signal. Clock Divider Sync must be enabled with OSTR set as sync source.
  - **SYNC:** sync from the external LVDS SYNC signal.
  - **SIF SYNC:** sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.
- NCO: allows fine mixing of the I/Q signal. The procedure to adjust the NCO mixing frequency follows.
  1. Enter the DAC sampling frequency in Fsample.
  2. Enter the desired mixing frequency in both NCO freq_AB and NCO freq_CD.
  3. Press Update freq.
  4. Synchronize the NCO block from the following options.
    - **REGWR:** auto-sync from SIF register write. Writing to either Phase OffsetAB or Phase OffsetCD can create a sync event.
    - **OSTR:** sync from the external LVPECL OSTR signal. Clock Divider Sync must be enabled with OSTR set as sync source. See the data sheet for OSTR period requirement.
    - **SYNC:** sync from the external SYNC signal.
    - **SIF SYNC:** sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.
2.2.3 Output Tab Control Options

- **Output Options**: allows the configuration of reference, output polarity, and output delay.
- **Data Routing**: provides flexible routing of the A, B, C, and D digital path to the desired output channels. **Note**: The DAC3482 does not support this mode.
- **DAC Gain**: configures the full-scale DAC current and DAC3484/DAC3482 mode. With $R_{bias}$ resistor set at $1.28 \, \text{k}\Omega$:
  - DAC Gain = 15 for 30-mA, full-scale current.
  - DAC Gain = 10 for 20-mA, full-scale current (default).
- **Output Shutoff On**: allows outputs to shut off when DACCLK GONE, DATACLK GONE, or FIFO COLLISION alarm event occurs.

![Figure 7. Output Tab Control Options – DAC348x](image-url)
2.2.4 LMK04800

Figure 8. LMK04800 Tab Control Options

Clock control is determined by register values in the LMK04800 Control tab. The LMK04800 has 12 available output clocks. See the LMK04800 family data sheet for detailed explanations of the register configurations.

The following LMK04806 outputs are used by the TSW3084EVM:

- **CLK3**: DAC3484 DAC sampling clock. This clock type is AC coupled LVPECL. If the DAC3484 is configured for internal PLL mode, this becomes the reference clock input for the PLL block.
- **CLK8**: TSW1400/TSW3100 FPGA input clock. This clock type is AC coupled LVDS. The clock rate must be set to $F_{DAC/interpolation}/2$.
- **CLK4**: DAC3484 FIFO OSTR Clock. This clock type is AC coupled LVPECL.
  - The OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - The OSTR clock rate must be at most $F_{DAC/interpolation}/8$. See the DAC348x data sheet for more detail.
  - The FIFO OSTR clock must be disabled when the DAC348x is using the on-chip PLL for DACCLK generation.
- **CLK6**: Spare output clock at SMA J5.
- **CLK0**: Spare output clock at SMA J2 and J3.

The following LMK04806 outputs are used by the TSW3085EVM:

- **CLK3**: DAC3482 DAC sampling clock. This clock type is AC coupled LVPECL. If the DAC3482 is configured for internal PLL mode, this becomes the reference clock input for the PLL block.
- **CLK8**: TSW1400/TSW3100 FPGA input clock. This clock type is AC coupled LVDS. The clock rate
must be set to $F_{\text{DAC}}/$interpolation$/4$.

- **CLK4**: DAC3482 FIFO OSTR Clock. This clock type is AC coupled LVPECL.
  - The OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - The OSTR clock rate must be at most $F_{\text{DAC}}$/interpolation$/16$ for word-wide interface and $F_{\text{DAC}}$/interpolation$/8$ for byte-wide interface. See the DAC348x data sheet for more detail.
  - The FIFO OSTR clock must be disabled when the DAC348x is using the on-chip PLL for DACCLK generation.
- **CLK6**: Spare output clock at SMA J5.
- **CLK0**: Spare output clock at SMA J2 and J3.

The following LMK04806 outputs are used by the TSW30H84EVM:

- **CLK4**: DAC34H84 DAC sampling clock. This clock type is AC coupled LVPECL. If the DAC34H84 is configured for internal PLL mode, this becomes the reference clock input for the PLL block.
- **CLK8**: TSW1400/TSW3100 FPGA input clock (#1). This clock type is AC coupled LVDS. The clock rate must be set to $F_{\text{DAC}}$/interpolation$/4$.
- **CLK9**: TSW1400 FPGA input clock (#2). This clock type is AC coupled LVDS. It is required to evaluate the TSW30H84 and TSW30SH84 with the TSW1400. The clock rate must be set to $F_{\text{DAC}}$/interpolation$/4$.
- **CLK3**: DAC34H84 FIFO OSTR Clock. This clock type is AC coupled LVPECL.
  - The OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - The OSTR clock rate must be at most $F_{\text{DAC}}$/interpolation$/8$. See the DAC34H84 data sheet for more detail.
  - The FIFO OSTR clock must be disabled when the DAC348x is using the on-chip PLL for DACCLK generation.
- **CLK6**: Spare output clock at SMA J5.
- **CLK0**: Spare output clock at SMA J2 and J3.

The clock settings are divided into subcontrol sections. These sections allow the user to set the divide ratio, digital delay, type, analog delay, and ON/OFF control. Note that clock pairs share several settings.

The OSCout control section allows the user to configure the settings for the OSCIN input. The TSW308xEVM uses this input as the reference input for Single Loop mode of operation (default configuration). This mode uses PLL2 of the device. This reference can be provided by either the onboard 10-MHz oscillator (default) or from an external source brought in through SMA J11. For details, see Section 5.

The PLL2 Settings control section allows the user to configure the settings for the internal PLL2. The LMK04800 family contains four devices that cover internal VCO frequencies from 1840 MHz to 3072 MHz. The VCO range of the LMK04806B is 2370 MHz to 2600 MHz. The TSW308xEVM default test case uses settings to set the internal VCO to 2457.6 MHz and is locked to the 10-MHz input source on OSCIN.

The default Single Loop PLL settings provided by the example file provide a 1228.8 MHz of DAC sampling clock, the divided-down FPGA clock(s) for the TSW1400/TSW3100 pattern generator FPGA input clock, and the divided-down OSTR clock for DAC348x's OSTR input. The CLK6 (J5) is configured as a divided-by-100 CMOS clock. This can be used as part of EVM functionality verification. For details, see Section 4.5.

After the default settings are loaded, the output clocks are synchronized with the onboard 10-MHz reference oscillator as indicated by LMK LOCK LED (D7) being illuminated.

Clicking on the Advance Settings tab at the bottom of the GUI opens a new window allowing the user to set other internal registers for different modes of operation as shown in Figure 9.
Figure 9. LMK04800 Advanced Settings Control Panel
2.2.5 Register Control

- Send All: sends the register configuration to all devices.
- Read All: reads register configuration from DAC348x and LMK04800 devices.
- Load Regs: loads a register file for all devices. For Windows XP system, example configuration files for the common frequency plan are located in the install directory: C:\Program Files\Texas Instruments\TSW308x\Configuration Files. For Windows 7 system, the files are located in the install directory: C:\Program Files (x86)\Texas Instruments\TSW308x\Configuration Files
  - Select Load Regs button.
  - Double-click on the Configuration Files folder and respective sub-folders for the EVM.
  - Double-click on the desired register file.
  - Click on Send All to ensure all the values are loaded properly.
- Save Regs: saves the register configuration for all devices.

2.2.6 Attenuator Control

![Figure 10. RF Attenuator Control](image)

Each of the RF path on the TSW308xEVM contains a 50-Ω, RF digitally controlled attenuator that operates from DC to 4 GHz. This highly versatile digital step attenuator (DSA) covers a 0-dB to 31.75-dB attenuation range in 0.25-dB steps. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss (1.9 dB, typical) and low-power consumption. The user can enter a value from 0 (minimum attenuation) to 31.75 (maximum attenuation) in 0.25 increments inside the Attenuator window (Figure 10) or by clicking on the drop-up/-down arrows.

2.2.7 Miscellaneous Settings

- Reset USB: toggle this button if the USB port is not responding. This generates a new USB handle address.
  - Note: It is recommended that the board be reset after every power cycle, and the reset USB button on the GUI be clicked.

![Figure 11. USB Port Reset](image)

- Exit: stops the program
3 Basic Test Procedure with TSW1400

This section outlines the basic test procedure for testing the EVM with the TSW1400.

3.1 TSW1400 Overview

The TSW1400 is a high speed data capture and pattern generator board. When functioning as a pattern generator, it has a maximum LVDS bus rate of 1.5 GSPS, and this allows evaluation of the DAC348x and also DAC34SH84 with maximum 750 MSPS of input data rate per channel.

See the TSW1400 user’s guide (SLWU079) for more detailed explanation of the TSW1400 setup and operation. This document assumes that the High Speed Data Converter Pro software (SLWC107) is installed and functioning properly.

3.2 Test Block Diagram for TSW1400

The test setup for general testing of the TSW3084/TSW30H84EVM with the TSW1400 pattern generator card is shown in Figure 12.

---

Figure 12. TSW1400 and TSW3084/TSW30H84 Test Setup Block Diagram

The test setup for general testing of the TSW3085 with the TSW1400 pattern generator is shown in Figure 13.
3.3 Test Setup Connection

**TSW1400 Pattern Generator.**

1. Connect the EVM-supplied 18-AWG wires to the DC plug cable (Tensility 10-01776) to a qualified lab bench power supply. The 18-AWG red wire is the 5-V wire while the 18-AWG black wire is the ground wire.

2. Connect a 5-V power supply cable to J12, the 5V_IN jack of the TSW1400 EVM.

3. Connect PC’s USB port to J5 USB port of the TSW1400 EVM. The cable should be a standard A to mini-B connector cable.

**TSW3084/TSW30H84 EVM**

1. Connect J13 connector of TSW3084/TSW30H84 EVM to J4 connector of TSW1400 EVM.

2. Connect the EVM-supplied 18-AWG wires to the DC plug cable (Tensility 10-01776) to a qualified lab bench power supply. The 18-AWG red wire is the 6-V wire while the 18-AWG black wire is the ground wire.

3. Connect the 6-V power supply cable to the J18, Power In jack of the TSW3084/TSW30H84 EVM.

4. Connect PC’s USB port to J14 USB port of the TSW3084/TSW30H84 EVM. The cable should be a standard A to mini-B connector cable.
5. Provide 10-dBm maximum, 300-MHz to 4-GHz LO source to connectors J19 and/or J22. The J19 or the J22 connector routes the LO source to the respective TRF3705 modulator TX path. Optionally, the EVM can be configured to share the LO source between the two TX paths through an on-board 3 dB splitter. The source should be connected to J22 in this case. See the TX Path Optional Configuration section for details.

6. Connect the RF output port of J7 and/or J9 to the spectrum analyzer.

7. If an external reference is to be used with LMK04806B in single PLL mode, provide a 3.3-Vpp maximum, 140-MHz maximum clock to J11. Change SJP5 solder jumper to position 2-3 to route the external reference source to the LMK04806B OSCIN input.

8. If the LMK04806B is configured in clock distribution mode, provide a 2.4-Vpp maximum, 3.1-GHz maximum clock to J12. The external clock source will route to the LMK04806B CLKin1 input.

**TSW3084/TSW30H84 EVM Jumpers: (make sure the following jumpers are at their default setting)**

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP2</td>
<td>1-2</td>
<td>DAC3484/DAC34H84 TXENABLE</td>
</tr>
<tr>
<td>JP3</td>
<td>2-3</td>
<td>DAC3484/DAC34H84 SLEEP</td>
</tr>
<tr>
<td>JP4</td>
<td>1-2</td>
<td>10-MHz TCXO Enable</td>
</tr>
<tr>
<td>JP12, JP13</td>
<td>2-3</td>
<td>TRF3705 Power Down</td>
</tr>
<tr>
<td>JP14, JP15</td>
<td>2-3</td>
<td>TRF3705 Gain Control</td>
</tr>
<tr>
<td>SJP2</td>
<td>2-3</td>
<td>CPLD EEPROM W/P</td>
</tr>
<tr>
<td>SJP3</td>
<td>1-2</td>
<td>USB Bus Power</td>
</tr>
<tr>
<td>SJP4</td>
<td>1-2</td>
<td>CPLD Clock Select</td>
</tr>
<tr>
<td>SJP5</td>
<td>1-2</td>
<td>Internal/External Reference Select for LMK04806B OSCIN</td>
</tr>
<tr>
<td>SJP9, SJP10, SJP11, SJP12</td>
<td>2-3</td>
<td>DAC3484/DAC34H84 DataCLK delay. Default is zero trace delay.</td>
</tr>
</tbody>
</table>

**TSW3085 EVM**

1. Connect J13 connector of TSW3085 EVM to J4 connector of TSW1400 EVM.
2. Connect the EVM-supplied 18-AWG wires to the DC plug cable (Tensility 10-01776) to a qualified lab bench power supply. The 18-AWG red wire is the 6-V wire while the 18-AWG black wire is the ground wire.
3. Connect the 6-V power supply cable to the J4, Power In jack of the TSW3085 EVM.
4. Connect PC’s USB port to J14 USB port of the TSW3085 EVM. The cable should be a standard A to mini-B connector cable.
5. Provide 10 dBm maximum, 300-MHz to 4-GHz LO source to connectors J1. The J1 connector routes the LO source to the respective TRF3705 modulator TX path.
6. Connect the RF output port of J7 to the spectrum analyzer.
7. If an external reference is to be used with LMK04806B in single PLL mode, provide a 3.3-Vpp maximum, 140 MHz maximum clock to J11. Change SJP5 solder jumper to position 2-3 to route the external reference source to the LMK04806B OSCIN input.
8. If the LMK04806B is configured in clock distribution mode, provide a 2.4-Vpp maximum, 3.1-GHz maximum clock to J12. The external clock source will route to the LMK04806B CLKin1 input.
3.4 **TSW308x Example Setup Procedure**

1. Turn on power to both boards, and press the reset button SW1 on the TSW308xEVM.
2. Start the TSW308x EVM GUI program. When the program starts, press the **RESET USB Port** button in the GUI, and verify USB communication.
3. Select the appropriate EVM platform on the software menu.

![TSW308x_v2p1.vi](image)

**Figure 14. EVM Platform Selection**

4. Click on **LOAD REGS**, browse to the installation folder, and load example files. The example files are located at `C:\Program Files\Texas Instruments\TSW308x\Configuration Files`. To configure the LMK04806B in single PLL mode, select the file in the LMK04806 PLL Mode 10-MHz reference folder. To configure the LMK04806B in clock distribution mode, select the file in the **LMK04806 Clock Distribution Mode** folder.

   - For the TSW3084, the files contain settings for 4x interpolation with the DAC3484 running at 1228.8 MSPS. The data rate for each DAC is at 307.2 MSPS. The NCO is enabled at 30 MHz.
   - For the TSW30H84, the files contain settings for 2x interpolation with the DAC34H84 running at 1228.8 MSPS. The data rate for each DAC is at 614.4 MSPS. The NCO is enabled at 30 MHz.
   - For the TSW3085, the files contain settings for 2x interpolation with the DAC3482 running at 1228.8 MSPS. The data rate for each DAC is at 614.4 MSPS. The NCO is enabled at 30 MHz.

5. Click on **Send All** to write all of the values to the devices. If the LMK04806B is programmed properly in single PLL mode, the **LMK LOCK** LED (D7) near the device illuminates. The updated register configuration for the LMK04806B now appears as shown in **Figure 8**.
6. Note: J5 (CLK6) is configured as a divide-by-100 CMOS clock. This is used to verify EVM functionality.
**TSW1400 Example Setup Procedure**

1. Start the High Speed Converter Pro GUI program. When the program starts, select the DAC tab and then select appropriate device in the “Select DAC” menu.

![Select DAC348x Family in the High Speed Converter Pro GUI Program](image1)

2. When prompted *Do you want to update the firmware for DAC?*, select **YES**.

![Load DAC Firmware Prompt](image2)

3. Click on the button labeled “Load File to transfer into TSW1400”, located near the top left of the GUI.
4. For the TSW3084, select the file "WCDMA_TM1_complexIF30MHz_Fdata307.2MHz_1000.tsw" under C:\Program Files\Texas Instruments\High Speed Data Converter Pro\1400 Details\Testfiles.

5. For the TSW30H84 and TSW3085, select the file "WCDMA_TM1_complexIF30MHz_Fdata614.4MHz_1000.tsw" under C:\Program Files\Texas Instruments\High Speed Data Converter Pro\1400 Details\Testfiles.

6. Enter 307.2M or 614.4M for the "Data Rate" and 2's complement for the "DAC Option".

7. Select Hanning for "Window".

8. In the "DAC Selection" panel on the left side of the GUI, click on "Send" to load the data into memory.

9. **Toggle the SIF SYNC button of the TSW308x EVM GUI to synchronize the appropriate digital blocks, if the example file with NCO setting is used.**

10. Verify the spectrum using the spectrum analyzer at the RF output port(s), J7 or J9.

11. With 1780 MHz of LO, the expect results are shown in Figure 18 (TRF3705 Low-Gain Mode) and Figure 19 (TRF3705 High-Gain Mode).
NOTE: Baseband = 30 MHz, NCO = 30 MHz with NCO Gain disabled, QMC Gain = 1446, LO = 1780 MHz

**Figure 18. TSW308x WCDMA Output (TRF3705 Low-Gain Mode)**

<table>
<thead>
<tr>
<th>Mode</th>
<th>Bandwidth</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx Channel</td>
<td>3.64 MHz</td>
<td>-10.03 dBm</td>
</tr>
<tr>
<td>Adjacent Channel</td>
<td>3.84 MHz</td>
<td>-73.81 dB</td>
</tr>
<tr>
<td>Alternate Channel</td>
<td>3.84 MHz</td>
<td>-80.01 dB</td>
</tr>
</tbody>
</table>

NOTE: Baseband = 30 MHz, NCO = 30 MHz with NCO Gain disabled, QMC Gain = 1446, LO = 1780 MHz

**Figure 19. TSW308x WCDMA Output (TRF3705 High-Gain Mode)**

<table>
<thead>
<tr>
<th>Mode</th>
<th>Bandwidth</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx Channel</td>
<td>3.64 MHz</td>
<td>-7.26 dBm</td>
</tr>
<tr>
<td>Adjacent Channel</td>
<td>3.84 MHz</td>
<td>-73.15 dB</td>
</tr>
<tr>
<td>Alternate Channel</td>
<td>3.84 MHz</td>
<td>-79.46 dB</td>
</tr>
</tbody>
</table>
4 Basic Test Procedure with TSW3100

This section outlines the basic test procedure for testing the EVM with the TSW3100.

4.1 TSW3100 Overview

The TSW3100 is a high speed pattern generator board. See the TSW3100 user’s guide (SLLU101) for more detailed explanations of the TSW3100 setup and operation. This document assumes that the TSW3100 software is installed and functioning properly. The TSW308x needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev D (or higher).

The TSW308xEVM sends the FPGA reference clock to the FPGA of the TSW3100EVM in LVDS format. Therefore, a 100-Ω LVDS termination resistor is needed at the TSW3100 FPGA clock input. All the latest TSW3100EVMs from TI have the 100-Ω termination installed at the bottom side of the board on pins T31 and T32 of the FPGA. Contact TI Application Support if the 100-Ω termination is missing and assistance is needed for the 100-Ω installation.

Figure 20. TSW3100 FPGA Clock 100-Ω LVDS Termination at Pins T31 and T32 of the FPGA
4.2 Test Block Diagram for TSW3100

The test setup for general testing of the TSW3084/TSW30H84EVM with the TSW3100 pattern generation board is shown in Figure 21.

External clock source is needed if LMK04800 is configured as the following:
- Clock Distribution Mode (Source to J12)
- Dual PLL Mode (Source to J12)
- Single PLL Mode (Source to J11)
See Optional Configuration Section for detail.

EVM includes additional RF signal path configurations such as:
- 3dB splitter for LO source
- Additional RF amp and attenuator path
See Optional Configuration Section for detail.

Figure 21. TSW3100 and TSW3084/TSW30H84 Test Setup Block Diagram
The test setup for general testing of the TSW3085EVM with the TSW3100 pattern generation board is shown in Figure 22.

![Figure 22. TSW3100 and TSW3085 Test Setup Block Diagram](image)

### 4.3 Test Setup Connection

**TSW3100 Pattern Generator**

1. Connect the EVM-supplied 18-AWG wires to the DC plug cable (Tensility 10-01776) to a qualified lab bench power supply. The 18-AWG red wire is the 5-V wire while the 18-AWG black wire is the ground wire.

2. Connect 5-V power supply cable to J9, **5V_IN** jack of the TSW3100EVM.

3. Connect the PC's Ethernet port to J13, **Ethernet** port of the TSW3100. The cable must be a standard crossover Cat5e Ethernet cable.

**TSW3084/TSW30H84/TSW3085 EVM**

1. Connect J13 connector of TSW3084/TSW30H84/TSW3085 EVM to J74 connector of TSW3100

2. See Section 3.3 Test Setup Connection for signal connections and jumper settings.

### 4.4 TSW308x Example Setup Procedure

See Section 3.4 TSW308x Example Setup Procedure for TSW308x Example setup for the GUI.
4.5 **TSW3100 Example Setup Procedure**

**TSW3100 Single-Carrier WCDMA Output Example Setup**

1. **TSW3100 Single-Carrier WCDMA Output Example Setup**
   - Start the TSW3100_CommsSignalPattern Software
   - For TSW3085 and TSW30H84, configure the TSW3100 to output a 614.4 MSPS, LVDS DDR format, 30-MHz IF Single-Carrier WCDMA output. See Figure 23 for details.
     - Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (that is, 1228.8 / 2 / 3.84 = 160)
     - Enter desired Offset Frequency (that is, 30 MHz) for each desired carrier
     - Select the **LVDS** output button
     - Check the **LOAD and Run** box
     - Press the green **Create** button

   - For TSW3084, configure the TSW3100 to output a 307.2 MSPS, LVDS Quad Interleave format, 30-MHz IF Single-Carrier WCDMA output.
     - Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (that is, 1228.8 / 4 / 3.84 = 80)
     - Enter desired Offset Frequency (that is, 30 MHz) for each desired carrier
     - Select the **16b QDAC** output button
     - Check the **LOAD and Run** box
     - Press the green **Create** button

   ![Figure 23. TSW3100 GUI for LVDS DDR Format](image-url)
2. (Toggle the SIF SYNC button to synchronize the appropriate digital blocks, if example file with NCO setting is used.)

3. Verify the spectrum using the Spectrum Analyzer at the two RF outputs of the TSW308xEVM (J7 for TSW3085, J7 and J9 for TSW3084 and TSW30H84).

4. With 1780 MHz of LO, the expect results are shown in Figure 18 (TRF3705 Low-Gain Mode) and Figure 19 (TRF3705 High-Gain Mode).

5. Optional Configuration

The onboard LMK048000 has the following configuration options for the flexible clocking of the DAC348x.

![Figure 25. LMK048000 Mode Selection](image-url)
5.1 Configuring the LMK04800 for Clock Distribution Mode

To use this mode:
- Provide a 2.4-Vpp maximum, 3.1-GHz maximum external clock at SMA J12.
- Select the Clock Distribution option in the LMK04800 Control tab.

5.2 Configuring the LMK04800 for Single PLL (PLL2 Only) Mode

To use this mode:
- The default reference is a 10-MHz crystal oscillator for the Single PLL mode. For the TSW3084/TSW30H84, set SJP5 to the 1-2 position. For the TSW3085, set SJP5 to the 2-3 position.
- Optionally, a 3.3-Vpp maximum, 140-MHz maximum external reference can be applied at SMA J11. For the TSW3084/TSW30H84, set SJP5 to the 2-3 position. For the TSW3085, set SJP5 to the 1-2 position.
- Select the PLL2 options in the LMK04800 Control tab.

5.3 Configuring the LMK04800 for Dual PLL (PLL1 + PLL2) Mode.

To use this mode, the following steps must be made to the EVM:
- Replace oscillator Y1 with a VCXO, such as a FVXO-HC73 series 3.3-V VCXO from Fox.
- Install R273, R274, R90, C177, and C300.
- Provide an external reference at SMA J12.
- Select the Dual PLL options in the LMK04800 Control tab.

Consult the LMK04800 data sheet for proper device configuration for this mode of operation.

6 Transmit Path Optional Configuration

6.1 Shared LO Path (TSW3084 and TSW30H84 only)

To share the LO source between the two transmit paths, the following configuration can be done:
- Install 0 Ω to R192
- Install 17.4 Ω to R190, R189, and R191
- Remove R188

6.2 Additional RF amp and attenuator path

To add additional gain and attenuation adjustment to the transmit path, the following configuration can be done:

For TX Path #1 (TSW3084/TSW3085/TSW30H84)
- Remove C258 and R165
- Install 0 Ω to R161, R163, and R293
- Install 0 Ω or ferrite bead to FB23

For TX Path #2 (TSW3084/TSW30H84)
- Remove C268 and R166
- Install 0 Ω to R162, R164, and R294
- Install 0 Ω or ferrite bead to FB21

With the default example pattern and LO of 1780 MHz, the RF signal chain output can be measured at J7 and J9 connectors. The expected results are shown in Figure 26 and Figure 27.
Figure 26. TSW308x RF Amp / Attenuator Output (TRF3705 Low-Gain Mode)

Figure 27. TSW308x RF Amp / Attenuator Output (TRF3705 High-Gain Mode)

Matching components can be changed depending on the RF frequency range. See the schematic in the TSW308x design package (listed in the References sections), TRF3705 data sheet (SLWS223), and the Avago MGA-30689 data sheet for details.
References

Related Products From Texas Instruments

- Quad-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC), DAC3484 (SLAS749)
- Dual-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC), DAC3482 (SLAS748)
- Quad-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC), DAC34H84 (SLAS751)
- Quad-Channel, 16-Bit, 1.5 GSPS Digital-to-Analog Converter (DAC), DAC34SH84 (SLAS808)
- 300-MHz to 4-GHz Quadrature Modulator, TRF3705 (SLWS223)
- LMK04800 Family Low-Noise Clock Jitter Cleaner with Dual Loop PLLs (SNAS489)

Related Tools From Texas Instruments

- TSW1400 High Speed Data Capture/Pattern Generator Card (SLWU079)
- TSW3100 High Speed Digital Pattern Generator (SLUU101)
- FMC-DAC-ADAPTER Physical Design Database Rev D Board (SLOR102)
- TSW3084EVM Design Package (SLAC515)
- TSW30H84EVM Design Package (SLAC517)
- TSW308x EVM Software (SLAC507)
- High Speed Data Converter Pro software (SLWC107)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2012) to B Revision  

- Changed information regarding power supplies and connections in the TSW1400 Test Setup Connection section........ 18
- Changed information regarding power supplies and connections in the TSW3084/TSW30H84 EVM Test Setup Connection section ................................................................. 18
- Changed information regarding power supplies and connections in the TSW3085 EVM Test Setup Connection section 19
- Changed information regarding power supplies and connections in the TSW3100 Test Setup Connection section........ 26
STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. **Delivery:** TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software.

1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 **Limited Warranty and Related Remedies/Disclaimers:**

2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 **Regulatory Notices:**

3.1 **United States**

3.1.1 **Notice applicable to EVMs not FCC-Approved:**

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 **For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:**

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.
FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) L'appareil ne doit pas produire de brouillage, et (2) L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/sds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/sds/ti_ja/general/eStore/notice_01.page

3.3.2 Notice for Users of EVMs Considered “Radio Frequency Products” in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan. If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan.
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.
【無線電波を送信する製品の開発キットをお使いになる際の注意事項】開発キットの中には技術基準適合証明を受けていないものがあります。技術基準適合証明を受けていないものご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿6丁目2-4番1号
西新宿三井ビル

3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/tpa/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/tpa/general/eStore/notice_02.page

4 EVM Use Restrictions and Warnings:

4.1 EVMs ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 Safety-Related Warnings and Restrictions:

4.3.1 User shall operate the EVM within TI’s recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User’s handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. Accuracy of Information: To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
6. **Disclaimers:**

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS AND CONDITIONS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSES OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT MADE, CONCEIVED OR ACQUIRED PRIOR TO OR AFTER DELIVERY OF THE EVM.

7. **USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.** USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. **Limitations on Damages and Liability:**

8.1 **General Limitations.** IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS AND CONDITIONS OR THE USE OF THE EVMS PROVIDED HEREUNDER, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS OCCURRED.

8.2 **Specific Limitations.** IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY WARRANTY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS AND CONDITIONS, OR ANY USE OF ANY TI EVM PROVIDED HEREUNDER, EXCEED THE TOTAL AMOUNT PAID TO TI FOR THE PARTICULAR UNITS SOLD UNDER THESE TERMS AND CONDITIONS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM AGAINST THE PARTICULAR UNITS SOLD TO USER UNDER THESE TERMS AND CONDITIONS SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. **Return Policy.** Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. **Governing Law:** These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products
- **Audio**: www.ti.com/audio
- **Amplifiers**: amplifier.ti.com
- **Data Converters**: dataconverter.ti.com
- **DLP® Products**: www.dlp.com
- **DSP**: dsp.ti.com
- **Clocks and Timers**: www.ti.com/clocks
- **Interface**: interface.ti.com
- **Logic**: logic.ti.com
- **Power Mgmt**: power.ti.com
- **Microcontrollers**: microcontroller.ti.com
- **RFID**: www.ti-rfid.com
- **OMAP Applications Processors**: www.ti.com/omap
- **Wireless Connectivity**: www.ti.com/wirelessconnectivity

### Applications
- **Automotive and Transportation**: www.ti.com/automotive
- **Communications and Telecom**: www.ti.com/communications
- **Computers and Peripherals**: www.ti.com/computers
- **Consumer Electronics**: www.ti.com/consumer-apps
- **Energy and Lighting**: www.ti.com/energy
- **Industrial**: www.ti.com/industrial
- **Medical**: www.ti.com/medical
- **Security**: www.ti.com/security
- **Space, Avionics and Defense**: www.ti.com/space-avionics-defense
- **Video and Imaging**: www.ti.com/video

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2016, Texas Instruments Incorporated