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TI Precision Designs: Verified Design

Ultra Low Power, 18 bit Precision ECG Data Acquisition System

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Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
ADS8881	Product Folder
OPA313	Product Folder
OPA2333	Product Folder
REF3330	Product Folder

Circuit Description

Electrocardiography (ECG), the measurement of the electrical activity of the heart, requires a precision analog front end instrumentation gain stage, filtering, and a high resolution analog to digital converter to achieve the highest performance. This design features the methodology for achieving a LEAD I ECG measurement system designed from discrete analog components. Ultra low power is achieved by creating a discrete instrumentation front end using an OPA2333 and then digitizing the signals with the 18 bit ADS8881 SAR ADC.

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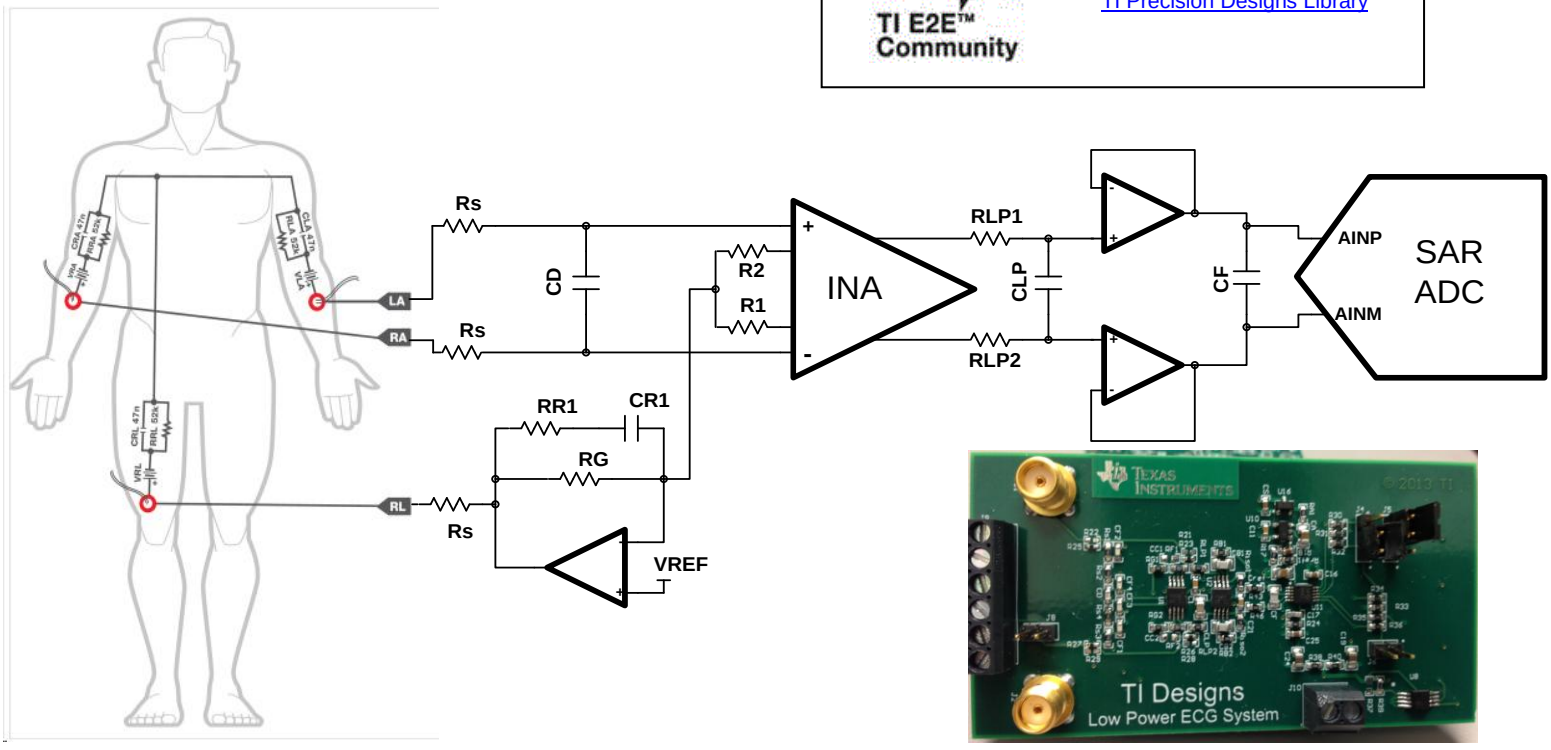

1 Design Summary

This design takes a block level approach for optimizing the precision components in the analog front end, post gain filter, input drive, reference, and analog to digital conversion conditioning circuitry typically found in a high precision analog data acquisition system for ECG. Also included will be recommendations on other low power, high precision alternative approaches as well as recommended power devices to make it easier to customize based on a unique set of design requirements.

The design requirements for this ECG data acquisition are:

- Total Power Consumption < 1 mW
- Resolution: 18 bits
- Input range: 0 – 3V dc
- Throughput Sampling Rate: 10ksps
- Analog/Digital Supply: 3.3V dc
- Input Bandwidth: 200Hz (ECG signals)

The design goals and performance are summarized in Table 1.

Figure 1 depicts the measured output of the ECG signal.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Power Consumption (mW)	< 1	0.550	0.700
System Noise (µV RMS)	47.4	38	48
Input-Referred Noise (µV RMS)	11.8	9.2	12
Signal-to-Noise Ratio (dB) (SNR @ 100Hz)	90	92	90
Common Mode Rejection Ratio (dB) (CMRR @ 60Hz)	-90	-80	-108

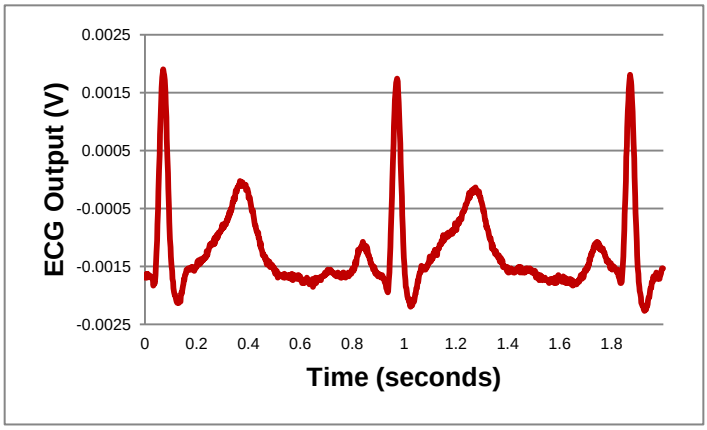

Figure 1: Measured ECG Output vs. Time

2 Theory of Operation

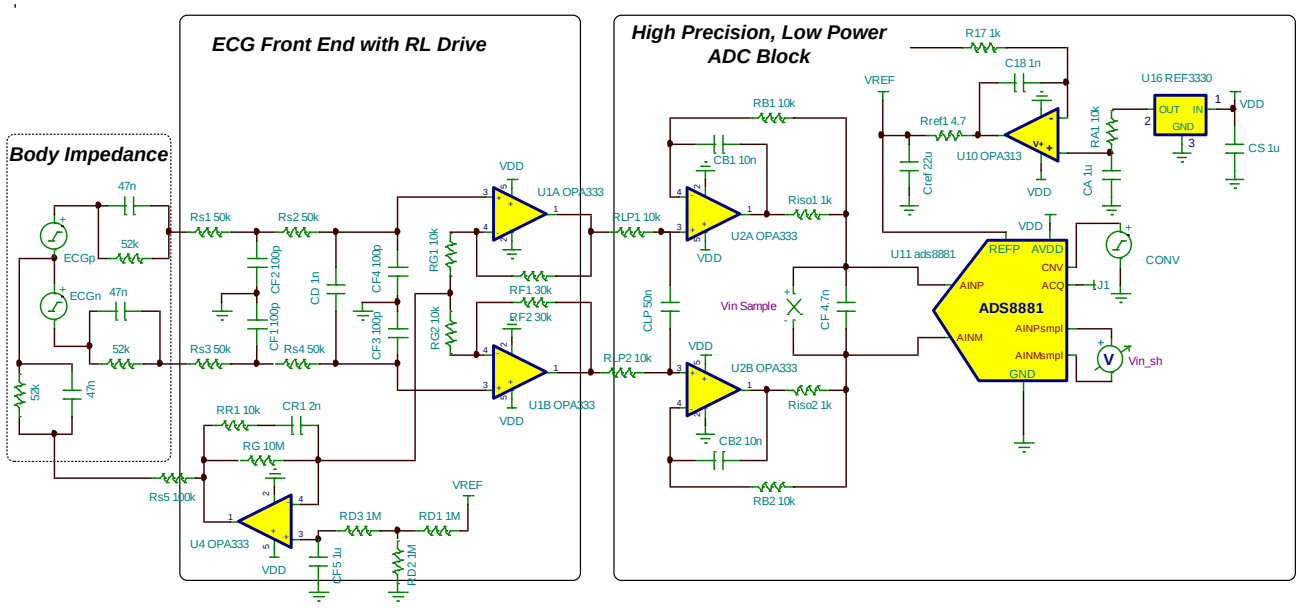

Figure 2: Complete Discrete Low Power ECG DAQ

2.1 Background on ECG Measurements

ECG is a method that converts the ionic polarization / depolarization from the heart muscle activity into a measurable electrical signal that can be detected and used to determine normal vs. problematic heart wave signatures. For this reason, it is imperative that the measurements are accurate and robust. Though the entire field of ECG includes a summation of measurements from many different reference configurations (i.e. chest lead, Wilson central, LEAD I, LEAD II, LEAD III), this design focuses solely on the LEAD I measurement, which is the electrical potential formed between the left arm (LA) and right arm (RA). The ECG signal is differential with respect to a right leg reference lead, typically in the range of 100µVpp – 2mVpp, and includes harmonics up to 200Hz; therefore, the small signal must be filtered, buffered, and amplified so that a clean signal can be digitized by the ADC.

To optimize the ECG front end design, the following 6 blocks need to be considered. Each block is numbered in Figure 3 and Figure 4.

Table 2: Six Design Blocks for Optimization in ECG System

Design Block	Function in ECG System
(1) Body Impedance:	Requires electrical model so that the proper analysis of the entire ECG front end can be properly considered
(2) Input filtering	Rejects EMI / RFI and protection resistance (typically ~ 100kΩ to minimize current that can be injected back into the patient)
(3) Pre-Amplifier Gain Stage	Relaxes requirements on ADC by amplifying the input signal, thereby requiring less bits to for an accurate ADC conversion
(4) Right Leg Drive (RLD) amplifier	Provides a common mode bias and reduces common mode noise
(5) V_{REF} Driver + Input Driver + ADC	This block is optimized for power, and its noise should dominate the signal chain
(6) Post Gain Low Pass Filter:	Ensures that the ADC block is the dominant noise source by filtering it to a minimum of 1/3 of the VREF Driver + Input Driver + ADC

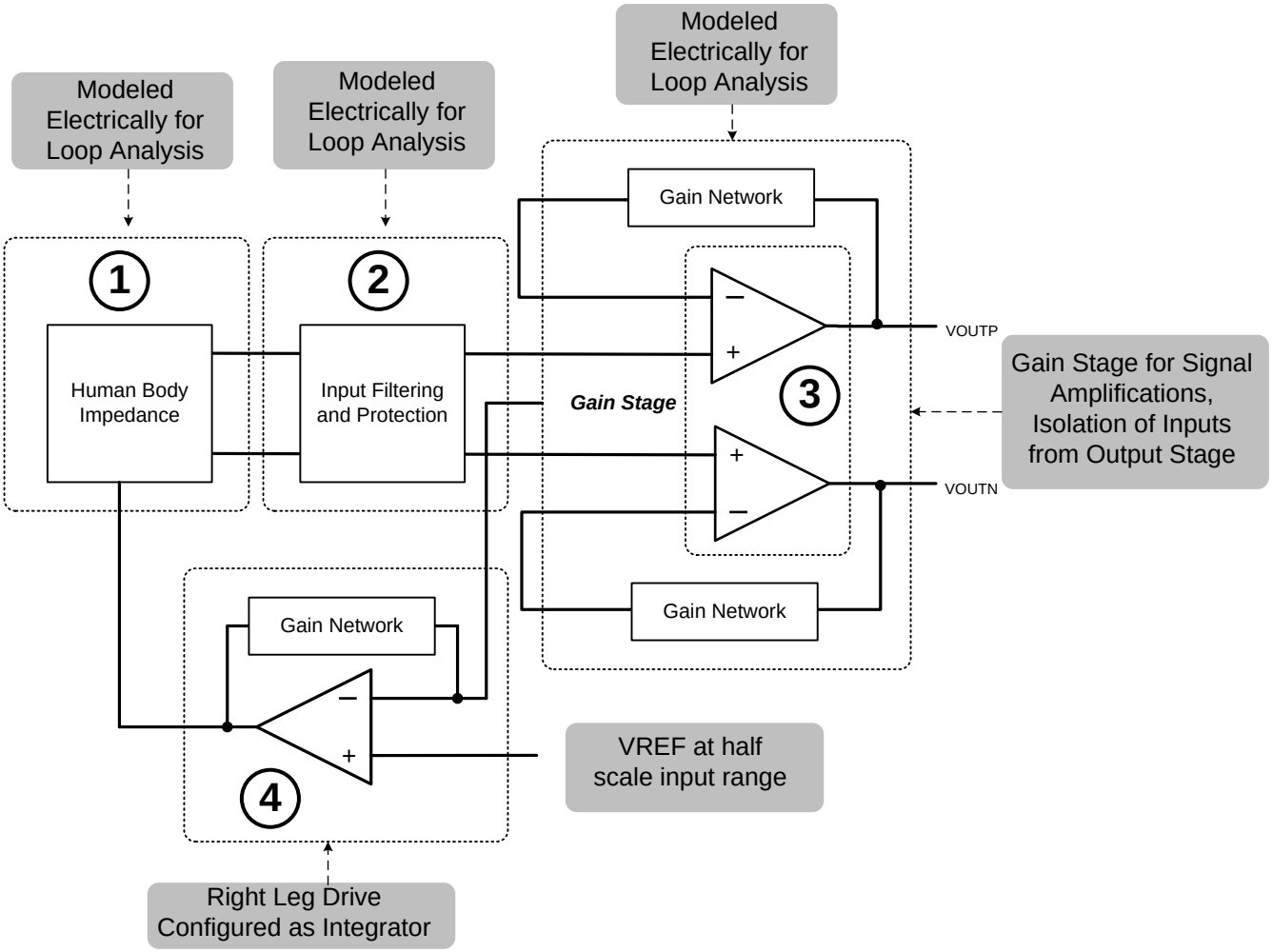

Figure 3: Block Level View of ECG Front End Design Steps

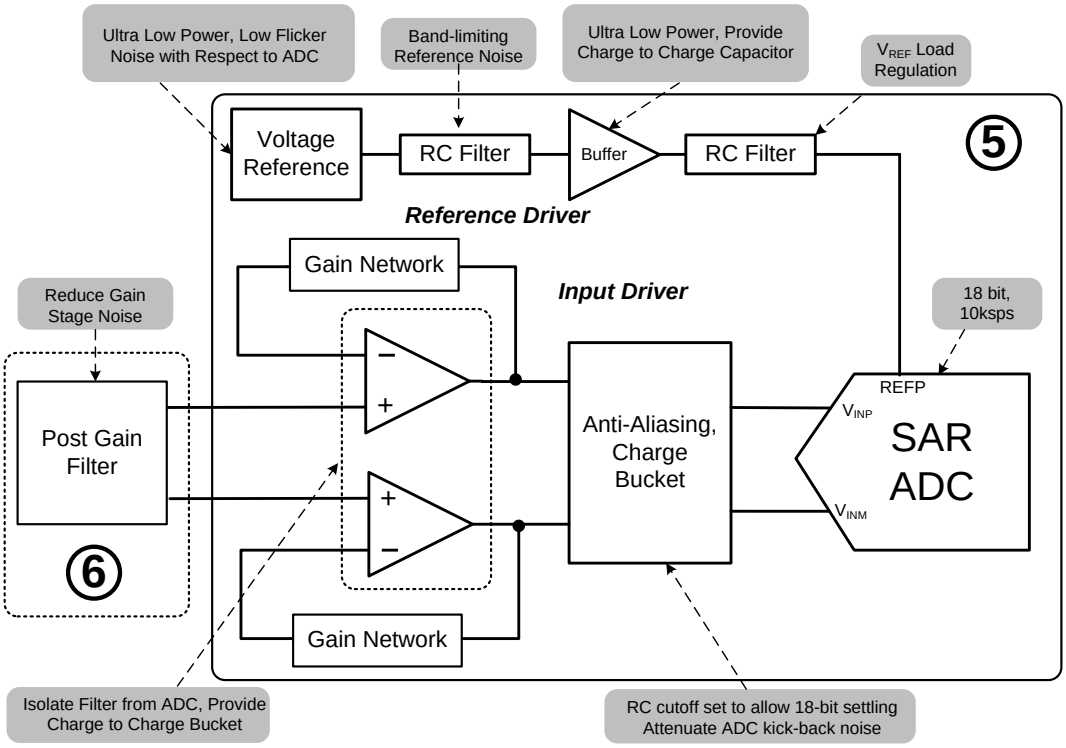

Figure 4: Block Level View of ECG ADC Design Steps

2.2 Electrode Impedance and Model

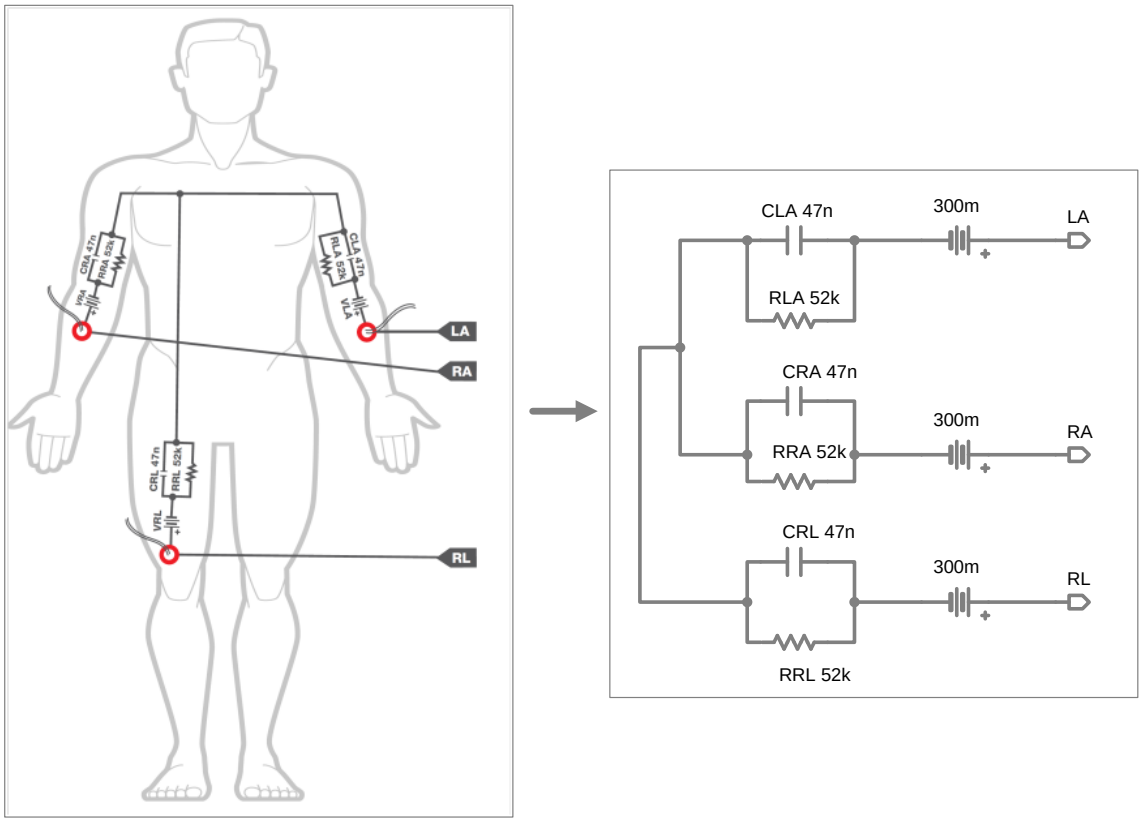

Figure 5: Electrical Model of the Human Body and ECG Electrode Impedance

The ECG data acquisition system is typically comprised of electrodes constructed from Ag-AgCl which make contact with the skin in order to effectively detect the electrical depolarization of the heart. Assuming a LEAD I configuration (i.e. voltage potential between left and right arm with respect to a right leg reference shown in Figure 6**)** the impedance of the electrode (along with the contact to the skin) can be lumped into a battery in series with a parallel RC combination of 47nF and 52kΩ. The battery model is ideally be 0V; however, over time and with varying external conditions it is possible for the Ag-AgCl voltage to become ±300mV, a factor that must be carefully considered when designing the front end gain stage.

An electrical model of the body impedance is very useful in helping design the analog front end of the ECG signal chain. The primary reason for this that the body itself forms an electrical path from the output of the right leg drive amplifier back to the input of the analog front end gain. The loop formed around the right leg drive amplifier (to be discussed in detail in a later section) can be inherently unstable and requires a secondary feedback path to compensate for this inherent instability.

2.3 Low Pass Filtering and Input Protection Resistance

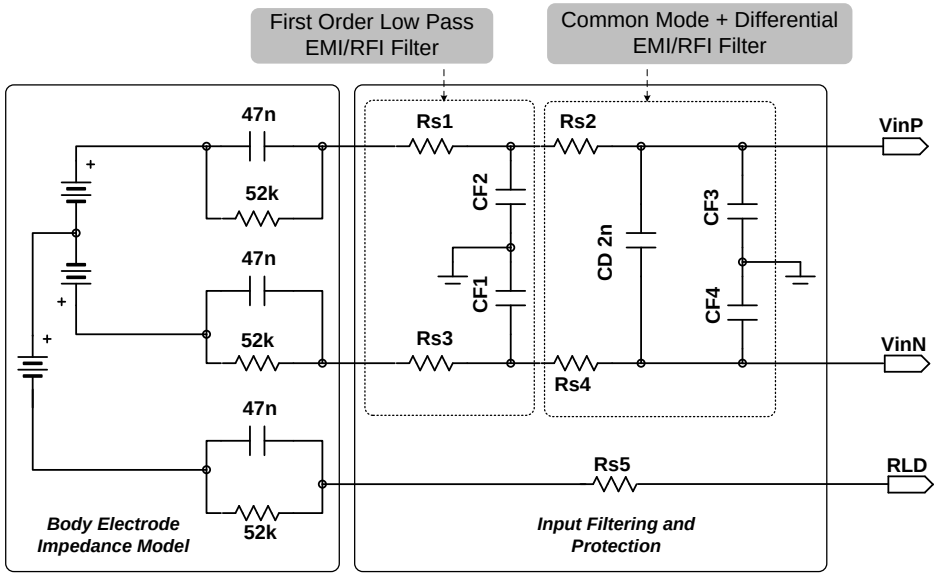

Figure 6: Input Protection and Filtering for ECG Front End

ECG front ends are required to have some level of protection resistance (usually 100kΩ) to minimize the amount of current that can be delivered from the electric circuitry back into the patient in a failure mode. In this design the 100kΩ protection resistance is split into two separate 50kΩ resistors (R_{S1} + R_{S2} and R_{S3} + R_{S4}) to allow for the creation of a second order common-mode low pass filter (with cutoff frequency, f_c) at the inputs for improved noise rejection. To further improve the rejection, a differential filter with cutoff frequency (f_D) is placed across the inputs. The capacitor selected for this filter must be large enough to keep f_D out of the way of the in band ECG signal, f_{ECG}, while at the same time filtering out high frequency noise. To accomplish this, is best to ensure the following:

$$f_D \geq 10 \bullet f_{ECG} \tag{1}$$

The second order filter can be easily understood through a single-ended analysis of the common mode filter at the positive input (i.e. R_{S1}, R_{S2}, C_{F1}, C_{F2}). Furthermore, to prevent any capacitive mismatch between C_{F1} and C_{F2} from reflecting itself as an in-band signal error (i.e. within the ECG bandwidth) it is necessary to place f_D at least a decade lower in frequency than f_c. The equations for both f_c and f_D are shown in (2) and (3) below:

$$f_c = \frac{1}{2\pi\sqrt{R_{s1}R_{s2}C_{F1}C_{F2}}} \tag{2}$$

$$f_D = \frac{1}{2\pi \times (R_{S1} + R_{S2} + R_{S3} + R_{S4}) \times C_D} \leq \frac{f_c}{10} \quad (3)$$

2.4 Instrumentation Amplifier

The instrumentation amplifier is a critical piece of the analog signal chain and can often have a dramatic impact on the performance of a precision signal chain. For the ECG signal chain, the INA chosen will perform the following primary functions:

(1) Buffers the inputs and electrode sensors from the post filtering and A/D block
(2) Provides amplification of the low level ECG signal

Table 3 gives a comprehensive list of the factors that need to be considered in determining the choice of the instrumentation amplifier.

Table 3: Selection Considerations for the Instrumentation Amplifier ECG Front End

Requirement	Benefit
High Input Impedance	Minimizing this reduces input loading on sensor, minimizes input current offsets on input resistors
Input Current Noise	Minimizing this reduces the amount of current noise that becomes converted to voltage noise on input resistors
Voltage Noise	Minimizing this improves the overall signal to noise ratio
CMRR vs. Frequency	Maximizing this reduces the amount of input offset changes due to 50/60Hz common noise coupling on the inputs
Resistive Gain Matching	Maximizing this improves the total unadjusted system error
Voltage Offset Drift	Minimizing this reduces the amount that the total unadjusted error changes at the output of the INA
Single Supply Operation	Designing a single supply amplifier simplifies the system supply requirements; usually correlates with a lower power architecture
Low Power	Enables use in power-sensitive or battery monitoring applications
Input Type	Using Differential Input Structure can improve common mode noise rejection
Output Type	Using Differential Output Structure can improve common mode noise rejection at ADC inputs as well as potentially reduce / relax signal conditioning circuitry

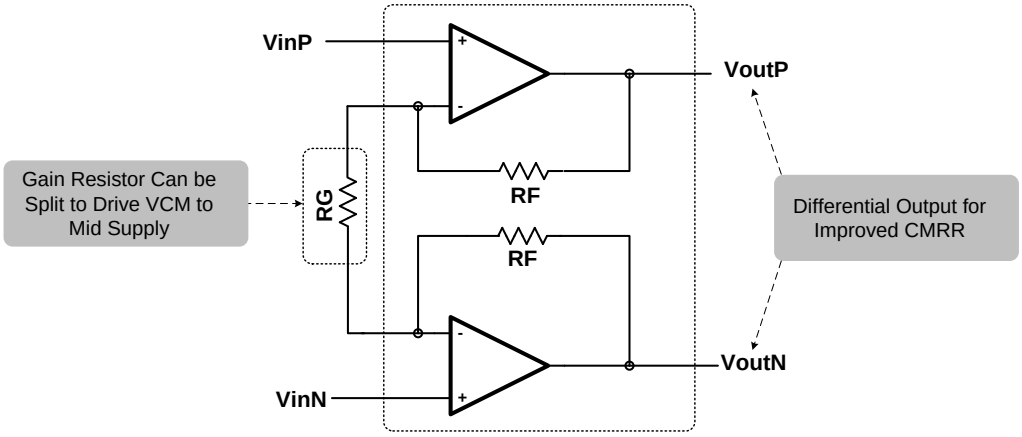

Figure 7: Differential In – Differential Out Instrumentation Amplifier Topology

Figure 7 shows an instrumentation gain block (INA) that will be used to amplify the ECG signal prior to sampling by the ADC. The reasons that this topology is the following:

(1) The differential output voltage will improve noise rejection at the inputs of the ADC
(2) The inputs are very high impedance which minimizes the loading and interaction of the input bias currents with the passive input impedances
(3) CMRR is dependent on the operational amplifiers selected and can be customized
(4) Uses 1 less amplifier than a 3 amplifier INA configuration which may be helpful in lowering power

The transfer function for this INA is given by the following:

$$\frac{V_{outP} - V_{outN}}{V_{inP} - V_{inN}} = 1 + 2 \bullet \frac{R_F}{R_G} \tag{4}$$

The differential output voltage which will be sampled by the ADC is given by the following:

$$V_{outP} - V_{outN} = \left(1 + 2 \bullet \frac{R_F}{R_G}\right) \bullet \left(V_{inP} - V_{inN}\right) \tag{5}$$

2.5 Right Leg Drive Amplifier

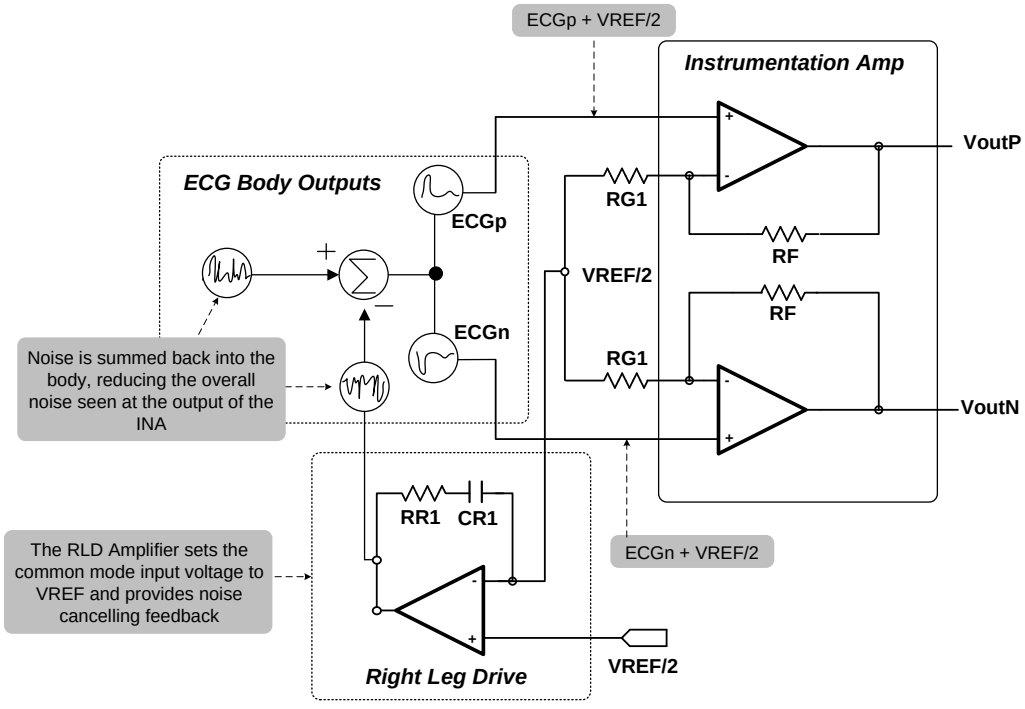

Figure 8: Simplified Diagram of Right Leg Drive Operation

Figure 8 shows a block level image of the right leg drive (RLD) amplifier in the ECG analog front end.

The purpose of the right leg drive amplifier is twofold:

(1) Provide a common mode, DC bias and input bias return path for the INA front end
(2) Reduce common mode noise at the inputs of the front end INA

The RLD amplifier is configured as an integrator that adjusts its output voltage to keep its inverting input at the same potential as the voltage applied at the non-inverting input. In doing so, the RLD amplifier ensures that the average value of the inputs (i.e. the common mode voltage) stays fixed. The RLD amplifier is properly biased when its non-inverting input is set to mid scale (V_{REF}/2) and the summing node is connected to a "midpoint" of the two inputs, which in this case is set up by splitting the gain resistor into R_{G1} and R_{G2}. Trans-Z INA topology lends itself to splitting the gain resistor, RG, in half to achieve the common mode midpoint.

Since the RLD amplifier is an integrator, the cutoff for the integrator time constant is determined by R_{R1} and C_{R1}. This RC combination establishes the dominant feedback path around the RLD to ensure stability of the overall loop. Without it, the dominant feedback path is through the INA which in most cases produces a loop that is not stable.

2.6 V_{REF} Driver + Input Driver + ADC (Ultra Low Power SAR ADC Block)

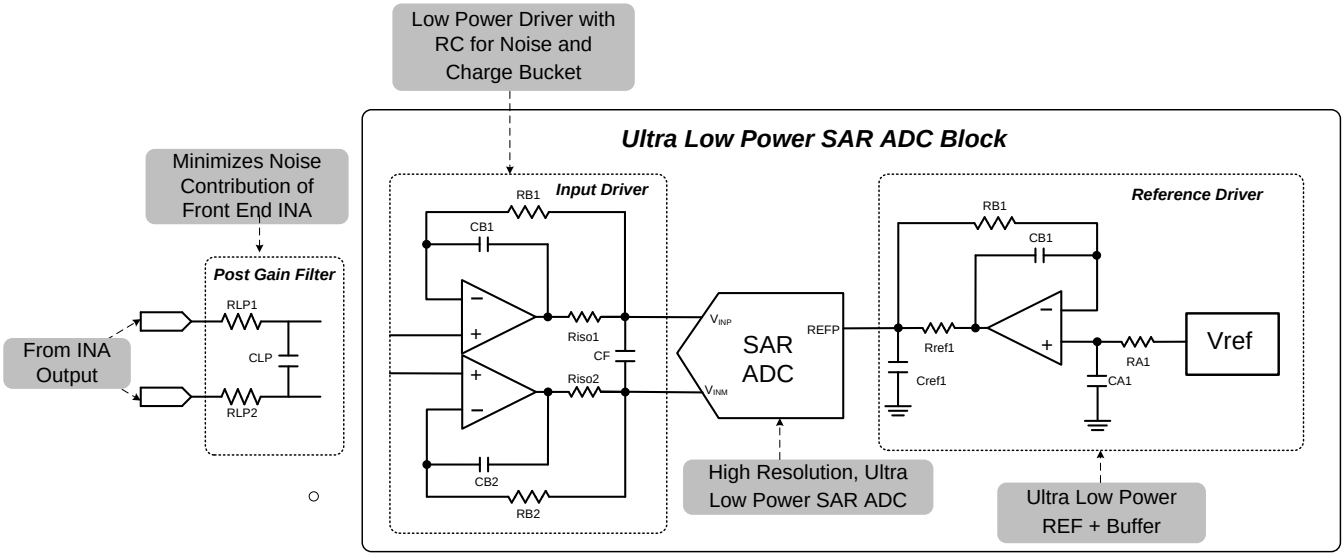

Figure 9: Ultra Low Power SAR ADC Block for ECG

The details for the overall design process for the "Ultra Low Power SAR ADC Block" shown in Figure 9 are contained within the document, SLAU514. In subsequent sections there will be a summary of the key concerns, equations, and design tricks that reference this document for designing a SAR ADC data acquisition block for high resolution and ultra low power.

2.6.1 V_{REF} Driver

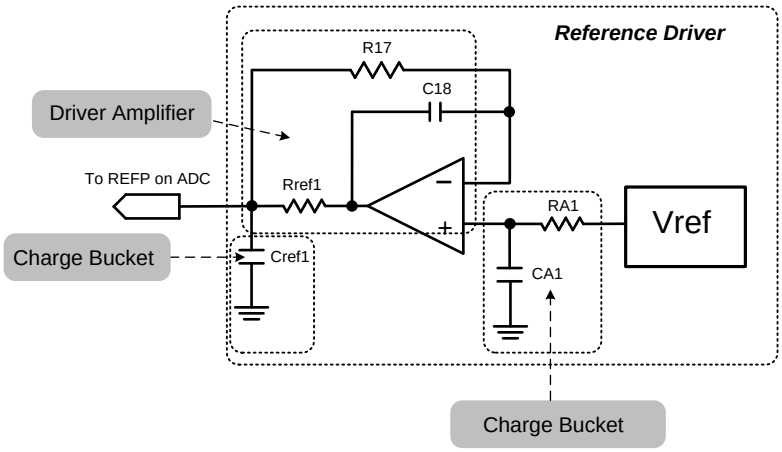

Figure 10: Ultra Low Power Voltage Reference and Buffer Circuit

2.6.1.1 Noise optimization of the V_{ref}

For the ADC to make a valid conversion, it must have an accurate "frame of reference". The overall goal is to reduce the noise of the voltage reference circuit so that the overall noise of the Ultra Low Power SAR ADC block is dominated by the inherent noise (ex. quantization) of the ADC. Moreover, this means choosing the values for R_{A1} and C_{A1} (shown in Figure 10) to ensure noise is limited to an acceptable level.

RMS Noise from the voltage reference (e_{noise}) is calculated via the root-sum-square of the RMS flicker noise e_f (1/f noise specified in peak to peak noise between .1Hz – 10Hz) and the broadband noise (e_{BB}):

$$e_{noise} = \sqrt{e_f^{\,2} + e_{BB}^{\,2}} \tag{6}$$

Also, there is a direct tradeoff in broadband noise density (e_{BBd}) and quiescent current consumption (I_{ref}):

$$e_{BBd} = \frac{\sqrt{\mu A}}{\sqrt{2} \bullet I_{ref}} \tag{7}$$

A good rule of thumb for scaling the noise of the reference buffer is given in equation 8. Note that a first order low pass filter formed by R_{A1} and C_{A1} (f_{cr}) must be inserted between the voltage reference and the buffer amplifier to limit e_{noise} to ≤ 3x the RMS noise of the analog to digital converter (e_{ADC}).

$$e_{noise} \le \frac{1}{3} \bullet e_{ADC} \tag{8}$$

The RMS noise of the ADC, e_{ADC}, is derived from the SNR which is specified in the data sheet. Using the following equation, it is possible to relate the RMS noise to the SNR and the full scale input range of the ADC based on the value of the voltage reference (V_{ref}):

$$SNR(dB) = 20\log_{10}\left(\frac{V_{ref}/\sqrt{2}}{e_{ADC}}\right) \tag{9}$$

Solving for e_{ADC} gives the following:

$$e_{ADC} = \frac{V_{ref}}{\sqrt{2} \bullet \left(10^{SNR/20}\right)} \tag{10}$$

Consequently, the selection of the voltage reference is a tradeoff between power consumption and noise. Therefore, if f_{cr} is made small enough it is possible to minimize the contribution of e_{BB} to the overall RMS noise of the Ultra Low Power ADC block (i.e. e_{ADC}) to a level where it is not significant with respect to the ADC. Also, from equation 6,

$$e_{BB} = \sqrt{e_{BBd} \bullet \frac{\pi}{2} \bullet f_{cr}} \tag{11}$$

2.6.1.2 Charge Bucket (C_{ref1}) Calculation

Referring again to Figure 10, C_{ref1} is referred to as a "charge bucket" because it acts like a reservoir from which the ADC pulls current while the buffer amplifier replenishes the average charge so that the voltage at the ADC reference pin may be well regulated.

The net charge ΔQ needed to be delivered to the ADC's voltage reference pin by the external capacitor, C_{ref1}, is directly proportional to the amount of current drawn by the ADC reference pin (I_{REF}) during one conversion time, $T_{throughput}$:

$$\Delta Q = I_{REF} \bullet T_{throughput} \tag{12}$$

The change in the reference buffer output voltage cannot exceed ½ LSB of the ADC (determined by n number of bits and range of $\pm V_{REF}$), given by the following equation:

$$\Delta V_{ref} \le \left(\frac{1}{2}\right) \bullet \left(\frac{2V_{REF}}{2^n}\right) \tag{13}$$

Therefore,

$$\frac{I_{REF} \bullet T_{throughput}}{C_{ref1}} \le \left(\frac{1}{2}\right) \bullet \left(\frac{2V_{REF}}{2^N}\right) \tag{14}$$

From this, the charge bucket capacitor, C_{ref1}, can be calculated:

$$C_{ref1} \ge 2^n \bullet \left(\frac{I_{REF} \bullet T_{throughput}}{V_{REF}}\right) \tag{15}$$

2.6.1.3 Buffer Amplifier + R_{ref1}

The buffer amplifier in Figure 10 is required to re-charge Cref1 in between conversions to ensure that the voltage provided to the ADC is well-regulated. Here are the tradeoffs to consider when selected a low power operational amplifier to drive the reference pin:

(1) **Gain Bandwidth**—this translates directly to the OPA's ability to recharge C_{ref1} in between conversions

(2) **Open Loop Output Impedance**—as an amplifier runs out of bandwidth its ability to keep the output impedance low in a closed loop reduces to the value of the open loop output impedance. This appears as a series resistor with the large value of C_{ref1} thereby forming a time constant that can prevent the buffer output from settling.

(3) **Stability**—large capacitive loads can have the effect of causing instability in the buffer amplifier. Even if this instability is a very small, low level oscillation, it can easily show up in the conversion of the ADC and degrade some, if not all of its DC and AC specifications.

(4) **R_{ref1}**—this resistor is crucial for isolating C_{ref1} from the buffer driver to help with stability. Selecting this resistor involves a delicate balance between stability, noise filtering, and current load regulation. Make this resistor too small and the amplifier becomes difficult to stabilize; however, make it too large and this will limit the amount of current the buffer can provide to C_{ref1} thereby limiting its ability to provide charge in between conversions. Therefore, the R-C time constant (τ) formed from R_{ref1} and C_{ref1} must have some restriction to make sure V_{ref} settling is achieved. The assumption is the following:

$$\tau = R_{ref1} \times C_{ref1} \leq \frac{1}{f_{sample}} \tag{16}$$

2.6.1.4 Input Driver

In designing and optimizing the ADC input driver, once again a balance must be struck between power consumption, ADC sampling rate, noise, settling time, and charge bucket filter. In general if the ADC is a SAR and is sampling at a lower conversion rate, a lower power drive amplifier can be used because there will be more time for settling due to the increased acquisition time.

Figure 11 shows a common configuration for voltage follower SAR drivers. Components such as Riso1, Riso2 help with stability by isolating the amplifier from the capacitive charge bucket (CF), while the dual feedback around the amplifier keeps the closed loop output impedance low thereby minimizing the interaction with the resistance internal to the ADC.

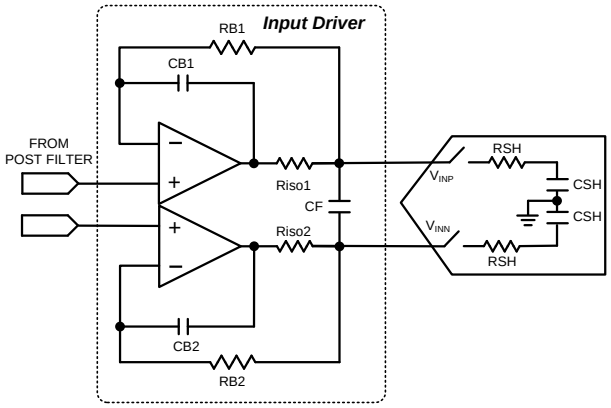

Figure 11: SAR ADC Input Driver

A differential, RC filter is placed across the inputs to filter input noise, minimize aliasing (i.e. frequency harmonics folding back into the pass band), and to serve as a "flywheel" or charge reservoir for the internal sample and hold circuitry from the ADC (formed by R_{SH} and C_{SH}).

R_{iso1}, R_{iso2}, and C_F form a low pass filter with the following cutoff frequency of f_{filter}:

$$f_{filter} = \frac{1}{2\pi \bullet 2R_{iso}C_F} \tag{17}$$

Assuming the voltage droop on the flywheel capacitor (C_F) from sampling during a single ADC conversion is represented by ΔV_F, the corresponding amount of charge ΔQ_F required to sustain this droop is given by the following:

$$\Delta V_F = \frac{\Delta Q_F}{C_F} \tag{18}$$

Assuming the rule of thumb that the voltage on C_F cannot droop more than 5% of its initial full scale value input value (V_{fs}, which is determined by the voltage reference), the following relationship is established:

$$\Delta V_F = \frac{\Delta Q_F}{C_F} \le .05 V_{fs} \tag{19}$$

$$\frac{C_{SH} \bullet V_{REF}}{C_{FLT}} \le \left(\frac{1}{20}\right) V_{fs} \tag{20}$$

$$C_{FLT} \ge 20 \bullet C_{SH} \tag{21}$$

2.7 Post Gain (INA) Low Pass Filter

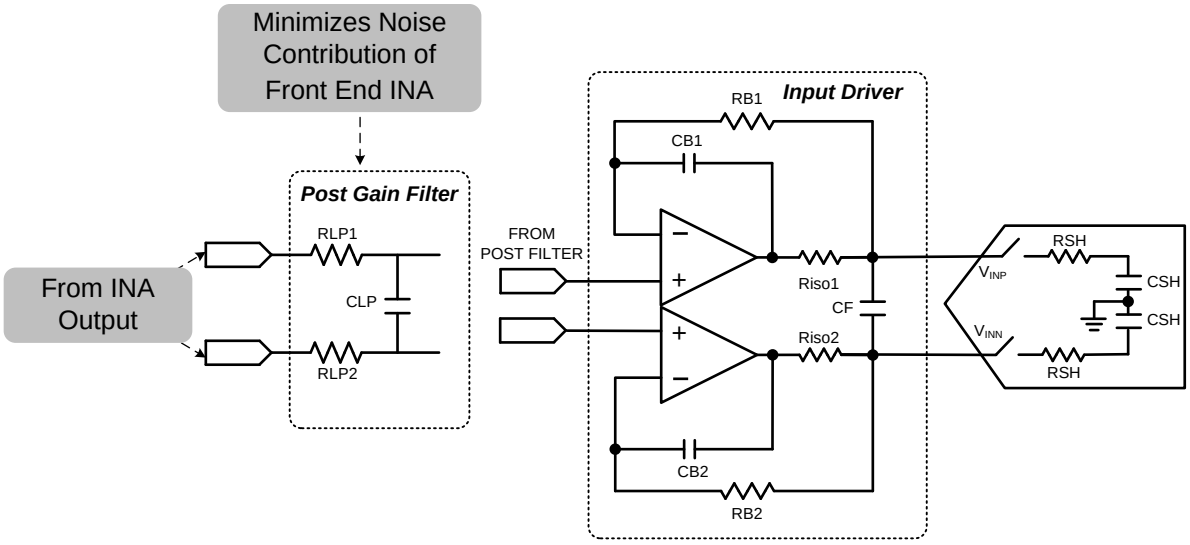

Figure 12: Post Gain Filter

The purpose of the low pass filter that follows the INA gain stage is to reduce the noise of the front end INA circuitry (e_{INA}) to a level that is statistically insignificant compared to the noise of the ADC circuitry (e_{ADC}). Since the noise will be Gaussian, the root-sum-squares method can again be employed to calculate the total ECG system noise, e_{ECG_OUT}.

$$e_{ECG\_OUT} = \sqrt{e_{INA}{}^2 + e_{ADC}{}^2} \tag{22}$$

Therefore, if e_{INA} is at least 3x smaller than e_{ADC}, the overall noise of the SAR ADC block may be approximated by e_{ECG_OUT}.

$$e_{ADC} \ge 3 \bullet e_{INA} = e_{ECG\_OUT} \tag{23}$$

Consequently, the desired filtered INA noise value ($e_{INA\_filtered}$) can be optimized using the following equation where $f_{INA\_filtered}$ is the cutoff frequency:

$$f_{INA\_filtered} = \frac{1}{2\pi R_{LP1} C_{LP}} \tag{24}$$

$$e_{INA\_filtered} = e_{INA} \sqrt{\left(f_{INA\_filtered}\right) \bullet \left(\frac{\pi}{2}\right)} \tag{25}$$

$$f_{INA\_filtered} = \frac{2}{\pi} \bullet \left(\frac{e_{INA\_filtered}}{e_{INA}} \right)^2 \quad (26)$$

Equation 25 is a recursive function which can be solved iteratively, yielding the cutoff frequency needed to achieve an RMS noise target from the front end INA. Alternatively, a much easier way to solve for $f_{INA\_filtered}$ is through a noise simulation using TINA-TI™ SPICE. See figure….

3 Component Selection

The overall goal is to design the lowest power, highest precision ECG data acquisition system out of discrete components. During normal mode of operation, the power consumed in the Vref driver and the input driver will eclipse that of the ADC. Since these blocks will be the dominant source of power, the following steps were taken to achieve the power consumption goals highlighted in Table 1:

(1) Start with the Ultra Low Power Data Acquisition block that was designed in SLAU514x. In this design, the ADS8881 was chosen for its excellent resolution (18bits) and power consumption (55µW @ 10ksps). The overall power consumed by this block was measured at 400µW, which leaves another 50µW that can be used on the front end INA.

(2) Using Table 3 as a reference for the key concerns for the selection of the INA, the following table lists some candidate devices that were considered in this design:

Table 4: Table of Amplifier Candidates for ECG INA Front End

Device	Power (µA)	Selected? Y/N
OPA2333	34	Yes—best power to noise, precision offered
OPA2336	40	No—flicker noise too high
INA333	50	No, single-ended output, requires extra OP AMP for reference pin and level shift
INA321	40	No, single-ended output, requires extra OP AMP for reference pin and level shift, noise too high

(3) Power Partitioning in ECG System

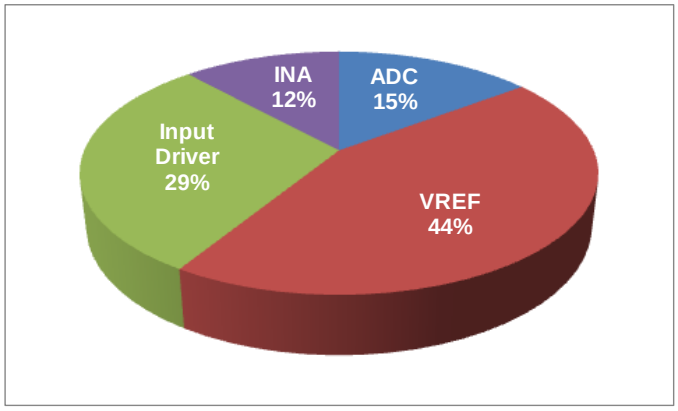

Figure 13: Total Current Allocation of ECG Design Blocks

3.1 Low Pass Filtering and Input Protection Resistance

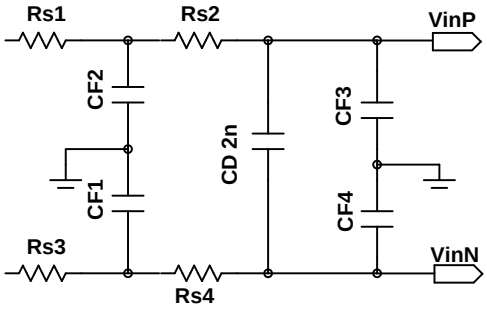

Figure 14: Input Filtering and Protection for ECG Front End

Using equations (1-3), and the selected values for RS1, RS2, RS3, and RS4 the input low pass filter formed by the common mode component can be calculated. Since the ECG bandwidth is ~200Hz, according to equation 1 the low pass cutoff frequency should not be any lower than 2kHz to keep the filter out of the way of the in band ECG signal. Also, equation 3 shows that the differential filter fD formed by RS1, RS2, and CD will have a decade will have a 10x lower cutoff frequency than fc, from which we can assign standard values for CF1, CF2, CF3, CF4 of 100pF, this gives the following:

$$f_c = \frac{1}{2\pi\sqrt{R_{s1}R_{s2}C_{F1}C_{F2}}} = \frac{1}{2\pi\sqrt{50k\Omega \bullet 50k\Omega \bullet 100pF \bullet 100pF}} = 32kHz \quad (27)$$

So now with the common mode filter cutoff frequency set to 32kHz, the differential cutoff frequency (f_D) now can be set by the following:

$$f_D = \frac{1}{2\pi\sqrt{(R_{s1} + R_{s2})C_D}} = \frac{f_c}{10} = 3.2kHz \quad (28)$$

Solving for C_D yields the following:

$$C_D = \frac{1}{2\pi\sqrt{(R_{s1} + R_{s2})f_D}} = 2nF \quad (29)$$

3.2 Instrumentation Amplifier

To minimize drift, noise as well as power consumption, the OPA333 was chosen as the amplifier from which the INA was constructed. The pros and cons of using this INA topology are listed in Table 5:

Table 5: Summary of Advantages / Disadvantages of OPA2333 INA

Requirement	Benefits of the OPA2333 "Trans-Z" Configuration
High Input Impedance	*Advantage: Input Bias current = 200pA and will cause minimal voltage offset errors at inputs
Input Current Noise	*Advantage: Overall Noise Contribution due to input current noise is minimal
Voltage Noise	*Advantage: Noise density = 50nV/√Hz, 1/f noise = 1.1μVpp
CMRR vs. Frequency	*Advantage: 90dB @ 60Hz for single amplifier
Resistive Gain Matching	Disadvantage: Requires discrete resistors for Gain Matching
Voltage Offset Drift	*Advantage: 0.05μV/°C
Single Supply Operation	*Advantage: Offers 3.3V operation with rail to rail I/O
Low Power	*Advantage: Quiescent current = 17μA / Amplifier
Input Type	*Advantage: Optimized for EMI / RFI Immunity see note *SBOZ004A*
Output Type	*Advantage: Using Differential Output Structure can improve common mode noise rejection at ADC inputs

3.3 Right Leg Drive Amplifier

The most effective way to analyze the RLD amplifier stability is through the use of TINA-TI™ SPICE. To do this, determine frequency, f_c, and rate of closure at the intersection of the open loop gain (AOL) and the feedback factor (1/β) on a Bode plot.

Recall that to ensure stability for a two pole system, the following must be true:

$$\text{Stable} = \text{AOL}_{f_c} - \left(\frac{1}{\beta}\right)_{f_c} \leq -20\frac{\text{dB}}{\text{dec}} \tag{30}$$

To test for stability, the outer loop of RLD Drive amplifier (1/β) is analyzed versus the AOL curve using the simulation circuit in Figure 15. The results show that the AOL intersects the 1/β curve at -40dB/dec at fcl = 50kHz. Therefore, the RLD amplifier needs a compensation feedback path to flatten out the upward slope of the 1/β curve.

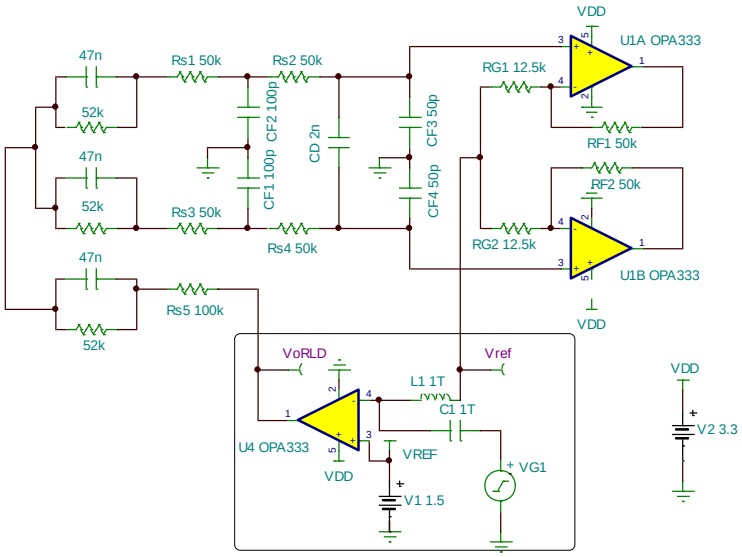

Figure 15: Right Leg Drive (no compensation) Simulation Circuit

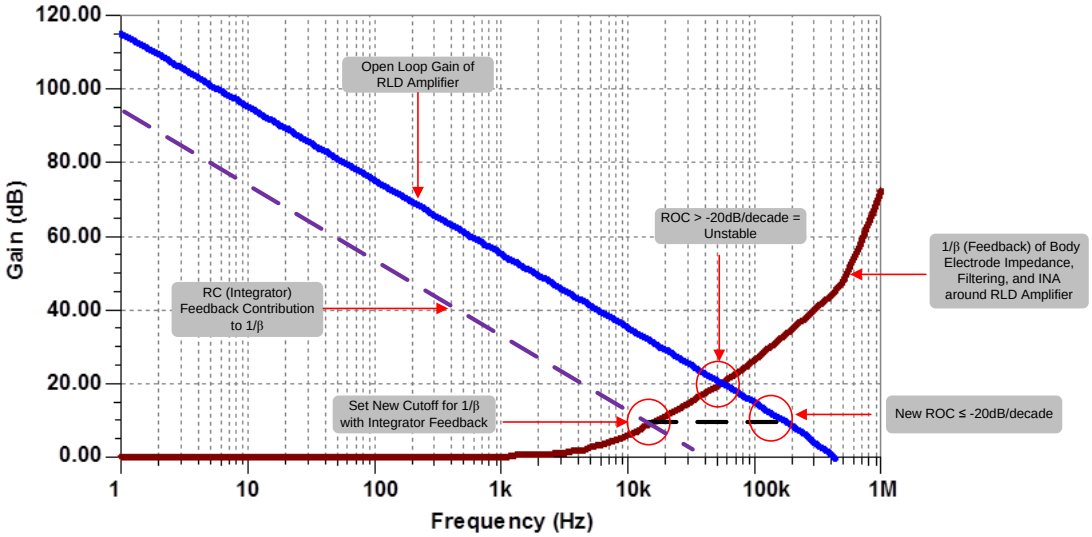

Figure 16: Plot of AOL vs. 1/Beta Showing Instability

The dotted line in Figure 16 shows the response that would be achieved with a series R_{R1} and C_{R1} (see Figure 17) placed in the feedback of the RLD amplifier. As shown, to make this system stable it is necessary to ensure the added compensation path dominates the feedback network so that it can intersect the AOL curve (blue) at -20dB/dec or less. It is also important to make sure that f_c is greater than at least a half a decade away from the AOL curve. The reason for this is to allow for process variation which could quickly erode the frequency margin that is needed to flatten the curve in time for the intersection. Therefore, the corner frequency (f_{RLD}) for the compensation path is selected to be 8kHz. Choosing a standard value of 10kΩ and 2nF gives the following:

$$f_{RLD} = \frac{1}{2\pi R_{R1} C_{RR1}} = 8kHz \tag{31}$$

The simulation of the compensated circuit is shown in Figure 17 below:

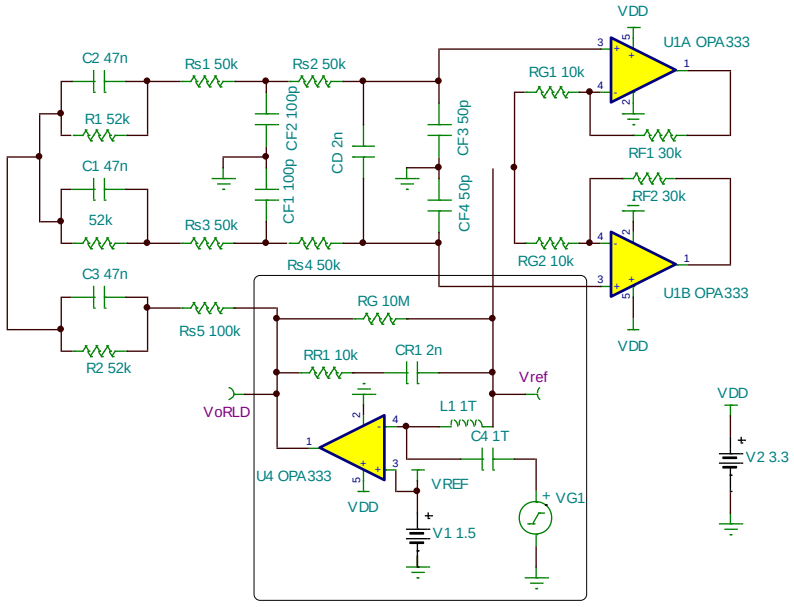

Figure 17: RLD Simulation Circuit with Compensation for Stability

Finally, Figure 18 confirms that RR1 and CR1 affect the 1/β curve to produce a < -20dB/dec rate of closure and a stable feedback loop.

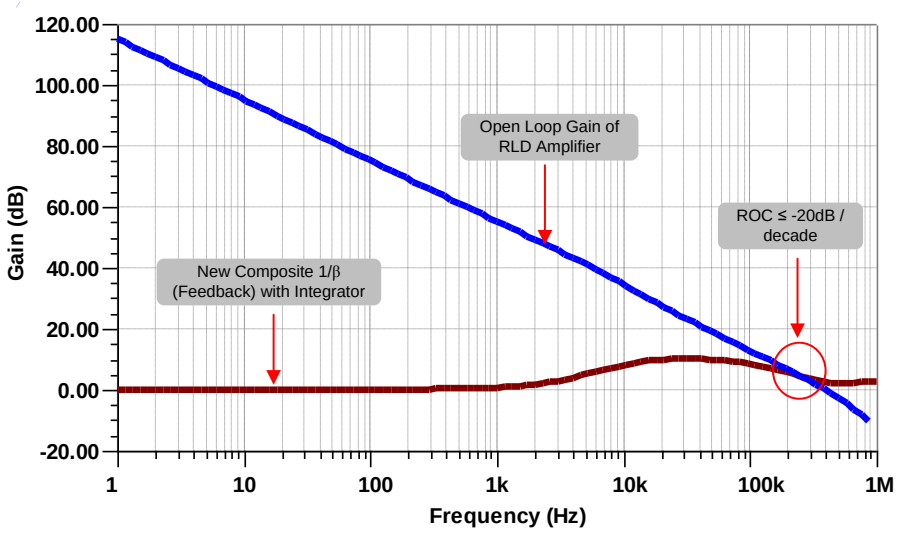

Figure 18: Plot of AOL vs. 1/Beta Showing Stability

3.4 V_{REF} Driver + Input Driver + ADC (Ultra Low Power SAR ADC Block)

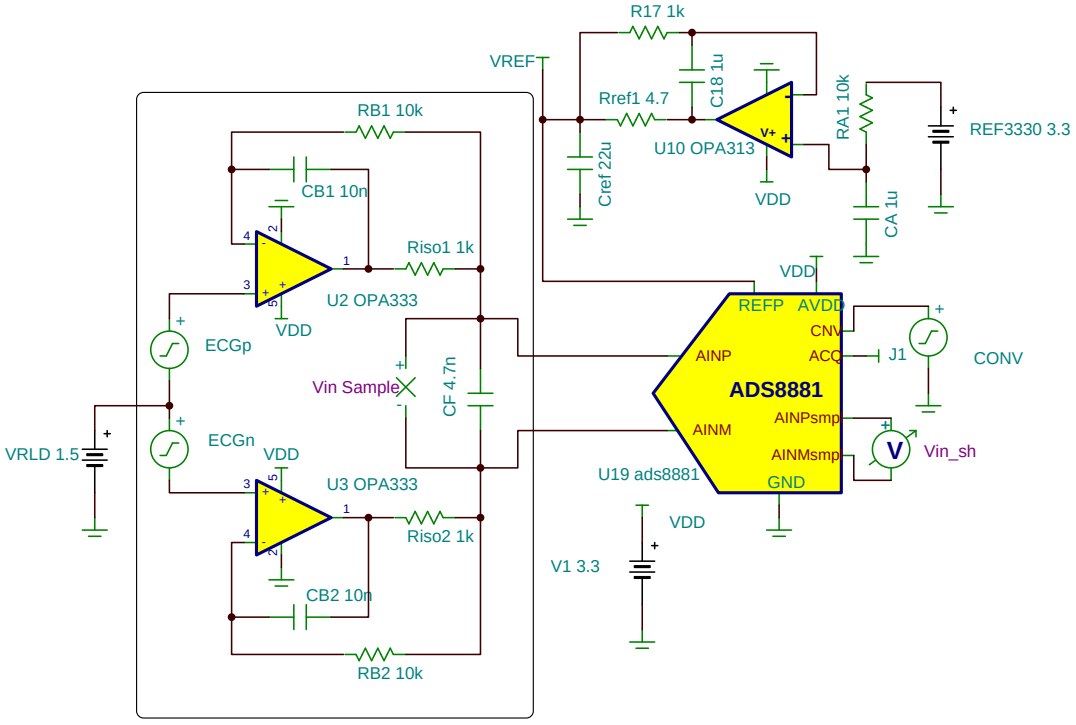

Figure 19: Input Driver Configuration

Table 6 gives a summary taken from SLAU514, in which the process for designing a picking the components for the input driver is given in more detail:

Table 6: Key Component Selection Tips for Input Driver

Parameters	Notes
V_{in} Range	Establish the V_{in} range from REF3330 = 3V. Give 100mV of input head room to ensure that the voltage of the **OPA2333** input driver never saturates. Therefore, 3V -100mV = 2.9V.
Flywheel Capacitor (C_F)	Use the value of the sample-and-hold capacitor from the ADS8881, C_{SH} = 59pF, and Equation 17: $C_F = 20 \times C_{SH} = 20 \times 59pF \geq 1.2nF$.
C_F Value	Choose the closest standard value for best noise rejection: **C_F= 4.7nF**. Another value that could improve noise rejection would be 10nF, but for COG capacitor price could become an issue.
C_F Type *Important*	***Choose a COG which is much higher quality than an X7R***. The X7R yields spurious harmonics in the FFT because its value of C changes with applied voltage.
Filter Resistor (Riso1, Riso2) **R_{iso} Value**	Choose 1kΩ for output impedance matching, 10kΩ degrades THD due to limited load regulation to re-charge CDAC, 100Ω causes spurs due to stability issues **Riso1 = Riso2 = 1kΩ.**
Feedback Filter of OPA2333	Choose **R_{B1} = R_{B2} = 10kΩ**, and **C_{B1} = C_{B2} =10nF** to keep R_{iso1}, R_{iso2}, from interacting with R_{SH} (see Figure 11: SAR ADC Input Driver) and causing attenuation in the sampled input signal.

3.5 V_{REF} Driver

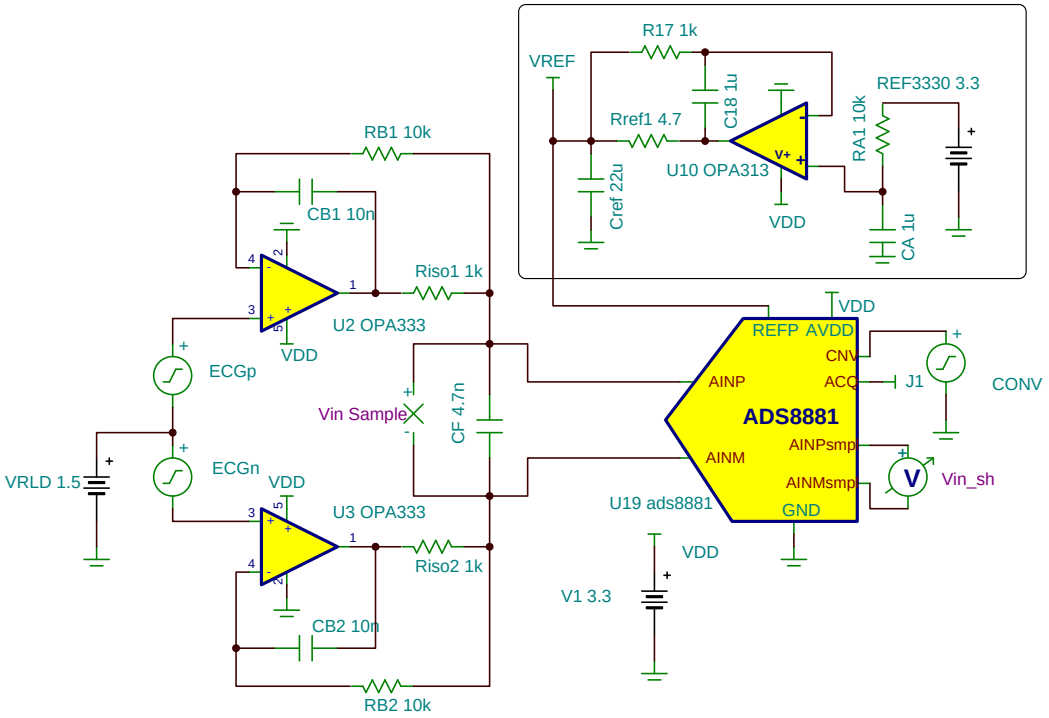

Figure 20: Reference Driver Configuration

Table 7 gives a summary taken from SLAU514, in which the process for designing a picking the components for the reference driver is given in more detail:

Table 7: Summary of Key Design Components and Parameters

Parameters	Notes
Voltage Reference Selection	From Table 5, Page 20 of SLAU514, choose **REF3330** (3.0V version of REF3325) family due to ultra low power (I_Q = 5µA) and RMS flicker noise (Noise PP / 6.6 = 10.6µV RMS), lower than RMS noise floor of ADS8881 (35µVRMS). Also, 3V means larger input range and improved SNR.
Reference Filter (R_{A1} and C_{A1})	Ensure that the noise contribution is 1/3 of the ADC RMS noise. **Choosing R_{A1} = 10kΩ** and **C_{A1} = 1µF** set f_{cr} = 16Hz
Charge Bucket Capacitor (C_{ref1})	Referring to Equation 13, assuming a sampling rate of 10ksps from the ADS8881, **C_{ref1} = 22 µF.** The average input current into the ADC reference pin can be obtained from the ADS8881 simulation model
Reference Driver Selection	Choose **OPA313**, an operational amplifier that is low power but has enough bandwidth (1MHz) to re-charge C_{ref1} and has enough capacitive load drive (stable up to 1nF) translates to less series isolation resistance (R_{ref1}).
Reference Driver Isolation Resistor (R_{ref1})	Using Equation 14, we use f_{sample} = 10ksps, C_{ref1} = 22 µF to calculate **R_{ref1} ≥ 4Ω. Choose closest standard value of 4.7Ω.**

3.6 Post Gain (INA) Low Pass Filter

The primary purpose of having this simple, first order low pass filter following the INA gain stage is to reduce the noise to a level that is statistically insignificant compared to the ADC driver, input driver, and reference driver circuitry. To accomplish this it is again necessary to appeal to equations 21-25. A summary is given below in

Table 8.

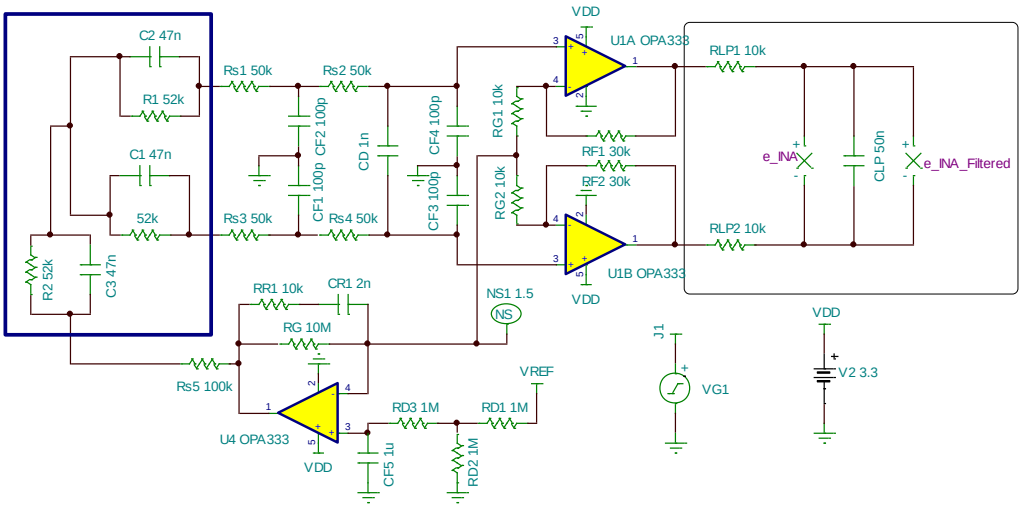

Figure 21: Post Gain Filter Component Selection Diagram

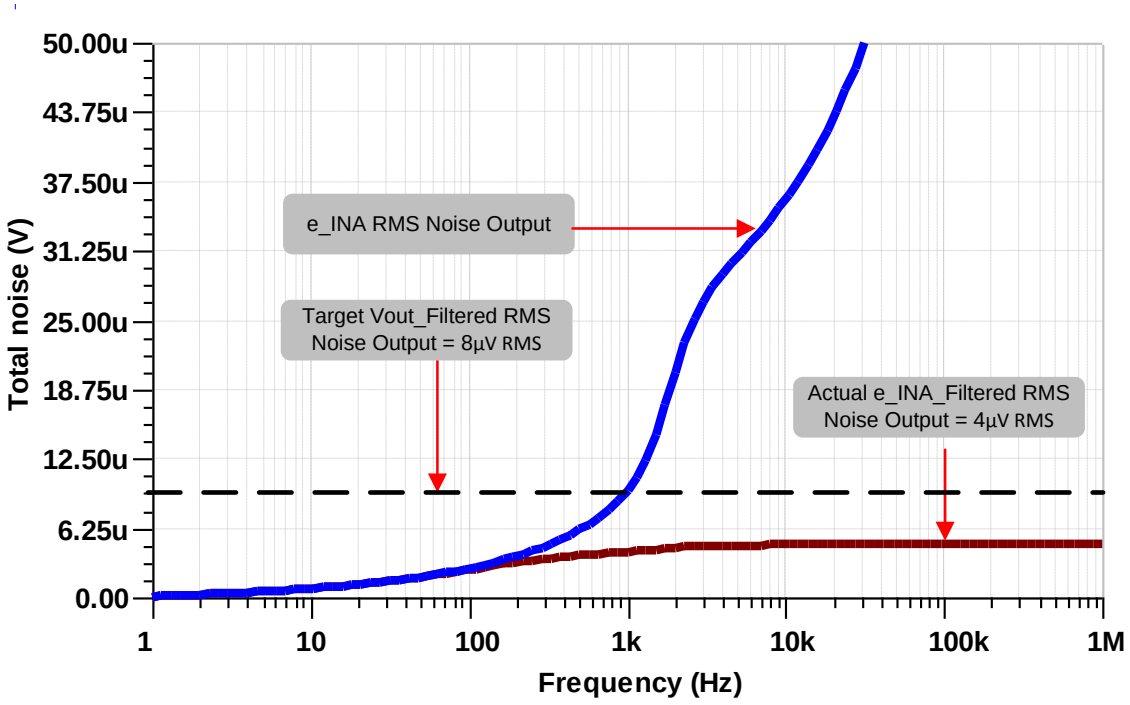

Figure 22: Filtered RMS Noise Plots from INA

Table 8: Component Selection Table for Post Gain Low Pass Filter

Parameters	Notes
Determine Filtered RMS value of INA front end ($e_{INA\_filtered}$)	Use equation 21 (root-sum-square of INA noise and ADC driver noise); using equation 22 solve for $\mathbf{e_{INA\_filtered}}$ = e_{ADC} / 3 = 25µVRMS / 3 = **8µVRMS**
Determine R_{LP1}, R_{LP2}, and C_{LP} using TINA SPICE parametric sweep	Choose **RLP1 = RLP2 = 10kΩ** and solve for C_{LP} using TINA SPICE to yield $e_{INA\_filtered}$ ≤ 8µVRMS (see Figure 22), $\mathbf{C_{LP}}$ **= 50nF** yields $e_{INA\_filtered}$ = 4 µVRMS for margin on the design

4 Simulations

4.1 Setting up the ECG Transient Simulation

To create an ECG voltage source first select an AC voltage source and choose the signal type to be "piecewise linear."

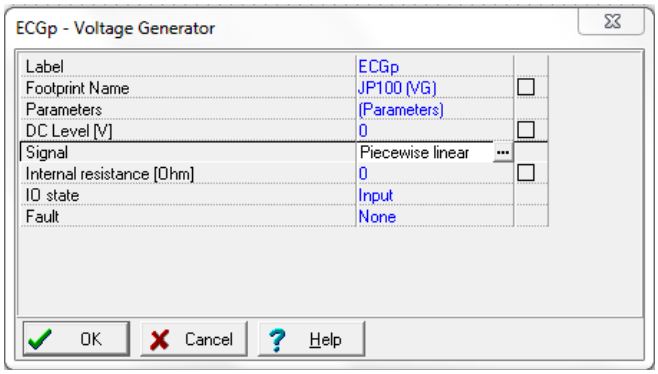

Figure 23: Step 1: Creating the ECG Voltage Source

Next, create the desired ECG signal in a spread sheet and copy and paste into the source by clicking on the 3 dots on the piecewise linear source. Use the following as a starting point:

```
REPEAT FOREVER
0      0
0.008                   0.000015
0.016                   0.00004
0.024                   0.000055
0.032                   0.00007
0.04 0.000075
0.048                   0.00007
0.056                   0.000055
0.064                   0.00004
0.072                   0.000025
0.08 0.00001
0.088                   0
0.096                   0
0.104                   0
0.112                   0
0.12 0
0.128                   0
0.136                   0
0.144                   0
0.152                   0
0.16 0
0.17 -0.000015
0.18 -0.00003
0.19 -0.000045
0.215                   0.00075
0.23 -0.00015
0.245                   0
0.385                   0
0.403                   0.000015
0.421                   0.00005
0.439                   0.00008
0.457                   0.000095
0.475                   0.0001
0.493                   0.000095
0.511                   0.00008
0.529                   0.00005
0.547                   0.000015
0.565                   0
0.605                   0
0.615                   0.0000075
0.625                   0.000015
0.635                   0.0000075
0.645                   0
0.725                   0
ENDREPEAT
```

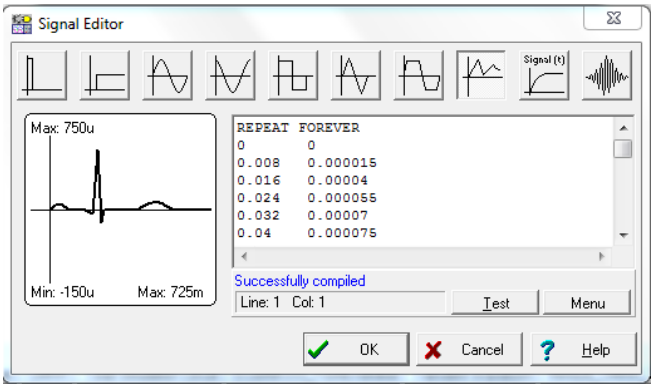

Figure 24: Step 2: Creating the ECG Voltage Source

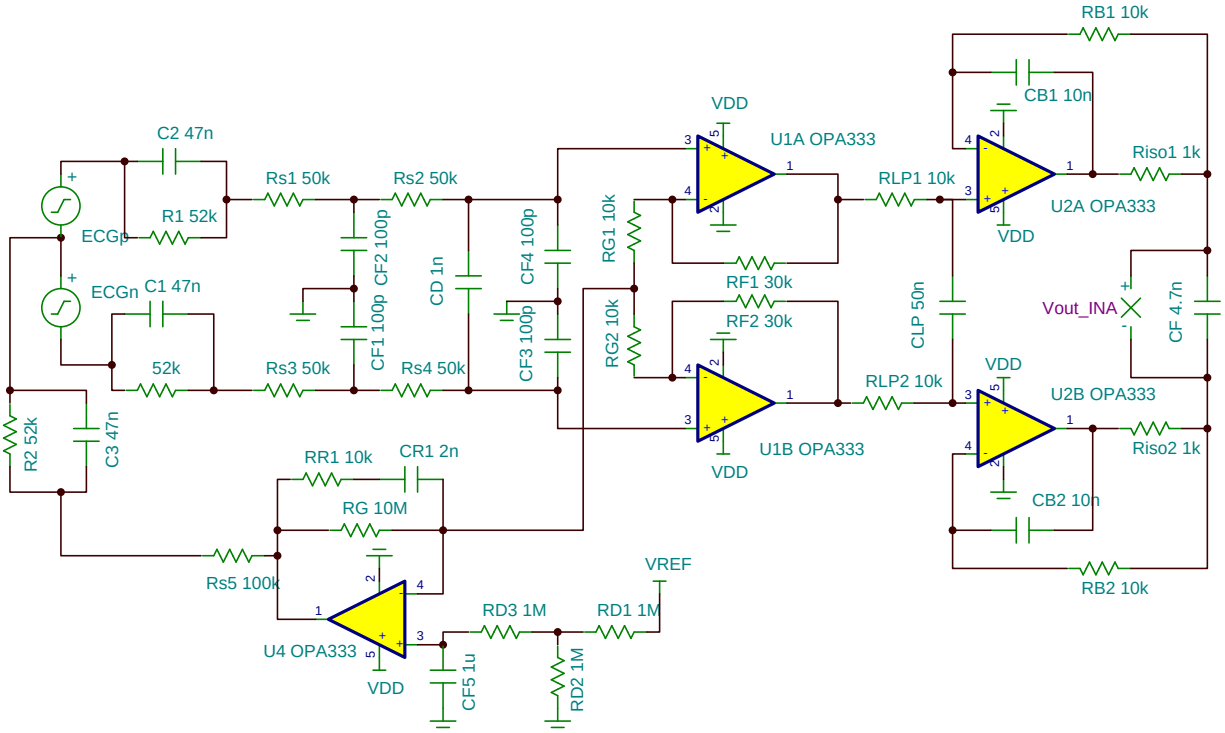

Figure 25: Transient ECG Simulation Circuit

Finally, here is a transient check on the ECG signals:

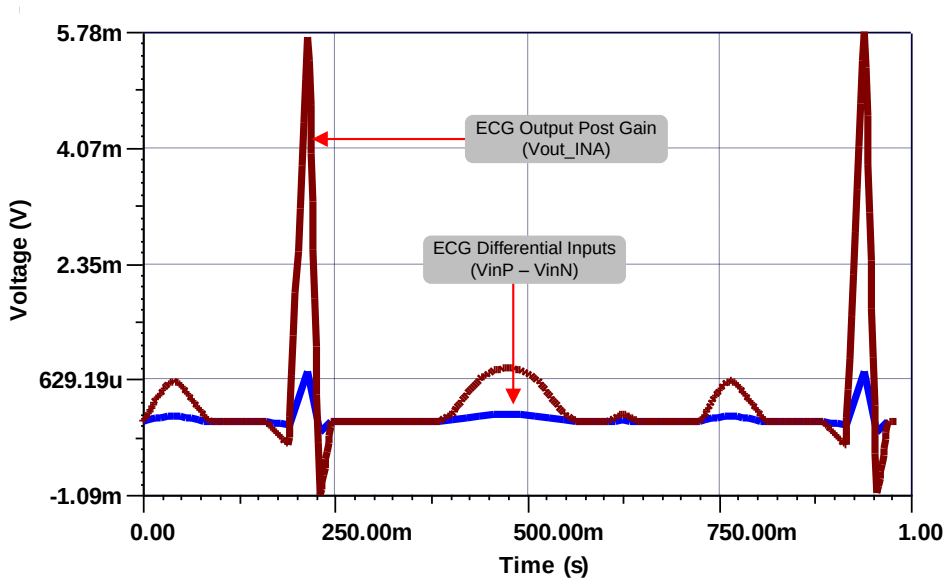

Figure 26: ECG Outputs, Pre and Post Gain

4.2 Simulating Common Mode Rejection Ratio (Front End Only) vs. Frequency

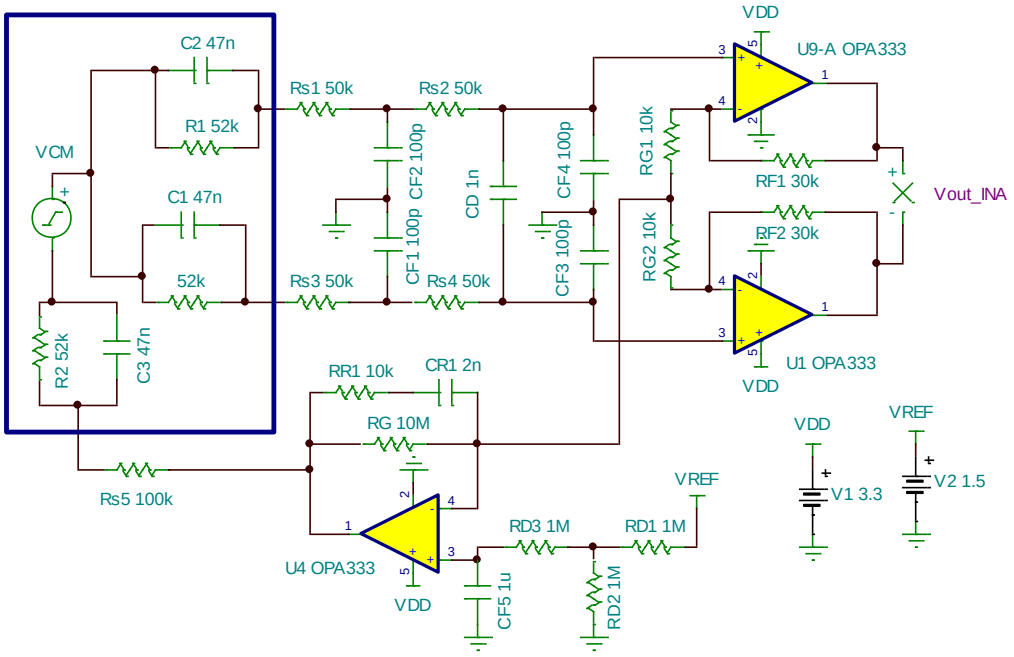

Figure 27: CMRR vs. Frequency Simulation Circuit

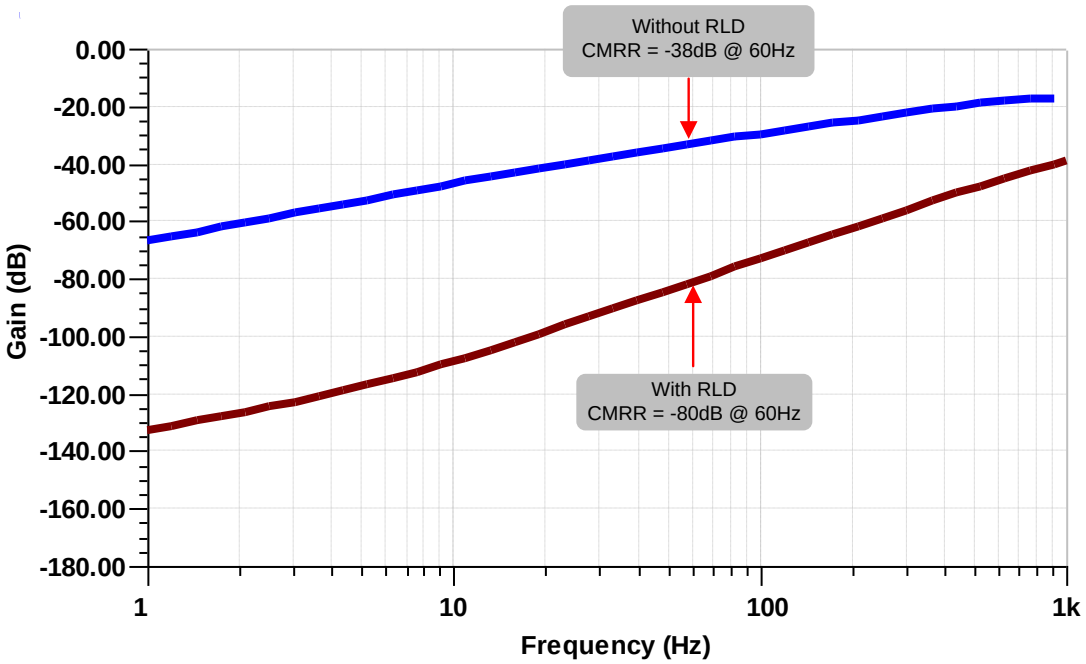

Figure 28: CMRR plots, with and without Right Leg Drive

Table 9: Table Summary of Simulation Results and Comments

Simulated Parameter	Comments
Power Consumption (mW)	Use Current Probe in series with VDD, use ADC specified power =55µW @ 10ksps, **P_D = 550µW**
Common Mode Rejection Ratio (dB) (CMRR @ 60Hz)	With perfect resistors, **CMRR = -80dB**

5 PCB Design / Layout

There are five key points that need to be considered in the PCB layout of this ECG system:

(1) Traces from the buffered, voltage reference (OPA313, U10) must be minimized to minimize trace inductance that can cause instability.
(2) Locate the Input Drive Circuitry (OPA2333, U2) as close as possible to the inputs to minimize loop area, thereby making a better layout for EMI/RFI rejection
(3) Minimize the loop area on the input RC filters (keep close together) and as close as possible to the input INA (OPA2333, U1) to minimize EMI/RFI susceptibility
(4) Ensure that traces coming from ECG signal source (i.e. body) are symmetric and do not have any sharp turns
(5) If possible leave the ground plane open underneath the summing node on the INA (OPA2333, U1). Added capacitance on this node can cause instability

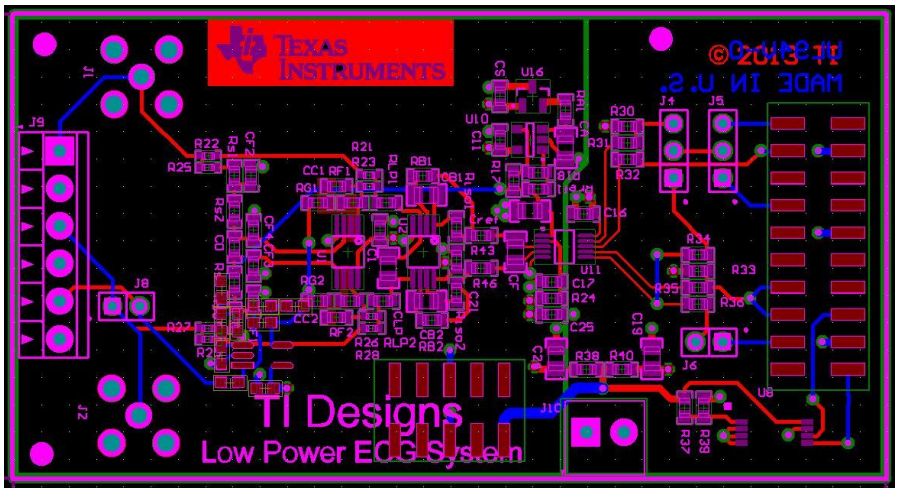

Figure 29: PCB Layout

6 Verification & Measured Performance

Measuring ECG system performance requires a very accurate signal source, clock generator, and synchronous measurement for coherent sampling. All measured data was taken using the setup depicted in Figure 30.

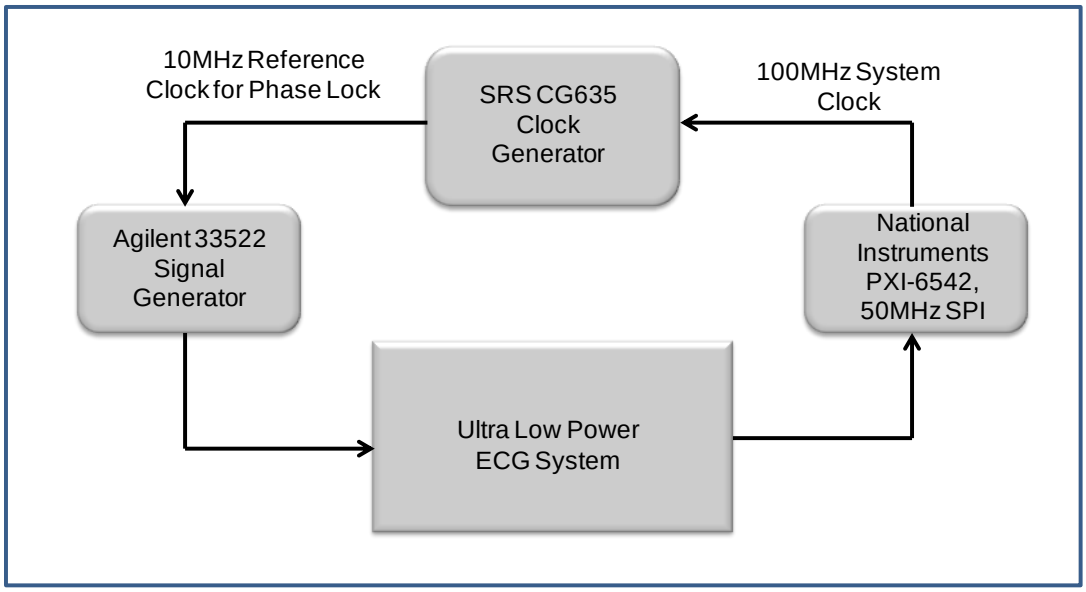

Figure 30: Precision Measurement Setup for ECG Low Power System

6.1 DC Histogram Test for RMS Noise

DC RMS noise was tested by shorting the inputs together with the right leg drive amplifier connected. The mean output code (MOC) represents the DC offset and the standard deviation gives the code spread of the noise. These quantities can then be converted into VRMS by multiplying by the LSB of the ADC (22µV). The DC histogram is shown in Figure 31and the table summary of measured values is shown in Table 10.

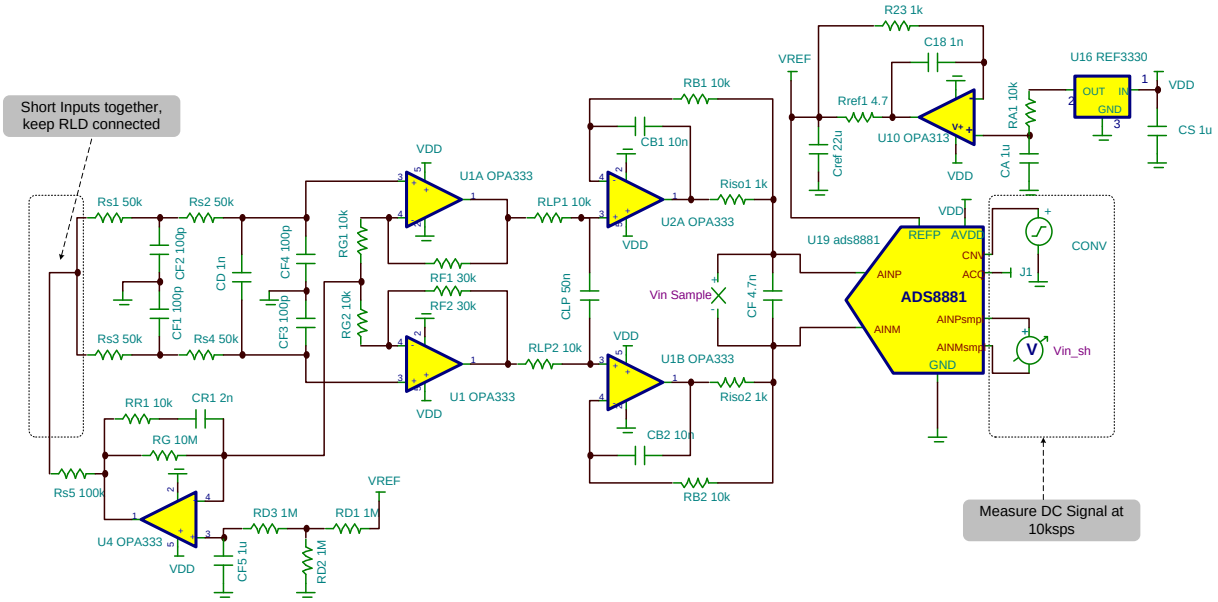

Figure 31: DC Histogram Test Circuit with Mid Scale Bias (1.5V)

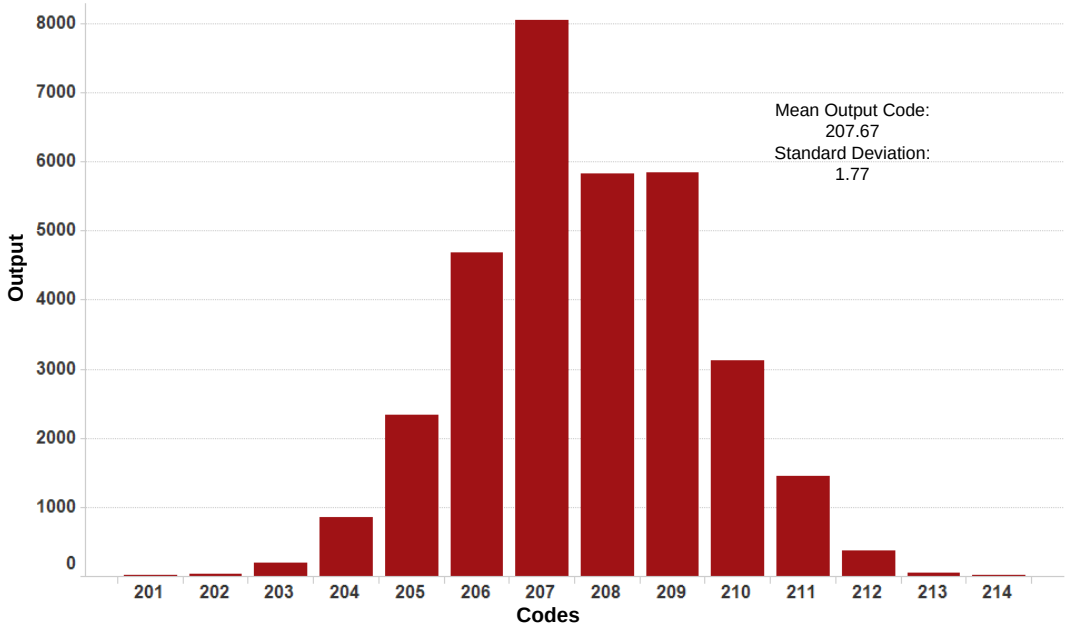

Figure 32: Measurement Data Showing DC Histogram with RLD Bias = 1.5V (mid scale)

The ADC LSB for the ADS8881 (18 bit) is calculated as follows:

$$ADC_{LSB} = \frac{2 \bullet V_{REF}}{2^{n} - 1} = \frac{6V}{2^{18} - 1} = 22.8\mu V \quad (32)$$

Conversion of mean output code (MOC) into VRMS:

$$V_{Offset} = MOC \bullet ADC_{LSB} \quad (33)$$

Conversion of standard deviation into VRMS:

$$e_{RMS} = \sigma \bullet ADC_{LSB} \quad (34)$$

Conversion of V_{offset} to Input-Referred Offset (V_{OS_Input}):

$$V_{OS\_Input} = \frac{V_{Offset}}{Gain} \quad (35)$$

See Table 10 for a summary of verified results:

Table 10: Summary of DC Offset and Noise Results

Parameter	Units	Goal	Measured	Simulated
Mean Output Code (MOC)	*	*	**207**	*
Output Offset Voltage	V	*	**4.55mV**	*
RMS Noise (DC)	µV RMS	**40**	**38.7**	*
Input-Referred Noise (DC)	µV RMS	**11.5**	**9.68**	**4**

6.2 SNR Test at 100Hz

Using equation 8, the measured SNR can be used to calculate the RMS noise at 100Hz:

$$SNR(dB) = 20\log_{10}\left(\frac{3V/\sqrt{2}}{e_{ADC}}\right) \quad (36)$$

Using equation 9, the RMS noise of the ADC at 100Hz can be calculated:

$$e_{ADC} = \frac{3V}{\sqrt{2} \bullet \left(10^{92/20}\right)} = 52\mu V \quad (37)$$

Table 11: Summary of Noise Test Results

Parameter	Units	Goal	Measured	Simulated
RMS Noise (100Hz)	µV RMS	**60**	**52**	*
Input-Referred Noise (100Hz)	µV RMS	**15**	**13**	**10**
Signal-to-Noise Ratio (SNR @ 100Hz)	dB	**90**	**89.9**	*

6.3 CMRR Test (60Hz) with RLD Connected

CMRR is measured by connecting a 1Vpp, 60Hz common mode input signal with the differential inputs shorted together (Figure 33) and sampling the ADS8881 at 10ksps. The test circuit for CMRR is shown in Figure 33—note that the input source in inserted in line with the RLD amplifier.

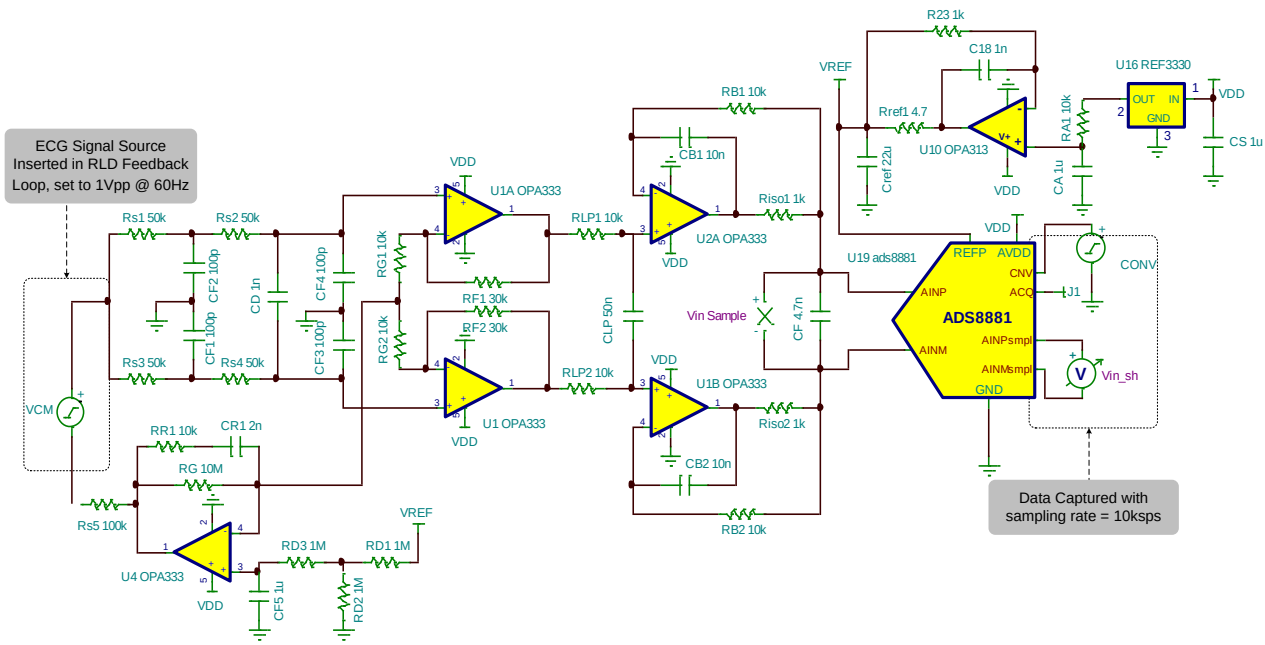

Figure 33: CMRR Test Circuit with RLD Connected

The histogram in Figure 34 shows the measured code spread using the test circuit in Figure 33. The "Std Dev" quantity σRMS is used to calculate the change in input-referred offset voltage (VOS) used to calculate CMRR.

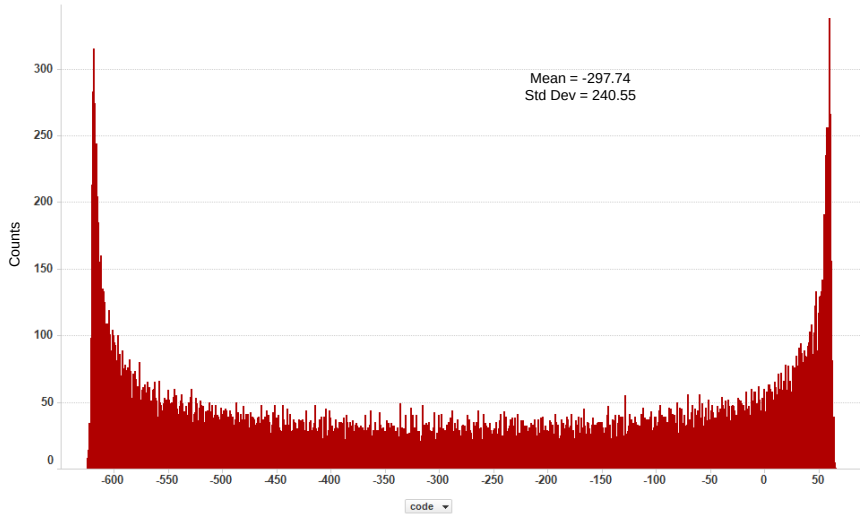

Figure 34: Code Spread of 1Vpp, 60Hz with RLD Drive Connected

The change in offset voltage, divided by the gain produces the input referred (RMS) offset voltage:

$$\Delta V_{OS} = \frac{\sigma_{RMS}}{Gain} = \frac{(240.55) \bullet 22.8\mu V}{4} = 1.37mV \tag{38}$$

The peak-to-peak input signal must be converted into VRMS:

$$\Delta V_{CM}(RMS) = \frac{Vin_{pp}}{2\sqrt{2}} = \frac{1V_{pp}}{2\sqrt{2}} = .3535V \tag{39}$$

Now CMRR can be calculated:

$$CMRR_{60Hz}(dB) = -20\log_{10}\left(\frac{\Delta V_{CM}}{\Delta V_{OS}}\right) \tag{40}$$

$$CMRR_{60Hz}(dB) = -48.2dB \tag{41}$$

6.4 CMRR Test (60Hz) with NO RLD Connected

For qualitative purposes, CMRR was also tested with the RLD disconnected as shown in Figure 35:

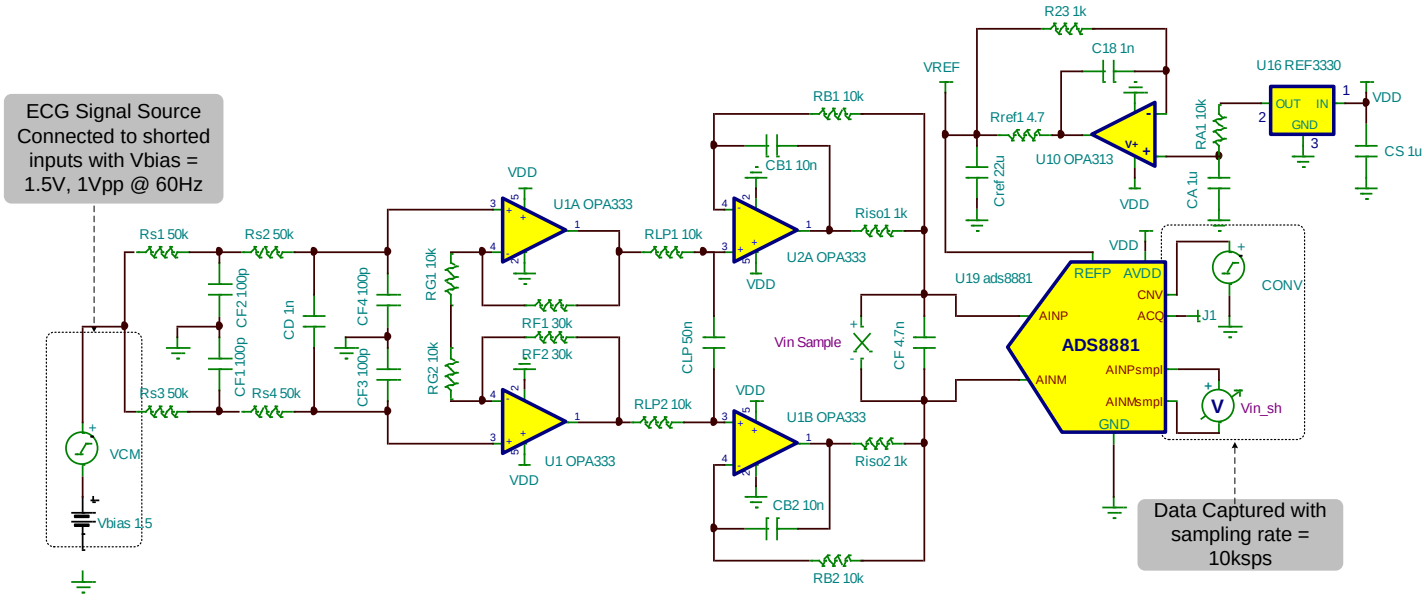

Figure 35: CMRR Test Circuit with no RLD

The resulting histogram shows an even larger standard deviation which indicates a further degradation in CMRR (see Figure 36).

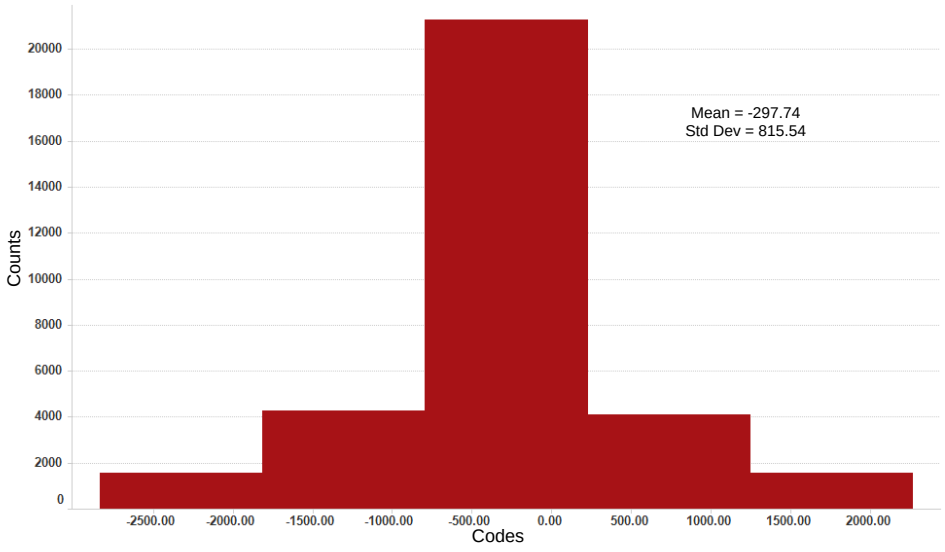

Figure 36: Code Spread of CMRR Test (1Vpp @ 60Hz) No RLD

$$CMRR_{60Hz}(dB) = -37.62dB \quad (42)$$

6.5 Improvement in the CMRR Test

In this design all calculations have not taken into consideration the tolerance of the discrete resistors used in the front end gain of the differential output INA. In reality, the discrete tolerance can add a significant amount of error due to variations in common mode, and this can be seen through the following analysis:

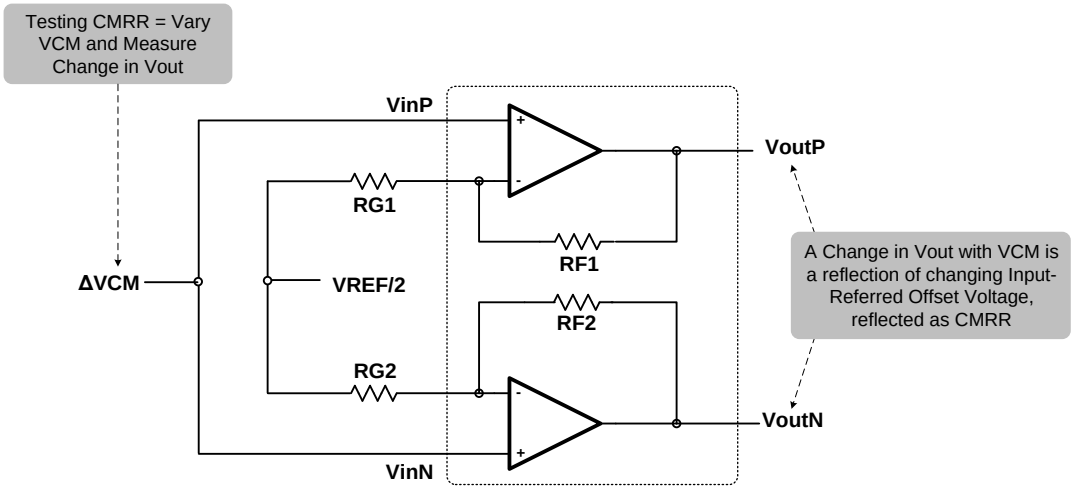

Figure 37: Simplified Diagram of Front End INA Showing Resistor Matching

Based on Figure 37, the transfer function one of the single-ended amplifiers is the following:

$$V_{outP} = \left(\Delta V_{cm} - V_{REF/2}\right) \bullet \frac{R_{F1}}{R_{G1}} + \Delta V_{cm} \tag{43}$$

$$V_{outN} = \left(\Delta V_{cm} - V_{REF/2}\right) \bullet \frac{R_{F2}}{R_{G2}} + \Delta V_{cm} \tag{44}$$

If $R_{F1} = R_{F2}$ and $R_{G1} = R_{G2}$, then all of the CMRR error will be a result of the inherent CMRR of the 2 amplifiers. The easiest way to analyze the effect of the mismatch error is through a Monte Carlo analysis in TINA-TI™ SPICE. Figure xx shows the test circuit used to perform the CMRR simulation; each resistor is initially set with a tolerance of 1%, a population size of 1000, and will have a Gaussian distribution.

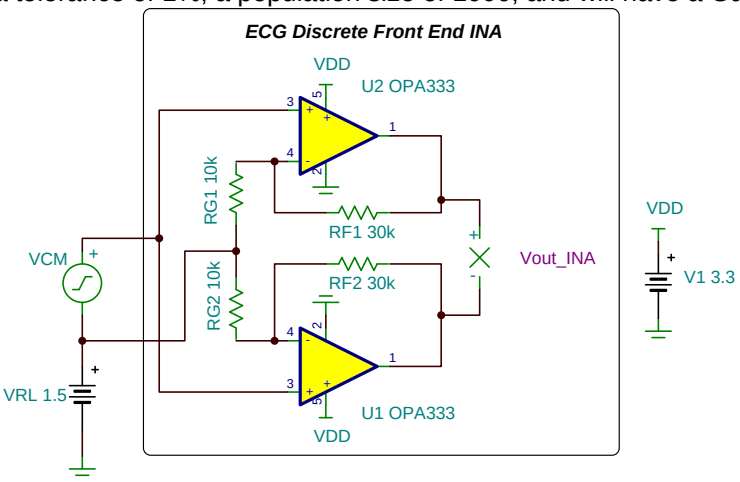

Figure 38: CMRR Resistor Mismatch Simulation Circuit

It is clear from Figure 39 that even 1% mismatch in these resistors can dramatically degrade the CMRR, which in this case has a mean of -29.9dB! This mismatch is responsible for the majority of the loss in CMRR; therefore, if resistors with improved tolerance are used this will make a significant impact on the CMRR of the entire ECG signal chain.

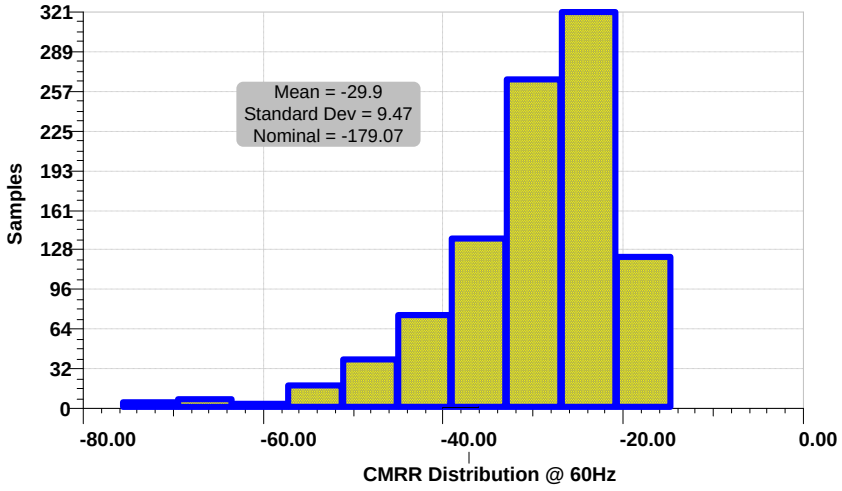

Figure 39: Monte Carlo Analysis of 1% Resistor Tolerance for R_{F1}, R_{F2}, R_{G1}, R_{G2}

One simple modification that can make a huge impact on CMRR is to decrease the tolerance R_{F1}, R_{F2}, R_{G1}, and R_{G2} from 1% to .01%. The new CMRR distribution can be seen in Figure 40 if .01% tolerances are used. With this improvement in resistor tolerance, achieving the goal of -70dB CMRR is much more realistic. Table 12 summarizes the CMRR with different gain setting resistor tolerances.

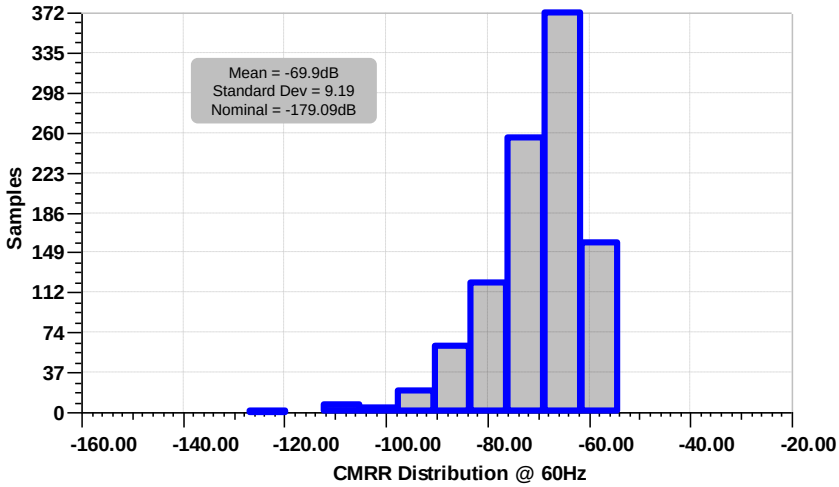

Figure 40: Monte Carlo Analysis for .01% Resistor Tolerance for R_{F1}, R_{F2}, R_{G1}, R_{G2}

With the replacement of the 1% resistors with resistors with “perfect” matching, the circuit in Figure 33 was used with a 1Vpp, 60Hz signal to test for CMRR. Because the noise reduction was so drastic, to extract the SNR it was necessary to use the FFT (showing a –SNR indicated that the actual power in the common mode input signal was smaller than the noise floor) to back calculate the CMRR.

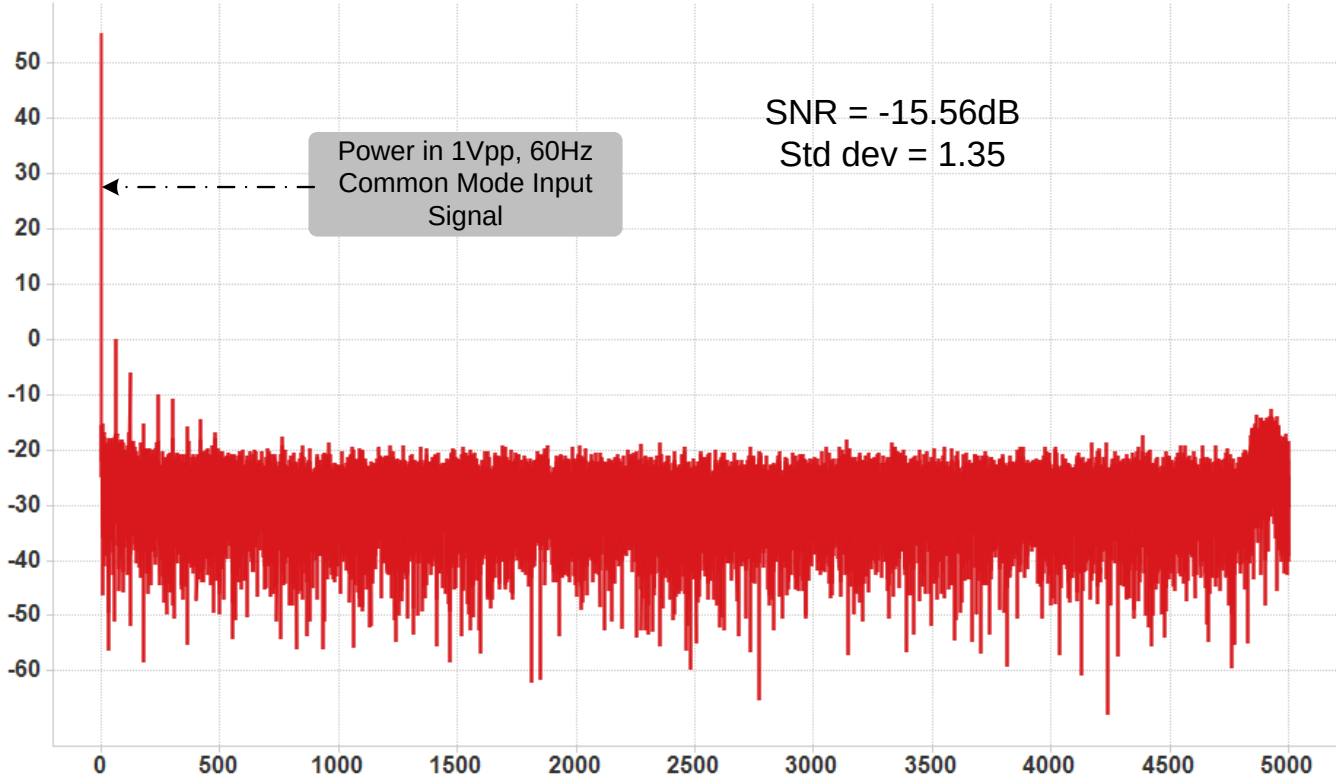

Figure 41: FFT Showing 1Vpp, 60Hz Common Mode Noise Power

Using the standard deviation from Figure 41, equation 34, and the LSB = 22.8µV established by equation 32, the RMS noise floor can be calculated:

$$e_{RMS} = \sigma \bullet ADC_{LSB} = 1.35 \bullet 22.8\mu V = 30.9\mu VRMS \quad (45)$$

Using the number for e_{RMS} from equation 45, the actual RMS noise power can be extracted using the SNR from Figure 41 by substituting into equation 36:

$$e_{RMS} = \sigma \bullet ADC_{LSB} = 1.35 \bullet 22.8\mu V = 30.9\mu VRMS \quad (46)$$

Using this value for RMS noise, the following equation is used to extract the signal magnitude in RMS:

$$SNR(dB) = 20\log_{10}\left(\frac{\Delta VOS_{60Hz}}{e_{RMS}}\right) \quad (47)$$

Rearranging equation 47 and referring to the input (i.e. dividing by gain = 4):

$$\Delta VOS_{60Hz} = \frac{e_{RMS} \bullet \left(10^{\frac{SNR(dB)}{20}}\right)}{Gain} = 1.28\mu VRMS \quad (48)$$

Using the results from equation 46 and 48, the CMRR can now be calculated:

$$CMRR(dB) = 20\log_{10}\left(\frac{\Delta VOS_{60Hz}}{Vin_{60Hz}}\right) = -108dB \quad (49)$$

Table 12: Table of CMRR Measurement Results with Different Gain Resistor Tolerances

Parameter	Units	Goal	Measured	Simulated
CMRR (60Hz), Perfect Matching	dB	**-90**	**-108**	**-80**
CMRR (60Hz), .01% Matching	dB	**-70**	**-67**	**-69**
CMRR (60Hz), 1% Matching	dB	*****	**-48.2**	**-35**

7 Modifications:

7.1 Monolithic INA Option

One circuit modification that could make life easier would be to choose a discrete monolithic INA for the front end such as the INA333. Such a device is manufactured with precision trimmed resistors internally, so the only external components needed are R_{G1} and R_{G2}. The compromise to using this INA is that it converts differential input signals to single-ended, meaning that the output could be more easily subject to external noise coupling which could be more easily rejected in a differential configuration. Lastly, the INA333 requires a reference buffer to offset the single-ended output to mid scale.

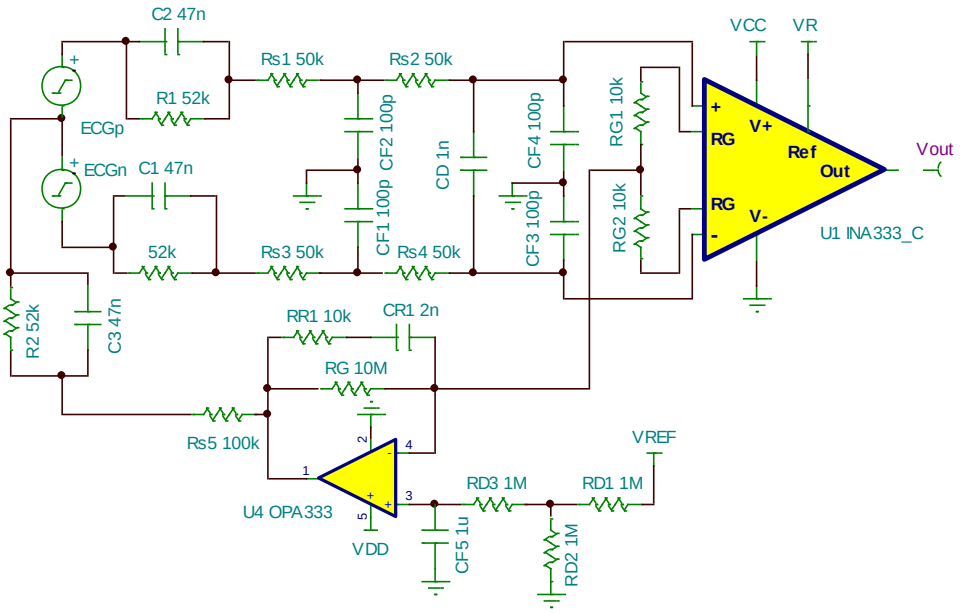

Figure 42: Modified ECG Front End with INA333

7.2 Integrated, Multi-Channel ECG Data Acquisition System (DAS) Option

The discrete approach offers the ability to customize power, sampling, and filtering based a fixed set of system requirements. One alternative that can greatly simplify the design process of an ECG data acquisition system is to use the ADS1292. The ADS129x family of devices offers an integrated front end PGA, RL drive amplifier, internal test functions, lead off detection, and a 24 bit data converter. Table 13 lists configuration options in the ADS129x family:

Table 13: ECG DAS Device List

Device	Resolution (Bits)	Sample Rate (max)(SPS)	# Input Channels	Power (Typ) (mW)
ADS1291	24	8kSPS	1	0.35
ADS1292	24	8kSPS	2	0.7
ADS1294	24	32kSPS	4	3
ADS1293	24	25.6kSPS	3	0.9
ADS1296	24	32kSPS	6	5.3
ADS1296R	24	32kSPS	6	5.3
ADS1298	24	32kSPS	8	6
ADS1298R	24	32kSPS	8	6
ADS1299	24	15kSPS	8	40
ADS1191	16	8kSPS	1	0.335
ADS1192	16	8kSPS	2	0.67
ADS1194	16	8kSPS	4	3
ADS1196	16	8kSPS	6	3.6
ADS1198	16	8kSPS	8	4.3

For low power precision systems such as ECG, power is always a prime consideration. Listed below are some options that could be used in a low power, single supply data acquisition system.

Table 14: Low Power LDO Options for ECG System

Device	Iq (µA)	I_{out}(mA)	V_{in}(V)	Package(s)	Features
TPS797xx	1.2	50	1.8-5.5	5SC70	Power Good Output, Low Dropout (105mV)
LP5900	25	150	2.2-5.5	4DSBGA, 6WSON	Low noise (6.5uVRMS), Low Dropout (80mV), 2% accuracy over line/load
TPS780/2	0.5	150	2.2-5.5	5SOT-23, 6SON	3% accuracy over line/load/temp, 2x2mm package, dual-level output voltage
LP5907	12	250	2.2-5.5	4DSBGA, 4X2SON, 5SOT-23	1x1mm package, Low Noise (<10uVRMS), Low Dropout (120mV), 2% accuracy over line/load
TPS727xx	7.9	250	2.0-5.5	6SON, 4DSBGA	2% accuracy over line/load/temp, Low Dropout (163mV), Excellent Load Transient Performance

8 About the Author

Matthew Hann is currently the Product Line Manager for the Precision SAR ADC team within Texas Instruments' Precision Analog Business Unit. Matt started his career at Burr Brown in 1998 and spent 8 years as an analog test engineer focusing on precision op amp, instrumentation amp, current shunt monitor, and power amplifier test solutions. Following that, Matt spent 5 years as an analog applications engineer focusing on front end instrumentation, power amplifier drivers, temperature sensing, 4-20mA transmitters, thermal control loops, and medical instrumentation applications.

9 Acknowledgements & References

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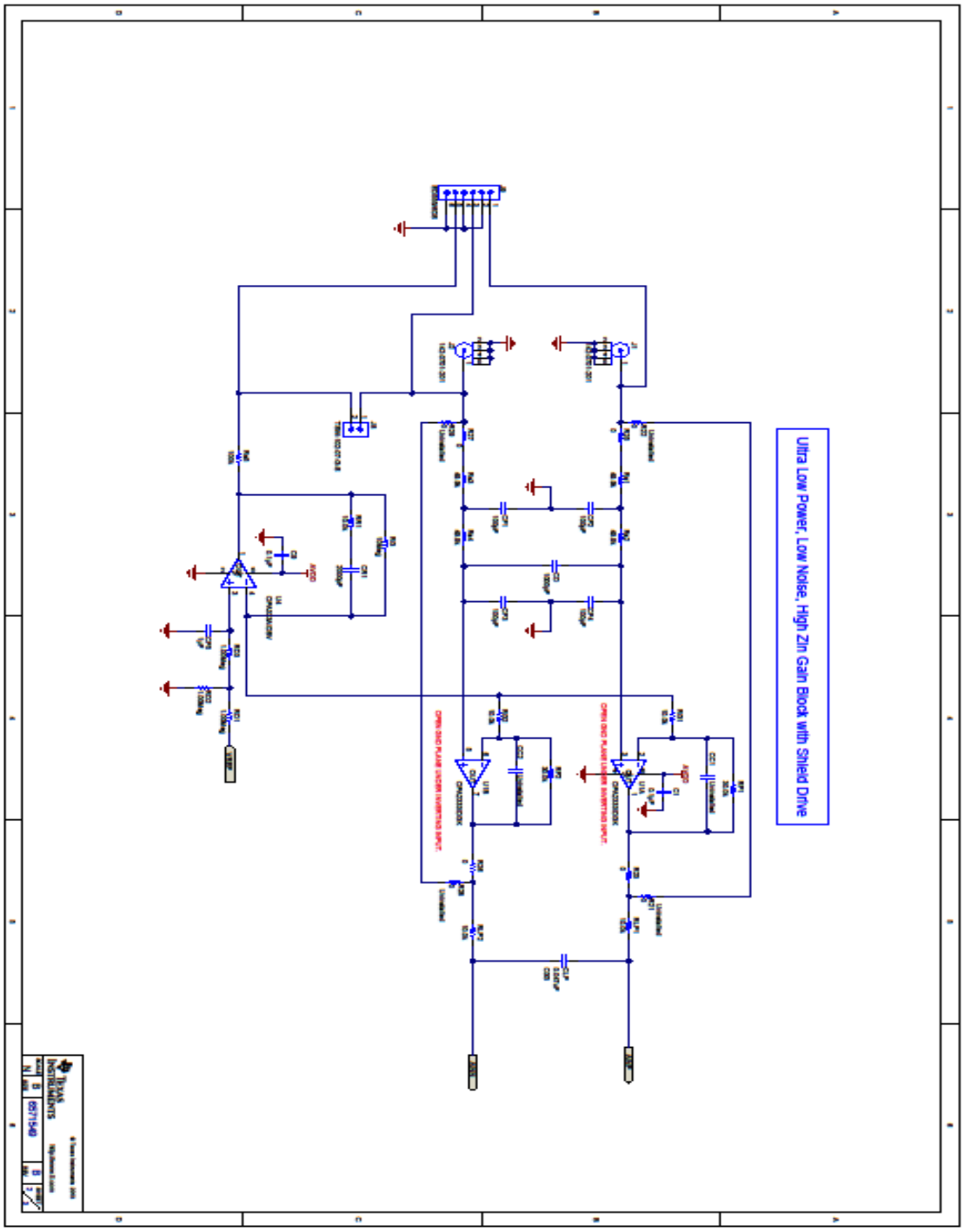
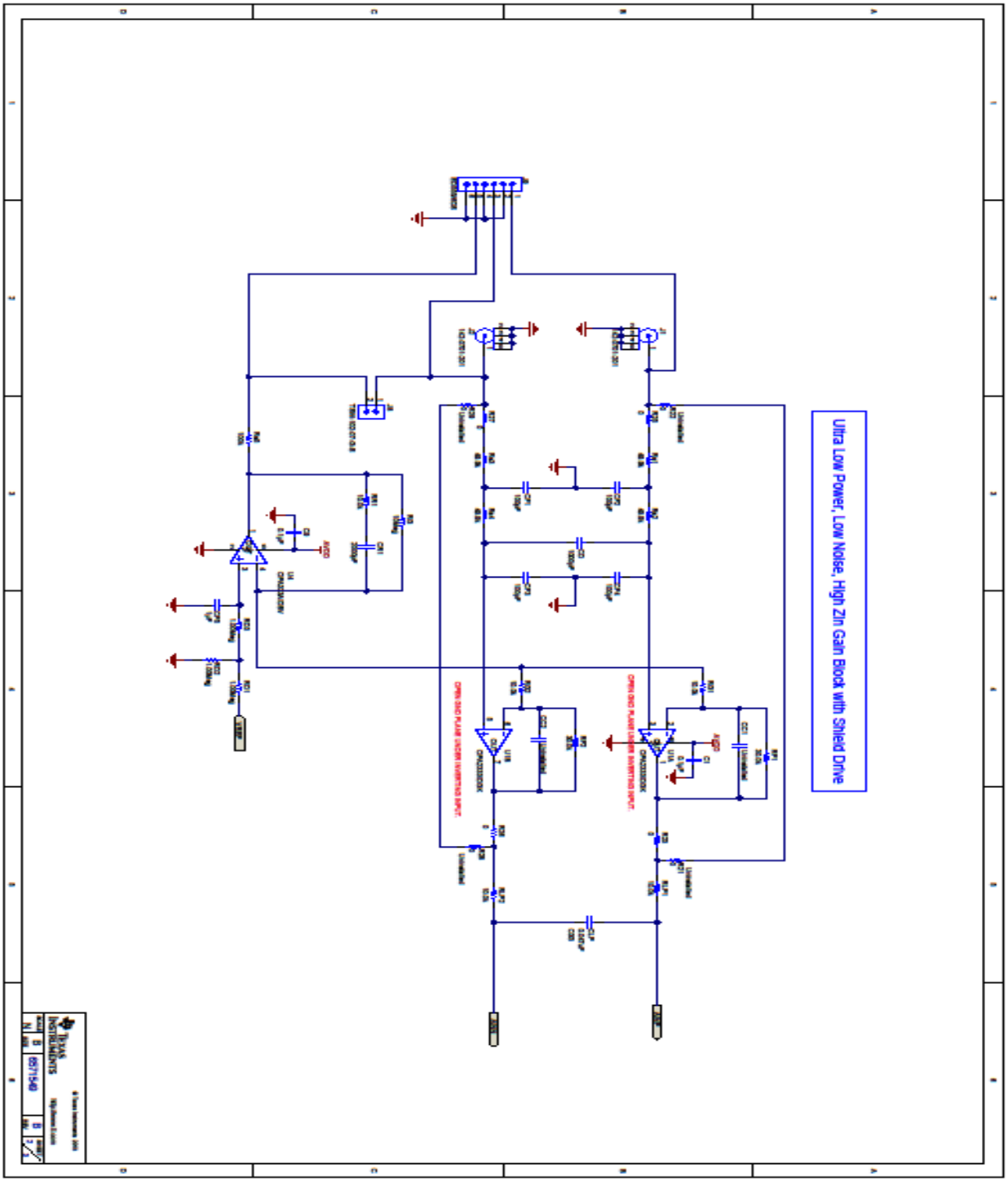
Ordonez, Rafael for his extensive help with measurements.

Appendix A.

A.1 Electrical Schematics





A.2 Bill of Materials

Drawing Type	BILL OF MATERIALS
Drawing Title	EVM,TI DESIGNS FORLOW POWER ECG SYSTEM
Drawing Number	6571549
Revision	B
Data Class	TI INTERNAL DATA
Engineer	TI SAR ADC ENGR
Released By	B McKay
Release date	05/30/2013

NOTE: ASTERISK(*) NEXT TO PART MANUFACTURER'S NAME DENOTES POSSIBLE LONG LEAD TIME ITEM.

ITEM	QTY	MFG	MFG PART#	REF DES	DESCRIPTION	VALUE or FUNCTION
		TBD by TI (TURNKEY)				
	REF	TBD by TI	6571549B	-	ASSEMBLY	-
	REF	-	6571549B	-	SCHEMATIC	-
	1	TBD by TI	6571549B	-	FABRICATION	-
	REF	-	6571549B	-	ARTWORK	-
1	2	Emerson Network Power	142-0701-201	J1, J2	Connector, TH, SMA	
2	1	Samtec, Inc.	SSW-105-22-F-D-VS-K	J7	Connector, Header, 10-Pos (10x2), Receptacle, 100x100-mil Pitch	
3	1	Samtec, Inc.	SSW-110-22-F-D-VS-K	J3	Connector, Receptacle, 100mil, 10x2, Gold plated, SMD	
4	1	On-Shore Technology, Inc.	ED555/6DS	J9	Terminal Block, 6A, 3.5mm Pitch, 6-Pos, TH	
5	2	Samtec, Inc.	TSW-103-07-G-S	J4, J5	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	
6	2	Samtec, Inc.	TSW-102-07-G-S	J6, J8	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	
7	1	On-Shore Technology, Inc.	ED555/2DS	J10	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	
8	1	Kemet	C0805C473J3GACTU	CLP	CAP, 0.047uF, 0805, C0G	
9	1	Kemet	C0603C102J5GAC	CD	CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603	
10	2	MuRata	GRM2195C1H103JA01D	CB1, CB2	CAP, CERM, 0.01uF, 50V, +/-5%, C0G/NP0, 0805	
11	1	TDK	C2012X5R0J226M	Cref	CAP, CERM, 22uF, 6.3V, +/-20%, X5R, 0805	
12	2	Kemet	C0805C106K8PACTU	C19, C24	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	
13	1	TDK	C2012C0G1E472J	CF	CAP, CERM, 4700pF, 25V, +/-5%, C0G/NP0, 0805	
14	1	Taiyo Yuden	EMK212B7105KG-T	CA	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0805	
15	1	TDK	C1608C0G1H102J	C17	CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603	
16	1	Vishay-Dale	CRCW060310R0FKEA	R24	RES, 10.0 ohm, 1%, 0.1W, 0603	
17	1	Vishay-Dale	CRCW0603100KFKEA	Rs5	RES, 100k ohm, 1%, 0.1W, 0603	
18	1	Vishay-Dale	CRCW060310M0JNEA	RG	RES, 10Meg ohm, 5%, 0.1W, 0603	
19	4	TDK	C1608X7R1C105K	C16, C25, CF5, CS	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	
20	2	Vishay-Dale	CRCW06031R00FKEA	R38, Rref1	RES, 1.00 ohm, 1%, 0.1W, 0603	
21	3	Vishay-Dale	CRCW06031K00FKEA	R30, Riso1, Riso2	RES, 1.00k ohm, 1%, 0.1W, 0603	
22	3	Vishay-Dale	CRCW06031M00FKEA	RD1, RD2, RD3	RES, 1.00Meg ohm, 1%, 0.1W, 0603	
23	9	Vishay-Dale	CRCW060310K0FKEA	R33, RA1, RB1, RB2, RG1, RG2, RLP1, RLP2, RR1	RES, 10.0k ohm, 1%, 0.1W, 0603	
24	4	Vishay-Dale	CRCW060349K9FKEA	Rs1, Rs2, Rs3, Rs4	RES, 49.9k ohm, 1%, 0.1W, 0603	
25	5	Vishay-Dale	CRCW06030000Z0EA	R18, R35, R40, R43, R46	RES, 0 ohm, 5%, 0.1W, 0603	
26	5	Vishay-Dale	CRCW060347R0JNEA	R31, R32, R34, R36, R39	RES, 47 ohm, 5%, 0.1W, 0603	
27	4	AVX	06035A101JAT2A	CF1, CF2, CF3, CF4	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	
28	4	Panasonic	ERJ-2GE0R00X	R23, R25, R26, R27	RES, 0 ohm, 5%, 0.063W, 0402	
29	2	Yageo America	RC0603FR-0730KL	RF1, RF2	RES, 30.0k ohm, 1%, 0.1W, 0603	
30	1	Texas Instruments	OPA313	U10	1-MHz, Micro-Power, Low-Noise, RRIO,1.8-V CMOS OP AMP	
31	1	Texas Instruments	ADS8588	U11	18-bit 1MSPS SAR ADC	
32	1	Analog Devices	REF3330	U16	3.0V, 3.9uA, SC70-3, 30ppm/°C Drift VOLTAGE REFERENCE	
33	6	Kemet	C0603C104K5RACTU	C1, C9, C11, C21, CC1, CC2	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603, CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603, CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603, CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603, Uninstalled, Uninstalled	
34	1	MuRata	GRM188R71H202KA01D	CR1	CAP, CERM, 2000pF, 50V, +/-10%, X7R, 0603	
35	8	N/A, N/A, N/A, Vishay-Dale, N/A, N/A, N/A, N/A	N/A	FID1, FID2, FID3, R17, R21, R22, R28, R29	Fiducial mark. There is nothing to buy or mount., Fiducial mark. There is nothing to buy or mount., Fiducial mark. There is nothing to buy or mount., RES, 0 ohm, 5%, 0.1W, 0603, Uninstalled, Uninstalled, Uninstalled, Uninstalled	
36	2	TI	OPA2333IDGK	U1, U2	IC, 1.8V, microPOWER Op Amp Zero-Drift Series	
37	1	TI	OPA333AIDBV	U4	IC, 1.8V, microPower, CMOS Op Amp, Zerø-Drift Series	
38	1	Microchip	24xx256-I/ST	U8	IC, 256K CMOS Serial EEPROM	

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