TI Precision Designs: Verified Design 12 Bit 1 MSPS Single Supply Dual Channel Data Acquisition System for Optical Encoders in Motor Control Application

TEXAS INSTRUMENTS

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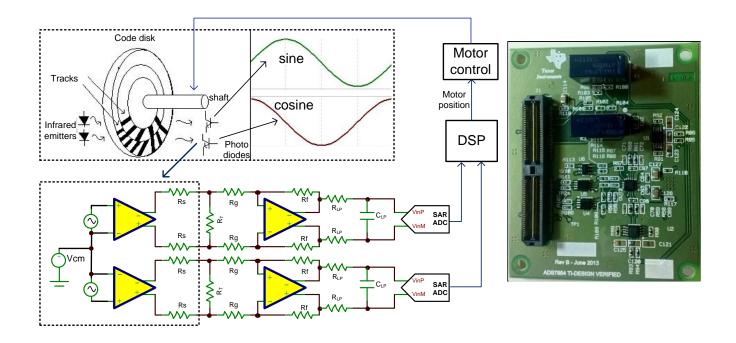
Circuit Description

This circuit describes a simultaneously sampling dual channel data acquisition system for optical encoders in motor control applications. Optical encoders provide sine and cosine outputs that represent the motor position. This circuit performs the signal conditioning and analog-to-digital conversion of both sensor outputs simultaneously. The differential sensor output is processed through a differential unity gain amplifier and low pass RC filter before being fed to a successive approximation register (SAR) analog-todigital converter (ADC).

Design Resources

Design Archive TINA-TI™ ADS7254 THS4531 All Design files SPICE Simulator Product Folder Product Folder





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1 Design Summary

- Supply Voltage: 5 V
- Input: ± 4.5 V differential voltage signal
- Output: 12-bit, 1 Mega Sample per second (MSPS) digital output
- Communication Protocol: 4-Wire SPI
- Clock: 32 MHz clock (SCLK)
- Chip Select: 1 MHz chip-select (CSZ) with 30 ns high-time
- Digital input: Serial digital input (SDI) pattern for device configuration

The design goals and performance are summarized in Table 1.

Table 1: Comparison of Design Goals, Simulation, and Measured Performance

Parameter	Goal	Simulation/estimation	Measured
Throughput (MSPS)	1	1	1
Resolution (bits)	12	12	12
SNR (dBFS) (2 kHz)	72	74	73.8
THD (dB) (2 kHz)	85	95	93.9
SINAD (dBFS) (2 kHz)	71.5	73.5	73.7
Supply current (mA)	15	13 (only amp & ADC)	16 (Total)

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Figure 1: Measured dynamic parameters

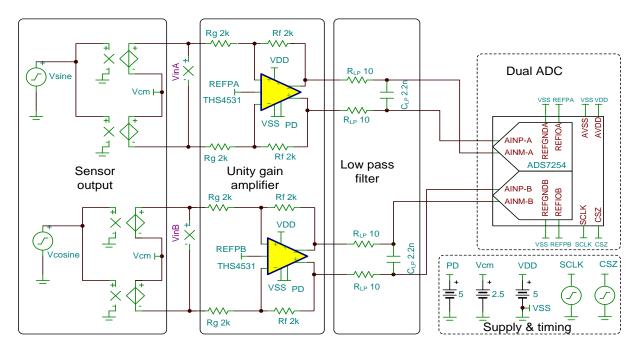


Figure 2: The dual channel data acquisition system

2 Theory of Operation



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2.1 Background on motor control system

Incremental encoders for servo drive applications generate sine and cosine voltages corresponding to the current position of a motor. In a typical position and speed control system, the encoder output is sampled by a SAR ADC and processed by a digital signal processing (DSP) system to determine the fine position of the motor. To determine the coarse position, a parallel pulse counter looks at the output of a comparator to count pulses per cycle of the motor. The overall resolution (R) of the motor position is defined by the ADC resolution (N) and the number of pulses per cycle. For an M-bit pulse counter, the effective resolution of the control system is given as:

$$Effective resolution = Pulse counter resolution (M) + ADC resolution (N)$$
(1)

The DSP computes a high resolution position from the pulse counter output and the ADC output data. This position information is fed to a motor control device in the feedback loop which controls the motor speed. Figure 3 shows a typical position control system. For more details about the encoder application see the encoder selection guide "Encoders for Servo Drives" [1].

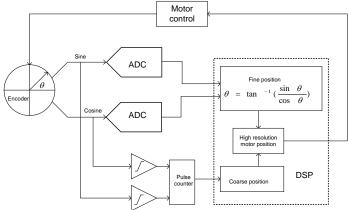
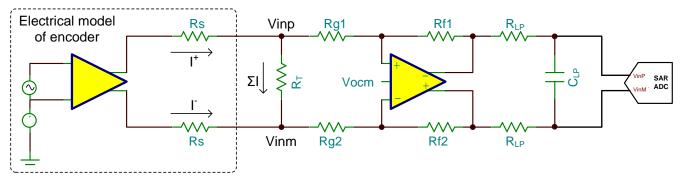


Figure 3: A typical Position Control System

2.2 Electrical model of the encoder

The encoder output can be considered as a differential voltage or current source with series impedance. The differential signal rides on a bias voltage called common mode voltage (Vcm). Figure 4 shows a typical encoder interface circuit with its electrical model. Typical peak to peak differential voltage is 1 V with a source impedance lesser than 100 Ω . Common mode voltages vary by ±0.5 V around 2.5 V. Maximum output current is about 1 mA. Signal frequency in these applications varies from few kHz to hundreds of kHz. A suitable termination resistance (R_T) is required for signal integrity at high frequency and to accommodate a current signal from the encoder.







2.3 Basics of SAR ADC

An analog-to-digital converter compares its input voltage to a reference voltage (V_{ref}) and generates a digital equivalent of the analog input. Figure 5 shows a simplified block diagram of a SAR ADC to highlight the basic signal integrity concerns. For a Differential ADC, the input ($V_{in-diff}$) and reference (V_{ref}) are defined as:

$$V_{in-diff} = V_{inP} - V_{inN} \tag{2}$$

$$V_{ref} = REFP - REFM \tag{3}$$

The differential input varies from V_{ref} to $-V_{ref}$ with a fixed common mode voltage (i.e. average voltage at ADC inputs). Digital output saturates at 0 and 2^{N} for negative and positive full scale inputs respectively. The ADC result, expressed as a digital output for a valid input voltage can be written as:

$$D_{out} = \frac{V_{in-diff}}{2*V_{ref}} * 2^N \tag{4}$$

The ADC samples the input voltage into a capacitor (C_{sample}) periodically and holds the same during conversion. It computes the digital output for the sampled voltage according to Equation 4. Typically, the sampling instance is controlled by the user through a timing signal called chip-select (CSZ). The conversion process requires a high speed clock to compute each bit serially within the specified conversion time.

The ADC input circuit presents a switched capacitor load to the output of the driver circuit. The sampling capacitor is connected to the analog input pin during sampling phase and remains isolated for the conversion phase, while the input signal charge during the conversion phase is preserved. The sampling capacitor requires incremental charges for each sample phase based on the deviation of the input signal from the previous sample. It also requires some extra charge to compensate for the charge injection of sampling switch. The on-resistance (R_{sw}) of the sampling switch varies with supply voltage, temperature and silicon process corner.

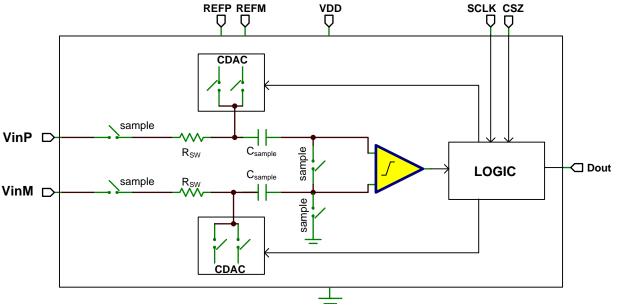


Figure 5: SAR ADC block diagram



2.4 Need for an amplifier

The output cannot be connected directly to the ADC because of several reasons like:

- Switched capacitor ADC input load.
- Different common mode voltage may degrade ADC performance.
- ADC cannot take a different type of signal like current or charge.

Thus, an amplifier is required to make the signal appropriate for the ADC. It may work as a simple low impedance buffer, a level translator, or an I-V converter. Typically, a fully differential amplifier (as shown in Figure 4) with independent common mode control (V_{ocm}) is used in a unity gain mode for this application. In most of the actual circuits, a low pass RC filter is used after the amplifier to reduce switching kickback from ADC and to help to reduce out of band noise from the signal chain. More details about the amplifier requirements are described in "Ultra Low Power, 18 bit Precision ECG Data Acquisition System" [2].

2.5 Effect of passive component mismatch

All feedback resistors (R_f) and gain resistors (R_g) shown in Figure 4 are expected to be equal to achieve unity gain. Any mismatch in real values of component lead to additional gain and offset error. Feedback factors for each side of the differential amplifier in Figure 4 can be expressed as:

$$\beta_1 = \frac{R_{f1}}{R_{f1} + R_{g1}} \tag{5}$$

$$\beta_2 = \frac{R_{f2}}{R_{f2} + R_{g2}} \tag{6}$$

Any mismatch between β_1 and β_2 results a differential signal at amplifier output depending on the desired output common mode. So differential output voltage becomes a function of individual input voltages (Vinp and Vinm in Figure 4) as well as desired output common mode voltage. The differential voltage at amplifier output can be given by:

$$V_{out-diff} = \left[\frac{2}{\beta_1 + \beta_2}\right] * \left[\frac{Vocm(\beta_1 - \beta_2) + Vinp(1 - \beta_1) - Vinm(1 - \beta_2)}{1 + \frac{2}{A(s)(\beta_1 + \beta_2)}}\right]$$
(7)

Here, A(s) is the gain bandwidth product of the amplifier. For $\beta_1 = \beta_2 = \beta$, Equation 7 simplifies to the well known form of a closed loop amplifier transfer function as in Equation 8. Interestingly, mismatch between R_g and R_f creates only offset and gain error with some extra noise. The offset and gain can be calibrated by channel calibration. Another source of error is impedance mismatch between the individual ADC input nodes. This mismatch leads to phase difference between complementary driver outputs which adds distortion at high frequency.

$$V_{out-diff} = \left[\frac{R_f}{R_g}\right] * \left[\frac{1}{1 + \frac{2}{A(s)\beta}}\right]$$
(8)



2.6 Computation of filter time constant (τ)

Bandwidth of the low pass filter is decided based on two parameters: noise bandwidth of the signal chain and harmonic distortion. Lower bandwidth helps reduce wide band noise present in the signal chain while adding distortion to the high frequency signals. Typically, the time constant is set to accommodate an expected step input so that the encoder outputs can be allowed to pass without any attenuation. The step size depends on several parameters like: maximum signal frequency and amplitude, throughput of the ADC, conversion time etc. The sampled input voltage (Vsample) of the ADC for a given amplifier input step (Vstep) can be expressed by the exponential relationship as in Equation 9. For a differential application, the full scale step size is 2^* Vref while available settling time is equal to the acquisition time (t_{aq}) of the ADC. Therefore the required time constant can be calculated using Equation 10 for an error of less than 1 LSB at N bit level.

$$Vsample = Vstep * (1 - e^{-\frac{t}{\tau}})$$
(9)

$$error = Vstep - Vsample = Vstep * e^{-\frac{1}{\tau}}$$

For
$$Vstep = 2*Vref$$
 and $error = \frac{2*Vref}{2^N}$, $\frac{2*Vref}{2^N} = 2*Vref*e^{-\frac{t_{aq}}{\tau}}$
 $\tau = \frac{t_{aq}}{N*\ln 2}$ (10)

Selection of R and C for a required time constant needs case specific consideration of two parameters: stability of the amplifier and harmonic distortion.

3 Component Selection

The goal of this design is to achieve the lowest power from a single power supply without compromising the primary performance, which includes parameters such as signal to noise and distortion ratio (SINAD), gain and offset matching between the channels, ADC linearity and sampling jitter matching. Another very important parameter is ensuring performance for a required clock (SCLK) frequency versus a given throughput.

3.1 ADC Selection

The ADS7254 is a 12-bit, dual channel, simultaneous sampling, SAR ADC with 1 MSPS throughput. This is specifically designed to interface with optical encoders for use in motor control applications. Listed below are the benefits of using this ADC:

- 1. Contains two well matched internal reference sources which allow for good gain matching between the two ADCs.
- 2. The sampling instance is dictated by the same chip select (CSZ) signal which helps to achieve very low sampling jitter mismatch, which is important because it reduces the time instance sampling error between channels.
- 3. It has an internal oscillator which provides the required conversion clock.
- 4. Since conversions take about 450 ns and the ADC starts sampling the analog input again just after the conversion completes, this makes the acquisition time for a 1 MSPS throughput case 550ns, which is enough time to make the design of the external drive buffer amplifier design easy.



- Also, this ADC provides the data output within the same timing frame or "on the fly." Specifically, a 32 MHz clock is sufficient to get 1 MSPS throughput which translates to a 1µs response time, which is very important in motor control applications
- Additional details are available in the ADS7254 datasheet. In this circuit, ADS7254 is configured in 2*V_{ref} mode with a 2.5 V internal reference source in 32-clock mode. Thus differential input (V_{indiff}) signal range becomes ±5 V for a 2.5 V reference voltage while input common mode voltage remains same as the reference voltage.

3.2 Buffer Amplifier Selection

The THS4531 is the best amplifier choice for this application for the following reasons:

- Input signal range compatibility. The THS4531 offers a programmable output common mode voltage. In this circuit, the 2.5 V internal reference voltage of the ADS7254 drives the desired output common mode voltage (Vocm) of the THS4531. It is used in a unity gain inverting configuration to accommodate wide common mode voltages at the sensor output.
- 2. Rail to rail output. This amplifier needs only 200 mV headroom from both positive supply and ground. So it can accommodate ±4.6 V signal range for a 5 V power supply.
- 3. Low power consumption versus bandwidth. THS4531 offers very good power to noise ratio with high bandwidth.

4 Simulations

The circuit has been simulated in TINA-TITM by using models for the ADS7254 and THS4531. These TINA-TITM-SPICE models are available in the product folder for each device. TINA-TITM-SPICE test bench for each simulations are available in the design archive. A simplified model of the signal chain as shown in Figure 6 is used to verify the following:

- Transfer curve that shows compliance to a full scale input signal swing of ±4.5V.
- Amplifier stability, shown by peaking in the ac response and step response curves.
- The effects of passive component mismatch, power consumption, and amplifier noise.
- System level functionality for a full scale sine and cosine input.

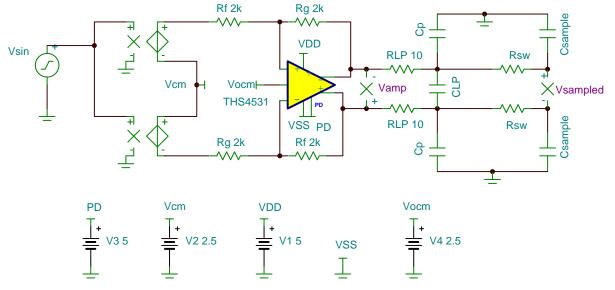


Figure 6: Circuit for Transfer Curve Simulation



4.1 Transfer curve

The differential output voltage is simulated for ± 6 V input signal range with various input common mode voltages (V_{cm}). Note that the differential input output transfer function remains same as Figure 7 and independent of input common mode voltage. This result shows a head room requirement of 200 mV from both the positive supply and ground. For a 5 V supply, the differential output is linear within the ± 4.6 V input range, but for guaranteed operation we recommend ± 4.5 V signal range.

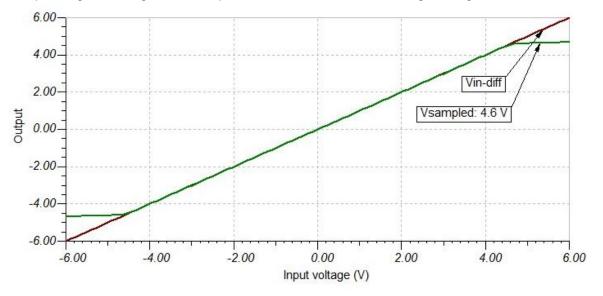


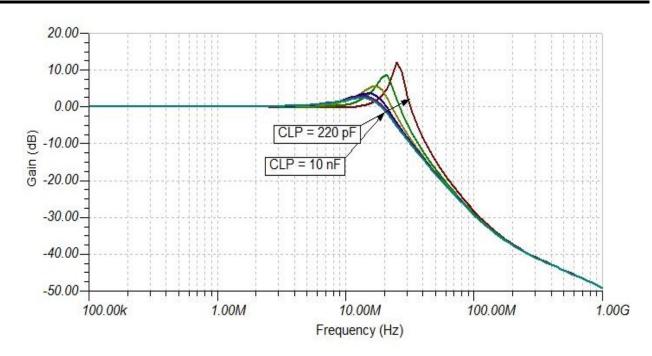
Figure 7: DC Transfer Curve

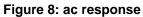
4.2 Amplifier Stability

The acquisition time of the ADC is 550 ns for a 1 MSPS throughput, and the low pass filter is designed for 14 bit settling of a full scale step. Thus, the filter time constant (τ) calculated from Equation 10 is 55 ns. The filter resistance value that is required 10 Ω is a result of the value need to isolate from the required filter capacitor value of 2.75 nF.

To see the effect of the required filter RC on amplifier stability, the ac response is simulated with a 10 Ω resistance and a variable capacitor. Figure 8 shows the ac response of the amplifier for different capacitor values in the range of 0.22-10 nF. This result reflects a larger peak in the amplitude response for smaller capacitor values which says a 10 Ω resistor is not sufficient to compensate the feedback loop for smaller capacitor values. Selecting a larger resistance and smaller capacitor value with same RC product may degrade harmonic distortion. The small-signal step response is shown in Figure 9. This simulation also shows some ringing as matching the ac response. Lower RC values show a larger overshoot and slower settling while larger RC values produce smaller overshoot and faster settling. Based on these simulations, the filter capacitor (C_{LP}) is selected as 2.2 nF for faster step settling. Also, the amplifier noise contribution is simulated as 48 µVrms which is negligible compared to the quantization noise of 350 µV for ADS7254.







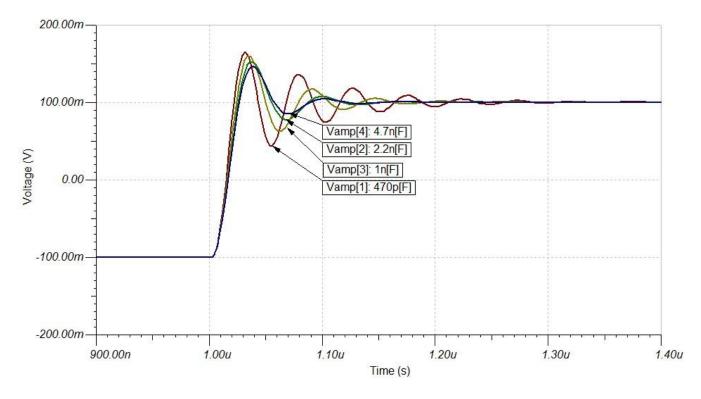


Figure 9: Step Response



4.3 Passive Mismatch Effects

The effect of passive component mismatch (i.e. R_g and R_f from Figure 6) is simulated to estimate the statistical error incurred from the offset and gain mismatch between channels. To accomplish this, a Monte Carlo simulation with sample size = 100 provides a good statistical look at this error. Histograms of the output error for different component tolerance are presented in Figure 10. This result shows a linear improvement in standard deviation (σ) with improved component tolerance. Simulation is performed for 1%, 0.1% and 0.01% tolerance value resulting standard deviation of 22 mV, 2.17 mV and 0.22 mV respectively for a 10 V signal range. Therefore, R_g and R_f are selected to have a 0.1% tolerance value due to the fact that 99.73% of the population remains within ±3* σ error range.

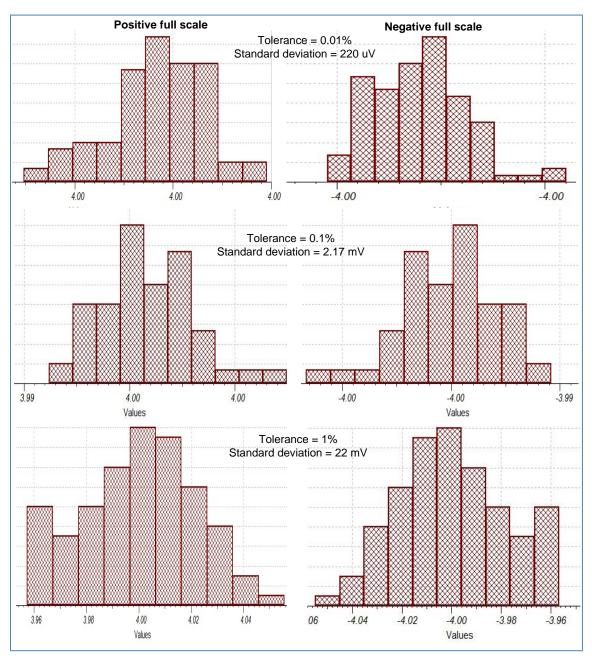


Figure 10: Output mismatch with different tolerance on Rf and Rg from circuit in Figure 6

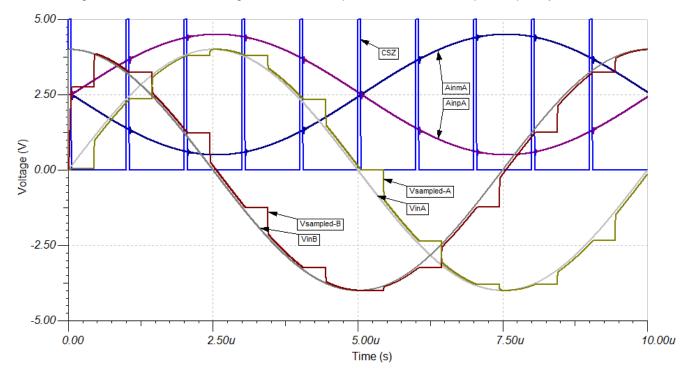


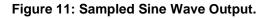
4.4 Power

The static power consumption for the circuit is defined by the quiescent power dissipation of the ADS7254 and THS4531; however, the values of R_g and R_f define the amplitude of load current for the THS4531. If the sensor output common mode voltage is different from 2.5 V, there will be common mode current flowing through R_g and R_f . Thus, higher values of R_g and R_f reduce the overall power. Unfortunately, higher values for R_g and R_f also impact the system noise and the stability of the amplifier. As an example, the THS4531 datasheet recommends a 1 k Ω resistor for R_g and R_f to get the best performance from it. The problem is that a 1 k Ω resistor results in a 2mA peak current through R_g for a 4 V_{pp} signal. In the case of the circuit shown in Figure 6, stability has been verified with 2k Ω for R_g and R_f which helps to reduce this signal current.

4.5 System Functionality

The overall function of the circuit shown in Figure 2 is simulated with an ideal differential input voltage source (representing the optical encoder output). The results shown in Figure 11 show the sampled voltage for a sine and cosine signal with 4.0V amplitude and 100 kHz input frequency.







5 PCB Design

The PCB schematic and bill of materials is shown in Appendix-A1. The circuit was developed on a simple 4 layer PCB with two dedicated plane layers for GND and supply. The final PCB dimension is 6.4 X 5.2 cm. Figure 12 shows the layout of the board. Critical layout concerns are listed here:

- The decoupling capacitors are placed close to the device supply pin
- 100 nF capacitor and 10 µF capacitors are placed close to each reference pins. Reference decoupling capacitors must be of X7R category with higher voltage rating (> 2*V_{ref}).
- Series termination resistors for each high frequency signal should be placed close to the source. 49.9 Ω resistors are being used for SCLK, CSZ, SDO-A and SDO-B with 50 Ω trace.
- The length of the feedback paths and parasitic capacitance at the amplifier input should be minimized to avoid undesirable oscillations.

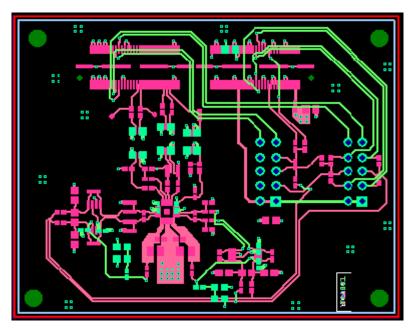


Figure 12: PCB Layout

6 Verification and Measured Performance

Linearity, THD, SNR, and SINAD were measured for both input channels to compare with the targeted specifications listed in Table 1. All of these parameters were measured for 1 MSPS throughput, and a 16 bit accurate ramp generator was used to measure INL and DNL of the ADC. A 32 MHz SCLK was used to achieve 1 MSPS throughput. The ADS7254 was configured into 2^*V_{ref} mode with a 2.5 V internal reference source. In this mode the ADC full-scale input range is ± 5 V. Though the recommended input signal range is only ± 4.5 V, linearity was measured up to ± 4.8 V input signal range at room temperature and 5 V supply. Figure 13 shows a typical DNL and INL plot.



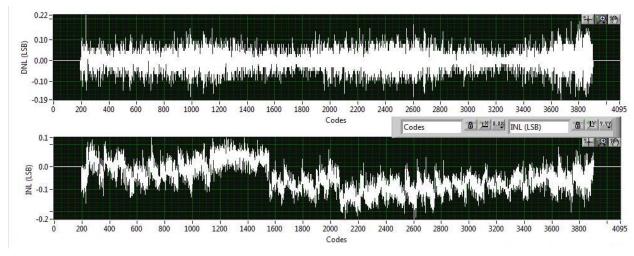
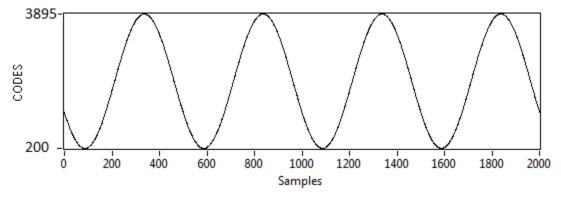
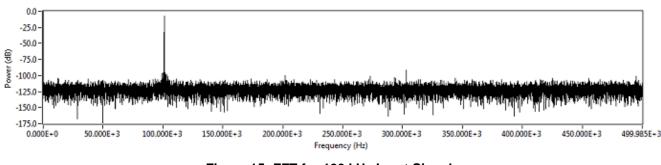


Figure 13: Typical DNL and INL Plot

A 2 kHz sinusoidal input was used to measure all dynamic parameters across a wide range of input common mode voltage. Also, a 2 kHz band pass filter was used to eliminate wide band source noise. Figure 14 shows a typical sinusoidal output result, and Figure 15 shows the FFT plot for 100 kHz signal frequency.







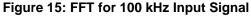


Table 2 shows all dynamic parameters measured across the 0 to 5 V input common mode voltage (Vincm) range. SNR and THD were also measured across different input frequencies without the band pass filter, which degrades SNR by 0.4 dB at 2 kHz. Table 3 shows all measured dynamic parameters up to 100 kHz.

Input common mode (V)	Signal power (dB)	SNR (dBFS)	THD (dB)	SINAD (dBFS)
0	-0.7	73.6	94.9	73.6
1	-0.7	73.8	95.1	73.7
2	-0.7	73.8	93.9	73.7
3	-0.7	73.8	93.4	73.7
4	-0.7	73.7	94.7	73.8
5	-0.7	73.8	94	73.7

Table 2: SNR vs. Input Common Mode Voltage (Vcm)

Frequency (kHz)	Signal power (dB)	SNR (dBFS)	THD (dB)	SINAD (dBFS)
1.0	-2.6	73.3	89.9	73.2
2.0	-2.6	73.4	90.2	73.3
5.0	-2.6	73.4	90.3	73.3
10.0	-2.6	73.3	91.8	73.3
20.0	-2.6	73.4	90.9	73.3
50.0	-2.7	73.4	90.7	73.3
100.0	-2.6	72.4	89.2	72.3

All active components on the board share a single 5 V supply. Total current consumption at 1 MSPS is measured as 16 mA which is larger than simulated value of 13 mA. This additional power consumption is due to high frequency digital signals. The digital input / output buffers on the board used for level translation are running on same 5 V supply and their purpose is to drive the parasitic trace capacitor on the board for SDO and SCLK. This current can be reduced by using a separate, lower power supply for DVDD pin of ADS7254 and onboard digital buffers. The difference between input common mode and output common mode voltages results in extra current through the feedback resistors. Table 4 shows the total current consumption for a wide range of input common mode voltages (V_{incm}).

1 MSPS, AVDD = 5 V						
V _{cm} (V)	I_AVDD (mA)					
0.0	17.1					
1.0	16.5					
2.0	16.0					
2.5	15.7					
3.0	15.5					
4.0	15.1					
5.0	14.8					

Table 4: Total Current vs. Input Common Mode Voltage



SNR performance of the system is limited by the ADC while THD is limited by the amplifier. This ADC has been designed as part of a pin compatible family of devices with variable throughput, resolution and interface modes. For 14/16 bit performance ADS7854/ADS8354 can be used with same PCB and software. For lower amplifier noise and distortion, the THS4521 should be used in place of THS4531. The filter RC should be optimized for the modified sampling time and noise requirements. The ADS7254 and ADS7854 also support a 16-clock mode interface where 1 MSPS throughput is achievable with an 18 MHz SCLK. Table 5 shows SNR, THD, SINAD and current consumption for some of the combinations possible with the same PCB and software.

Amplifier	ADC	clock mode	SCLK (MHz)	Throughput (MSPS)	SNR (dBFS)	THD (dB)	SINAD (dBFS)	Current (mA)
THS4531	ADS7254	32	32	1	73.7	88.3	73.6	15.7
THS4531	ADS7854	32	33	1	83.3	88.8	82.4	15.6
THS4531	ADS7254	16	17	1	73.7	80	73	12.6
THS4531	ADS7854	16	18	1	82	84.2	80.4	13.1
THS4521	ADS7254	16	17	1	73.9	89.8	73.8	16.7
THS4521	ADS7854	16	18	1	83.8	91.9	83.4	17.2
THS4521	ADS7854	32	33	1	83.9	95.2	83.7	19.7
THS4521	ADS8354	32	25	0.75	88.5	97.3	88.2	18

Table 5: Performance for different amplifier and ADC combination

8 About the Authors

Amal Kumar Kundu graduated from the Indian Institute of Technology - Kharagpur in 2008, where he earned a Master of Science in analog VLSI design. He joined Texas Instruments India in 2008 as an analog design engineer, where he has worked on high speed SAR ADC design and analog front-ends (AFE) for digital X-ray applications.

Deepak Mathew graduated from the National Institute of Technology - Calicut in 2011, where he earned a Bachelor of Technology in Electrical Engineering. He joined Texas Instruments India in 2011 as a test engineer, where he works on testing and characterization of SAR ADCs.

9 References and Acknowledgements

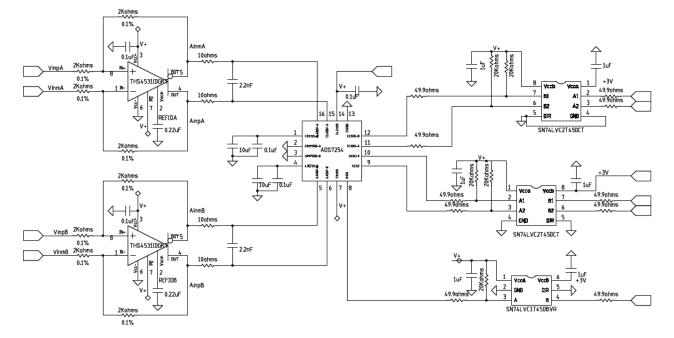
- 1. "Encoders for Servo Drives", Product catalog from Heidenhain, December 2010.
- 2. Matthew W. Hann, "Ultra Low Power, 18 bit Precision ECG Data Acquisition System ", TI Precision Designs: Verified Design, June 2013

The authors wish to acknowledge KG Ramachandra for help with the PCB design, Sharat Chandra, Rafael Ordonez, and Luis Chioye for valuable suggestions during the circuit development.



Appendix A.

A.1 Electrical Schematic





A.2 Bill of Materials

Item	Qty	Designator	Value	Part Number	Description	Manufacturer
1	4	C63,C64,C99,C100	0.1uF	0402YC104KAT2A	CAPACITOR,SMT,0402,CER,16V,10%,0.1 uF	AVX
2	4	C69,C70,C71,C72		CAP-SMT0402- UNINSTALLED	(Uninstalled Part) CAP SMT0402 UNINSTALLED	Uninstalled
3	2	C75,C113	0.1uF	04023C104KAT2A	CAPACITOR,SMT,0402,CERAMIC,0.1uF,2 5V,10%	AVX
4	3	C92,C114,C115	10uF	LMK107BJ106MALTD	CAPACITOR,SMT,0603,CERAMIC,10uF,1 0V,20%,X5R	TAIYO YUDEN
5	2	C97,C98	0.0015uF	C0402C152J5GACTU	CAPACITOR,SMT,0402,CERAMIC,1500pF ,50V,5%,C0G/NP0	KEMET
6	2	C101,C102	0.22uF	0402ZG224ZAT2A	CAPACITOR,SMT,0402,CERAMIC,0.22uF, 10V,-20~+80%,Y5V(F)	AVX
7	6	C111,C112,C116,C117,C1 18,C119	1uF	C1608X7R1C105K	CAPACITOR,SMT,0603,CERAMIC,1.0uF,1 6V,10%,X7R	ток
8	6	C120,C121,C122,C123,C1 24,C125	0.01uF	06033C103KAT2A(UN)	Uninstalled	
9	2	C126,C127	10uF	GRM21BR71A106KE51L	CAPACITOR,SMT,0805,CERAMIC,10uF,1 0V,10%,X7R	MURATA
10	1	DUT2		DUT_QFN_RTE-16	DUT,SMT,16P,QFN,RTE- 16,3x3x1mm,0.5mmLS,HS PAD	ті
11	1	J1	value	QTH-060-01-L-D-A	HEADER,SMT,120P,0.5mm,FEM,2BANK, RECEPTACLE,168/198H	SAMTEC
12	1	J1		QTH-060-01-L-D-A	HEADER,SMT,120P,0.5mm,FEM,2BANK, RECEPTACLE,168/198H	SAMTEC



	-	1	1	T		1
13	-	J1	THDCON	QTH-060-01-L-D-A	HEADER,SMT,120P,0.5mm,FEM,2BANK, RECEPTACLE,168/198H	SAMTEC
14	2	К1,КЗ		TN2-L2-5V	SPDT,5V,125 OHM,LATCH,10P,2COILS	PANASONIC / NAIS
15	7	R55,R56,R87,R88,R110,R1 11,R112	49.9ohms	TNPW040249R9BEED	RESISTOR,SMT,0402,49.9 OHM,0.1%1/16W	VISHAY
16	1	R57	10Kohms	RG1005P-103-B-T5	RESISTOR,SMT,0402,THIN FILM,10.0K,0.1%,1/16W,25ppm	SUSUMU
17	4	R58,R59,R60,R61	4.7ohms	CRCW04024R70JNED	RESISTOR,SMT,0402,4.7 OHM,5%,1/16W	VISHAY
18	8	R89,R90,R91,R92,R93,R94 ,R95,R96	1Kohms	RG1005P-102-B-T5	RESISTOR,SMT,0402,THIN FILM,1.00K,0.1%,1/16W,25ppm	SUSUMU
19	7	R97,R98,R99,R100,R101,R 102,R103		CRCW0402000Z(UN)	(UNINSTALLED PART)	VISHAY
20	1	R104	0ohms	CRCW0402000Z	ZERO OHM JUMPER,SMT,0402,THICK	VISHAY
20	1	R104	00hms	ERJ-2GEOR00X	FILM,0 OHM,1/16W,5% RESISTOR/JUMPER,SMT,0402,0 OHM,5%,1/16W	PANASONIC
22	3	R106,R107,R113	49.9ohms	CRCW040249R9F100	RESISTOR,SMT,0402,49.9 OHM,1/16W,1%,100ppm	VISHAY
23	5	R108,R109,R114,R115,R1 16	20Kohms	CRCW04022002F100	RESISTOR,SMT,0402,20K,1/16W,1%,100	VISHAY
24	3	R117,R118,R119	0ohms	CR0402-16W-000T	RESISTOR,SMT,0402,0 OHM,1/16W,ZERO JUMPER	VENKEL
25	4	R120,R121,R122,R123	10Kohms	ERA-3YEB103V(UN)	Uninstalled	Uninstalled
26	2	R124,R125	0ohms	CRCW04020000Z0ED(UN)	Uninstalled	Uninstalled
27	2	TP1,TP2		TP108(UN)	TEST POINT SMT, C SHAPE	COMPONENTS CORP
28	2	U1,U2		THS4531IDGKT	WIDEBAND LOW-DISTORTION FULLY DIFFERENTIAL AMPLIFIER	ті
29	2	U4,U5		SN74LVC2T45DCT	DUAL-BIT DUAL SUPPLY BUS TRANSCEIVER	ті
30	1	U6		SN74LVC1T45DBVR	SINGLE BIT DUAL SUPPLY BUS TRANSEIVER	ті

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