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TI Precision Designs: Verified Design

Combined Voltage and Current Output Terminal for Analog Outputs (AO) in Industrial Applications

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Circuit Description

Standard industrial analog output (AO) circuits are dedicated to either voltage or current outputs. This design using the DAC8760 can output both the standard industrial voltage and current outputs on a single terminal, thus reducing the number of terminals needed from three to two. A combined output succeeds in reducing the wiring cost, connector count, and increasing the versatility of the AO design. The possible outputs of the design include: 4-20 mA, 0-20 mA, 0-24 mA, 0-5 V, 0-10 V, +/-5 V, +/-10 V, as well as voltage over-ranges.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
DAC8760	Product Folder
OPA192	Product Folder

TI E2E™ Community

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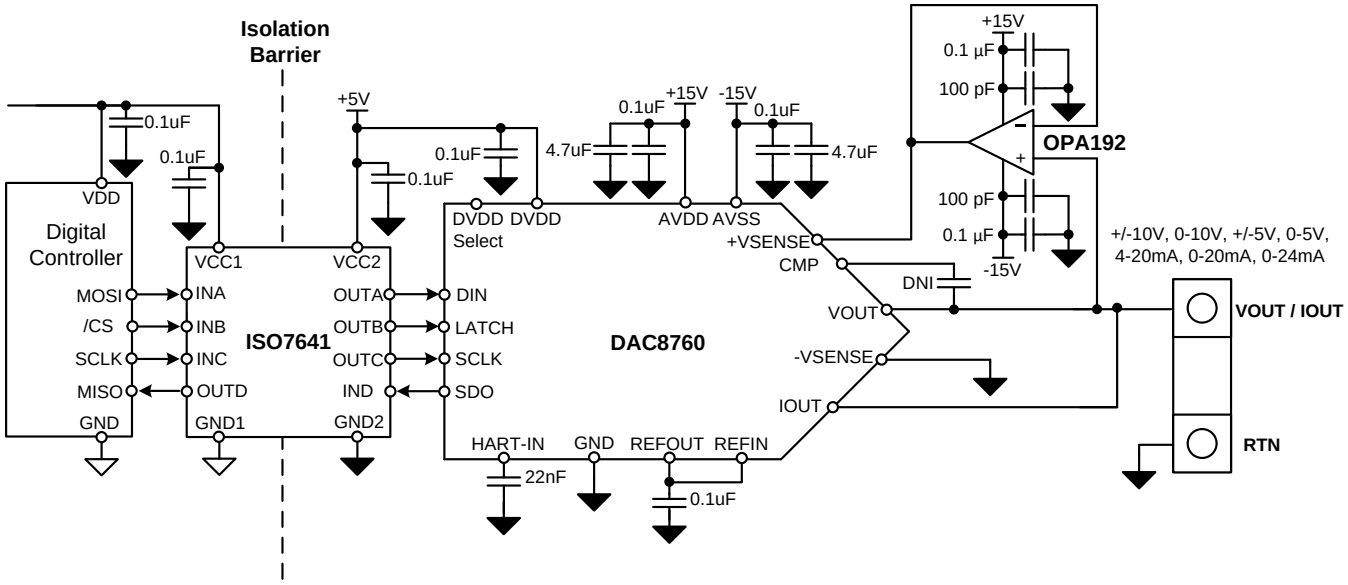

1 Design Summary

The design requirements are as follows:

- Supply Voltage: +/-15 V
- Digital Input: 4-Wire SPI
- Digital Isolation: 4 kV
- Resolution: 16-Bit
- Voltage Output: +/-10 V, with 10% over-range option
- Current Output: 0 mA – 24 mA
- Temperature: 25 °C

The design goals and performance are summarized in Table 1. Figure 1 depicts the dc transfer function of the design measured in both voltage and current output modes.

Table 1. Comparison of Design Goals, Simulated, and Measured Performance

		Goals	Calculated	Measured
Current (0-24 mA)	**TUE (%FSR)**	0.1%	0.02	0.048
Voltage (+/-10 V)	**TUE (%FSR)**	0.1%	0.015	0.014

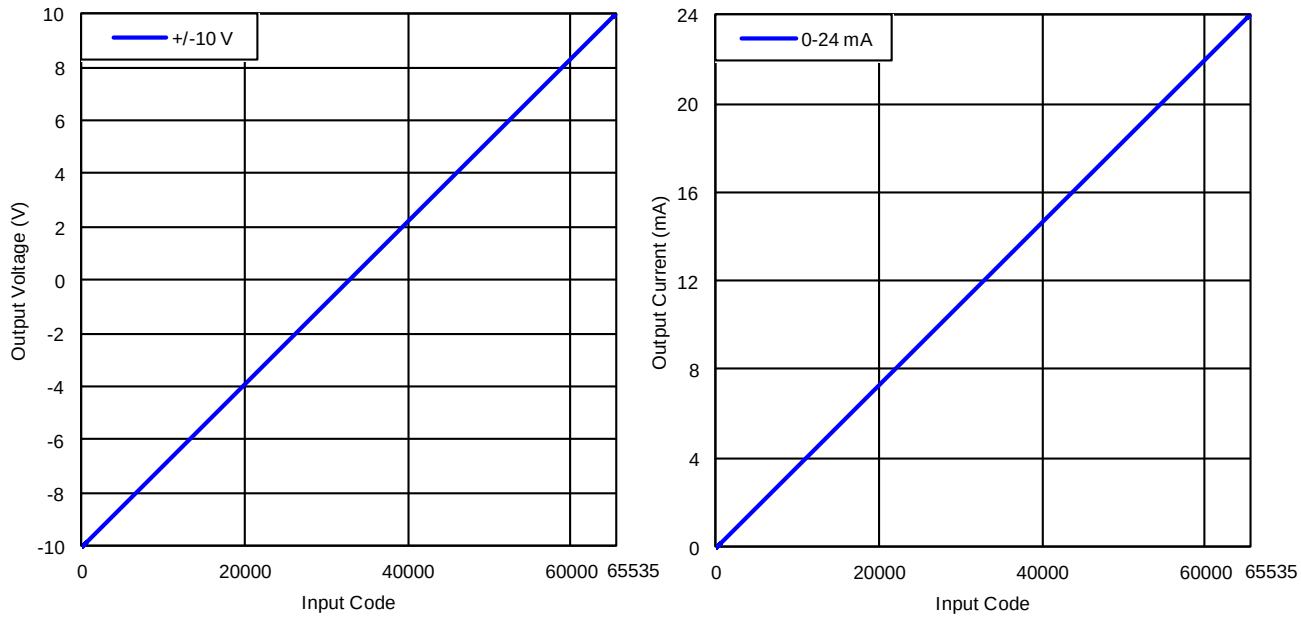

Figure 1: Measured dc Transfer Function

2 Theory of Operation

Figure 2 displays a simplified version of the circuitry inside the DAC8760 that is used to create a combined voltage and current (V+I) output driver. A 0 V to 5 V digital-to-analog converter (DAC) drives the inputs for both the voltage (V_{OUT}) and current (I_{OUT}) output stages. The DAC requires an accurate, low-drift reference voltage (V_{REF}) to deliver strong dc performance, along with a voltage regulator (V_{REG}) to drop the analog supply, AVDD, down to +5 V for the low-voltage analog and digital circuitry.

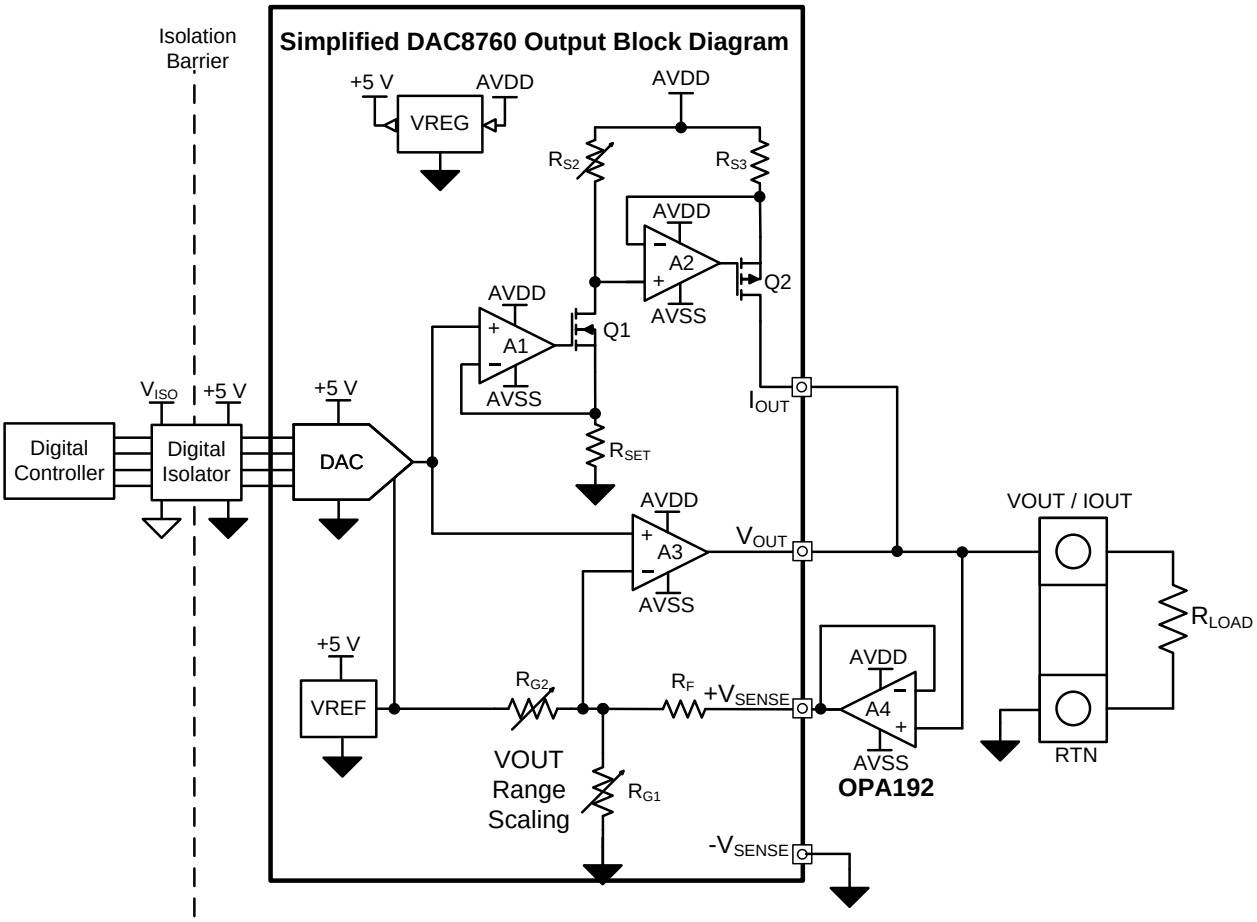

Figure 2: Circuit Schematic

2.1 I_{OUT} Circuitry

The I_{OUT} circuit is composed of amplifiers A1 and A2, MOSFETs Q1 and Q1, and the three current sensing resistors, R_{SET}, R_{S2}, and R_{S3}. The two-stage current source enables the GND referenced DAC output to drive the high-side amplifier required for the current-source. For detailed design information on the design of a high-side voltage-to-current output stage, please refer to TIPD502.

When V_{OUT} is active, Q2 is kept in a high-impedance state and does not negatively affect the V_{OUT} circuit performance. Refer to SBAA199 for a more detailed investigation of the effects that occur when creating a combined voltage and current output driver with the DACx760 family.

2.2 V_{OUT} Circuitry

The V_{OUT} circuit is composed of amplifiers A3, A4, and the feedback network around A3 consisting of R_F, R_{G1}, and R_{G2}. A3 operates as a modified summing amplifier where the DAC controls the non-inverting input and the inverting input has one path to GND and a second to V_{REF}. This configuration allows the single ended 0-5 V DAC to create both the unipolar 0-5 V and 0-10 V outputs and the bi-polar +/-5 V and +/-10 V outputs. A resistor switching network is used to change the values of R_{G1} and R_{G2} depending on the selected voltage output range.

A4 is used to buffer the resistive feedback network of A3 so the feedback resistors do not present a resistive load on the I_{OUT} circuitry which would reduce the current delivered to the load. A4 is therefore inside the feedback loop of A3 and contributes directly to errors of the voltage output stage. In a buffer configuration the gain and linearity errors will be negligible but the offset voltage will add directly to the V_{OUT} circuit offset voltage.

2.3 Digital Isolation

Most AO modules require isolation from the backplane and other AO modules. This is typically accomplished by isolating the digital signals between the host processor/controller and the DAC in the AO circuit. There are many topologies available to achieve the isolation but galvanic (capacitive) isolation has many advantages over other topologies and will be selected for this design.

3 Component Selection

A detailed schematic for the design with the final components is shown in Figure 3.

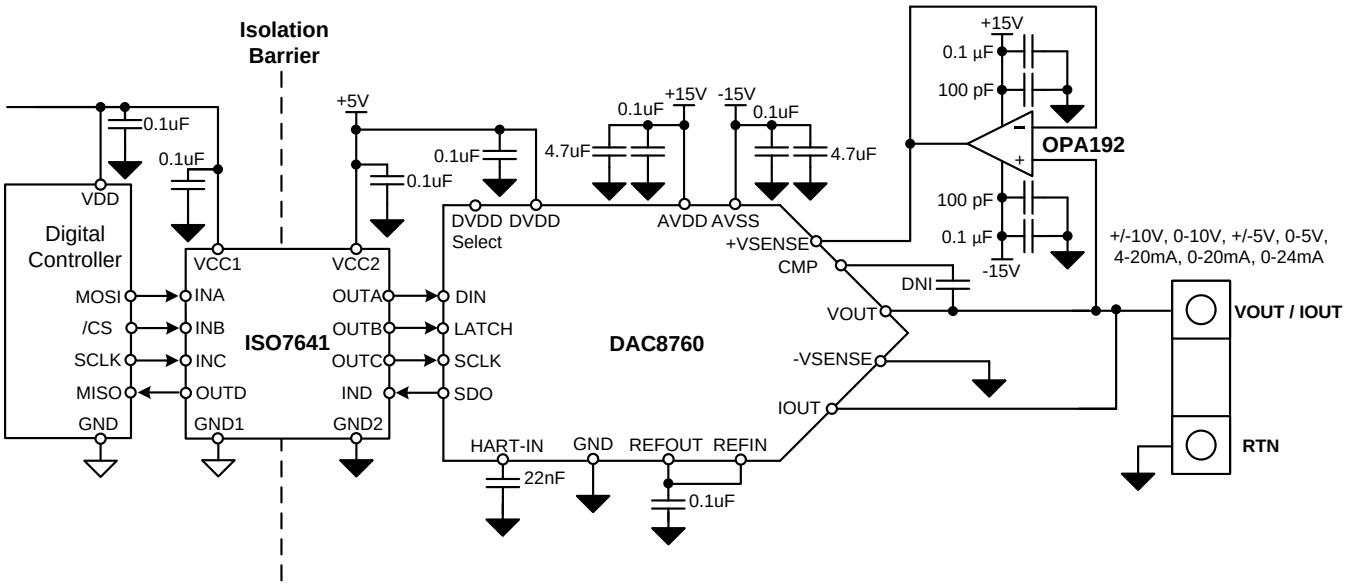

Figure 3: Complete Schematic for Combined V+I Analog Output

3.1 DAC – DAC8760

The DAC8760 includes the DAC, amplifiers A1, A2, and A3, V_{REG}, V_{REF}, and all of the switches, transistors, and resistors required to create a configurable integrated solution for industrial voltage and current output drivers. The DAC8760 features a max 0.1% full-scale range (FSR) total-unadjusted-error (TUE) specification, which includes offset error, gain error, and integral non-linearity (INL) errors at 25°C. The 0.1% FSR TUE is valid for all of the voltage and current output stages providing a baseline for the final system accuracy. The max differential non-linearity (DNL) specification of +/-1 least significant bit (LSB) provides fully monotonic operation for both V_{OUT} and I_{OUT}.

The integral non-linearity (INL) specifications of 0.022% FSR for V_{OUT} and 0.024% FSR for I_{OUT} demonstrate high linearity and accuracy. The integrated V_{REF} circuit provides a low temperature drift reference for the DAC, specified at 10 ppm/°C. The 4-wire SPI communication bus features a daisy-chain option that allows multiple DAC8760 devices to be controlled through a single 4-channel digital isolator, enabling a group-isolated multiple output system.

Another integrated option is the 12-bit DAC7760. For discrete options refer to Section 7.

3.2 Amplifier Selection – OPA192

The buffer amplifier becomes a part of the feedback network of the DAC8760 V_{OUT} circuit and any dc errors will directly contribute to the final V_{OUT} accuracy. An amplifier with low offset voltage (V_{OS}), low V_{OS} drift ($V_{OS(DRIFT)}$), high common-mode rejection ratio (CMRR), and high power-supply rejection ratio (PSRR) will help keep the error contribution of the amplifier as low as possible. A JFET, CMOS, or low input bias current BJT input topology amplifier should be used to prevent the input bias current from affecting the I_{OUT} circuit. The OPA192 was chosen for its precision e-trim™ topology that achieves 5uV typical, 25 uV max, V_{OS} and 0.2 uV/°C typical, 0.5 uV/°C max $V_{OS(DRIFT)}$ without the use of chopping or other switching offset cancellation techniques. The rail-to-rail CMOS input stage features a typical CMRR of 110 dB and a typical PSRR of 0.5 µV/V over the full supply range of +4 V to +36 V. The CMOS inputs result in a maximum input bias current (i_B) of 20pA which will not noticeably affect the I_{OUT} circuit performance. A bandwidth of 10 MHz, slew rate of 20 V/µs, and 0.01% settling time of 1 µs keeps the amplifier from limiting system bandwidth. The rail-to-rail output and output current drive capabilities allow for good swing to GND if operated in a single-supply configuration.

3.3 Digital Isolator – ISO7641

The four serial data signals required to communicate bi-directionally with the DAC8760 are SCLK, DIN, SDO, and LATCH. In order to maintain isolation from the host controller, these signals must be isolated through a digital isolator. The ISO7641 is a 25 MBPS digital isolator that features >4 kV galvanic isolation.

3.4 Passive Component Selection

Although it was not tested in this design, a footprint was included for an external R_{SET} resistor (R_1). Unless the R_{SET} resistor is populated, there are not any passive components that require high precision for this design. If an external R_{SET} resistor is used with this design then it should be chosen for high accuracy and low temperature coefficient.

The voltage compensation capacitor, C_{COMP}, was not installed for this design because the output capacitive load was very small. If capacitive load drive capabilities are required then C_{COMP} will need to be installed and sized based on the DACx760 datasheet requirements. All capacitors in the signal path should be sized for a voltage coefficient that well exceeds the voltage that will be placed across them to keep the capacitance values constant during. Use C0G/NP0 dielectric capacitors when possible and X7R when C0G/NP0 are not available.

4 Circuit Performance Calculations

4.1 I_{OUT} Accuracy

The I_{OUT} circuit performance is based on the specifications of the DAC8760. The small 20 pA i_B current of the OPA192, shown in Figure 4, is lower than the output noise of the DAC8760 and will not negatively affect the output. The expected performance can be calculated based on the specifications in the product datasheet that are shown in Figure 5.

INPUT BIAS CURRENT						
I_B	Input bias current			±5	±20	pA
		T_A = –40°C to +125°C			±5	nA

Figure 4: OPA192 i_B Specification

Accuracy (for 0-mA to 20-mA and 0-mA to 24-mA range settings)(4)						
Total unadjusted error, TUE		T_A = –40°C to +125°C	–0.2		+0.2	%FSR
		T_A = –40°C to +85°C	–0.16		+0.16	%FSR
		T_A = +25°C	–0.08	±0.02	+0.08	%FSR
Differential nonlinearity, DNL		Monotonic			±1	LSB
Relative accuracy, INL(5)		T_A = –40°C to +125°C			±0.080	%FSR
		T_A = –40°C to +85°C			±0.024	%FSR
Offset error		T_A = –40°C to +125°C	–0.17		+0.17	%FSR
		T_A = –40°C to +85°C	–0.1		+0.1	%FSR
		T_A = +25°C	–0.07	±0.01	+0.07	%FSR
Gain error	Internal R_{SET}	–40°C to +125°C	–0.2		+0.2	%FSR
		–40°C to +85°C	–0.15		+0.15	%FSR
		T_A = +25°C	–0.08	±0.01	+0.08	%FSR
	External R_{SET}	–40°C to +125°C	–0.17		+0.17	%FSR
		–40°C to +85°C	–0.12		+0.12	%FSR
		T_A = +25°C	–0.05	±0.01	+0.05	%FSR

Figure 5: DAC8760 DC I_{OUT} Specifications

Based on the product specifications, the expected output performance for the I_{OUT} circuit at room temperature (25°C) is displayed in Table 2.

Table 2. Calculated I_{OUT} Circuit Performance

		Goals	Calculated
Current (0-24 mA)	**Offset (%FSR)**	N/A	+/-0.01
	Gain Error (%FSR)	N/A	+/-0.01
	INL (%FSR)	N/A	+/-0.024
	TUE (%FSR)	0.1%	+/-0.02

4.2 V_{OUT} Accuracy

The op amp is included within the feedback loop of the DAC8760 V_{OUT} circuit. Therefore the op amp errors combine with the errors of the DAC8760 for the final V_{OUT} error. In a buffer configuration, the high open-loop gain of the OPA192 won't contribute any significant gain or linearity errors. The OPA192 offset voltage and CMRR specifications are shown in Figure 6. Since the OPA192 is in a buffer configuration, the common-mode voltage changes with the input signal and will cause additional offset voltage. The worst-case will be at the +10V and -10V levels resulting the total offset voltage calculated in Equation 1. The OPA192 offset voltage will directly add to the bipolar zero offset voltage of the DAC8760, shown in Figure 7.

$$V_{OS\_OPA192} = V_{OS} + V_{OS\_CMRR} = 5\ \mu V + 10V / 10^{\frac{110}{20}} = 36.62\ \mu V \quad (1)$$

PARAMETER		TEST CONDITIONS		OPA192 MIN	OPA192 TYP	OPA192 MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = (V+) – 3 V			±5	±25	µV
		V_{CM} = V_S / 2		See *Common-Mode Voltage Range* section			µV
		V_{CM} = (V+) – 1.5 V			±10	±25	µV
		T_A = –40°C to +125°C, V_{CM} = (V+) – 3 V				±75	µV
CMRR	Common-mode rejection ratio		(V–) – 0.1 V < V_{CM} < (V+) – 3 V	94	110		dB
			(V+) – 3 V < V_{CM} < (V+) – 1.5 V	See Typical Characteristics			dB
			(V+) – 1.5V < V_{CM} < (V+) + 0.1 V	100	120		dB

Figure 6: OPA192 Specifications

Accuracy(1)					
Total unadjusted error, TUE	T_A = –40°C to +125°C	–0.07		+0.07	%FSR
	T_A = –40°C to +85°C	–0.06		+0.06	%FSR
	T_A = +25°C	–0.04	±0.015	+0.04	%FSR
Differential nonlinearity, DNL	Monotonic			±1	LSB
Relative accuracy, INL	T_A = –40°C to +125°C			±0.040	%FSR
	T_A = –40°C to +85°C			±0.022	%FSR
Bipolar zero error	T_A = –40°C to +125°C	–7		+7	mV
	T_A = –40°C to +85°C	–6		+6	mV
	T_A = +25°C, ±5 V and ±5.5 V	–1.5	±0.5	+1.5	mV
	T_A = +25°C, ±10 V and ±11 V	–3	±1	+3	mV
Gain error	T_A = –40°C to +125°C	–0.07		+0.07	%FSR
	T_A = –40°C to +85°C	–0.06		+0.06	%FSR
	T_A = +25°C	–0.04	±0.01	+0.04	%FSR

Figure 7: DAC8760 V_{OUT} Specifications

Since the two offset voltages are uncorrelated, a probable total offset error can be calculated by taking the root of the sum of squares (RSS) of their individual offset voltages, as shown in the equations below.

$$V_{OS\_TOTAL} = \sqrt{(V_{OS\_OPA192})^2 + (V_{OS\_DAC8760})^2} = \sqrt{(0.0366\ mV)^2 + (1\ mV)^2} \approx 1\ mV \quad (2)$$

Based on the product specifications, the expected output performance for the V_{OUT} circuit at room temperature is displayed in Table 3.

Table 3. Calculated V_{OUT} Circuit Performance

		Goals	Calculated
Voltage (+/-10 V)	**Offset (mV)**	N/A	+/-1
	Gain Error (%FSR)	N/A	+/-0.01
	INL (%FSR)	N/A	+/-0.022
	TUE (%FSR)	0.1%	+/-0.015

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.1.

5.1 PCB Layout

For optimal performance of this design follow standard precision PCB layout guidelines, including proper decoupling very close to all mixed signal integrated circuits and providing adequate power and GND connections with large copper pours. The +VSENSE signal routed directly from the output terminal to reduce errors from PCB wiring resistance that would be present if it was connected to V_{OUT} before the output terminal. The layout for the design is shown in Figure 8.

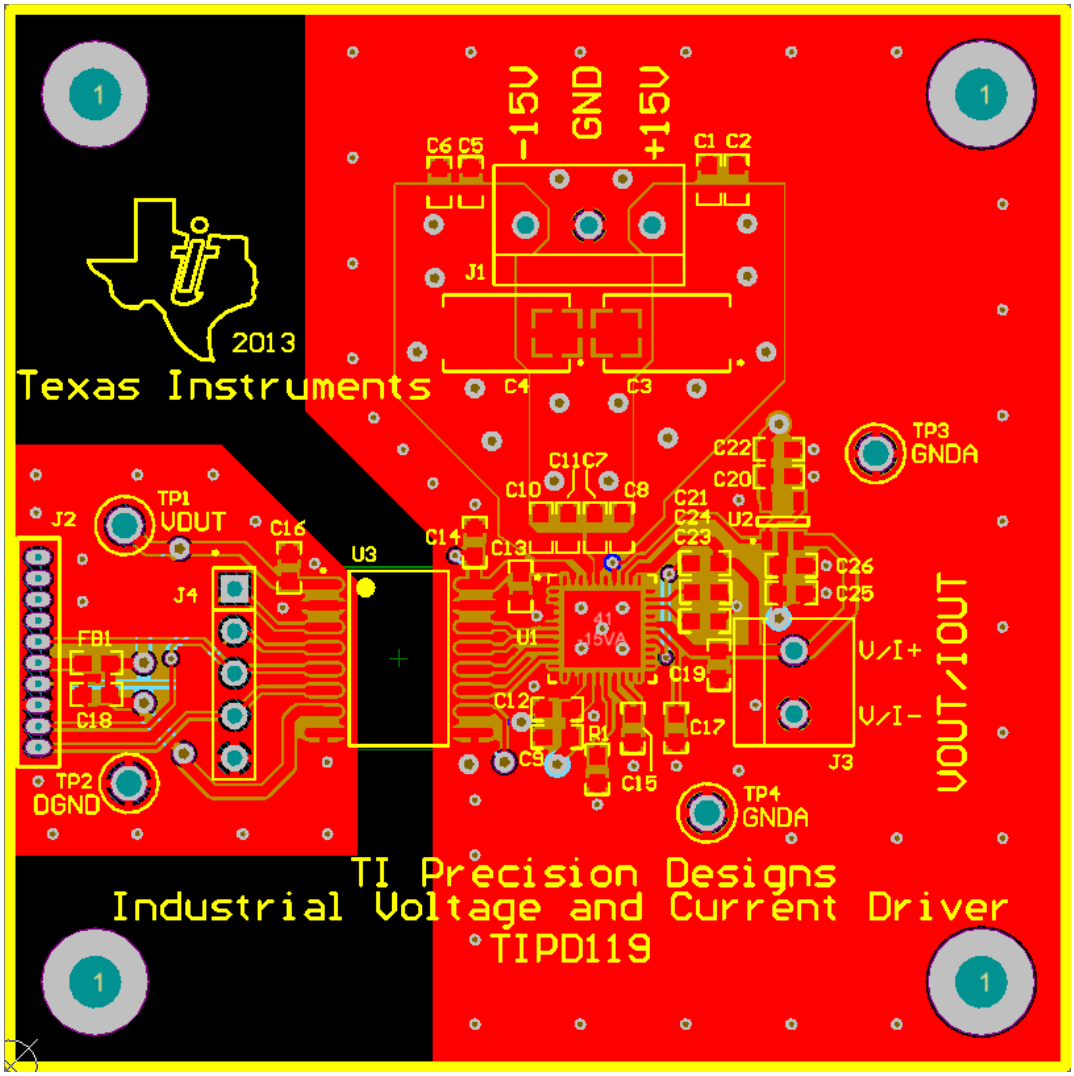

Figure 8: Altium PCB Layout

6 Verification and Measured Performance

6.1 I_{OUT} Circuit

DC transfer function data for the I_{OUT} circuit in 0-24 mA mode was collected using an 8.5 digit multi-meter to measure the output of the circuit while driving a 300 Ω load with +/-15 V supplies. The measurement results are shown in Table 4, Figure 9, and Figure 10. I_{OUT} data for a single-supply 0-24 mA output can be found in Appendix B.2.

Table 4. Measured I_{OUT} Circuit Performance

		Goals	Calculated	Measured
Current (0-24 mA)	**Offset (%FSR)**	N/A	+/-0.01	0.0054
	Gain Error (%FSR)	N/A	+/-0.01	0.039
	INL (%FSR)	N/A	+/-0.024	0.009
	TUE (%FSR)	0.1%	+/-0.02	0.048

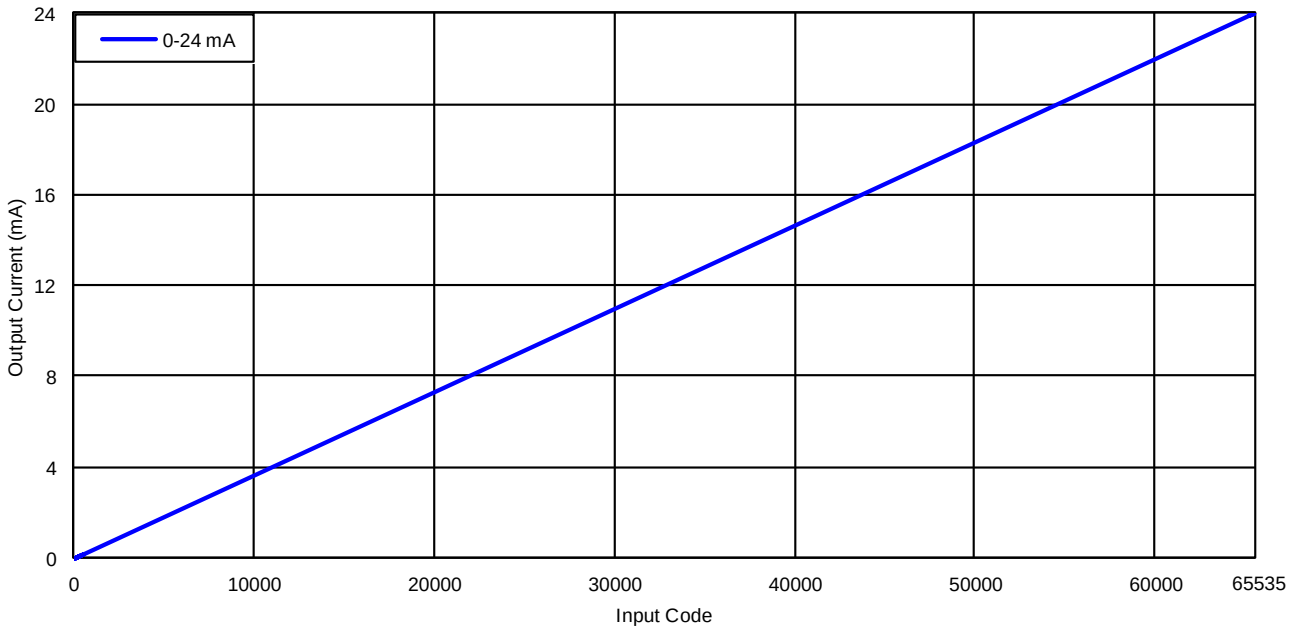

Figure 9. I_{OUT} Circuit 0-24 mA Output Transfer Function

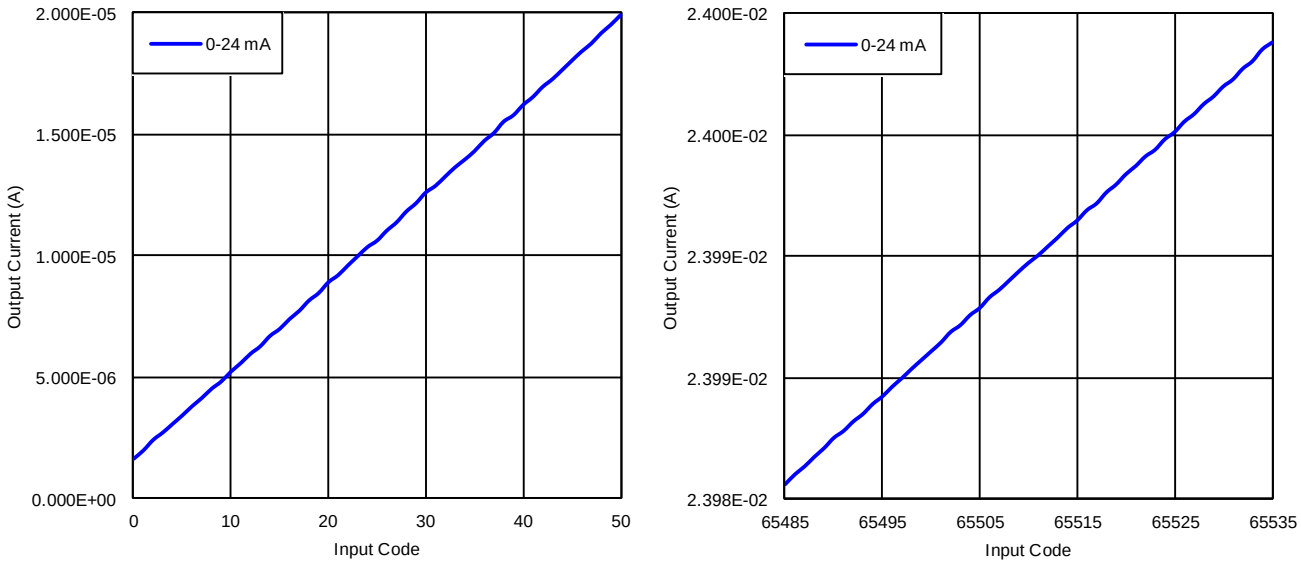

Figure 10. 0-24 mA Zero-Scale and Full-Scale Outputs

6.2 V_{OUT} Circuit

DC transfer function data for the V_{OUT} circuit in +/-10V mode was collected using an 8.5 digit multi-meter to measure the output of the circuit while driving a 1 kΩ load with +/-15 V supplies. V_{OUT} data for a single-supply 0-10V output can be found in Appendix B.3.

Table 5. Measured V_{OUT} Circuit Performance

		Goals	Calculated	Measured
Voltage (+/-10 V)	**Offset (mV)**	N/A	+/-1	0.61
	Gain Error (%FSR)	N/A	+/-0.01	0.023
	INL (%FSR)	N/A	+/-0.022	0.007
	TUE (%FSR)	0.1%	+/-0.015	0.014

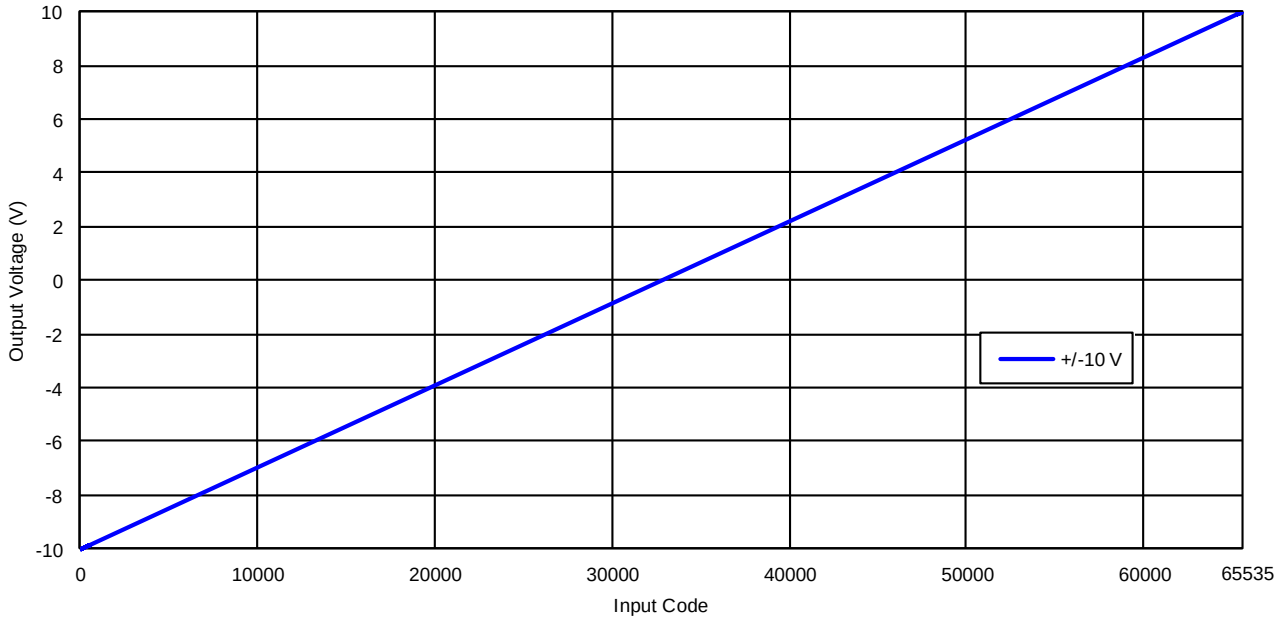

Figure 11. V_{OUT} +/-10 V Output Transfer Function

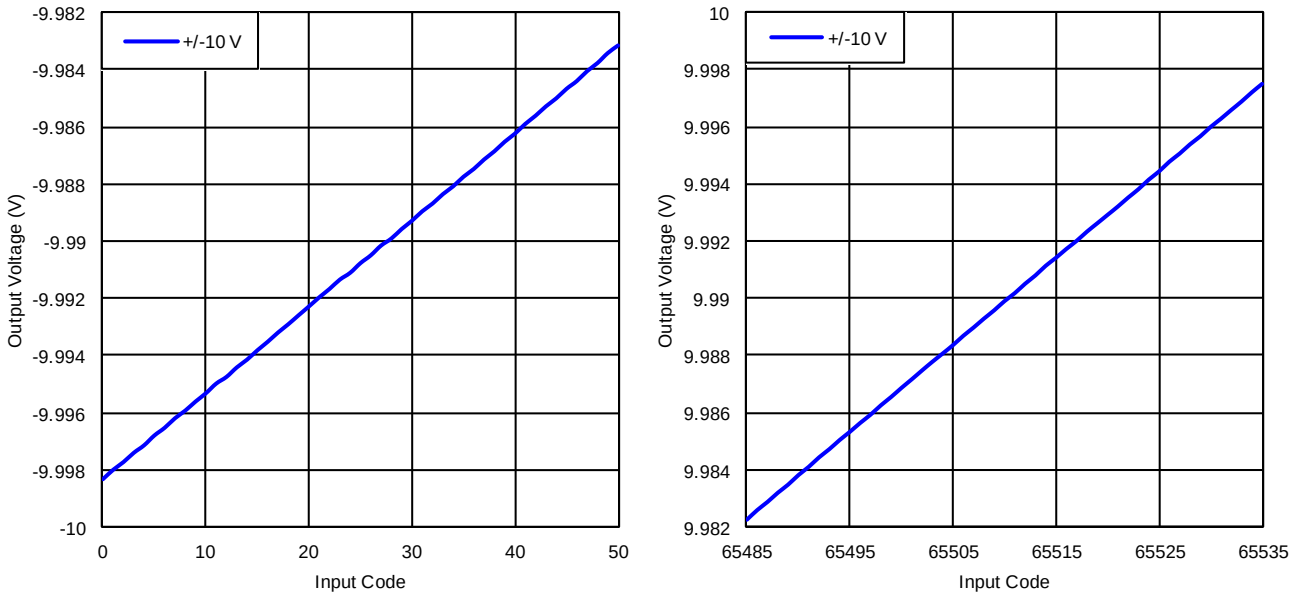

Figure 12. +/-10 V Zero-Scale and Full-Scale Outputs

6.3 Measured Result Summary

The measured results are summarized and compared against the design goals and calculations in Table 6.

Table 6: Measured Result Summary

		Goals	Calculated	Measured
Current	**Offset (mV)**	N/A	+/-0.01	0.0054
	Gain Error	N/A	+/-0.01	0.039
	INL	N/A	+/-0.024	0.009
	TUE	0.1%	+/-0.02	0.048
Voltage	**Offset (mV)**	N/A	+/-1	0.61
	Gain Error	N/A	+/-0.01	0.023
	INL	N/A	+/-0.022	0.007
	TUE	0.1%	+/-0.015	0.014

7 Modifications

The DAC7760 is the 12-bit equivalent to the DAC8760 and can be directly substituted for applications where 16-bit resolution is not required. Another option for a combined output is to use a discrete DAC, such as a DAC856x device, and the XTR300 output driver.

For designs that only require I_{OUT}, the DACx750 family offers 12-bit and 16-bit integrated solutions. A DAC856x device and the XTR111 output driver can be used for a discrete current only solution.

Any +36 V op amp can be used as the buffer amplifier in this design. However, as mentioned in Section 3.2, dc errors from the op amp combine with the dc errors of the DAC affecting the V_{OUT} performance. Therefore, selecting an op amp with low offset voltage, low offset drift, high CMRR, and high PSRR will prevent the op amp from reducing the performance of the DAC. The OPA192 is a precision e-trim™ device and other devices in this family will work well in this application. Devices in the zero-drift™ offset cancellation series such as the OPA188 are also very good options for the best drift and offset performance. Other +36 V amplifiers for this application are the OPA277, OPA170, or OPA140. Op amps for single-supply applications must have input and output stages that include the negative rail for proper operation.

Table 7: Alternate +36V Amplifiers

Amplifier	Typical Offset Voltage (µV)	Max Offset Voltage Over Temp (µV)	Typical Offset Drift (µV/°C)	Min CMRR (dB)	Max PSRR (µV/V)	Max Input Bias Current (pA)	Min Aol (dB)	Noise at 1 kHz (nV/√Hz)	Quiescent Current (mA)
OPA192	10	150	0.2	110	3	20	110	5.5	1
OPA188	6	33.5	0.03	114	0.3	1400	120	8.8	0.425
OPA277*	10	30*	0.1*	130*	0.5*	2800	126*	8	0.79
OPA170	250	2	0.3	104	5	15	110	19	0.110
OPA140	30	220	0.35	126	0.5	10	120	5.1	1.8

*OPA277 is only rated to +85°C where the other devices are rated to +125°C.

8 About the Authors

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

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9 Acknowledgements & References

1. *Collin Wells, Reza Abdullah, "Creating a Combined Voltage and Current Output with the DACx760" SBAA199, October 2013.*

Appendix A.

A.1 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure 13.

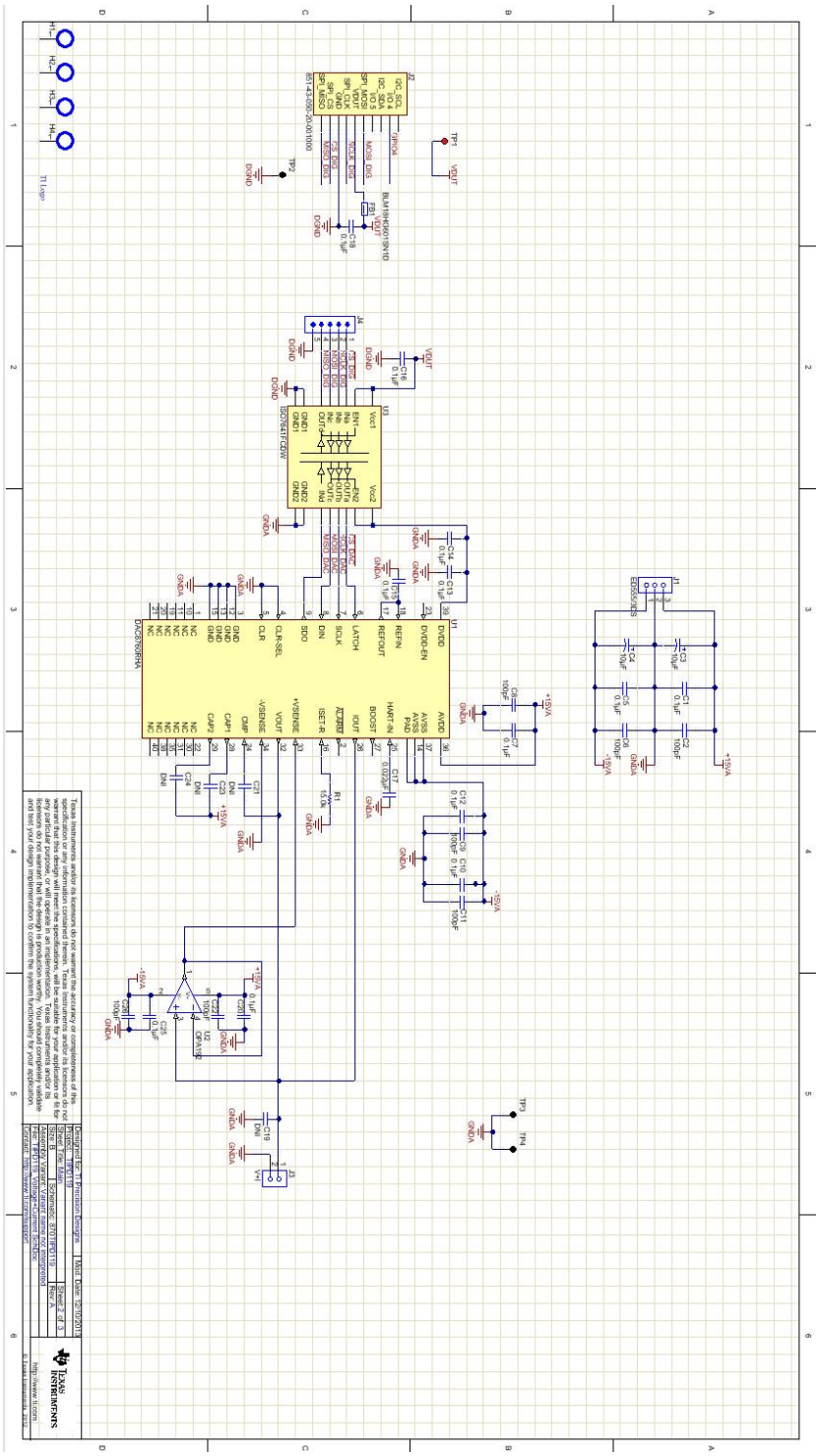

Figure 13: Altium Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 14.

Texas Instruments

Bill of Materials

TI DESIGNS

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	12	C1, C5, C7, C10, C12, C13, C14, C15, C16,	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H104KA93D
2	7	C2, C6, C8, C9, C11, C22, C26	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A101JAT2A
3	2	C3, C4	10uF	CAP, TANT, 10uF, 50V, +/-10%, 0.8 ohm, 7343-43 SMD	Vishay-Sprague	293D106X9050E2TE3
4	1	C17	0.022uF	CAP, CERM, 0.022uF, 50V, +/-10%, X7R, 0603	TDK	C1608X7R1H223K
5	4	C19, C21, C23, C24	1000pF	CAP, CERM, 1000pF, 100V, +/-10%, X7R, 0603	MuRata	GRM188R72A102KA01D
6	1	FB1		FERRITE CHIP 600 OHM 200MA 0603	MuRata	BLM18HG601SN1D
7	1	J1		TERMINAL BLOCK 3.5MM 3POS PCB	On Shore Technology Inc	ED555/3DS
8	1	J2		CONN SOCKET 50PIN .050 R/A SNGL	Mill-Max Manufacturing	851-43-050-20-001000
9	1	J3		TERMINAL BLOCK 3.5MM 2POS PCB	On Shore Technology Inc	ED555/2DS
10	1	J4		Header, TH, 100mil, 5x1, Gold plated	Samtec, Inc.	TSW-105-07-G-S
11	1	R1	DNI	RES, 15.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-153-B-T5
12	1	TP1		Test Point, Compact, Red, TH	Keystone	5005
13	3	TP2, TP3, TP4		Test Point, Compact, Black, TH	Keystone	5006
14	1	U1		Single-Channel, 16-Bit Programmable Voltage and	Texas Instruments	DAC8760RHA
15	1	U2		Precision e-Trim Op Amp	Texas Instruments	OPA192AIDBVT
16	1	U3		ISOLATOR DGTL 25MBPS 4CH 16SOIC	Texas Instruments Inc	ISO7641FCDW

Figure 14: Bill of Materials

Appendix B.

B.1 Single-Supply Result Summary

Table 8: Measured Result Summary

		Goals	Calculated	Measured
Current	**Offset (mV)**	N/A	+/-0.01	0.005
	Gain Error	N/A	+/-0.01	0.037
	INL	N/A	+/-0.024	0.009
	TUE	0.1%	+/-0.02	0.048
Voltage	**Offset (mV)**	N/A	+/-1	0.07
	Gain Error	N/A	+/-0.01	0.024
	INL	N/A	+/-0.022	0.006
	TUE	0.1%	+/-0.015	0.026

B.2 Single-Supply 0-24 mA I_{OUT} Results

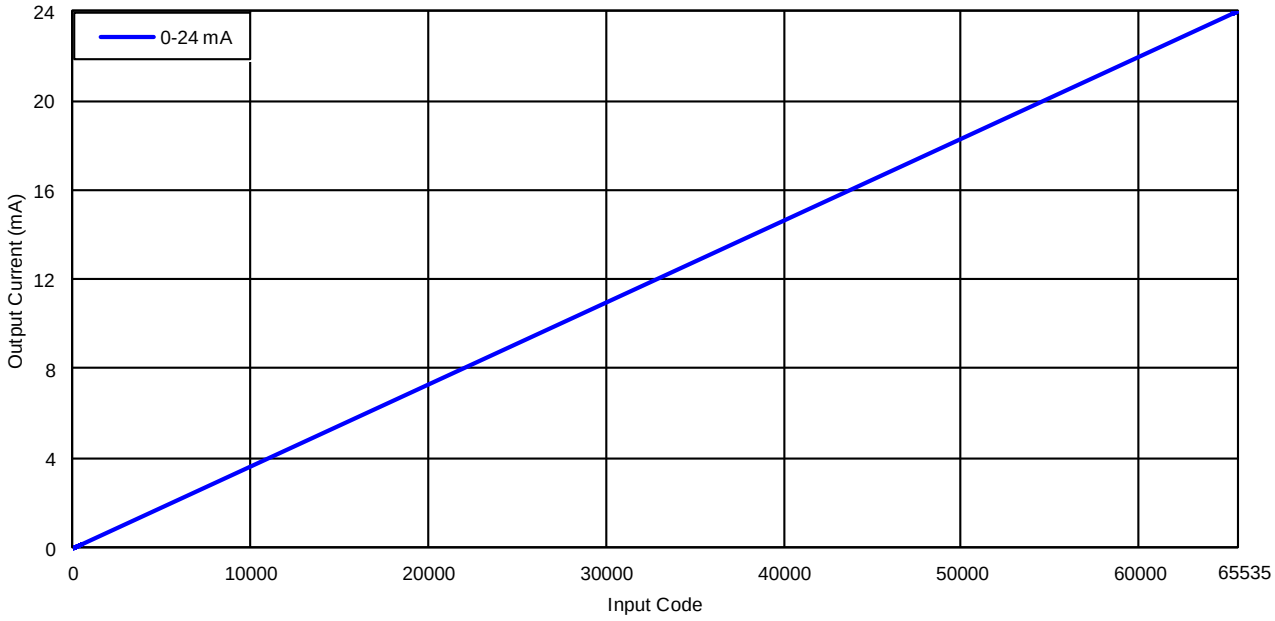

Figure 15. Single-Supply I_{OUT} 0-24 mA Output Transfer Function

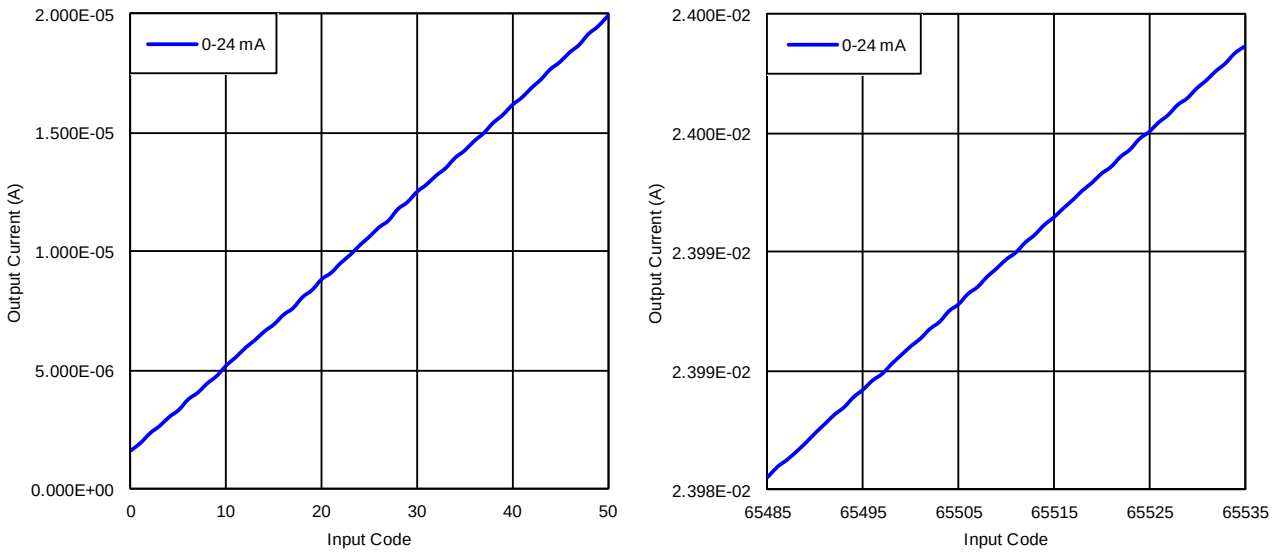

Figure 16. Single-Supply I_{OUT} 0-24 mA Zero-Scale and Full-Scale Outputs

B.3 Single-Supply 0-10V Results

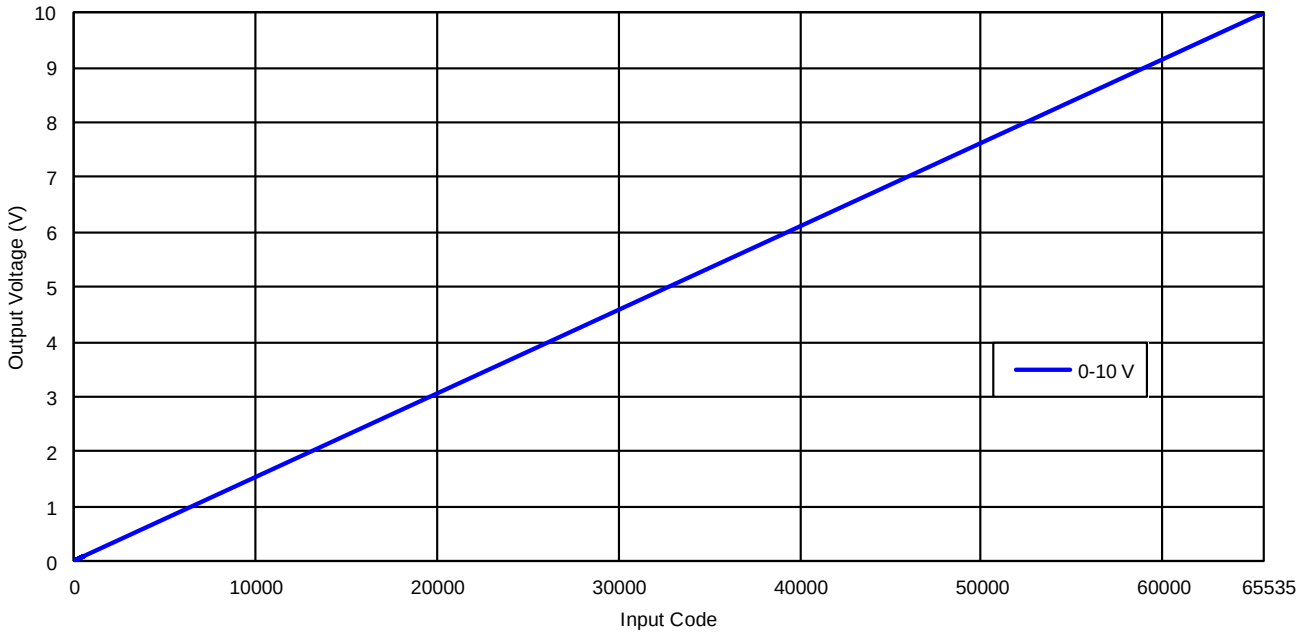

Figure 17. 0-10V Output Transfer Function

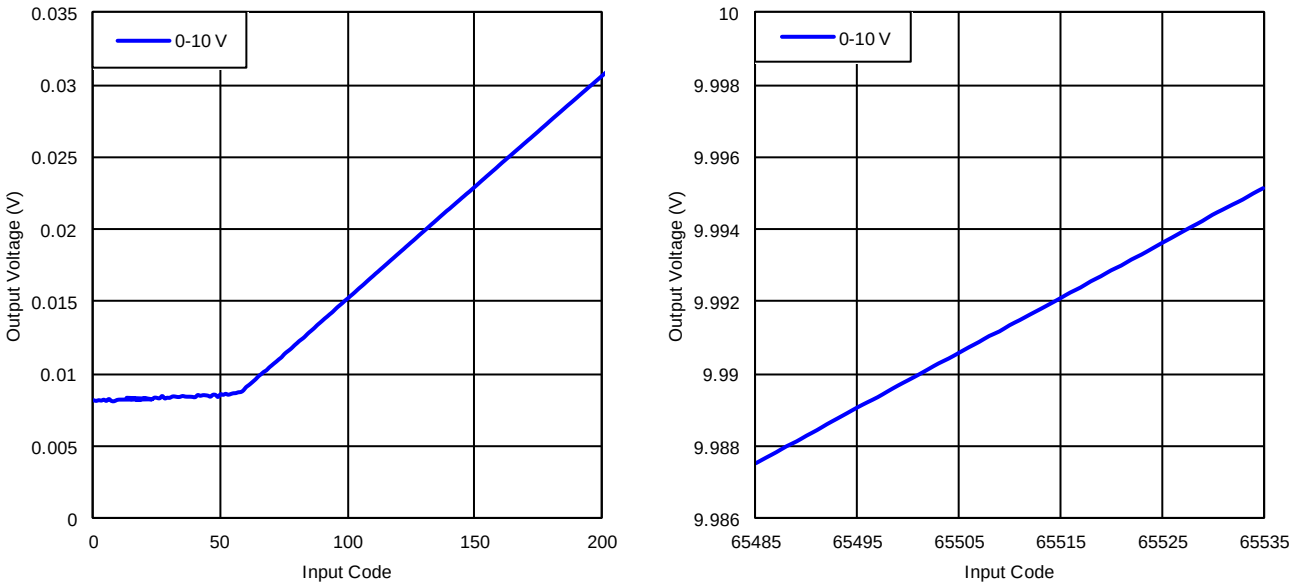

Figure 18. Single-Supply V_{OUT} Circuit 0-10 V Zero-Scale and Full-Scale Outputs

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