The ADC32RFxx-EVM is the circuit board for evaluating the ADC32RFxx family of analog-to-digital converters. This document is intended to guide the ADC32RFxx-EVM user through the process of setting up the EVM successfully. The configuration of the ADC32RF45, ADC32RF44, ADC32RF42, ADC32RF82 and ADC32RF80 in Digital Down-Convert (DDC) and Bypass-DDC modes with different clocking schemes are covered in this document. The steps for ADC32RF8x also apply to ADC31RF80 (Channel A). ADC31RF80 is a single channel variant.

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1 Overview

The ADC32RFxx-EVM is an evaluation module (EVM) designed to evaluate the ADC32RFxx family of high-speed, JESD204B interface ADCs. The EVM includes an onboard clocking solution (LMK04828), transformer-coupled analog inputs, full power solution, and easy-to-use software GUI and USB interface. The following features apply to this EVM:

- Transformer-coupled signal input network allowing a single-ended signal source from 30 MHz to 3000 MHz.
- LMK04828 system clock generator that generates field-programmable gate array (FPGA) reference clocks for the high-speed serial interface and may optionally be used to generate the ADC sampling clock.
- Transformer-coupled clock input network to test the ADC performance with a very low-noise clock source.
- LMX2582 (or LMX2592) clock synthesizer to generate a very low-noise clock source for clocking the ADC32RFxx ADC.
- High-speed serial data output over a standard FPGA Mezzanine Card (FMC) interface connector.
The ADC32RFxx-EVM is designed to work seamlessly with TI's TSW14J56 EVM JESD204B data capture/pattern generator card, through the High Speed Data Converter Pro (HSDC Pro) software tool for high-speed data converter evaluation. It is also designed to work with many of the development kits from leading FPGA vendors that contain an FMC connector.

1.1 **Required Hardware**

The following equipment is **included** in the EVM evaluation kit:
- ADC32RFxx evaluation board (EVM)
- Power supply cable
- Mini-USB cable

The following list of equipment are items that are **not included** in the EVM evaluation kit but are items required for evaluation of this product in order to achieve the best performance:
- TSW14J56EVM data capture board, two 5-V power supplies, and mini-USB cable
- Computer running Microsoft® Windows® XP, or newer
- One low-noise signal generator. **Recommendations:**
  - RF generator, > +17 dBm, < –40 dBc harmonics, < 500 fs jitter 20 kHz–20 MHz, 10-MHz to 3-GHz frequency range
    *Examples:* HP HP8644B, Rohde & Schwarz SMA100A
  - Bandpass filter for desired analog input. **Recommendations:**
    - Bandpass filter, ≥ 60-dB harmonic attenuation, ≤ 5% bandwidth, > +18-dBm power, < 5-dB insertion loss
    *Examples:* Trilithic 5VH-series Tunable BPF, K&L BT-series Tunable BPF, TTE KC6 or KC7-series Fixed BPF
- Signal path cables, SMA or BNC with BNC-to-SMA adapters

1.2 **Required Software**

The following software is required to operate the ADC32RF45 EVM and is available online. See the **References** section for links.
- ADC32RFxx EVM SPI GUI

The following software is required to operate the TSW14J56EVM and is available online. See the **References** section for links.
- High Speed Data Converter Pro software, version 4.2 or higher

1.3 **Evaluation Board Feature Identification Summary**

The EVM features are labeled in Figure 1.
Figure 1. EVM Feature Locations
1.4 References

Use the following links to available documentation and software:

- ADC32RF45 data sheet (SBAS747)
- ADC32RF45 product page [www.ti.com/product/ADC32RF45](http://www.ti.com/product/ADC32RF45)
- ADC32RF44 data sheet (SBAS809)
- ADC32RF44 product page [www.ti.com/product/ADC32RF44](http://www.ti.com/product/ADC32RF44)
- ADC32RF8x data sheet (SBAS774)
- ADC32RF80 product page [www.ti.com/product/ADC32RF80](http://www.ti.com/product/ADC32RF80)
- LMK04828 data sheet (SNAS605)
- TSW14J56EVM User's Guide (SLWU086)

NOTE: The EVM schematics, layout, and BOM are available on the ADC32RF45EVM tool page on [www.ti.com](http://www.ti.com).
2 Quick Start Guide

The EVM test procedure to obtain a valid data capture from the ADC32RFxx-EVM using the TSW14J56EVM capture card is provided in this section. This is the starting point for all evaluations.

2.1 Introduction

The ADC32RFxx-EVM includes the ADC32RF4x or ADC32RF8x analog-to-digital converter with JESD204B interface, and the LMK04828 clock chip to generate the device clock and SYSREF to the ADC. Also included on the EVM is the optional LMX2582 or LMX2592 clock synthesizer device. Jumpers and solder options on the EVM allow selection of the ADC sample clock from the LMX2582, the LMK04828, or from a transformer-coupled external SMA input. The default assembly option is the transformer-coupled external clocking option as set by jumper JP3. The EVM has an FMC connector suitable for connection to readily-available FPGA development boards or to the TSW14J56 capture card.

The FPGA on the capture card also requires a device clock and SYSREF signal and the LMK04828 clock device also supplies these signals to the FMC connector for that purpose.

This document is meant to convey all information needed to bring up the ADC32RFxx-EVM and TSW14J56 capture card and get valid data capture with a good FFT result.

The JESD204B interface requires a number of important parameters to be decided in advance of setting up the data link, such as; number of lanes, number of converters, number of samples per frame, and a value K number of frames per multi-frame, among other parameters. Both sides of a JESD204B link must be set up with the same values for all these parameters or else the FPGA that receives the data will not be able to establish a synchronized link. Getting these parameters inconsistent between ADC and FPGA is perhaps the biggest single reason for an EVM setup to not function as expected. The GUI installers that come with the ADC32RF4xx and the TSW14J56 come with configuration files that are meant to enable quick initial setup of a number of basic configurations. TI strongly suggests setting up the EVM and capture card with a configuration described in this document and getting a working setup before modifying the configuration to be closer to what the end-application requires. In this way the user can know that the hardware is functioning, and that there is a working configuration that they can go back to in the event of difficulty developing their own configuration.

The HSDC Pro GUI that comes with the TSW14J56 requires initialization files for both the decimation and mixer logic (DDC) and the non-decimated full-rate mode called LMF82820 or 5-sample mode. (LMF82820 mode means that there are 8 lanes in use for 2 channels of ADC, with 8 octets of information on each lane per frame, for 20 samples of data per frame per channel. That is equivalent to 5 samples per lane per frame, hence the mode being called 5 sample mode. 5 samples per lane times 8 lanes is 40 samples, or 20 samples per channel. This mode is sometimes called bypass mode because the decimation and mixer logic is bypassed in favor of full rate output.)

Please note that the configuration files for setting up the LMK04828 clocking device are different for the DDC case than they are for the non-decimation (5-sample) case. The different modes of operation of the ADC will affect the data rate on the JESD204B interface and thus affect the clocking needed for the FPGA. The configuration files are not interchangeable. For example, the LMK_ADC32RF45_bypass_2457Msps.cfg file and LMK_ADC32RF45_2457Msps.cfg file will both set the sample clock for the ADC at 2.4576 GHz, but the SYSREF and the device clock to the FPGA will be different for the two files.

This document introduces the software that must be installed on a PC, and presents a basic setup for the Bypass and DDC modes available in the ADC32RF45, both modes being clocked by an externally supplied clock. The LMK04828 clock chip supplies SYSREF to the ADC and clock and SYSREF to the TSW14J56. ADC32RF8x can be configured in DDC mode by following the same steps as that for ADC32RF45. ADC32RF44 only supports a maximum clock rate of 2.6 Gsps and an example configuration with internally generated clock (on-board LMX2582) is shown. The last section covers the steps to supply an internally-generated sample clock to the ADC, by either the LMK04828 or LMX2582.
2.2 Software Installation

The proper software must be installed before beginning evaluation. See Section 1.2 for a list of the required software. The References section of this document contains links to find the software on the TI website.

Important: The software must be installed before connecting the ADC32RFxx-EVM and TSW14J56 to the computer for the first time.

The ADC32RFxx-EVM is controlled through an easy-to-use graphical user interface (GUI) to provide access to the ADC (ADC32RF4x or ADC32RF8x), clock chip (LMK04828), and clock synthesizer (LMX2582 or LMX2592) SPI interfaces. There is a tab in the GUI for each of the devices. This GUI requires the LabVIEW™ runtime engine, which is automatically installed during the loading of the software.

2.2.1 ADC32RFxx EVM GUI Installation

1. Copy the provided installer software called ADC32RFxx EVM GUI Installer.zip (or newer revision on the TI web, if available) under the ADC32RFxx Customer Files\Software folder to a local host PC.
2. Unzip the installer.
3. Go to ADC32RF4xx EVM SPI GUI Installer\Volume and double click on setup.exe.
4. Follow the installer instructions. After the installer is completed, the executable is located at C:\Program Files(86)\Texas Instruments\ADC32RFxx EVM GUI
5. Start the GUI by double clicking on ADC32RFxx EVM GUI.exe or Start Menu → All Programs → Texas Instruments → ADC32RFxxGUI.
6. When plugging the board into the computer for the first time through the USB cable, you may be prompted to install the USB drivers.
   • Windows XP: If Windows XP does not automatically install the drivers, follow the prompts on the screen to do so. Do not let Windows XP search Microsoft Update for the drivers, but do let Windows XP install the drivers automatically.
   • Windows 7: After installing the GUI, Windows 7 should automatically be able to install the drivers for the ADC32RFxx-EVM with no input from the user.

2.2.2 High Speed Data Converter Pro GUI Installation

High Speed Data Converter Pro (HSDC Pro) is used to control the TSW14J56EVM and analyze the captured data. Please see the HSDC Pro GUI user’s guide (SLWU087) for more information.

1. Download HSDC Pro from the TI website. The References section of this document contains the link to find the software on the TI website.
2. Extract the files from the zip file.
3. Run setup.exe and follow the installation prompts.
4. If the version of HSDC Pro is 4.5 or lower, download HSDC Pro GUI updates from the TI website. The References section of this document contains the link to find the software on the TI website.
5. Extract the files from the zip file, run HSDC Pro Patch vx.xx.exe and follow the installation instructions.
2.3  **Hardware Setup Procedure**

A typical test setup using the ADC32RFxx-EVM and TSW14J56EVM is shown in Figure 2. This is the test setup used for the quick-start procedure.

![ADC32RFxx-EVM GUI Bench Setup Block Diagram](image-url)

**Figure 2. ADC32RFxx-EVM GUI Bench Setup Block Diagram**
Quick-Start Procedure for Bypass LMFS82820 Mode in ADC32RF45

This mode is available only in the ADC32RF4x family and is not available in ADC32RF8x family of devices. Please check the package marking on the ADC to confirm compatibility of the device mounted on the EVM with this mode.

3.1 TSW14J56

1. Connect the ADC32RFxx EVM to the TSW14J56 using the FMC connectors.
2. Connect a 5-V power supply to connector J11 (+5V IN).
3. Connect a USB cable to the USB connector (J9).
4. Flip the power switch (SW6) to the “ON” position.

3.2 ADC32RFxx EVM

1. Verify the clocking selection jumper JP3 is set to EXT for external clocking.
2. Connect a 5-V, 3-A power supply to connector J15. Do not use a supply that is rated less than 3 A.
3. Connect a USB cable to the USB connector (J11 bottom side of board).
4. Connect an analog RF signal from the signal source to the AINP SMA (J2).
5. Connect a signal generator set for 2.94912 GHz to the external clock input J5.
6. Connect another signal generator set for 2.94912 GHz to the LMK04828 reference clock input J7. (Make sure the two signal generators for the ADC clock and LMK04828 clock are synchronized to the same timebase, or use a single signal generator and a splitter to generate two copies of the clock to go to the EVM.)

Fs = 2.94912 GHz, 5-Sample Example

This example captures data from channel A of the ADC32RFxx EVM sampling at 2.94912 GHz with a 1900-MHz input source. The ADC requires the device clock and SYSREF signals to be present before the ADC can be properly configured. The steps to configure into this mode follow:

1. Open the ADC32RFxx EVM GUI.
2. Verify that the green USB Status indicator is lit. If it is not lit, click the Reconnect? button and check the USB Status indicator again. If it is still not lit then verify the EVM is connected to the computer through USB. Whenever the USB link is disturbed, the GUI must obtain a new handle to address the proper USB port, and the Reconnect? button does that.
3. On the PLL1 tab of the LMK04828 tab, press the RESET button.

Fs = 2.94912 GHz, 5-Sample Example

This example captures data from channel A of the ADC32RFxx EVM sampling at 2.94912 GHz with a 1900-MHz input source. The ADC requires the device clock and SYSREF signals to be present before the ADC can be properly configured. The steps to configure into this mode follow:

1. Open the ADC32RFxx EVM GUI.
2. Verify that the green USB Status indicator is lit. If it is not lit, click the Reconnect? button and check the USB Status indicator again. If it is still not lit then verify the EVM is connected to the computer through USB. Whenever the USB link is disturbed, the GUI must obtain a new handle to address the proper USB port, and the Reconnect? button does that.
3. On the PLL1 tab of the LMK04828 tab, press the RESET button.

Figure 3. ADC32RFxx-EVM GUI LMK04828 PLL1 Page Bypass Mode

4. On the ADC32RFxx-EVM, press SW1 (ADC RESET) to provide a hardware reset to the ADC.
5. Click on the Quick Setup tab.

6. Select the Nyquist Zone for the input. It will be 2nd Nyquist in this example setup (Fs = 2949.12M, Fin = 1900M).

7. Select the Clock Source to ADC. In this example, External Clocking is selected.

8. Select ADC32RF45 Mode. In this example, Bypass is chosen.

9. Select Resolution. In this example, 12 bit is selected.

10. Press PROGRAM EVM.
11. After pressing the **PROGRAM EVM** button, the device will be configured as shown in Figure 4 and Figure 5 indicating the 12 bit packed 5 sample mode for LMFS82820.

![ADC32RFxx-EVM GUI JESD204B Tab Bypass Mode](image)

**Figure 5. ADC32RFxx-EVM GUI JESD204B Tab Bypass Mode**

### 3.3 High Speed Data Converter Pro (HSDC Pro)

1. Open High Speed Data Converter Pro (v4.5 or newer) by going to **Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro**.

2. Click **OK** to connect to the TSW14J56. If there is more than one TSW14J56 connected to the host PC, select the appropriate serial number of the board to be programmed.

3. Select the **ADC** tab at the top of the GUI.

4. Use the **Select ADC** drop-down menu at the top left corner to select **ADC32RF45_LMF_82820**.

![HSDC Pro Device Selection LMFS_82820 Mode](image)

**Figure 6. HSDC Pro Device Selection LMFS_82820 Mode**
5. When prompted to update the firmware for the ADC, click Yes and wait for the firmware to download to the TSW14J56.

6. After the firmware download has completed, enter “2949.12M” into the ADC Output Data Rate field at the bottom left corner of the HSDC Pro GUI.

7. Select “Channel 1/2” in the channel select window located at the top middle of the GUI.

8. Click the Instrument Options menu at the top of HSDC Pro and select Reset Board.

9. Click the Capture button in HSDC Pro to capture data from the ADC.

10. The result should match the example capture in Figure 7.

Figure 7. Example Capture from Channel A – Bypass Mode
Quick-Start Procedure for Digital DDC (Decimation Plus NCO) Mode in ADC32RF82

The clock rate in this example is 2Gsp.

4.1 TSW14J56
1. Connect the ADC32RF82 EVM to the TSW14J56 using the FMC connectors.
2. Connect a 5-V power supply to connector J11 (+5 V IN).
3. Connect a USB cable to the USB connector (J9).
4. Flip the power switch (SW6) to the "ON" position.

4.2 ADC32RF82 EVM
1. Verify jumper JP3 is set for position EXT to select external clocking.
2. Connect a 5-V, 3-A power supply to connector J15. Do not use a supply that is rated less than 3 A.
3. Connect a USB cable to the USB connector (J11 on the bottom side of board).
4. Connect an analog RF signal from a signal source to the AINP SMA (J2).
5. Connect a signal generator set at 2 GHz to the external clock input J5.
6. Connect another signal generator set for 2 GHz to the LMK04828 reference clock input J7. (Make sure the two signal generators for the ADC clock and LMK04828 clock are synchronized to the same timebase, or use a single signal generator and a splitter to generate two copies of the clock to go to the EVM.)

Fs = 2 GHz, 8x Decimation Example, External Clocking

This example captures 8x decimated data from channel A of the ADC32RF82 EVM sampling at 2 GHz with a 1860-MHz RF input source. The ADC requires the device clock and SYSREF signals to be present before the ADC can be properly configured so the LMK (and optional LMX, if used) setup must have been done before configuring the ADC.
1. Open the ADC32RFxx EVM GUI.
2. Verify that the green USB Status indicator is lit. If it is not lit, click the Reconnect? button and check the USB Status indicator again. If it is still not lit then verify the EVM is connected to the computer through USB. Whenever the USB link is disturbed, the GUI must obtain a new handle to address the proper USB port, and the Reconnect? button does that.
3. On the LMK04828 PLL1 tab, press the **RESET** button.
4. On the ADC32RFxx-EVM, press SW1 (**ADC RESET**) to provide a hardware reset to the ADC.
5. Click on the **Quick Setup** tab.
6. Select the **Nyquist Zone** for the input. It will be 2nd Nyquist in this example setup (Fs=2000M, Fin=1860M).
Figure 9. ADC32RFxx-EVM Quick Setup View DDC Mode

7. Select the Clock Source to ADC. In this example, External Clocking is selected.
8. Select ADC32RF45 Mode. In this example, DDC is chosen.
9. Press the PROGRAM EVM button.
10. After pressing the **PROGRAM EVM** button, the device will be configured as shown in Figure 9 and Figure 10.

Figure 10. ADC32RFxx-EVM GUI JESD204B Configuration Tab DDC Mode
Figure 11. ADC32RFxx-EVM GUI DDC Configuration Tab

11. Enter "2000" in the box for Sample Clock rate in MHz.

12. Enter "1850" in the box for the Channel A DDC0 NCO1 frequency. The control value for NCO1 should become 60621 as shown in Figure 11.

**NOTE:** These settings only apply with Fs = 2000 MHz. The NCOs in the ADC32RFxx are set to a desired LO frequency by a numeric control that is a fraction of the sampling frequency. If the sampling frequency changes, then the NCO frequency changes. In order to find the input tone in the resulting FFT capture, the sampling frequency and the NCO frequency must be known in order to know where the input tone should be located in the final FFT result.
4.3 **High Speed Data Converter Pro (HSDC Pro)**

1. Open High Speed Data Converter Pro by going to **Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro**.

2. Click **OK** to connect to the TSW14J56. If there is more than one TSW14J56 connected to the host PC, select the appropriate serial number of the board to be programmed.

3. Select the **ADC** tab at the top of the GUI.

4. Use the **Select ADC** drop-down menu at the top left corner to select **ADC32RF80_LMF_8821** as Figure 13 shows.

5. When prompted to update the firmware for the ADC, click **Yes** and wait for the firmware to download to the TSW14J56. The following message appears while the firmware is downloading to the FPGA. (Downloading firmware does not mean the GUI is looking for newer revisions at ti.com. It simply means the bitfile for the firmware for the FPGA is being pushed to the FPGA through the USB cable.)
6. After the firmware download has completed, enter “250M” into the ADC Output Data Rate field at the bottom left corner of the HSDC Pro GUI (2 GHz sample rate divided by 8). A common mistake is to type ‘m’ instead of ‘M’ in which case the frequency entered is in milli-Hz instead of mega-Hz. Another common mistake is to omit the ‘M’ in which case the frequency entered is in Hz.

7. Select “Channel 1/8” in the channel select window located at the top middle of the GUI.

8. Click the Instrument Options menu at the top of HSDC Pro and select Reset Board.

9. Click Capture in HSDC Pro to capture data from the ADC.

10. Select Complex FFT

11. The result should match the example capture in Figure 17.

   The input tone is seen to be near 10 MHz because the signal generator is set to 1.86 GHz while the NCO in the ADC is set to 1.85 GHz. So, the input tone is mixed down to 10 MHz. If the signal generators for the analog input tone and the clocking are synchronized, then HSDC Pro is able to locate the expected tone after the NCO and decimation by way of the popup parameter window of Figure 16. If this popup is used, the frequency values entered must be exact.
Figure 17. Example Capture From Channel A – 8x Decimation Mode
Quick-Start Procedure for Digital DDC (Decimation Plus NCO) Mode in ADC32RF4x and ADC32RF8x

The clock rate in this example is 2.94912 Gsps and is only supported by the ADC32RF45 and ADC32RF80. For the ADC32RF44, the same steps can be followed, albeit at a lower clock rate (≤ 2.6 Gsps).

5.1 TSW14J56

Follow these steps to use the TSW14J56 with the ADC32RFxx EVM:
1. Connect the ADC32RFxx EVM to the TSW14J56 using the FMC connectors.
2. Connect a 5-V power supply to connector J11 (+5 V IN).
3. Connect a USB cable to the USB connector (J9).
4. Flip the power switch (SW6) to the “ON” position.

5.2 ADC32RFxx EVM

Use the following steps to prepare the ADC32RFxx EVM for use:
1. Verify jumper JP3 is set for position EXT to select external clocking.
2. Connect a 5-V, 3-A power supply to connector J15. Do not use a supply that is rated less than 3 A.
3. Connect a USB cable to the USB connector (J11 on the bottom side of board).
4. Connect an analog RF signal from a signal source to the AINP SMA (J2).
5. Connect a signal generator set for 2.94912 GHz to the external clock input J5.
   (Make sure the two signal generators for the ADC clock and LMK04828 clock are synchronized to the same timebase, or use a single signal generator and a splitter to generate two copies of the clock to go to the EVM.)

Fs = 2.94912 GHz, 8x Decimation Example, External Clocking

This example captures 8x decimated data from channel A of the ADC32RFxx EVM sampling at 2.94912 GHz with a 1960-MHz IF input source. **The ADC requires the device clock and SYSREF signals to be present before the ADC can be properly configured so the LMK (and optional LMX, if used) setup must be done before configuring the ADC.**
1. Open the ADC32RFxx EVM GUI.
2. Verify that the green USB Status indicator is lit. If it is not lit, click the Reconnect? button and check the USB Status indicator again. If it is still not lit then verify the EVM is connected to the computer through USB. Whenever the USB link is disturbed, the GUI must obtain a new handle to address the proper USB port, and the Reconnect? button does that.
3. On the LMK04828 PLL1 tab, press the **RESET** button.
4. On the ADC32RFxx-EVM, press SW1 (**ADC RESET**) to provide a hardware reset to the ADC.
5. Click on the **Quick Setup** tab.
6. Select the **Nyquist Zone** for the input. It will be 2nd Nyquist in this example setup (Fs=2949.12M, Fin=1960M).
7. Select the **Clock Source to ADC**. In this example, **External Clocking** is selected.

8. Select **ADC32RF45 Mode**. In this example, **DDC** is chosen.

9. Press the **PROGRAM EVM** button.
10. After pressing the **PROGRAM EVM** button, the device is configured as shown in **Figure 19** and **Figure 20**, indicating the 12-bit packed, 5-sample mode for LMFS82820.

**Figure 20. ADC32RFxx-EVM GUI JESD204B Configuration Tab DDC Mode**
11. Enter "2949.12" in the box for Sample Clock rate in MHz.

12. Enter "1900" in the box for the Channel A DDC0 NCO1 frequency. The control value for NCO1 should become 42222 as shown in Figure 21.

**NOTE:** These settings only apply with Fs = 2.94912 GHz. The NCOs in the ADC32RF80 are set to a desired LO frequency by a numeric control that is a fraction of the sampling frequency. If the sampling frequency changes, then the NCO frequency changes. In order to find the input tone in the resulting FFT capture, the sampling frequency and the NCO frequency must be known in order to know where the input tone should be located in the final FFT result.
5.3 High Speed Data Converter Pro (HSDC Pro)

1. Open High Speed Data Converter Pro by going to Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro.

2. Click OK to connect to the TSW14J56. If there is more than one TSW14J56 connected to the host PC, select the appropriate serial number of the board to be programmed.

3. Select the ADC tab at the top of the GUI.

4. Use the Select ADC drop-down menu at the top left corner to select ADC32RF80_LMF_8821 as Figure 23 shows.

5. When prompted to update the firmware for the ADC, click Yes and wait for the firmware to download to the TSW14J56. The following message appears while the firmware is downloading to the FPGA. (Downloading firmware does not mean the GUI is looking for newer revisions at ti.com. It simply means the bitfile for the firmware of the FPGA is being pushed to the FPGA through the USB cable.)
6. After the firmware download has completed, enter “368.64M” into the **ADC Output Data Rate** field at the bottom left corner of the HSDC Pro GUI (2.94912 GHz sample rate divided by 8). A common mistake is to type ‘m’ instead of ‘M’ in which case the frequency entered is in milli-Hz instead of mega-Hz. Another common mistake is to omit the ‘M’ in which case the frequency entered is in Hz.

7. Select “Channel 1/8” in the channel select window located at the top middle of the GUI.

8. Click the **Instrument Options** menu at the top of HSDC Pro and select **Reset Board**.

![Figure 25. Resetting the TSW14J56](image)

9. Click **Capture** in HSDC Pro to capture data from the ADC.

10. Select **Complex FFT**

11. The result should match the example capture in **Figure 27**.

   The input tone is seen to be near 60 MHz because the signal generator is set to 1.96 GHz while the NCO in the ADC is set to 1.90 GHz. So, the input tone is mixed down to 60 MHz. If the signal generators for the analog input tone and the clocking are synchronized, then HSDC Pro is able to locate the expected tone after the NCO and decimation by way of the popup parameter window of **Figure 26**. If this popup is used, the frequency values entered must be exact.

![Figure 26. Popup Window for Setting HSDC Pro Decimation Factor and NCO Frequency](image)
Figure 27. Example Capture From Channel A – 8x Decimation Mode
6 Quick-Start Procedure for Bypass LMFS8224 Mode in ADC32RF44 and Internal Clocking

This section lists the steps to configure ADC32RF44 in bypass mode. The steps are the same as that in Section 3 with lower clock rate being the only difference.

6.1 TSW14J56

Please follow the steps listed in Section 3.1.

6.2 ADC32RF44 EVM

Please follow the steps listed in Section 3.2, with the exception of steps 5 and 6. Instead of supplying an external clock as was done in steps 5 and 6, we will supply the clocking from the onboard LMX2582 frequency synthesizer.

Fs = 2.4576 GHz, LMFS 8224 Example

This example captures data from channel A of the ADC32RF44 EVM sampling at 2.4576 GHz with a 1800-MHz input source. The ADC requires the device clock and SYSREF signals to be present before the ADC can be properly configured. Use the following steps to configure into this mode:

1. Open the ADC32RFxx EVM GUI.
2. Verify that the green USB Status indicator is lit. If it is not lit, click the Reconnect? button and check the USB Status indicator again. If it is still not lit then verify the EVM is connected to the computer through USB. Whenever the USB link is disturbed, the GUI must obtain a new handle to address the proper USB port, and the Reconnect? button does that.
3. On the PLL1 tab of the LMK04828 tab, press the RESET button.
4. On the ADC32RF44-EVM, press SW1 (ADC RESET) to provide a hardware reset to the ADC.
5. Click on the Quick Setup tab.
6. Select the Nyquist Zone for the input. It will be 2nd Nyquist in this example setup (Fs = 2.4576M, Fin = 1800M).
7. Select the Clock Source to ADC. In this example, LMX2582 is used to Clock the ADC.
8. Select the Internal Clk Freq. In this example, 2457.6 Msps is selected.
9. Select ADC32RF45 Mode. In this example, Bypass is chosen.
10. Select Resolution. In this example, 14 bit is selected.
11. Press PROGRAM EVM.
12. After pressing the PROGRAM EVM button, the device will be configured in 14 bit LMFS8224 LMFS mode.
6.3 High Speed Data Converter Pro (HSDC Pro)

1. Open High Speed Data Converter Pro (v4.5 or newer) by going to Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro.
2. Click OK to connect to the TSW14J56. If there is more than one TSW14J56 connected to the host PC, select the appropriate serial number of the board to be programmed.
3. Select the ADC tab at the top of the GUI.
4. Use the Select ADC drop-down menu at the top left corner to select ADC32RF45_LMF_8224.

![Figure 29. HSDC Pro Device Selection LMFS_824 Mode](image)

5. When prompted to update the firmware for the ADC, click Yes and wait for the firmware to download to the TSW14J56.
6. After the firmware download has completed, enter “2949.12M” into the ADC Output Data Rate field at the bottom left corner of the HSDC Pro GUI.
7. Select “Channel 1/2” in the channel select window located at the top middle of the GUI.
8. Click the Instrument Options menu at the top of HSDC Pro and select Reset Board.
9. Click Capture in HSDC Pro to capture data from the ADC.
10. The result should match the example capture in Figure 30.

![Figure 30. Example Capture from Channel A – LMFS8224 Mode](image)
Quick-Start Procedure for Bypass LMFS 42810 Mode in ADC32RF42 With Internal Clocking

This section lists the steps to configure ADC32RF42 in 12-bit bypass mode. The steps are the same as those listed in Section 3 with a lower clock rate. The ADC32RF42 is internally 2-way interleaved instead of 4-way interleaved as with the ADC32RF45, so many aspects of the operation of the EVM are halved. The maximum sample rate is 1536 MSPS, half of what the ADC32RF45 would support. The number of lanes used to transmit the data is halved when in bypass mode, so the LMFS 82820 lane configuration used by the ADC32RF45 becomes LMFS 42810 with the ADC32RF42. It is important to note that many of the decimation modes while using the DDC functions are not halved, and the number of lanes and the LMFS formats are the same as with the 4-way interleaved device. What is halved is the amount of effective decimation after setting the decimation factor. For example, to get a decimation factor of 8 with the ADC32RF42 the SPI register field would be set with the value that would previously have been used to get a decimation factor of 16 with the ADC32RF45. This may lead to confusion when using the SPI GUI with the ADC32RF42 and seeing a decimation factor of 16 being reported by the GUI when it is really decimation by 8 when the ADC32RF42 is being used. The configuration files supplied with the GUI for the ADC32RF42 already take this difference in decimation factor into account.

7.1 TSW14J56
Follow the steps listed in Section 3.1.

7.2 ADC32RF42 EVM
Follow the steps listed in Section 3.2, with the exception of steps 5 and 6. Instead of supplying an external clock as was done in steps 5 and 6, we will supply the clocking from the onboard LMX2582 frequency synthesizer.

Fs = 1.536 GHz, LMFS 42810 Example
This example captures data from channel A of the ADC32RF42 EVM sampling at 1.536 GHz with a 900-MHz input source. The ADC requires the device clock and SYSREF signals to be present before the ADC can be properly configured. Use the following steps to configure into this mode:
1. Open the ADC32RFxx EVM GUI.
2. Verify that the green USB Status indicator is lit. If it is not lit, click the Reconnect? button and check the USB Status indicator again. If it is still not lit then verify the EVM is connected to the computer through USB. Whenever the USB link is disturbed, the GUI must obtain a new handle to address the proper USB port, and the Reconnect? button does that. When the GUI is first launched or the Reconnect? button is used, the GUI will query the EVM for the type of EVM and the GUI will display the EVM type. In this case, ADC32RF42 should be displayed.
3. On the PLL1 tab of the LMK04828 tab, press the RESET button.
4. On the ADC32RF42-EVM, press SW1 (ADC RESET) to provide a hardware reset to the ADC.
5. Click on the Quick Setup tab.
6. Select the Nyquist Zone for the input. It will be 2nd Nyquist in this example setup (Fs = 1.536M, Fin = 900M).
7. Select the Clock Source to ADC. In this example, LMX2582 is used to clock the ADC.
8. Select the Internal Clk Freq. In this example, 1536 Msps is selected. (Upon first launch of the GUI, the default clock rate selection may be grayed out if the clock rate is too fast or too slow for the ADC. If the GUI comes up with a grayed out selection then a valid selection must be chosen before pressing PROGRAM EVM, else an error message will pop up saying that a config file for this clock rate could not be found.)
9. Select ADC32RF45 Mode. In this example, Bypass is chosen.
10. Select Resolution. In this example, 12 bit is selected.
11. Press PROGRAM EVM.
12. After pressing the PROGRAM EVM button, the device will be configured in 12-bit, LMFS 42810 LMFS mode.
7.3 High Speed Data Converter Pro (HSDC Pro)

1. Open High Speed Data Converter Pro (v4.5 or newer) by going to Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro.

2. Click OK to connect to the TSW14J56. If there is more than one TSW14J56 connected to the host PC, select the appropriate serial number of the board to be programmed.

3. Select the ADC tab at the top of the GUI.

4. Use the Select ADC drop-down menu at the top left corner to select ADC32RF45_LMF_42810. (If this device selection is not available, a newer version of HSDCPro may need to be downloaded or a device .ini file for the mode may be obtained from TI and copied into the HSDCPro installation.)

5. When prompted to update the firmware for the ADC, click Yes and wait for the firmware to download to the TSW14J56.

6. After the firmware download has completed, enter “1536M” into the ADC Output Data Rate field at the bottom left corner of the HSDC Pro GUI.

7. Select “Channel 1/2” in the channel select window located at the top middle of the GUI.

8. Click the Instrument Options menu at the top of HSDC Pro and select Reset Board.

9. Click Capture in HSDC Pro to capture data from the ADC.

10. The result should match the example capture in Figure 33.

Figure 32. HSDC Pro Device Selection LMFS_42810 Mode
Figure 33. Example Capture from Channel A – LMFS42810 Mode
8 ADC32RFxx Internally Generated Clocking

8.1 ADC32RF45 EVM LMX2582 (or LMX2592) Clocking

Set up the TSW14J56 and ADC32RF45 the same way as it was set up for external clocking, but with the following modifications for internal clocking. Section 6 has already demonstrated the use of the LMX2582 for generating the clocking internal to the EVM, but this section covers more completely the use of either the LMX2582 or LMK04828 for clocking the ADC.

1. Verify the clocking selection jumper JP3 is set to the INT position to select the clock to the ADC to be generated on the EVM, either by the LMX2582 or the LMK04828. The default configuration for the EVM is for the LMX2582 to be the clock source to the ADC while in internal clock mode. (To select the LMK04828 as the ADC clock source, there are two AC coupling caps to unsolder and resolder in a different position.) There need not be any input to the J5 external clock SMA. If the LMK04828 is to be synchronized to the timebase of the signal generator used for the analog input, then connect the 10-MHz sync signal from the signal generator to the LMK04828 reference input J7.

2. All but one step to configure the device in this mode are the same as previously described in Section 3.2. The only step different is the choice of Clock Source to ADC. That step is to be selected as shown in Figure 34. The rest of the steps in Section 3.2 must be followed.

![Figure 34. ADC32RFxx EVM GUI With LMX Clock Configuration](image-url)
8.2 ADC32RF45 EVM LMK04828 Clocking

Set up the TSW14J56 and ADC32RF45 as before, with the following exceptions for internally generated clocking:

1. Verify the clocking selection jumper JP3 is set to the INT position to select the clock to the ADC to be generated on the EVM, either by the LMX2582 or the LMK04828. The default configuration for the EVM is for the LMX2582 to be the clock source to the ADC while in internal clock mode. Unsolder the two AC coupling caps from positions C409 and C410 and solder them into positions C431 and C432. This disconnects the ADC device clock from the LMX2582 outputs and instead connects the LMK04828 device clock output to be the clock source to the ADC. There need not be any input to the J5 external clock SMA. If the LMK04828 is to be synchronized to the timebase of the signal generator used for the analog input, then connect the 10-MHz sync signal from the signal generator to the LMK04828 reference input J7. The LMK04828 is still used to supply SYSREF to the ADC and Clock and SYSREF to the TSW14J56.

2. All but one step to configure the device in this mode are the same as previously described in Section 3.2. The only step different is the choice of Clock Source to ADC. That step is to be selected as shown in Figure 35. The rest of the steps in Section 3.2 must be followed.

![Figure 35. ADC32RFxx EVM GUI With LMK Clock Configuration](image-url)
Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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<td>• Added ADC32RF82 to list of supported devices in the abstract.</td>
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<td>• Added Quick-Start Procedure for Digital DDC (Decimation Plus NCO) Mode in ADC32RF82 section.</td>
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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

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Concernant les EVMs avec appareils radio:

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Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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http://www.tij.co.jp/lstds/itja/general/eStore/notice_01.page

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3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.
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