This user’s guide describes the function and use of the TSW54J60 evaluation module (EVM). Included in this document are a quick-start guide, instructions for optimizing evaluation results, software description, alternate hardware configurations, and jumper, connector, and LED descriptions.

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Overview

The TSW54J60EVM is an evaluation module (EVM) designed to evaluate the ADS54J60, LMH6401, LMH3401, and LMK04828 devices. The EVM has the LMH6401 fully-differential, ultra-wideband, digitally-controlled, variable-gain amplifier (DVGA) feeding one channel of the ADS54J60, 16-bit, 1-GSPS analog to digital converter. The LMH3401, a fully differential, ultra-wideband fixed gain amplifier is connected to the second channel of the ADC. Between the amps and ADC is a 400 MHz low-pass filter that can be modified for other custom applications. The EVM includes an onboard clocking solution (LMK04828), options for true fully-differential inputs, full power solution, and easy-to-use software GUI controlled through a USB interface.

The following features apply to this EVM:

• Amplified 50-Ω single-ended (default) or 100-Ω differential inputs that can be either AC (default mode) or DC coupled, allowing testing with a signal source from DC to 400 MHz (LPF 3-dB cutoff).
• LMK04828 system clock generator that generates field-programmable gate array (FPGA) reference clocks for the high-speed serial interface and may be used to generate the ADC sampling clock (default setting)
• Transformer-coupled ADC clock input network to test the ADC performance with an external, low-noise clock source
• High-speed serial data output over a standard FPGA Mezzanine Card (FMC) interface connector

The TSW54J60EVM is designed to work seamlessly with the TSW14J56EVM, Texas Instruments’ JESD204B data capture/pattern generator card, through the High-Speed Data Converter Pro (HSDC Pro) software tool for high-speed data converter evaluation. The TSW54J60EVM was also designed to work with many of the development kits from leading FPGA vendors that contain an FMC connector.

1.1 Required Hardware

The following equipment is included in the EVM evaluation kit:

• TSW54J60 Evaluation Board (EVM)
• Input Power cable
• Mini-USB cable

The following list of equipment are items that are not included in the EVM evaluation kit but are items required for evaluation of this product in order to achieve the best performance:

• TSW14J56EVM Data Capture Board, +5-V power supply and USB cable
• 5-VDC, 3-A power supply, HP E3631A or equivalent
• Computer running Microsoft® Windows® 8, Windows 7, or Windows XP
• One Low-Noise Signal Generator. Recommendations:
  – RF generator, > +10 dBm, < –40 dBc harmonics, < 500 fs jitter 20 kHz–20 MHz, 10-MHz to 500-MHz frequency range
  – Examples: TSW2170EVM, HP HP8644B, Rohde & Schwarz SMA100A
• Bandpass filter for desired analog input. Recommendations:
  – Bandpass filter, ≥ 60-dB harmonic attenuation, ≤ 5% bandwidth, > +18-dBm power, < 5-dB insertion loss
  – Examples: Trilithic 5VH-series Tunable BPF, K&L BT-series Tunable BPF, TTE KC6 or KC7-series Fixed BPF
• Signal path cables, SMA and/or BNC with BNC-to-SMA adapters
  – 6-dB attenuator
1.2 Required Software
The following software is required to operate the TSW54J60EVM and is available online. See References, Section 1.4 for links.

- ADS54Jxx EVM GUI
The following software is required to operate the TSW14J56EVM and is available online. See References, Section 1.4 for links.
- High Speed Data Converter Pro software

1.3 Evaluation Board Feature Identification Summary
The EVM features are labeled in Figure 1.

![Figure 1. EVM Feature Locations](image)

1.4 References

**NOTE:** Schematics, layout, and BOM are available on the TSW54J60EVM product page on [www.ti.com](http://www.ti.com).
2 Quick Start Guide

This section guides the user through the EVM test procedure to obtain a valid data capture from the TSW54J60EVM using the TSW14J56EVM capture card. This should be the starting point for all evaluations.

2.1 Software Installation

The proper software must be installed before beginning evaluation. See Section 1.2 for a list of the required software. The References section of this document contains links to find the software on the TI website.

Important: The software must be installed before connecting the TSW54J60EVM and TSW14J56 to the computer for the first time.

2.1.1 ADS54Jxx EVM GUI Installation

The ADS54Jxx EVM GUI is used to control the TSW54J60EVM. It must be used to properly configure the devices on the EVM.

1. Download the ADS54Jxx EVM GUI from the TI website. The References section of this document contains links to find the software on the TI website.
2. Extract the files from the zip file.
3. Run setup.exe and follow the installation prompts.

2.1.2 High Speed Data Converter Pro GUI Installation

High Speed Data Converter Pro (HSDC Pro) is used to control the TSW14J56EVM and analyze the captured data. Please see the HSDC Pro user’s guide (SLWU087) for more information.

1. Download HSDC Pro from the TI website. The References section of this document contains the link to find the software on the TI website.
2. Extract the files from the zip file.
3. Run setup.exe and follow the installation prompts.
2.2 Hardware Setup Procedure

A typical test setup using the TSW54J60EVM and TSW14J56EVM is shown in Figure 2. This is the test setup used for the quick start procedure. The rest of this section describes the hardware setup steps.

2.2.1 TSW14J56EVM Setup

First, setup the TSW14J56EVM using the following steps:

1. Connect the TSW54J60EVM to the TSW14J56EVM using the FMC connectors.
2. Connect the included 5-V power supply to connector J11 (+5V IN).
3. Connect the included USB3.0 cable to the USB connector (J9).
4. Flip the power switch (SW6) to the ON position.

Figure 2. Quick Start Test Setup
2.2.2 TSW54J60EVM Setup

Next, setup the TSW54J60EVM using the following:

1. Connect the included power supply cable into connector J9 of the EVM. Connect the white stripped black wire to +5 VDC ±0.1 VDC of a 5-VDC power supply rated for at least 3 A. Connect the other black wire to GND. Turn on the 5-VDC power supply. The power supply should draw around 0.66 A. When configured, the EVM will draw approximately 1.35 A.

2. Connect the included mini-USB cable to the USB connector J8.

3. Set the analog input signal generator for 70 MHz, and about 6 dBm of power.

4. Place a narrow pass-band band-pass filter at the output of the analog signal generator to remove noise and harmonics from the signal generator.

5. Connect a 6-dB attenuator between the output of the band pass filter and SMA connector INBP (J3) of the TSW54J60EVM to provide a robust 50-Ω source impedance.

2.3 Software Setup Procedure

The software can be opened and configured once the hardware is properly setup.

2.3.1 TSW54J60 GUI Configuration

1. Open the ADS54Jxx EVM GUI by going to Start Menu → All Programs → Texas Instruments ADCs → ADS54Jxx EVM GUI. The GUI now looks as shown in Figure 3.

![Figure 3. ADS54Jxx GUI Low Level View Tab](image)

2. Verify that the green USB Status indicator is lit in the top right corner of the GUI. If it is not lit, click the Reconnect USB button and check the USB Status indicator again. If it is still not lit, then verify the EVM is connected to the computer through the included mini-USB cable.

3. Click on the Low Level View tab then click the Load Config button.
4. Navigate to \Program Files(86)\Texas Instruments\ADS54Jxx EVM GUI\Configuration Files, select the file called LMK_Config_Onboard_983p04_MSPS.cfg, then click OK. This programs the LMK04828 to provide a 983.04-MHz clock to the ADC. This configuration file also generates the required SYSREF clock for both boards and the device clock for the FPGA on the TSW14J56.

5. Verify that the LMK04828 phase lock loop (PLL) is locked by checking that the PLL2 LOCKED LED (D2) is lit.

6. Once the LMK04828 PLL is locked, press SW1 (ADC RESET) to provide a hardware reset to the ADC. This switch is located in the middle of the EVM.

7. In the Low Level View tab, click Load Config. Select the file called ADS54J60_LMF_8224.cfg and click OK. The TSW54J60EVM is now configured for no decimation and 8 JESD204B lanes.

8. Click on the LMH6401 tab. Set the Gain to "A" by entering the value in the box (see Figure 4) and then click outside the box or press enter on the keyboard. This will provide 16 dB of voltage gain from the LMH6401.

![Figure 4. LMH6401 Gain Setting Control](image-url)
2.3.2 HSDC Pro GUI Configuration

1. Open High Speed Data Converter Pro by going to Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro. The GUI main page looks as shown in Figure 5.

2. When prompted to select the capture board, select the TSW14J56 whose serial number corresponds to the serial number on the TSW14J56EVM and click OK. This popup can be accessed through the Instrument Options menu.

3. If no firmware is currently loaded, there is a message indicating this. Click on OK.

4. Verify the ADC tab at the top of the GUI is selected.

5. Use the Device drop-down menu at the top left corner to select ADS54J60_LMF_8224.

6. When prompted to update the firmware for the ADC, click Yes and wait for the firmware to download to the TSW14J56. This takes about 3 seconds.

7. Enter “983.04M” into the ADC Output Data Rate field at the bottom left corner then click outside this box or press return on the PC keyboard.

8. The GUI displays the new lane rate of the SerDes interface based off of the sample rate and other parameters from the loaded configuration files. Click OK.

9. Click the Instrument Options menu at the top of HSDC Pro and select Reset Board.

10. Change the channel panel to Channel 2/2 to view the data from the LMH6401 path.

11. Click Capture in HSDC Pro to capture data from the ADC.

12. The results from the captured data of Channel 2 (LMH6401) should look like Figure 6 and the performance should be similar to Table 1. If this result is not achieved, then see the Quick Start Troubleshooting section of this document. Make sure the fundamental power is less than –1 dBFs. Adjust the gain setting of the LMH6401 or the amplitude of the signal from the source, if needed.
13. Move the signal source to SMA J1. This will allow the user to capture data from the LMH3401 path. Change the channel panel to Channel 1/1.
Table 1. Quick Start Example Typical Performance Measurements

<table>
<thead>
<tr>
<th>Result</th>
<th>Measured Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6401 Path</td>
<td>63</td>
<td>dBFS</td>
</tr>
<tr>
<td>SNR</td>
<td>74</td>
<td>dBFS</td>
</tr>
<tr>
<td>SFDR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LMH3401 Path</td>
<td>65</td>
<td>dBFS</td>
</tr>
<tr>
<td>SNR</td>
<td>76</td>
<td>dBFS</td>
</tr>
<tr>
<td>SFDR</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

14. Click on Capture. The results from the captured data of Channel 1 (LMH3401) should look like Figure 7 and the performance should be similar to Table 1. If this result is not achieved, then see the Quick Start Troubleshooting section of this document. Make sure the fundamental power is less than –1 dBFS. Adjust the amplitude of the signal from the source, if needed.
2.4 Quick Start Trouble Shooting

Use Table 2 to assist with problems that may have occurred during the quick start procedure.

Table 2. Troubleshooting Tips

<table>
<thead>
<tr>
<th>Issue</th>
<th>Troubleshooting Tips</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>General Problems</strong></td>
<td>Verify the test setup shown in Figure 2 and repeat the setup procedure as described in this document.</td>
</tr>
<tr>
<td></td>
<td>Check power supplies to the EVMs. Verify that the power switches are in the ON position.</td>
</tr>
<tr>
<td></td>
<td>Check signal and clock connections to the EVM.</td>
</tr>
<tr>
<td></td>
<td>Check that all boards are properly connected together.</td>
</tr>
<tr>
<td></td>
<td>Try pressing the CPU_RESET button on the TSW14J56EVM.</td>
</tr>
<tr>
<td></td>
<td>Try power-cycling the external power supply to the EVM and reprogram the LMK and ADC devices.</td>
</tr>
<tr>
<td><strong>TSW14J56 LEDs are not correct:</strong></td>
<td></td>
</tr>
<tr>
<td>D1, D5 – N/A</td>
<td>Verify the settings of the configuration switches on the TSW14J56EVM.</td>
</tr>
<tr>
<td>D2, D4 – Blinking</td>
<td>Verify that the EVM configuration GUI is communicating with the USB and that the configuration procedure has been followed.</td>
</tr>
<tr>
<td>D3, D6, D7 – OFF</td>
<td>(LEDs Not Blinking) Reprogram the LMK device.</td>
</tr>
<tr>
<td>D8, D28 – ON</td>
<td>Try pressing the CPU_RESET button on the TSW14J56EVM.</td>
</tr>
<tr>
<td></td>
<td>Try capturing data in HSDC Pro to force an LED status update.</td>
</tr>
<tr>
<td><strong>Device GUI is not working properly</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Verify that the USB cable is plugged into the EVM and the PC.</td>
</tr>
<tr>
<td></td>
<td>Check the computer’s Device Manager and verify that a USB Serial Device is recognized when the EVM is connected to the PC.</td>
</tr>
<tr>
<td></td>
<td>Try restarting the configuration GUI.</td>
</tr>
<tr>
<td></td>
<td>Check default jumper connections as shown in Appendix A.</td>
</tr>
<tr>
<td><strong>HSDC Pro Software is not capturing good data or analysis results are incorrect</strong></td>
<td>Verify that the TSW14J56EVM is properly connected to the PC with an USB cable and that the board serial number is properly identified by the HSDC Pro software.</td>
</tr>
<tr>
<td></td>
<td>Check that the proper ADC device is selected. In default conditions, ADS54J60_LMF_8224 should be selected.</td>
</tr>
<tr>
<td></td>
<td>Check that the analysis parameters are properly configured.</td>
</tr>
<tr>
<td></td>
<td>Check that the fundamental power is no larger than –1 dBFs.</td>
</tr>
<tr>
<td><strong>HSDC Pro Software gives a Time-Out error when capturing data</strong></td>
<td>Try to reprogram the LMK device and reset the JESD204 link.</td>
</tr>
<tr>
<td></td>
<td>Verify that the ADC sampling rate is correct in the HSDC Pro software.</td>
</tr>
<tr>
<td><strong>Sub-Optimal Measured Performance</strong></td>
<td>Make sure an ADC hardware reset was issued after loading the LMK but before loading the ADC configuration file.</td>
</tr>
<tr>
<td></td>
<td>Check that the spectral analysis parameters are properly configured.</td>
</tr>
<tr>
<td></td>
<td>Verify that bandpass filters and 6-dB attenuator are used in the input signal paths and that low-noise signal sources are used. It is recommended to include the attenuator between the filter and SMA connector to provide a wide-band 50-Ω source impedance connection.</td>
</tr>
<tr>
<td></td>
<td>Verify that a bandpass filter is used in the clock path and that low-noise signal source is used when operating in external clock mode.</td>
</tr>
</tbody>
</table>
3 Optimizing Evaluation Results

This section assists the user in optimizing the performance during evaluation of the product.

3.1 Clocking Optimization

The sampling clock provided to the ADC needs to have very low phase noise to achieve optimal results. The default EVM configuration uses the LMK04828 clocking device to generate the sampling clock. There are two options to improve the clock noise performance:

1. To achieve the best performance, the LMK04828 can be bypassed in favor of an externally provided clock that is transformer-coupled to the ADC. The clock must have very low noise and must use an external narrow pass-band filter to achieve optimal noise performance. The clock amplitude must be within the datasheet limits. See Section 5 for more information regarding this setup.

2. The LMK04828 can be used as a clock distributor by using an external clock as the input to the LMK04828. Filters should still be used on the clock to optimize the noise performance. See Section 5.2 for more information regarding this setup.

3.2 Coherent Input Source

A Rectangular window function can be applied to the captured data when the sample rate and the input frequency are set precisely to capture an integer number of cycles of the input frequency (sometimes called coherent frequency). This may yield better SNR results. The clock and analog inputs must be frequency locked (such as through 10-MHz references) in order to achieve coherency.

3.3 HSDC Pro Settings

HSDC Pro has some settings that can help improve the performance measurements. These are highlighted in Table 3.

<table>
<thead>
<tr>
<th>HSDC Pro Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analysis Window (samples)</td>
<td>Selects the number of samples to include in the selected test analysis. Collect more data to improve frequency resolution of Fast-Fourier Transform (FFT) analysis. If more than 65,536 samples are required, the setting in the Data Capture Options needs to be increased to match this value.</td>
</tr>
<tr>
<td>Data Windowing Function</td>
<td>Select the desired windowing function applied to the data for FFT analysis. Select Blackman when sampling a non-coherent input signal or Rectangle when sampling a coherent input signal.</td>
</tr>
<tr>
<td>Test Options → Notch Frequency Bins</td>
<td>Select bins to be removed from the spectrum and back-filled with the average noise level. May also customize which Harmonics/Spurs are considered in SNR and THD calculations and select the method for calculating spur power.</td>
</tr>
<tr>
<td>Test Options → Bandwidth Integration Markers</td>
<td>Enable markers to narrow the Single-Tone FFT test analysis to a specific bandwidth.</td>
</tr>
<tr>
<td>Data Capture Options → Capture Options</td>
<td>Configure the number of contiguous samples per capture (capture depth). May also enable Continuous Capture and FFT Averaging.</td>
</tr>
</tbody>
</table>
4 Software Description

4.1 TSW54J60 EVM GUI

Figure 8 shows the front page of the ADS54Jxx EVM GUI as it should be seen upon opening the GUI. Descriptions for each of the tabs of the GUI are shown in Table 4.

Table 4. TSW54J60 GUI Tab Descriptions

<table>
<thead>
<tr>
<th>Tab</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS54Jxx</td>
<td>Enables control of the ADS54J60 features. None of these controls need to be touched for basic operation. Instead, use the Low Level View tab to load configuration files.</td>
</tr>
<tr>
<td>LMK04828</td>
<td>Enables control of many of the LMK04828 features. Configuration files can be used to setup the LMK04828 in known working configurations, however, this tab can be used to setup more advanced clocking schemes.</td>
</tr>
<tr>
<td>LMH6401</td>
<td>Allows writes to the gain setting register of the LMH6401.</td>
</tr>
<tr>
<td>Low Level View</td>
<td>Allows write and read access to all device registers. Also allows loading and saving of configuration files. The device configurations can be saved from this tab for use in the user’s system. See Section 4.2 for more information.</td>
</tr>
</tbody>
</table>
4.2 Low Level View

The Low Level View tab, shown in Figure 9, allows configuration of the devices at the bit and field level. At any time, the controls described in Table 5 may be used to configure or read from the device.

![Figure 9. Low Level View Tab](image)

Table 5. Low Level View Controls

<table>
<thead>
<tr>
<th>Control</th>
<th>Description</th>
</tr>
</thead>
</table>
| Register Map             | Displays the devices on the EVM, registers for those devices, and the states of the registers.  
|                          |   • Selecting a register field allows bit manipulation in the Register Data section.  
|                          |   • The Value column shows the value of the register at the time the GUI was last updated due to a read or write event. |
| Write Register button    | Write to the register highlighted in the Register Map with the value in the Write Data field. This button must be clicked after changing bits in the register data section. |
| Write All button         | Update all registers shown in the Register Map with the values shown in the Register Map log.  
|                          | The log can be viewed by double left clicking in the bottom left status bar of this page. |
| Read Register button     | Read from the register highlighted in the Register Map and display the results in the Value column. |
| Read All button          | Read from all registers in the Register Map and display the current state of hardware. Also updates the controls in the other tabs. |
| Load Config button       | Load a configuration file from disk and write the registers in the file. |
| Save Config button       | Save a configuration file to disk that contains the current register configuration. |
| Register Data Cluster    | Manipulate individual accessible bits of the register highlighted in the Register Map. |
| Generic Read/Write Register buttons | Perform a generic read or write command to the device shown in the Block drop-down box using the Address and Write Data information |
5 Alternate Hardware Configurations

This section describes alternate hardware configurations in order to achieve better results or to more closely mimic the system configuration.

5.1 Clocking Options

The default clocking mode uses the LMK04828 to generate the ADC sampling clock and FPGA clocks. There are three additional clocking options that the EVM supports. These options are described in the following sections.

5.1.1 External ADC Sampling Clock

An external clock can be used as the sampling clock for the ADC. This clock can be provided through a transformer using the EXT_ADC_CLK connector (J5). For this option, C65 and C73 need to be uninstalled and installed at C64 and C72. The LMK04828 must still be used to provide the device clock to the TSW14J56 and the SYSREF signals to both boards. This option provides the best performance, as long as the clock source has better phase-noise performance than the LMK04828. The source of the EXT ADC clock must be synchronized with the LMK04828. To accomplish this, send the 10-MHz reference output from the signal generator and connect it to J6 (LMK_CLKIN1) of the TSW54J60EVM. This causes LED D1 to illuminate indicating the LMK VCXO source is locked to the external reference clock. The default LMK configuration file mentioned in Section 2.3.1 will work in this mode as well. To turn off the ADC clock provided by the LMK04828 to reduce switching noise, click on the LMK04828 tab, then click on Clock Outputs tab, then select Powerdown for DCLK Type under CLKout 2 and 3 as shown in Figure 10.

![Figure 10. LMK04828 Clock Outputs Tab](image)

5.1.2 External LMK04828 Clock (Clock Distribution Mode)

The LMK04828 can be used as a clock distributor. In this case, the LMK04828 uses an input clock source from LMK_CLKIN1 SMA connector (J6). SJP2 (XO_PWR) can be left open to turn off the onboard VCXO to minimize clock switching noise. To use this mode, load the configuration file named LMK_Config_External_Clock.cfg. This mode allows generation of frequencies that are not possible with the LMK when using the on-board VCXO.
5.1.3 Clock Generator Using Onboard VCXO

The LMK04828 is used as a clock generator using the onboard 122.88-MHz VCXO. SJP2 must be shorted to turn on the onboard VCXO. The internal PLLs of the LMK04828 can be used with the onboard VCXO to generate the desired frequencies. To use this mode, load one of the configuration files named `LMK_Config_Onboard_xxxx_MSPS.cfg`, where `xxxx` corresponds to the desired ADC sampling rate. A 10-MHz signal can be brought into the LMK_CLKIN1 input to synchronize to external instruments. This is the board default mode of operation.

5.2 Analog Input Options

The TSW54J60EVM allows for differential analog input configurations for both paths as well as DC coupling. These options are described in the following sections.

5.2.1 LMH6401 Differential Input

The analog input transformer on the LMH6401 path can be bypassed in favor of a differential input source. This allows for a wider range of input frequencies, including the possibility of DC coupling. To configure the LMH6401 path on the EVM for a 100-Ω differential analog input, remove R119 and T1, and install 0-Ω resistors for R120, R121, R122, and R123. When driving the LMH6401 with a differential DC coupled input, it is required to DC bias the differential signal within the input common-mode (CM) specifications of the device. For optimal performance, it is recommended to bias the input close to the LMH6401 mid-supplies (2.5 V) on this EVM. Using 6-dB attenuator pads on the differential SMA inputs is recommended for wide-band interface to external filters and SMA cables.

5.2.2 LMH3401 Differential Input

To configure the LMH3401 path for 100-Ω differential input, remove R12 and replace R64 and R67 with 37.5-Ω resistors. This configures the LMH3401 path for differential voltage gain of 12 dB.

5.2.3 DC Coupling

For a DC coupled application on either path, swap the series capacitors before the amplifier with 0-Ω resistors. The input signal must be biased to the required amplifier input common mode voltage. For the LMH3401, remove termination resistor R12. It is required to maintain the undriven input of the LMH3401 to the same DC voltage as the signal source input bias voltage in order to eliminate any output CM offset errors.

5.2.4 LMH5401

The LMH3401 can be replaced with a LMH5401 device. To use this EVM with a LMH5401 in a single-ended input mode, replace the LMH3401 with the pin-for-pin compatible LMH5401, replace R64 and R67 with 0.01-µF capacitors (for AC coupling only), install 365-Ω resistors for R11 and R12, install 127-Ω resistors for R3 and R10, replace C204 and C205 with 22.6-Ω resistors and use a 50-Ω termination plug on J2.

To use the LMH5401 in a fully differential mode, configure per the LMH3401 in differential mode and install 174-Ω resistors for R3 and R10, install 49.9-Ω resistors at R64 and R67 to provide a differential voltage gain of 12 dB. For AC coupling, use the default values for C204 and C205. For a DC-coupled application, replace these with 0-Ω resistors. See the LMH5401 datasheet (SBOS710B) for more information regarding the use of this device.
Appendix A

Jumper, Connector, and LED Descriptions

A.1 Jumper Descriptions

The EVM jumpers are shown in Table 6 as well as the default settings for the jumpers. Use this table to reset the EVM in the default configuration, in case of issues.

Table 6. Jumper Descriptions and Default Settings

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Description</th>
<th>Default setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1</td>
<td>ADC hardware reset (active high)</td>
<td>Logic low</td>
</tr>
<tr>
<td>SJP1</td>
<td>Selects either 3.3 V or GND for Y1 enable. Default is open</td>
<td>Open</td>
</tr>
<tr>
<td>SJP2</td>
<td>Power enable to VCXO oscillator Y1. Default is power on.</td>
<td>Shunt pins 1-2</td>
</tr>
<tr>
<td>SJP3</td>
<td>Selects either diff sync or single-ended sync from FMC. Default is diff.</td>
<td>Shunt pins 2-3</td>
</tr>
</tbody>
</table>

A.2 Connector Descriptions

The EVM connectors and their function are described in Table 7.

Table 7. Connector Descriptions

<table>
<thead>
<tr>
<th>Connector</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>LMH3401 positive analog input. Used for differential input mode only.</td>
</tr>
<tr>
<td>J1</td>
<td>LMH3401 negative analog input</td>
</tr>
<tr>
<td>J3</td>
<td>LMH6401 positive analog input</td>
</tr>
<tr>
<td>J4</td>
<td>LMH6401 negative analog input. Used for differential input mode only.</td>
</tr>
<tr>
<td>J5</td>
<td>External ADC sample clock input</td>
</tr>
<tr>
<td>J6</td>
<td>LMK04828 reference clock input</td>
</tr>
<tr>
<td>J7</td>
<td>JESD204B FMC connector. Interfaces to TSW14J56EVM or FPGA evaluation boards.</td>
</tr>
<tr>
<td>J8</td>
<td>USB interface connector</td>
</tr>
<tr>
<td>J9</td>
<td>5-V power supply input</td>
</tr>
</tbody>
</table>
A.3 LED Descriptions

The EVM LEDs are described Table 8.

Table 8. LED Descriptions

<table>
<thead>
<tr>
<th>LED</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D3</td>
<td>Not used</td>
</tr>
<tr>
<td>D4</td>
<td>5 VDC power present</td>
</tr>
<tr>
<td>D2</td>
<td>LMK04828 locked to VCXO</td>
</tr>
<tr>
<td>D1</td>
<td>VCXO locked to external reference applied to J6</td>
</tr>
</tbody>
</table>

Revision History

Changes from Original (September 2015) to A Revision

- Changed input power supply in included hardware list in the Required Hardware section. ........................................... 2
- Added 5-VDC, 3-A power supply to list of equipment not included. ................................................................. 2
- Changed Quick Start Test Setup image. ............................................................................................................. 5
- Changed step 1 in TSW54J60EVM Setup section. ......................................................................................... 6

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
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3.1.2 **For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:**

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.
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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### 3.2 Canada

**3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210**

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan.
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.
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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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Products

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