TVP7000EVM User's Guide

Digital Video Department

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1 Functional Description

The TVP7000EVM refers to the TVP7000 board and the THS8200 board when they are connected together. Both boards share a common interface via a 120-pin connector. This interface provides all data, clocks, I^2C communication, and 5-V power to each board.

The THS8200 is a Texas Instruments Triple DAC providing component analog RGB or YPbPr outputs. As such, the THS8200 supports resolutions up to SXGA for PC graphics and up to 1080p for video. This triple DAC minimizes artifacts commonly associated with backend processing. Its purpose is only to convert the digital data from the TVP7000 Triple ADC back to analog. Use of a quality TV or display capable of supporting both component RGB and YPbPr analog inputs is recommended.

1.1 Description Overview

The TVP7000EVM is powered by a single, 5-V, universal supply. I^2C communication is emulated using a PC parallel port configured for the extended capability port (ECP) or bidirectional mode. The parallel port mode can be changed using the PC BIOS setup, available during the reboot process.

The TVP7000 Triple ADC converts three channels of analog video input into digital component data. This digital data and the associated clocks from the TVP7000 are sent to the THS8200.

Control of the TVP7000EVM is provided by WinVCC, a Windows-based application developed by Texas Instruments and provided free of charge. This application uses the parallel port to provide I^2C communication to the TVP7000EVM. WinVCC provides a graphics user interface (GUI) and a register level interface to program and vary the controls available within the TVP7000 Triple ADC and the THS8200.

2 Board Level Description

The following subsections describe the various features available on the TVP7000EVM. Figure 1 shows the block diagram for the TVP7000EVM.

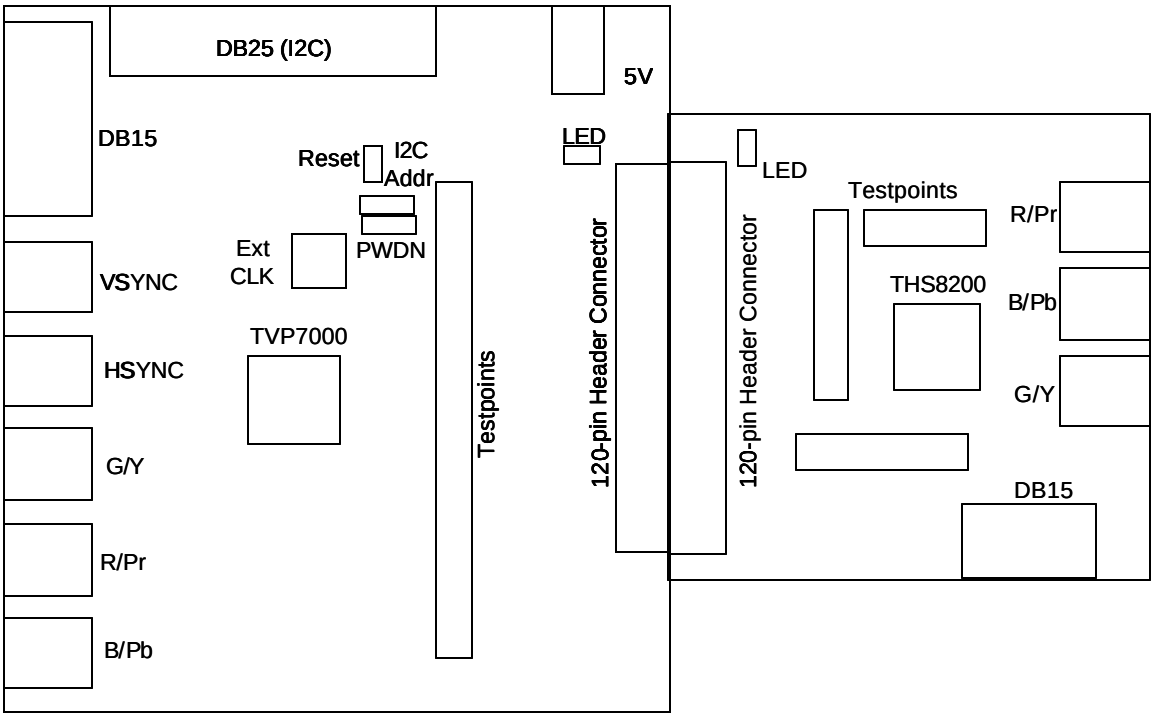


Figure 1. TVP7000EVM Block Diagram

2.1 Analog Inputs

The TVP7000EVM makes use of all the available inputs on the TVP7000 Triple ADC. The following inputs are available for use:

- Five BNC connectors (Y/G, Pb/B, Pr/R, HSYNC, and VSYNC)
- One DB15 graphics connector (Y/G, Pb/B, Pr/R, HSYNC, and VSYNC)

Table 1 shows the pins used for the inputs described above.

Table 1. Analog Inputs and Pin Terminals

Input Type	TVP7000 Pin(s)
5 BNC	RIN_1, GIN_1, BIN_1, VSYNC_B, HSYNC_B
DB15	RIN_3, GIN_3, BIN_3, VSYNC_A, HSYNC_A

2.2 External Clock Input

An SMA connector (EXT CLK) is provided on the TVP7000EVM for use with an external ADC sample clock. This input is end-terminated with a 50-? resistor for use with a lab clock generator and is routed to pin 80 (EXT CLK) of the TVP7000.

An external sample clock can be used by placing the TVP7000 in the PLL free-run mode (I^2C register 0Fh[0] = 1). The free-run mode decouples the internal PLL clock from the ADCs and establishes a direct connection from EXT CLK pin to the ADC sample clock. Removal of the termination resistor may be required for some clock sources incapable of driving the 50-? load. The EXT CLK input can be left unconnected for applications using the internal PLL clock.

2.3 Test Points and Jumpers

Various test points are available on the TVP7000EVM. This includes COAST, CLAMP, TEST, SOG_OUT, SDA, SCL, power, and GND. Each test point is clearly labeled on the TVP7000EVM silkscreen. The primary test point headers for the TVP7000 are H2, H3, and H4 which provide access to the RED, GREEN, and BLUE data, respectively.

There are two jumpers on the TVP7000 board that configure the power-down mode and I^2C address select. Each jumper is set by default in its preferred state for the TVP7000EVM. Around each jumper on the TVP7000 board is a silkscreen that describes the two states of the jumper configuration.

Table 2. TVP7000 I^2C Address Selection Jumper (I2C ADDR)

I2C ADDR	
1 - 2	0xB8 (default)
2 - 3	0xBA

Table 3. Power-Down Mode Selection Jumper (PWDN)

PWDN	
1 - 2	Normal Operation (default)
2 - 3	Power Down

NOTE: If the I^2C address is changed on either the TVP7000 board or the THS8200 board while the TVP7000EVM is powered up, then that device will not recognize the new I^2C address. The reset button on the TVP7000EVM must be pressed and WinVCC must be reconfigured for the new I^2C address.

2.4 Common Board Interface

The TVP7000EVM uses a 120-pin connector to connect the TVP7000 board (P3) to the THS8200 board (P2). This interface shares all common signals including the I^2C and the 5-V supply. This modularizes the TVP7000 board and allows users to interface it to a variety of other Texas Instruments products including DVI transmitters, video encoders, or to any other platform that shares the same interface.

This connector shares all digital video data (R[9:0], G[9:0], and B[9:0]), all video clocks (DCLK_OUT, VSYNC, and HSYNC), RESET, I^2C, and 5 V as mentioned above.

2.5 Component Analog Outputs

The THS8200 board provides component RGB or YPbPr analog outputs to a display monitor. The configuration settings for the TVP7000EVM use the RGB color space for PC graphics and the YPbPr color space for video (480i – 1080p).

3 System Level Description

The system block diagram illustrated in Figure 2 provides an example of how the TVP7000EVM may be used for evaluation. Typically, an RGB or YPbPr component analog input is provided by a graphics/video source such as a pattern generator or a DVD player.

The TVP7000EVM is configured with the provided 5-V supply and the parallel port cable. The output is provided by the THS8200 triple DAC to convert the digital data from the TVP7000 back to analog. This analog output is then fed into a quality display monitor.

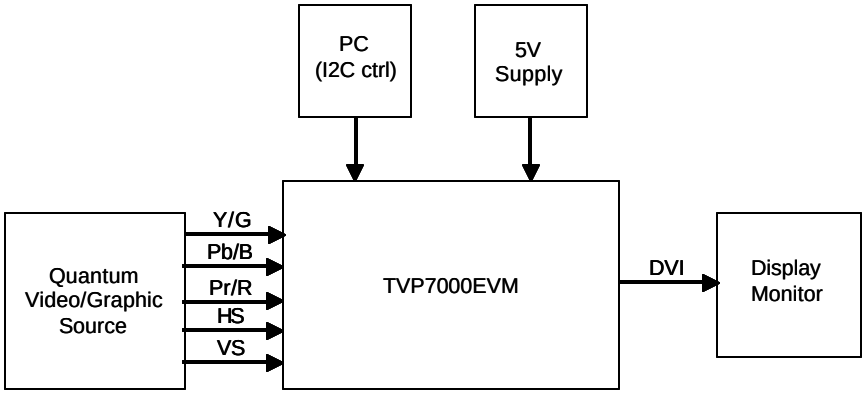


Figure 2. TVP7000EVM System Level Block Diagram

4 Required Hardware and Equipment

The required hardware and equipment necessary to use the TVP7000EVM are:

- TVP7000EVM (provided)
- Universal 5-V power supply (provided)
- Parallel cable (provided)
- Windows-based PC
- One cable with five BNC connectors (RGB, HS, VS)
- One cable with three BNC connectors (RGB or YPbPr)
- Two DB15 PC cables
- Video source (pattern generator, Quantum generator, or DVD player)
- Display monitor that supports PC graphics and video up to 1080p

5 Hardware Setup

Perform the following steps to set up the hardware for the TVP7000EVM:

1. Connect the TVP7000 board and the THS8200 board using the 120-pin board connector. This becomes the TVP7000EVM.
2. Connect a video or graphics source to the DB15 input connector and the RGB, HSYNC, and VSYNC input connectors of the TVP7000 EVM.
3. Connect a DB15 cable and three BNC cables to the THS8200 board.
4. Connect the parallel port cable from the TVP7000EVM to the PC.

   NOTE: There are footprints for a dc jack on the THS8200 board, but the default power is provided by the TVP7000 board via the 120-pin connector, P3.
5. Connect the 5-V power supply to the dc jack on the TVP7000 board. A green LED on each board should now be lit.

6 Software Installation

WinVCC is a Windows application that uses the PC parallel port to emulate I^2C, providing access to each device on the I^2C bus. WinVCC makes use of CMD files, a text editable file that allows preset video setups to be programmed easily.

This feature allows the user to easily set multiple I^2C registers with the press of a button. WinVCC also has property sheets for the TVP7000 which allow the user to control the I^2C registers with a GUI.

All necessary software for the TVP7000EVM is provided on the enclosed CD. Perform the following steps to install WinVCC:

1. Explore the provided TVP7000EVM Software CD.
2. Install Port95NT.exe. This is the parallel port driver used by WinVCC. This driver must be installed and the PC must be rebooted before WinVCC will operate correctly.
3. Install Setup.exe. Click *Next* at all prompts and click *Finish* to complete the installation process. This will install WinVCC onto the PC. No reboot is required.
4. Run WinVCC.exe

NOTE: A shortcut to WinVCC should now be available on the desktop. WinVCC and additional TVP7000 related documentation can also be found at *Start->Programs-> TVP7000EVM Software* to start WinVCC and to browse the documentation.

7 WinVCC Quick Start

Perform the following steps in order to get video out of the TVP7000EVM.

1. Once WinVCC is executed, the WinVCC Configuration screen appears. This dialog box configures the I^2C bus. Next to TVP7000, select the TVP7000 and ensure the I^2C address is set to 0xB8. This must match the I2C ADDR jumper on the TVP7000 board.

2. Next to THS8200, select the THS8200 and ensure the I^2C address is set to 0x40. This must match the I2C ADDR jumper on the THS8200 board.

   NOTE: If WinVCC is running and the TVP7000 or THS8200 board I^2C address is changed, then power must be cycled on the EVM.

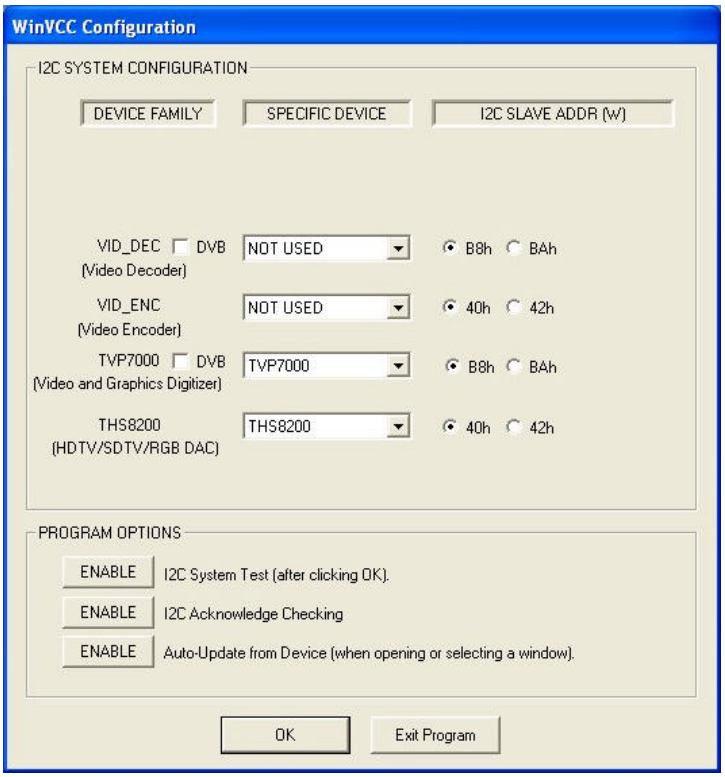


Figure 3. WinVCC – I^2C Configuration Screen

3. Ensure that all other boxes are selected as "Not Used" and that all program options buttons are set to ENABLE. Click OK.

4. If there are no I^2C communication issues, then the Main Screen window displays next. If there are I^2C issues, then an I2C Test Report box displays. Completely exit out of WinVCC, double-check the parallel port cable connections, cycle power on the TVP7000EVM, and re-run WinVCC.

5. Load the provided Initialize.CMD file into WinVCC by clicking on Tools -> System Initialization -> Browse. The default directory is c:\Program Files\Texas Instruments\TVP7000EVM\Initialization.

Figure 4. WinVCC – Main Screen

6. Click the "TVP7000 + THS8200_..." dataset in the window and then click the Program Dataset button to initialize the TVP7000EVM.

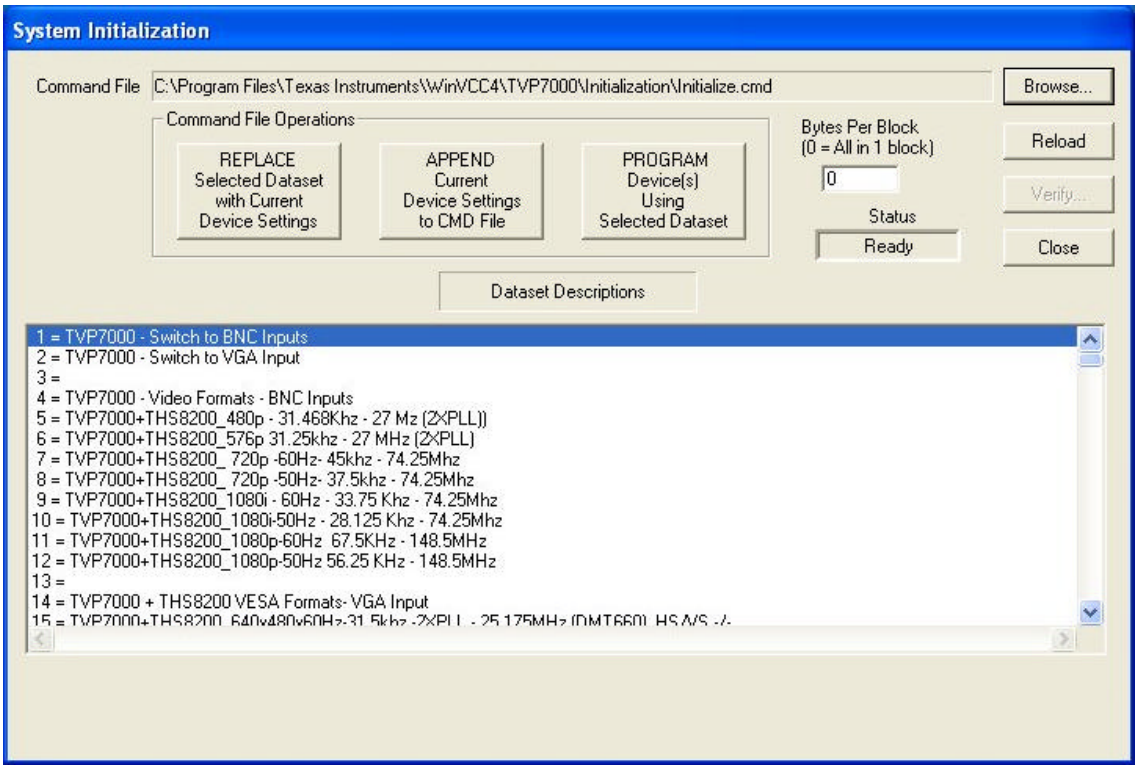


Figure 5. WinVCC – System Initialization

7. With a graphics/video source provided at the BNC or DB15 connectors and with the proper resolution configured, video should be viewable on the display monitor.

   NOTE: To ensure the TVP7000 is working properly, go to Status and check the HSYNC and VSYNC detection status. If using YPbPr inputs, then the SOG status detection will also be beneficial.

8 WinVCC in Depth

The following sections describe how to use WinVCC in depth. It discusses various features and screens which the user may encounter while evaluating the TVP7000EVM.

8.1 Starting WinVCC

The Port95NT parallel port driver must be installed before using WinVCC. WinVCC may be started by clicking on *Start->All Programs->TVP7000EVM Software->WinVCC.*

If the dialog box shown in Figure 6 is displayed, then it means one of two things:

1. WinVCC did not run to completion the last time it ran. In this case, click *OK* to exit the program and restart WinVCC.
2. There is more than one instance of WinVCC running at the same time. In this case, click *OK* to exit the program. Then, press CTRL-ALT-DELETE to bring up the *Task Manager*. Select and click *End Task* on all occurrences of WinVCC or WinVCC CONFIGURATION. Then restart WinVCC.

Figure 6. WinVCC Multiple Occurrences Error Message

8.2 WinVCC Configuration Dialog Box

The *WinVCC Configuration* dialog box, as seen in Figure 7, should now be visible. This dialog box configures the I^2C bus on the TVP7000EVM. All settings from this dialog box are stored in the Windows registry and are restored the next time the program is started. After initial installation, the TVP7000 Video and Graphics Digitizer drop down box will be set to TVP7000.

The I^2C slave address for each device must match the I^2C slave address selected by jumpers on the TVP7000EVM. These jumpers are set by the factory to use 0xB8 for the TVP7000 and 0x40 for the THS8200 triple DAC.

It is also important to ensure only the TVP7000 is selected when using the TVP7000EVM. All Program Options must be enabled. Disabling these options is only required if you are debugging a problem with the I^2C bus.

Clicking *OK* begins I^2C communication with the selected devices.

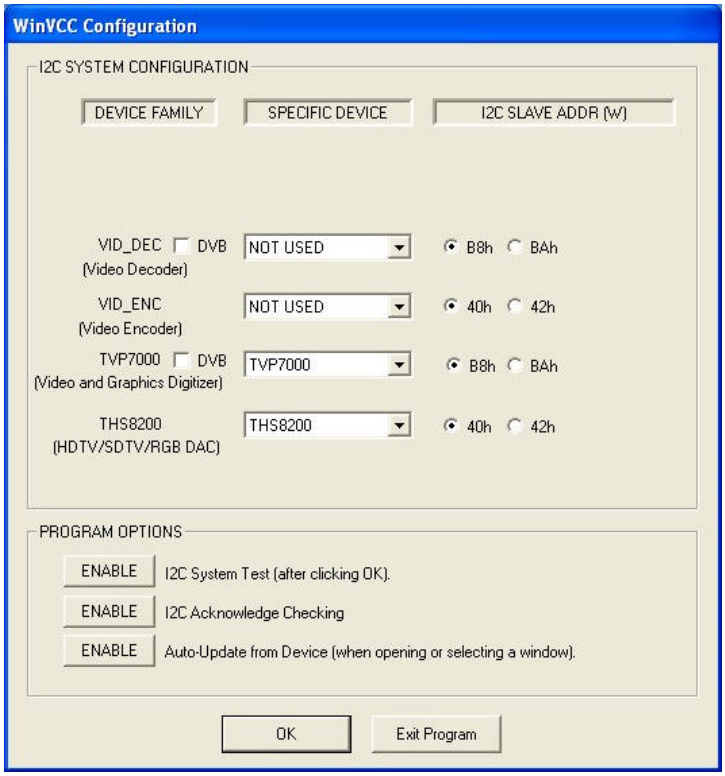


Figure 7. WinVCC I^2C Address Configuration

8.3 I^2C System Test

The I^2C system test of selected registers runs immediately after closing the *WinVCC Configuration* dialog box with *OK* (unless the I^2C system test program options button was disabled).

If the I^{2}C system test passes, then only a PASS message will appear. If the test failed, then a dialog box like Figure 8 appears. See Section 9, *Troubleshooting*, for details on how to resolve this issue.

The I^{2}C system test can be run at anytime by clicking *Run System I2C Test* in the *Tools* menu.

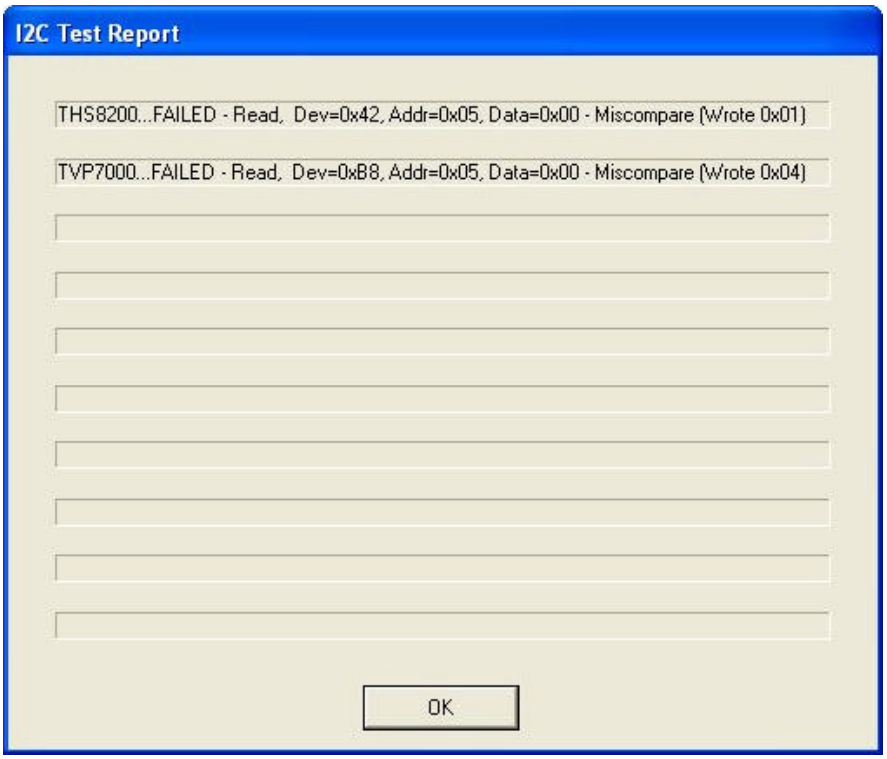


Figure 8. I^{2}C System Failure

8.4 Main Menu

After configuring the I^2C, the main menu is displayed as shown in Figure 9. The menus, which are used to operate WinVCC, are *File*, *Edit*, *Tools*, *Window*, and *Help*. The *File* menu's only function is *Exit*, which terminates the program. Table 4 summarizes the main menu contents.

Figure 9. WinVCC – Main Screen

Table 4. Main Menu Summary

Menu	Contents
File	Exit
Edit	Register Map TVP7000PNP Generic I^2C Editor Property Sheets TVP7000PNP
Tools	System Initialization Real-time Polling TV Tuner Control (FQ12xx series only) Multiple-Byte I^2C Transfers Set I^2C Bit Rate Run System I^2C Test Run Continuous I^2C Test Read VBI FIFO Capture Live VBI Data
Window	Allows selection of the active window. Multiple windows can be open at the same time.
Help	Displays program version

8.4.1 System Initialization

Clicking *System Initialization* in the *Tools* menu displays the dialog box shown in Figure 10. This dialog box provides the means for initializing the TVP7000 Triple ADC and/or THS8200 for a particular video mode. The details of the initialization are contained in the command file (with a CMD file extension).

The command file is loaded using the *Browse…* button. Once the command file is opened, a text list displays descriptions of the individual data sets contained within the command file.

Click once on the desired data set description to select it. Click the *Program Device(s) Using Selected Dataset* button to run the selected data set, which loads the devices via the I^2C bus. When the device initialization has completed, the status indicator reads *Ready*.

NOTE: If *Ready* does not display, then the devices are not initialized and the I^2C bus is not communicating. See Section 9, *Troubleshooting*, for possible solutions.

Click the *OK* button to close the dialog box. Each time the *System Initialization* dialog box is closed, the initialization file pathname and the data set selection number are saved in the Windows™ registry to allow these settings to be retained for the next time *WinVCC* runs.

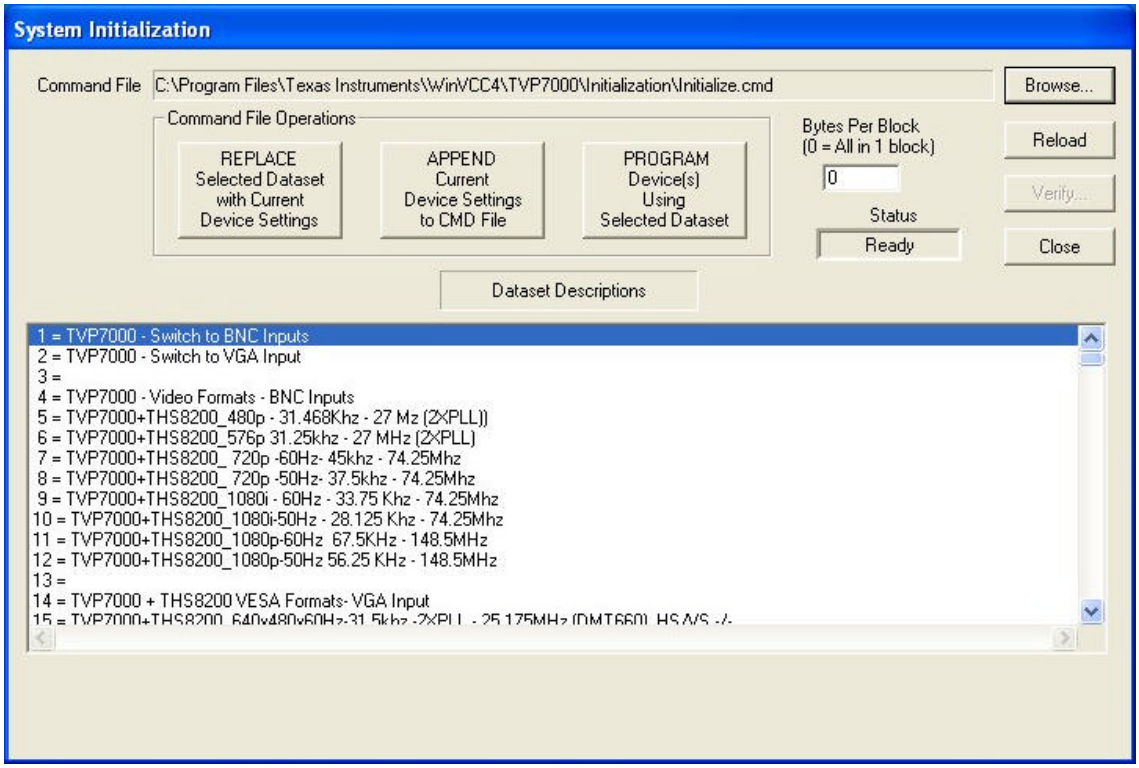


Figure 10. System Initialization

8.4.1.1 Adding a Custom Data Set

After programming the EVM via the *System Initialization* tool using the factory-supplied command file through the *Property Sheets* tool, you can customize the device register settings to suit your needs. Perform the following steps to save your custom settings:

1. Reopen the *System Initialization* dialog box via the *Tools* menu.
2. Click the *Append Current Device Settings to Command File* button. A dialog box requesting a description of the new data set appears.
3. Optionally, click the drop-down box and select one of the existing descriptions.
4. Modify the description text or type your own description.
5. Click *OK*. All nondefault register values from the TVP7000 and THS8200 are appended to the current command file as an additional data set.

Now, you can select your custom data set and send it with a press of the *Program*… button.

NOTE: The command file (.CMD) must be saved as plain text.

8.4.1.2 Command Files

The command file is a text file that can be generated using any common editor; however, it must be saved as plain text. Command files are especially useful for quickly switching between the various system configurations. These .CMD files are unrelated to the typical Windows .CMD files.

A default command file has been provided on the CD. This command file contains most of the desired setups. This command file is located at:

c:\Program Files\Texas Instruments\WinVCC\TVP7000\Initialization Files\Initialize.cmd

A command file can contain up to 250 data sets. A data set is a set of register settings to initialize the TVP7000 Triple ADC and/or THS8200 for a particular video mode. Each data set includes a description that is displayed in one row of the dataset descriptions list. The register settings may be located in the command file itself and/or may be stored in separate include file(s) (with an .INC file extension) and be included into the command file using the INCLUDE statement.

8.4.1.3 Example Command File

An example of one data set within a command file is shown below.

```
BEGIN_DATASET

DATASET_NAME,"TVP7000+THS8200_640x480x75Hz- 37.5khz -2XPLL - 31.5MHz (DM675)  HS/VSin"

// TVP7000 I2C register settings
WR_REG,TVP7000,0x01,0x01,0x69 // PLL DIVMSB     1680 - 2x
WR_REG,TVP7000,0x01,0x02,0x00 // PLL DIVLSB
WR_REG,TVP7000,0x01,0x03,0x58 // PLL CONTROL
WR_REG,TVP7000,0x01,0x04,0xb9 // PHASE SEL(5) CKDI CKDI DIV2
WR_REG,TVP7000,0x01,0x05,0x06 // CLAMP START
WR_REG,TVP7000,0x01,0x06,0x10 // CLAMP WIDTH
WR_REG,TVP7000,0x01,0x0F,0x0E // PLL and CLAMP CONTROL bit0 (0=  HSPO by chip)
WR_REG,TVP7000,0x01,0x10,0x80 // SOG Threshold-(RGB Clamp)
WR_REG,TVP7000,0x01,0x19,0xAA // INPUT MUX SELECT    RGB CH3 selected
WR_REG,TVP7000,0x01,0x1A,0x80 // INPUT MUX SELECT  HSYNC_A and VSYNC_A selected
WR_REG,TVP7000,0x01,0x1E,0x1F // COARSE OFFSET BLUE
WR_REG,TVP7000,0x01,0x1F,0x1F // COARSE OFFSET GREEN
WR_REG,TVP7000,0x01,0x20,0x1F // COARSE OFFSET BLUE
WR_REG,TVP7000,0x01,0x21,0x08 // HSOUT START
WR_REG,TVP7000,0x01,0x26,0x80 // ALC RED and GREEN LSB
WR_REG,TVP7000,0x01,0x28,0x73 // AL FILTER Control
WR_REG,TVP7000,0x01,0x2A,0x07 // Enable FINE CLAMP CONTROL
WR_REG,TVP7000,0x01,0x2B,0x00 // POWER CONTROL-SOG ON
WR_REG,TVP7000,0x01,0x2C,0x50 // ADC Setup
WR_REG,TVP7000,0x01,0x31,0x18 // ALC PLACEMENT
WR_REG,TVP7000,0x01,0x07,0x40 // HSYNC OUTPUT WIDTH - 64
WR_REG,TVP7000,0x01,0x0E,0x00 // SYNC CONTROL  HSout-

// THS8200 I2C register settings
WR_REG,THS8200,0x01,0x03,0xC1 // chip_ctl
WR_REG,THS8200,0x01,0x19,0x03 // csc_offset3
WR_REG,THS8200,0x01,0x1C,0x70 // dman_cntl
WR_REG,THS8200,0x01,0x34,0x03 // dtg_total_pixel_msb
WR_REG,THS8200,0x01,0x35,0x48 // dtg_total_pixel_lsb
WR_REG,THS8200,0x01,0x36,0x80 // dtg_linecnt_msb
WR_REG,THS8200,0x01,0x37,0x02 // dtg_linecnt_lsb
WR_REG,THS8200,0x01,0x38,0x87 // dtg_mode
WR_REG,THS8200,0x01,0x39,0x11 // dtg_frame_field_msb
WR_REG,THS8200,0x01,0x3A,0xf4 // dtg_frame_size_lsb
WR_REG,THS8200,0x01,0x3B,0xf4 // dtg_field_size_lsb
WR_REG,THS8200,0x01,0x3C,0x80 // dtg_vesa_cbar_size
WR_REG,THS8200,0x01,0x4A,0x00 //
WR_REG,THS8200,0x01,0x4F,0x00 // csm_mode
WR_REG,THS8200,0x01,0x70,0x40 // dtg_hlength_lsb
WR_REG,THS8200,0x01,0x71,0x03 // dtg_hdly_msb
WR_REG,THS8200,0x01,0x72,0x1f // dtg_hdly_lsb
WR_REG,THS8200,0x01,0x73,0x04 // dtg_vlength_lsb
WR_REG,THS8200,0x01,0x74,0x00 // dtg_vdly_msb
WR_REG,THS8200,0x01,0x75,0x01 // dtg_vdly_lsb
WR_REG,THS8200,0x01,0x76,0x00 // dtg_vlength2_lsb
WR_REG,THS8200,0x01,0x77,0x07 // dtg_vdly2_msb
WR_REG,THS8200,0x01,0x78,0xFF // dtg_vdly2_lsb
WR_REG,THS8200,0x01,0x79,0x00 // dtg_hs_in_dly_msb
WR_REG,THS8200,0x01,0x7A,0x29 // dtg_hs_in_dly_lsb
WR_REG,THS8200,0x01,0x7B,0x00 // dtg_vs_in_dly_msb
WR_REG,THS8200,0x01,0x7C,0x00 // dtg_vs_in_dly_lsb
WR_REG,THS8200,0x01,0x82,0x40 // pol_cntl

END_DATASET
```

Each command file may contain individual write-to-register (WR_REG) commands.

1. The comment indicator is the double-slash //.
2. The command file is not case-sensitive and ignores all white-space characters.
3. All numbers can be entered as hexadecimal (beginning with 0x) or as decimal.
4. Every data set in a command file begins with BEGIN_DATASET and ends with END_DATASET. The maximum number of datasets is 250.
5. The dataset text description is entered between double quotes using the DATASET_NAME command. The enclosed text can be up to 128 characters in length. This text appears in the *System Initialization* dialog box when the command file is opened.
6. The INCLUDE command inserts the contents of an include file (with an .INC file extension) in-line in place of the INCLUDE command. Therefore, the include file must not contain the BEGIN_DATASET, END_DATASET, and DATASET_NAME commands.

   NOTE: All included files must be located in the same directory as the command (CMD) file.

7. The write-to-register command is written as follows:

   WR_REG, <DeviceFamily>, <Number of data bytes (N)>, <subaddress>, <Data1>,…, <DataN>

   or

   WR_REG, <Literal slave address>, <Number of data bytes (N)>, <subaddress>, <Data1>,…, <DataN>

   The valid device family mnemonics are:

   VID_DEC for the video decoders

   VID_ENC for the video encoders

   THS8200 for the THS8200 device

   WinVCC translates the device family mnemonic to the slave address that was selected in the *WinVCC Configuration* dialog box upon program startup. This eliminates having to edit command files if the alternate slave address must be used.

   If the literal slave address method is used, then the slave address entered will be used directly. This method is normally used for programming the video encoder.

8. A delay may be inserted between commands using the WAIT command, which is written as follows:

   WAIT,<# milliseconds>

8.4.2 Register Editing

The next section describes the four available modes of register editing: *Register Map Editor*, *Encoder Module Editor*, *Generic I2C Register Editor*, and *Property Sheets*. Each of these functions can be selected from the *Edit* menu.

8.4.2.1 Register Map Editor

The register map editor, as shown in Figure 11, allows the display and editing of the entire used register space of the device within a simple scrolling text box. To open this, click on *Edit Register Map* in the *Edit* menu and click on the device type to edit. If the intended device type is not shown, then use the Windows menu to activate the existing window.

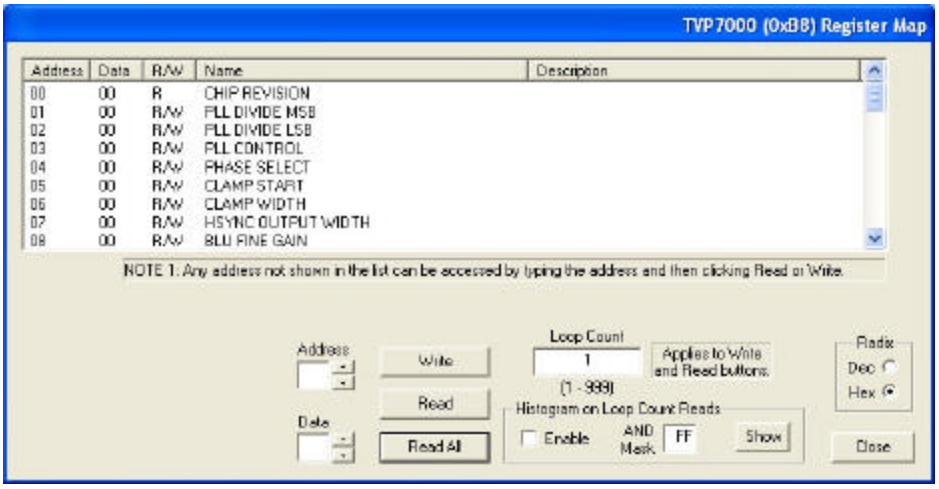


Figure 11. TVP7000 Register Map

Figure 12 is the THS8200 register map.

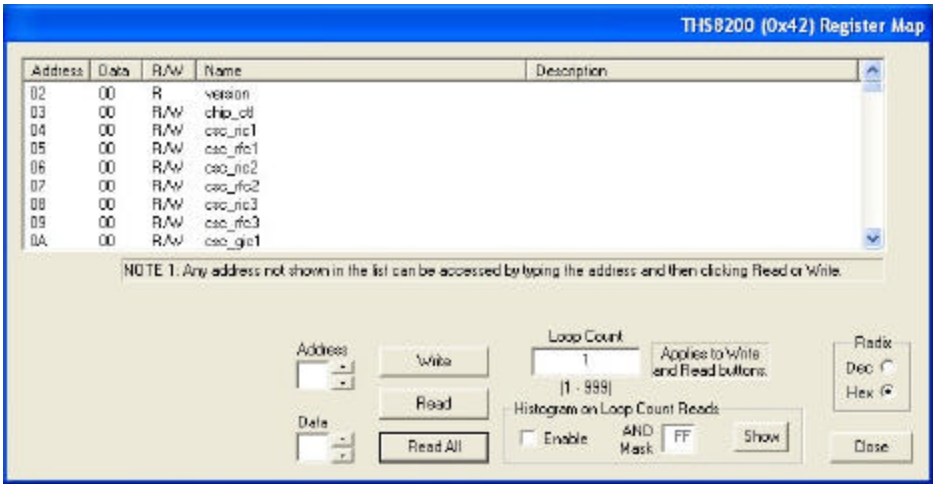


Figure 12. THS8200 Register Map

Table 5. Register Map Editor Controls

Control	Definition
Register Window	Scrolling text box that displays the address and data for the I^2C registers that are defined for the device.
Address Edit Box	This contains the I^2C subaddress that will be accessed using the *Write* and *Read* buttons. Clicking on a row selects an address, which then appears in the address edit box. NOTE: After clicking on a row, the *Data Edit* box contains the data that was in the register window. The device has not yet been read. The address up/down arrows are used to jump to the next/previous subaddress that is defined for the device. If an address is not defined for the device, then it can still be accessed by typing the subaddress in the *Address Edit* box.
Data Edit Box	This contains the data which will be written to or was read from the I^2C subaddress. The data up/down arrows increment/decrement the data value by 1.
Write Button	Writes the byte in the *Data Edit* box to the address in the *Address Edit* box. The I^2C register is written to whether or not the data is different from the last time the register was read.
Read Button	Reads the data from the address in the *Address Edit* box into the *Data Edit* box and the register window.
Read All Button	Reads all defined readable registers from the device and updates the register window.
Hex Button	Converts all values in the register window and address and data edit boxes to hexadecimal.
Dec Button	Converts all values in the register window and address and data edit boxes to decimal.
Close Button	Closes the dialog. NOTE: Multiple edit register map windows can be open at the same time (one for each device). Use the Window menu to navigate.
Loop Count	Causes subsequent write or read operations to be performed N times. N is entered as a decimal number from 1 to 999.
Edit Indirect Registers	Opens the indirect register editor of the TVP7000.

8.4.2.2 Generic I²C Register Editor

The *Generic I2C Register Editor*, see Figure 13, allows the display and editing of any device on the I²C bus. This editor works like the *Register Map Editor*, except that the I²C slave address must be entered and the *Read All* button is disabled.

To open this, click on *Edit Register Map* in the *Edit* menu and then click on *Generic I2C*.

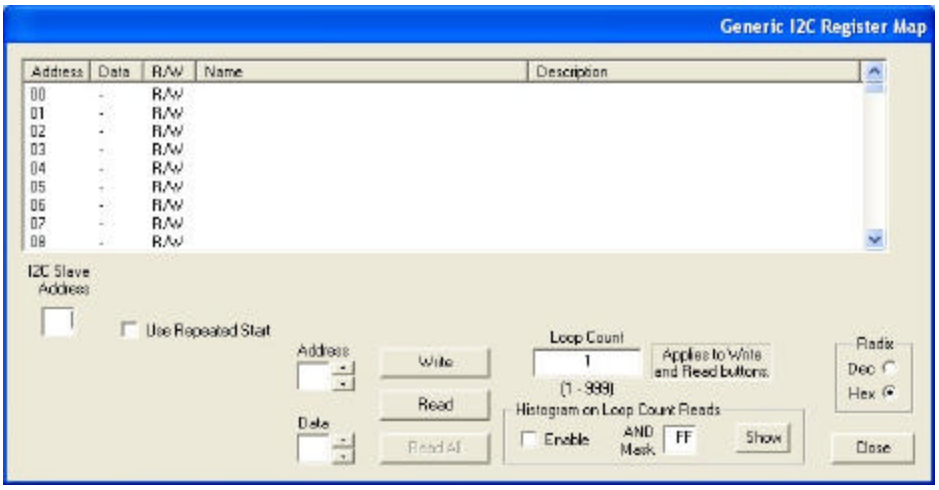


Figure 13. Generic I²C Register Editor

8.5 TVP7000 Property Sheets

The property sheets represent the register data in a user-friendly format. The data is organized by function, with each function having its own page and being selectable via tabs at the top.

To open this, click on *Edit Property Sheets* in the *Edit* menu and select the device type to edit.

When the property sheet function is started or whenever you tab to a different page, all readable registers in the device are read from hardware to initialize the dialog pages. Values on the page are changed by manipulating the various dialog controls.

There are *OK*, *Cancel*, and *Apply* buttons at the bottom of each property page.

With the TVP7000, there are six different tabs available within its property sheets. The tabs are organized by the TVP7000 functions. The following subsections describe the additional details and recommendations of the controls within each tab.

8.5.1 Input Mux

Auto detect is recommended for HSYNC/VSYNC selection and HSYNC input polarity. The TVP7000 automatically senses the presence of SOG and discrete HSYNC and VSYNC inputs. If SOG and discrete syncs are both present, then the TVP7000 automatically selects and uses the discrete syncs. Input sync status is available in the sync detect status I^2C register (14h) and can be viewed using the status property sheet. The BNC on the TVP7000 EVM inputs must be used for SOG operation.

SOG threshold (register 10h) sets the voltage level of the SOG slicer comparator. Each step represents an 11-mV change in slice level. A middle range setting of 10h is recommended.

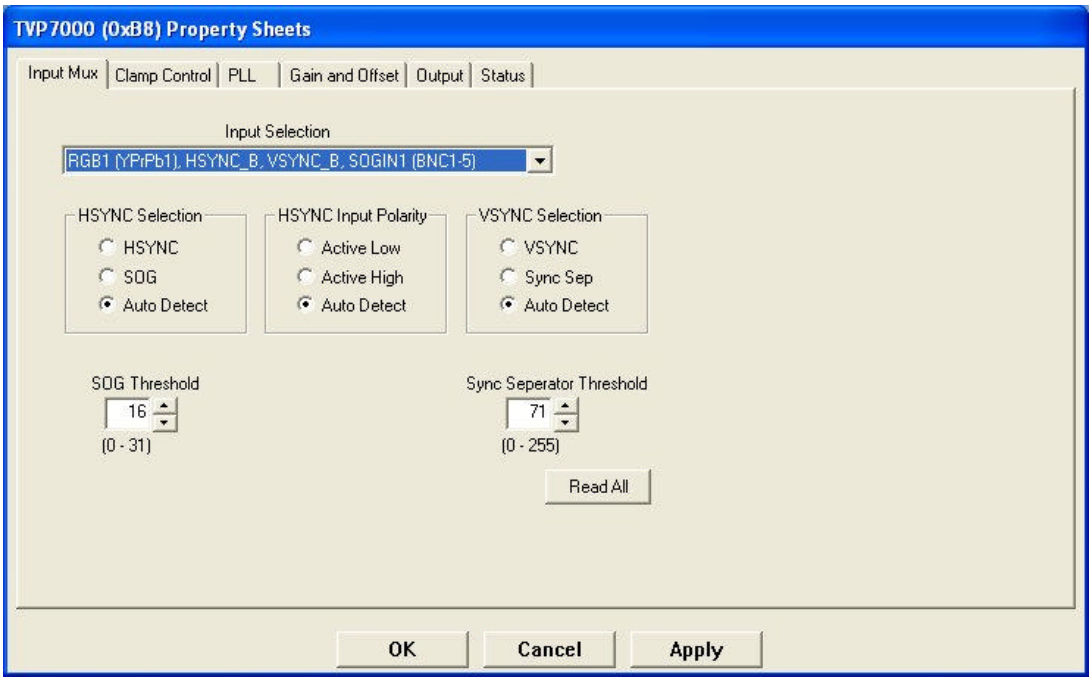


Figure 14. Input Mux – Property Sheet

8.5.2 Clamp

Most ac-coupled video applications use the internally-generated clamp pulse for dc restoration prior to the ADCs. The fine clamp must be enabled for all three channels and correctly positioned during the horizontal blanking interval. The fine clamp start (I^2C register 05h) is relative to HSYNC trailing or leading edge depending on the clamp REF bit setting in I^2C register 15h. See Figure 15 for recommended clamp placement settings for various input formats.

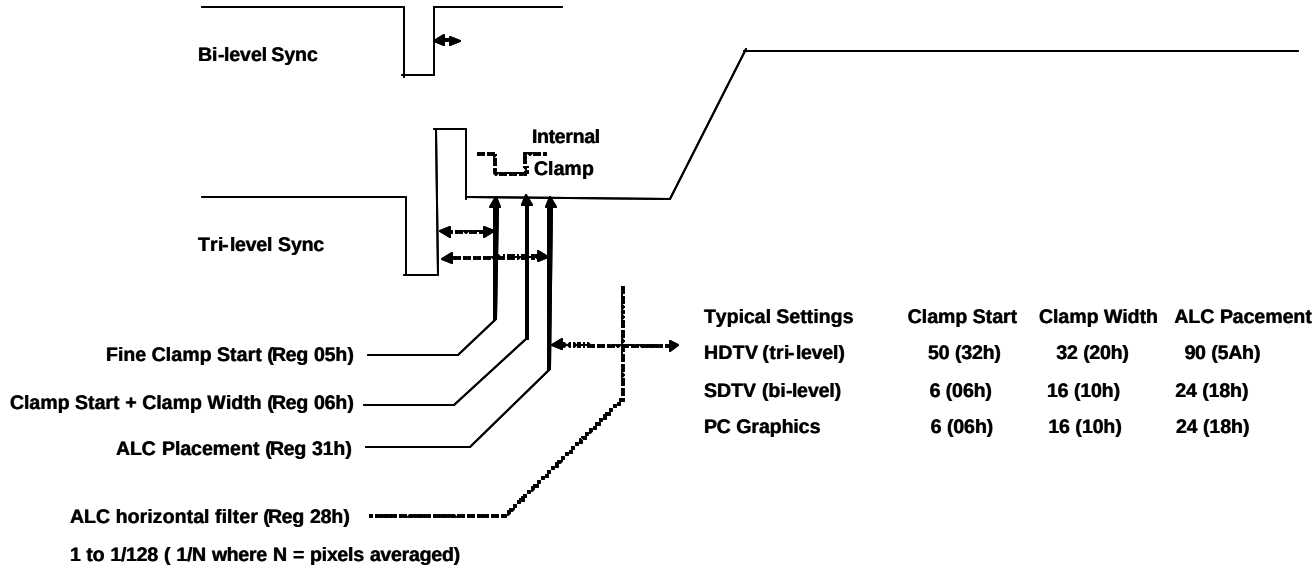


Figure 15. Clamp Placement

Placement is relative to end of negative SYNC tip. ALC horizontal filter may be limited by back porch area for some formats.

Either bottom or middle level clamping can be selected. These must be set according to the video input format. Bottom level clamping must be used for Y and RGB inputs. Middle level clamping must be used for Pb and Pr inputs. Coarse clamp must be left disabled for most applications. A typical clamp setup for RGB graphics is shown in Table 6 and Figure 16.

Clamp charge pump current must be left on highest setting. Clamp polarity is only effective when an external clamp is used.

Table 6. Typical Clamp Setup for RGB Graphics

I2C Address	Setting	Description
05h	06h	Clamp start
06h	10h	Clamp width
0Fh	0Eh	Internal Clamp enabled
10h	80h	Bottom level clamping for RGB
15h	00h	Clamp pulse relative to HSYN trailing edge
2Ah	07h	Enable fine clamps
2Dh	00h	Coarse Clamp disabled

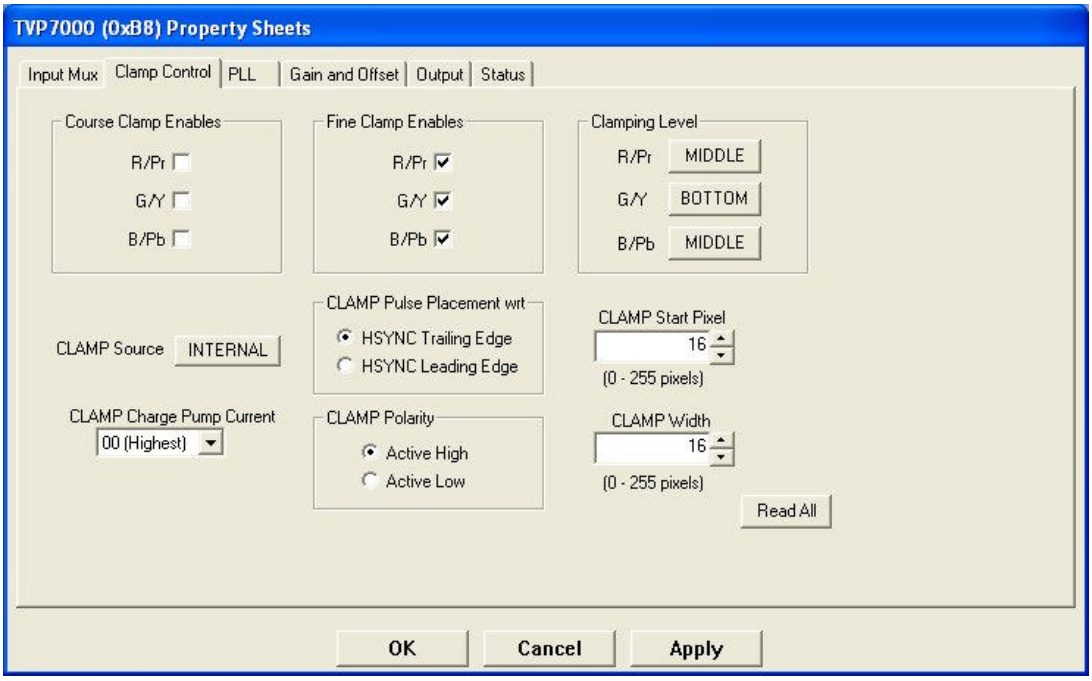


Figure 16. Clamp Control – Property Sheet

8.5.3 PLL

The feedback divider is typically set to the total number of pixels per line. A 2x feedback divider value can be used if the DIV2 bit (DATACLK/2) in I^2C register 04h is set to 1. This can offer improved jitter performance, when low pixel rate formats are used. The pixel clock rate is derived from the HSYNC input frequency, feedback divider, and the DIV2 bit.

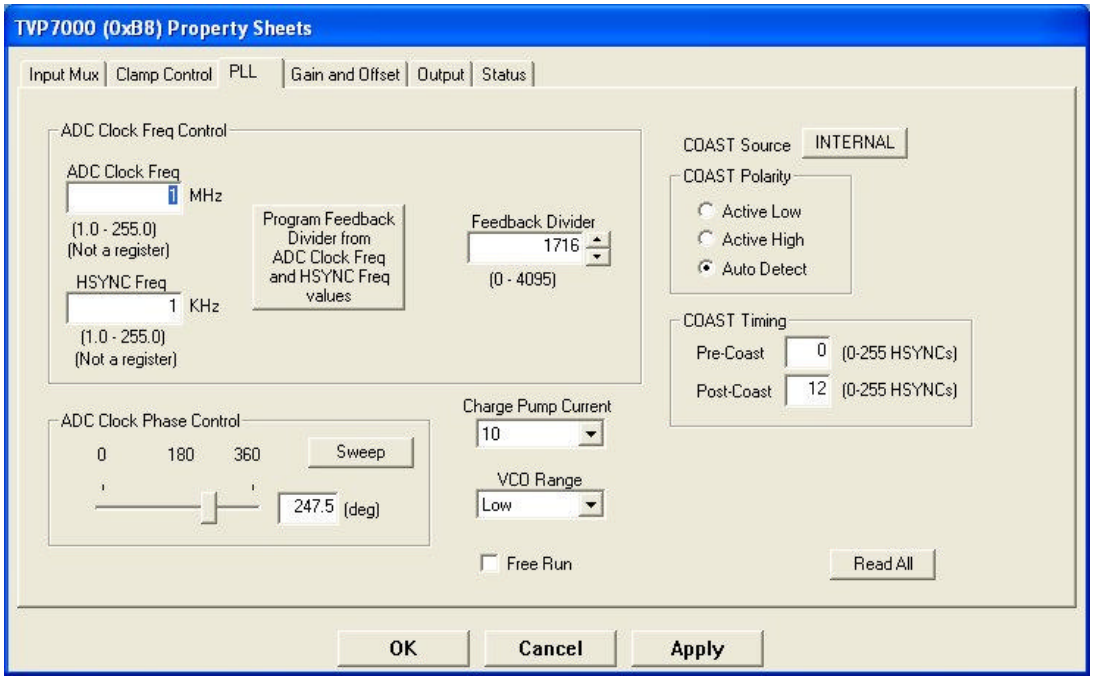


Figure 17. PLL – Property Sheet

An internally- or externally-generated coast signal can be used to put the PLL in coast or free-run mode to avoid disruptions in HSYNC during vertical blanking. When the internal coast is in use, the pre-coast and post-coast settings specify the coast interval range relative to the internally-detected VSYNC. Pre-coast specifies the number of lines before detecting VSYNC, and post-coast specifies the number of lines after VSYNC that are used for the coast interval. Additional post-coast lines are required when Macrovision is present on the video input. The MAC_EN bit in I^2C register 22h must be set to 1 for Macrovision compatibility. External coast must be enabled when discrete HSYNC and VSYNC are used.

Table 7. Recommended Coast Settings

Format	Pre-Coast	Post-Coast
480i/p with Macrovision	03h	0Ch
576i/p	03h	0Ch
1080i	03h	00h
1080p	00h	00h
720p	00h	00h

8.5.4 Gain and Offset – ALC

Stable output offset levels are maintained by use of the ALC feedback level control in the TVP7000. Two sets of filter coefficients are available that define the level of filtering applied on each line (horizontal) and the amount of feedback correction that is applied per line update (vertical). The horizontal coefficient (register 28h, NSH[2:1]) specifies the number of pixels that are used in the horizontal filter. The ALC filter must be applied during the horizontal blank interval following the clamp pulse, so it must be correctly positioned using the ALC placement register (register 31h). NSH coefficients range from 1 to 1/N, where N is the number of pixels used in the filter. The amount of horizontal filtering that can used will depend on the ALC placement and the horizontal blanking interval of the input video format. See Table 8 for recommended ALC placement settings.

The vertical coefficient (register 28h, NSV[3:0]) specifies the amount of feedback error correction derived from the horizontal filter that is applied to each line update. The NSV coefficient can range from 1 (maximum error applied) to 1/32768 (minimum error applied).

The ALC must be enabled by setting bit 7 of I^2C register 26h to 1. In the ALC operating mode, the fine offset registers are used to position the digital output levels. The coarse offset levels must be set to 1Fh and left unchanged for optimum ALC performance. Fine offset settings are relative to the bottom level (ADC code 0) for bottom-clamped signals and the middle level (ADC code 512) for middle-clamped signals.

Table 8. Typical ALC Setup for RGB Graphics

Address	Setting	Description
05h	06h	Clamp Start
06h	10h	Clamp Width
0Bh	80h	Blue Fine Offset
0Ch	80h	Green Fine Offset
0Dh	80h	Red Fine Offset
26h	80h	Enable ALC
28h	73h	ALC Filter
31h	18h	ALC Placement
1Eh	1Fh	Coarse Offset Blue
1Fh	1Fh	Coarse Offset Green
20h	1Fh	Coarse Offset Blue

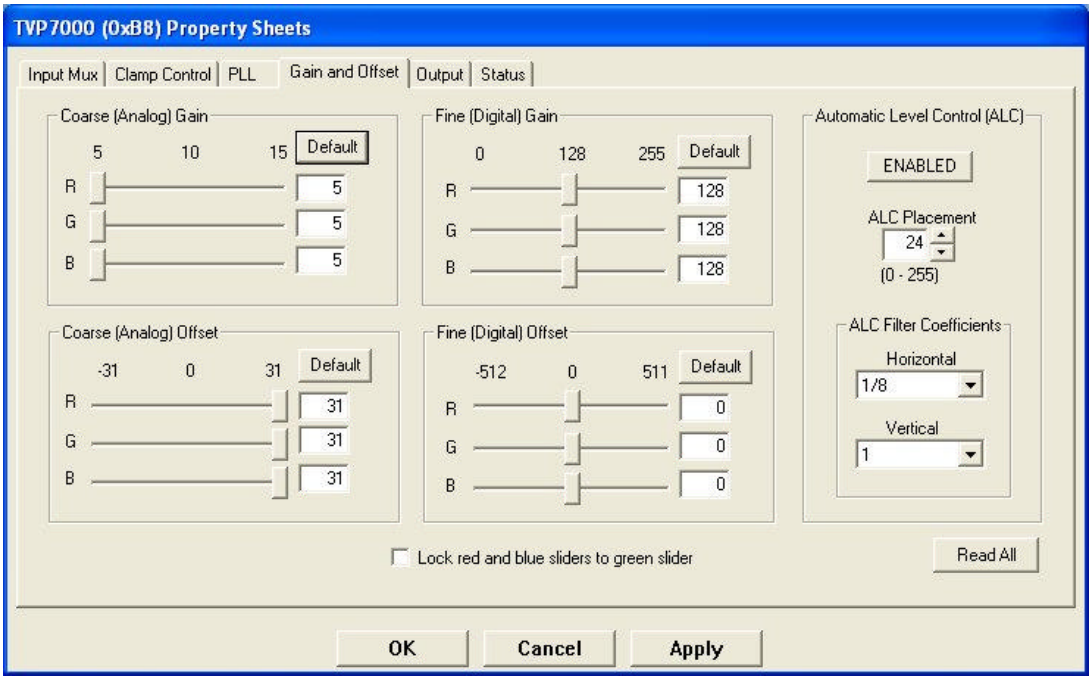


Figure 18. Gain and Offset – Property Sheet

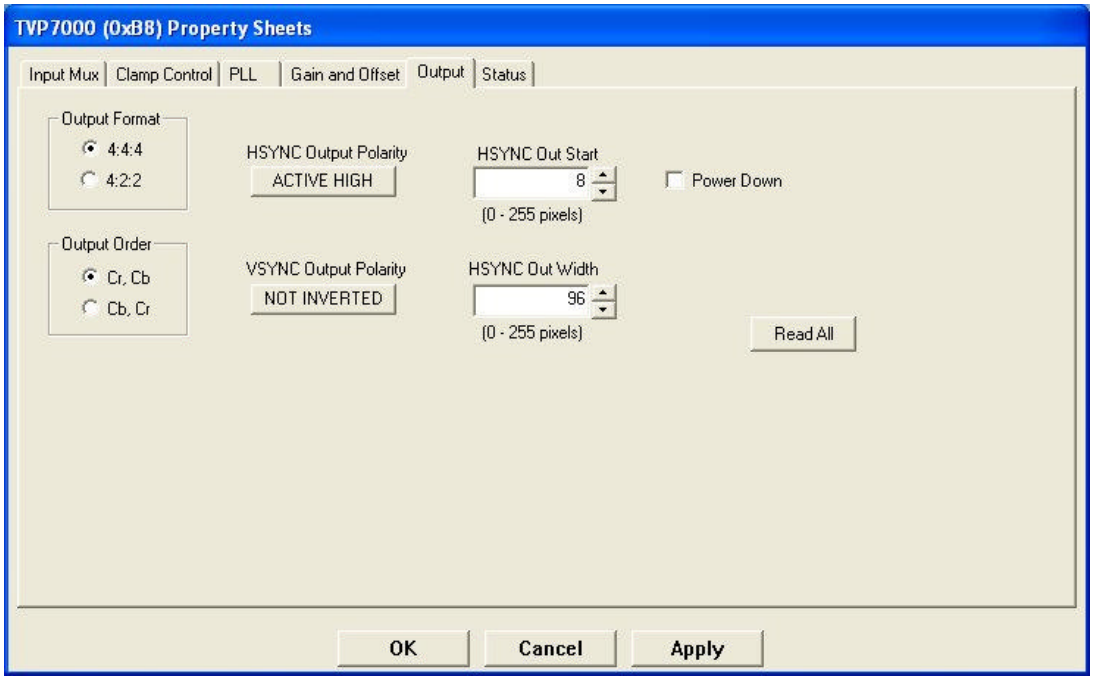


Figure 19. Output – Property Sheet

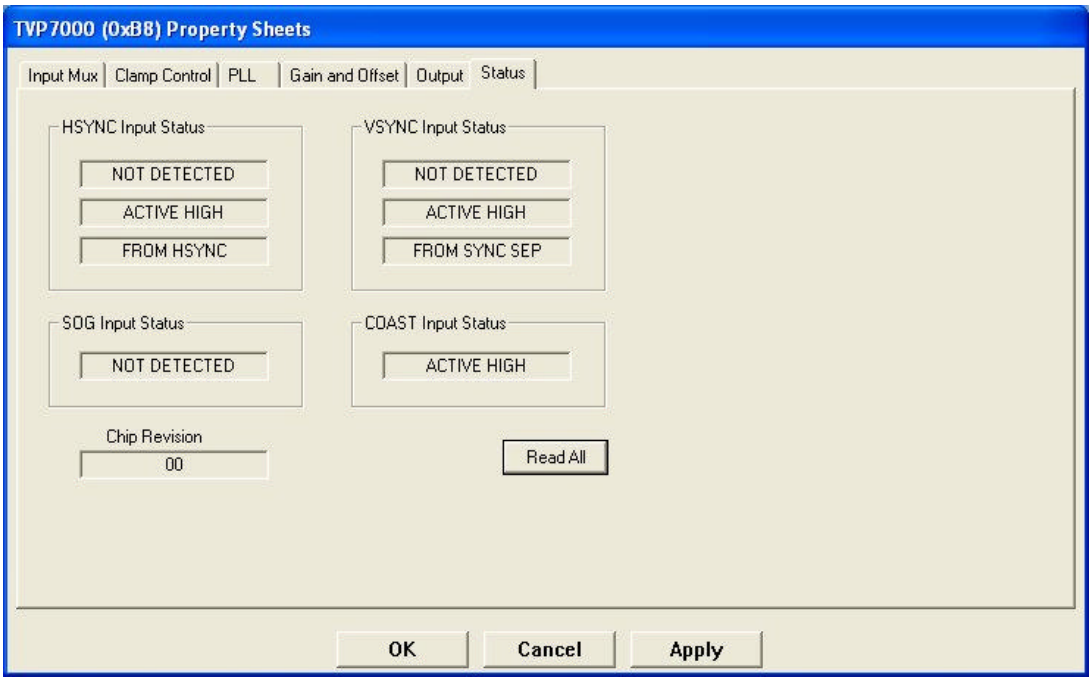


Figure 20. Status – Property Sheet

8.5.4.1 Reading the Register Map

The property sheets were designed so that the data displayed is always current. Certain actions cause the entire register map to be read from the device and to update the property sheets. This happens when:

1. Property sheets are initially opened.
2. When tabbing from one page to another.
3. When *Read All* is clicked.
4. When making the *Property Sheets* window the active window (by clicking on it).
5. When making a *Register Map Editor* window the active window (by clicking on it).

8.5.4.2 Auto-Update from Device

Items 4 and 5 above are referred to as the *Auto-Update* feature. *Auto-Update* can be disabled by setting its program option button to DISABLED. This button is located on the initial dialog box (WinVCC Configuration).

With *Auto-Update* enabled (default), the user can open both the *Property Sheets* and the *Register Map Editor* at the same time. Changes made to the *Property Sheets* (and applied) are updated in the register map window as soon as the *Register Map* window is clicked on. It also works the other way; changes made in the *Register Map Editor* are updated in the *Property Sheets* as soon as the *Property Sheets* window is clicked on.

Table 9. Use of Property Sheet Controls

Dialog Control	What Do I Do With It?	When is Hardware Updated?
Read-Only Edit Box	Read status information	N/A
Check Box	Toggle a single bit	After *Apply*
Drop-Down List	Select from a text list	After *Apply*
Edit Box	Type a number	After *Apply*
Edit Box with Up/Down arrows	Use up/down arrows or type a number	Up/Down Arrows: Immediately Type a number: After *Apply*
Slider	Slide a lever	Immediately
Pushbutton	Initiate an action	Immediately

Table 10. Property Sheet Button Controls

Button Control	Definition
OK	Writes to all writeable registers whose data has changed. A register is flagged as changed if the value to be written is different from the value last read from that address. Closes the dialog.
Cancel	Causes all changes made to the property page since the last *Apply* to be discarded. Changes made to dialog controls with 'immediate hardware update' are not discarded, since they have already been changed in hardware. Does not write to hardware. Closes the dialog.
Apply	Writes to all writeable registers whose data has changed. A register is flagged as changed if the value to be written is different from the value last read from that address.

9 Troubleshooting

This chapter discusses ways to troubleshoot the TVP7000EVM.

9.1 Troubleshooting Guide

If you are experiencing problems with the TVP7000EVM hardware or the WinVCC software, see Table 11 for available solutions.

Table 11. TVP7000EVM Troubleshooting

Symptom	Cause	Solution
At startup, the error message *Cannot find DLL file DLPORTIO.DLL* appears.	The parallel port driver supplied with the EVM has not been installed.	Run Port95NT.EXE on the CD to install the driver.
Blank screen	Wrong analog input is selected.	Go to Edit->Property Sheets->TVP7000, Analog Video page, select the correct video input(s) and click *Apply*. (The Composite Video 1 input is default.)
	Source is connected to the wrong input connector.	Connect source to the correct input connector.
Vertical Stability Or Flashing display	Mode detect issue due to HSYNC/VSYNC alignment	Adjust HSYNC output delay
Line Noise present with High Frequency vertical line input pattern	PLL phase setting is not set correctly for the input source	Adjust PLL phase setting
Line noise present with flat field	Excessive noise on the input source	Filter the inputs or try a different source
Picture too dark	Clamp or ALC not set correctly	Reposition Clamp or ALC. Reduce ALC horizontal filter coefficient
SOG/Y does not work	SOG clamp disabled	Set SOG_CE bit in register 2Eh to 1.
SOG does not work when using the VGA connector	The VGA input is not connected to an SOG input pin	The BNC connectors must be used for SOG operation

Table 12. I²C Troubleshooting

Symptom	Cause	Solution
No I²C communication	I²C slave address is wrong.	Close and restart WinVCC. Choose the alternate slave address in the WinVCC Configuration dialog.
	Parallel cable is not connected from PC parallel port to the EVM DB25 connector.	Connect cable.
	EVM is not powered on.	The power supply must be plugged into a 100-V to 240-V/ 47-Hz to 63-Hz power source and the cord must be plugged into the power connector on the EVM.
	Wrong type of parallel cable.	Some parallel cables are not wired straight through pin-for-pin. Use the cable supplied with the EVM.
	PC parallel port mode is not set correctly.	Reboot PC, enter BIOS setup program, set parallel port LPT1 mode (address 378h) to ECP mode or bidirectional mode (sometimes called PS/2 mode or byte mode). If already set to one of these two modes, switch to the other setting. See Section 4.2.1.
	Device was placed in power–down mode.	Press the reset button on the TVP7000EVM.
	EVM was configured for an external I²C master.	Reinstall 0-? resistors R5 and R6. Control EVM using the PC parallel port.
	Still no I²C communication	The PC may not be capable of operating in the required parallel port mode. This is true of some laptop computers. Use a different computer, preferably a desktop PC.

When WinVCC is started and the WinVCC Configuration dialog box is closed with *OK*, the I²C system test is performed (unless the I2C System Test program options button was disabled).

If the I^2C system test fails, a dialog box will appear. Figure 21 reports that a read from TVP7000 failed, using slave address 0xB8, subaddress 0x05. The data read was 0x00.

After noting which device had a problem, click *OK* to continue. Next, the *Corrective Action Dialog* box appears to help fix the problem.

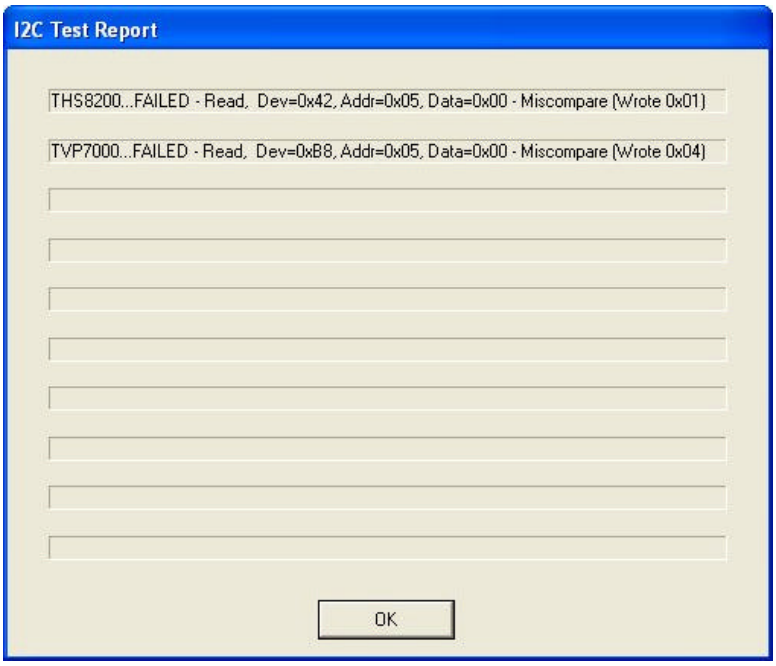


Figure 21. I^2C System Failure Dialog Box

9.2 Corrective Action Dialogs

After closing the I^2C system test report dialog box, the dialog box in Figure 22 appears.

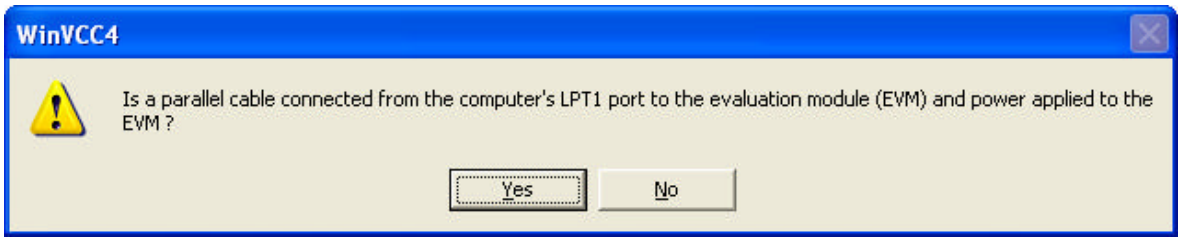


Figure 22. Corrective Action Dialog Box

1. If the parallel port cable is NOT connected between to PC and the TVP7000EVM or if the EVM power is not on, then:
   a. Click *NO*.
   b. The dialog box shown in Figure 23 appears instructing you to correct the problem.
   c. Correct the problem.
   d. Click *OK* to continue

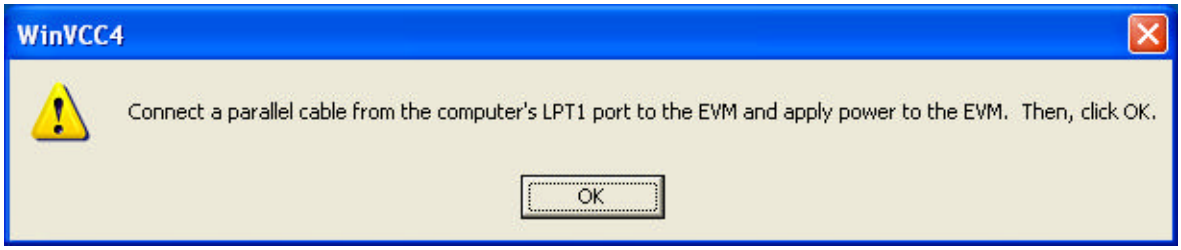


Figure 23. Corrective Action Required

2. If the cable is connected from the PC parallel port to the TVP7000EVM and the EVM power is on:
   a. Click *Yes*.
   b. The dialog box shown in Figure 24 appears. This dialog box appears if the PC parallel port mode setting may need to be changed.

   NOTE: Only run the PC BIOS setup program if the I^2C communication problem cannot be resolved in another way (correct slave address settings, reset or power cycle the EVM, and/or check that the device type selected was TVP7000).

   c. Click *OK* to continue.
   d. Click *OK* to close it and get to the main menu.
   e. Click *Exit* in the *File* menu to exit the program.

f. See troubleshooting guide above.

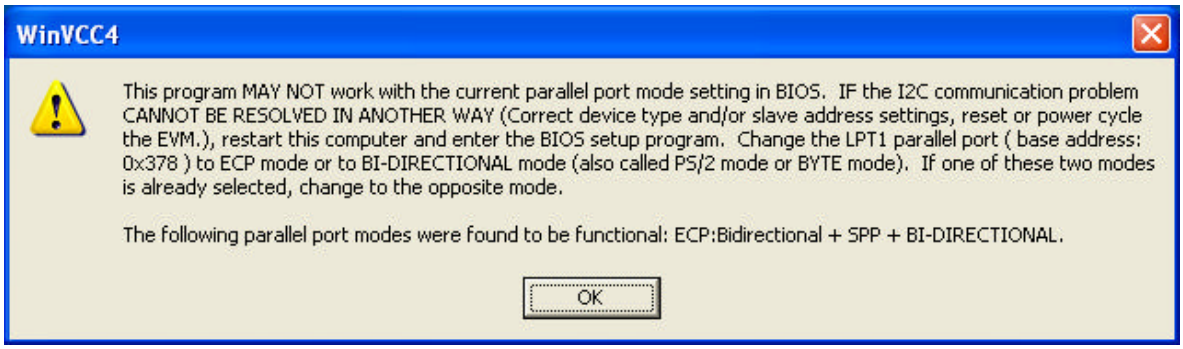


Figure 24. Corrective Action Required

9.2.1 Setting the PC Parallel Port Mode

NOTE: Only run the PC BIOS setup program if the I^2C communication problem cannot be resolved in another way (correct slave address settings, reset or power cycle the EVM, and/or check that the device type selected was TVP7000).

1. Restart the PC.
2. During the boot process, enter the BIOS setup program by pressing the required key (usually the initial text screen tells you which key to press).
3. Find the place where the parallel port settings are made.
4. Set the parallel port LPT1 at address 378h to ECP mode or bidirectional mode (sometimes called PS/2 mode or byte mode). If one of these two modes is already selected, then change to the opposite mode.
5. Exit and save changes.

9.2.2 General I^2C Error Report

The error report shown in Figure 25 appears when an I^2C error occurs at any time other than after the I^2C system test. In this example, there was an acknowledge error at slave address 0x54 (the video Triple ADC module). The error occurred on *Read Cycle Phase 1* on the device (slave) address byte.

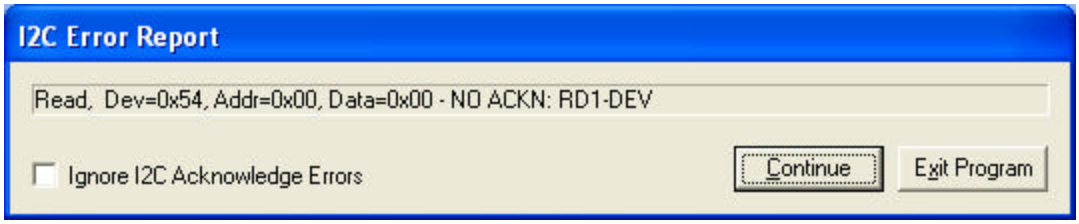
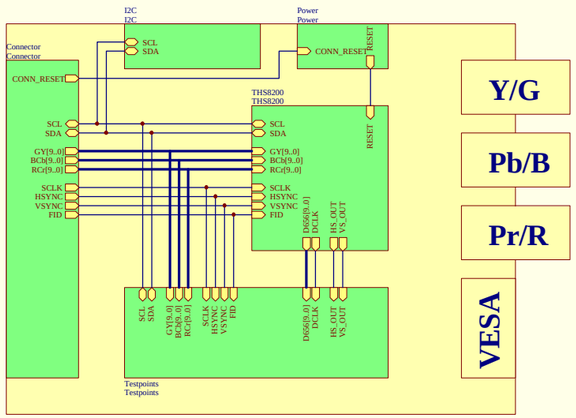


Figure 25. I^2C Error

10 TVP7000EVM Schematics

This chapter contains the TVP7000EVM schematics.

THS8200EVM REV1_1



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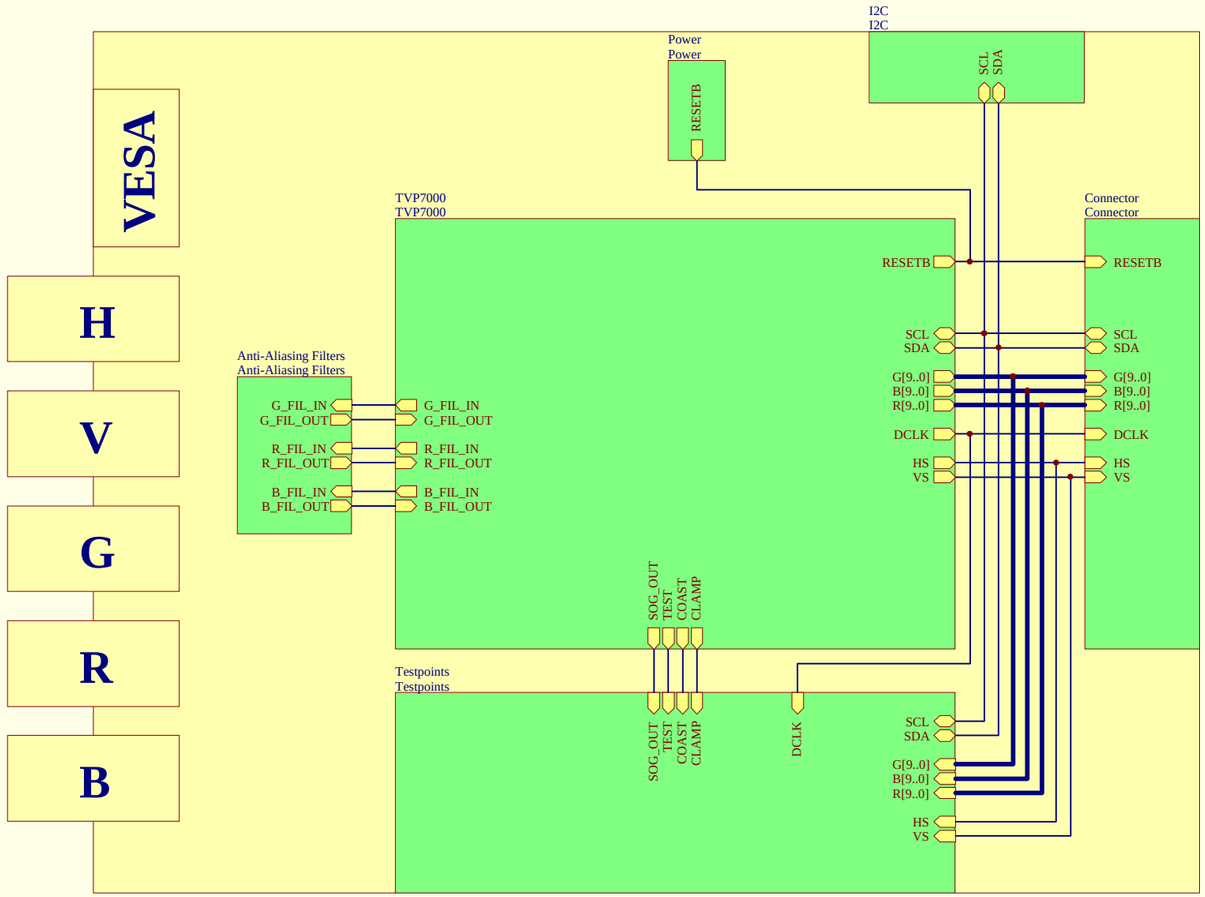
TVP7000EVM Rev 1.0



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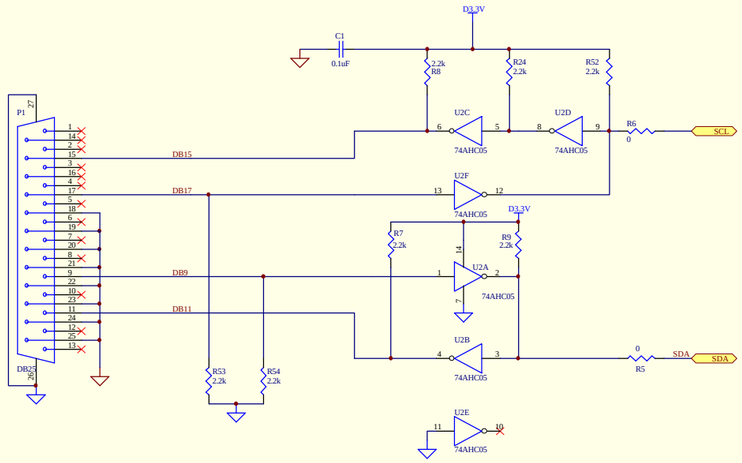

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Sheet of	
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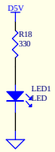
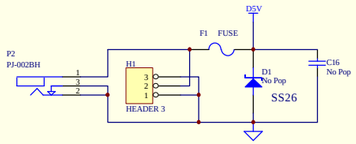
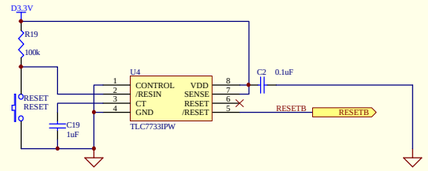
POWER ON LED (+5V)



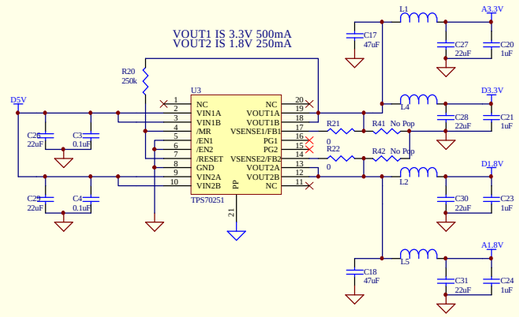
5V, 3.0A DC INPUT



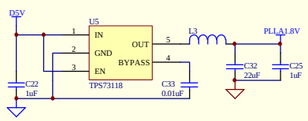
RESET ON POWER UP



VOUT1 IS 3.3V 500mA
VOUT2 IS 1.8V 250mA



PLL A1.8V 150mA



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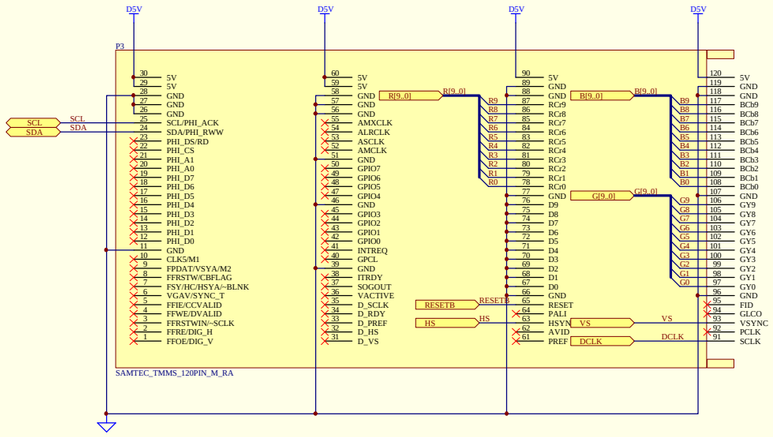

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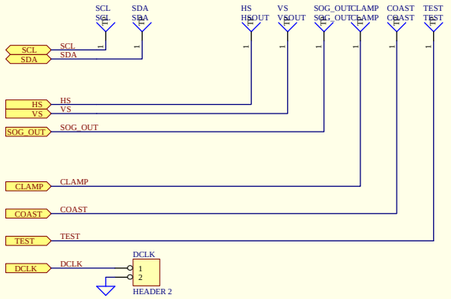

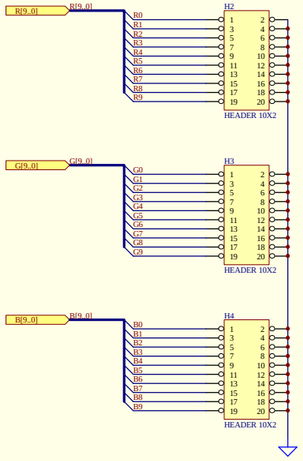

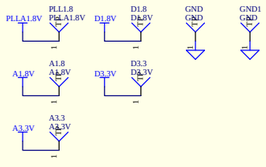

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Size: C	Number:	Revision: REV 1.1
Date: 3-Aug-2005	Sheet of	
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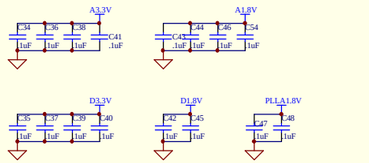
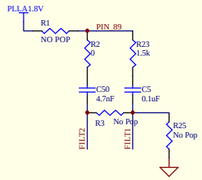
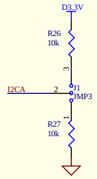


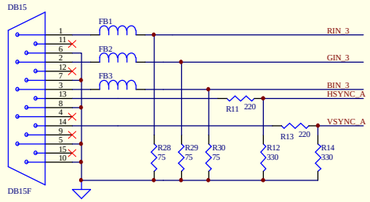


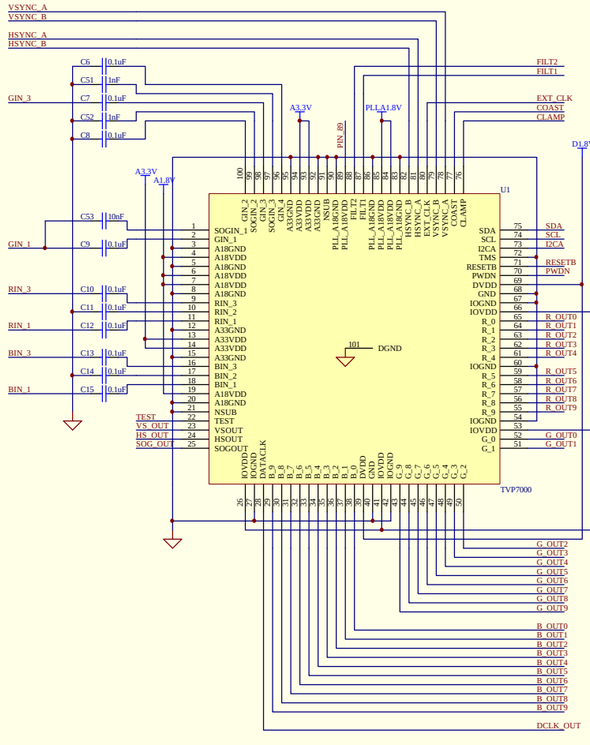
I2C ADDRESS SELECTION

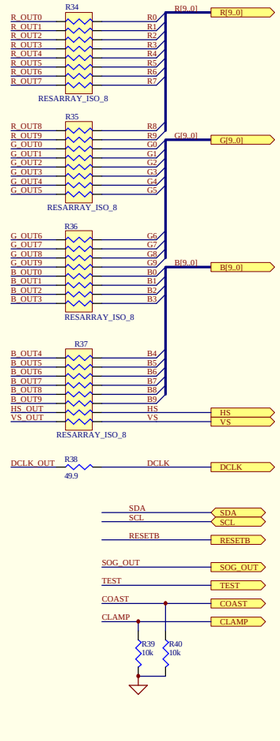
2-3: Base Addr 0xBA

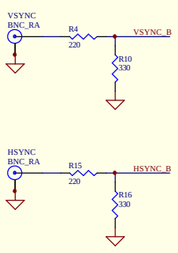
1-2: Base Addr 0xB8 - Default

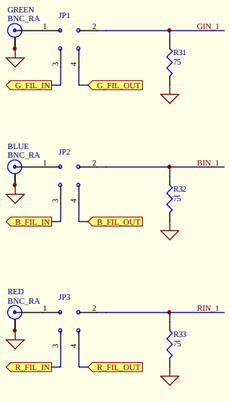


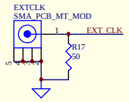












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Size: C	Number:	Revision: REV 1.1
Date: 3-Aug-2005	Sheet of	
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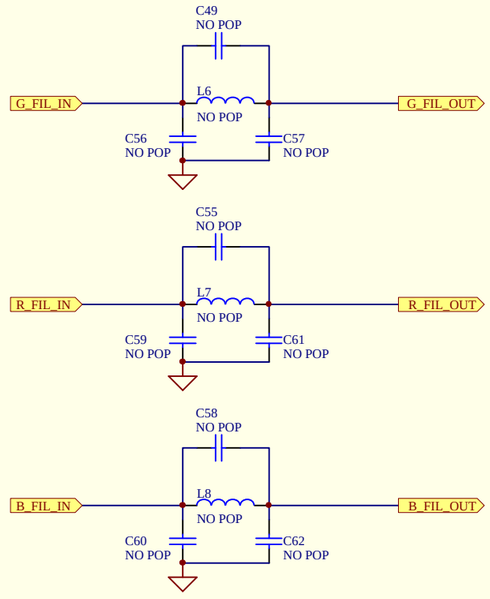

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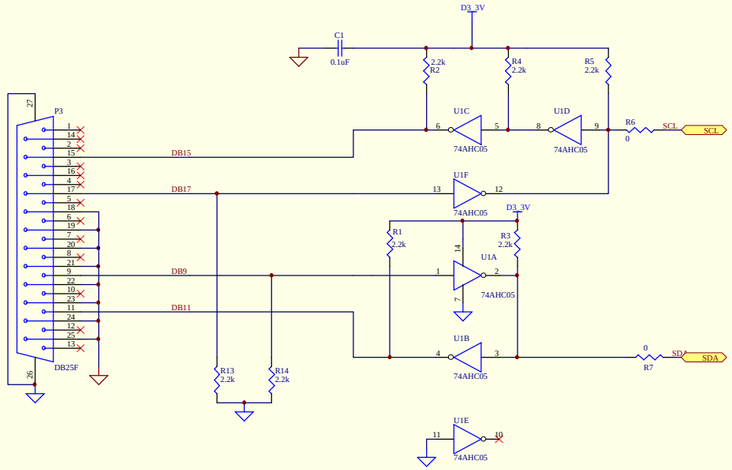
Size	B	Number		Revision	REV 1.1
Date:	3-Aug-2005			Sheet of	
File:	E:\EVM Design Files\TVP7000_EVM_MODULE_REV1.0\TVP7000_EVM_MODULE_REV1.0.ddb			Drawn By:	



Title	THS8200 EVM REV1.1 - I2C	
Size: C	Number:	Revision: REV 1.1
Date: 27-Sep-2005	Sheet 2 of 6	
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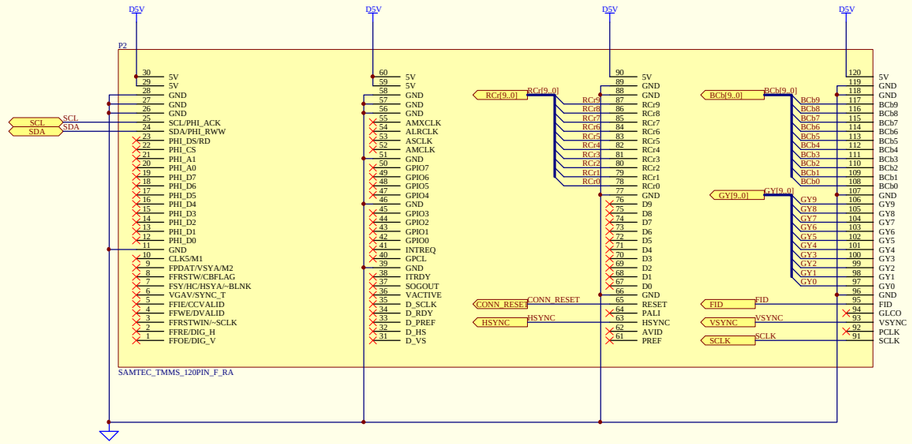
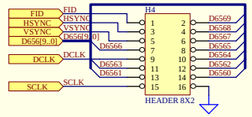
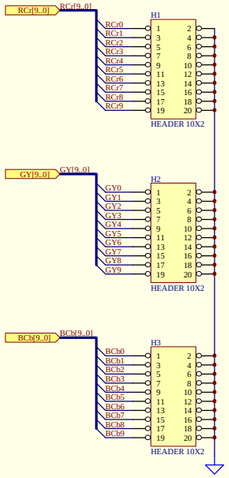
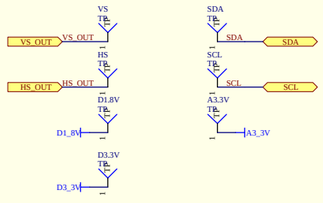


Title	THS8200 EVM REV 1.1 - CONNECTOR		
Size C	Number	Revision REV 1.1	
Date: 27-Sep-2005	Sheet 3 of 6		
File: X:\EVM Design Files\TVP7000_EVM_MODULE_REV1.0\TVP7000EVM_RTM\THS8200EVM_MODULE_REV1_2\THS8200EVM_MODULE_REV1_2.ddb			



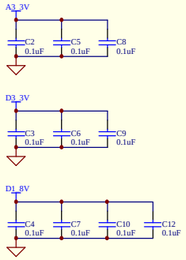




Title
THS8200 EVM REV1.1 - TESTPOINTS

Size	Number	Revision
C		REV 1.1

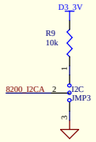
Date: 27-Sep-2005 Sheet 4 of 6
File: X:\EVM Design Files\TVP7000_EVM_MODULE_REV1.0\TVP7000EVM_RTM\THS8200EVM_MODULE_REV1_2\THS8200EVM_MODULE_REV1_2.ddb

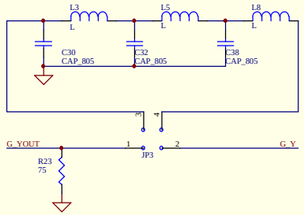


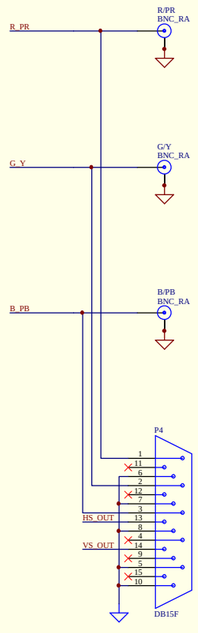
THS8200 I2C ADDRESS SELECT

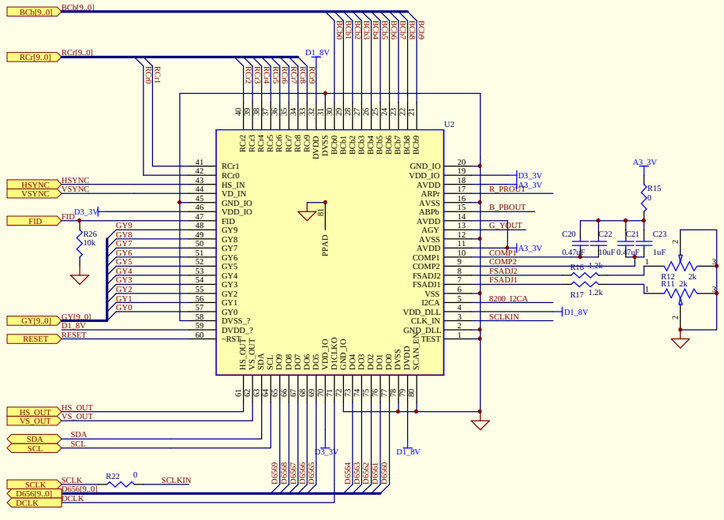
1-2 0x42 - Default

2-3 0x40



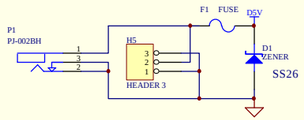






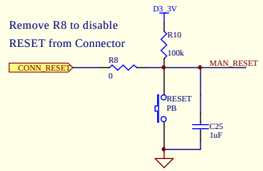
Title	THS8200 EVM REV1.1 - MAIN	
Size: C	Number	Revision: REV 1.1
Date: 27-Sep-2005	Sheet 5 of 6	
File: X:\EVM Design Files\TVP7000_EVM_MODULE_REV1.0\TVP7000EVM_RTM\THS8200EVM_MODULE_REV1_2\THS8200EVM_MODULE_REV1_2.ddb		

OPTIONAL 5V, 3.0A DC INPUT
MAIN SUPPLY FROM CONNECTOR



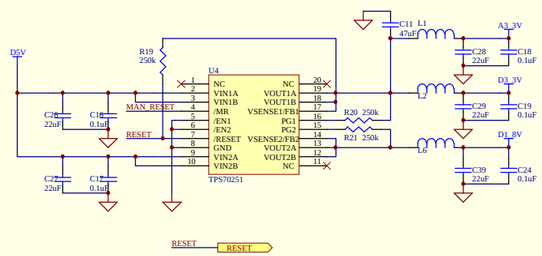
RESET ON POWER UP

Remove R8 to disable
RESET from Connector

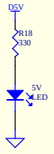


THS8200 POWER SUPPLY

VOUT1 IS 3.3V 500mA
VOUT2 IS 1.8V 250mA



POWER ON LED (+5V)



Title: THS8200 EVM REV1.1 - POWER		
Size: C	Number:	Revision: REV 1.1
Date: 27-Sep-2005	Sheet 6 of 6	
File: X:\EVM Design Files\TVP7000_EVM_MODULE_REV1.0\TVP7000EVM_RTM\THS8200EVM_MODULE_REV1_2\THS8200EVM_MODULE_REV1_2.ddb		

Appendix A. Recommended PLL Settings

Standard	Resolution	Refresh (Hz)	Horizontal (kHz)	Pixel Rate (MHz)	PLL Divider Total pix/line	PLLDIV MSB Reg01h	PLLDIV LSB Reg02h[11:4]	Reg03h	Output Divider Reg04h[0]	VCO Range Reg03h[7:6]	CP Current Reg03h[5:3]
VGA	640x480	60	31.5	25.175	1600(2x)	64h	00h	68h	1	Low (01b)	101b
		72	37.9	31.5	1664(2x)	68h	00h	58h	1	Low (01b)	011b
		75	37.5	31.5	1680(2x)	69h	00h	58h	1	Low (01b)	011b
		85	43.3	36	832	34h	00h	68h	0	Low (01b)	101b
SVGA	800x600	56	35.1	36	1024	40h	00h	68h	0	Low (01b)	101b
		60	37.9	40	1056	42h	00h	68h	0	Low (01b)	101b
		72	48.1	50	1040	41h	00h	68h	0	Low (01b)	101b
		75	46.9	49.5	1056	42h	00h	68h	0	Low (01b)	101b
		85	53.7	56.25	1048	41h	80h	68h	0	Low (01b)	101b
XGA	1024x768	60	48.4	65	1344	54h	00h	58h	0	Low (01b)	011b
		70	56.5	75	1328	53h	00h	A8h	0	Med (10b)	101b
		75	60	78.75	1312	52h	00h	A8h	0	Med (10b)	101b
		85	68.7	94.5	1376	56h	00h	A8h	0	Med (10b)	101b
SXGA	1280x1024	60	64	108	1688	69h	80h	A8h	0	Med (10b)	101b
		75	80	135	1688	69h	80h	98h	0	Med (10b)	011b
Video	720x480p	60	31.468	27	1716(2x)	6Bh	40h	68h	1	Low (01b)	101b
	720x576p	50	31.25	27	1728(2x)	6Ch	00h	68h	1	Low (01b)	101b
	1280x720p	60	45	74.25	1650	67h	20h	A8h	0	Med (10b)	101b
	1280x720p	50	37.5	74.25	1980	7Bh	C0h	A8h	0	Med (10b)	101b
	1920x1080i	60	33.75	74.25	2200	89h	80h	A8h	0	Med (10b)	101b
	1920x1080i	50	28.125	74.25	2640	A5h	00h	A8h	0	Med (10b)	101b
	1920x1080p	60	67.5	148.5	2200	89h	80h	D8h	0	High (11b)	011b
	1920x1080p	50	56.25	148.5	2640	A5h	00h	D8h	0	High (11b)	011b

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