User's Guide
SLLU286–November 2017

TDP142 Evaluation Module

This document describes how to use the TDP142 evaluation module (EVM). Throughout this user's guide, the abbreviation EVM and the term evaluation module are synonymous with the TDP142EVM, unless otherwise noted.

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1 TDP142EVM Overview

The TDP142EVM is designed to evaluate the TDP142 device at a system level using a standard DisplayPort™ (DP) connection. The EVM provides standard DP connectors which can be used to connect to a DisplayPort source or sink systems, to evaluate the TDP142 settings. PCB design files can be provided, upon request, to aid in PCB design with the TDP142 device. The layout files can be used as a guideline to implement the device, with illustrations of the routing and placement rules. The EVM design may include test components for evaluation purposes, but not applicable for production.

Figure 1 shows the EVM block diagram.

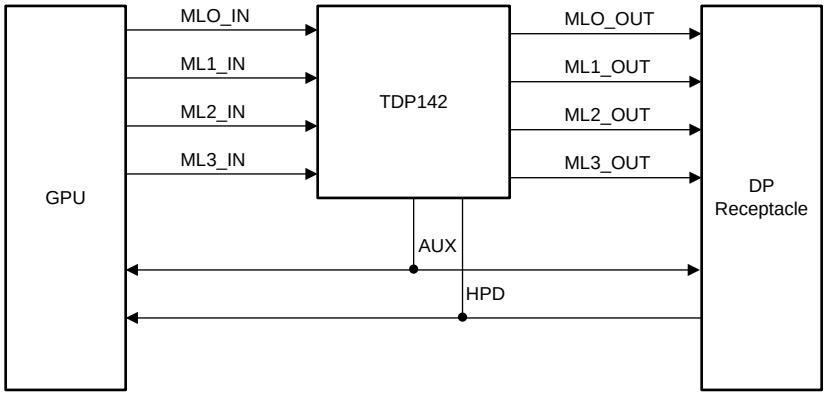

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Figure 1. TDP142 Block Diagram

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The EVM can be configured to operate in either GPIO or I^2C mode (see Figure 2). In GPIO mode, test headers are provided to configure the input pins for the equalizer (EQ) gain and Voltage Out Differenial (VOD) settings. In I^2C mode, the I^2C can be accessed through a 2 × 5 test header pinned out to match the Total Phase™ Aardvark™ I2C programming module.

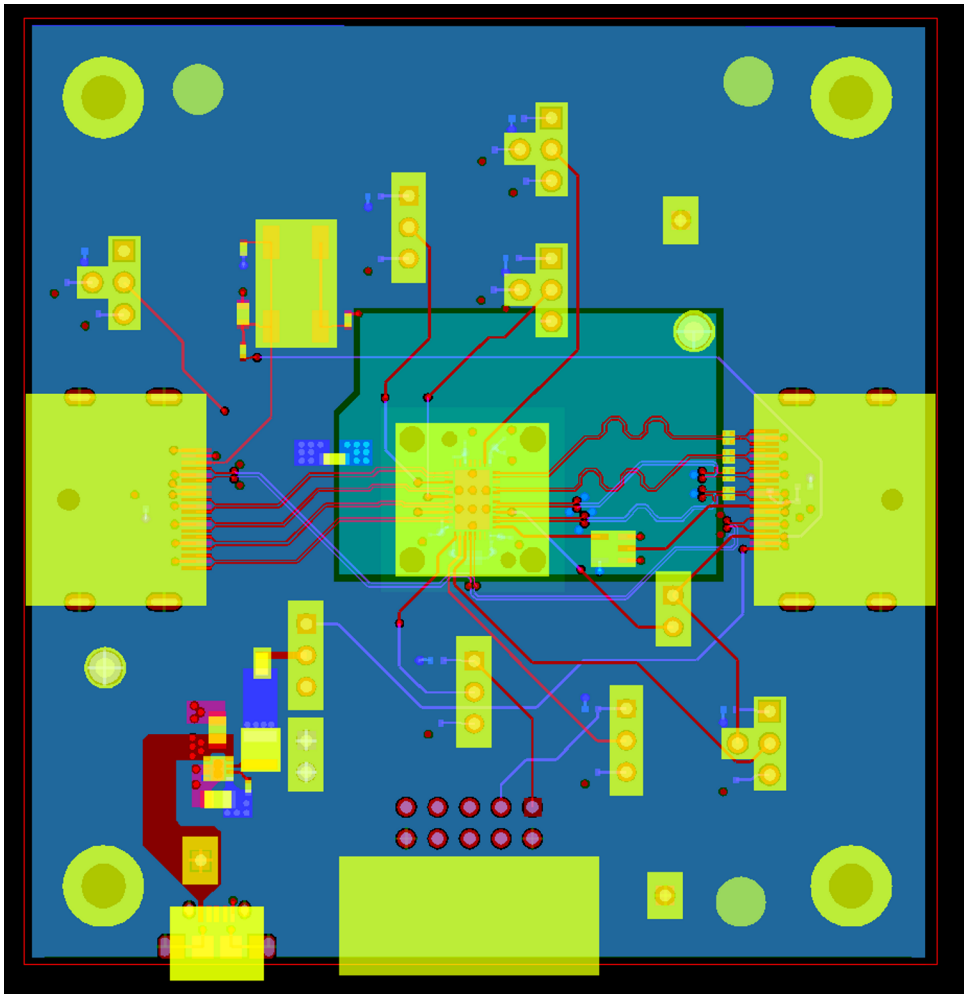

Figure 2. TDP142EVM Board

2 TDP142EVM Features

2.1 Power

2.1.1 Board Power

The EVM operates using the 5-V VBUS from the Micro AB USB connection (J13). If users do not wish to use a USB external power supply, either 5 V or 3.3 V can be provided using the test headers onboard: 5 V through TP3, 3.3 V through J11. It is important that only one power source is used, do not connect multiple sources at the same time.

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2.1.2 DP Power

The DP power (PWR) can be passed through from the DP input connected through J9, or tied directly to 3P3V on the board. See Table 1 for DP PWR configuration through J12.

Table 1. Board Power Configuration

Reference Number	Name	Default Configuration	Description
J11	3P3V	Open	Provided in case power will be provided externally
J12	DP_PWR	Pin 2 - 3	Configures the source for DP_PWR. Default is to use the DP_PWR input from J9.

2.2 Connectors

The EVM has two standard DisplayPort connectors: J9 and J10. J9 is intended to be connected to a DP source, and J10 to a DP sink. Figure 3 and Figure 4 show example configurations. The connection between the DP Source and DP Branch/Dock does not have to be through a DisplayPort cable, it can be through other cable connections such as USB Type-C™.

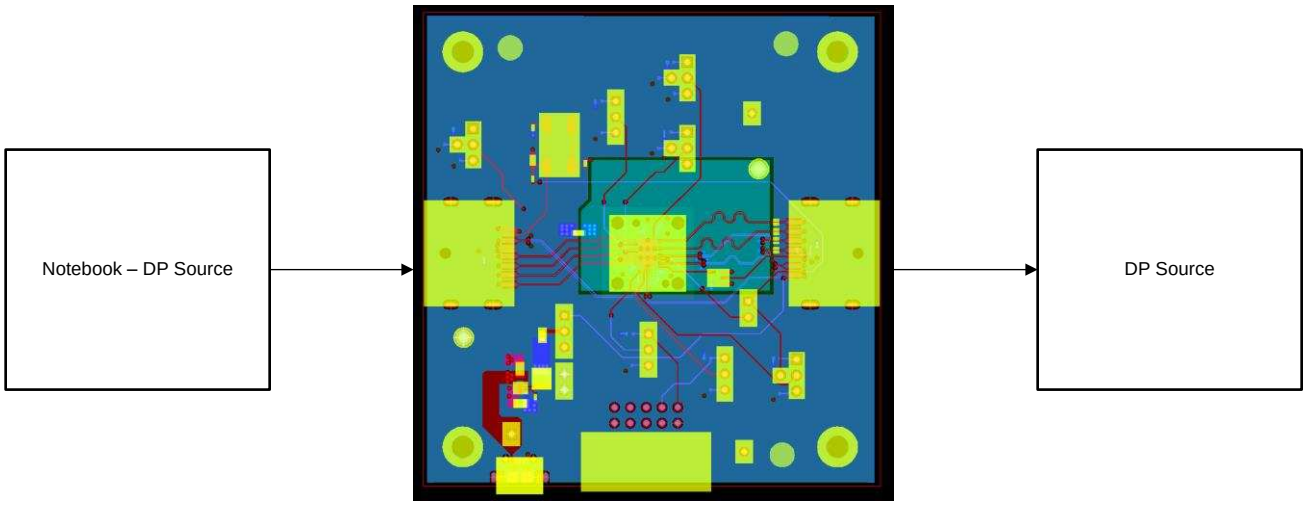

Figure 3. TDP142EVM Between Notebook and DP Monitor

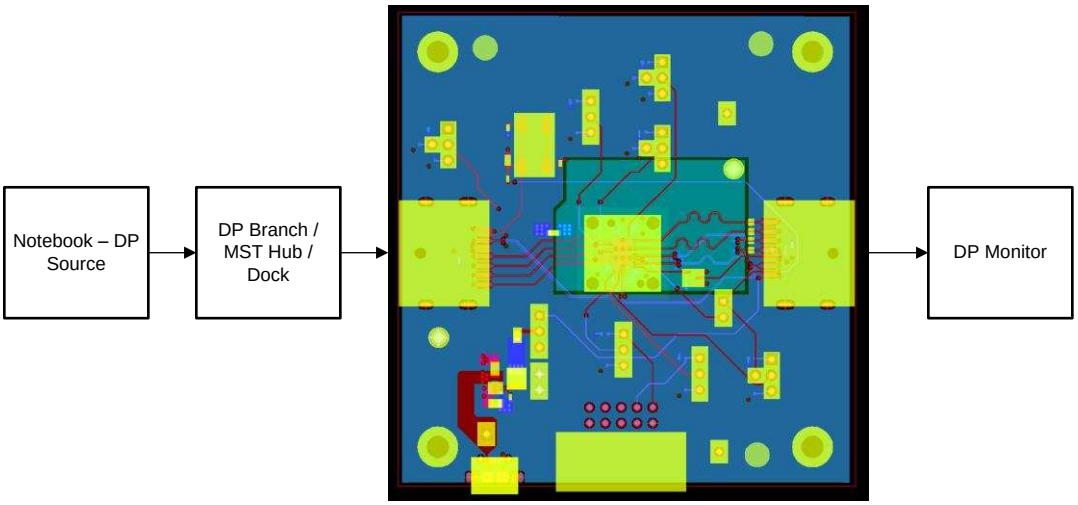

Figure 4. TDP142 Between Dock and DP Monitor

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2.3 EQ and Gain Test Configuration Headers

The TDP142 settings are configurable through the test configuration headers provided on the board. Table 2 summarizes the configuration settings. See the TDP142 data sheet for the details on the device operation in different settings.

Table 2. EQ and Gain Configuration

Reference Number	Signal Name	Default Configuration	Description
J1	DRV_PK#	Low – enable DRV	Disable and enable driver peaking
J2	I2C_EN	Open – GPIO mode	Configures device to operate in I^2C or GPIO mode
J3	VOD	High – high VOD	Configures VOD mode – high or low
J4	EQ0	Configurable	See data sheet for details
J5	EQ1	Configurable	See data sheet for details
J6	EQ_MODE	Open – Cable mode	Configures device to operate in Cable or Trace mode
J7	GAIN	Low or open – See data sheet	Work with EQ0 and EQ1 to set total EQ gain

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