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- Model t1 damaged before next step by shorting Remote_sense+ to ground causing Vout to rise and damage output caps, put aside. Following tests done with model t2

- Testing with GUI current limit/ start up/ margining: Pages 10-11
- Load step and dump with model t2: Page 12

Thermal image:

- PMP6997 TPS40400 & CSD86350 495kHz sw
  - 12.03Vin 2.33Ain 1.206Vout 20.0A 50nsec delay
  - CSD86350 hottest at 62; snubber R at 60; controller at 52; choke top at 46.4; choke at PCB 51; ambient ~22 degrees Celsius

3.91 Watts total on board loss
PMP-6997 1.2V 20A off 12Vin Test Report (TPS40400 & CSD86350) Texas Instruments

60.7 °C

25.2

Qq
PMP6997 TPS40400 & CSD86350 295kHz sw
12.03Vin 2.30Ain 1.206Vout 20.0A 50nsec delay
CSD86350 hottest at 57; snubber R at 54.4; controller at 47; choke top at 43; choke at PCB 48; ambient ~22 degrees Celsius

3.55 Watts total on board loss
Major waveform: R21 to slow high side turn on of CSD86350Q5D set to 10 ohms, same as in PMP5783. Goal is to have max Vds well below 25V rating at 12Vin and full load: The GUI allows either a 25nsec or 50nsec delay between high and low side switches. My testing found that using the longer 50nsec delay reduced max Vds from 25V to 22V at full load with about a 5mA cost in input current at the 495kHz operation and less than that at 295kHz operation. Hence, the 50nsec delay was used in all testing (including thermal above and efficiency below) as it gives a good margin of safety for the FETs.
PMP6997 1.2V 20A off 12Vin Test Report (TPS40400 & CSD86350) Texas Instruments

Maximum V = 21.56 V
Min V = 24.38 V
Max Rise Time = 1.8 ns
Max Fall Time = 2.9 ns

Note high to low delay of 40ns
And low to high delay of 40ns
Major waveforms: 295kHz operation with 25nsec and 50nsec delays:

- 295kHz operation
- 25nsec delay
- 50nsec delay
- 2.4 ns rise
- 3.5 ns fall
- Max Vds of 25.3V vs. 25V rating
- Note high to low delay of 30-40nsec
- And low to high delay of ~10nsec
Again, based upon these waveforms the 50nsec setting is being used.

In model t2: Tested with R21=6.8 ohms (vs. 10 ohms in model t1) and also got ~20Vds max when delay set at 50nsec. Hence, either 6.8 or 10 ohms can be used with **6.8 ohms preferred for R21**.
Output ripple at ceramics: First 495kHz operation:

Then 295kHz operation:
295kHz operation

Output Ripple at ceramics

20MHz BW and 1x probe
16mV peak to peak

PMP6997 TPS40400 12Vin 1.2Vout 20A

max(1) 11.86mW
pk-pk(1) 16.88mW 470uH 2x330uF +4x100uF
rise(1) 962.4 ns
fall(1) 4.5640 μs

10 μV
5 μV AC
2.2 V DC
3.1 V DC
4.10 μV 4Ω

1 DC 7.2mW 250 Ms/s

STOPPED
Output ripple: 295kHz free running, but sync’ed to 485kHz with on board clock:

With model t2 similar ripple was confirmed in all 3 above cases.
Bode Plot:

Load dynamics: First step load response using on board dynamic load:
And now Load Dump response:
Peak overshoot varies from 30 to 40mV apparently depending upon when in switching cycle the load is dumped. Shown above is the worst case. The step load response does not show this added 10mV. Load dump is faster than step load with load dumping in 50nsec vs. 150nsec for load to be applied.
### Regulation / efficiency at 1.2V setting, 12Vin and 495kHz switching model t1:

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<tr>
<th>Vin Volts</th>
<th>Iin A</th>
<th>Vout Volts</th>
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<th>% Efficiency</th>
<th>Losses in W</th>
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### Qq

### Regulation / efficiency at 1.2V setting, 12Vin and 295kHz switching model t1:

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<th>Vout Volts</th>
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<th>% Efficiency</th>
<th>Losses in W</th>
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With model t2 got 12.03Vin 2.31Ain 1.208Vout 20.0aout for 288kHz operation: This gives 0.25% lower efficiency. At 500kHz setting got 2.34Ain, also for about 0.25% lower efficiency. However, step resolution of input current is 0.43%.

Comparison note vs. PMP6932:
Tested with Vishay IHLP5050CE-01 470nHy value with max height of 3.5mm vs. 5mm height for the part used in PMP6932: Nominal on resistance is 1.6mOhms vs 1.1mOhms. PMP6932 was tested with Delta (Susumu) PCMC135T-R47MF which is 13.8mm by 12.8mm by 5mm max with nominal ESR of 1.1mOhms with thermal 38A rating and Saturation 65A rating. This part is intended to be a replacement for Vishay IHLP5050EZ-01 of same inductance. Based upon Vishay loss calculator (295kHz operation), going to the higher profile part would decrease choke losses from 1235mW to 944mW at 20A load and help efficiency by about 1%.
Current sense gain set at 2.00mV/A for best fit at 20A in 0.47uHy output choke:
See note on previous page: At full 20.0A load on model t2 got 20.2A on GUI
With warning threshold set at 22A got warning displayed at 24.8A on GUI and 24A as measured at load.
With overload shutdown threshold set at 25A got shutdown at 28A on GUI and 27A as measured at load.

PMP6997_TPS40400_Script.xml has all settings used. Overcurrent set to shut down and recover automatically. Verified in Test.

Vout at nominal and at 10% margin low and 10% margin high 8-10mV above programmed targets on model t2. 1087mV, 1208mV and 1329mV vs. 1079mV, 1200mV and 1319mV targets.

Vout set to come on when “Control” goes high:
PMP697 model t2: 288kHz setting
12.0Vin 1.208Vout at 10A after Enable
GUI rise time set to 2.6msec upon
Control pin going high
Actual rise time is 3.0msec with no
overshoot
Model t2: Margin high to margin low:

Margin low to margin high:
Load step and load dump on model 12: 1.208V out 288kHz setting 45kHz loop
7.5A step or dump in ~100nsec:

PMP6997: TPS40400 12Vin 288kHz
10A load: 1.20V out nom. margin hi
target 1.32V, margin low target 1.08V
Shown is transition from margin low to
margin high in ~700usec linearly with
no overshoot.
Per DVM: error ~10mV above targets
10mV/s
Load dump: Now also in ~100nsec vs. 50nsec in Model t1 above
PMF6997 load dump & drain 12Vin with
fixed load of 10A & dynamic load of
7.5A dumped in 100msec.  Model 12
258kHz operation with 38.5kHz Jig
Peak overshoot 34mV vs. 43mV on
model 11.  Here get "worst case",
load to inherent Zt + 50ohms from
10ohms to 499 ohms...
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