PMP6672 RevB Test Results

1 Introduction

TPS23754EVM-420 is an IEEE802.3at, Type 2 compliant powered device. Output power is 5V at 5A from either an adapter input (21.6 – 57VDC) or power over ethernet. Steps were taken to improve the efficiency of the catalog EVM. In general, the efficiency gain was on the order of 3-4% with the EVM design changes listed below.

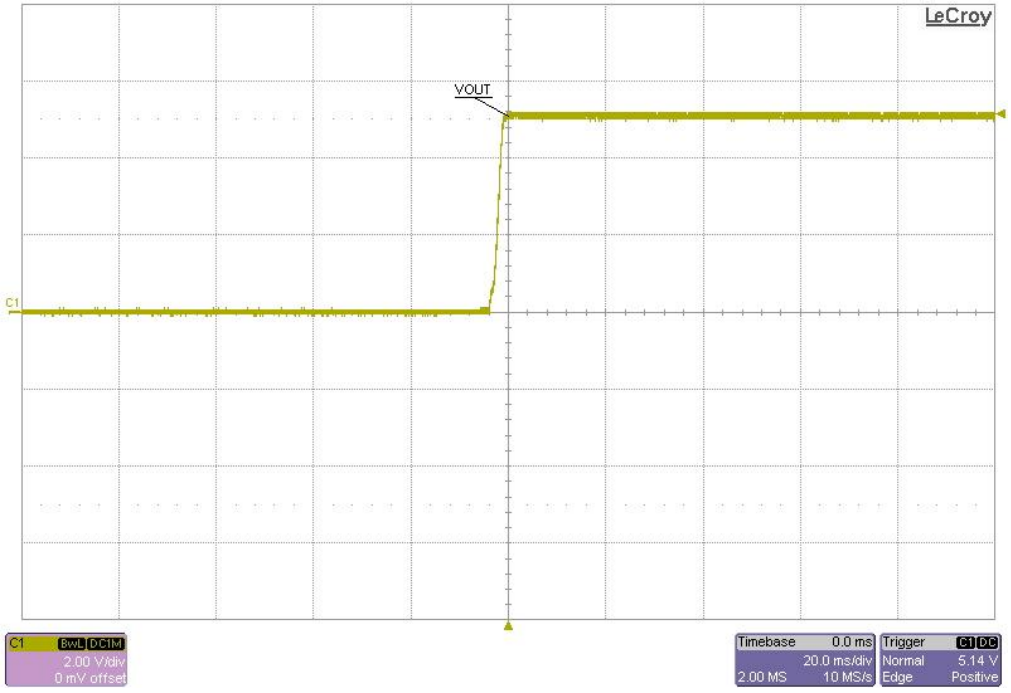
Component	Function	New Value
R17	Dead time resistor	22.1kohm
R12	Primary clamp snubber resistor	39.2kohm, 0.25W, 1206 package
D15	Primary clamp snubber diode	MURS120
R21	Slope compensation resistor	332ohm
D100 (new)	Primary FET gate drive speed up diode	1N4148
R100 (new)	Voltage feed forward resistor	121kohm
R24	Compensation	1.5kohm
C31	Compensation	6.8nF
T2	Flyback transformer	JA4456-DL
Q1	Synchronous rectifier FET	SiR422DP

2 Improvement summary

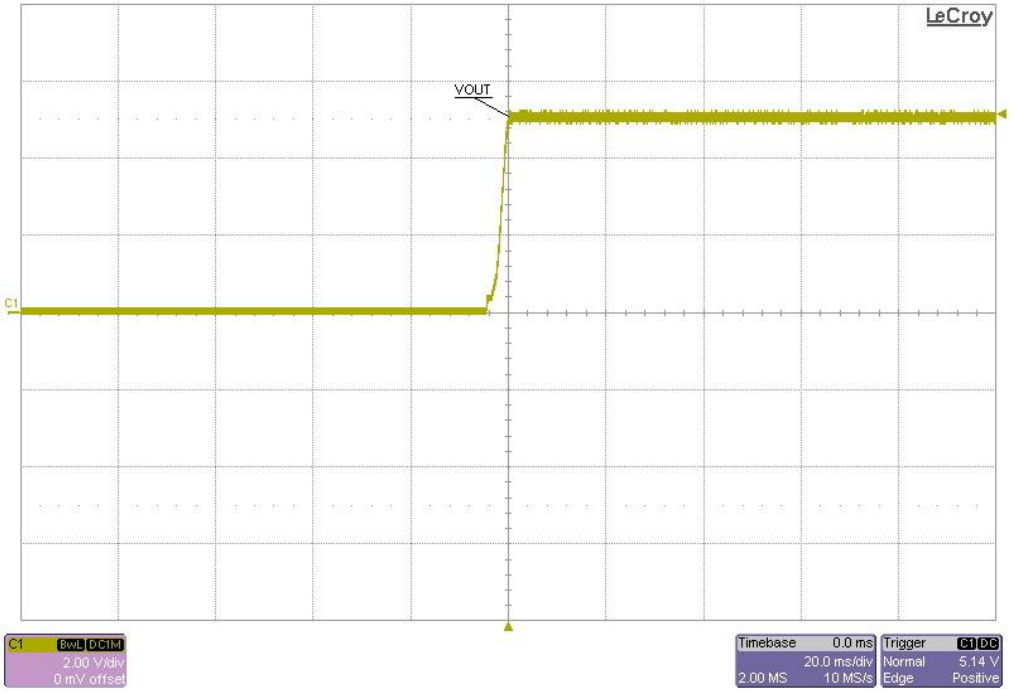
- New Flyback Transformer Design
  - Better selection of magnetizing inductance for CCM operation
  - New winding strategy to reduce copper losses
  - Uses same core and bobbin size and footprint
- RCD clamp improvements
- Diode used for faster primary FET turn off
- New dead time resistor value for optimum efficiency at full load and acceptable efficiency at no load.
- Use of feed forward resistor for better control of peak current and voltage at higher input voltage.
- Other updates: Compensation, improved slope comp, 40-V Sync FET for low drain-source stress.
- Other Benefits
  - Lower primary MOSFET Peak drain-source voltage during overloads
  - Much better current limit control

3 Start up

The scope plot below shows the 5V output voltage startup waveform after the application of 48Vdc at J2 (PoE). The output was loaded to 0A.

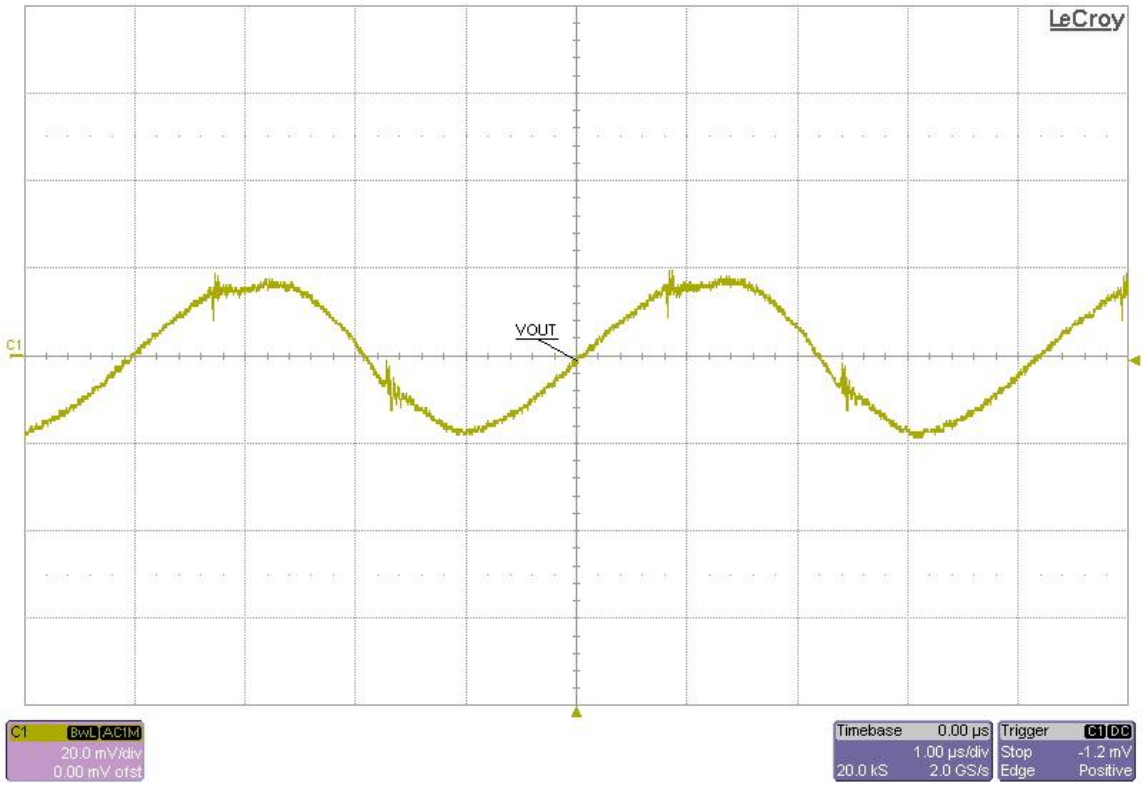


The scope plot below shows the 5V output voltage startup waveform after the application of 48Vdc at J2 (PoE). The output was loaded to 5.0A.



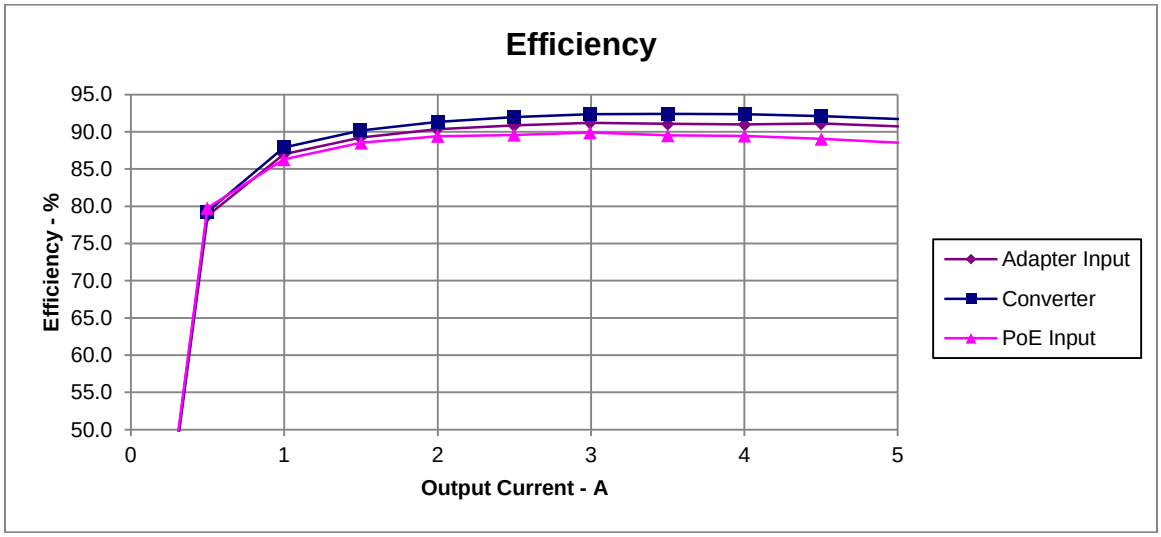
4 Output Ripple Voltage

The 5V output ripple voltage is shown in the scope plot below (J11 connector). The scope plot was taken with the output loaded to 5.0A.Vin = 48Vdc at J2.



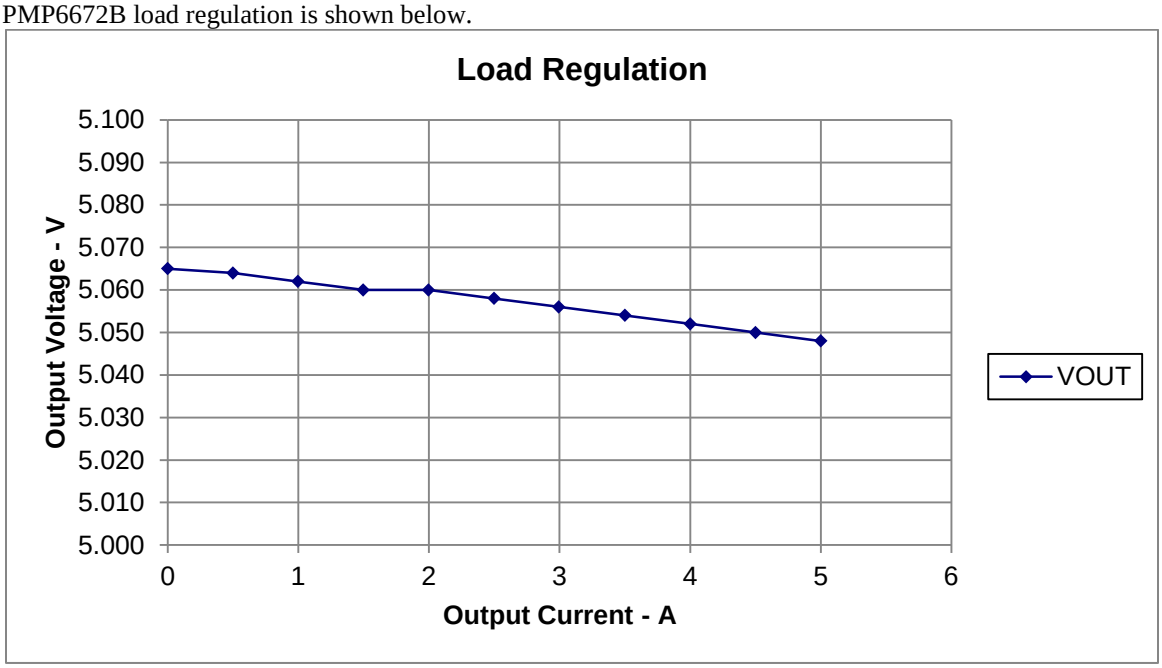
5 Efficiency

PMP6672B efficiency is shown below. POE Input shows PoE+ end-end efficiency with 48Vin (power input at J2). Converter is the DC-DC converter only efficiency. Adapter is adapter input efficiency at 48Vin (power input at J3 connector)



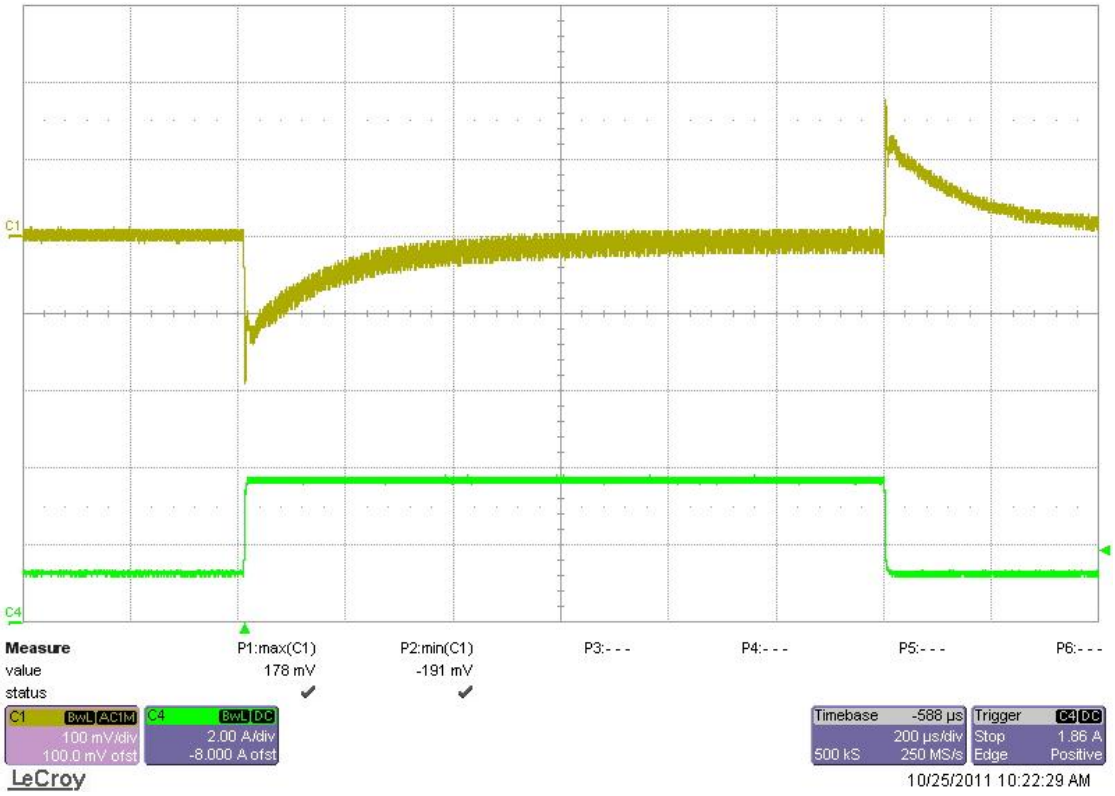
6 Load Regulation

PMP6672B load regulation is shown below.



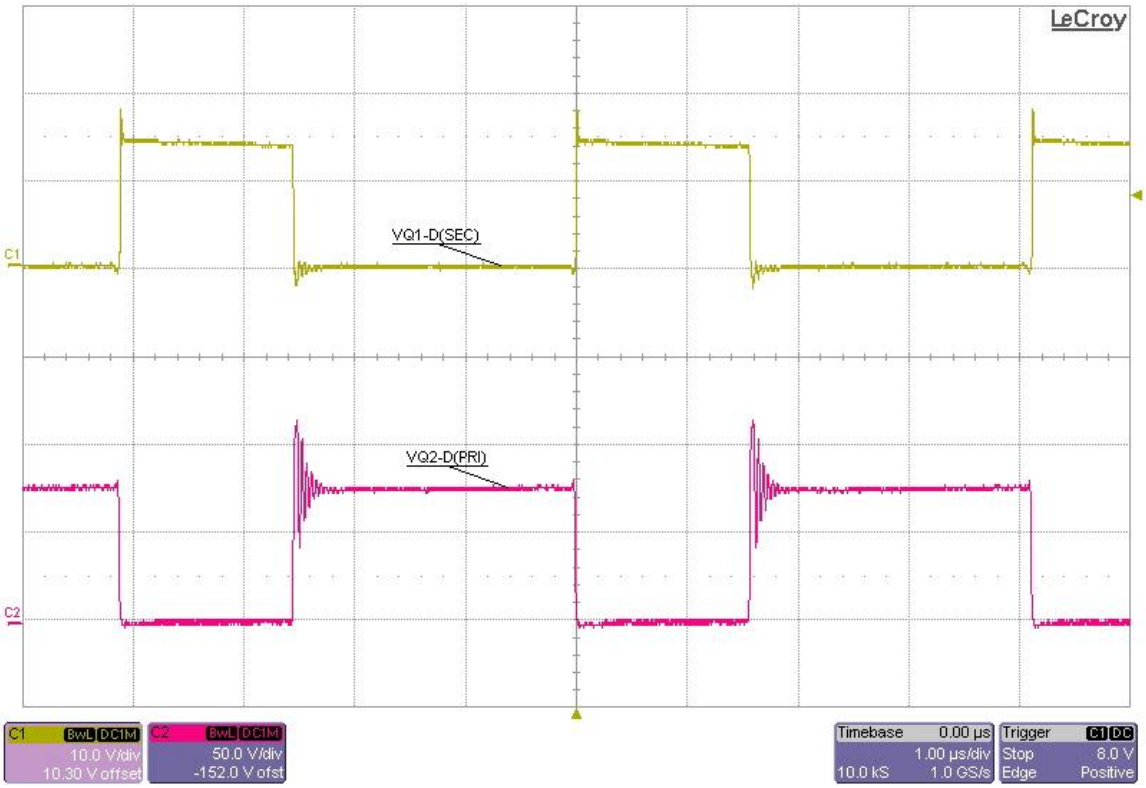
7 Load Transients

The scope plot below shows the 5V output voltage (at J11) when the load current is pulsed between 1.0A and 4.0A. Vin = 48Vdc at J2



8 Switch Node Waveforms

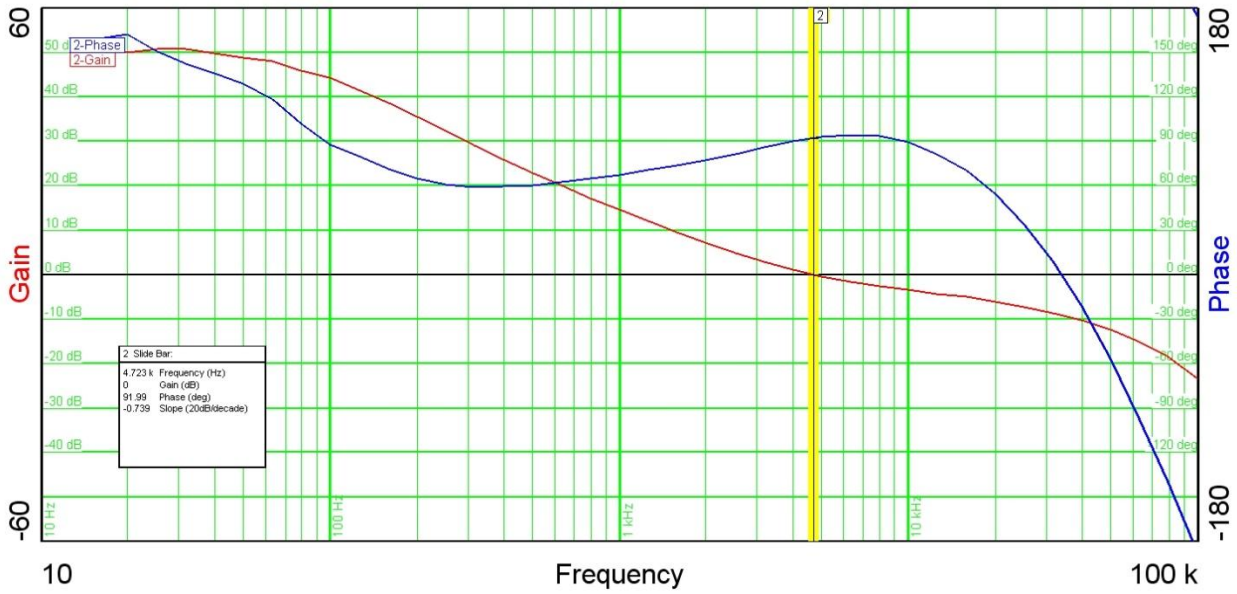
The scope plots below shows the waveforms on the drain of the secondary side FET (CH1) and primary side FET (CH2). The output is loaded at 5.0A. Vin = 48Vdc at J2



9 Control Loop Gain / Stability

The table below shows the loop gain and phase margin. The output was loaded to 5.0A.

Input voltage	48VDC	
Gain/Phase	Crossover	Phase Margin
PMP6672B (5V)	4.723kHz	92°



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