Application Report
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200-VA HF Inverter Design Based on UCD8220 and MSP430G2330 for Automotive Application

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ABSTRACT

This document presents low-cost, small size, robust 200-VA DC to AC inverter based on TI's MSP430G2553 and UCD8220-digitally managed push-pull controller. In this design, UCD8220 is used for a boost stage to get 250-V DC from a 12-V battery. The MSP430G2553 acts as a host controller and provides a 100-kHz clock to UCD8220 and drives for output DC-AC bridge. UCD8220 internally generates push-pull drives for MOSFETs. Current limit is set through a simple resistor divider at the ISET pin. In the case of an overcurrent limit, the UCD8220 sets the current flag (CF) pin high and the device is turned off by the host controller if the current limit exceeds a certain number of cycles. Low-Rdson MOSFETs help keep conduction losses within limit. This inverter has a peak efficiency of 90%. This design has natural cooling and does not require a fan for cooling. The features of this design include ignition sensing, engine-on sensing, reverse battery protection and overcurrent latch. Target applications of this design are for car inverters and small-segment inverters for commercial applications.

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TrueDrive is a trademark of Texas Instruments.

1 Design Parameters

The design parameters for this design are presented in Table 1.

Table 1. Design Parameters

Parameter	Minimum	Typical	Maximum
Vin (V)	10.5	13.2	14.5
Vout RMS (V)	230	240	250
Iout (A)	0	1	
Efficiency (%)	84	86	88

2 Device Selection

2.1 Push-Pull Converter (UCD8220)

The push-pull stage is designed to boost 12-V battery voltage to a stable 250-V DC bus. TI offers a wide range of analog as well as digital push-pull controllers. For this application, the UCD8220 digitally managed push-pull controller is considered because of the following advantages over traditional analog controllers:

- Dual 4-A high current drive (TrueDrive™)
- Programmable current limit
- Digital overcurrent flag indication to host controller
- Internal programmable slope compensation

2.2 Inverter Stage (MSP430G2330-Q1)

The inverter stage is a traditional H-Bridge driven by the MSP430 through opto-couples at 50 Hz, chopping the 250-V bus to get a smooth modified square-wave output. The MSP430 series has features such as ultra-low quiescent current and low cost.

3 Design Stage

3.1 200-W Push-Pull Stage

The push-pull topology is basically a forward converter with two primaries. The primary switches alternately power their respective windings. Refer to Figure 1 for a generalized representation of push-pull topology.

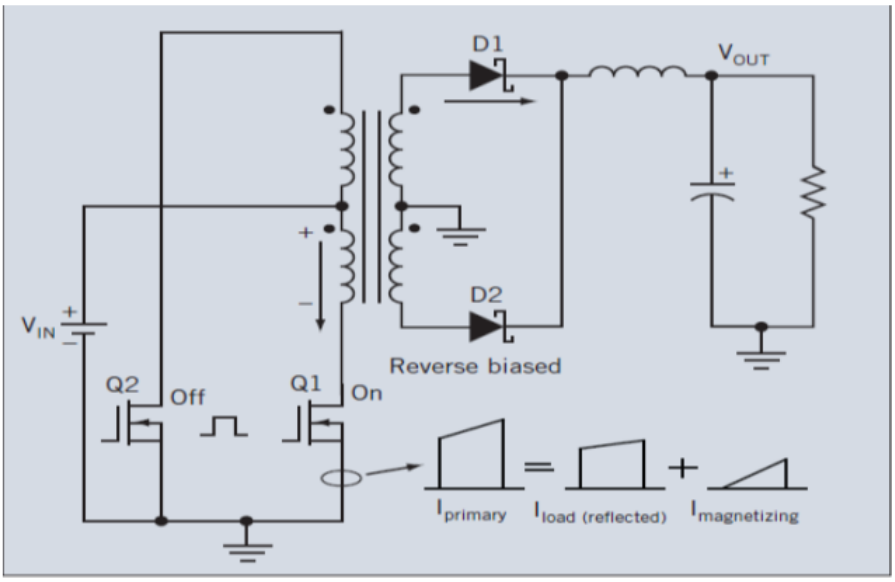


Figure 1. Push-Pull Topology

The schematic in Figure 1 shows that when Q1 is conducting, current flows through D1. When Q2 is conducting, current flows through D2 on the secondary side. As the secondary side conducts in both cycles, output sees twice the switching frequency of either Q1 or Q2.

The push-pull topology is selected for this stage due to its better core utilization. One of the disadvantages with this topology is voltage stress on MOSFET compared to other topologies. When Q1 is on, Vin appears across ½ of the primary winding. Vin will also appear across the other half of the primary that connects to the drain of Q2. That forces the drain of Q2 to 2 × Vin.

In current design, this stage is responsible for generating a stable 250-V DC bus from a 12-V battery input. UCD8220 is digitally managed analog the PWM controller, configured with push-pull logic. The UCD8220 includes circuitry and features to ease implementing converter managed by the microcontroller. Programming and monitoring power-supply parameters such as switching frequency, maximum duty cycle, current limit, shutdown, and input Under Voltage Lockout (UVLO) and Over Voltage Lockout (OVLO) is possible.[1]

The MSP430 provides a constant-frequency, fixed duty cycle clock (100 kHz at 80% duty cycle) to UCD8220. UCD8220 internally generates separate push-pull drives for the MOSFETs.

The maximum peak-current threshold is set by a resistor divider on the ISET pin. This allows monitoring for OC fault on a cycle-by-cycle basis. In case of overcurrent, the UCD8220 sets the current limit flag high which can be read by microcontroller and converter and can be put in shutdown state if the OC fault continues for a certain number of cycles, based on designer's preference.

Power MOSFETs play a critical role along with magnetic, as far as power dissipation is considered. For this application, considering high peak currents at the input side, TI's low-Rdson and low-Qgs MOSFET, CSD18532, is selected to keep switching as well as conduction losses in control. Below is the design example which explains key parameter calculations for the push-pull stage.

3.2 Push-Pull Design Parameters

Vin (min) = 9 V, Vin (nominal) = 12 V, Vin (max) = 15 V

Vout = 240 V, Iout = 0.85 A, Efficiency (η): 90%, Switching Frequency (Fs): 100 kHz (T = 10 µs)

Dmax = 0.38, Ton = Dmax × T = 3.5 µs

Start the push-pull topology using the following steps:

3.2.1 Turns Ratio

Push-pull topology is designed keeping in mind the output voltage duty cycle and turns ratio required to achieve the required output voltage.

(a) Dmax is usually chosen less than 50% to start, this to ensure accommodation is made for the losses both conduction and switching and the voltage drop across the Rds_{on} of the MOSFET. The amount of voltage transferred to secondary is dependent on the Volts seen by the primary of the transformer, the transformer ratio. A Dmax of 0.38 is chosen for this particular application.

(b) The turns ratio is given by Equation 1

$$Nsp = \frac{Ns}{Np} = \frac{\frac{Vout}{2 \times Dmax} + 2 \times Vdiode}{Vin(min) - RdsonDrop - RsenseDrop} \quad (1)$$

Where Ns is secondary turns, Np is primary turns, Vout is output voltage, Vin (min) is minimum input voltage, Dmax is maximum duty cycle at Vin (min), and Vdiode is the diode drop at the output. Since a full-bridge rectifier is used at the secondary side to save the winding space in the transformer, the drop is multiplied by a factor of 2, however, if the center-tapped secondary is used, a single diode drop should be considered while designing.

RdsonDrop and RsenseDrop are defined in Equation 2.

$$RdsonDrop = Rdson \times Iaverage(at\ Vin\ min) = Rdson \times \frac{Vout \times Iout}{\eta Vin(min)} \quad (2)$$

Where Rdson is the on resistance of the MOSFET used.

Similarly, calculate for RsenseDrop with Equation 3:

$$RsenseDrop = Rsense \times \frac{Vout \times Iout}{\eta Vin(min)} \quad (3)$$

Where Rsense is the sense element resistance.

It is evident that the choice of the turns ratio is from start dependent on the different elements used in the push-pull topology, this results in a few iterations to reach to optimum turns ratio.

A MOSFET of Rdson = 0.008 Ω and Rsense = 0.005 Ω was chosen for this design, as is explained later.

Putting various design parameters in Equation 1, Equation 2, and Equation 3, Nsp = 36.88, and 36 turns is chosen. This changes the actual duty cycle as Dmax = 0.389.

When wound on the transformer core, turns form the primary inductance, which is mathematically modeled in parallel to the primary winding. The magnetic inductance is used to estimate, note – just estimate, the leakage inductance of the transformer, which leads to voltage spikes seen at the drain of the both the primary MOSFETs. The transformer chosen is the ETD3411, the core selection is not discussed in this document.

3.2.2 Primary Peak Current

The previous choices dictate the peak primary current through the coil. The peak equivalent of flat-topped primary current is given in Equation 4:

$$Ipft = \frac{Vout \times Iout}{\left(Vin(min) - RdsonDrop - RsenseDrop\right) \times \eta \times 2 \times Dmax}$$

$Dmax$ is chosen to be ~ 0.39

$$Ipft = 36A \tag{4}$$

3.2.3 Primary and Secondary RMS Currents

$$Iprms = Ipft \times \sqrt{Dmax} = 22A \tag{5}$$

$$Isrms = Iout \times \sqrt{Dmax} = 0.52A \tag{6}$$

3.2.4 MOSFET Selection

Unlike other topologies, push-pull MOSFET sees more stress during off time, due to reverse voltage from additional primary winding and reflected voltage from the secondary side. In ideal conditions, peak reverse voltage seen by the MOSFET is twice the input voltage. Care should be taken while selecting the MOSFET voltage because sometimes the leakage spikes add up to twice the Vdd voltage. While designing the transformer the vendors are specified with 2.5% leakage to primary ratio, but it is not always easy to maintain the same. The transistor voltage is specified for 5% leakage in this design. Considering a leakage inductance of 500 nH and a switching frequency of 100 kHz, the snubber for the clamp is designed at 15-V max.

Thus MOSFET rating is given in Equation 7:

$$Vds > \left(2 \times Vinmax + Vclamp\right) \times SafetyFactor \tag{7}$$

The safety factor of 30% was chosen, in this case, resulting in a drain voltage choice of greater than 58 V. TI's 60-V, 100-A MOSFETs **CSD18537KCS** was also used.

3.2.5 Output Inductor

An output inductor is selected so that your converter does not go into discontinuous mode at maximum input voltage and minimum output current. Design for the minimum output current of 70 mA at output. The secondary switch node equation is given in Equation 8:Equation 8:

$$Vswitch\ node = \frac{Vo}{2 \times Dmax} \tag{8}$$

The inductance for the output inductor is calculated using equation Equation 9:

$$Loutput = (Vswitchnode - Vo) \times \frac{Dmin}{Fs \times Imin} \tag{9}$$

In this case it was calculated to be around 2.3 mH.

4 Inverter Stage

The inverter stage is a traditional full-bridge topology. This bridge is driven by a 50-Hz modified square wave from MSP430 via opto-couplers in order to provide isolation. The push-pull transformer also serves the purpose of providing a floating bias supply (VCC_DRA, VCC_DRB) for opto-couplers, thus eliminating the need of a special high-side driver for MOSFETs Q3 and Q4. There is provision for an output LC filter if an inverter output is needed as a quasi-sine wave. One can even think of converting this reference design to pure sine wave by modifying gate drive of the MOSFETs by using a better algorithm at the host controller side.

4.1 Microcontroller Algorithm Features

The algorithm for the controller provides the following features:

1. Overcurrent latch protection and indication
2. Short-circuit protection and indication
3. Soft start for startup inrush current limit
4. USB charging voltage, overcurrent shutdown voltage

The controller algorithm can be modified to make a 200-VA, sine wave inverter. Note that this would require the use of fast opto-couplers or gate drivers to drive inverter MOSFETs.

4.2 Top-Level Flowchart

- DC-DC converter inputs and inverter bridge is managed in infinite ‘while (1)’ loop.
- USB voltage and current loop and other parameter monitoring is done via ADC interrupt.

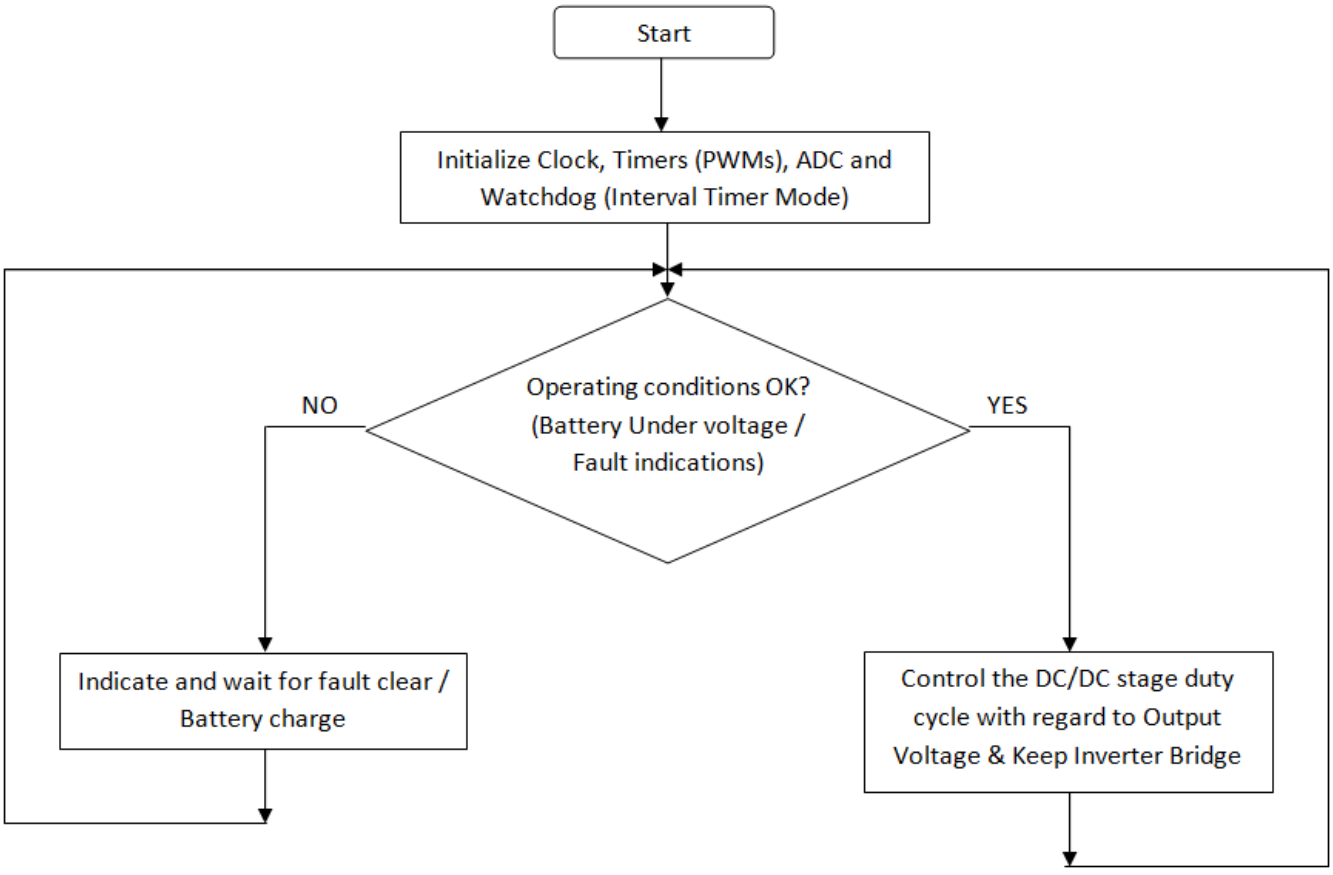


Figure 2. Top-Level Flowchart

The software implementation of the flow chart in Figure 2 can be found in (SLVA578 associated zip file).

5 Experimental Results and Discussion

Scope shots for various nodes on the board were taken to show voltage and current levels to verify and ensure proper operation of the board.

5.1 Soft Start Up and No-Load Operation

The MSP430G2553 provides clocking pulses to UCD8220. Using the calculations given above, the maximum duty cycle of each MOSFET is around 38%, thus the MSP430 provides a clock signal with a duty cycle of 76% and with a frequency of 100 kHz. UCD internally generates push-pull gate drives for the MOSFETS. In order to achieve soft start, the duty cycle of the clock signal is gradually increased from 0% to 76%. At no load, the overall system consumes around 60 mA to 70 mA. Corresponding clock waveform and MOSFET gate-drive waveforms are shown in Figure 3.

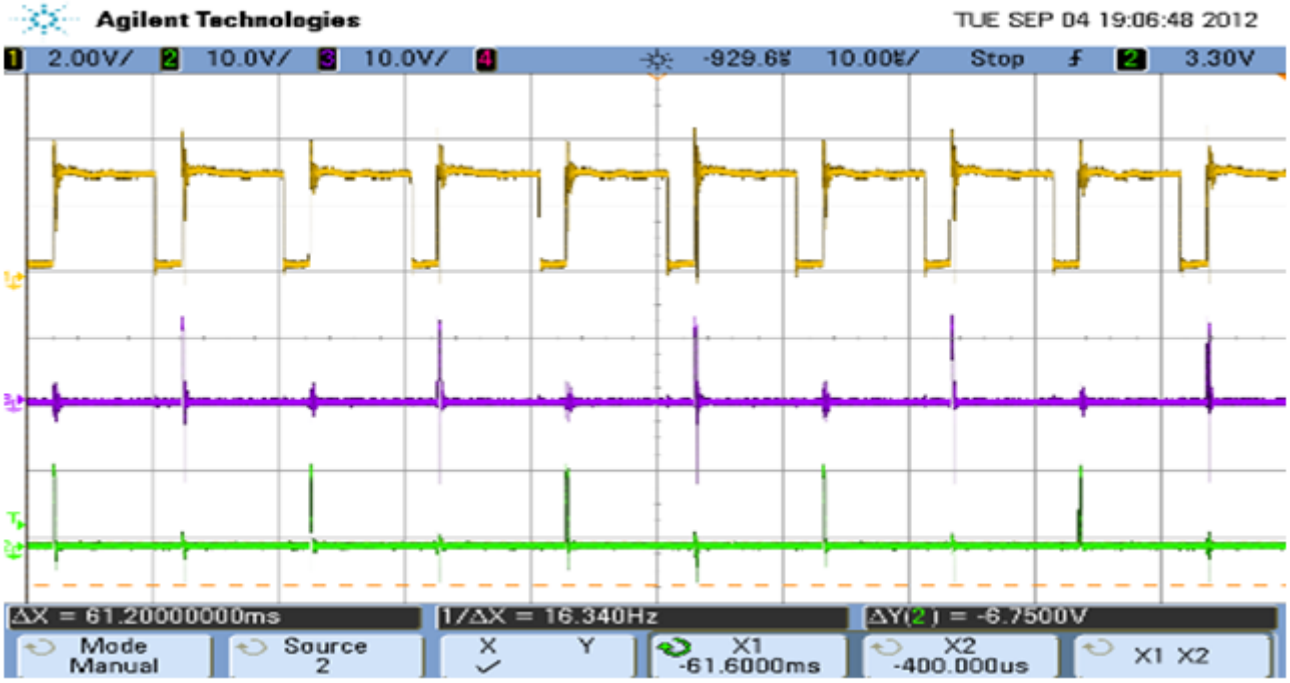


Figure 3. MSP430 Clock Output (Channel1) and Gate Drive for each MOSFET at No Load

5.2 Working Under Active Condition

The following waveforms are captured at the MOSFET gate, drain and current sense during normal working conditions. The inverter was loaded with 150-W load. From the drain waveform, it shows that during off time, MOSFET is subjected to drain voltage which is twice the input voltage, that is, 24 V in this case. For this particular design, the MOSFET drain ringing peak was around 38 V, which is comfortably within the limit of maximum VDS rating (60 V).

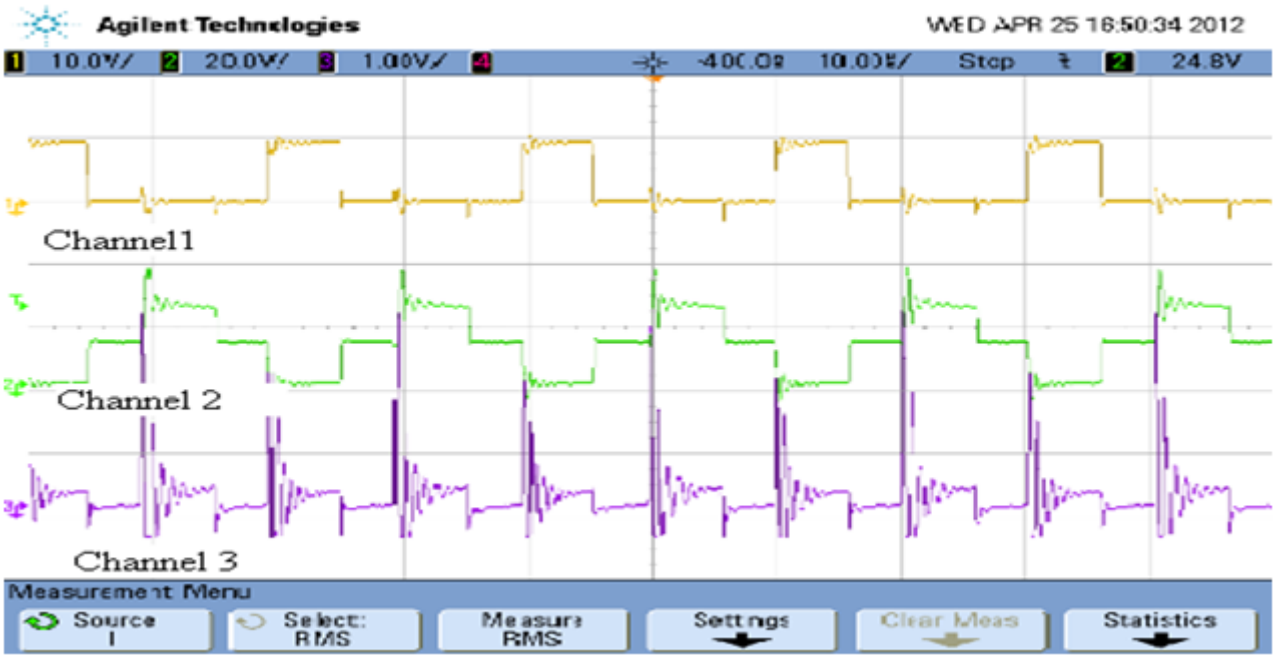


Figure 4. Gate Drive (Channel 1), Drain Voltage (Channel 2), Peak current (Channel 3), Respectively at 150 W

5.3 Efficiency Versus Output Power

The following graph shows the efficiency plot of the inverter with respect to output power. The nature of the output load was a combination of resistive load and inductive load (CFL + Resistive Bulb). The peak efficiency of this design with a mixed-load combination is around 90%. With pure resistive load, peak inverter efficiency approaches close to 92%.

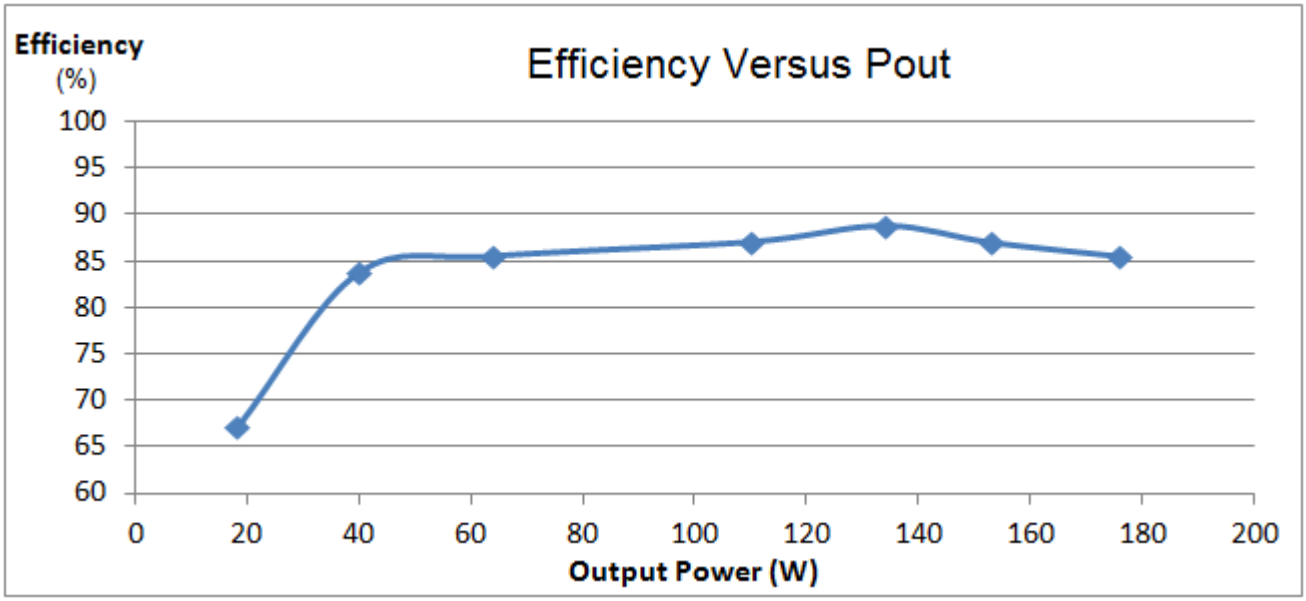
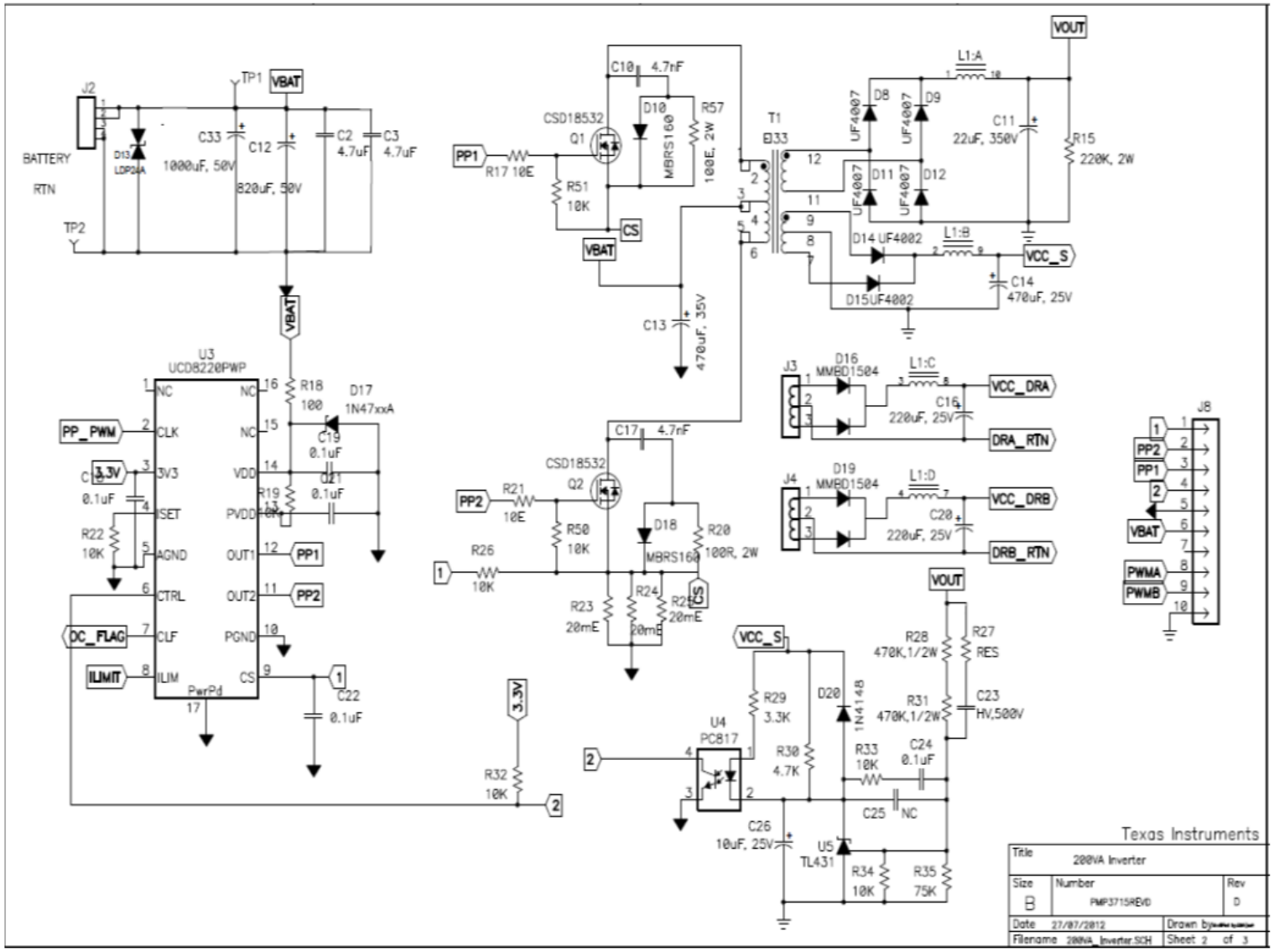


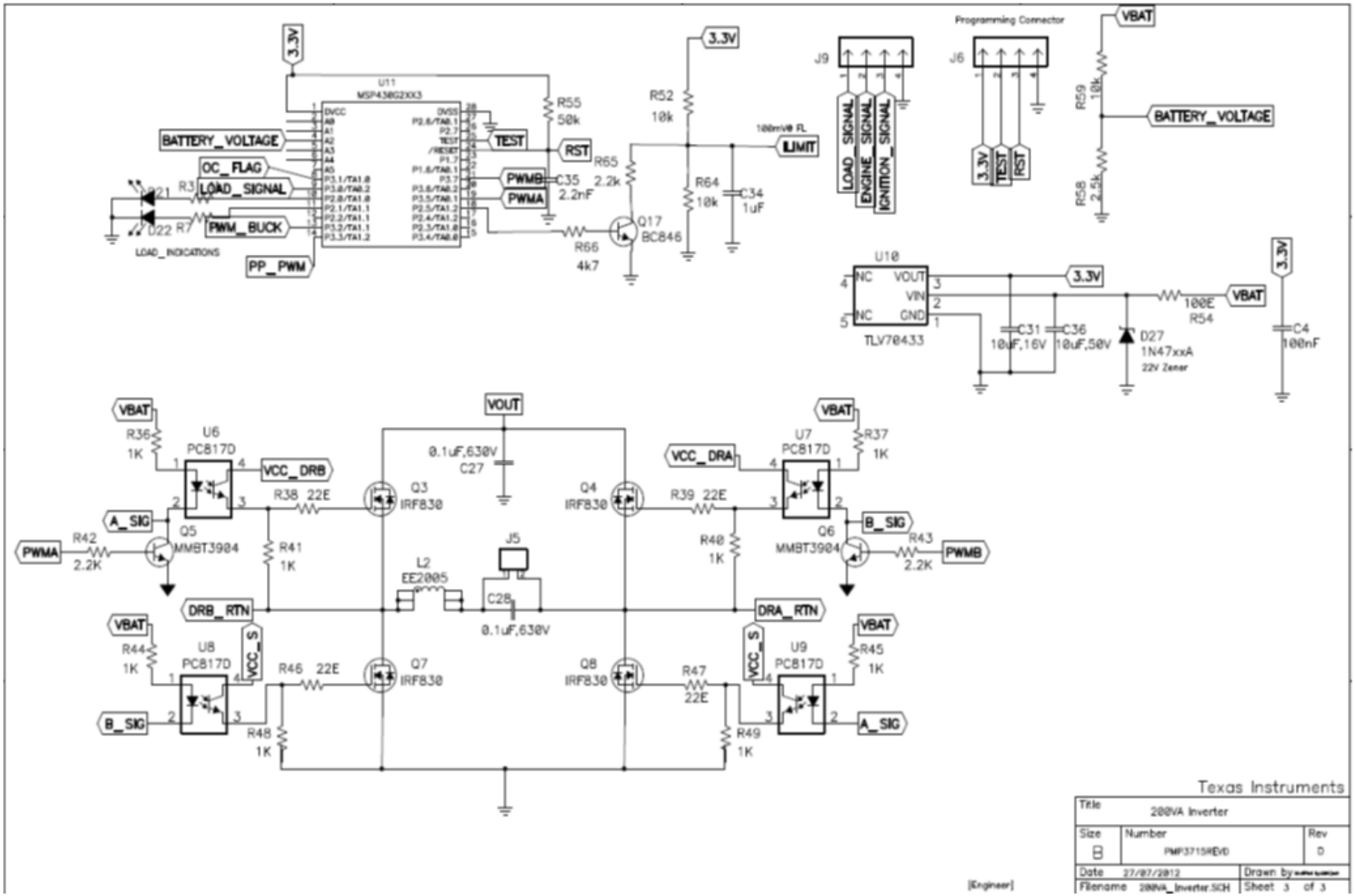
Figure 5. Efficiency Curve with Respect to Output Wattage

6 Schematic

6.1 Push-Pull Stage



6.2 Inverter Stage



7 Bill of Materials

The bill of materials for this design is presented in Table 2.

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number
1	C1	100nF	Capacitor, Ceramic, Low Inductance, 10V, 10%	0603	
2	C10, C17	4.7nF	Capacitor, High Voltage Film Chip, 400V, ±10%	0.150 X 0.300 inch	
1	C11	100uF, 350V	Capacitor, Aluminum, 350VDC, ±20%	13 x 28 mm	
1	C12, C33	1000uF, 50V	Capacitor, Aluminum, 50V, 20%, Low ESR	0.315 inch	
2	C14	470uF, 35V	Capacitor, Aluminum, 35V, 20%, Low ESR	0.394 X 0.630	
5	C16, C20	220uF, 25V	Capacitor, Aluminum, 25V, 20%	0.315 inch	
2	C18, C19, C21, C22, C24	0.1uF	Capacitor, Ceramic, 25V, 15%	0603	
1	C2, C3	4.7uF	Capacitor, 4.7uF,Ceramic, 50V,10%	1210	
1	C23	4.7nF,500V	Capacitor, Leaded, 300 VAC, ±x%	4.00 x 13.00 mm	
1	C25	10nF	Capacitor, Ceramic, 10V, 15%	0603	
2	C26	10uF, 25V	Capacitor, MLP, Multilayer Polymer, vvV, [temp], [tol]	6.3x11mm	
1	C27, C28	0.1uF,630V	CAP, PROPYLENE FILM, 630V, 10%	0.885 x 0.370 inch	
1	C29	10uF,25V	Capacitor, Ceramic, 25V, 20%	1210	
1	C31	10uF,35V	Capacitor, Ceramic, 35V, 20%	1210	
1	C32	2.2nF	Capacitor, Ceramic, 10V, 15%	0603	
1	C6	10uF,16V	Capacitor, Ceramic, 10V, 15%	0603	
4	C7	10uF,50V	Capacitor, Ceramic, 10V, 15%	0603	
2	C8, C9, C15, C30	1uF	Capacitor, Ceramic, 10V, 15%	0603	
1	D1, D2		Diode, LED, Red, 100 mA	805	
8	D16, D19		Diode, Switching, Dual, 200-V, 200-mA	SOT23	
4	D8,D9,D12,D11		Diode, Signal, 1000V, 3A	DO-41	
1	D20		Diode,Schottky, 200ma, 30V	DO-35	
6	D3, D4, D5, D6, D21, D22		Diode, Schottky, 100-mA, 100-V	SMA	
2	D7, D17		Diode, Zener, 15V, 0.5W	DO-41	
2	J1, J7		Header, Male 4-pin, 100mil spacing,	0.100 inch x 4	
1	J2		Header, 4-pin, 100mil spacing, (36-pin strip)	0.100 x 4	
	J4				
1	J5		Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 inch x 2	
1	J6		RMC-2PIN		
1	J8		Header, Male 10-pin, 100mil spacing,	0.100 inch x 10	
1	L1		EE2507, 10 pin vertical	EE25	
1	L2	10uH	Boost Inductor, EE20 6 Pin Vertical		
1	L3	220uH	Inductor, 3A, 70milliohm	220uH, 3A peak	

Table 2. Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number
2	Q1, Q2		MOSFET, N-ch, 60-V, 80-A, 6-milliOhms	TO-220V	
4	Q3, Q4, Q7, Q8		MOSFET, N-ch, 500-V, 6-A,	TO-220V	
1	Q11		N-Channel NexFET Power MOSFET	SON 2X2MM	
3	Q12, Q14, Q16		Transistor, N-Chan GP, 45V, 100mA	SOT23	
1	Q13		Trans, P-Chan GP, 65V, 100mA,	SOT-23	
2	Q5, Q6		Bipolar, NPN, 40-V, 200-mA	SOT23	
40	R1, R2, R36, R37, R40, R41, R44, R45, R48, R49, R42, R43, R6, R13, R14, R29, R56, R62, R30, R53, R17, R21, R4, R8, R9, R10, R11, R16, R33, R34, R54, R55, R61, R38, R39, R46, R47, R5, R35, R27	STD	Resistor, Chip, 1/16W, 5%	603	
1	R12	100E	Resistor, 1/2W, 5%	1210	
1	R52	0.5E	Resistor, 1W, 5%	0.150 x 0.700 inch	
6	R19, R22, R26, R32, R50, R51	STD	Resistor, Chip, 4.99 KOhms, 1/16-W, 5%	603	
2	R20, R57	STD	Resistor, Wirewound, 100Ohms, 2W, 5%	0.130 × 0.600 inch	
3	R28, R31	R23, R24, R25	STD	Resistor, 20 mΩ, 2W, 5%	2512
2	std	Res, Power, 0.5W 300v 5%	1206		
5	R15, R58, R63, R59, R18	STD	Resistor, Metal Film, 1/4 watt, ± 5%	1206	
1	T1		EI33 12PIN BOBIN		EI33
1	U1		MIXED SIGNAL MICROCONTROLLER	TSSOP(PW)28	MSP430G2233
1	U2		IC, 150mA, Low IQ, LDO Regulator	SOT23-5	TLV70433DDC
1	U3		IC, Digital control Compatible Double-Ended PWM Controllers	PWP16	UCD8220PWP
5	U4, U6, U7, U8, U9		IC, Photocoupler, High Speed Switching	DIP-4	PS2513-1
1	U5		DIODE, ADJ. PRECISION SHUNT	TO-92	TL431C-LP

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

8 References

1. UCD8220: Digitally-Assisted Push-Pull PWM Controller http://www.ti.com/product/ucd8220
2. MSP430G23xx: Value-Line MSP430 Series http://www.ti.com/product/msp430g2553
3. Design Review: 140-W, Multiple Output DC-DC Converter http://www.ti.com/lit/ml/slup117/slup117.pdf

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