Evaluation Module for the TPS65235-1 LNB Voltage Regulator With I²C Interface for DiSEqC1.x Application

This document presents the information required to operate the TPS65235-1 as well as the support documentation including schematic, layout, hardware setup, software application, key waveforms, and bill of materials.

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Trademarks

1 Background

The TPS65235-1 is designed to provide 13-V/18-V output voltage for a satellite receiver, with an operational range of 4.5 to 16 V.

The TPS65235-1 features I²C-controlled output voltage from 11 V to 20 V with 16 options; output current limit with ±10% accuracy is set with the ISET pin connecting different resistors. The maximum output current limit is up to 1 A.

The TPS65235-1 can also run without I²C. In non-I²C mode, the SCL pin and VCTRL pin are used to control 13-V/18-V output, these two pins can be controlled by GPIO from the processor. A dedicated enable pin, EN, is available to turn the LNB output on and off.

The evaluation module is designed to provide access to the features of the TPS65235-1 for DiSEqC1.x application. Some modifications can be made to this module to test performance at different input and output voltages, current and switching frequency. Please contact TI Field Applications Group for advice on these matters.

2 Schematic

Figure 1 illustrates the TPS65235-1 EVM schematic.

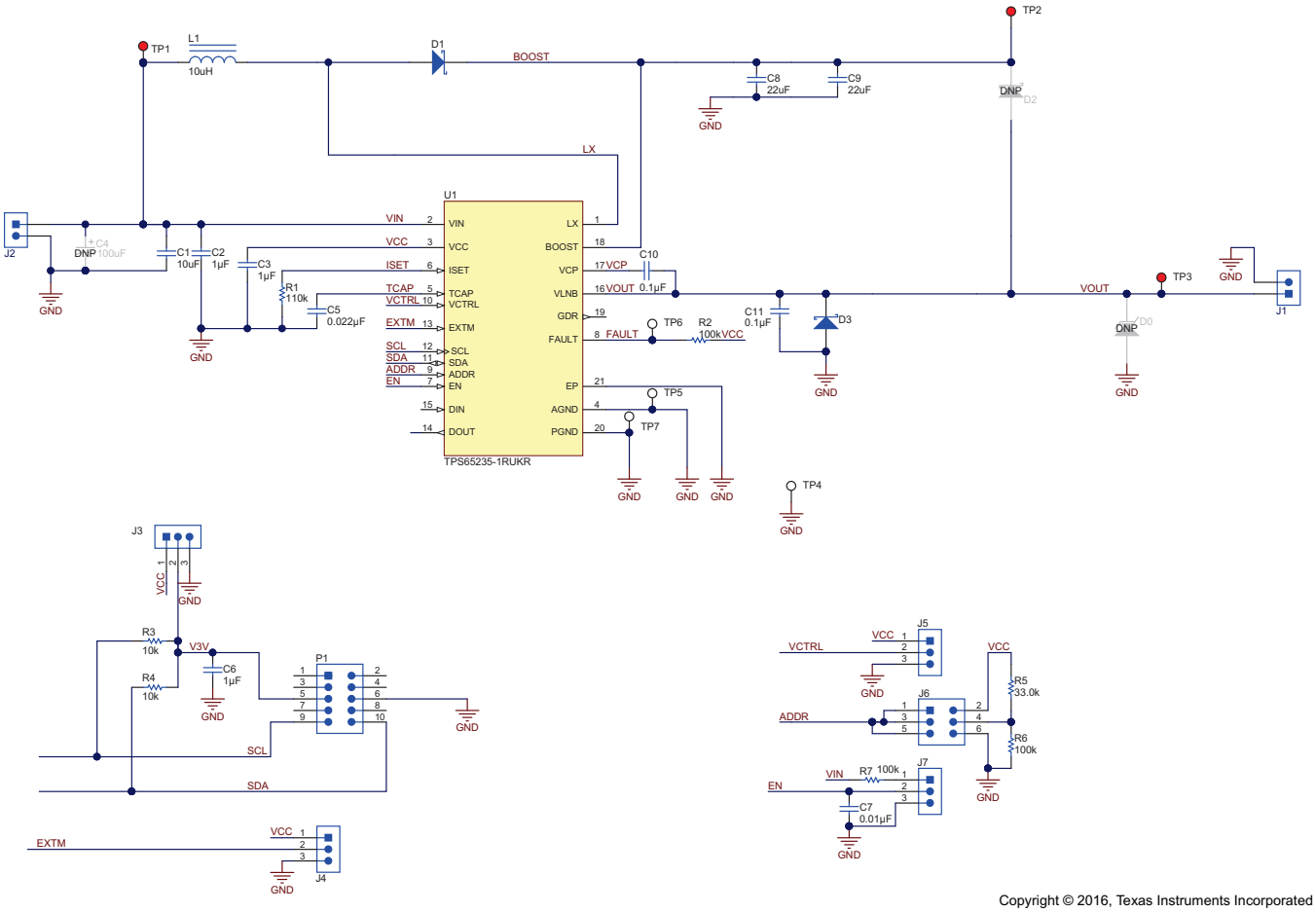

Figure 1. TPS65235-1 EVM Schematic

In the TPS65235-1 application, the recommended ceramic capacitors rated are at least X7R/X5R, 35-V rating and 1206 size for achieving lower LNB output ripple. For this EVM, two 22-µF, 35-V capacitors, C8 and C9, are put at the output of the boost converter. If lower cost is demanded, a 100-µF electrolytic (low ESR) and a 10-µF/35-V ceramic capacitor also works well.

3 Board Layout

Figure 2 shows the component placement on the EVM. Figure 3 and Figure 4 illustrate the top and bottom layers, respectively.

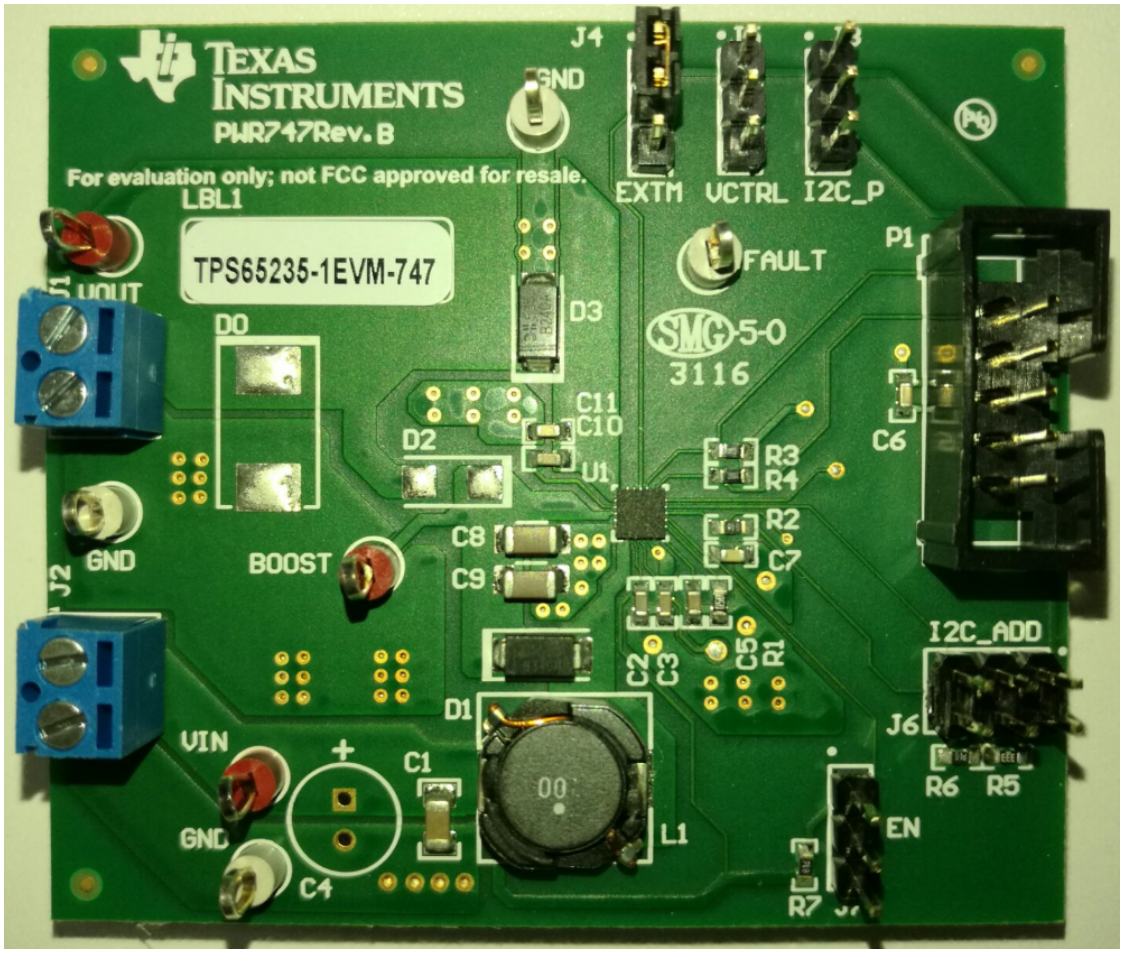

Figure 2. Component Placement (Top Layer)

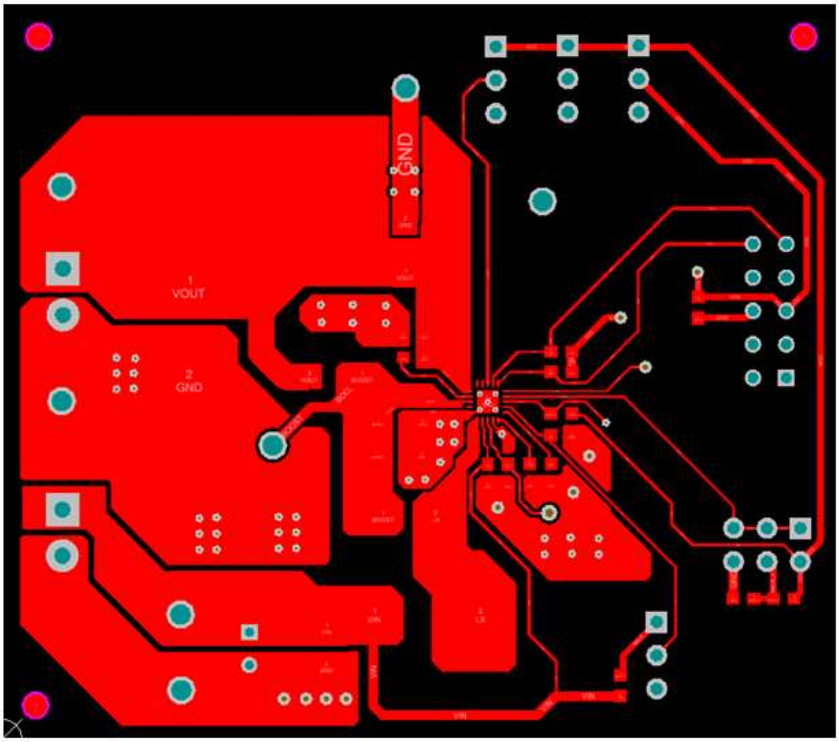

Figure 3. Board Layout (Top Layer)

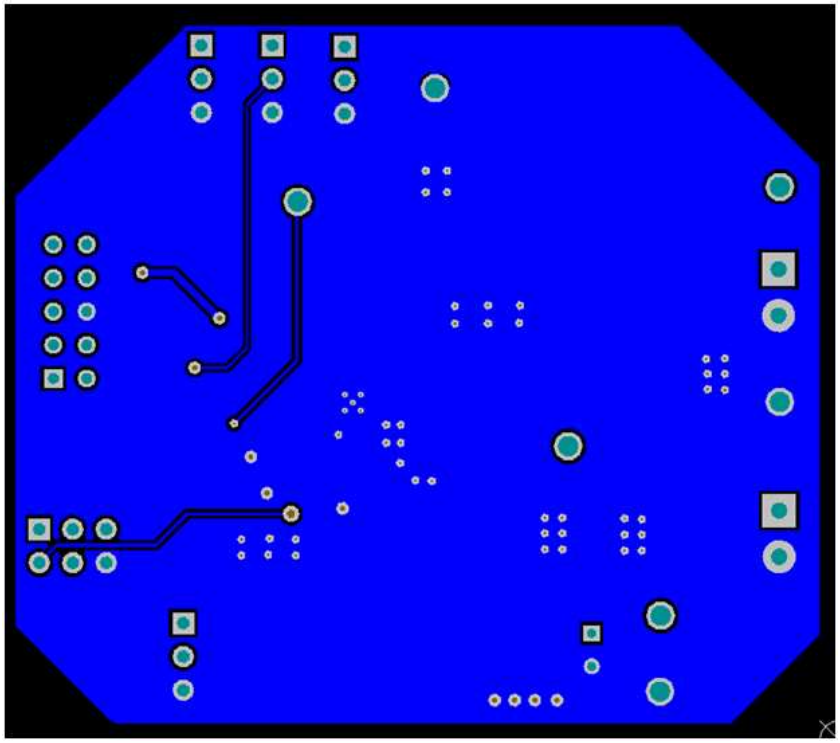

Figure 4. Board Layout (Bottom Layer)

4 Bench Test Setup Conditions

4.1 Headers Description and Jumper Placement

Figure 5 shows the header descriptions and jumper placement.

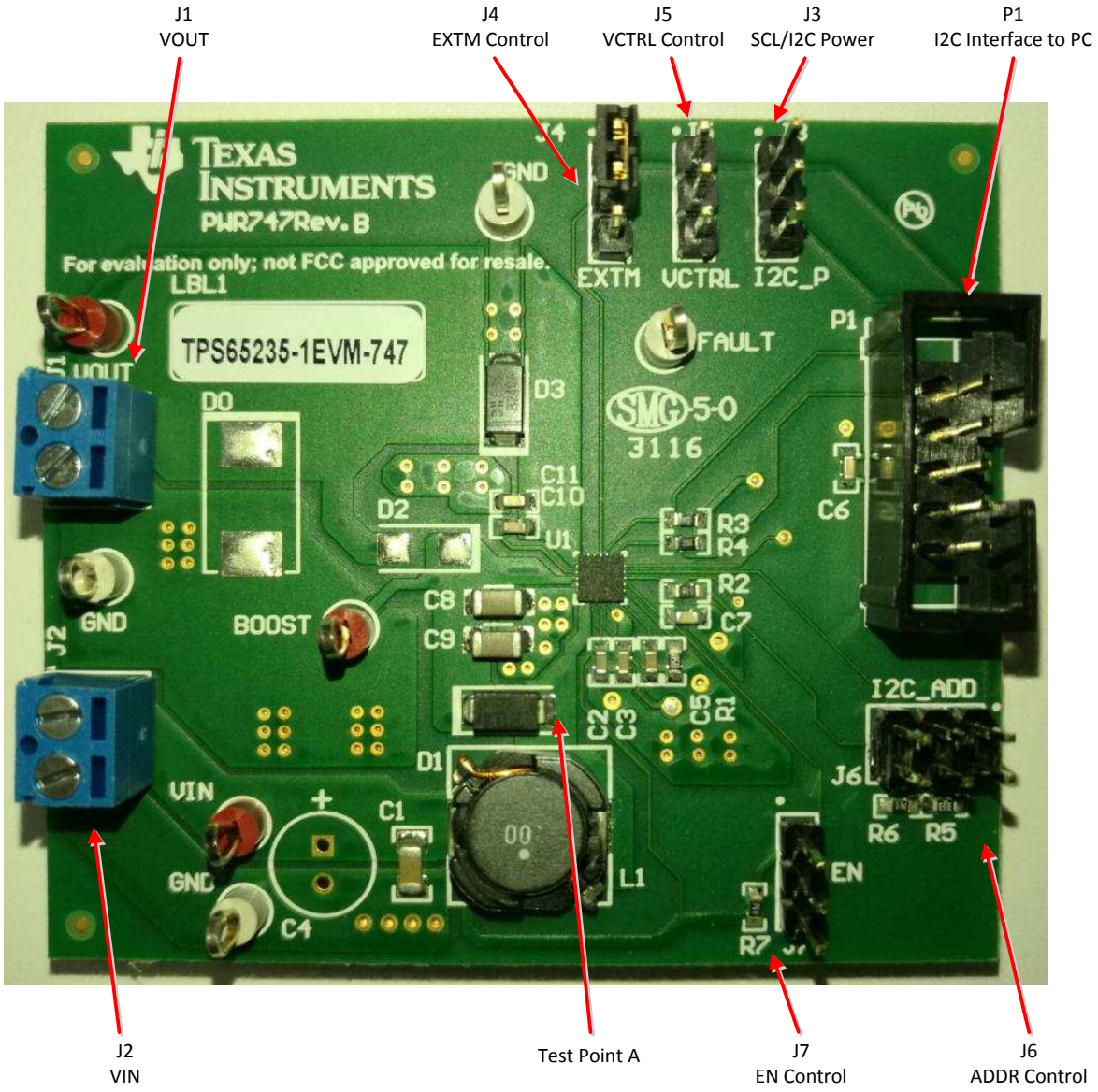

Figure 5. Headers Description and Jumper Placement

Test points:

A: LX for Boost

Notes:

- At non-I^{2}C mode, P1 should be floating, J5 and J3 are used to set the output, refer to Table 3.
- At I^{2}C mode, P1 is connected to the PC through the USB-TO-GPIO box, which makes the SCL signal to H. J5 can be used to set the default output when powered on, refer to Table 3.
- P1 and J3 cannot be connected at the same time.

Table 1 lists the I/O connections and Table 2 lists the EVM jumpers and switches.

Table 1. Input/Output Connection

#	Function	Description
J1	VOUT Connector	VLNB output
J2	VIN Connector	Apply power supply through this connector

Table 2. Jumpers and Switches

#	Function	Placement	Comment
J3	Output voltage control (SCL)	If the IC is not controlled by I²C, the VCTRL pin and SCL pin are combined to control the VLNB output voltage. Refer to Table 3 for details. Jumper J3-2 and J3-1 makes SCL to VCC connection and gives VLNB with output 14.6 V or 19.4 V Jumper J3-2 and J3-3 makes SCL to GND connection and gives VLNB with output 13.4 V or 18.2 V	
	I²C Power	If the IC is controlled by I²C, this is used to provide the I2C power which is connected to the SCL and SDA through pull-up resistors Leaving non jumpers connected sets the power to be 3.3 V from the I²C interface adaptor Shorting the J3-1 and J3-2 with a jumper sets the power to be VCC	On-board VCC is 6.3 V
J4	Tone control (EXTM)	Toggle the EXTM signal (J4-2 to J4-3 and then J4-2 to J4-1), the internal tone signal is superimposed at the VLNB output VOUT EXTM to GND (J4-2 to J4-3), no internal tone signal is superimposed at VOUT	
J5	Output voltage control (VCTRL)	If the IC is not controlled by I²C, the VCTRL pin and SCL pin are combined to control the VLNB output voltage. Refer to Table 3 for details. Jumper J5-2 and J5-1 makes VCTRL to VCC connection and gives VLNB with an output of 18.2 V or 19.4 V Jumper J5-2 and J5-3 makes VCTRL to VCC connection and gives VLNB with an output of 13.4 V or 14.6 V	
J6	I²C address set (ADDR)	This pin is the I²C address set pin; tie to VCC sets I²C address with 0x08H; floating, sets I²C address with 0x09H; tie to GND sets I²C address with 0x10H; resistor divider R9A and R9B make ADDR pin at the voltage to set the I²C address with 0x11H. Refer to Table 4 for details.	With 3 V- VCC - 0.8 V will set the I²C address 0x11H;
J7	VLNB output enable (EN)	Connect jumper EN to GND to disable the VLNB output (shorts J7-2 to J7-3), connect EN to V_{IN} through a 100-kΩ resistor to enable the VLNB output (short J7-2 to J7-1) Leaving open enables VLNB output too.	

Table 3. VLNB Output Control Without I²C Interface Connection

EN	SCL	VCRTL	VLNB
H	H	H	19.4 V
H	H	L	14.6 V
H	L	H	18.2 V
H	L	L	13.4 V
L	X	X	0 V

4.2 Hardware Requirement

This EVM requires an external power supply capable of providing 4.5 V to 16 V at 4 A.

The EVM kit includes the USB-TO-GPIO interface box which, when installed on a PC and connected to the EVM, allows the user to communicate with the EVM via a GUI interface. (The EVM and USB-TO-GPIO interface box must be ordered separately.) The minimum PC requirements are:

- Microsoft® Windows ® 2000, Windows XP or Windows 7 operating system
- USB port
- Minimum of 30MB of free hard disk space (100MB recommended)
- Minimum of 256MB of RAM

4.3 Hardware Setup

After connecting the power supply to J2, floating J7, connect J3, J4, and J5 to GND, J6 and P1 floating, turning on the power supply, the EVM will regulate the output voltages to 13.4 V without tone superimposed.

In order to change the output voltage by sending the digital control signal via a PC running the TPS65235-1 controller software and USB-TO-GPIO interface box, perform the following steps:

- Connect one end of the USB-TO-GPIO box to the PC using the USB cable and the other end to P1 of the TPS65235-1 using the supplied 10-pin ribbon cable, per Figure 6. The connectors on the ribbon cable are keyed to prevent incorrect installation.
- Floating J3
- Connect the power supply on J2 and turn on the power supply
- Run the software as explained in the next section.

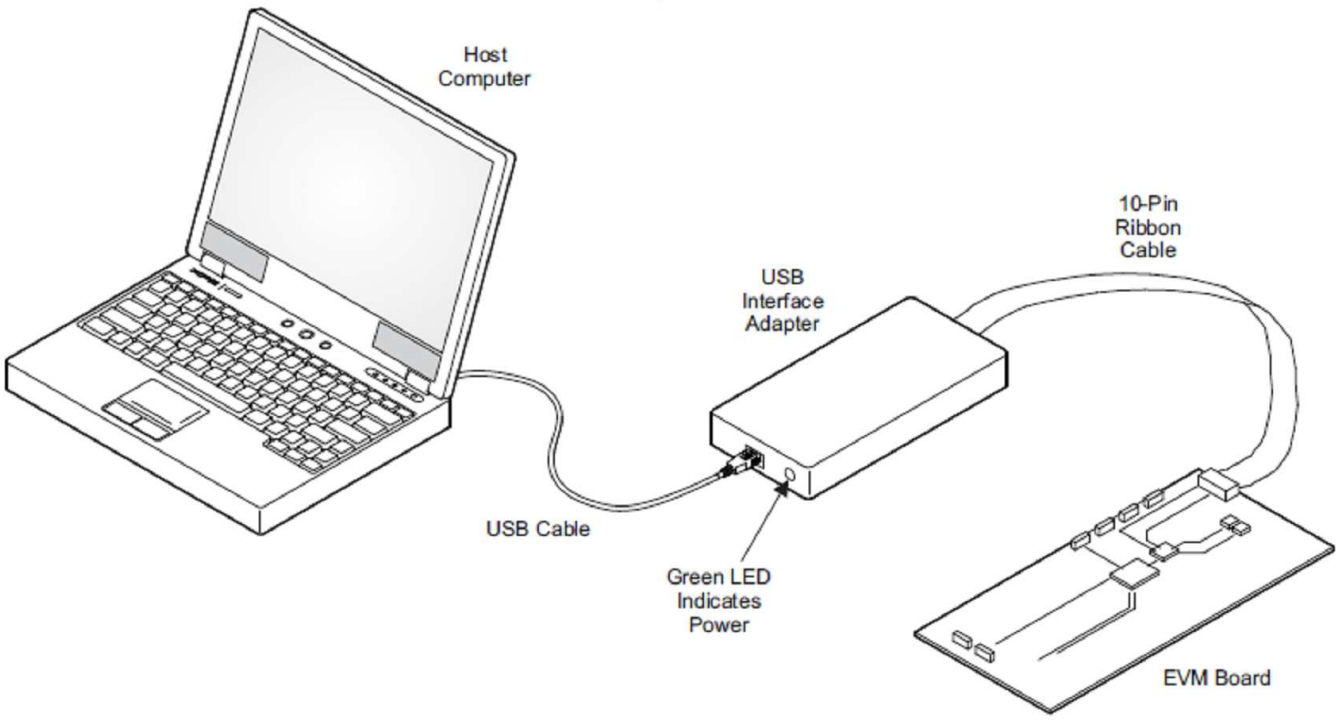

Figure 6. USB Interface Adapter Quick Connection Diagram

5 Installing the Software

If installing from the TI Web site, visit the www.ti.com/product/TPS65235-1/toolssoftware URL.

NOTE: This installation page is best viewed with Microsoft Internet Explorer® browser (it may not work correctly with other browsers).

1. Click on the install button; your PC should display a security warning and ask if you want to install this application. Select *Install* to proceed.
2. To run the software after installation, either use the desktop icon, which is created by the installer if the user agrees to creating a desktop icon, or go to Start → All programs → Texas Instruments → TPS65235-1.

   At start-up, the software first checks the firmware version of the USB-to-GPIO adapter box. If an incorrect firmware version is installed, the software automatically searches on the Internet (if connected) for updates. If a new update is available, the software notifies the user of the update, and downloads and installs the software. Note that after the firmware is updated, the user must disconnect and then reconnect the USB cable between the adapter and PC, as instructed during the install process. The host PC software also automatically searches on the Internet (if connected) for updates. If a new update is available, the software notifies the user of the update and downloads and installs it. During future use of the software, you are prompted to install a new version if one becomes available on the Web.

NOTE: VERISIGN® Code Signing is used to prevent any malicious code from changing this application. If at any time in the future the binaries are modified, the code will no longer attempt to run.

6 Software Operation

This section provides descriptions of the EVM software.

The supplied software is used to communicate with the TPS65235-1EVM. Click on the icon on the host computer to start the software. The software first displays the home page for the user interface. Entrances are available for the expert user or beginner.

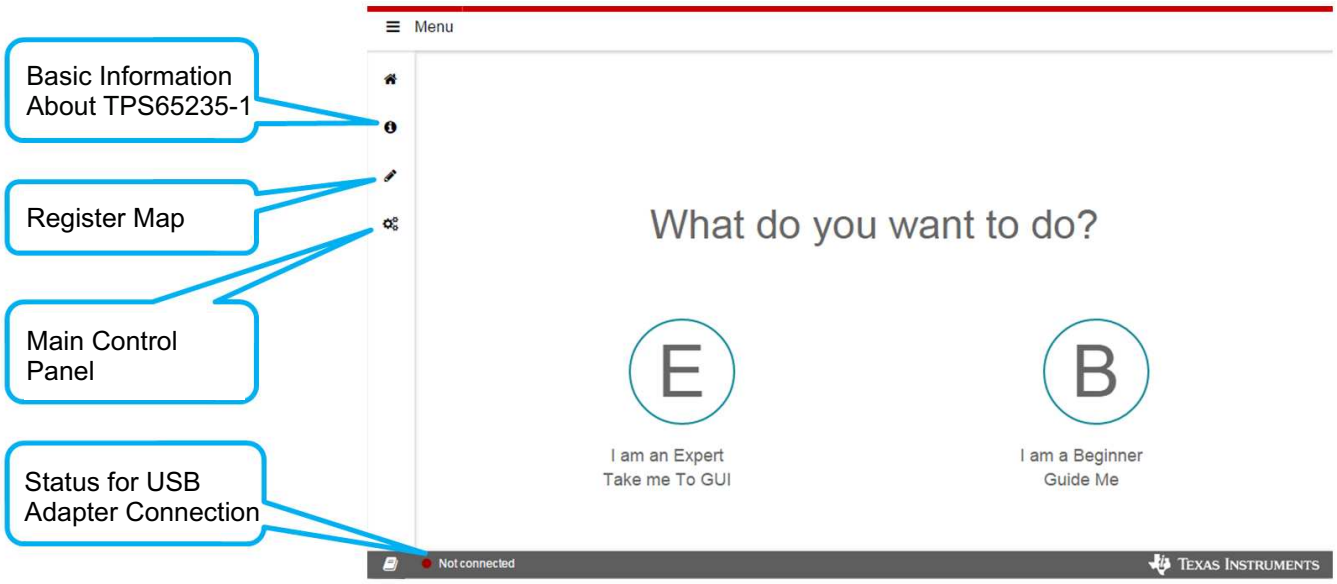

Figure 7. GUI Interface Home Page

Click on the “B” button, the “Basic information about TPS65235-1” page comes up which lists the features and application information for TPS65235-1. Follow the steps, the GUI guides the beginner to setup the EVM and GUI step by step to do the basic check for the EVM.

6.1 Register Map Page

Click the “E” button, the Register Map interface (Figure 8) displays.

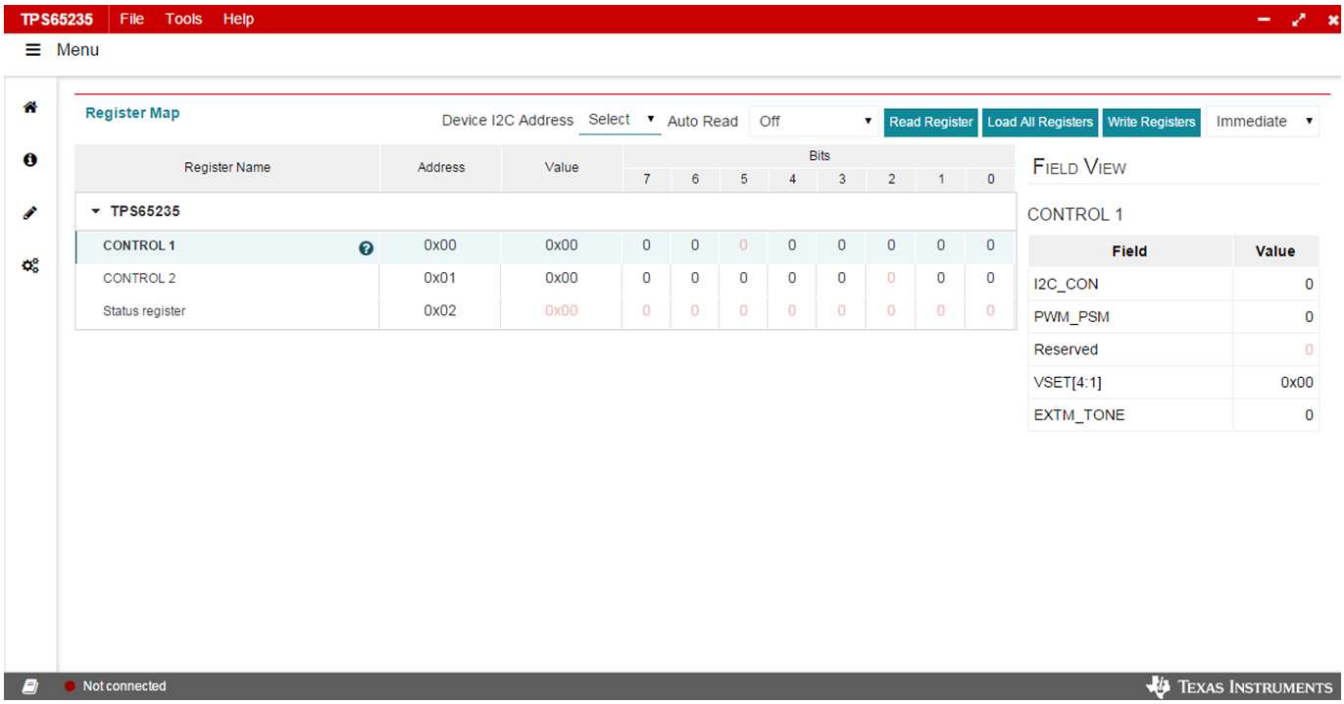

Figure 8. GUI Bit Register Map Page

Single click on the register, the right “FIELD VIEW” comes up showing the detail setting of each bit.

Double clicking on the bit can change the it to “0” or “1”.

Single click on the “?” for the register, the detail description page for this register displays.

For the “Write Registers” option, when the “Immediate” button is selected, any change is sent to the EVM immediately; otherwise, “Write Registers” button for each register must be clicked to send the control signal.

Register values can be read back from the EVM by clicking “Read Register” for each register or “Load All Registers” or set the “Auto Read” choice.

The *Status for USB Adapter Connection* only shows the status for the adapter, not the EVM board. The customer can click the Write Registers on the Register Map page to verify the board communication.

6.2 Basic Settings

Clicking the main control panel displays the “Basic Settings” interface. This interface provides a simple method for setting registers. Clicking the “Auto Read” button allows the register status to be monitored automatically.

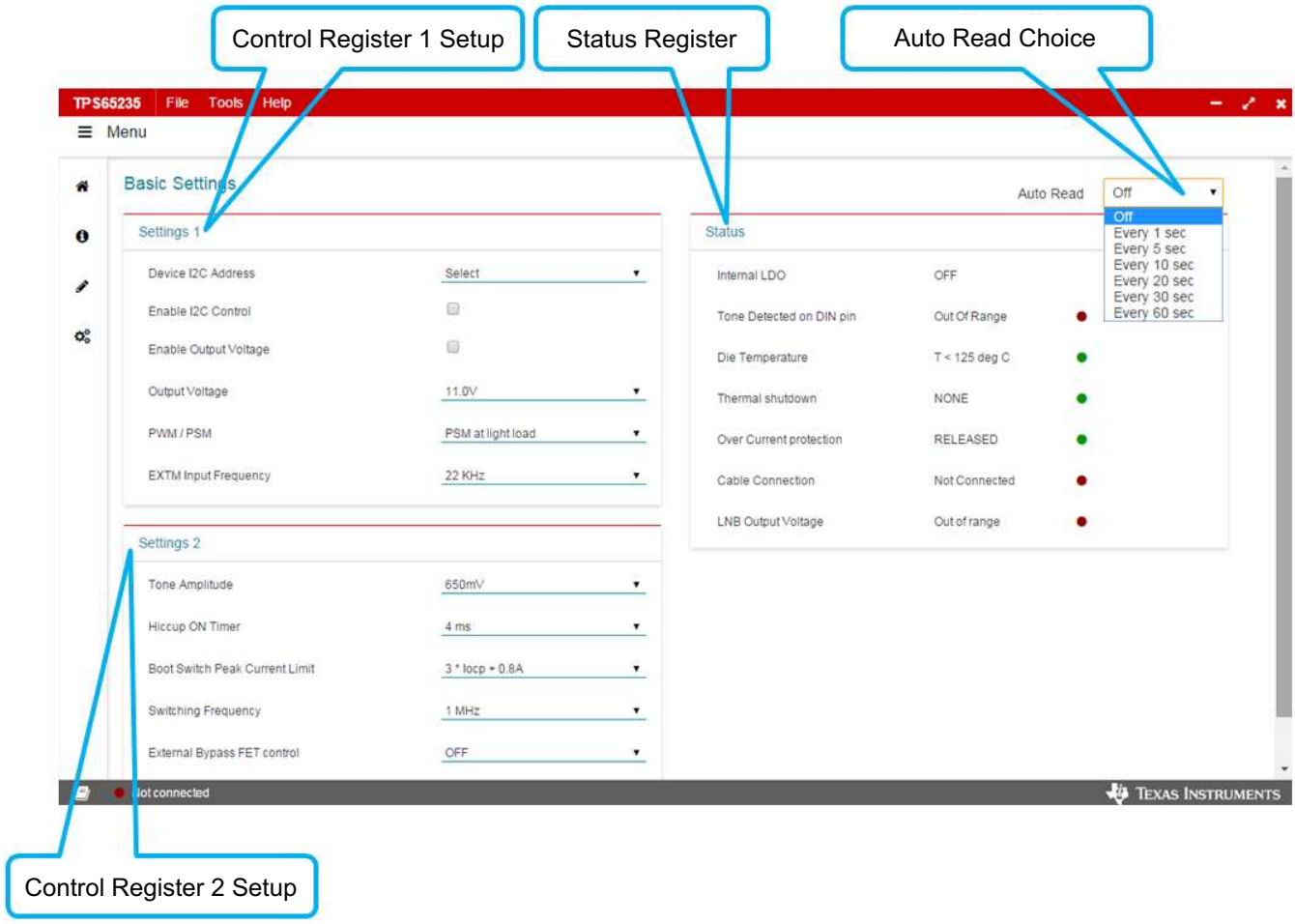

Figure 9. GUI Main Control Panel

Figure 7 to Figure 9 show the control GUI interface. There are three 8-bit registers embedded in the TPS65235-1; two to control the output voltage characteristics, and one for status feedback. Make changes by selecting and checking the components on the *Basic Settings* page in the GUI. Changes are also made by directly clicking the bits of each register on the *Register Map* page. Set the I^2C address with J6 to control the ADDR pin, refer to Table 2 and Table 4.

Table 4. I^2C Address Selection

ADDR Pin	I^2C Address
Connect to VCC	0x08H
Floating	0x09H
Connected to GND	0x10H
Resistor divider to make ADDR pin voltage in 3 V ~ VCC-0.8 V	0x11H

7 Test Procedure Example

7.1 Voltage Output Check

Use the following voltage output checks while testing the EVM:

1. Connect I2C adapter to P1
2. Floating J3, J6, and J7, J4 to GND, J5 to GND
3. Apply 12 V to J2
4. Apply loads or non load to the output connector J1, check the output
5. Set the control register 0x00H and 0x01H to the expected output value and then check the output
6. Monitor the status register 0x02H for the IC status

7.2 Tone Output

Use the following tone output checks while testing the EVM:

1. Connect I2C adaptor to P1
2. Floating J3, J6, and J7, J5 to GND
3. Apply 12 V to J2
4. Toggle the EXTM (J4) from low to high, check the tone output at VOUT
5. Apply loads or non-load to the output connector J1, check the output

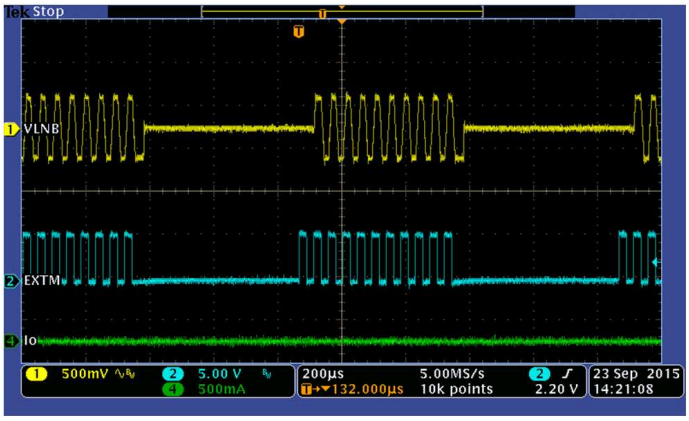

Figure 10. EXTM has 22-kHz External Tone Input

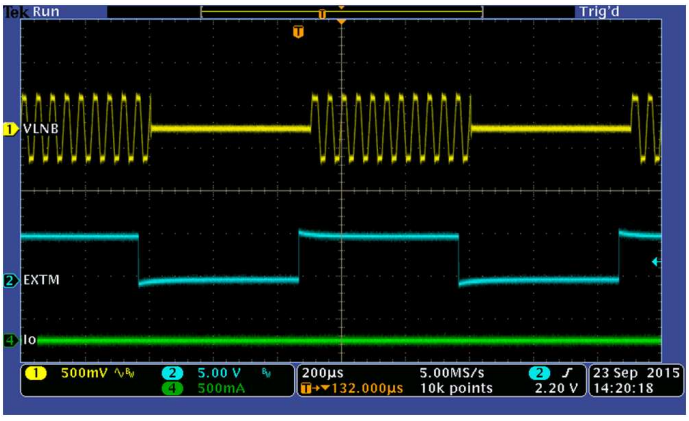

Figure 11. EXTM has Envelope Input for Tone Output Control

8 Bill Of Materials

Table 5 lists the EVM BOM.

Table 5. TPS65235-1EVM Bill Of Materials

Designator	Description	Manufacturer	Part Number	Qty
PCB1	Printed Circuit Board	Any	PWR747	1
C1	CAP, CERM, 10 µF, 25 V, +/- 10%, X5R, 1206	Murata	GRM31CR61E106KA12L	1
C2, C3, C6	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0603	Murata	GRM188R61E105KA12D	3
C5	CAP, CERM, 0.022 µF, 50 V, +/- 10%, X7R, 0603	Murata	GRM188R71H223KA01D	1
C7	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0603	Murata	GRM188R71H103KA01D	1
C8, C9	CAP, CERM, 22 µF, 35 V, +/- 20%, X5R, 1206_190	TDK	C3216X5R1V226M	2
C10	CAP, CERM, 0.1 µF, 16 V, +/- 5%, X7R, 0603	AVX	0603YC104JAT2A	1
C11	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	Murata	GRM188R71H104KA93D	1
D1	Diode, Schottky, 40 V, 3 A, SMA	Diodes Inc.	B340A-13-F	1
D3	Diode, Schottky, 40 V, 2 A, SMA	Diodes Inc.	B240A-13-F	1
H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
J1, J2	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS	2
J3, J4, J5, J7	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	4
J6	Header, 100mil, 3x2, Gold, TH	Samtec	TSW-103-07-G-D	1
L1	Inductor, Shielded, Ferrite, 10 µH, 4 A, 0.0312 ohm, SMD	TDK	CLF10040T-100M	1
P1	Header (shrouded), 100mil, 5x2, Gold, TH	Omron Electronic Components	XG4C-1031	1
R1	RES, 110 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603110KFKEA	1
R2, R6, R7	RES, 100 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KFKEA	3
R3, R4	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	2
R5	RES, 33.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060333K0FKEA	1
SH-J1	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA	1
TP1, TP2, TP3	Test Point, Multipurpose, Red, TH	Keystone	5010	3
TP4, TP5, TP6, TP7	Test Point, Multipurpose, White, TH	Keystone	5012	4
U1	LNB VOLTAGE REGULATOR WITH I2C INTERFACE	Texas Instruments	TPS65235-1RUKR	1

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3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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