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Introduction

The TSW4100 contains a signal chain consisting of an ADC, DDC, DUC, and DAC to create a repeater application. The design has a clock distribution solution, and an interface for programming and reading programmable devices on the TSW4100 with a PC. In addition to the interfaces, the TSW4100 provides test connectors, which can be used to monitor the RX outputs or provide inputs to the TX portion of the chain.

The TSW4100 requires only a single 5-6 V DC power source at 3 A to operate.

The block diagram of the TSW4100 is shown in Figure 1.
Figure 1. TSW4100 Block Diagram
2 TSW4100 Interfaces

2.1 USB Port J26

USB port connector J26 provides a PC interface to allow writes and reads between a PC/Laptop and the FPGA and the two GC5016 ([SLWS142](#)) devices. This interface helps program the two GC5016 devices with existing software provided by TI. The parallel port connector provides the same functionality when configured. The default TSW4100 configuration has the USB port enabled and leaves the parallel port disabled.

2.2 USB Connector J25

USB connector J25 provides a PC interface to allow writes and reads between a PC/Laptop and the DAC5688 and the CDCM7005 ([SCAS793](#)) devices. There is an option to allow this interface to write to the ADS5545 ([SLWS180](#)) device when configured for serial interface, but the board has this part configured for parallel interface mode. With this configuration, the part operation is determined by jumpers.

3 Hardware Configuration

By using the provided software and on-board jumpers, the TSW4100 can be set up in a variety of configurations to accommodate a specific operation mode. Before starting evaluation, the user should decide on the configuration and make the appropriate connections and load the appropriate parameters for the GC5016's, DAC5688, ADS5545, and CDCM7005 devices.

3.1 Power Requirements

The TSW4100 requires 5V-6V DC at approximately 3.0 Amps. The board contains several on-board regulators that generate the necessary voltages from the 5V-6V DC source. The board provides banana jacks J4 (red) and J5 (black) for use with a separate power supply. When using this mode, connect 5V-6V DC to J4 and the return to J5.

3.2 Jumper Settings

The board jumper description and default settings are shown in Tables 1, 2, and 3. Details of the software operation modes can be found in the software section of this document. Table 1, Table 2, and Table 3 explain the functionality of the board jumpers.

Table 1. Two Pin Jumper List

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Function</th>
<th>Installed</th>
<th>Removed</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>J7</td>
<td>DUC clock input test point</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>J10</td>
<td>DDC clock input test point</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>J18</td>
<td>Sets Parallel port J2 interface drive mode</td>
<td>Open drain</td>
<td>Totem pole</td>
<td>Removed</td>
</tr>
<tr>
<td>J19</td>
<td>Used to disable VCXO U19 when providing external oscillator at J20</td>
<td>Enables U19</td>
<td>Disables U19</td>
<td>Installed</td>
</tr>
</tbody>
</table>

Table 2. Three Pin Jumper List

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Function</th>
<th>Location: Pins 1-2</th>
<th>Location: Pins 2-3</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP7</td>
<td>CDCM7005 reference select</td>
<td>Reference clock provided by J21</td>
<td>Reference clock provided by Y1 or Y2</td>
<td>2-3</td>
</tr>
<tr>
<td>JP5</td>
<td>CDCM7005 complimentary clock</td>
<td>input select Clock provided from VCXO U19</td>
<td>Input connected to VBB of CDCM7005</td>
<td>1-2</td>
</tr>
<tr>
<td>JP6</td>
<td>CDCM7005 clock input select</td>
<td>Clock provided from VCXO U19</td>
<td>Input clock provided from J20</td>
<td>1-2</td>
</tr>
<tr>
<td>JP1</td>
<td>ADS5545 output enable</td>
<td>Output enabled</td>
<td>Output disabled</td>
<td>1-2</td>
</tr>
<tr>
<td>SJP3</td>
<td>ADS5545 output clock direction</td>
<td>Sends output clock to DDC</td>
<td>Sends output clock to FPGA</td>
<td>1-2</td>
</tr>
</tbody>
</table>
Table 2. Three Pin Jumper List (continued)

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Function</th>
<th>Location: Pins 1-2</th>
<th>Location: Pins 2-3</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>SJP11</td>
<td>ADC input clock select</td>
<td>Provides clock from CDCM7005 to T5</td>
<td>Provides clock from SMA connector J13</td>
<td>removed</td>
</tr>
<tr>
<td>JP4</td>
<td>ADC clock buffer enable</td>
<td>Enables ADC clock buffer U14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J17</td>
<td>Selects cable side operation voltage</td>
<td>Sets VCAB to +3.3V</td>
<td></td>
<td>2-3</td>
</tr>
<tr>
<td>JP12</td>
<td>Selects signal path for DAC5688</td>
<td>CDCM7005 output Y1A to DAC CLK1CB</td>
<td>Connects DAC CLK1C to LED D9.</td>
<td>1-2</td>
</tr>
<tr>
<td>JP13</td>
<td>Selects signal path for DAC5688 CLK1</td>
<td>Connects CDCM7005 output Y1B to DAC CLK1C</td>
<td>Connects DAC CLK1C to FPGA.</td>
<td>1-2</td>
</tr>
<tr>
<td>SJP9</td>
<td>DDC input clock select</td>
<td>ADC output clock to DDC</td>
<td>FPGA output clock to DDC</td>
<td>1-2</td>
</tr>
<tr>
<td>SJP8</td>
<td>DUC input clock select</td>
<td>FPGA output clock to DUC</td>
<td>CDCM705 output clock to DUC</td>
<td>1-2</td>
</tr>
<tr>
<td>SJP1</td>
<td>Selects +5V source for USB controller</td>
<td>+5V sourced from board.</td>
<td>+5V sourced from USB cable.</td>
<td>1-2</td>
</tr>
<tr>
<td>SJP2</td>
<td>Selects +5V source for USB controller</td>
<td>+5V sourced from board.</td>
<td>+5V sourced from USB cable.</td>
<td>1-2</td>
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</table>

Table 3. Jumper J15 List

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Function</th>
<th>Location = +3.3V</th>
<th>Location = GND</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL_VDD</td>
<td>Sets logic value of SYNC pin of DAC5688</td>
<td>Sets SYNC to GND</td>
<td>Sets SYNC to +3.3V</td>
<td>1-2</td>
</tr>
<tr>
<td>Sleep</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Not Used</td>
</tr>
<tr>
<td>EXT_LO</td>
<td>Sets logic value of EXTLO pin of DAC5688</td>
<td>Sets EXTLO to GND</td>
<td>Sets EXTLO to +3.3V</td>
<td>7-8</td>
</tr>
<tr>
<td>TXENABLE</td>
<td>Sets logic value of TXENABLE pin of</td>
<td>Sets TXENABLE to GND</td>
<td>Sets TXENABLE to +3.3V</td>
<td>11-12</td>
</tr>
<tr>
<td>CDC_PD</td>
<td>Sets logic value of Power Down pin of CDCM7005</td>
<td>Sets PD to GND</td>
<td>Sets PD to +3.3V</td>
<td>14-15</td>
</tr>
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</table>

3.3 Apply Power to Board

The TSW4100 contains an Altera EP2C8 Cyclone II™ FPGA (U10) and an Altera EPCS4™ reprogrammable serial configuration PROM. The EPCS4 is pre-programmed to a default configuration. To prepare the board for operation:

1. Plug in the provided power supply to connector J3 and the other end to +110 VAC.
2. Press the DAC RESET switch SW5 on the TSW4100 board.
3. Ensure the FPGA is configured by verifying the D2 LED is on.
4. Verify the CDCM7005 VCXO and reference clock are present (D4 and D5 LEDs are on).

4 Software Installation

This section describes the software installation procedures needed to operate the TSW4100:

- Section 4.1 Installing the TSW4100 interface to the GC5016 CDC and DAC Software
- Section 4.2 Installing the USB Driver Software
- Section 4.3 Installing the MATLAB Runtime Engine
- Section 4.4 Installing the TSW4100GUI Software
4.1 Installing the TSW4100 Interface to GC5016 CDC and DAC Software

The TSW4100 uses a modified version of the existing DAC5688 EVM LabView software program for writing and reading to the DAC5688 and CDCM7005. This software is separate from the TSW4100 software used to design and load GC5016 filter configurations.

Note: Once all software is loaded, TI recommends the host computer be restarted. This software has been verified to be functional for the Windows 2000 and Windows XP operating systems.

1. Copy the folder **TSW4100_DAC_CDC_Installer** found on the TSW4100 Installation CD-ROM to a temporary directory on the host PC.
2. Double-click the **setup.exe** filename found under this directory.
3. Follow the standard Windows Installation procedure that includes accepting the License Agreement and using the default installation directory.

   **CAUTION**

   Do not start the software after completing the installation.

4.2 Installing the USB Driver Software

The USB interface adapter provides an additional, dedicated PC IP address to connect to the TSW4100 IP address. To install this adapter:

1. Plug in one of the USB cables between J25 of the TSW4100 board and a PC. The software should recognize the connection and ask for drivers.
2. After the **Welcome to the Found New Hardware Wizard** message displays, select the **No, not at this Time** option.
3. Select the **Install from a list or specific location (advanced)** option.
4. If asked, click on the **Don't search. I will choose the driver to install** option.
5. If a window opens with the following driver name **Texas Instruments TSW4100 DAC and CDC Controller**, select this then click next. If this does not appear, navigate to the **C:\Program Files\TSW4100_DAC_CDC\TSW4100 Dr**

   Drivers directory.
6. Click **Open**.
7. The software loads the drivers in this directory. When prompted, select the **Continue anyways** option.
8. Complete the USB driver installation. If the driver cannot be found, click on the option **Don't search. I will choose the driver to install**. Click **Next**.
9. A new widow should open with a couple of options to choose from. Select **TSW4100 DAC and CDC Controller**. Click **Next**.
10. Repeat steps 6 and 7. This completes the TSW4100 DAC and CDC driver installation.
11. Copy the folder **TSW4100_GC5016 Drivers** found on the **TSW4100 Installation CD-ROM** to a temporary directory on the host PC.
12. Plug in the other USB cable between J26 of the TSW4100 board and a PC. The software should recognize the connection and ask for drivers.
13. After the **Welcome to the Found New Hardware Wizard** message displays, select the **No, not at this Time** option.
14. Select the **Install from a list or specific location (advanced)** option.
15. Navigate to the **TSW4100_GC5016 Drivers** directory.
16. Click **Open**.
17. The software loads the drivers in this directory. When prompted, select the **Continue anyways** option.
18. Complete the USB driver installation.
4.3 Installing the MATLAB Runtime Engine

This section helps you install the MATLAB Runtime engine which is used to run the provided MATLAB executable code.

1. Double-click on the `MCRInstaller.exe` file located on the TSW4100 installation CD. The Choose Setup Language (Figure 2) displays. Click OK for English (United States).

![Figure 2. Choose Setup Language](image)

2. When the MATLAB Component Runtime 7.5 screen (Figure 3) displays, click Next.

![Figure 3. MATLAB Welcome Screen](image)

3. For the Customer Information (Figure 4) screen, specify the User Name, Organization, select the desired user option button, and click Next.
4. When the Destination Folder screen (Figure 5) displays, click Next to install the MATLAB software in the default directory.

5. When the Ready to Install the Program screen (Figure 6) displays, click Install to begin the installation. The installation lasts approximately five minutes.
6. Click Finish once the InstallShield Wizard Completed screen (Figure 7) displays.

Figure 6. Ready to Install the Program

Figure 7. InstallShield Wizard Completed
4.4 Installing the TSW4100GUI Software

1. Double-click the `TSW4100GUI\installer.exe` filename found in the top-level folder of the TSW4100 Installation CD-ROM. The TSW4100 Installation Wizard (Figure 8) displays. Click Next.

Figure 8. TSW4100 Installation Welcome

2. When the License Agreement (Figure 9) displays, select the *I accept the terms in the License agreement* option and click Next to accept the TSW4100 Software License Agreement.

Figure 9. TSW4100 License Agreement
3. On the Customer Information (Figure 10) screen, provide User Name, Organization information, and select the appropriate Install this Application for option. Click Next.

![Figure 10. Customer Information](image)

4. On the Setup Type (Figure 11) display, select the Complete Setup Type option and click Next.

![Figure 11. Setup Type](image)
5. On the Ready to Install the Program (Figure 12) display, click Install. The installation takes between one and three minutes to complete.

![Figure 12. Ready to Install the Program](Image)

6. Click Finish once the InstallShield Wizard Completed screen (Figure 13) displays.

![Figure 13. InstallShield Wizard Completed](Image)
5 Running the TSW4100 CDC and DAC Interface

5.1 Starting the TSW4100 Interface

The TSW4100 software is now ready to use. To start the application program, click the Windows menu sequence **start → All Programs → Texas Instruments TSW4100 DAC and CDC Control → TSW4100 DAC and CDC Control** (Figure 14).

*Note:* Click **OK** if a warning message about Internet connections is received. This provides a link for the current TSW4100 data sheets on the TI Internet Site. Unplug and plug the USB connector if necessary. The user may need to click the **USB Reset** button (on the left side of the GUI) to reinitialize the USB connection.

![Figure 14. TSW4100 CDC/DAC Graphical User Interface](image)

If the error message **DAC5688 EVM not detected** is displayed, indicating that the host is unable to communicate with the DAC5688, perform these actions:

1. Press the DAC RESET switch SW5 on the TSW4100 board.
2. Click the **Read All** button on the **DAC5688 Registers** window.
3. Click **Reset USB** button on the left side of the TSW4100 DAC CDC GUI.
4. If this does not fix the problem, reboot the host computer. If the problem still exists, uninstall the software and any other TI software such as the DAC5688 or TSW3003 if it exists on the computer. Re-install the TSW4100 DAC CDC software.
5.2 Loading the CDCM7005 with Default Values

By using the provided CDCM7005 serial peripheral interface (SPI) software, the user can load settings to the CDCM7005 internal registers. This must be performed every time power is applied to the TSW4100 EVM. The CDCM7005 device has default settings that are loaded at powerup and are different than the settings needed to operate the TSW4100.

To load the CDCM7005 with the TSW4100 default values:

1. Open the TSW4100 DAC CDC GUI. Upon opening, the GUI will automatically send the TSW4100 default values to the CDCM7005. LED D6 should now be illuminated indicating the CDCM7005 is locked to the internal 10MHz reference.

2. Click on Reset USB Port. After this, if no changes are going to be made to the CDCM7005, the user can skip steps 2-10 and go the Loading the DAC5688 section.

3. To make changes to the CDCM7005, click the CDCM7005 Registers option in the top, left-hand corner. The CDCM7005 interface (Figure 15) displays.

4. The PLL tab goes to another window which allows the user to change the VCXO, reference, and output frequency. The current default values are set to match the VCXO and reference oscillator that are installed on the TSW4100.

5. The Output tab allows the user to set the divide ratio, output drive standard, and output mode for all of the outputs. The current default values are what is required for the TSW4100 to operate with.

6. The Advanced tab allows the user to change several parameters used by the internal PLL of the CDCM7005 along with other parameters. Consult the CDCM7005 data sheet for more information on these controls.

7. After making any changes to any of these settings, click the SEND All button to load the CDCM7005 registers with the new values.

8. The default values are also stored in a file provided by TI. To load the stored settings, click the Load Settings button on the lower left side of the GUI.

Figure 15. CDCM7005 Interface
9. Navigate to the directory (C:\Program Files\Texas Instruments\TSW4100GUI\CDCandDACregisters) for the default register settings and select the file TSW4100_DAC_CDC_example_1.txt. This file is also located on the provided CD as well.

10. Click OK to load the CDCM7005 registers with default values.

11. To save a custom configuration, click on the Save Settings button and provide a file name. This file will then save all of the current settings for both the DAC5688 and CDCM7005.

The TSW4100 uses differential and single-ended clocks from the CDCM7005:
- Y0A and Y0B to drive the DAC5688 CLK2 inputs.
- Y1A and Y1B to drive the DAC5688 CLK1 inputs.
- Y2A provides an option to drive the DUC. This is currently not used and the output is 3-stated.
- Y2B to drive the single-ended FPGA input clock.
- Y3A and Y3B to drive the FPGA differential input clock.
- Y4A provides an option to drive the ADS5545 along with Y4B and bypass the transformer. This is currently not used and the output is 3-stated.
- Y4B to drive the crystal filter and transformer which generate the ADS5545 differential input clock.

This default configuration generates:
- 320 MHz clock for CLK2 inputs of the DAC5688.
- 160 MHz clock for CLK1 inputs of the DAC5688.
- Two 160 MHz clocks for the FPGA.
- 160 MHz clock input for the ADS5545.

5.3 Loading the DAC5688

The default values for the DAC5688 and CDCM7005 are stored in a file provided by TI. To load the stored settings, click the Load Settings button on the lower left side of the GUI.

Navigate to the directory (C:\Program Files\Texas Instruments\TSW4100GUI\CDCandDACregisters) and select the file TSW4100_DAC_CDC_example_1.txt. The GUI loads both the DAC5688 and CDCM7005 with the settings contained in this file every time the Load Settings function is used. After the DAC5688 is configured, the user must make sure the internal PLL is locked. To verify this, click on the DAC5688 Registers button in the top, left-hand corner of the GUI. Click on the PLL tab. The GUI shall now look as shown in Figure 16. If the PLL Lock indicator is Green, the DAC5688 has been loaded properly and is ready for operation. If the indicator is Red, indicating the PLL is not locked, press the DAC5688 reset switch SW5, then click on the Auto-Sync button on the top right side of the GUI. If PLL Lock indicator still does not turn Green, press the DAC Reset button SW5 on the TSW4100 and reload the DAC and CDC settings. The PLL Lock Indicator must be Green for the DAC5688 to be working properly.

To make changes to the DAC5688, do the following:
1. Click the DAC5688 Registers button in the top, left-hand corner of the GUI.
2. The GUI should now be displaying the Input tab settings, as shown in Figure 17. In this window, the user can change the Input Formats, MUX options, Output path, and Fixed Data settings.
3. Click on the Digital tab. The GUI display shall now look as shown in Figure 18. In this window, the user can change the DAC interpolation rate, FIFO settings, Mixer settings, Quadrature Modulation Correction settings, and Offset adjustments.
4. Click on the Clock tab. The GUI display shall now look as shown in Figure 19. In this window, the user can change the Clock Settings and Clock Adjustments.
5. Click on the PLL tab. The GUI display shall now look as shown in Figure 16. In this window, the user can change the PLL mode, view the PLL status, change the PLL Ratios and PLL Gain settings. After the DAC5688 and CDCM7005 have been configured, make sure that the PLL Lock indicator on the GUI turns from Red to Green. If this does not work, click on the Auto-Sync button on the top right side of the GUI. If PLL Lock indicator still does not turn Green, press the DAC Reset button SW5 on the TSW4100 and reload the DAC and CDC settings. The PLL Lock Indicator must be Green for the DAC5688 to be working properly.
6. Click on the *Output* tab. The GUI display shall now look as shown in Figure 20. In this window, the user can change the DAC gains, turn on or off the two DAC channels, and modify the DAC output delays and enable or disable the LPF option for each DAC.

7. Click on the *Sync* tab. The GUI display shall now look as shown in Figure 21. In this window, the user can change the SIF control, the FIFO sync source, the Clock Divider, the QMC, and the NCO.

8. The *Advanced* tab is for factory test only. This window should not be used.

9. More information regarding the operation of these registers can be found in the DAC5688 Data Sheet.

10. After completion of all changes, click the *Send All* button on the top right side of the GUI. The register values will now be loaded into the DAC5688.

11. Click on the *Read All* button, located on the top right side of the GUI, to view the current register settings of the DAC5688. If an error message is not received, the program is working properly.

![Figure 16. DAC5688 Interface](image-url)
Running the TSW4100 CDC and DAC Interface

Figure 17. DAC5688 Options

Figure 18. DAC5688 Filters
Figure 19. Clock Settings

Figure 20. DAC Gain
6 TSW4100 Graphical User Interface (GUI) Software

Using the provided software, the user can download control register and coefficient information data to the GC5016 and read back status register information.

**Note:** The TSW4100 ships with firmware installed to operate this interface with a PC. This interface must be added to any new firmware that is installed or generate an alternative method of writing and reading to the GC5016.

The next two sections describe how to start the TSW4100GUI user interface (Section 6.1) and the graphical user interface controls (Section 6.2).

6.1 **Starting the TSW4100GUI**

**Note:** To interface with the TSW4100, the CDCM7005 must be operating and locked.

To start the TSW4100GUI interface:

1. Click the Windows menu sequence **start → All Programs → Texas Instruments → TSW4100GUI → TSW4100GUI_vXpXX.exe**, (Figure 14) where vXpxx represents the version of software. The application first displays a DOS Test Window. The text *Extracting CTF... CTF archive extraction complete* only displays the first time the TSW4100GUI application runs.
2. The TSW4100 graphical user interface displays.

**Figure 22. TSW4100GUI DOS Test Window**

**Figure 23. TSW4100GUI Interface**

**Tip:** The DOS Test window displays the same information as the MATLAB command window would display. Use it to monitor the application for internal MATLAB errors.

**Note:** If the TSW4100 GUI display does not fit on the user’s monitor, a second version of the GUI can be loaded which reduces the size of the GUI. This executable is called *TSW4100GUI_vXpXX_resize.exe* and can be found at **C:\Program Files\Texas Instruments\TSW4100GUI**.
6.2 Graphical User Interface Controls

General Settings area

This area helps the user load and save the necessary configurations and results (filter response figures):

- **Save Plots (.bmp)**—saves the filter response figures (Section 6.3) as bitmap (*.bmp filename extension) graphic files.
- **Save Structs (.mat)**—saves the Matlab structures used to setup the channels in files (*.mat filename extension).
- **Real Time Delay**—adjusts the delay between DDC and DUC sync to occur when Sync delay setting is adjusted without reprogramming the DDC and DUC. (Enabled after the TSW4100 is programmed.)
- **Program TSW4100**—loads configurations into the TSW4100 and starts the sync sequences when selected.
- **Configure**—generates the DDC and DUC configurations and loads them to TSW4100 when the Program TSW4100 check box is selected.
- **USB Interface**—use the USB connector to interface to the TSW4100, when selected. This is the default hardware configuration. The parallel port interface is not typically supported by hardware.
- **Base File Name**—name of the folders and files containing the programming and sync information.

![Figure 24. General Settings Controls](image)

Status area

This area displays context-sensitive information and error messages. Also check the DOS Test window for MatLab and other diagnostic information.

![Figure 25. Status area](image)

Left Column area

The user interface controls (Figure 26) on the left side of the screen control major functionality settings and the content of the output filter response displays.
Figure 26. Left Column Interface Controls

- **Channel Mode selections**—Choose between SPLIT IQ and 4 CHANNEL modes.

**CAUTION**

The mixed mode $\text{Ch} = \text{SPLIT IQ}$ and $\text{Ch 3/4} = \text{4 CHANNEL}$ is invalid. In this case, swap $\text{Ch} = \text{SPLIT IQ}$ and $\text{Ch 3/4} = \text{4 CHANNEL}$ option selections.

Figure 27. Channel Selection Controls
Table 4. Channel Selection Options

<table>
<thead>
<tr>
<th>Ch = Option Selected</th>
<th>Ch 3/4 Option Selected</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPLIT IQ</td>
<td>SPLIT IQ</td>
<td>Valid selection</td>
</tr>
<tr>
<td>SPLIT IQ</td>
<td>4 CHANNEL</td>
<td>Invalid selection</td>
</tr>
<tr>
<td>4 CHANNEL</td>
<td>SPLIT IQ</td>
<td>Valid selection</td>
</tr>
<tr>
<td>4 CHANNEL</td>
<td>4 CHANNEL</td>
<td>Valid selection</td>
</tr>
</tbody>
</table>

- GC5016 Output options:
  - Complex output sent to DAC.
  - Dual Real sends CH1 and CH2 outputs combined as a real signal to DAC channel A. Output frequency is in first Nyquist zone. Set DAC mixer to \( F_s/2 \) for second Nyquist zone output.
  - Single Real sends CH1–CH4 outputs combined as a real signal to DAC channel A. Output frequency is in first Nyquist zone. Set DAC mixer to \( F_s/2 \) for second Nyquist zone output.

- Nyquist Zone—ADC Nyquist Zone for the input signal. The frequency band and DAC settings are listed in Table 5.

Table 5. Nyquist Zone Frequencies and DAC Settings

<table>
<thead>
<tr>
<th>Nyquist Zone</th>
<th>Minimum Frequency</th>
<th>Maximum Frequency</th>
<th>DAC NCO (Complex Output) / Real Output</th>
<th>DAC NCO Dual Real IF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>Clock( \times 2 )</td>
<td>Clock( \times 4 )</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>Clock( \times 2 )</td>
<td>Clock</td>
<td>Clock( \times 3 )( \times 4 )</td>
<td>( F_s/2 )</td>
</tr>
<tr>
<td>3</td>
<td>Clock</td>
<td>Clock( \times 3 )( \times 2 )</td>
<td>Clock( \times 5 )( \times 4 )</td>
<td>NA</td>
</tr>
</tbody>
</table>

- Clock (MHz)—clock rate for the GC5016. The default TSW4100 uses a 320 MHz VCXO, which is divided by 2 to produce a 160 MHz clock for the GC5016.
- Plots - RX + TX PFIRs—plots RX and TX PFIR filter spectra before CIC compensation and scaling. Displays the number of taps used for each filter. (See Figure 30 for an example.)
- Plots - RX/TX CONV—plots the convolved RX + TX filter response, including CIC compensation and design limits. (See Figure 31 for an example.)

Channel Configuration area

This area configures the channel signal, prior to filtering.

Figure 28. Channel Configuration Controls

- CIC rate—CIC decimation or interpolation.
- PFIR rate—PFIR decimation or interpolation. Only a value of 2 can be selected.
- IF (MHz)—frequency in ADC second Nyquist Zone of channel.
- PFIR Max Taps—maximum number of PFIR taps available for this mode. Includes CIC compensation taps, so the number of Taps\(_{raw\ filter} = PFIR_{Max\ Taps} - \text{number of CIC compensation taps} + 1. \) (See Section 7.8 for more information and examples of CIC compensation taps design.)
6.2.1 Load Filter controls

- **Gain (dB)**—Nominally digital gain of channel from ADC input to DAC output. Does not include inherent analog gain loss (ADC input full scale is 11.2 dBm and DAC output full scale is 4 dBm). To disable a channel, set Gain (dB) to a large negative gain (approximately –80 dB).

**Filter Settings area**

Use this portion of the GUI to load a filter (Section 6.2.1) without CIC compensation or design a filter (Section 6.2.2 and Section 6.2.1) based on spectral information. For the Load Filter option, the Passband BW (MHz) needs to be set for calculating the CIC compensation.

![Filter Load and Design Settings](image)

**Figure 29. Filter Load and Design Settings**

6.2.1 Load Filter controls

- **DDC**—loads the filter digital down converter (DDC) file (default filename extension is *.taps). This filter is used before adding cascaded integrator-comb (CIC) compensation and does not need to be quantized.
- **DUC**—loads the filter digital up converter (DUC) file (default filename extension is *.taps). This filter is used before adding CIC compensation and does not need to be quantized.
- **CIC taps**—sets 0, 3, or 5 CIC compensation taps to add for externally generated filters to be loaded. When no taps are added, the filter input is expected to be properly scaled.

6.2.2 Design Filter controls

- **Passband BW (MHz)**—full bandwidth across which the ripple is specified.
- **Ripple (dB)**—maximum ripple of passband.
- **Stopband Freqs (MHz)**—stopband frequencies *offset from center of passband*. Separate multiple input frequencies with spaces (multiple spaces permitted).
- **Stopband Amps (dB)**—stopband amplitudes (dB) that correspond to each stopband frequency specified in the **Stopband Freqs (MHz)** text box. Stopband amplitude is held until stopband frequency (stair step). Separate multiple amplitudes with spaces (multiple spaces permitted).

6.2.3 Interface controls

- **Clk ratio**—clock divider ratio for DDC-DUC interface. Automatically set to **CIC rate**×**PFIR rate** for **SPLIT IQ** mode.
- **Sync Delay**—delay in DDC to DUC syncs. After TSW4100 is programmed, check real time sync for a new sync to be issued for the channel each time this is changed.
6.3 Filter Response Windows

After clicking the **Configure** button (if the filter is successfully designed) in the General Settings area the frequency response for each PFIR filter BEFORE CIC compensation and quantization is displayed in a window labeled Figure 2*N–1 (Figure 30), where N is the channel number. The odd-numbered figures also display the number of PFIR taps used, plus if the filter is symmetric or asymmetric.

![Figure 1](image)

**Figure 30. (Figure 2*N–1 Window) Frequency Response Before CIC Compensation and Quantization**

The frequency response for the convolved end-to-end response is displayed in a window labeled Figure 2*N (Figure 31), where N is the channel number. The even-numbered figures also display ripple and stopband limits in red, and actual ripple and stopband amplitudes.

**Note:** The stopband amplitudes are one half the input values, as the DDC and DUC filter operate in series, doubling the attenuation. The final band, which is the image band, is 1× the final stopband amplitude. These figures also include the image bands.
7 Designing and Testing a Filter (Step-by-Step)

This example takes the user through the steps to design a new filter and configure the TSW4100.

Assume there are filter spectral requirements:
- Passband Bandwidth = 12 MHz
- Peak-to-Peak passband Ripple = 1 dB
- Stopband = 50 dB at 6.5 MHz (.05 MHz from band edge)
- 4 channels

**Note:** The TSW4100 GUI can be used stand alone (not connected to the TSW4100) to do filter design or generate the DUC and DDC configuration.

7.1 Step 1—Start TSW4100GUI

Click the Windows menu sequence **start** → **All Programs** → **Texas Instruments** → **TSW4100GUI** → **TSW4100GUI.exe** to start the TSW4100GUI.
7.2 **Step 2—Channel Selection**

Since 4 channels are needed, change the Ch = mode to the 4 CHANNEL option.

Also, the user only wants to design a filter for channel 1. Turn off channels 2 and 3 by clicking on the "OFF" button on the GUI for Channel 2 and Channel 3. This prevents the software from doing the filter design for these channels, saving time.

7.3 **Step 3—Selecting Filter Design Parameters**

Begin by choosing the decimation rate for the CIC. For 12 MHz bandwidth, the total maximum decimation is calculated using **Equation 1**:

\[
\text{Trunc} \left( \frac{\text{Clock \( M(Hz) \)}}{\text{filter \ BW}} \right) = \text{Trunc} \left( \frac{160}{12} \right) = 12
\]  

(The final result in **Equation 1** needs to be the next even value lower than the calculated value).

Because the PFIR has a fixed decimation of 2 (only value allowed), this results in a value of 6 for the maximum CIC decimation.

However, if the spectral requirements can be met with less decimation (more difficult as the number of PFIR taps is less and each tap covers less time), lower decimation typically results in a shorter latency. This is because other components (such as the interface circuits) are operating at a higher clock rate than the PFIR. Start with a decimation of 6, but then also try to decrease the decimation (Section 7.9) to find the minimum required to meet the spectral requirements (Section 7).

![Figure 33. CIC Decimation Rate](image)

**Note:** As the user changes the **CIC rate** value, the value for the **PFIR Max Taps** is recalculated (191 in the case of the CIC decimation rate of 6 for Figure 33).

To set up the **Filter Design** parameters, the user needs to translate the spectra requirements.

a. Set the **Passband BW (MHz)** to 12 for full bandwidth.

b. Set the **Ripple (dB)** to 1 for full bandwidth.

c. Set the **Stopband Freqs (MHz)** to 6.5 as shown in **Equation 2**.

d. Set the **Stopband Amps (dB)** to 50.

Stopband Frequency = Passband BW / 2 + Bandedge Frequency = 12 / 2 + .5 = 6.5

![Figure 34. Filter Design Parameters](image)
7.4 **Step 4—Saving Filter Design Information**

Before running the design, go to the bottom left-hand corner and select the **Save Plots (.bmp)** and **Save Structs (.mat)** check boxes. This saves the filter response images (Section 6.3) and the MATLAB data structures containing channel configuration information.

![Figure 35. Save Filter Design and Responses](image)

7.5 **Step 5—Running the Filter Design**

Now run the filter design program and calculate if the filter is achievable using the number of available PFIR taps. If there are other filters to design, use the other channels to design these filters simultaneously. However, for now keep the defaults in Ch 2 and Ch 3/4—these filters are designed but do not affect the design of our filter in Channel One.

Click the **Configure** button.

7.6 **Step 6—Briefly Examining the Filter Response Windows**

As the program calculates the spectra responses, the **Status** area (lower right-hand corner) displays the messages, *generating filter 1*, *generating filter 2*, and so forth. A total of six windows display when the filter design calculations are complete. Each Channel has two figures showing the:

- DDC and DUC separate PFIR spectral responses (Figure 36)
- Composite DDC filter input to DUC filter output (Figure 37)

First, look at Figure 36. This plot shows the PFIR spectral response of the DUC (TX) and DDC (RX) *before* convolution with CIC correction taps (using 3 or 5 taps).
Designing and Testing a Filter (Step-by-Step)

Figure 36. DDC (TX) and DUC (RX) PFIR Responses - Before CIC Correction Convolution

Now look at Figure 37, which shows the composite frequency response from DDC input to DUC output. There are three response curves; the composite response of the PFIRs and CIC filters, plus the images from the CIC decimation and interpolation filter.

Figure 37. Composite Frequency Response
Also shown in red are the ripple and stopband targets, which are also reported in the text in the upper right-hand corner. As can be seen, the 50 dB stopband requirement is met by the composite response. However, focusing in on the passband ripple (Figure 38) shows the ripple is approximately 1 dB peak-to-peak, meeting our requirement. In some cases, the passband ripple can be slightly larger than the target ripple, due to the CIC compensation having a small error.

![Diagram of CH1 PFIR Response: Convolved RX and TX PFIRs](image)

**Figure 38. Passband for the Composite Frequency Response**

### 7.7 Step 7—Examine the Filter Response Passband

The X-axis in Figure 36 has a frequency range from 0 Hz to $F_{PFIR}/2$, where $F_{PFIR} = \text{Clock} \div \text{CIC rate}$ or 160 MHz/6 (13.333 MHz). The Y-axis displays the filter response amplitude relative to the gain at 0 Hz. Image rejection for the DDC decimation and DUC interpolation of 2 requires that each filter response be 50 dB in the stopband $F_{PFIR}/2$ – Passband BW (13.333–6 = 7.333 MHz) to $F_{PFIR}/2$.

The passband in Figure 36, expands the display by choosing the hourglass (+) icon, click a location on the window, and drag the mouse to define the passband area to magnify.

![Define the Passband Area to Magnify](image)

**Figure 39. Define the Passband Area to Magnify**

Releasing the mouse, yields the magnified filter response passband in Figure 40. The passband ripple for each filter is roughly equal at ±0.25 dB each, or 0.5 dB peak-to-peak. The filter design program divides the allowed ripple equally between the DUC and DDC PFIR design; not including the CIC compensation and CIC. This allows no margin for incomplete CIC compensation, which is discussed in section Section 7.8.
7.8 Step 8—Evaluate Effect of Taps on Filter Latency

In the original frequency response, the upper right-hand corner contains annotation regarding the number of filter taps and symmetry (or lack) of the DUC and DDC filters.

The number of TX taps used in the DUC PFIR without CIC compensation is 69. After convolving with the 5 CIC compensation taps, the total PFIR length is 74 taps. Since this is less than one-half of the maximum PFIR taps (191), the DUC is asymmetric in time around the center of the PFIR coefficient memory, which is 96 taps. This is done to minimize the latency of the filter. The PFIR coefficient memory locations for taps 60 to 96 (Figure 41) are set to zero.
The latency of the PFIR filter (excluding other latency in the GC5016–CIC filter, interface circuits, NCO, gain, and so forth) is the time from the beginning of the filter taps to half of (number of taps + 1). By placing the filter in the forward part of the memory space and appending with zeros, as opposed to the placing it symmetrically in the coefficient memory space, the latency is minimized. However, the number of available taps for an asymmetric coefficient memory space is only half of a symmetric coefficient memory, so it may not be possible to design a filter meeting the spectral requirements asymmetrically.

The number of RX taps is 91 without CIC compensation and is also asymmetric. After including the 5 tap CIC correction, the number of RX taps is 95.

### 7.9 Step 9—Redesign by Decreasing the CIC Decimation

Now modify the Channel 1 filter design to include less CIC decimation. Reset the CIC rate to 4 and click on the “Configure” button (Figure 42) The maximum number of PFIR taps is reduced to 127, when the CIC rate is reduced.

![Figure 42. Redesigned Filter Settings](image)
As shown in Figure 43, the redesign is successful and resulted in 71 uncompensated DUC PFIR taps and 123 uncompensated PFIR taps.

Examine the Passband ripple for the complete response in Figure 31, measure it at 1.12 dB or 0.1 dB greater than the design requirement.

---

**Figure 43. Redesigned Filter Response (without CIC Compensation)**

**Figure 44. Redesigned Filter Passband**
Also, looking at the stopband, the attenuation is only about 46 dB or 4 dB less than the 50 dB design requirement.

![Graph showing CH1 PFIR Response: Convolved RX and TX PFIRs]

Figure 45. Redesigned Filter Stopband

### 7.10 Step 10—Redesign by Changing the Filter Parameters

By adjusting the Filter parameters for the passband (0.9 dB ripple) and stopband (60 dB) the user can meet the design requirements. Figure 46 displays the magnified passband for the successfully redesigned filter.

![Graph showing CH1 PFIR Response: Convolved RX and TX PFIRs]

Figure 46. Passband of Successful Filter Design
Changing the target ripple to 0.9 dB increases the DUC uncompensated filter taps to 105, but reduces the ripple to 1 dB.

Since both the total PFIR taps for the DUC and DDC are greater than half the maximum PFIR taps, filters must be symmetric in the PFIR coefficient memory space. This implies the latency is fixed, regardless of the number of PFIR taps in the design (up to the maximum).
So without any penalty, make the filter requirements more stringent, such as reduce the transition band. By trial and error, reduce the Stopband Frequency to 6.46 MHz and still design the filter.

![Graph showing CH1 PFIR Response: TX and RX](image)

**Figure 49. Filter with Reduced Stopband**

With this target, the number of DDC and DUC PFIR taps are both 123 taps (before adding 4 taps for the CIC compensation), at the maximum for CIC decimation of 4. Reducing the Stopband Frequency further, to approximately 6.4 MHz, gives an error in the Status area, indicating the filter requirements are not achievable:

![Status message indicating filter requirements not met](image)

### 8 Programming the TSW4100

#### 8.1 Connecting an input source and output analyzer

To match the test below, connect a 100 MHz, 0 dBm tone to the ADC input SMA. The IF of the channel is tested at 95 MHz with a 12 MHz bandwidth, so 100 MHz is within the channel passband. Ideally this tone should be filtered to reduce spurious products outside the 80 to 160 MHz Nyquist band of the ADC. Removing unwanted output harmonics is described later in Section 8.7.

Connect the DAC output SMA to a spectrum analyzer.
8.2 **Program clock PLL and DAC**

The first step in programming the TSW4100 is to program the clock PLL and DAC. This procedure assumes the installation of the TSW4100GUI in Section 4.4.

1. Apply power to the TSW4100. Connect the USB and parallel port cables.
2. Before programming the GC5016 DDC and DUC, perform the DAC5688 stand alone test.
3. Select the *Load Settings* button and load the file TSW4100_DAC CDDL_example_1.txt, as was done in section 5.2.
4. **Click on the DAC5688** Register button. The Input tab should now be displayed. In the Input Options window, change the Format from 2's compliment to offset binary. The DAC5688 will now be operating in stand alone mode.
5. Verify there is an output tone at SMA connectors J11 and J12 at 120 MHz with approximately 4 dBm power and 70 dBc SFDR between 80 and 160 MHz per Figure 50.

![Figure 50. DAC Stand Alone Test Spectrum](image)

6. Now program the DAC5688 normal operation as described in Section 5.3 by changing the output format back to *two's complement*. This should result in removing the tone.
8.3 Programming the DUC and DDCs

Following the filter design steps in Section 7 the TSW4100 GUI should look like Figure 51. If the settings are different, adjust the settings to match Figure 51.

The Sync Delay setting of 5 controls the delay between the start of channel 1 in the DDC and the start of channel 1 in the DUC, and is critical to align the timing of the (interleaved I and Q) data transfer between the DDC and DUC for each channel in the 4 CHANNEL modes.

1. Change the Sync Delay in the Channel 1 Interface to 5.
2. Select the Real Time Delay and Program TSW4100 check boxes in the interface lower left corner. These settings are also saved in the filename C:\Program Files\Texas Instruments\TSW4100GUI\TSW4100example1_config.mat.
3. Click Configure. The filter design starts. After the design is complete, the GUI programs the DDC, followed by the DUC. These actions display in the Status area. After Finished displays in the Status area, the user should see the output spectrum in Figure 52.

The spectra should have a single tone present at exactly the same frequency as the input. The output amplitude should be approximately –10 dBm, reflecting 7 dB loss between the ADC and DAC full scale and another 3 dB loss due to cables, transformers, and so forth.
8.4 Setting the Sync Delay for a Channel

In 4 channel mode, the DDC I and Q data is transferred interleaved to the DUC. The GC5016 is the master of the interleave timing in both DDC and DUC modes — the DDC sends an indication with the frame strobe signal of when the I and Q data are present, and likewise, the DUC sends an indication with the frame strobe signal of when I and Q data should be present, see Figure 53. Since neither chip can use the others frame strobe as an input, a synchronization delay is needed between the DDC and DUC to align the DDC output I and Q samples to the DUC input I and Q samples.

Figure 52. Filter Design Output Spectrum

Figure 53. Proper DDC Output and DUC Input Timing Alignment
Similarly, in splitIQ mode, where I and Q are output in parallel, the DDC output data is held a maximum of 16 clock cycles. Therefore, if the decimation ratio exceeds 16, synchronization of the DDC output and DUC input is needed to make sure the DDC output data is present during the input time of the DUC. See Figure 54.

The TSW4100 can send an external sync signal to the SyncA input of both the DDC and DUC. The SyncA is used to individually synchronize each DDC or DUC channel, which for a given configuration will result in a deterministic and repeatable delay between the DDC SyncA signal and DDC output timing or DUC SyncA signal and DUC input timing. A time delay between the DUC SyncA signal and the DDC SyncA signal of up to 256 clock periods can be programmed using the TSW4100GUI. By adjusting the delay between the DUC and DDC SyncA signals, the output timing of the DDC can be adjusted to be properly aligned with the input timing of the DUC. Once the delay is found for a given configuration, it should be repeatable for a given channel configuration.

Output channels 1 and 2 of the DDC are routed through and latched by the FPGA using the DDC divided output clocks. As a result, when adjusting the DDC output data to DUC input timing using the SyncA delay, the timing of the DUC input data will only shift in steps of one divided clock cycle. To allow finer control for these channels, the polarity of the divided clock can be inverted from positive to negative, which results in a cycle shift in the DDC output data and DUC input timing. This is illustrated in the examples below.

There are two methods to find the proper DDC and DUC timing — either by observing the output signal with a spectrum analyzer or using an oscilloscope to directly monitor the DDC & DUC framestrobes, input clocks and data bits (LSB). The spectrum analyzer method is convenient as it does not require additional equipment, but can be tedious for larger decimation values. For a CIC decimation of > 8 (overall decimation of 16), it is recommended to use the oscilloscope method.
8.5  **Calibrating the Sync Delay Using an Oscilloscope**

For this example, the starting configuration example_200kHz_load_start_config.mat was loaded and the TSW4100 programmed using the instructions in Section 8.4. Make sure the setting for the Nyquist Zone is set to "2" before running this configuration. After configuring the TSW4100, verify that the “Real Time Delay” box is checked, which allows immediate update of the DDC to DUC delay without completely reprogramming the parts.

To calibrate each channel 1–4 corresponding to the DUC inputs A–D, oscilloscope probes should be connected to the appropriate frame strobe (AFS/BFS/CFS/DFS), DUC input clock (ACK/BCK/CCK/DCK) and the DUC input LSB (A0/B0/C0/D0). All these signals are available on test points near the DUC device (see Figure 55). The DUC input LSB test points are small pads and the input clock and frame strobe are loops.

Starting with Channel 1, connect 3 probes to AFS, ACK and A0. The oscilloscope display should look like this:
The traces are as follows: yellow = ACK, pink = AFS and blue = A0. In this case, with the default Channel 1 sync delay of 0, the data signal A0 comes 10.5 divided clock cycles too late, compared to the dashed cursor showing ideal timing. Since the data can only be delayed (not advanced) by the sync delay, and the total number of divided clocks for an AFS cycle is 16, delay the data 5.5 divided clock cycles. As discussed in Section 8.4, the sync delay will only result in delays that are integer multiples of the divided interface clock period. To align the timing, first delay the data by 6 divided clock cycles with an SCK ratio of 16, or $6 \times 16 = 96$ high speed clock cycles by setting the sync delay to 96 and pressing the sync button. This should result in a shifting of the data A0 to divided clock cycles after AFS, as shown in the oscilloscope display in Figure 57:

**Figure 56. Starting Interface Timing for Channel 1**
Figure 57. Channel 1 Interface Timing After a Sync Delay of 96

To backup the data clock cycles (again, this is only needed for channels 1 and 2, not 3 and 4, where the minimum delay step size is 1 divided clock cycle), change the SCK polarity for channel 1 to negative and resync. This should shift the data to the appropriate time as shown in the oscilloscope display in Figure 58.
Finally, to verify that a sync delay of 96 is repeatable, find the middle point of the sync delay setting that has the correct delay. For this board, the delay settings for 83 to 96 have the correct delay, so the final delay setting should be the mid-point of 90.

The timing for Channels 1 and 2 are identical, so if the decimation and filters are identical, the same setting should work for channel 2.

Channels 3 and 4 are easier to align, as the DUC data to DUC framestrobe delay can be controlled to 1 fast clock cycle. Using the default settings from the configuration file loaded previously and connecting the oscilloscope to CFS, CCK and C0, the user finds that the data is again out of timing alignment with the framestrobe (Figure 59):
By trial and error, it is determined that the ideal sync delay is 129, which results in the following oscilloscope display shown in Figure 60.
Figure 60. Channel 3 Interface Timing With a Sync Delay of 129

Note that the timing for channel 4 will be identical to channel 3 if the decimation and filter are the same. The user can now load the configuration file called configuration example_200kHz_load_final_config.mat, which will load the default sync delay values as mentioned above.

The oscilloscope method can also be used with much lower decimation rates. For example, with a total decimation of 6 and a SCK divider ratio of 2, Figure 61 and Figure 62 show examples of incorrect and correct interface timing:
Figure 61. Incorrect Interface Timing for a Decimation of 6 and SCK Divider Ratio of 2

Figure 62. Correct Interface Timing for a Decimation of 6 and SCK Divider Ratio of 2
8.6 Calibrating the Sync Delay Using an Spectrum Analyzer

The correct sync delay can be determined by looking at the TSW4100 output with a single input tone that is set slightly off center of the band center.

Consider the example presented in Section 8.5. In the interface settings, the interface clock ratio is set to 2:

![Interface settings diagram]

This means that two GC5016 input clock cycles (at 160 MHz) are used for 1 interface clock cycle (80 MHz). See the GC5016 Input Output Mode Application Note (SLWA037) for details on the interleave IQ interface.

For proper data transfer, align the DDC output and DUC input timing to look like Figure 62.

With a decimation/interpolation of 8, there are 8 possible phases between the DDC output data and DUC input timing. With the interface clock ratio of 2, I and Q are held for two input clock cycles. For the DUC input, the I latch and Q latch occur 2 input clock cycles apart. By adjusting the sync delay, find the appropriate timing for the channel. This is represented in Table 6, where each row is an input clock cycle and the 8 possible Sync phases of the DUC are shown.

<table>
<thead>
<tr>
<th>DUC Input</th>
<th>Phase 1</th>
<th>Phase 2</th>
<th>Phase 3</th>
<th>Phase 4</th>
<th>Phase 5</th>
<th>Phase 5</th>
<th>Phase 7</th>
<th>Phase 8</th>
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</thead>
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<tr>
<td>1</td>
<td>I latch</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>2</td>
<td>—</td>
<td>I latch</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<tr>
<td>3</td>
<td>Q latch</td>
<td>—</td>
<td>I latch</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>4</td>
<td>—</td>
<td>—</td>
<td>Q latch</td>
<td>—</td>
<td>I latch</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<tr>
<td>5</td>
<td>I</td>
<td>—</td>
<td>Q latch</td>
<td>—</td>
<td>I latch</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<tr>
<td>6</td>
<td>Q</td>
<td>—</td>
<td>Q latch</td>
<td>—</td>
<td>Q latch</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>7</td>
<td>Q</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Q latch</td>
<td>I latch</td>
</tr>
<tr>
<td>8</td>
<td>Q</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>I latch</td>
</tr>
</tbody>
</table>

The correct value of the sync delay is dependent on decimation, filter mode, filter length, etc. and is deterministic and repeatable. As is seen in Table 6, there are two phases that should be “good”. In this case, both I and Q are correctly transferred and a single tone in the spectrum above is observed. However, it cannot be predicted ahead of time. For the TSW4100 example above, a value 5 should be correct. However, a design flaw in the timing for the TSW4100 (there is board to board latency uncertainty in the crystal filter for the ADC) means some boards may have slightly different values – this will be corrected in a revised version.

As an example, consider the configuration described above with the decimation ratio is 8, with an input tone offset from the center of the channel. There are 4 phases where only I or Q are transferred (and swapped). Observing the output of these 4 phases, this results in two tones with 6 dB lower power:
And finally, there are 2 phases where neither I nor Q are transferred. In this case, there is no tone observed in Figure 64.
This may appear complicated, but the TSW4100 GUI eases the adjustment and finds the right setting. Note that each channel will require separate adjustment, even if the configurations are the same (this is because 2 channels are routed through the FPGA, which adds a set delay to the data).

Note that for the test, the input tone must be offset from the center of the filter and with the “Real Time Delay” box checked.

Changing the Sync Delay value in the interface box will enable the sync for that channel, send sync pulses to the DDC and DUC with a delay determined by the pull down menu, and then disable the sync.

If either 2 or 0 tones are observed, make sure “Real Time Delay” is checked and adjust the Sync Delay value until 1 tone is observed. At most, only the range of 1 to the decimation ratio need to be tried.

The same steps can be done using a network analyzer. In the case where neither I nor Q are transferred, there will be no signal in the network analyzer. If there is I or Q but not both, the gain will be 6 dB too low, except for a spike at the center as the two tones merge. When set properly, the output power will increase 6 dB.

8.7 Requirement for Nyquist Filtering for the ADC

Even high performance signal generators have harmonics at multiples of the output frequency. Unless a filter is used between the signal generator and the ADC to limit the passband to one Nyquist zone of the ADC (in this case 80 to 160 MHz), these harmonics can alias back into a passband and result in increase spurious output. This is shown in the two spectral plots for Figure 65. On the left, a filter is used for the 100 MHz tone, resulting in the highest spur is at –70 dBm. Without the input filter, the highest spur is at –56 dBm, or 14 dB worse.

![Figure 65. With and Without an ADC Filter to Remove Output Frequency Harmonics](image-url)
8.8 Adding Other Channels

Although the filter design example was for a single channel, it is easy to test multiple channels simultaneously. To enable the other channels, deselect the **OFF** check box in the Channel N Configure area. This setting is also saved as in the `C:\Program Files\Texas Instruments\TSW4100GUI\TSW4100example2_config.mat` example MATLAB settings file.

![Multiple Channel Configuration](image)

**Figure 66. Multiple Channel Configuration**

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**Note:** The center spacing and bandwidth should be chosen so that there is no overlap between channels, or else the channels output adds together, resulting in possible signal saturation.

To test the TSW4100 response across the entire Nyquist band (80–160 MHz), the input signal is swept from 80 to 160 MHz while the spectrum analyzer has a trace set to MAX HOLD (blue in **Figure 67**) and a trace set to clear/write (yellow). Clicking the **Configure** button generates the output (observed after allowing the sweep to complete).
8.9 Using Other Nyquist Zones

8.9.1 Third Nyquist Zone Example

The previous example used the 2nd ADC Nyquist Zone (80–160 MHz) for a 160 MSPS clock rate. Other Nyquist zones can be selected in the TSW4100GUI by using the Nyquist Zone drop-down list (Figure 68, under the TI Logo). Figure 68 and Figure 69 show the TSW4100GUI settings and TSW4100 output for a 3rd Nyquist Zone Example. This setting is saved as C:\Program Files\Texas Instruments\TSW4100GUI\TSW4100example3_config.mat and also on the provided CD. Make sure that the Nyquest Zone is set to "3" before running this example.
Figure 68. TSW4100GUI Settings to Generate Third Nyquist Zone

Figure 69. Third Nyquist Zone Example Output Spectrum
Appendix A  Firmware Downloading (if updates are needed)

The TSW4100 contains an Altera EP2C8 Cyclone II™ FPGA device (U10) and an Altera EPCS4 reprogrammable serial configuration device (U13). Upon power application or reset (SW4), the EPCS4 programs the FPGA. If firmware (other than what is delivered with the EVM) is used, either the EPCS4 or the FPGA can be reprogrammed through JTAG connector J14.

Reprogram the EPCS4 with these steps:
1. Connect an Altera ByteBlaster II™ parallel port download cable to J14. Ensure pin 1 of cable lines up with pin 1 of J14. Connect the other end to the PC parallel port.
2. Start the Altera Quartus II™ Programming software. The Quartus II application window displays as in Figure A-1.

![Figure A-1. Quartus II Programming Interface](image)

3. Click **Tools** icon.
4. Select **Programmer** option.
5. Ensure the **Mode** text box uses the **JTAG** selection.
6. Make sure **Hardware Setup** text box has the **ByteBlaster [LPT1]** selection. If not:
   a. Click the **Hardware Setup** text box in the top left-hand corner of the Quartus II application (Figure A-1).
   b. Click the **Add Hardware** button.
   c. In the **Currently selected hardware widow**, select **ByteBlasterMV[LPT1]**. The **Hardware Setup** window should look similar to Figure A-2.
   d. Click **Close**.
7. Click **Auto Detect**. The software should recognize the EP2C8 device, as shown in Figure A-3.
8. Click on the line with the device name to select it. Click **Delete**.
9. To load a new configuration, click **Add File** button.
10. Search for desired `filename.jic` file and double-click to select it.
11. Select the **Program/Configure** check box for both files.
12. Click the **Start** button.
Figure A-3. EP2C8 Device Detected

The software first erases the serial configuration PROM, loads it, and configures the FPGA. The progress indicator increases from 0% to 100%, indicating the configuration progress. Upon completion, LED D2 lights, indicating the FPGA is properly configured.

To reprogram the FPGA directly, repeat steps nine through 12, but use a *.sof file instead of a *.jic file. If power is cycled or reset switch SW4 is pressed, the *.sof file is over written by the *.jic file loaded inside the serial PROM.

Table A-1. JTAG Connector J14 Pinout

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<tr>
<th>Pin</th>
<th>Signal</th>
<th>I/O</th>
<th>Description</th>
<th>Pin</th>
<th>Signal</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
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<td>TCK</td>
<td>I</td>
<td>Clock</td>
<td>2</td>
<td>GND</td>
<td>–</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>3</td>
<td>TDO</td>
<td>O</td>
<td>Data from Device</td>
<td>4</td>
<td>VCC</td>
<td>I</td>
<td>System Power</td>
</tr>
<tr>
<td>5</td>
<td>TMS</td>
<td>I</td>
<td>JTAG State Machine Control</td>
<td>6</td>
<td>VCC</td>
<td>I</td>
<td>System Power</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>–</td>
<td>No Connect</td>
<td>8</td>
<td>NC</td>
<td>–</td>
<td>No Connect</td>
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<td>9</td>
<td>TDI</td>
<td>I</td>
<td>Data to Device</td>
<td>10</td>
<td>GND</td>
<td>–</td>
<td>Digital Ground</td>
</tr>
</tbody>
</table>
# Appendix B Bill of Materials

**Table B-1. TSW4100 Bill of Materials**

<table>
<thead>
<tr>
<th>Qty</th>
<th>Part Reference</th>
<th>Value</th>
<th>Manufacturer</th>
<th>Manufacturer's Part Number</th>
<th>Note</th>
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<td>A B C CCK D DCK</td>
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<td>N/A</td>
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It is important to operate this EVM within the input voltage range of 5 V to 6 V and the output voltage range of 0.0 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.
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