

# TSW3725EVM Evaluation Module

This document outlines the basic steps and functions that are required to ensure the proper operation of the TSW3725EVM evaluation module. This guide helps the user to quickly evaluate the performance of the TSW3725EVM TX, RX, and Feedback signal chain.

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Overview

# 1 Overview

The TSW3725EVM consists of the following components:

- TSW3725EVM board
- TSW3725 adaptor board
- USB cable

For evaluating the TX chain, the additional hardware requirements are:

• TSW3100EVM (includes 5-/6-V power supply, Ethernet cable, and Ethernet to USB adaptor)

For evaluating the RX or Feedback chain, the additional hardware requirements are:

• TSW1200EVM (includes 5-/6-V power supply and USB cable)



# 2 General Description

The TSW3725EVM is a small-cell basestation development platform. It provides two real receive paths, two complex transmit paths, and a shared real feedback path.



#### Figure 1. TSW3725EVM Block Diagram

The TSW3725 can be evaluated as a stand-alone board with the TSW3100EVM as a digital source board and the TSW1200EVM as a digital capture board. In this configuration, the TSW3725 adaptor board is required. A few of the possible configurations to evaluate this board in stand-alone are shown in Section 4.2 of this document.

General Description

### 2.1 TSW3725 and TSW32725 Adaptor Board



Figure 2. TSW3725EVM

Figure 2 shows the TSW3725 without RF shields over the Transmit (TX), Feedback (FB), and Receive (RX) signal chains. Shown in this figure are the locations for several connectors used to operate the TSW3725. The USB connector is used in Stand-Alone mode, which is described in following text. The J8 connector can either connect to the TSW3725 adaptor boards or the small-cell basestation platform (SCBP). The supply voltage can be connected from the 6-Vdc connector or the banana plug connectors shown in Figure 2, or it can be supplied directly form the TSW3725 adaptor or SCBP boards. The primary 30.72-MHz reference for the TSW3725 is supplied from the TSW3725 adaptor board or the SCBP. However, a connector option on the TSW3725 for a secondary reference is shown in Figure 2.



Figure 3. TSW3725 Rev-A Adaptor

Figure 3 shows the TSW3725 adaptor board. This board is used in the stand-alone configuration to connect the TSW3725 to the TSW3100 digital source board for TX evaluation and the TSW1200 digital capture board for RX and FB evaluation. This board was also designed to work with the TSW1400, which is both a digital source and a capture board. At the time of publication of this document, the TSW1400 has not been released to market.

# 2.2 TSW3725 – Stand-Alone Configuration



Figure 4. TSW3725 in Stand-Alone Configuration (TSW1200 Not Shown)

Figure 4 provides an example of the stand-alone configuration. In this figure, the TSW3725 adaptor board connects the TSW3725 to the TSW3100. In this mode, the 6-V power and a 30.72-MHz reference must be supplied to the TSW3725 adaptor board. Also in this mode, the TSW3725 requires a USB connection to configure the SPI interfaces of the TSW3725 components

# 3 Software Installation

For the TSW3725 stand-alone configuration, users must install the TSW3725EVM software, the TSW1200EVM software, and the TSW3100EVM software. The TSW1200EVM and TSW3100EVM software installation procedures are discussed in their respective user's guides. This section only discusses how to install the TSW3725EVM software.

# 3.1 Downloading TSW3725 Software and MATLAB<sup>™</sup> MCR 7.13 (MATLAB<sup>™</sup> Compiler Runtime)

- 1. Unzip file TSW3725 GUI and MCR INSTALLER.zip.
- 2. TSW3725 software is located in directory: TSW3725 GUI and MCR INSTALLER\TSW3725\_GUI\_EXE.
- 3. MATLAB<sup>™</sup> 7.13 MCR installer is located in directory: TSW3725 GUI and MCR INSTALLER\2010a\_MCR.

# 3.2 Installing FT245R Drivers

The TSW3725 uses the FT245R chip as the USB interface. If the FT245R D2XX drivers are not installed, the TSW3725 GUI will have the following error if the *Program All* button is selected.

- ??? Error using  $\rightarrow$  loadlibrary at 480
- There was an error loading the library "pathname\TSW3725\_GUI\_EXE\TSW3725\_GUI\_mcr\DLL\_drivers\tsw6011\_usb\_spi.dll"
- The specified module could not be found

In most cases, installing these drivers occurs automatically when the TSW3725 USB cable is connected to a computer and a TSW3725 that have been powered up. The latest version of the D2XX driver can also be found on the FTDI chip Web site (<u>http://www.ftdichip.com/Drivers/D2XX.htm</u>). From here, users can download the files and executables required.



Software Installation

# 3.3 Installing MATLAB<sup>™</sup> MCR 7.13 (MATLAB<sup>™</sup> Compiler Runtime)

- 1. Enter Directory: TSW3725 GUI and MCR INSTALLER\2010a\_MCR.
- 2. Select the file: MCRInstaller.exe. This starts the installation process.
- 3. Select desired language, and press OK.



4. When the following window appears, press Install.

InstallShield Wizard
MATLAB(R) Compiler Runtime 7.13 requires that the following requirements be installed on your computer prior to installing this application. Click OK to begin installing these requirements:
Status Requirement
Pending VCREDIST X86



5. The following box appears while installing

InstallShield ¥	Vizard	
	2	Preparing to Install
		MATLAB(R) Compiler Runtime 7.13 Setup is preparing the InstallShield Wizard, which will guide you through the program setup process. Please wait.
		Configuring Windows Installer
		Cancel

6. Select *Next* in the following three windows that follow.

Larry A.D.		MATLAD/D) Constitute 7.40 Total (Child (Record		
VIATLAB	Tustamer Information			
Compiler Runtime	The InstallShield(R) Wizard will install MATLAB(R) Compile Runtime 7.13 on your computer. To continue, click Next.	Please enter your information.		
	MATLAB and Simulink are registered trademarks of The MathWorks, Inc. Please see www.mathworks.com/trade	User Name:		
	for a list of other trademarks owned by The MathWorks, Other product or brand names are trademarks or register			
	traumans of their respective owners.	Texas Instruments, Inc		
	WARNING: This program is protected by copyright law ar international treaties. Copyright 1984-2010, The MathW Inc.			
The MathWorks				
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Click Next to install to this	folder, or click Change to install to a different folder.			
Install MATLAB(	R) Compiler Runtime 7.13 to:			
C:\Program File:	s\MATLAB\MATLAB Compiler Runtime\ Cha	ange		
cəliShield —				

7. Select *Install* in the following box; a new box appears that says installation will take several minutes.

MATLAB(R) Compiler Runtime 7.13	- InstallShield	Wizard	×
Ready to Install the Program			
The wizard is ready to begin installation	l.		
Click Install to begin the installation.			
If you want to review or change any of exit the wizard.	your installation	settings, click Back.	Click Cancel to
nstallShield			
	< Back	Install	Cancel

8. Select Finish.

MATLAB Compiler Runtime	InstallShield Wizard Completed		
	The InstallShield Wizard has successfully installed MATLAB(R) Compiler Runtime 7.13, Click Finish to exit the wizard.		
MThe MathWorks			

9. Installation is complete.

### 4 Hardware Overview

The TSW3725 hardware can be used in two modes:

- 1. SCBP mode: Small-cell basestation platform
- 2. Stand-Alone

Section 4.1 discusses how to convert the TSW3725 from SCBP mode to Stand-Alone mode.

Section 4.2 discusses the hardware connections required in Stand-Alone mode.

Section 4.3 discusses the power-up sequence required in Stand-Alone mode.



# 4.1 Converting From SCBP Mode to Stand-Alone Mode

Only one board modification is required to switch between SCBP mode and Stand-Alone mode. The switch 1 on SW2 determines if the TSW3725 is in SCBP or Stand-Alone mode.

### 1. Stand-Alone mode:

- (a) Push switch 1 on SW2 to the right, with respect to the following picture.
- (b) If board is powered, then LED D11 starts blinking and LED D14 should be off.

# 2. SCBP mode:

- (a) Push switch 1 on SW2 to the left, with respect to the following picture.
- (b) If board is powered, then LED D14 starts blinking and LED D11 should be off.



The TSW3725 does have two SPI settings updates when switching between modes. These are important to understand and perform, if the user is creating configuration files in Stand-Alone mode, and using this configuration file to program the SCBP in SCBP mode. These SPI settings are listed in the following table under default settings.

Stand-Alone Mode					
TSW3725 GUI	Comments				
GC5330/TSW3100 CLK pulldown menu	Set to /8	TSW3100 clock rate determined by DAC3484 interpolation rate and DDR clock TSW3725 default DAC3484 interpolation setting = 4x; set clock rate = 1/(interpolation setting *2); the *2 is due to DDR clock			
DAC3484 config 2, addr 02, bit 16 (MSB)	Set to 1	TSW3100 requires word wide mode			
SCBP Mode					
TSW3725 GUI Default Setting Comments					
GC5330/TSW3100 CLK pulldown menu	Set to /2	GC5330 requires data clock equal to half the DAC data rate			
DAC3484 config 2, addr 02, bit 16 (MSB)	Set to 0	GC5330 on SCBP requires byte-wide mode			

# 4.2 Hardware Setup and Connections – TSW3725 Stand Alone Configuration

The purpose of this section is to assist the user to set up the TSW3725 hardware quickly, using the TSW3100 digital source board and TSW1200 digital capture board. This document assumes that the user has familiarity with the TSW3100 and TSW1200 hardware and software, or that the user has access to the TSW3100 and TSW1200 EVM user's guides for TSW3100- or TSW1200-specific issues. Both user's guides are available on the TI Web site (www.ti.com).

When using the TSW3100 and TSW1200, the TSW3725 can be configured to run in almost any variety of measurement configurations as shown in the following illustration. To capture the feedback path and the RX path simultaneously with multiple TSW1200s, a second computer is required.

















### 4.3 Power-Up Sequence

This section provides the order in which to connect and power up the TSW3725, TSW3100, and TSW1200 hardware. Depending on the user's desired configuration, some of the following optional sections can be disregarded.

Section A: Required:- this section is used for all TSW3725 Stand-Alone measurements.

Section B: Optional:- required to evaluate the TX Path.

Section C: **Optional:**– required to evaluate the Feedback Path.

Section D: Optional:- required to evaluate the RX Path.

#### **Section A. Required Connection:**

This section describes how to connect the TSW3725 to the TSW3725 Adaptor board.

- 1. Connect TSW3725 connector J8 to TSW3725 Adaptor board connector J1.
- 2. Connect TSW3725 to a 6-V/4-A supply via any of the three following options.
  - (a) Option 1: TSW3725 Adaptor board connector J3 (+6V\_IN)
  - (b) Option 2: TSW3725 connector J5
  - (c) Option 3: TSW3725 banana plugs J7 (GND) and J6 (6 V)
- 3. Verify the following LEDs are lit on the TSW3725.
  - (a) D1 6 Vdc: green D2: CDC\_STATUS: green
  - (b) D6: FPGA CONFIG: green
  - (c) D10: USB POWER: blue
  - (d) D11: green (blinking), if D14 is blinking instead, then refer to Section 4.1.
- 4. Connect a 30.72M reference to TSW3725 Adaptor board connector J2.
  - (a) Refin Input amplitude can range from 0.2 Vpp 3.3 Vpp



### Section B. Optional Connection: TX Path Digital Source

This section describes how to connect the TSW3100 to the TSW3725 Adaptor board to evaluate the TSW3725 TX paths. A detailed explanation for the TSW3100 setup is described in the TSW3100EVM guide, which is available on the TI Web site (www.ti.com)

- 1. Connect TSW3725 Adaptor board connector J4 to TSW3100 connector J74.
- 2. Connect TSW3100 connector J9 (5V\_IN) to a 5-V or 6-V supply.
- 3. Set TSW3100 SW1 (BRD\_PWR) to ON.
- 4. Verify the following LEDs are illuminated on the TSW3100.
  - (a) D3: green
  - (b) D4: green
  - (c) D5: green
  - (d) D6: green
  - (e) D11 FPGA CONFIG: orange
  - (f) D13 PAT GEN IDLE: orange
  - (g) D18 LVDS PLL LOCK: orange
  - (h) D19 DDR2 PLL LOCK: orange
  - (i) D20 NIOS PLL LOCK: orange
  - (j) D25 STATUS 1: orange
  - (k) D26 STATUS2: orange
- 5. Connect TSW3100 J13 Ethernet connector to the Ethernet cable; connect Ethernet cable to computer directly or through an Ethernet/USB adaptor.
- 6. Verify orange and green LEDs near J13 are illuminated.
- 7. See TSW3100 High Speed Digital Pattern Generator user's guide (SLLU101) for a detailed explanation on how to set the TSW3100 IP address

#### Section C. Optional Connection: Feedback Path Capture

This section describes how to connect the TSW1200 to the TSW3725 Adaptor board to evaluate the TSW3725s Feedback path. See *TSW1200EVM: High-Speed LVDS Deserializer and Analysis System* user's guide (SLAU212) for a detailed explanation for the TSW1200 setup.

- 1. Connect TSW3725 Adaptor board connector J10 to TSW1200 connector J9.
- 2. Connect 5-V supply to TSW1200 banana plugs J14 (GND) and J15 (+5 V).
- 3. Verify that the following LEDs are illuminated on the TSW3100.
  - (a) D1: blue
  - (b) D2: blue (blinks)
  - (c) D4: blue (blinks)
  - (d) D7: blue
  - (e) D16: green
- 4. Connect TSW1200 USB port J8 to USB cable; connect USB cable to computer.

### Section D. Optional Connection: RX Path Capture

This section describes how to connect the TSW1200 to the TSW3725 Adaptor board to evaluate the TSW3725s RX paths. See *TSW1200EVM: High-Speed LVDS Deserializer and Analysis System* user's guide (SLAU212) for a detailed explanation for the TSW1200 setup.

- 1. Connect TSW3725 Adaptor board connector J6 to TSW1200 connector J9.
- 2. Connect 5-V supply to TSW1200 banana plugs J14 (GND) and J15 (+5 V).
- 3. Verify that the following LEDs are illuminated on the TSW3100.
  - (a) D1: blue
  - (b) D2: blue (blinks)
  - (c) D4: blue (blinks)
  - (d) D7: blue
  - (e) D16: green
- 4. Connect TSW1200 USB port J8 to USB cable; connect USB cable to computer.

# 4.4 Power-Down Sequence

- 1. If used, turn off TSW3100 power using SW1.
- 2. Disconnect power to TSW3725EVM.
- 3. If used, disconnect power to the TSW1200EVM.

# 5 Quick Setup

This section assumes that the hardware setup was completed in Section 4 and that the hardware is powered up. The goal of this section is to provide the user a quick setup procedure to start the software and evaluate a simple single tone signal by using the TSW1200 and/or the TSW3100. This allows users to become familiar with all the software and hardware components required to use the TSW3725 hardware.

Section 6 discusses more complex waveforms and the related setup. Section 7 discusses the TSW3725 GUI in detail.

# 5.1 Starting the TSW3725 GUI Software

- 1. Ensure that TSW3725 hardware connections are completed as discussed in Section 4.
- 2. Start TSW3725 GUI by selecting the file TSW3725\_GUI.EXE. This file resides in the directory TSW3725 GUI and MCR INSTALLER\TSW3725\_GUI\_EXE..



Figure 8. TSW3725\_GUI.exe

3. The GUI appears as shown in Figure 9

Quick Setup



W3725 Canfiguration Control Load itrom File Program A1 CUSTOM TX1 CUSTOM TX1 TX2 TX2 FB CUSTOM TX1 TX2 FB FC CUSTOM TX1 TX2 FB FC CUSTOM TX1 TX2 FB FC CUSTOM TX1 TX2 FB FC CUSTOM TX1 TX2 FB FC CUSTOM TX1 TX2 FB FC CUSTOM TX1 TX2 FB FC CUSTOM TX1 TX2 FB FC CUSTOM TX1 TX2 FC CUSTOM TX1 FC CUSTOM TX1 FC FC CUSTOM TX1 FC CUSTOM TX1 FC CUSTOM TX1 FC CUSTOM TX1 FC CUSTOM TX1 FC FC CUSTOM TX1 FC FC CUSTOM TX1 FC FC CUSTOM TX1 FC FC CUSTOM TX1 FC FC CUSTOM FC FC CUSTOM TX1 FC FC CUSTOM TX1 FC FC FC CUSTOM FC FC FC FC FC FC FC FC FC FC	and the second		_
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C Log SPI       Custom TX       TX2       FB       Cutot       TX2       FB       Cutot       C	Load from File Program A		
Jocks - COCCF2019       WHz       Output Dividers       Output Frequency       Output Dividers       Output Di	C Low CDL		
Jocks - CDCE72019       Output Dividers       Output Dividers       Output Frequency       Output Prequency       NA       NA         REF OPT       GCS3300/TSW3100 CLK       NA       REFOUT1       NA       NA         REF IN FREO       MHiz       TX-DAC CLK       NA       NA       ADDR       DATA         NA       FB-ADC CLK       NA       NA       ADDR       DATA         NA       REF IN FREO       Miz       REF IN FREO       NA       ADDR       DATA         TV20-1       L0 (MHz)       REF IN       see CDCE72010 FPOA, 3720 REF       ADDR       DATA       Mode       Image: Comparison of	Log SPI		108 - Contra 10
VCKO  REF OPT  Mitz  FPCA, 3720 REF  PCAA, 3720 REF  NA  REF OUT  REF IN FREC  Mitz  Tx-DAC CLK  NA  ADDR DATA  REFOUT  NA  REFOUT  REFIN  REFOU  REFIN  REFOU  REFN  REFOU  REFN  REFOU  REFN  REFOU  REFN	ocks - CDCE72010		4 European
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FB-ADC CLK • NA   Rx and Feedback   TRF3720-1   LO (MHz)   PFD (MHz)   REF IN   see CDCE72010 FPGA, 3720 REF   ADDR   DATA   MXNNO   •   DAC3484   GMC   •   Interpolation   •   TX Attenuation   Feedback Path   Peedback Path   See CDCE72010 FPGA, 3720 REF   ADDR DATA NCO freq (MHz) NA NA NA NA NCO 1 NCO2 NCO2 NCO4 NCO4 NCO2 NCO4 NCO4 NCO2 NCO4	MHz	TX-DAC CLK	
RX-ADC CLK     NA       TX and Feedback       TRF3720-1       LO (MHz)       PFD (MHz)       REF IN       see CDCE72010 'FPGA, 3720 REF'       ADDR       DAC3484       GMC       Interpolation       *       ADDR       DATA       MIXING       *       *       ADDR       DATA       MIXING       * <t< td=""><td>arged the events meetin manually</td><td>FB-ADCICLK NA</td><td></td></t<>	arged the events meetin manually	FB-ADCICLK NA	
Tx and Feedback   TVF3726-1   LO (MHz)   PFD (MHz)   REF IN   see CDCE72010 'FPGA, 3720 REF'   ADDR DATA Mode    OAC3484   GMC   Inderstand   GMC   Inderstand   REF IN   see CDCE72010 'FPGA, 3720 REF'   Inderstand   Inderstand   Interpolation   TX Aftenuation   TX Aftenuation   TX Aftenuation   TX Aftenuation   Feedback Path   Feedback Path   Gabro Feedback Path Gein   GB   ADDR   DATA   Mode   PGA870 Feedback Path Gein   GB   PGA870 Rx1 Path Gein   GB   PGA870 Rx2 Path Gein   GB   PGA870 Rx2 Path Gein   GB   ADSP DX2 Path Gein   GB	regentrite COC's M.M. H disden	RX-ADC CLK	
TRF3720-1       LO (MHz)       REF IN       see CDCE72010 'FPGA, 3720 REF'       ADDR       DATA       Mode       -         DAC3484       Input/View GMC Settings       Restore GMC Defaults       Fine Mixing         MXING       -       -       NCO1       NCO2         MXING       -       -       NCO1       NCO2         FIFO       -       ADDR       DATA       NCO1       NCO2         FIFO       -       ADDR       DATA       NCO1       NCO2         Interpolation       -       -       ADDR       DATA       NCO1       NCO2         TX Attenuation       -       -       ADDR       DATA       PhaseAdd(0x)       NA       NA         Feedback Path       - <t< td=""><td>x and Feedback</td><td></td><td></td></t<>	x and Feedback		
ADDR DATA Mode  ADDR DATA NCO1  NCO1  NCO2  FIFO  ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR DATA NCO1 NCO2  FIFO ADDR ADDR ADDR ADDR ADDR ADATA NCO1 NCO2  FIFO ADDR ADDR ADDR ADDR ADDR AD  NCO1 NCO2 FIFO ADDR ADDR ADDR ADDR AD  NCO1 NCO2 FIFO ADDR ADDR ADDR ADDR AD  NCO1 NCO2 FIFO ADDR ADDR ADDR AD  NCO1 NCO2 FIFO ADDR ADDR ADDR AD  NCO1 NCO2 FIFO ADDR AD  NCO1 NCO2 FIFO ADDR ADDR AD  NCO1 NCO2 FIFO ADDR ADDR AD  NCO1 NCO2 FIFO AD  N	_ TRF3720-1		
PFD (MHz)       REF IN       see CDCE72010 FPGA, 3720 REF         DAC3484       Fine Mixing         GMC       Input/View QMC Settings       Restore QMC Defaults       Fine Mixing         MIXING       Imput/View QMC Settings       Restore QMC Defaults       Fine Mixing         FIFO       Imput/View QMC Settings       Restore QMC Defaults       Fine Mixing         FIFO       Imput/View QMC Settings       Restore QMC Defaults       Fine Mixing         FIFO       Imput/View QMC Settings       Restore QMC Defaults       Fine Mixing         FIFO       Imput/View QMC Settings       Restore QMC Defaults       Fine Mixing         FIFO       Imput/View QMC Settings       Restore QMC Defaults       Fine Mixing         FIFO       Imput/View QMC Settings       DATA       NCO1       NCO2         FIFO       Imput/View QMC Settings       DATA       PhaseAdd(0x)       NA       NA         Interpolation       Imput/View QMC Settings       Imput/View QMC Settings       Imput/View QMC Settings       PhaseAdd(0x)       NA       NA         TX Attenuation       Imput/View QMC Settings         Feedback Path       Gath <td>LO (MHz)</td> <td>ADDR DATA Mode</td> <td>-</td>	LO (MHz)	ADDR DATA Mode	-
DAC3484.       Fine Mixing         QMC       Input/View QMC Settings       Restore QMC Defaults       FDAC       NA         MIXING       Input/View QMC Settings       Restore QMC Defaults       FDAC       NA         MIXING       Interpolation       Interpolation       NCO1       NCO2         FIFO       Interpolation       Interpolation       Interpolation       Interpolation       Interpolation         Tx Attenuation       TX1 ATTN       dB       TX2 ATTN       dB       Attenuation regis       D255 stops         Feedback Path       Feedback Path       ADSR       ADSR       DATA       ADDR       DATA         PGA870 Feedback Path Gain       dB       Attenuation regis       ADDR       DATA       DATA         PGA870 Feedback Path Gain       dB       Attenuation regis       ADDR       DATA         PGA870 Feedback Path Gain       dB       Attenuation regis       ADDR       DATA         PGA870 Feedback Path Gain       dB       Attenuation regis       ADDR       DATA         PGA870 Rx1 Path Gain       dB       FOAd570 pass regis       ADDR       DATA         PGA870 Rx2 Path Gain       dB       FOAd570 pass regis       ADDR       DATA	PFD (MHz)	REF IN see CDCE72010 'FPGA, 3720 REF'	
DAC 3484       Input/View QMC Settings       Restore QMC Defaults       Fine Mixing         MIXING       Interpolation			
CMC       Input/view CMC Settings       Restore CMC Defaults       FDAC       NA         MIXING       •       •       NCO1       NCO2         FFO       •       ADDR       DATA       NCO1 freq (MHz)       NCO2         Interpolation       •       •       PhaseAdd(0x)       NA       NA         Interpolation       •       •       PhaseAdd(0x)       NA       NA         Tx Aftenuation       •       •       •       •       •       •         Tx Aftenuation       •       •       •       •       •       •         Feedback Path       •	- DAC3484	Eine L	living
MIXING ADDR DATA NCO1 NCO2 FIFO ADDR DATA NCO1 NCO2 NCO1 NCO2 N	GIMC Iniput	Internet in the second device and	winking
FIFO       •       ADDR       DATA       NCO freq (MHz)       NA       NA         Interpolation       •       PhaseAdd(0x)       NA       NA       NA         Tx Attenuation       •       PhaseOffset(0x)       •       NA       NA         Tx Attenuation       •       •       •       •       •       •         Tx Attenuation       •       •       •       •       •       •       •         Feedback Path       •       •       •       •       •       •       •       •       •       •       •         Feedback Path       • <td>MIXING -</td> <td>* NCO1</td> <td>NCO2</td>	MIXING -	* NCO1	NCO2
FIFO Interpolation   Interpolation   Tx Attenuation   B Tx 2 ATTN   B Tx 2 ATTN   B Attenuation   Feedback Path   Feedback Path   Feedback Path Selection   PGA870 Feedback Path Gain   B Attenuation   C (MHz)   PFD (MHz)   REF IN   see CDCE72010 'FPGA, 3720 REF'   ADDR   DATA   Mode   PGA870 Rx2 Path Gain   B Attractor renge   ADDR   DATA		NCO freq (MHz)	
Interpolation       Image: Contract of the second sec	FIFO	ADDR DATA	NIA
PhaseOffset(0x)         Tx Attenuation         Tx Attenuation         TX ATTN       dB       Attenuation       Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2"         Feedback Path         Feedback Path Selection       Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2"       Colspan="2"        Colspan="2"       Colspan="2"          Colspan="2"			ne
Tx Attenuation         Tx1 ATTN       dB       Tx2 ATTN       dB       Attenuation range Ddf is 51.7558 in D.2565 steps         Feedback Path       Feedback Path Selection       Image: Control of the	Interpolation	PhaseAdd(Ux) NA	NA
TX1 ATTN       dB       TX2 ATTN       dB       Attenuation range Ddf to 51.75d0 in 0.25d5 dags         Feedback Path       Feedback Path Selection       •       ADDS41xx/ADS5681x Register         PGA870 Feedback Path Gain       •       PM4670 gab range       ADDR       DATA         PGA870 Feedback Path Gain       •       •       •       •       •         PGA870 Feedback Path Gain       •       •       •       •       •       •         PGA870 Feedback Path Gain       • <td< td=""><td>Interpolation</td><td>PhaseAdd(Ux) NA PhaseOffset(0x)</td><td></td></td<>	Interpolation	PhaseAdd(Ux) NA PhaseOffset(0x)	
Feedback Path       ADS41xx/ADS58B1x Register         Feedback Path Selection       Image: Selection and the selectio	Interpolation	PhaseAdd(Ux) NA PhaseOffset(0x)	
Feedback Path         Feedback Path Selection         PGA870 Feedback Path Gain       Colspan="2">ADDR       DATA         PGA870 Feedback Path Gain       Colspan="2">Colspan="2">ADDR       DATA         PGA870 Feedback Path Gain       Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2">Colspan="2"         PGA870 Feedback Path Gain       Colspan="2">Colspan="2"       ADDR       DATA         PGA870 Feedback Path Gain       Colspan="2">Colspan="2"       Colspan="2">Colspan="2"         TRF3720-2         LO (MHz)       DATA       Mode         PFD (MHz)       REF IN see CDCE72010 'FPGA, 3720 REF'       ADDR       DATA         PGA870 Rx1 Path Gain       dB       MODE ODE ODE ODE ODE ODE ODE ODE ODE ODE	Interpolation	PhaseAdd(Ux) NA PhaseOffset(0x)	
ADS41xx/ADS5681x Register       PGA870 Feedback Path Gain     MB     It Sch to 20d to 350 steps     ADDR     DATA       PGA870 Feedback Path Gain     dB     It Sch to 20d to 350 steps     DATA       TRF3720-2     LO (MHz)     REF IN     see CDCE72010 'FPGA, 3720 REF'     ADDR     DATA       PFD (MHz)     REF IN     see CDCE72010 'FPGA, 3720 REF'     ADDR     DATA       PGA870 Rx1 Path Gain     dB     F04870 gasn renge     ADS42xx/ADS58C2x Register       PGA870 Rx2 Path Gain     dB     F04870 gasn renge     ADDR     DATA	Interpolation Tx Attenuation TX1 ATTN dB	TX2 ATTN dB Attenuation range bat to 31 7545 in 0.2545 abpa	
PGA870 Rx2 Path Gain dB PGA870 Rx2 Path Gain dB dB th Set to 2000 th 0 550 steps	Interpolation Tx Attenuation TX1 ATTN Feedback Path	TX2 ATTN dB Attenueton range Det to 31.7545 in 0.2545 about	
PGA870 Feedback Path Gain     dB     -11 5x8 to 20x8 to 0.5x8 to 0.	Interpolation TX Attenuation dB TX1 ATTN dB Feedback Path Feedback Path Selection	TX2 ATTN dB Attenueton rege Det to 51.7545 in 0.2545 steps	
TRF3720-2     LO (MHz)       PFD (MHz)     REF IN see CDCE72010 'FPGA, 3720 REF'       PR Path       PGA870 Rx1 Path Gain     dB       PGA870 Rx2 Path Gain     dB	Interpolation TX Attenuation B TX1 ATTN B Feedback Path Selection	TX2 ATTN B Attenueton rege Det to 51.7555 in 0.2545 dags  ADS41xx/ADS58B1x Register  ADDR DATA	
TRF3720-2	Interpolation TX Attenuation Attenuation Attenuation Attenuation Attenuation Attenuation Attenue Atten	TX2 ATTN dB Attenueton rege 0x8 to 31 75x8 in 0.25x8 dags  ADS41xx/ADS58B1x Register ADDR DATA  dB 41 5x8 tri0 5x8 tri0 5x8 trigge	
LO (MHz) PFD (MHz) REF IN see CDCE72010 'FPGA, 3720 REF' PGA870 Rx1 Path Gain PGA870 Rx2 Path Gain B COASTO gash range ADS42xx/ADS58C2x Register ADDR DATA ADDR DATA ADDR DATA ADDR DATA	Interpolation TX Attenuation TX1 ATTN Market dB Feedback Path Feedback Path Selection PGA870 Feedback Path Gain	PhaseAdd(0x)     NA       PhaseOffset(0x)     PhaseOffset(0x)       TX2 ATTN     dB     Attenuation range (bit to 51.7555 in 0.2555 steps)       ADS41xx/ADS58B1x Register     ADDR     DATA       B     41 5d5 to 20d5 in0 5d5 steps     Image: Color of the col	
PFD (MHz) REF IN see CDCE72010 'FPGA, 3720 REF' ADDR DATA Wode ADDR PGA870 Rx1 Path Gain B POARD gas range ADS42xx/ADS58C2x Register ADDR DATA	Interpolation TX Attenuation Attenuation Attenuation Attenuation Attenuation Attenuation Attenue Atten	PhaseAdd(0x)     NA       PhaseOffset(0x)     PhaseOffset(0x)       TX2 ATTN     dB     Attenuation range 0x8 to 31 75x8 in 0.25x8 dags       ADS41xx/ADS58B1x Register     ADS41xx/ADS58B1x Register       ADDR     DATA       adB     -11 5x8 in 0.25x8 in 0.25x8	
PGA870 Rx2 Path Gain dB H1 560 to 2000 to 560 targe ADS42xx/ADS58C2x Register ADDR DATA	Interpolation TX Attenuation TX1 ATTN dB Feedback Path Feedback Path Selection PGA870 Feedback Path Gain REF3720-2 LO (MHz)	TX2 ATTN  B A A B A A B A B A B A B A B A B A B	
PGA870 Rx1 Path Gain     dB     ADS42xx/ADS58C2x Register       PGA870 Rx2 Path Gain     dB     11 550 to 2000 in 0.550 three     ADDR	Interpolation		
PGA870 Rx1 Path Gain dB POARD gas range ADS42xx/ADS58C2x Register PGA870 Rx2 Path Gain dB 411 590 to 2000 in 0.500 three	Interpolation	PhaseAdd(0x)       NA         PhaseAdd(0x)       NA         PhaseOffset(0x)       MaseAdd(0x)         TX2 ATTN       dB       Attenuation range 0x8 to 31 75x8 in 0.25x8 steps         ADS41xx/ADS58B1x Register       ADDR       DATA         Mode       ADDR       DATA       Mode         REF IN       see CDCE72010 FPGA, 3720 REF'       ADDR       DATA       Mode	
PGA870 Rx2 Path Gain dB d1 560 to 300 in 0.560 steps ADDR DATA	Interpolation TX1 ATTN dB TX1 ATTN dB Feedback Path Selection PGA870 Feedback Path Gain PGA870 Feedback Path Gain RF3720-2 LO (MHz) PFD (MHz)	PhaseAdd(0x)       NA         PhaseOffset(0x)       PhaseOffset(0x)         TX2 ATTN       dB       Attenuation range 0x8 to 31 75x8 in 0.25x8 dags         ADS41xx/ADS58B1x Register       ADDR       DATA         dB       -11 5x8 in 0.25x8 dags       DATA         MB       -11 5x8 in 0.25x8 dags       DATA         MB       -11 5x8 in 0.5x8 dags       DATA         MOde	
PGA870 Rx2 Path Gain dB 411 add to 2006 in Usable street	Interpolation TX1 ATTN dB TX1 ATTN dB Feedback Path Selection PGA870 Feedback Path Gain REF3720-2 LO (MHz) PFD (MHz) RX Path PGA870 Rx1 Path Gain	PhaseAdd(Ux) NA PhaseOffset(0x) TX2 ATTN dB Attenuation angle Diff to 51 7555 in 0.2555 steps ADS41xx/ADS58B1x Register ADDR DATA ADDR DATA Mode REF IN see CDCE72010 FPGA, 3720 REF' ADS42xx/ADS58C2x Register	
	Interpolation	TX2 ATTN  dB  Attenueton renge  D  ADS41xx/ADS58B1x  Register  ADDR  D  ATA  Mode  dB  dB  dB  dB  Att Stdt to 20x81 ind Stdt steps  dB  ADDR  D  ATA  Mode  dB  dB  ADS42xx/ADS58C2x  Register  ADDR  D  AD  AD  AD  AD  AD  AD  AD  A	

Figure 9. TSW3725 GUI at Start-Up

### 5.2 Load the Default TSW3725 Configuration

- 1. Select the yellow *Program All* button to program the recommended default settings to the TSW3725. Default settings are set up for Band 1 LTE and Band 1 WCDMA.
  - (a) After the yellow *Program All* button is selected, it turns white and makes text updates as to which section of the board is being programmed.
  - (b) This procedure takes approximately 25 seconds to complete.

**NOTE:** If the following error appears in the cmd tool window that appears with the TSW3725 GUI, then see Section 3 about installing the FT245 drivers.

??? Error using → loadlibrary at 480 There was an error loading the library "pathname\TSW3725\_GUI\_EXE\TSW3725\_GUI\_mcr\DLL\_drivers\tsw6011\_usb\_spi.dll" The specified module could not be found



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2. When programming is complete, the TSW3725 GUI appears as Figure 10 shows.

TSW3725_GUI	
5W3725	
Configuration Control	Master Power Enable/Disable
default_config.m	MAIN ALL ON-reset *
Load from File Program All	CUSTOM TX1 ON + TX2 ON + FB ON + RX1 ON + RX2 ON +
Save Config C Log SPI	
Clocks - CDCE72010	
VCXO 614.4 * MHz	Output Dividers Output Frequency Output Dividers Output Frequency
REF OPT Primary	FPGA, 3720 REF 20 - 30.72MHz REFOUTI OFF OFF
REF IN FREQ 20.72	5330/TSW3100 CLK 18 - 76.8MHz REFOUT2 OFF - OFF
MHZ MHZ	TX-DAC CLK
hanged the star sill energits that solid	FB-ADC CLK /3 * 204.8MHz 0 0000000 RD WR DISPLAY
properties LOC's P. M. H. Bieders	RX-ADC CLK /3 204.8MHz
fx and Feedback	
LO (MHz) 1990	
PFD (MHz) 15.36	ADDR DATA Mode Practional
	Reg0 1 0000000 RD VVR DISPLAY
DAC3484	
QMC ON <u> </u>	iew QMC Settings Restore QMC Defaults Fine Mixing
MIXING Coarse + 4Es(4	FDAC NA: Coarse
	NCO1 NCO2
FIFO ON *	ADDR DATA
Interpolation 4x -	00 0000 RD WR DISPLAY PhaseAdd(Ux) NA Coarse NA Coarse
	PhaseOffset(0x) 0000 0000
Tx Attenuation	
TX1 ATTN 31.75 dB	TX2 ATTN 31.75 dB Attenue to the to in 75 Em 0.25 Exten
Eandback Bath	
Feedback Path Selection	FF AUS41xx/AUS58B1x Register
DO 1970 Faculturali Dalla Onia	
PGA670 Peedback Path Gain	UU UU RD VVR DISPLAY
tx	
_ TRF3720-2	
PED (MHz) 45 26	ADDR DATA Mode Fractional
11 D (MILE)   13.30	REF IN See CDCE72010 FPGA, 3720 REF Reg0 7 0000000 RD WR DISPLAY
Rx Path	
PGA870 Rx1 Path Gain -11.5	dB ADS42xx/ADS58C2x Register
instanting and and	ADDR DATA
PGA870 Rx2 Path Gain -11.5	

Figure 10. TSW3725 GUI After Load is Complete

- 3. When programming is complete, verify that the following LEDs on the TSW3725 HW are illuminated. If they are, then the TSW3725 was programmed correctly. If they are not, then start over at step 1.
  - (a) D3 POLLOCK: green (confirms CDC chip is locked)
  - (b) D4 LD: green (confirms TRF3720 for TX and Feedback paths is locked)
  - (c) D5 LD: green (confirms TRF3720 for RX path is locked. Note: on Rev A hardware, this LED is under the RX RF Shield; this LED was moved outside of the RX RF Shield on Rev B hardware.)

### 5.3 TX Path: TSW3100 Software Setup – Single Tone Example

For a detailed explanation for the TSW3100 setup, see *TSW3100 High Speed Digital Pattern Generator* user's guide (<u>SLLU101</u>).

 From the TI Web site, download and install the TSW3100EVM GUI v2.7 or later version. Earlier versions of the TSW3100EVM GUI software do not support the DAC3484 input data format that is required to run the TSW3725.



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- www.ti.com
- 2. Load the TSW3100\_MultitonPattern\_v2p7 GUI, and program the following settings to run a single tone at 5 MHz with the default settings of the TSW3725 GUI.
  - (a) Signal Characteristics
    - (i) Sample Rate: 153.6
    - (ii) Back off: 0.99
    - (iii) Resolution: 16
    - (iv) Vector size: 2^15
  - (b) Signal Type
    - (i) Complex
  - (c) Tone Groups
    - (i) Select Group 1.
    - (ii) Tone BW = 1
    - (iii) # = 1
    - (iv) Tone Center = 5
    - (v) Gain(dB) = 0
  - (d) TSW3100 Control
    - (i) Select *master*.
    - (ii) Select 16b QDAC.
    - (iii) Select Two's Comp.
    - (iv) Select Load and Run.
    - (v) Select 16b MSB Justify.
    - (vi) Ensure IP setting is correct (see SLLU101).
- 3. The TSW3100 appears as shown in Figure 11.

TEXAS	153.6 Sample 0.99 Backoff	Rate (MSPS) 16 32768	Resolution	Random Seed Invert			Γe	xternal Fig	ure		
Fone Groups Enable Tone EV	₩ # Tone	Signal Type Complex Swea IG Since Correct Data Band DAC FM 1 DAC Inter Center Gain (dB) 5 0	0.8 Real 0.6 2.4 2.5 2.5 2.5 2.5 2.5 2.5 2.5 2.5								
Group 1 1	1	01 0	o l	0.1	0.2	0.3 0.4	0.5	0.6	0.7	0.8	0.9
Group 1 1	1	01 0	00 TSW3100	0.1 Control	0.2	0.3 0.4	0.5	0.6	0.7	0.8	0.9
Group 1 1 Group 2 1 Group 3 1			TSW3100 (* master (* slave	0.1 Control C LVDS C CMOS C BWDDR	0.2	0.3 0.4	0.5 s Comp et Bin	8.0 6.0 50 도 Friter	0.7	0.8	0.9 Star

Figure 11. TSW3100 GUI



4. Click on the green button *Create and Save/Run TSW3100*, when the TSW3100 is finished. The TSW3100 appears as shown in Figure 12.



Figure 12. TSW3100GUI After Waveform Created

- 5. Verify that the following TSW3100 LEDs are illuminated. If these LEDs are not, verify that the TSW3725 is connected properly and its default settings are loaded,
  - (a) D14: PAT GEN CLK
  - (b) D15: PAT GEN RUN
- 6. If TSW3100 LED D16: FIFO EMPTY ERROR is illuminated, then the TSW3100 did not load correctly and step 4 needs to be repeated. If this continues, then power cycle the TSW3100 board before repeating step 4.
- 7. Ensure that the TSW3725 hardware is programmed with the *default\_config.m* file.
- 8. The TSW3725 TX1 or TX2 output with these settings have roughly a -25-dBm signal at 2148.6. This can be calculated by the following equation.
  - (a) LO frequency = 1990 MHz
  - (b) Coarse mixer = Fs/4 = 614.4/4 = 153.6 Hz
  - (c) Tone center in TSW3100 GUI = 5 MHz
  - (d) Equation = LO frequency + coarse mixer + tone center = 1990 MHz + 153.6 MHz + 5 MHz = 2148.6 MHz



#### Quick Setup

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# 5.4 Feedback Path: TSW1200 Software Setup – Single Tone Example

A detailed explanation for the TSW1200 setup is described in the user's guide <u>SLAU212</u>.

- 1. From the TI Web site, download and install the TSW1200GUI-SW v2.5 or later version.
- 2. Load TSW1200\_v2p5 or later. The TSW1200 GUI appears as shown in Figure 13.



Figure 13. TSW1200 GUI

- 3. The text box in the bottom left states *TSW1200 found on COM3*. If the text box does not state this, then type CTRL+SHIFT+I. If that des not work, then power cycle the TSW1200 and type CTRL+SHIFT+I.
- 4. From the *TI ADC Selection* pulldown menu, select the Feedback ADC family that is installed on the TSW3725. The default ADC in the TSW3725 bill of materials is the ADS4149. In this case, select *ADS414x*.



Figure 14. TSW1200 GUI – ADC Selection

5. Ensure that the TSW1200 data capture is in *Two's Complement Mode*. From the TSW1200 main toolbar, select *Data Capture options* → *Capture Options* → *Two's Complement Mode*. This matches the ADS4149 default SPI setting on the TSW3725 board.





Figure 15. TSW1200 GUI – Capture Option

6. From the TSW1200 Test pulldown menu, select Single Tone FFT.



Figure 16. TSW1200 GUI – Test Selection

- 7. Ensure that the TSW3725 hardware is programmed with the *default\_config.m* file.
- 8. Program the TSW1200 GUI Single Tone Test Setup as follows
  - (a) ADC Sample Rate (Fs) = 204.8M
  - (b) ADC Input Frequency (Fc) = 153.6M
  - (c) FFT Record Length (Ns) = 16384
  - (d) Select the Auto Calculation of Coherent Input Frequency check box
- 9. The GUI now appears as shown in Figure 17.



—Single Tone Test S ADC Sampling Rate 204.8M	etup —— (Fs)
ADC Input Frequent 153.61250000M	cy (Fc)
FFT Record Length	(Ns)
Auto Calculation Coherent Input I	of Frequency

Figure 17. TSW1200 GUI – Test Setup Frequencies

- 10. Apply a +5-dBm, 1836.3875-MHz tone to the TSW3725 FB\_IN1 J27 connector (Feedback Path 1). This frequency can be calculated from the following equation.
  - (a) LO frequency = 1990 MHz
  - (b) ADC input frequency = 153.6125 Hz
  - (c) Equation = LO frequency ADC input frequency = 1990M-153.6 MHz = 1836.3875 MHz
- 11. This signal can come from an external source or the TSW3725 TX chain.
- 12. From the TSW3725 GUI Feedback Path Selection pulldown menu, select *FB1* to select the Feedback Path 1.
- 13. From the TSW3725 GUI PGA870 Feedback Path, set Gain to 12dB

	TX1 ATTN 31.75 dB TX2 ATTN 31.75 dB Attenuation range 0c
ľ	Feedback Path
	Feedback Path Selection FB1
	PGA870 gain range PGA870 Feedback Path Gain 12 dB -11.5dB to 20dB in 0.5dB steps
Ľ	

14. From the TSW1200 GUI click on the Capture button and view the results

# 5.5 RX Path: TSW1200 Software Setup – Single Tone Example

A detailed explanation for the TSW1200 setup is described in the TSW1200 EVM guide, which is available on the TI website (<u>www.ti.com</u>)

- 1. From the TI website download and install the TSW1200GUI-SW v2.5 or later version.
- 2. Load TSW1200\_v2p5 or later. The TSW1200 GUI appear as shown in Figure 18





Figure 18. TSW1200 GUI

- The text box in the bottom left states TSW1200 found on COM3. If the text box does not state this, then type CTRL+SHIFT+I. If that does not work, then power cycle the TSW1200, and type CTRL+SHIFT+I.
- From the *TI ADC Selection* pulldown menu, select the Feedback ADC family that is installed on the TSW3725. The default ADC in the TSW3725 BILL OF MATERIALS is the ADS4249. In this case, select ADS424x.



Figure 19. TSW1200 GUI – ADC Selection

5. Ensure that the TSW1200 data capture is in *Two's Complement Mode*. From the TSW1200 main toolbar, select *Data Capture options* → *Capture Options* → *Two's Complement Mode*. This will match the ADS4249 default SPI setting on the TSW3725 board.





Figure 20. TSW1200 – Capture Option

6. From the TSW1200 Test pulldown menu, select Single Tone FFT.

1		
ions	Data Capture options <u>T</u>	est Option
	Test	Capti
-	Setup Diagram 🛛 💌	C
	🗸 Setup Diagram	
	Time Domain	
	Single Tone FFT	
	Two Tone FFT	Low
	ACPR	Sig
	SPI Setup	
	10M Referen	nce

Figure 21. TSW1200 – Test Selection

- 7. Ensure that the TSW3725 hardware is programmed with the default\_config.m file
- 8. Program the TSW1200 GUI Single Tone Test Setup as follows.
  - (a) ADC Sampling rate (Fs) = 204.8M
  - (b) ADC Input Frequency (Fc) = 140M
  - (c) FFT Record Length (Ns) = 16384
  - (d) Select the Auto Calculation of Coherent Input Frequency check box
- 9. The GUI now appear as follows.



—Single Tone Test S	etup —
ADC Sampling Rate	(Fs)
204.8M	
ADC Input Frequent 139.96250000M	cy (Fc)
FFT Record Length	(Ns)
16384	-
Auto Calculation Coherent Input I	of Frequency

Figure 22. TSW1200 GUI – Test Setup Frequencies

10. From the TSW1200 GUI *Display Channel* pulldown menu, determine if Channel A or Channel B is going to be captured.

75W1200 2p5.vi				
ile Instrument Options Data Captur	e options <u>T</u> est Options <u>H</u> elp			
TI ADC Selection Test	Capture Data	, 📃 External Trigger	Display Channel	Window
ADS424x 🔽 Single Tone	e FFT 💌 Capture	Continuous capture	Channel A 🛛 🗸	Rectangi
			🗸 Channel A	
ADC Sampling Rate (Fs)	ADS424× Single Tone FFT Plot - 4/	/20/2011 - 12:43:05 PM - S/N:	Channel B	
204.8M	0.0-			

Figure 23. TSW1200 GUI – ADC Channel Selection

- 11. For a Channel A capture: apply a +5-dBm, 1660.0375-MHz tone to the TSW3725 RX\_IN1 J17 connector. For a Channel B capture, apply this signal to the RXIN2 J21 connector. This frequency can be calculated from the following equation.
  - (a) LO frequency = 1800 MHz
  - (b) ADC input frequency = 139.9625 Hz
  - (c) Equation = LO frequency ADC input frequency = 1800 MHz 139.9625 MHz = 1660.0375 MHz This signal can come from an external source or the TSW3725 TX chain.
- 12. For a Channel A capture, program the TSW3725 GUI's PGA870 RX1 Path Gain to -3 dB. For a Channel B capture, program the TSW3725 GUI's PGA870 RX2 Path Gain to -3 dB.

- Dy Dath				300 00001 2010 11 0A, 31 20101	
PGA870 Rx1 Path Gain	-3	dB	PGA8	370 gain range	A
PGA870 Rx2 Path Gain	-3	dB	-11.50	B to 20dB in 0.5dB steps	

# Figure 24. TSW3725 GUI – RX Path Gain

13. From the TSW1200 GUI, click on the Capture button and view the results



### LTE Demonstration

www.ti.com

### 6 LTE Demonstration

A detailed explanation for the TSW3100 setup is described in the TSW3100EVM guide (SLLU101).

- From the TI Web site, download and install the TSW3100EVM GUI v2.7 or later version. Earlier versions of the TSW3100EVM GUI software do not support the DAC3484 input data format that is required to run the TSW3725.
- Enter the *application* folder in the TSW3100 download. Select the file TSW3100\_LTE\_v2p7.exe to open the TSW3100 LTE GUI. Program the following settings to run a 5-MHz, single-carrier signal using the TM3.1 signal type.
  - (a) Properties
    - (i) Resolution: 16
    - (ii) Back off(dB): 0.1
    - (iii) Complex: check 6
    - (iv) Freq (MHz): 153.
    - (v) Frames: 1
  - (b) Carriers
    - (i) Center Freq (MHz): 0 This controls the frequency offset for all carriers in the list.
    - (ii) Relative Amplitude (dBc/Hz)
    - (iii) Check the box for carrier 1 On
    - (iv) Freq (MHz): 0 This controls the frequency offset for carrier 1.
    - (v) Amp (dB rel): 0
    - (vi) Bandwidth: 5 MHz TM3.1
  - (c) TSW3100 Control
    - (i) Select master.
    - (ii) Select 16b QDAC.
    - (iii) Select Two's Comp.
    - (iv) Select Load and Run.
    - (v) Select 16b MSB Justify.
    - (vi) Ensure that IP setting is correct (see SLLU101).
- 3. The TSW3100 appears as shown in Figure 25.



Properties		Gen	erate and	d Trans	fer to	TSW	3100	-	TE	AS	TC
Resolution 16 Back	off (dB) 0.1 Complex Swap I/Q Time and Points	Tew/240/	Contro	, i	_			1193	ver. 2.7	ABC	
Freq (MHz) 153.6	Frames 1 Total Time ~ 10 ms Points =	© master C slave	C LVDS C CMOS C BwDD	R	6	Two's C Offset E	Comp Bin	다 Inte 다 Los	nieaved ad and Ru	n	জ জ
			C GC532	25 DAC malLVDS		Bit Rev	erse I erse Q	192.16	58.1.12 <sub>3</sub>		-
Center Freq (MHz)	Relative Amplitude							ł			Pin
On Freq (MHz) Amp (	dB rel) Bandwidth	1									
1 🔽 🚺 🚺	5 MHz TM3.1 •	0.8 -									
2 0 0	5 MHz TM3.1 -	0.6 -									
3 - 0 0	5 MHz TM1.1 -	0.4 -									
4 - 0 0	3 MHz TM3.1 -	0.2 -									
5 0 0	3 MHz TM1.1 -		1 0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	-1
6 0 0	3 MHz TM1.1 -	1									
7 0 0	3 MHz TM1.1 +	0.8									
8 0 0	3 MHz TM1 1	0.6 -									
and the second second		0.4									
		0.2									

Figure 25. TSW3100 LTE GUI

- 4. Click on the gray button Generate and Transfer TSW3100. When the TSW3100 is finished, the TSW3100 appears as shown in Figure 26. This process takes 1 to 2 minutes. Version 2p7 of the TSW3100 does have some errors in generating certain LTE signals. This will be fixed in a later version of the TSW3100 software. The following signal types are generated correctly in version 2p7.
  - (a) TM3.1 single carrier for 5-MHz, 10-MHz, 15-MHz, and 20-MHz bandwidths (1.4-MHz and 3-MHz do not demodulate).
  - (b) TM1.1 single carrier for 5-MHz and 10-MHz bandwidths (1.4-MHz and 3 MHz do not demodulate).



operue	8				Gen	erate and Transf	er to TSW3100	INSTRUM	S
Resolut	tion 16	Backoff (d	B) 0.1 Com	nplex				Ver 27	APOUT
Fracti	ional Output R	ate	Time and Points		TSW3100	) Control		101.04.1	AD001
Freq	a (MHz) 15	3.6	Frames 1 Total Time ~ 10 m Points =	ns	<ul><li>master</li><li>slave</li></ul>	C LVDS C CMOS C BWDDR	<ul> <li>Two's Comp</li> <li>Offset Bin</li> </ul>	Interleaved     Load and Run     16b MSB Justify	Star
						GC5325     GC 5325     G 16b QDAC     C 2w Seriell VDS	Bit Reverse I	192.168.1.12 3	*
rriers			Relative Amplitude			V 2W Serial VDS	1 Dit Neverse &		Ping
Center	Freq (MHz)	>0	C dBc C dBc/	Hz	, x 10 <sup>4</sup>				
On	Fred (MHz)	Amp (dB re	l) Bandwidth		4		3 1 1		
On	· · · · · · · · · · · · · · · · · · ·					2 10 10 10 10 10 10 10 10 10 10 10 10 10			
1 🔽	0	0	5 MHz TM3.1	┓.		en dila di mana di binte		ndean Al billet a dan haradaa	and bullah
	0	0	5 MHz TM3.1		E 2 When	en atter le protonne le black	and all the property of the states of the	nban Alexandra and an an	linn hild ale
	0	0	5 MHz TM3.1 5 MHz TM3.1			หลางเป็นๆไป <mark>่างระบบและ</mark> ไปไป <sub>ก</sub> ุ่มม	والجادية والمراسية والمراسية والمراسية	nbailthalaite faile an	la ne hidak
		0	5 MHz TM3.1 5 MHz TM3.1 5 MHz TM1.1		Code (Linear)	kantiteritäyyväyvyvä <mark>ltelesi</mark> u	in the second	nkapi (1446, jánky) dar	ikus n
		0	5 MHz TM3.1 5 MHz TM3.1 5 MHz TM1.1 3 MHz TM1.1		2 (Lugar) 0 (Lugar) 0 -2 (114)	en etterlig met und blade Alfred vite a sameter bistorier	en Den en programmente de la companya de la company A companya de la comp	alansi katelen katelen jara	athledgenet
			5 MHz TM3.1 5 MHz TM3.1 5 MHz TM1.1 3 MHz TM3.1 3 MHz TM1.1		2 (Timear) 0 0 -2 000 -4	en attesti verson atteste erjannes, energia, erjanja		alasti fi fit fites, fi fallest alasti fi fitt fites, fi fallest alasti fi fitt fittes 7	4101400
			5 MHz TM3.1 5 MHz TM3.1 5 MHz TM1.1 3 MHz TM3.1 3 MHz TM1.1			en alle de la constante de la c Constante de la constante de la c	Alternation and a second se	olani koloni alan da sa	9 10
			5 MHz TM3.1 5 MHz TM3.1 5 MHz TM1.1 3 MHz TM3.1 3 MHz TM1.1 3 MHz TM1.1		2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	en etter för atter för etter för etter för etter för atter för atter för atter för atter för atter för atter för 2 3	4 5 6 Time (ms)	nhanik (Killer Pohra) <sup>20</sup> an aparlan sa Sana Japan 7 B	анандак араландак 9 10
			5 MHz TM3.1 5 MHz TM3.1 5 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1		2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4		4 5 6 Time (ms)	olani kulta kata da 19. na polani da pol 7 B	9 10
			5 MHz TM3.1 5 MHz TM3.1 5 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1		2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4		4 5 6 Time (ms)	olanik fekter fakter 194 - Angele Angele fakter 7 B	9 10
			5 MHz TM3.1 5 MHz TM3.1 5 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1	네 네 너 너 너 너 너 너 너 hude (dB)	2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4		4 5 6 Time (ms)	olando fel filo de la superiorente 1947 - Santa Santa Santa Santa Santa 7 B	9 10
			5 MHz TM3.1 5 MHz TM3.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1 3 MHz TM1.1	Montitude (dB)	2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4		4 5 6 Time (ms)		9 10

Figure 26. TSW3100 LTE GUI After Waveform Created

- 5. Verify that the following TSW3100 LEDs are illuminated. If these LEDs are not illuminated, verify that the TSW3725 is connected properly and its default settings are loaded,
  - (a) D14: PAT GEN CLK
  - (b) D15: PAT GEN RUN
- 6. If TSW3100 LED D16: FIFO EMPTY ERROR is illuminated, then the TSW3100 did not load correctly and step 4 needs to be repeated. If this continues, then power cycle the TSW3100 board before repeating step 4.
- 7. Ensure that the TSW3725 hardware is programmed with the *default\_config.m* file.
- 8. The TSW3725 TX1 or TX2 output with these settings must have a 5-MHz LTE signal centered at 2143.6 MHz. This can be calculated by the following equation.
  - (a) LO frequency = 1990 MHz
  - (b) Coarse mixer = Fs/4 = 614.4/4 = 153.6 Hz
  - (c) Tone Center in TSW3100 GUI = 0 MHz
  - (d) Equation = LO frequency + coarse mixer + tone center = 1990 MHz + 153.6 MHz +0 MHz = 2143.6 MHz



# 7 GUI Functions

This section describes how to program each panel of the TSW3725 GUI.

W3725	
onfiguration Control	Master Power Fnahle/Disable
default config.m	MAIN ALL ON work
Load from File	
Load from File	CUSTOM TX1 ON - TX2 ON - FB ON - RX1 ON - RX2 ON
Save Config C Log SPI	
locks - CDCE72010	
VCXO 614.4 MHz	EDG A 2720 DEC DO - 30 72MH7 DECOUTA OCC - OFF
REF OPT Primary	TREFOUTIOFF OFF
REF IN FREQ 30.72 MH-	5330/TSW3100 CLK /8 - F0.04112 REPOUL2 OFF - 0.1
INFL P VERD of REF IN FRED an	TX-DAC CLK A DIT OIT ANNIE ADDR DATA
anged the startail seed to indexidy	FB-ADC CLK /3 * 204 BMHz 0 0000000 RD WR DISPLAY
	RX-ADC CLK 13 1 204.0With2
x and Feedback	
LO (MHz) 1990	Mode Provident -
PFD (MHz) 15,36	ADDR DATA wood Practional
	Reg0 T 0000000 RD WR DISPLAY
QMC ON The Input/V	iew QMC Settings Restore QMC Defaults Fine Mixing
	FDAC NA: Coarse
MIXING Coarse 1+Fs/4	NC01 NC02
FIED ON *	ADDR DATA NCO freq (MHz) 153.6 153.6
	00 0000 PD WE DISDLAY PhaseAdd(0x) NA: Coarse NA: Coarse
Interpolation 4x	PhaseOffset(0x) 0000 0000
Tx Attenuation	
TX1 ATTN 31.75 dB	TX2 ATTN 31.75 dB Attenuation range bill to 31.750E in 0.350E steps
Feedback Path	
Feedback Path Selection O	
DO 8970 Esculturals Dath Onia	UD UD KD VVR DISPLAY
PGA870 Feedback Path Gain	
PGA870 Feedback Path Gain	
PGA870 Feedback Path Gain x - TRF3720-2	
PGA870 Feedback Path Gain x TRF3720-2 LO (MHz) 1800	ADDR DATA Mode Fractional
PGA870 Feedback Path Gain <b>TRF3720-2</b> LO (MHz) 1800 PFD (MHz) 15.36	REF IN see CDCE72010 FPGA, 3720 REF Red 0 0000000 RD VVR DISPLAY
PGA870 Feedback Path Gain TRF3720-2 LO (MHz) 1800 PFD (MHz) 15.36 PPD Path	REF IN see CDCE72010 FPGA, 3720 REF Reg0 T 0000000 RD V/R DISPLAY
PGA870 Feedback Path Gain	REF IN see CDCE72010 FPGA, 3720 REF Reg0 T 0000000 RD V/R DISPLAY
PGA870 Feedback Path Gain           x           - TRF3720-2           LO (MHz)           PFD (MHz)           15.36           - Rx Path           PGA870 Rx1 Path Gain	REF IN see CDCE72010 FPGA, 3720 REF Reg0 T 0000000 RD V/R DISPLAY
PGA870 Feedback Path Gain           x           TRF3720-2           LO (MHz)         1800           PFD (MHz)         15.36           Rx Path           PGA870 Rx1 Path Gain         -11.5           PGA870 Rx2 Path Gain         -11.5	REF IN     see CDCE72010 FPGA, 3720 REF     ADDR     DATA     Mode     Fractional       dB     PCASSD gen mage     ADSR2xx/ADS560C2x Register       dB     PCASSD gen mage     ADDR     DATA

Figure 27. TSW3725 GUI

# 7.1 Configuration Control Panel

The Configuration Control panel consist of the following.

- 1. Display Configuration box: displays the configuration file that is loaded when Program All is selected.
- 2. Load from File button: when pressed, allows the user to select which configuration to load.
- 3. **Program All button:** when pressed, the TSW3725 hardware is programmed with the configuration displayed in the *Display Configuration Box*.
- 4. **Save Config button:** when pressed, allows user to save the configuration currently displayed in the TSW3725 to a new configuration file name.
- 5. Log SPI radio button: when selected, the TSW3725 records all the SPI commands sent to the TSW3725 in the file tsw3725\_SPI\_commands.csv.

**GUI** Functions



Figure 28. Configuration Control Panel

#### At Start Up

When the TSW3725 is first started, the Configuration Control panel appears as shown in Figure 29. Notice that the *Save Configuration* button has been blacked out. This implies that no configuration has been loaded to the TSW3725 hardware yet.

– Configuration Control							
default_config.m							
Load from File	Program All						
	C Log SPI						

### Figure 29. Configuration Control Panel on Initial Start-Up

### Loading the Default Config

To load the file named *default\_config.m*, press the *Program All* button. After the *Program All* button has been pressed, it turns white and provides status updates on the TSW3725 hardware section that is being programmed. After the TSW3725 hardware programming is complete, the *Program All* button displays the word *Done*; then it turns yellow and displays *Program All*. This process takes approximately 25 seconds.

- Configuration Control	- Configuration Control
default_config.m	default_config.m
Load from File Prg Clocks	Load from File Done
C Log SPI	C Log SPI

Figure 30. Configuration Control Panel While Programming the TSW3725



If the TSW3725 hardware is not powered up, or if SW2 is in the wrong state (see Section 4.1), or if the TSW3725 USB cable is not connected, then the TSW3725 GUI fails to connect to the TSW3725 hardware. When the GUI fails to connect to the TSW3725 hardware, the Configuration Control panel displays the term *usb not connected* in the *Program All* button as shown in Figure 31. If this happens, fix the connection problem, and then press the *Program All* button again. Note: the *Program All* button still reads *usb not connected* when the button is pressed the second time.

- Configuration Co	ontrol						
default_config.m							
Load from File	usb not connected						
Save Config	C Log SPI						
Clocks - CDCF72	010						

# Figure 31. Configuration Control Panel When TSW3725 not Powered Up or USB Cable Not Connected

The *default\_config.m* file is set up for Band 1 LTE and Band 1 WCDMA frequencies. To improve TX carrier suppression and sideband suppression numbers, see the immediately following section.

#### **Loading Other Configuration Files**

To load a configuration file other than the one displayed in the Display Configuration Box, press the *Load from File* button. The following file loader is displayed. Select the desired \*\_*config.m*, and press the *Open* button. The Display Configuration Box now displays the new configuration file name. To load this new configuration file, press the *Program All* button.

Select File to Op	en			<u>?</u> ×	
Look in:	D TSW3725_G	UI	- 🗈 💣 💷		
My Recent Documents	DLL_drivers DLL_drivers FTD245_Drive QMC_configs TSW6011 default_config	rs by_SN .m			- Configuration Control
Desktop My Documents	XYZ_config.m				Load from File         Program All           Save Config         Cog SPI
a0216737 on LTA0216737A					Remember to press the 'Program All' button to
My Network Places	File name: Files of type:	XYZ_config.m (*config.m)	-	Open Cancel	program the hardware

Figure 32. Configuration Control – Loading Other Configuration Files

The *default\_config.m* file is setup for Band 1 LTE and Band 1 WCDMA frequencies. To improve TX carrier suppression and sideband suppression numbers for Band 1 LTE and Band 1 WCDMA at 25C, some board-specific files are available in the *QMC\_configs\_by\_SN* (TSW3725 Stand-Alone mode) and *QMC\_configs\_by\_SN/SCBP configs* (TSW3725 SCBP mode) directories located in the main TSW3725 GUI directory. These files have factory-adjusted DAC3484 settings that correct for offset, phase, and gain errors in the TX modulator. If this file does not exist for a certain serial number, one can either perform a self-calibration using the *DAC3484*: *QMC CONTROL* GUI or contact the factory to see if this file was created after the latest TSW3725 software release. **Refer to section 7.5.2** for instructions on how to program the *DAC3484*: *QMC CONTROL* GUI.



#### Saving a New Configuration File

In some cases, the user may modify the settings in the TSW3725 GUI and want to save these settings to a unique file. To save the configuration currently programmed in the TSW3725 to a new file, press the *Save Configuration* button. The following file box is displayed (Figure 33). Save the file to a unique filename. The filename must end with *\_config.m*.

Select File to Op	en				? ×
Look in:	TSW3725	GUI	•	+ 🗈 💣 🖽 -	
My Recent Documents Desktop My Documents	backup files DLL_drivers FTD245_Driv QMC_config TSW6011 default_con XYZ_config.	vers s_by_SN fig.m m			
My Network	File name:	new[_config.m			Open
Places	Files of type:	(*config.m)			Cancel

Figure 33. Configuration Control – Saving New Configuration Files

# Log SPI Radio Button

By selecting the Log SPI radio button, the following happens:

- 1. The existing file *tsw3725\_SPI\_commands.csv* is removed.
- 2. A new file tsw3725\_SPI\_commands.csv is created.
- 3. All SPI commands are recorded in the file tsw3725\_SPI\_commands.csv until Log SPI is deselected.

The file *tsw3725\_SPI\_commands.csv* has the following columns:

- 1. **chipid:** The FPGA on the TSW3725 selects which device the SPI command is sent to based on the chip ID number.
- 2. **spi\_word\_hex:** The hexadecimal word sent to the device that has been designated. This hexadecimal word includes the address and register bits in the order that the device is expecting.
- 3. **spi\_word\_length:** The length of the word sent to the designated device. This adds the number of address bits and register bits.
- 4. **addr\_bin:** The address that is being programmed in binary form. This is another way of showing the same information in spi\_word\_hex.
- 5. **reg\_bin:** The register bits in binary form that are sent to the address. This is another way of showing the same information in spi\_word\_hex.

This button allows the user to load any working configuration file and record all the spi commands sent to the TSW3725. At this point, the user can use the *tsw3725\_SPI\_commands.csv* to aid in programming the SCBP board to the user's unique configuration.



1B				Microsof	t Exc	el - tsw3725_5	PI_commands.c	sv				
	– Configuration Con	rtrol		] Eile	Edit	View Insert	Format Tools	Data Wir	ndow <u>H</u> elp			
1	C:)Documente e	nd Setting	10	) 💕 🕻			* 12 8	a 🖪 🛪 🥥	19-6	- 8	Σ	Ŧ
	je. Documents a		1	1 21 2	2 (2)	S 213	S 🔒 🖷 🖗	I TeReply	with Changes	End	Revie	w.
	Load from File	Program All		Aria	K -	- 1	10 - <b>B</b> I	⊻   ≣ ₹		\$ %		*.0
	Loud Hom Hic	: Trogram car	100	G21		✓ fx						
-11	0	(C. L	1.7	A		В	C	D	E	F		
11	Save Config	<ul> <li>Log SPI</li> </ul>	1	chipid		spi_word_hex	spi_word_len	addr_bin	reg_bin			
-1			2		11	2403410	32	0	1E+25			
			3		11	860070C0	32	1000	1.1E+26			
			4		11	40007004	32	100	1.11E+14			
			5		11	C0804156	32	1100	1E+23			
			6	6	11	200041C4	32	10	1E+14			
			7		11	A00041C4	32	1010	1E+14			
			8		11	60004104	32	110	1E+14			
			9		11	E88002C1	32	1110	1E+27			
			10		11	1B8020D7	32	1	1.01E+27			
			11		44	9000000	27	1001	15,05			

Figure 34. Log SPI

# 7.2 Master Power Enable/Disable Panel

The Master Power Enable/Disable panel consists of the following:

- 1. Main pulldown menu: allows the user three options (ALL ON -reset, ALL-OFF-reset, CUSTOM)
- 2. Individual *Custom* pulldown menus: In *CUSTOM* mode, these menus allow the user to power on or off individual sections of the TSW3725 hardware.

I 🗖 Master I	ower Enable/Disable
MAIN	ALL ON-reset
сизтом	TX1 ON - TX2 ON - FB ON - RX1 ON - RX2 ON -

Figure 35. Master Power Enable/Disable Panel

The ability to quickly turn on and turn off large sections of circuitry can aid in debugging if the user is interested in optimizing performance. It also can be used to disable a specific signal chain if the user is interested in a subset of the TSW3725 functionality. The following tables describe the actions taken for certain combinations *CUSTOM* GUI settings.

TX1	TX2	ТХ3	Device State Changes
ON	ON	ON	All TX and FB components active
OFF	ON	ON	DAC3484: DAC A and B set to sleep mode DAC3484: QMC C&D GAIN = 0, QMC PHASE A and B = 0
ON	OFF	ON	DAC3484: DAC C and D set to sleep mode DAC3484: QMC C and D GAIN = 0, QMC PHASE C and D = 0
OFF	OFF	ON	DAC3484: DAC A, B, C, and D set to sleep mode DAC3484: QMC A, B, C, and D GAIN = 0, QMC PHASE A , B, C, and D = 0 DAC input clock output and divider from CDCE72010 disabled
ON	ON	OFF	FB PGA870 set to sleep mode FB ADC(ADS4149) set to sleep mode FB ADC input clock output and divider from CDCE72010 disabled

Table	1.	ΤХ	and	FB	Custom	settings
Table		17	ana		oustonn	Jounga

TX1	TX2	TX3	Device State Changes
OFF	OFF	OFF	DAC3484: DAC A, B, C, and D set to sleep mode DAC3484: QMC A, B, C, and D GAIN = 0, QMC PHASE A and B, C and D = 0 DAC input clock output and divider from CDCE72010 disabled FB PGA870 set to sleep mode FB ADC(ADS4149) set to sleep mode FB ADC input clock output and divider from CDCE72010 disabled TX and FB LO (TRF3720-1) set to sleep mode TX and FB LO reference (TRF3720-1) output from CDCE72010 disabled (divider still enabled)

#### Table 1. TX and FB Custom settings (continued)

### Table 2. RX Custom Settings

RX1	RX2	Device State Changes
ON	ON	All RX components active
OFF	ON	RX1 PGA870 set to sleep mode
ON	OFF	RX2 PGA870 set to sleep mode
OFF	OFF	RX1 and RX2 PGA870 set to sleep mode RX ADC(ADS4249) set to sleep mode RX ADC input clock output and divider from CDCE72010 disabled RX LO (TRF3720-2) set to sleep mode RX LO reference (TRF3720-2) output from CDCE72010 disabled (divider still enabled)

The MAIN pulldown menu options of *ALL ON-reset* and *ALL OFF-reset* are equivalent to programming a CUSTOM mode of TX1 = TX2 = FB = RX1 = RX2 = ON and TX1 = TX2 = FB = RX1 = RX2 = OFF, respectively.

# 7.3 RD/WR/DISPLAY and the DISPLAY GUI

The TSW3725 GUI provides boxes and menus for the most common functions that the user will use to configure the TSW3725. However, for the less common options, the TSW3725 GUI has six RD/WR/DISPLAY options. These allow the user to program the serial interface directly to the following six parts.

- 1. CDCE72010
- 2. TRF3720-1 (TX LO)
- 3. DAC3484
- 4. ADS41xx/ADS58B1x (FB ADC)
- 5. TRF3720-2 (RX LO)
- 6. ADS42xx/ADS58C2x (RX dual ADC)

See the individual parts data sheets for part-specific register settings and functions.



#### Figure 36. Master Power Enable/Disable

The RD/WR/DISPLAY section consist of the following:

- 1. ADDR: input a valid address from the data sheet to read from or write to.
- 2. **DATA:** when the RD button is pressed, this displays the data programmed in the ADDR specified; when the WR button is pressed, this writes the data in this box to the ADDR specified.
- 3. RD: when pressed, this reads register DATA from the ADDR specified.
- 4. WR: when pressed, this writes register DATA to the ADDR specified.
- 5. **DISPLAY:** when pressed, this calls the DISPLAY GUI for the device of interest. The DISPLAY GUI provides read-back information for all registers of a given device. See the following *Display GUI* section for a more detailed description.



# 7.4 DISPLAY GUI

The DISPLAY GUI is used to quickly verify all register settings for a device. It also allows the user to compare the register data that was written to the part versus the register data read from the part. If a mismatch in the data written versus the data read is found, this may mean that the register is a read-only register or that an issue exists and the TSW3725 needs to be reprogrammed.

The DISPLAY GUI is a read-only GUI. It also does not update automatically when a change is made in the TSW3725 GUI. To see the new updates in the DISPLAY GUI, the user needs to press the DISPLAY button in the TSW3725 GUI.

The DISPLAY GUI consist of the following:

- 1. Part Number: displays the part number whose serial register information is displayed.
- 2. **Part ID:** This number refers to the ID number that the MATLAB<sup>™</sup> software sends to the TSW3725 hardware to program a certain device.
- 3. **Reg Name:** in the individual device data sheet, the registers are given a name assignment for each register address.
- 4. Reg Addr: the register address programmed, displayed in hexadecimal format (MSB to LSB).
- 5. Write Reg Data: displays the data that was most recently written to a specific register address, displayed in hexadecimal format (MSB to LSB).
- 6. **Reg Readback:** displays the actual data read back from the device's specific register address, displayed in hexadecimal format (MSB to LSB).

display	y_reg									
Part Nu	mber D	AC3484								
Part	ID	1								
	Reg Name	Reg	Addr	Write Reg Data	Reg Readback		Reg Name	Reg Addr	Write Reg Data	Reg Readback
0	config0	0:	(00)	0x029C	0x029C	25	config25	0x19	0x0440	0x0440
1	config1	0:	:01	0x050E	0x050E	26	config26	0x1A	0×0020	0×0020
2	config2	0:	(02	0xF0E2	0xF0E2	27	config27	0x1B	0x0000	0×0000
3	config3	0:	:03	0xF000	0×F000	28	config28	0x1C	0x0000	0x0000
4	config4	0:	04	0x0000	0xFFFE	29	config29	0x1D	0x0000	0x0000
5	config5	0:	:05	0x0000	0x3D60	30	config30	0x1E	0x1111	0x1111
6	config6	0:	06	0x0000	0x2B00	31	config31	0x1F	0x1140	0x1140
7	config7	0:	07	0×FFFF	0×FFFF	32	config32	0x20	0x2201	0x2201
8	config8	0:	08	0x0000	0x0000	33	config33	0x21	0x0000	0x0000
9	config9	0:	:09	0x8000	0x8000	34	config34	0x22	0x1B1B	0x1B1B
0	config10	0	:OA	0×0000	0x0000	35	config35	0x23	0×FFFF	0xFFFF
1	config11	0:	OB	0x0000	0x0000	36	config36	0x24	0×1400	0x1400
2	config12	0:	OC	0×0400	0x0400	37	config37	0x25	0x0000	0x0000
3	config13	config13 0x00		0x4400	0x4400	38	config38	0x26	0x8000	0x8000
4	config14	0:	OE	0x0400	0x0400	39	config39	0x27	0×FFFF	0×FFFF
15	config15	0:	OF	0×0400	0x0400	40	config40	0x28	0x8000	0x8000
16	config16	0:	10	0×0000	0x0000	41	config41	0x29	0x0000	0x0000
7	config17	0:	(11	0x0000	0x0000	42	config42	0x2A	0x8000	0×8000
8	config18	0:	(12	0x0000	0x0000	43	config43	0x2B	0×FFFF	0xFFFF
19	config19	0:	13	0x0000	0x0000	44	config44	0x2C	0×8000	0×8000
20	config20	0:	14	0x0000	0x0000	45	config45	0x2D	0×0000	0×0000
21	config21	0:	15	0x0000	0x0000	46	config46	0x2E	0x0000	0x0000
22	config22	0:	(16	0x0000	0x0000	47	config47	0x2F	0x0000	0x0000
23	config23	0:	(17	0x0000	0x0000	48	config48	0x30	0×0000	0x0000
24	config24	0:	18	0x2802	0x2807	49	version	0x7F	0x5409	0x5409

Figure 37. DISPLAY GUI for DAC3484

**GUI** Functions

**GUI** Functions

# 7.5 Clocks – CDCE72010 Panel



Figure 38. CDCE72010 Panel

The Clocks - CDCE72010 panel consist of the following:

# 1. VCXO/REF Section:

- (a) VCXO: VCXO frequency in MHz, matches the frequency of schematic component Y1. The default hardware comes with a 614.4-MHz VCXO. If a different VCXO frequency is selected in the GUI, remember to manually reprogram the CDCE72010's P-, —, and N-dividers so that the VCXO and REF IN divide down properly.
- (b) REF OPT: Primary (default setting) or Secondary reference
  - (i) The Primary reference is connected through the TSW3725 high-speed connector J8 on pin 179. This is the option used when the external reference is applied to J2 of the TSW3725 Adaptor Board or if the user has connected the digital baseband board.
  - (ii) Secondary reference is the option used when the external reference is applied to J9 of the TSW3725 hardware.
- (c) REF IN FREQ: The default setting is 30.72 MHz. This is the frequency supplied to the connector described in the REF OPT section. If a different REF IN frequency is written to the GUI, remember to manually reprogram the CDCE72010's P-, —, and N-dividers so that the VCXO and REF IN divide down properly. This frequency must meet the CDCE72010 data sheet frequency and amplitude specifications.
- 2. **Divider Pulldown Menus:** Allows for direct programming of seven of the CDCE72010 output divider frequencies. The default setting for each is provided in Table 3. These settings are the defaults based on the TSW3725 default hardware configuration used with the TSW3100 for driving the TX chain.
  - (a) For the most part, if any of these settings are changed, then some hardware modifications are required.
  - (b) The FPGA, 3720 reference must not be programmed *OFF* in most cases, as this is the clock supplied to the FPGA that allows the serial interface programming to work.
  - (c) The TSW3100 CLK is calculated by this equation: VCXO frequency/(DAC3484 interpolation setting × 2). The × 2 in the denominator is due to the DDR clock of the DAC3484.

See Table 3 for individual divider information.

Divider Pulldown Menu Name	CDCE72010 Pin Name/Signal Type	TSW3725 Function
FPGA, 3720 REF	U0N/LVCMOS U1P/LVCMOS U1N/LVCMOS	FPGA clock reference TRF3720-1 reference input (TX and FB) TRF3720-2 reference input (RX)
REFOUT1	U2P/LVCMOS	Sent to SMA connector J10 (ac coupled)
RX-ADC CLK	U4P/LVCMOS	Sent to Bandpass filter, converted to a differential signal via a transformer than sent to RX Dual ADC
FB-ADC CLK	U5P/LVCMOS	Sent to Bandpass filter, converted to a differential signal a via transformer than sent to Feedback ADC
REFOUT2	U6P/LVCMOS	Sent to MCX connector J38 (dc coupled)

#### Table 3. Divider Pulldown Menu Description

Divider Pulldown Menu Name	CDCE72010 Pin Name/Signal Type	TSW3725 Function
TX-DAC CLK	U7/LVPECL	DAC3484 DACCLK pins
GC5330/TSW3100 CLK	U8/LVDS	Sent to high-speed connector J8. J8 connects to the TSW3725 adaptor board for the TSW3100 FPGA clock, or to the digital baseband board for the GC5330 clock

- (d) **Divider Output Frequency Display Boxes:** these are display-only boxes for quick reference. The display boxes show the result of this equation, (VCXO frequency)/(output divider setting)
- (e) **RD/WR/DISPLAY:** read/write programmability of the CDCE72010 serial interface. See the 'RD/WR/DISPLAY' section for more details.

### 7.6 TX and Feedback Panel

#### 7.6.1 TRF3720-1 Panel

The 'TRF3720-1' panel consists of the following:

- LO (MHz): Type in the desired LO frequency and press enter. Several TRF3720 register values are automatically calculated and updated when the LO frequency is changed. This text box will turn red if the REF IN frequency in the CDCE72010 menu changes after the TRF3720 is programmed. The red indicates the TRF3720 needs to be reprogrammed. The REF IN text box will also turn red and state 'REF from CDC changed, update LO'. To reprogram the TRF3720 set your cursor in the LO text box and press enter.
- 2. PFD (MHz): Type in the desired PFD frequency and press enter. Several TRF3720 register values are automatically calculated and updated when the PFD frequency is changed. This text box will turn red if the TRF3720 reference frequency from the CDCE72010 device is not an integer multiple of the PFD frequency. The REF IN text box will also turn red and state 'PFD&REFIN, are not integer multiples'. To correct this, enter a PFD frequency that is an integer sub-multiple of the TRF3720 reference frequency.
- REF IN: A text box that reminds the user that the TRF3720 reference input frequency is set by one of the CDCE72010 output dividers. When this box turns red it indicates the TRF3720 register settings are not programmed correctly. The text in the box will either read 'PFD&REFIN, are not integer multiples' or 'REF from CDC changed, update LO'. The actions taken to correct these errors are described directly above in the LO (MHz) and PFD (MHz) descriptions.
- 4. **Mode:** Allows users to choose between Fractional and Integer mode. In Integer mode, the LO frequency is updated by rounding down to the next closest working integer LO frequency. Several TRF3720 register values are automatically calculated and updated when the mode is switched from integer to fractional or vice versa.
- 5. **RD/WR/DISPLAY:** read write programmability of the TRF3720 serial interface. See the *RD/WR/DISPLAY* section for more details.???

LO (MHz)	1990				DOTO	Mode Fractional	
PFD (MHz)	15.36	REF IN	see CDCE72010 FPGA, 3720 REF	ADDR			
	·			Reg6 📩	4A48080	RD VVR DISPLAY	
DAC3484							-

Figure 39. TRF3720-1 Panel



# Figure 40. TRF3720-1 Error, TRF3720's Ref Is Changed in CDCE72010 Menu





Figure 41. TRF3720-1 Error, REFIN Is Not an Integer Multiple of PFD.

### 7.6.2 DAC3484 Panel

The DAC3484 panel consists of the following:

- 1. **QMC section (Quadrature Modulation Correction):** allows user to easily program the QMC section of the DAC3484. A detailed description of the QMC section is follows.
- 2. Mixing options: allows user to easily program the digital coarse or fine mixers in the DAC3484.
- 3. **FIFO menu:** allows user to turn the FIFO on or off. The default state is on.
- 4. Interpolation menu: allows users to select the 1x, 2x, 4x, 8x, or 16x interpolation modes. The default state is 4x interpolation. Changing the interpolation mode requires users to change the GC5330/TSW3100CLK frequency or the TX-DAC CLK frequency in the Clock CDCE72010 section, because TX-DAC CLK clock = (DAC input data rate x interpolation mode). The TSW3100 accepts a DDR clock; remember this when determining the GC5330/TSW3100CLK. The TSW3100 input waveform may need to be recalculated if the interpolation mode is changed.
- 5. **RD/WR/DISPLAY:** read/write programmability of the DAC3484 serial interface. See Section 7.3 for more details.





#### **Detailed Descriptions:**

- 1. DAC3484 QMC section:
  - (a) QMC pulldown menu: allows the user to turn the DAC3484's QMC mode on or off.
  - (b) **Restore QMC Defaults button:** When pressed, the default QMC settings are loaded from the configuration file that was loaded to the TSW3725 in the *Configuration Control* panel of the TSW3725 GUI. This allows the user the ability to reload the ideal QMC configuration setting without having to reload the \*\_*config.m* file.
  - (c) Input/View QMC Settings button: When pressed, the DAC3484: QMC CONTROL GUI is made available. The instructions to program this GUI are provided in the bottom left corner of the GUI window. This GUI allows the user to view/program the QMC offset, gain, and phase adjust values more efficiently than using the RD/WR/DISPLAY boxes provided in the DAC3484 panel. This allows users to find an ideal QMC setting for their specific board and conditions. The user can then save this setup to a new configuration file using the Save Configuration button in the Configuration Control panel of the TSW3725 GUI.

dac3484qmc							_ 🗆
	DAC	C3484	:QN		ONT	ROL	
Channel A	OFFSET		GAIN		- Channel /	PHASE	
config8	0×0000	config12	0.499994	(0 to 1.9990)	config16	-2.9304e-006	(-0.5 to 0.49975)
- Channel B-	0,0000	Tiex equity	0x200		hex equiv	0×000	
config9 hex equiv	0x0000 0x0000	config13	0.499994 0x200	(0 to 1.9990)			
- Channel C-					- Channel	C&D	
config10   hex equiv	0×0000	config14 hex equiv	0.499994 0x200	(0 to 1.9990)	config17	-2.9304e-006	(-0.5 to 0.49975)
- Channel D-	0~0000	config15	0 400004	(0 to 1 9990)		0,000	
hex equiv	0×0000	hex equiv	0x200	(0.10.1.0000)			
<ul> <li>Instructions</li> <li>1. Enter desired</li> <li>2. Press Enter</li> <li>3. Verify the blue</li> <li>4. After all input</li> <li>5. Verify buttor</li> <li>*The DAC3484</li> <li>This order is a pressed. If been program</li> </ul>	d values in white 1 ue Text Box updat ts are made - Pre: n now reads 'Prog GMC registers ha performed when t f this button is not nmed.	Text Boxes above les with the correct v ss the 'Program QMC ram QMC Settings - ( ve a required progra the 'Program QMC Se pressed the QMC se	value Settings' button Complete' mming order. ttings' button 4ttings have not		Progra	am QMC Set	tings

Figure 43. DAC3484 QMC CONTROL

# 2. QMC Carrier Correction Technique Hints

- (a) For TX1: modify Channels A & B OFFSET configurations.
- (b) For TX2: modify Channels C & D OFFSET configurations.
- (c) Set TSW3725 TX paths to minimum attenuation (see section 7.6.3)
- (d) Monitor the appropriate channels TX carrier frequency (LO frequency) amplitude on a spectrum analyzer.
- (e) After programming a new OFFSET configuration, verify this lowered the amplitude of the carrier on a spectrum analyzer.
- (f) Example TX1:
  - (i) Record carrier amplitude with default settings.
  - (ii) Change Channel A offset to 0x0100.
     If carrier amplitude decreases, change Channel A offset to 0x0200.
     If carrier amplitude increases, change Channel A offset to 0x1FF.
  - (iii) Continue increasing or decreasing offset values until no improvement is seen.
  - (iv) Change Channel B offset to 0x0100.
    - If carrier amplitude decreases, change Channel A offset to 0x0200.
    - If carrier amplitude increases, change Channel A offset to 0x1FF.
  - (v) Continue increasing or decreasing offset values until no improvement seen.
  - (vi) Repeat Step b to e, except this time, vary the hexadecimal location denoted by an Y; 0x00Y0.
  - (vii) Repeat Step b to e, except this time, vary the hexadecimal location denoted by an Z; 0x000Z.



### 3. QMC Sideband Correction Technique Hints

- (a) For TX1: modify Channels A and B GAIN, PHASE configurations.
- (b) For TX2: modify Channels C and D GAIN, PHASE configurations.
- (c) Set TSW3725 TX paths to minimum attenuation (see section 7.6.3).
- (d) Monitor the appropriate channels TX sideband frequency (LO frequency) amplitude on a spectrum analyzer.
- (e) After programming a new GAIN or PHASE configuration, verify this lowered the amplitude of the carrier on a spectrum analyzer.
- (f) Example TX1:
  - (i) Record sideband amplitude with default settings.
  - (ii) Change Channel A gain to 0.498.
    - If sideband amplitude decreases, change Channel A gain to 0.497.
    - If sideband amplitude increases, change Channel A gain to 0.501.
  - (iii) Continue increasing or decreasing gain values until no improvement is seen.
  - (iv) Now Change Channel B gain to 0.498.
    - If sideband amplitude decreases, change Channel A gain to 0.497.
    - If sideband amplitude increases, change Channel A gain to 0.501.
  - (v) Continue increasing or decreasing offset values until no improvement is seen.
  - (vi) Change Channel A&B Phase to 0.001.
    - If sideband amplitude decreases, change Channel A&B phase to 0.002.
    - If sideband amplitude increases, change Channel A&B phase to -0.001.
  - (vii) Repeat Steps b to d except varying smaller significant digits for each setting; repeat until sideband amplitude is acceptable or cannot be decreased anymore.

#### 4. DAC3484 Mixing Options:

- (a) **Mixer Selection menu:** Allows the user to select between the Coarse Mixer, the Fine Mixer, and the option of turning the coarse and fine digital mixers in the DAC3484 off.
- (b) Coarse Mixer Programming menu: Enabled when the *Mixer Selection* menu is set to Coarse. Allows user to chose between the coarse mixer frequency settings of –Fs/4, +Fs/2, +Fs/4, +Fs/8, –3Fs/8, +3Fs/8, and –Fs/8. When the *Mixer Selection* menu is set to Fine or Off, the Coarse Mixer Programming turns gray and displays the word N/A.
- (c) Fine Mixer Programming section: Enabled when the *Mixer Selection* menu is set to Fine. When Fine Mixing is enabled, the FDAC text box displays the same frequency that is shown in the CDCE72010 'TX-DAC CLK' output frequency text box. The user can manually enter the NCO frequencies and phase offset for both NCOs in this section. After a value is entered, press *enter* and the GUI programs the DAC3484 to the new setting. The PhaseADD text boxes are updated after a new NCO freq (MHz) or FDAC frequency are programmed.

The following examples show what the Fine Mixer Programming section looks like when the Mixer Selection box is set to Coarse, Fine, or OFF.



Figure 44. DAC3484 Mixing Options – Coarse Mixing





Figure 45. DAC3484 Mixing Options – Fine Mixing

	View QMC Settings	Restore QMC Defaults	FDAC	Fine NA	e Mixing A: OFF
	ADDR DA	ATA	NCO freq (MHz)	NCO1 153.6	NCO2 153.6
Interpolation 4×	02 F0	082 RD WR DISPLA	PhaseAdd(0x) PhaseOffset(0x)	NA: OFF 0000	NA: OFF

Figure 46. DAC3484 Mixing Options - OFF

# 7.6.3 TX Attenuation Panel

The TX Attenuation panel allows for individual control of the attenuators on the TX1 and TX2 paths. The default attenuators on the TSW3725 have an attenuation range from 0 dB to 31.75 dB in 0.25-dB steps. In the default\_config configuration file, the attenuation settings default to the maximum attenuation of 31.75 dB to reduce the chances of damaging components connected to the TX1 and TX2 output SMA connectors.

To program a different attenuation setting in the GUI, type a new value and press *Enter*. If an improper value is typed, then the GUI software automatically modifies the value to the closest valid attenuation setting.

- Tx Attenuation						_
TX1 ATTN 31.75	dB	TX2 ATTN	31.75	dB	Attenuation range 0dB to 31.75dB in 0.25dB steps	



# 7.6.4 Feedback Path Panel

The Feedback Path panel consists of the following:

- Feedback Path Selection: The TSW3725 has a shared feedback path for TX1 and TX2. The Feedback Path Selection menu has three options – FB1, FB2, or OFF. This menu allows the user to control the RF switch that selects the SMA to feedback path 1 (FB1), the SMA to feedback path 2 (FB2), or it deselects both feedback paths (OFF).
- 2. PGA870 Feedback Path Gain: Allows the user the ability to set the gain of the PGA870 in the feedback path. The PGA870 has a gain range of -11.5 to 20 dB in 0.5-dB steps. To program a different gain setting in the GUI, type a new value and press *Enter*. If an improper value is typed, then the GUI software automatically modifies the value to the closest valid gain setting. The PGA870 does have a power-down mode, but that can only be programmed via the *Master Power Enable/Disable* panel of the TSW3725 GUI.
- 3. **RD/WR/DISPLAY:** Generally, the ADC settings remain constant after the TSW3725 is initialized. However, read/write programmability of the Feedback ADC serial interface is provided. See the *RD/WR/DISPLAY* section for more details.



GUI	Functions
-----	-----------

Feedback Path		
Feedback Path Selection OFF	DO 1970 voie vez ve	ADS41xx/ADS58B1x Register
PGA870 Feedback Path Gain -11.5 dB	-11.5dB to 20dB in 0.5dB steps	00 00 RD WR DISPLAY

Figure 48. Feedback Path Panel

# 7.7 RX Panel

- Kx						
LO (MHz)	1800			ADDR	DATA	Mode Fractional
PFD (MHz)	15.36	REF IN	see CDCE72010 FPGA, 3720 REF	Red T	4448080	
Rx Path					1	
PGA870 Rx1 Path G	ain -11.5	dB		ADS42xx/ADS	58C2x Regis	ster
PGA870 Rx1 Path G	≽ain11.5	dB PGA8	70 gain range IR to 200R is 0 5dR steps	ADS42xx/ADS ADDR	58C2x Regis	ster
PGA870 Rx1 Path G PGA870 Rx2 Path G	eain -11.5 ∋ain -11.5	dB PGA8 dB <sup>-11.5d</sup>	70 gain range IB to 20dB in 0.5dB steps	ADS42xx/ADS ADDR	58C2x Regis	RD WR DISPLAY

Figure 49. RX Path

# 7.7.1 TRF3720-2 Panel

The TRF3720-2 panel provides the LO frequency for the RX1 and RX2 mixers. Programming of this panel is identical to TRF3720-1 panel in the TX section. See *TX and Feedback, TRF3720-1* for an overview of this panel.

# 7.7.2 RX Path Panel

The RX Path panel gives the user the ability to program the RX path 1 PGA870 gain, RX path 2 PGA870 gain, and the Dual RX ADC. This panel behaves much like the *TX and Feedback, Feedback Path* programming. See *TX and Feedback, Feedback Path* for an overview of this panel.

# 8 Typical Performance Numbers

# 8.1 TSW3725 Electrical Characteristics

PARAMETER	TEST CONDITION	TYP	UNIT
DC PARAMETERS			
Supply voltage		6	V
Supply current	TX1 TX2 EP DX1 DX2 ON: default configuration	3.2	А
Supply current		19.2	W
DM/DN ourrept	TV4 TV2 ED DV4 DV2 DWDNL default configuration		A
		11.4	W
SERIAL INTERFACE PAR	RAMETERS		
FCLK (maximum)		5	MHz

# 8.2 TSW3725 Electrical Characteristics

Test conditions (unless otherwise noted): Power = 6 V, TX attn = 0 dB, DAC3484 IF=153.6 MHz, DAC3484 QMC gain setting = 0.5, DAC clk = 614.4 MHz, Fractional LO

PARAMETER		TEST CONDITION	TYP	UNIT
TRANSMIT PARAME	TERS		r	
TX LO		Default schematic		
	Max freq	Limited by LPF on LO path	2200	MHz
Min free		Limited by splitter on LO path	1350	MHz
RF output power		RFOut = 1550 MHz to 2250 MHz	6	dB
RF output	Max		31.75	dB
attenuation	Min		0	dB
	step size		0.25	dB
Cain flatnoss		RF = 1650 MHz to 2250 MHz, TX attn = 0	1	dB
Gain flatness		RF = 1650 MHz to 2250 MHz, TX attn = 15	1	dB
		Pout = -16 dBm, integrate 1 kHz to 10 MHz		
Output noise		RF out = 1550 MHz	410	mdeg
		RF out = 1900 MHz	360	mdeg
		RF out = 2250 MHz	380	mdeg
OIP2		RF out = 2050 MHz; fbb = 5 MHz, 6 MHz	45	dBm
OIP3		RF out = 2050 MHz; fbb = 5 MHz, 6 MHz	33	dBm
Sideband	Unadjusted		-38	dBc
suppression	Adjusted	Hand-tuned for given temp/frequency	-70	dBc
Carrier	Unadjusted		-22	dBm
	Adjusted	Hand-tuned for given temp/frequency	-70	dBm
		TX2 to TX1 (aggressor to victim)	68	dB
		FB1 to TX1	95	dB
		FB2 to TX1	95	dB
		RX1 to TX1	90	dB
Crosstall		RX2 to TX1	90	dB
Crossiaik		TX1 to TX2 (aggressor to victim)	78	dB
		FB1 to TX2	85	dB
		FB2 to TX2	95	dB
		RX1 to TX2	90	dB
		RX2 to TX2	90	dB



Typical Performance Numbers

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# 8.3 TSW3725 Electrical Characteristics

Test conditions (unless otherwise noted): Power = 6 V, TX attn = 0 dB, DAC3484 IF=153.6 MHz, DAC3484 QMC gain setting = 0.5, DAC clk = 614.4 MHz, Fractional LO

PARAMETER	TEST CONDITION	TYP	UNIT							
TRANSMIT PARAMETERS										
ACPR LTE Single Carrier	TM1.1									
	RF out = 1700 MHz	-70	dBc							
ACPR: 5 MINZ DW	RF out = 2050 MHz	-70	dBc							
ACPR: 10 MHz BW	RF out = 1700 MHz	-69	dBc							
	RF out = 2050 MHz	-69	dBc							
	RF out = 1700 MHz	-67	dBc							
ACER. 20 IVINZ DVV	RF out = 2050 MHz	-67	dBc							
EVM LTE Single Carrier 1	ГМ ПОЛИТИИ ПОЛИ									
	RF out = 1700 MHz	0.85	%rms							
	RF out = 2050 MHz	0.85	%rms							
	RF out = 1700 MHz	0.85	%rms							
	RF out = 2050 MHz	0.85	%rms							
	RF out = 1700 MHz	0.85	%rms							
	RF out = 2050 MHz	0.85	%rms							

### 8.4 TSW3725 Electrical Characteristics

Test conditions (unless otherwise noted): Power = 6 V, RX PGA Gain = 20 dB, IF Frequency=140 MHz, ADC clk = 204.8 MHz, Fractional LO = 1800 MHz

PARAMETER		TEST CONDITION	TYP	UNIT
RECEIVE PARAMETER	RS			
RX LO		Default schematic		
	Max freq	Limited by LPF on LO path	2200	MHz
	Min freq	Limited by splitter on LO path	1350	MHz
IF filter		Frequency	140	MHz
		BW	20	MHz
IF programmable gain	Max		20	dB
	Min		-11.5	dB
	Step size		0.5	dB
Idle channel noise		LO=1880 MHz	–153	dBF <sub>s</sub> /Hz
SNR		ADC amplitude = –1 dBFs, PGA = 20 dB notch 6.25 MHz BW LO noise around carrier	65	dBc
HD2		ADC input amplitude = $-1$ dBFs, PGA = 10 dB	73	dBc
HD3		ADC input amplitude = $-1$ dBFs, PGA = 10 dB	65	dBc
Maximum RF input amp	litude	ADC input amplitude = $-1$ dBFs, PGA = 20 dB	-9	dBm
		ADC input amplitude = $-1$ dBFs, PGA = 10 dB	1	dBm
		ADC input amplitude =-1 dBFs, PGA = 5 dB	6	dBm
P1dB		RX input	8	dBm
OIP3		PGA = 20 dB, RF1 = 1690 MHz, RF2 = 1700.7 MHz, LO = 1840 MHz, Ain = –9 dB	40	dBm
EVM LTE Single Carrie	er LTE Upli	ink(SC-FDMA), 64QAM		
EVM: 5 MHz BW		RF in = 1700 MHz, RX input power = -30 dBm	0.7	%rms
		RF in = 2050 MHz, RX input power = -30 dBm	0.8	%rms
EVM: 10 MHz BW		RF in = 1700 MHz, RX input power = -30 dBm	0.8	%rms
		RF in = 2050 MHz, RX input power = -30 dBm	0.8	%rms
EVM: 20 MHz BW		RF in = 1700 MHz, RX input power = -30 dBm	0.8	%rms
		RF in = 2050 MHz, RX input power = -30 dBm	0.9	%rms



Typical Performance Numbers

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### 8.5 TSW3725 Electrical Characteristics

Test conditions (unless otherwise noted): Power = 6 V, RX PGA Gain = 20 dB, IF Frequency=153.6 MHz, ADC clk = 204.8 MHz, Fractional LO = 1990 MHz

PARAMETER	TEST CONDITION	TYP	UNIT
FEEDBACK PARAMETERS		1	4
FB LO	Default schematic		
Max freq	Limited by LPF on LO path	2200	MHz
Min freq	Limited by mixer input frequency range	1700	MHz
FB Filter	Frequency	153.6	MHz
	BW	100	MHz
FB programmable gain			
Max		20	dB
Min		-11.5	dB
step size		0.5	dB
Idle channel noise	LO = 2140 MHz	150	dBF <sub>s</sub> /H z
SNR	ADC amplitude = -1 dBFs, PGA=20dB notch 6.25 MHz BW LO noise around carrier	63	dBc
HD2	ADC input amplitude = -1 dBFs, PGA = 20 dB	73	dBc
HD3	ADC input amplitude = -1 dBFs, PGA = 20 dB	87	dBc
Maximum RF input amplitude	ADC input amplitude = -1 dBFs, PGA = 20 dB	-3	dBm
	ADC input amplitude = -1 dBFs, PGA = 10 dB	7	dBm
	ADC input amplitude = $-1$ dBFs, PGA = 5 dB	12	dBm
P1dB	RX input	23.3	dBm
OIP3	PGA = 20 dB, RF1 = 1847 MHz, RF2 = 1846 MHz, LO = 2000 MHz, Ain = -6.5 dB	41	dBm
ACPR LTE Single Carrier TM	1.1		
ACPR: 5 MHz BW	RF in = 1700 MHz; FB input power = -10 dBm	-67	dBc
	RF in = 2050 MHz; FB input power = -10 dBm	-67	dBc
ACPR: 10 MHz BW	RF in = 1700 MHz; FB input power = -10 dBm	-65	dBc
	RF in = 2050 MHz; FB input power = -10 dBm	-65	dBc
ACPR: 20 MHz BW	RF in = 1700 MHz; FB input power = -10 dBm	-62	dBc
	RF in = 2050 MHz; FB input power = -10 dBm	-62	dBc
EVM LTE Single Carrier TM3.1			
EVM: 5 MHz BW	RF in = 1700 MHz; FB input power = -20 dBm	0.6	%rms
	RF in = 2050 MHz; FB input power = -20 dBm	0.6	%rms
EVM: 10 MHz BW	RF in = 1700 MHz; FB input power = -20 dBm	0.6	%rms
	RF in = 2050 MHz; FB input power = -20 dBm	0.6	%rms
EVM: 20 MHz BW	RF in = 1700 MHz; FB input power = -20 dBm	0.7	%rms
	RF in = 2050 MHz; FB input power = -20 dBm	0.7	%rms



 $R_FOUT = 953.6 MHz$ 

R<sub>F</sub>OUT = 1703.6 MHz

R<sub>F</sub>OUT = 2053.6 MHz

#### 9 **Typical Performance Plots**







Figure 51. Tx EVM vs Frequency/Attenuation LTE 10 MHz TM3.1

-60

-62

-64



Figure 52. Tx EVM vs Frequency/Attenuation LTE 20 MHz TM3.1



MHz TM1.1



Figure 53. Tx ACLR vs Frequency/Attenuation LTE 5 MHz TM1.1



Figure 54. Tx ACLR vs Frequency/Attenuation LTE 10 Figure 55. Tx ACLR vs Frequency/Attenuation LTE 20 MHz TM1.1





Figure 60. Rx EVM vs Frequency/RF Input Amplitude LTE 5-MHz Uplink, 64 QAM

Figure 61. Rx EVM vs Frequency/RF Input Amplitude LTE 10-MHz Uplink, 64 QAM





Typical Performance Plots



PGA870 Gain (dB) Figure 64. Rx Idle Channel Noise vs PGA870 Gain Setting



140

160

180

RF=953.6MHz RF=1703.6MHz

RF=2053.6MHz

RF=953.6MHz

RF=1703.6MHz

RF=2053.6MHz

RF=2403.6MHz

-20

-10

G000

200

G000

Figure 65. FB EVM vs Input Amplitude/Frequency LTE 5 MHz TM3.1

5

4

3

2

1

0

\_60

LTE Single Carrier

20MHz BW TM3.1

PGA870 Gain=20dB

-50

EVM (%)



10 MHz TM3.1



Amplitude (dBm)

-40

-30











Figure 69. FB ACLR vs Input Amplitude/Frequency LTE 10 MHz TM1.1



LTE 20 MHz TM1.1







# **10 Programming Information**

In Stand-Alone mode the TSW3725 GUI handles all the serial interface programming. However, as a debug or development aid, the following information is provided.

The following table lists the device ids required to access the serial interface of given device.

Device ID [xxxx]	Device P/N	Schematic Designator	Description	Comment
1	DAC3484	U1	TX quad DAC	
2	ADS4149	U17	FB ADC	
3	ADS4249	U13	Dual RX ADC	
4	TRF3720-1	U27	TX and FB LO	
5	TRF3720-2	U31	RX LO	
6	PGA870 - RX1	U40	RX path 1	
7	PGA870 - RX2	U43	RX path 2	
8	PGA870 - FB	U50	FB feedback	
9	PE43701 - TX_1	U9	TX path 1	
10	PE43701 - TX_2	U12	TX path 2	
11	CDCE72010	U23	clock	
14	MISC		FB SWITCH and PGA PWDN BITS	D0: HIGH D1: FB SWITCH: CTRL1_PE4257 D2: FB SWITCH: CTRL2_PE4257 D3: RX1 PGA870 PWDN BIT D4: RX2 PGA870 PWDN BIT D5: FB PGA870 PWDN BIT

The following table lists the bit sequence that the TSW3725 expects to receive from the SCBP board

MSB>LSB																																
Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	- 7	6	5	4	3	2	1	0
				N	A	A Address								Data																		
DAC3484									- 7	6	-5	4	3	2	1	0	15	14	13	12	11	10	9	8	- 7	6	-5	4	3	2	1	0
								N	A								Address							Data								
ADS4149																	- 7	6	-5	4	3	2	1	0	- 7	6	- 5	- 4	3	2	1	0
						NA										1	٨dd	ress	6			Data										
ADS4249																	- 7	6	-5	- 4	3	2	1	0	- 7	6	-5	- 4	3	2	1	0
	Address Data																															
TRF3720	0	1	2	3	4	0	1	2	З	- 4	-5	6	-7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
													N	A										G	Gain Bits							
PGA870																											-5	- 4	3	2	1	0
								N	A								Data							Address								
PE43701																	0	1	2	3	- 4	-5	6	- 7	0	1	2	3	4	5	6	-7
	1	Add	ress	3														Da	ata													
CDCE72010	0	1	2	3	0	1	2	3	4	-5	6	- 7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
													N	A															Da	ta		
RESERVED																											-5	- 4	3	2	1	0

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It is important to operate this EVM within the input voltage range of 5.5 V to 6.25 V and the output voltage range of 0 V to 5 V. Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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#### General Statement for EVMs including a radio

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#### For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

#### Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

#### FCC Interference Statement for Class B EVM devices

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

#### For EVMs annotated as IC – INDUSTRY CANADA Compliant

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#### Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### Concerning EVMs including detachable antennas

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Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

#### Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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- 2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
- 3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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