

User's Guide SNAU118A–December 2011–Revised February 2018

LMK01801 User's Guide

This user's guide describes how to set up and operate the LMK01801 evaluation module (EVM). The LMK01801 Evaluation Board simplifies evaluation of the LMK01801 Dual Clock Buffer Divider. Configuring and controlling the board is accomplished using Texas Instrument's TICS Pro software, which can be downloaded from TI's website: http://www.ti.com/tool/ticspro-sw. The LMK01801 can also be configured to operate in a pin control mode via headers on the PCB.



Figure 1. LMK01801 EVAL



Contents

1	Block [Diagram	3
2	Evalua	tion Board Kit Contents	4
3	Quick	Start – SPI Mode (TICS Pro)	6
	3.1	Quick Start – SPI Mode (TICS Pro) Description	7
4	Quick	Start – Pin Control Mode	8
	4.1	Quick Start – Pin Control Mode Description	9
	4.2	Pin Control Modes	9
5	Using ⁻	TICS Pro to Program the LMK01801	10
	5.1	Start TICS Pro Application	10
	5.2	Select Device	10
	5.3	Program/Load Device	10
	5.4	Restoring a Default Mode	11
	5.5	Enable Clock Outputs	12
6	Evalua	tion Board Inputs/Outputs	14
7	Recom	nmended Test Equipment	15
	7.1	Power Supply	15
	7.2	Phase Noise / Spectrum Analyzer	15
Appen	dix A	TICS Pro Usage	16
Appen	dix B	Typical Phase Noise Performance Plots	21
Appen	dix C	Schematics	29
Appen	dix D	Bill of Materials	37
Appen	dix E	Balun Information	40
Appen	dix F	Differential Voltage Measurement Terminology	41

List of Figures

1	LMK01801 EVAL	. 1
2	LMK01801 Block Diagram	. 4
3	Quick Start - SPI Mode Diagram	. 6
4	Quick Start - Pin Control Mode Diagram	. 8
5	Selecting the LMK01801	10
6	Loading the Device	11
7	Setting the Default Mode	11
8	Setting Divider, CLKout_TYPE, Enabled for CLKoutX on "Bank A" Page	12
9	CLKout_TYPEs	12
10	TICS Pro - User Controls Page	17
11	TICS Pro - Raw Registers Page	18
12	TICS Pro - Bank A Page	19
13	TICS Pro - Bank B Page	19
14	TICS Pro - Burst Page	20
15	LMK01801 Phase Noise @ 100 MHz with Output Divider = 1	22
16	LMK01801 Phase Noise @ 100 MHz with Output Divider = 4	23
17	LMK01801 Phase Noise @ 983.04 MHz with Output Divider = 1	23
18	LMK01801 Phase Noise @ 983.04 MHz with Output Divider = 4	24
19	Phase Noise Measurement Set-Up	25
20	Noisy vs. Clean Phase Noise	26
21	LMK01801 Sample Clock Output Waveforms	27
22	CLKout12 and CLKout13 No Analog Delay	28
23	CLKout12 with 100 pSec of Delay Relative to CLKout13	29
24	NOTE: The 51 Ω resistors R310 and R318 will need to be removed for the USB2ANY to assert IC_SYNC0 and IC_SYNC1.	31

2



Block Diagram

25	Typical Balun Frequency Response	40
26	Two Different Definitions for Differential Input Signals	41
27	Two Different Definitions for Differential Output Signals	42

List of Tables

Clock Output Configuration	4
EN_PIN_CTRL = LOW Configuration	9
EN_PIN_CTRL = HIGH Configuration	9
LMK01801 Evaluation Board I/O	14
Phase Noise Output Test Configuration	21
LMK01801 Test Conditions	21
Clock Output Modes	27
Common Bill of Materials for Evaluation Boards	37
	Clock Output Configuration EN_PIN_CTRL = LOW Configuration EN_PIN_CTRL = HIGH Configuration LMK01801 Evaluation Board I/O Phase Noise Output Test Configuration LMK01801 Test Conditions Clock Output Modes Common Bill of Materials for Evaluation Boards

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1 Block Diagram

Figure 2 illustrates the functional architecture of the LMK01801 clock divider buffer. The LMK01801 is a very low noise solution for clocking systems that require distribution and frequency division of precision clocks. The LMK01801 features extremely low residual noise, frequency division, digital and analog delay adjustments, and fourteen (14) programmable differential outputs: LVPECL, LVDS and LVCMOS (2 outputs per differential output). The LMK01801 features two independent inputs that can be driven differentially or in single-ended mode. The first input drives output Bank A consisting of eight (8) outputs. The second input drives output Bank B consisting of six (6) outputs.

3





Figure 2. LMK01801 Block Diagram

2 Evaluation Board Kit Contents

The evaluation board kit contains:

- An LMK01801 Evaluation board.
- USB2ANY-UWIRE
 - Evaluation board instructions are downloadable from the product folder on Texas Instruments' website, http://www.ti.com/.

TICS Pro is the recommended program to program the evaluation board with the USB2ANY interface adapter and the USB2ANY-uWire Adapter Board.

Clock	Output Type	Output Connector Installed
0	LVPECL	Yes
1	LVPECL	No
2	LVPECL	Yes
3	LVPECL	No
4	LVPECL	Yes
5	LVPECL	No
6	LVPECL	Yes
7	LVPECL	No
8	LVPECL	Yes

Table 1. Clock Output Configuration



Clock	Output Type	Output Connector Installed
9	LVPECL	Yes
10	LVPECL	Yes
11	LVPECL	Yes
12	LVPECL	Yes
13	LVPECL	Yes

Table 1. Clock Output Configuration (continued)

5



Quick Start – SPI Mode (TICS Pro)

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3 Quick Start – SPI Mode (TICS Pro)



Figure 3. Quick Start - SPI Mode Diagram

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3.1 Quick Start – SPI Mode (TICS Pro) Description

- 1. Connect a voltage of 3.3 V to either the V_{cc} SMA connector or the alternate terminal block.
- 2. Connect a reference clock from a signal generator or other source. Exact frequency depends on programming.
- 3. Connect the PC to USB2ANY. Connect the USB2ANY-uWire Adapter Board from USB2ANY with a 10pin ribbon cable. Install jumpers as shown in Figure 3 and connect another 10-pin ribbon cable to the uWire header on the EVM.
- 4. Install jumpers on TYPE0, TYPE1, TYPE2, DivVal0, DivVal1, DivVal2 in the middle uWire (pins 3,4) position but NOT on EN_PIN_CTRL.
- 5. Program the device with TICS Pro. TICS Pro is available for download at http://www.ti.com/tool/ticsprosw.
 - Select USB2ANY mode from the Communication Setup window. To access this, select "USB communications" → "Interface". Confirm PC to USB communications by clicking "Identify" to see blinking green LED on USB2ANY.
 - 2. Select LMK04906 from the "Select Device" Menu. Click "Select Device" \rightarrow "Clock Distribution with Divider" \rightarrow "LMK01801".
 - 3. Select a default mode from the "Default configuration" Menu. For the quick start, use "Default configuration".
 - Ctrl+L must be pressed at least once to load all registers. Alternatively click "USB communications" → "Write All Registers" or the "Write All Registers" button on the Raw Registers page.
- 6. Measurements may be made at any CLKout port via its SMA connector if enabled by programming.
 - **NOTE:** If required to assert SYNC signals through USB2ANY, remove resistors R310 and R318. Refer to Section C.2 for details. This is not required for basic functionality. These resistors terminate an external SYNC signal.



Quick Start - Pin Control Mode

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Figure 4. Quick Start - Pin Control Mode Diagram

Quick Start - Pin Control Mode



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4.1 Quick Start – Pin Control Mode Description

- 1. Connect a voltage of **3.3 V** to either the V_{cc} SMA connector or the alternate connector.
- 2. Connect a reference clock from a signal generator or other source. Exact frequency depends on programming.
- 3. Install a jumper on EN_PIN_CTRL header in either the High or Low position.
- 4. Install other jumpers on Type0, Type1, Type2, DivVal0, DivVal1, and DivVal2 headers based on the configurations shown in Table 2 and Table 3.

4.2 Pin Control Modes

For Table 2 and Table 3, LOW is defined as installing a jumper between pins 5 and 6 on the desired header. A HIGH is defined as installing a jumper between pins 1 and 2 on the desired header.

If EN_PIN_CTRL = LOW (jumper installed between header positions 5 and 6) then the following table describes possible output configurations:

Header	Output Groups	Header = Low	Header = Middle	Header = High
TurneQ	CLKout0 to CLKout3		Powerdown	
Турео	CLKout4 to CLKout7	LVDS	LVCMOS (Norm/Inv)	
Type1	CLKout8 to CLKout11	LVDS	LVCMOS (Norm/Inv)	LVPECL
Type2	CLKout12 to CLKout13	LVDS	LVCMOS (Norm/Inv)	LVPECL
DivVal0	CLKout0 to CLKout3 Divider	÷1	÷4	÷2
DivVal1	CLKout4 to CLKout7 Divider	÷1	÷4	÷2
	CLKout8 to CLKout11 Divider	÷1	÷4	÷2
Divvalz	CLKout12 to CLKout13 Divider	÷8	÷512	÷16

Table 2. EN_PIN_CTRL = LOW Configuration

If EN_PIN_CTRL = HIGH (jumper installed between header positions 1 and 2) then the following table describes possible output configurations:

Header	Output Groups	Header = Low	Header = Middle	Header = High
Type0	CLKout0 to CLKout3		LVPECL	
турео	CLKout4 to CLKout7		LVCMOS (Norm/Inv)	
Type1	CLKout8 to CLKout11	Kout8 to CLKout11 LVDS LVCMOS (Norm/Inv)		LVPECL
Type2	CLKout12 to CLKout13	LVDS	LVCMOS (Norm/Inv)	LVPECL
DivVal0	CLKout0 to CLKout7 Dividers	÷1	÷4	÷2
DivVal1	CLKout8 to CLKout11 Divider	÷1	÷4	÷2
DivVal2	CLKout12 to CLKout13 Divider	÷4	÷512	÷16

Table 3. EN_PIN_CTRL = HIGH Configuration

9



5 Using TICS Pro to Program the LMK01801

The purpose of this section is to walk the user through using TICS Pro to make some measurements with the LMK01801 device. For more information on TICS Pro, refer to Appendix A. TICS Pro is available for download at http://www.ti.com/tool/ticspro-sw.

Another option is to use CodeLoader4. The tool page for CodeLoader4 is located at http://www.ti.com/tool/codeloader/.

Before proceeding, be sure to follow the Quick Start in Section 3 to ensure proper connections.

5.1 Start TICS Pro Application

Click "Start" \rightarrow "Programs" \rightarrow "Texas Instruments" \rightarrow "TICS Pro"

The TICS Pro program is installed by default to the Texas Instruments application group.

5.2 Select Device

Click "Select Device" \rightarrow "Clock Distribution with Divider" \rightarrow "LMK01801".

Once started, TICS Pro will load the last used device. To load a new device click "Select Device" from the menu bar, then select the subgroup "Clock Distribution with Divider" and finally the device to load. For this example, the LMK01801 is chosen. Selecting the device does cause the device to be programmed. However, it is advisable to press "Ctrl+L" to ensure programming.

🕅 TI	TICS Pro - LMK01801									
File	USB communications	Select Device	Options	Tools	Default co	nfiguration	Help			
	Import User Device									
	Delete User Device(s)			F		Channel C	ontrol – t0_3_P[
	User Devices			VN		CLKou	t4_7_PC			
	PLL			•		CLKou	t8_11_P			
	PLL + VCO			•		CLKou	t12_13_			
	Clock Distribution with I	Divider		•	LMK010>	√ 0 ►				
	Clock Generator/Jitter C	Cleaner (Single L	.oop)	•	LMK0180	01				
	Clock Generator/Jitter C	Cleaner (Dual Lo	op)	•						
	CDC Devices			•						

Figure 5. Selecting the LMK01801

5.3 Program/Load Device

Press "Ctrl+L"

Alternatively, click "USB communications" \rightarrow "Write All Registers" from the menu to program the device to the current state of the newly loaded LMK01801 file. "Ctrl+L" is the accelerator key assigned to the "Write All Registers" option and is very convenient.

Using TICS Pro to Program the LMK01801

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🔛 TI	TICS Pro - LMK01801										
File	USB communications	Select Device	Options	Tools	Default cont	figuration	Help				
	Interface		Others								
	Write All Registers	Ctrl+L	ode Contro	ol		Channel C	ontrol t0 3 PD				
Bank A Bank B Burst Mode						CLKout4_7_P					
							t12_13_P				

Figure 6. Loading the Device

Once the device has been initially loaded, TICS Pro will automatically program changed registers, so it is not necessary to reload the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the "Options" \rightarrow "AutoUpdate"

Because a default mode will be restored in the next step, this step isn't really needed but is included to emphasize the importance of pressing "Ctrl+L" to load the device at least once after starting TICS Pro, restoring a mode, or restoring a saved setup using the File menu.

5.4 Restoring a Default Mode

Click "Default configuration" \rightarrow "Default Mode"; then

Press "Ctrl+L"

TICS Pro - LMK01801								
File USB communications	Select Device	Options	Tools	Default	configuration	Help		
▲ LMK01801 User Controls Raw Registers Bank A Bank B Burst Mode		Others lode Contro RESET	DOWN	Default N	Aode Channel C CLKou CLKou	control t0_3_PD t4_7_PD t8_11_PD		

Figure 7. Setting the Default Mode

For the purposes of this walkthrough a default mode will be loaded to ensure a common starting point. This is important because TICS Pro saves the state of the selected LMK01801 device when exiting the software.

NOTE: Loading a mode does not automatically program the device, so it is necessary to press "Ctrl+L" again to program the device.



5.5 Enable Clock Outputs

- To measure phase noise at the clock outputs:
- 1. Click on the Bank A page.
- 2. Enable an output.
- 3. Then set the:
 - CLKout Type
 - Divide value

	Clock Output			
Clock Divider	LVPECL 1.6	CLKout0	122.88	MHz
. 1	LVPECL 1.6 Y	CLKout1	122.88	MHz

Figure 8. Setting Divider, CLKout_TYPE, Enabled for CLKoutX on "Bank A" Page

NOTE: This CLKoutX frequency value is only valid if the correct clock in value is specified. It may not necessarily represent the actual frequency unless manually entered. This is a mathematical calculation only, not a measured value.

- 4. Connect the clock output SMAs to a spectrum analyzer or signal source analyzer.
 - For LVDS, a balun is recommended such as the ADT2-1T (for frequency range of 0.4 MHz to 450 MHz).
 - For LVPECL
 - 1. A balun can be used, or
 - 2. One side of the LVPECL signal can be terminated with a 50- Ω load and the other side can be run to the test equipment single ended.
 - For LVCMOS
 - 1. One side of the LVCMOS signal can be terminated with a 50- Ω load and the other side can be run to the test equipment single ended.

_		LVPECL 1.6	~
	Р	owerdown	
	Ľ	VDS	
	P	ECL (Low Power)	
	R	Reserved	
	Ľ	VPECL 1.6	
	Ľ	VPECL 2.0	
	Ľ	VCMOS (Norm\Inv)	
	Ľ	VCMOS (Inv\Norm)	
	Ľ	VCMOS (Norm\Norm	n)
	ני	VCMOS (Inv\Inv)	
	Ľ	VCMOS (Off\Norm)	
	Ľ	VCMOS (Off\Inv)	
	Ľ	VCMOS (Norm\Off)	
	ני	VCMOS (Inv\Off)	
	Ľ	VCMOS (Off\Off)	

Figure 9. CLKout_TYPEs



5. The phase noise may be measured with a spectrum analyzer or signal source analyzer

See Appendix B for phase noise plots of the clock outputs



Evaluation Board Inputs/Outputs

6 Evaluation Board Inputs/Outputs

Table 4 contains descriptions of the various inputs and outputs for the evaluation board.

Table 4. LMK01801 Evaluation Board I/O

Connector Name	Input/Output	Description
CLKout0 / CLKout0*, CLKout2 / CLKout2*, CLKout4 / CLKout4*, CLKout6 / CLKout6*, CLKout8 / CLKout8, CLKout9/ CLKout9*, CLKout10 / CLKout10*, CLKout11 / CLKout11*, CLKout12 / CLKout12*, CLKout13 / CLKout13*	Output	Populated connectors. Differential clock output pairs. All outputs are configured in LVPECL mode. On the evaluation board, all clock outputs are AC-coupled to allow safe testing with RF test equipment. All LVPECL/2VPECL clock outputs are terminated to GND with a 240- Ω resistor, one on each output pin of the pair.
V _{cc}	Input	Populated connector. DC power supply for the PCB. Removing R1, R2, or R3 allow for splitting the power to various devices on the board. Note: The LMK01801 Family contains internal voltage regulators for the VCO, PLL and related circuitry. The clock outputs do not have an internal regulator. A clean power supply is required for best performance.
V _{CC2}	Input	Unpopulated connector. Vcc input to power the output planes separately from the Aux Plane. Refer to schematics for more information.
CLKin0/CLKin0*, CLKin1/CLKin1*	Input	Populated connectors. The default board configuration is setup for a single-ended reference source at CLKin0* (CLKin0 pin is AC-coupled to ground). If a DC-coupled clock is used to drive either of the inputs, the high voltage level must be at least 2 volts and the low voltage no greater than 0.4 volts.
uWire	Input/Output	Populated connector. 10-pin header programming interface for the board. Of Most important are the CLKuWire, DATAuWire, and LEuWire programming lines from this header. Each of these signals, TEST, and SYNC0, and SYNC1 can be monitored through test points on the board.
SYNC0, SYNC1	Input	Unpopulated connector. Access to SYNC0 or SYNC1 of device.



7 Recommended Test Equipment

7.1 Power Supply

The Power Supply must be a low noise power supply.

7.2 Phase Noise / Spectrum Analyzer

For measuring phase noise an Agilent E5052A Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052A is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.



Appendix A SNAU118A–December 2011–Revised February 2018

TICS Pro Usage

TICS Pro is the recommended program to program the evaluation board with the USB2ANY interface adapter and the USB2ANY-uWire Adapter Board. TICS Pro can also be used to generate register maps for programming the device. This appendix outlines the basic purpose and usage of each page. TICS Pro is available for download at http://www.ti.com/tool/ticspro-sw.

A.1 TICS Pro Tips

• Mousing over different controls will display some help prompt with the register address, data bit location/length, and a brief register description in the lower left Context help pane.

A.2 Communication Setup

The USB communications window allows the USB2ANY or DemoMode to be selected. In case multiple evaluation boards are to be connected and run with multiple instances of TICS Pro, the dropdown box will allow specific USB2ANY devices to be selected. Pressing the identify button will identify which USB2ANY is currently selected. Devices used by other instances of TICS Pro won't display in this list.



A.3 User Controls

The User Controls page has controls not included on one of the previously discussed dedicated pages.

🔀 TICS Pro - LMK01801					- 🗆 X
Eile USB communications	Select Device Options Tool	s Default configuration <u>H</u> elp			
▲ LMK01801 User Controls Raw Registers Bank A Bank B Burst Mode General Context Field Name : Syuc1 0100	Others Mode Control RESET POWERDOWN Channel Control CLKout0_3_PD CLKout4_7_PD CLKout8_11_PD CLKout12_13_PD	CLKin0_BUF_TYPE Bipolar ▼ CLKin1_BUF_TYPE Bipolar ▼	SYNC SYNC1_QUAL Off • SYNC0_POL_INV SYNC1_POL_INV NO_SYNC_CLKout0_3 NO_SYNC_CLKout4_7 NO_SYNC_CLKout8_11 NO_SYNC_CLKout12_13	SYNC0_FAST SYNC1_FAST SYNC0_AUTO SYNC1_AUTO	Readback uWireLock
Register Name: R3 Start Bit : 11 Stop Bit : 12 Length : 2	Pins Program Pins SYNC0 SYNC1 TRIGGER				
Loading Device LMK01801 Detected 1 USB2ANY interfa Completed loading Device L	aces MK01801. Version = 2017-01-09	, v2.0.1	Connection Mode:		kas Instruments

Figure 10. TICS Pro - User Controls Page



A.4 Raw Registers Page

The **Raw Register** page displays the register map including address. The address bits have the shaded background and are not editable. The unshaded bits are the data bits. This register map may be directly manipulated by clicking into the bit field, moving around with the arrow keys, and typing '1' or '0' to change a bit.

All registers may be read or written in addition to individual registers. For individual register read/write, the active register is highlighted in the list of registers and displayed in the top right. An individual register or field may be read back by entering the name into the bottom right and clicking the "Read" button.

Register maps may be exported, but also imported. The import format may simply be the address and register data in hex format as illustrated in the address/value column, one register to a line.

🔀 TICS Pro - LMK01801						- 🗆 X
Eile USB communications	Select Device Options Tools	Default configuration	<u>H</u> elp			
 ▲ LMK01801 User Controls Raw Registers Bank A Bank B Burst Mode General Context Register Name: R0 (INIT) Register Name(in Hex): R0x0 	Register Map Register Name Value/Address R0 (INIT) 0x48108020 R0 0 0x48108000 R1 0x0020021 0x00200221 R2 0x00200023 0x00200033 R4 0x04540054 0x0020495 R15 0x000005EF 0x000005EF	3 3 2 2 2 2 2 2 1 0 9 8 7 6 5 4 0 1 0		1 1 1 1 0 0 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 7 6 5 4 3 2 1 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0 1 1 0 1 0 1 0 1 0 1 0 1 1 1 1 0 1 1 1 1 	Data 0x4810B020 Write Register Read Register Read All Registers Write All Registers Write All Register Map Export Register Map Export Register Map Register/Field Name Name Value Read
Loading Device LMK01801 Detected 1 USB2ANY interfa	aces MK01801 Version = 2017-01-09	v2 0 1	Protoc	ol: UWIRE		
Completed loading Device L	Millo 1001. Version – 2017-01-09,	V2.U. I	↓ Conne	ction Mode: USB2ANY	🜵 Texas In	ISTRUMENTS

Figure 11. TICS Pro - Raw Registers Page

A.5 Bank A Page

The **Bank A** page allows control of the clock outputs format and other options relating to the clock outputs, 0 through 7.





Figure 12. TICS Pro - Bank A Page

A.6 Bank B Page

The **Bank B** page allows control of the clock outputs format and other options relating to the clock outputs 8 through 13. For outputs 12 and 13, the user can enable and set the clock output delay value.



Figure 13. TICS Pro - Bank B Page



Burst Page

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A.7 Burst Page

The Burst page allows the user to program sequences of register programming or pin control.

🛗 TICS Pro - LMK018	01						- 🗆 X
<u>F</u> ile USB communica	ations <u>S</u> elect De	evice <u>O</u> ptions	Tools	Default configuration	n <u>H</u> elp		
 LMK01801 User Controls Raw Registers Bank A Bank B Burst Mode General Context 							Operations Delay 1 Sec Load Register Set Pins
Burst Mode							Edit Options
							Delete
							Delete All
							Overwrite?
	Load	Save		Run	top	Pattern	Loop?
Loading Device LMK0 Detected 1 USB2ANY Completed loading De	/1801 / interfaces evice LMK01801. '	Version = 2017-()1-09, v	/2.0.1		Co	nnection Mode: USB2ANY

Figure 14. TICS Pro - Burst Page



Typical Phase Noise Performance Plots

B.1 Clock Outputs

The LMK01801 Family features LVDS, LVPECL, 2VPECL, and LVCMOS types of outputs. Include are the phase noise plots for the following outputs.

Device	CLKoutX	Output Divide	Output Type
	8	1	LVPECL
	8	4	LVPECL
	8	1	2VPECL
1 MK01901	8	4	2VPECL
LIVINOTOOT	4	1	LVDS
	4	4	LVDS
	4	1	LVCMOS(Norm/Inv)
	4	4	LVCMOS(Norm/Inv)

Table 5. Phase Noise Output Test Configuration

B.2 Clock Output Measurement Technique

The measurement technique for each output type varies.

LVPECL/2VPECL – Measured by using an Minicircuits ADT2-1T balun on the input and on the output.

LVCMOS and LVDS – Measured by using an Minicircuits ADT2-1T balun on the output and single ended input.

Parameter	Test Case 1	Test Case 2	Test Case 3	Test Case 4
Input Source	Wenzel XTAL	Wenzel XTAL	SMHU	Rohde & Schwarz SMHU
Input Frequency	100 MHz	100 MHz	983.04 MHz	983.04 MHz
Input Power	0 dBm	0 dBm	0 dBm	0 dBm
Output Divider	1	4	1	4
Figure	Figure 15	Figure 16	Figure 17	Figure 18

Table 6. LMK01801 Test Conditions



Clock Output Measurement Technique





Figure 15. LMK01801 Phase Noise @ 100 MHz with Output Divider = 1





B.2.2 LMK01801 Phase Noise, CLKin = 100 MHz, Output Divider = 4

Figure 16. LMK01801 Phase Noise @ 100 MHz with Output Divider = 4



B.2.3 LMK01801 Phase Noise, CLKin = 983.04 MHz, Output Divider = 1





Clock Output Measurement Technique

B.2.4 LMK01801 Phase Noise, CLKin = 983.04 MHz, Output Divider = 4



Figure 18. LMK01801 Phase Noise @ 983.04 MHz with Output Divider = 4



B.3 Phase Noise Measurement



Figure 19. Phase Noise Measurement Set-Up

The phase noise of the signal source will impact the measured phase noise of the LMK01801.







Figure 20. Noisy vs. Clean Phase Noise



B.4 LMK01801 Sample Output Waveforms



Figure 21. LMK01801 Sample Clock Output Waveforms

The output waveforms shown in Figure 21 were taken at a clock in frequency of 122.88 MHz, AC coupled. These measurements follow the VID voltage convention – See Appendix F for more information.

The output modes are as follows:

Table 7. Clock Output Modes

Trace	Clock Output	Output Type
A	CLKout0	2VPECL
В	CLKout1	PECL (Low Power)
С	CLKout4	LVDS
D	CLKout5	LVCMOS (Normal/Invert)

B.5 LMK01801 Analog Delay Sample Data

The sample analog delay data was taken at a clock in frequency of 122.88 MHz, output format of 2VPECL. Notice in Figure 22 that with analog delay enabled there is approximately 460 ps of delay. Then, in Figure 23, we added 100 ps of delay and the resulting delay is approximately 550 ps.



LMK01801 Analog Delay Sample Data



Figure 22. CLKout12 and CLKout13 No Analog Delay



Figure 23. CLKout12 with 100 pSec of Delay Relative to CLKout13



Appendix C SNAU118A–December 2011–Revised February 2018

Schematics





and CG2 supply planes.



Main - LMK01801

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C.2

IC_SYNC1>> R310 Vcc6_CLKin1 Vcc8_Digital Vcc7_CLKout_CG3 51.0 -GND IC_uWireDATA Q, Q. Q, Q, CLKout12_P IC_uWireCLK CLKout13_N CLKout12_N CLKout13_P CLKin1_N CLKin1_P 4 39 88 4 Ω 40 5 U1 LMK01801 Vcc8_DIG CLKout13 CLKout13* CLKout12 CLKin1 CLKout12* CLKin1* DATAuWire/CLKoutDIV0 CLKout13/12 KuWire/CLKoutDIV1 KoutTYPE2 /cc6_CLKin1 Vcc7 36 CLKout11 P 🗢 LEuWire/CLKoutDIV2 건 IC_uWireLE CI Kout11 CLKout0 P 2 35 CLKout11_N , C CLKout0 CLKout11 CLKout0_N_3 CLKout10_N 🔎 CLKout0* CLKout10 CLKout1_N 4 33 CLKout10_P 🔑 CLKout1* CLKout10 CLKout1_P 5 CLKout1 Vcc5_CLKout8_9_10_1 Vcc5_CLKout_CG2 CLKout9_P 🔎 🗢 Vcc1_CLKout_CG0 Vcc1 CLKout0 1 2 3 CLKout9 LMK01801 CLKout2_P 7 30 CLKout9_N 🗢 CI Kout2 CLKout9 29 CLKout8_N 🗡 CLKout2_N 8 CLKout8* CLKout2⁴ _CLKout8_P _ CLKout3_N 9 28 CLKout3* CLKout8 DAP PAD CLKout3 P 10 CI Kout3 EN PIN CTRL - IC_EN_PIN_CTRL 11 26 IC_TEST Test/CLKoutTYPE0 Bias 12 25 IC_SYNC0 SYNC0/CLKoutTYPE1 Vcc4_Bias PC358 R318 C359 /cc2_CLKin0 1µF CLKout6* CLKout7* CLKout4 CLKout5 CLKin0 CLKin0* CLKout4 CLKout5 5 CLKout6 CLKout7 ŝ Vcc4_Bias Э 6 4 2 2 22 23 CLKout6_N CLKout7_N CLKout6_P CLKout7_P CLKout4_N CLKout5_N CLKout5_P CLKin0_N CLKout4 CLKin0 ő Ö Ö 0 Ő Vcc3_CLKout_CG1 Vcc2_CLKin0

Designators greater than and equal to 200 are placed on bottom of PCB

Figure 24. NOTE: The 51 Ω resistors R310 and R318 will need to be removed for the USB2ANY to assert IC_SYNC0 and IC_SYNC1.



C.3 Inputs

Inputs







Inputs









Clock Outputs

C.4 Clock Outputs

C.4.1 Clock Outputs Page 1





Notes:

1. Designators greater than and equal to 300 are placed on bottom of PCB











Notes:

1. Designators greater than and equal to 300 are placed on bottom of PCB



Clock Outputs



Notes:

1. Designators greater than and equal to 300 are placed on bottom of PCB



Bill of Materials

D.1 Bill of Materials

ltem	Designator	Description	RoHS	Manufacturer	PartNumber	Quantity
CAP	ACITORS			1		
1	C1, C7, C8, C10, C12, C13, C16, C17, C18, C19, C22, C23, C24, C25, C28, C29, C30, C31, C35, C36, C37, C40, C41, C42, C43, C46, C47, C48, C49, C52, C53, C56, C301, C302, C304, C314, C321	CAP, CERM, 0.1 μF, 25 V, ±5%, X7R, 0603	Y	Kemet	C0603C104J3RACT U	37
2	C4	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, 0603	Y	Kemet	C0603C101J5GACT U	1
3	C5, C55, C313, C320, C325, C328, C338, C342, C359	CAP, CERM, 1 µF, 10 V, ±10%, X5R, 0603	Y	Kemet	C0603C105K8PACT U	9
4	C34, C326, C329, C339, C343	CAP, CERM, 0.1 µF, 25 V, ±10%, X7R, 0603	Y	Kemet	C0603C104K3RACT U	5
5	C54, C303, C312, C319	CAP, CERM, 10 µF, 10 V, ±10%, X5R, 0805	Y	Kemet	C0805C106K8PACT U	4
6	C318, C348	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0603	Y	TDK	C1608X7R1C104K	2
7	C341, C345	CAP, CERM, 1 µF, 16 V, ±10%, X7R, 0603	Y	ТДК	C1608X7R1C105K	2
8	C333, C346	CAP, CERM, 2200 pF, 100 V, ±5%, X7R, 0603	Y	AVX	06031C222JAT2A	2
9	C347	CAP, CERM, 10 µF, 10 V, ±20%, X5R, 0805	Y	Kemet	C0805C106M8PAC TU	1
10	C349	CAP, CERM, 4.7 μF, 10 V, ±10%, X5R, 0603	Y	Kemet	C0603C475K8PACT U	1
11	C337, C350	CAP, CERM, 0.01 µF, 25 V, ±5%, C0G/NP0, 0603	Y	ТDК	C1608C0G1E103J	2
12	C351, C352	CAP, CERM, 0.47 μF, 25 V, ±10%, X7R, 0603	Y	MuRata	GRM188R71E474K A12D	2
CON	NECTORS	·		I		
13	CLKin0*, CLKin1, CLKin1*, CLKout0, CLKout0*, CLKout2, CLKout2*, CLKout4, CLKout4*, CLKout6, CLKout6*, CLKout8, CLKout8*, CLKout10, CLKout10*, CLKout12, CLKout12*, CLKout13, CLKout13*, Vcc, Vtune	Connector, SMT, End launch SMA 50 Ohm	Y	Emerson Network Power	142-0701-851	21

Table 8. Common Bill of Materials for Evaluation Boards

SNAU118A–December 2011–Revised February 2018 Submit Documentation Feedback



ltom	Decimator	Description	Delle	Manufacturar	DertNumber	Quantitu
item	Designator		копо	Wanufacturer	Partinumber	Quantity
14	J1	2POS OR	Y	Weidmuller	1594540000	1
RESI	STORS			1	1	
15	R2, R179, R303, R329, R332, R334, R336, R344, R346, R349	FB, 1000 Ω, 600 mA, 0603	Y	Murata	BLM18HE102SN1D	10
16	R3, R5, R10, R16, R17, R21, R22, R301, R305, R331, R335, R337, R338, R347, R350, R352, R356	RES, 0 Ω, 5%, 0.1 W, 0603	Y	Vishay-Dale	CRCW06030000Z0 EA	17
17	R4, R11	RES, 0 Ω, 5%, 0.125 W, 0805	Y	Vishay-Dale	CRCW08050000Z0 EA	2
18	R7, R30, R46, R52, R68, R74, R90, R96, R112, R118, R134, R140, R156, R310, R318	RES, 51.0 Ω, 1%, 0.1 W, 0603	Y	Yageo America	RC0603FR-0751RL	15
19	R20	RES, 100 Ω, 1%, 0.1 W, 0603	Y	Yageo America	RC0603FR- 07100RL	1
20	R31, R33, R39, R40, R53, R55, R61, R62, R75, R76, R83, R84, R97, R98, R105, R106, R119, R121, R127, R128, R141, R143, R149, R150, R163, R165, R171, R172	RES, 240 Ω, 1%, 0.1 W, 0603	Y	Yageo America	RC0603FR- 07240RL	28
21	R35, R36, R57, R58, R79, R80, R101, R102, R123, R124, R145, R146, R167, R168	RES, 68 Ω, 5%, 0.1 W, 0603	Y	Vishay-Dale	CRCW060368R0JN EA	14
22	R302	RES, 39k Ω, 5%, 0.1 W, 0603	Y	Vishay-Dale	CRCW060339K0JN EA	1
23	R311, R312, R315, R320, R322, R325, R328	RES, 27k Ω, 5%, 0.1 W, 0603	Y	Vishay-Dale	CRCW060327K0JN EA	7
24	R308, R309, R314, R317, R321, R324, R327	RES, 15k Ω, 5%, 0.1 W, 0603	Y	Vishay-Dale	CRCW060315K0JN EA	7
25	R342, R353, R357	RES, 51k Ω, 5%, 0.1 W, 0603	Y	Vishay-Dale	CRCW060351K0JN EA	3
26	R343, R354	RES, 2.00k Ω, 1%, 0.1 W, 0603	Y	Vishay-Dale	CRCW06032K00FK EA	2
27	R345, R355	RES, 866 Ω, 1%, 0.1 W, 0603	Y	Vishay-Dale	CRCW0603866RFK EA	2
INTE	GRATED CIRCUITS		ŀ			
28	U1	LMK01801				1
29	U300, U301	Micropower 800 mA Low Noise 'Ceramic Stable' Adjustable Voltage Regulator for 1 V to 5 V Applications	Y	Texas Instruments	LP3878SD-ADJ	2
30	U302	Ultra Low Noise, 150 mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor	Y	Texas Instruments	LP5900SD-3.3	1
31	uWire	Low Profile Vertical Header 2x5 0.100"	Y	FCI	52601-G10-8LF	1

Table 8. Common Bill of M	laterials for Evaluation	Boards (continued)
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Item	Designator	Description	RoHS	Manufacturer	PartNumber	Quantity
32	DivVal0, DivVal1, DivVal2, EN_PIN_CONTROL, TYPE0, TYPE1, TYPE2	Header, 2.54mm, 3x2, Gold, SMT	Y	Samtec	TSM-103-01-L-DV	7
OTHER						
33	Kitting Item	USB2ANY-UWIRE	Y	Any	SV600857-001	1
34	SH_DivVal0_3-4, SH_DivVal1_3-4, SH_DivVal2_3-4, SH_EN_PIN_CONTROL _6-FLOAT, SH_TYPE0_3-4, SH_TYPE1_3-4, SH_TYPE2_3-4	Jumper, Shunt, 100mil, Gold plated, Black	Y	ЗМ	969102-0000-DA	7
35	S1, S2, S3, S4, S5, S6	0.875" Standoff	Y	VOLTREX	SPCS-14	6

Table 8. Common Bill of Materials for Evaluation Boards (continued)



Appendix E SNAU118A–December 2011–Revised February 2018

Balun Information

E.1 Typical Balun Frequency Response

The following figure illustrates the typical frequency response of the Mini-circuit's ADT2-1T balun.



Figure 25. Typical Balun Frequency Response



Appendix F SNAU118A–December 2011–Revised February 2018

Differential Voltage Measurement Terminology

F.1

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically VID or VOD depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is VSS and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. VSS can be measured directly by oscilloscopes with floating references; otherwise this value can be calculated as twice the value of VOD as described in the first section

Figure 26 illustrates the two different definitions side-by-side for inputs and Figure 27 illustrates the two different definitions side-by-side for outputs. The VID and VOD definitions show VA and VB DC levels that the non-inverting and inverting signals toggle between with respect to ground. VSS input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

VID and VOD are often defined in volts (V) and VSS is often defined as volts peak-to-peak (VPP).



Figure 26. Two Different Definitions for Differential Input Signals





GND

Figure 27. Two Different Definitions for Differential Output Signals

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NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

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- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
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